P3)

A)

```
SW   R16, 12(R6)  |  IF  ID  EX  MEM  WB
LW   R16, 8(R6)   |      IF  ID  EX   MEM  WB
BEQ  R5 , R4, Lbl |          IF  ID   EX   MEM  WB
ADD  R5 , R1 , R4 |              IP   ID   EX   MEM  WB
SLT  R5 , R15, R4 |                   IF   ID   EX   MEM  WB
```

I started out with writing out the pipeline with no structural hazard. The IF of the ADD and SLT instructions will line up with the MEM stage of the SW and LW instructions. This is a structural hazard since them will try to access the memory at the same time. The ADD and SLT instructions need to be delayed to eliminate this structural hazard.

The total execution time with the structural hazard removed is 11 cc.

b) If we can assume that the store and load instructions have addresses with no offsets so that the ALU is not needed for those instructions. In this case the first 2 instructions cannot use register R6 since they will both access the same location in memory. The instructions then need to modify so that the load instruction uses a different register than R6. The MEM and Ex stages can overlap to rewrite the stage.

Instruction

```
IF  ID  EX/MEM  WB
    IF  ID      EX/MEM  WB
        IF      ID      EX/MEM  WB
                IF      ID      EX/MEM  WB
                        IF      ID      EX/MEM  WB
```

The above table shows now that it takes 8 cc to complete the given sequence of instructions. Now to calculate the speed up from the last step where it took 9 cc

= Speed up = $9/8 = 1.13$

c) If the branch outcome is determined in the EXE stage then the next instructions must be delayed by 2 cc so that the correct instruction is fetched. It would take 11 cc to complete this instruction sequence. If the branch outcome is determined in the ID stage then the next instruction needs to be delayed by 1 cc which means that only 10 cc

would be required to execute this instruction sequence.

Speed up = 11/10 = 1.1

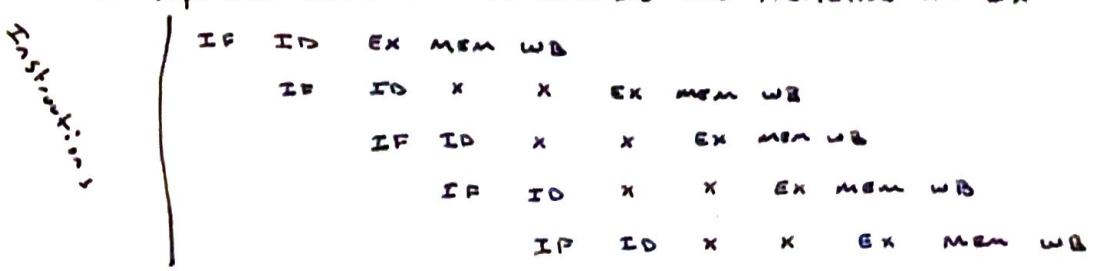
d)

IF	ID	EX	MEM	WB
200	120	150	190	100

The table is given & takes 8cc to complete the given sequence of instructions. The new combined MEM and EX stage has a latency that is longer than the given 5 stage latencies. The latency for the new stage is 210ps and now the latency for this stage is longer than the other latencies. The new cc in this case is 210 ps.

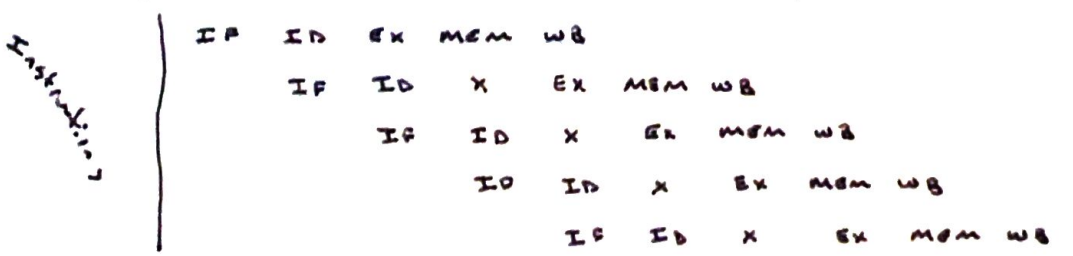
Speed up = $\frac{9(200)}{8(210)}$ = 15/14 = 1.07

e) The Pipeline with stall on branches and Prediction at EX



The number of cc is 11

The Pipeline with stall on branches and predictions at ID stage



The number of cc is 10

Latency of ID is increased by 50% = $120 + \frac{50}{100} \times 120 = 180$ ps

Latency of EX is decreased by 10% = 150 − 10 = 140 ps

The new latencies are:

IF	ID	EX	MEM	WB
200	180	140	190	100

The highest latency is still 200ps and is the new cc time.

Speed up = $\frac{11(200)}{10(200)}$ = 11/10 = 1.1

There is No change in the speed up