(P2)

a) add t_0, $s0$, $s1$ = Adds s_0 and s_1 and is stored in t_0.

=> Add s_0 and s_1

= 1 0101 0000 0000 0000 0000 0000 0000 00000

= 32 bits

= 0101 0000 0000 0000 0000 0000 0000 0000

= 0x50000000

= Overflow has occurred

b) sub t_0, $s0$, $s1$ => $t_0 = s_0 - s_1$

= adding the 2's compliment is the same as subtracting s_1

= $-s_1$ = 0011 0000 0000 0000 0000 0000 0000 00000

= $s_0 - s_1$ = 1011 0000 0000 0000 0000 0000 0000 0000

= t_0 = 1011 0000 0000 0000 0000 0000 0000 0000

= No overflow

c) add $t0, $s0, $s1

add $t0, $t0, $s0 = t_0 = 0101 0000 0000 0000 0000 0000 0000 00000

= Adding $t0 and $s0

=> 1000 0000 0000 0000 0000 0000 0000 0000

\+ 0101 0000 0000 0000 0000 0000 0000 0000

t_0 = 1101 0000 0000 0000 0000 0000 0000 0000

= Overflow has occurred

The actual denial value is

=> 1000 0000 0000 0000 0000 0000 0000 00000

\+ 1 0101 0000 0000 0000 0000 0000 0000 00000

1 1101 0000 0000 0000 0000 0000 0000 00000