CSE 3100 Digital Logic

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Lab 7: Design a Binary Counter using T Flip-Flops that counts 0, 1, 2, 3, 4, 5, 0, ….

State Table:

Present State			Next State			FF Inputs		
Q_2	Q_1	Q_0	Q_2*	Q_1*	Q_0*	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	0	0	1	0	1

K-map for $T_2 = minterms\ (3,\ 5)$

0	0	1	0
0	1	0	0

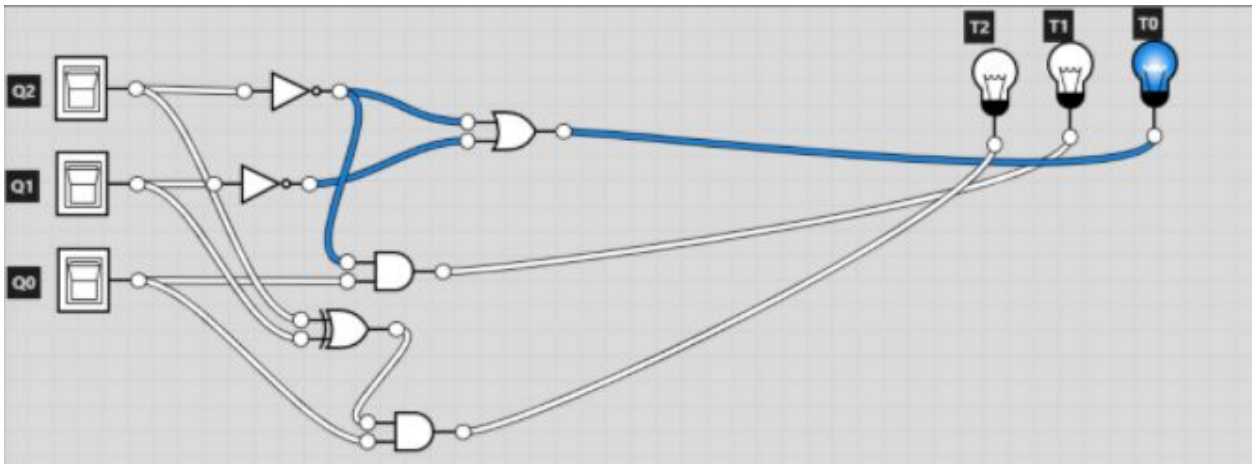
K-map for $T_1 = minterms\ (1, 3)$

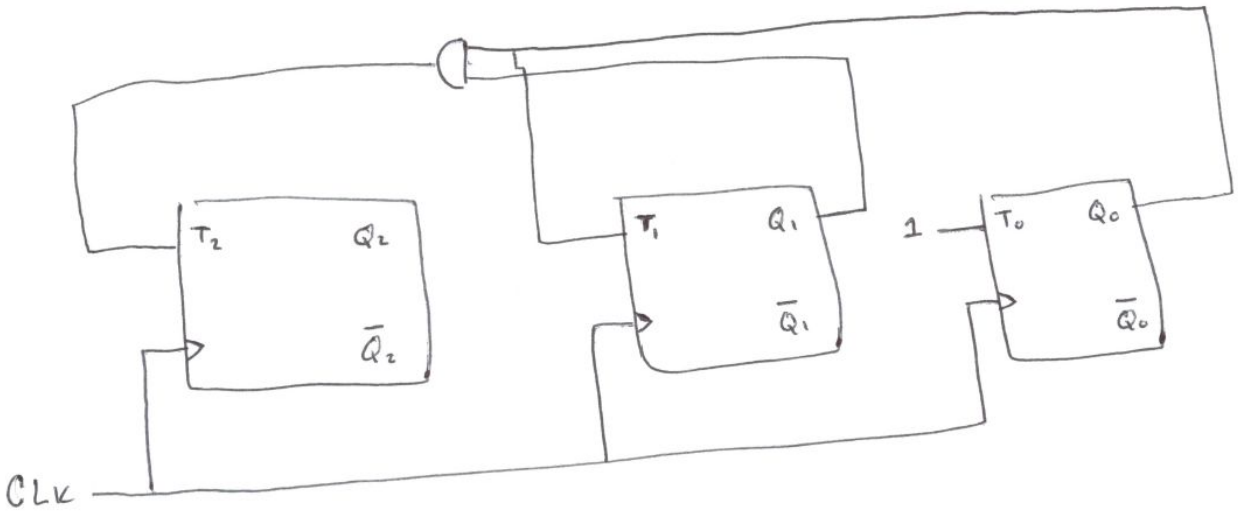
0	1	1	0
0	0	0	0

K-map for $T_0 = minterms\ (0, 1,\ 2,\ 3,\ 4,\ 5)$

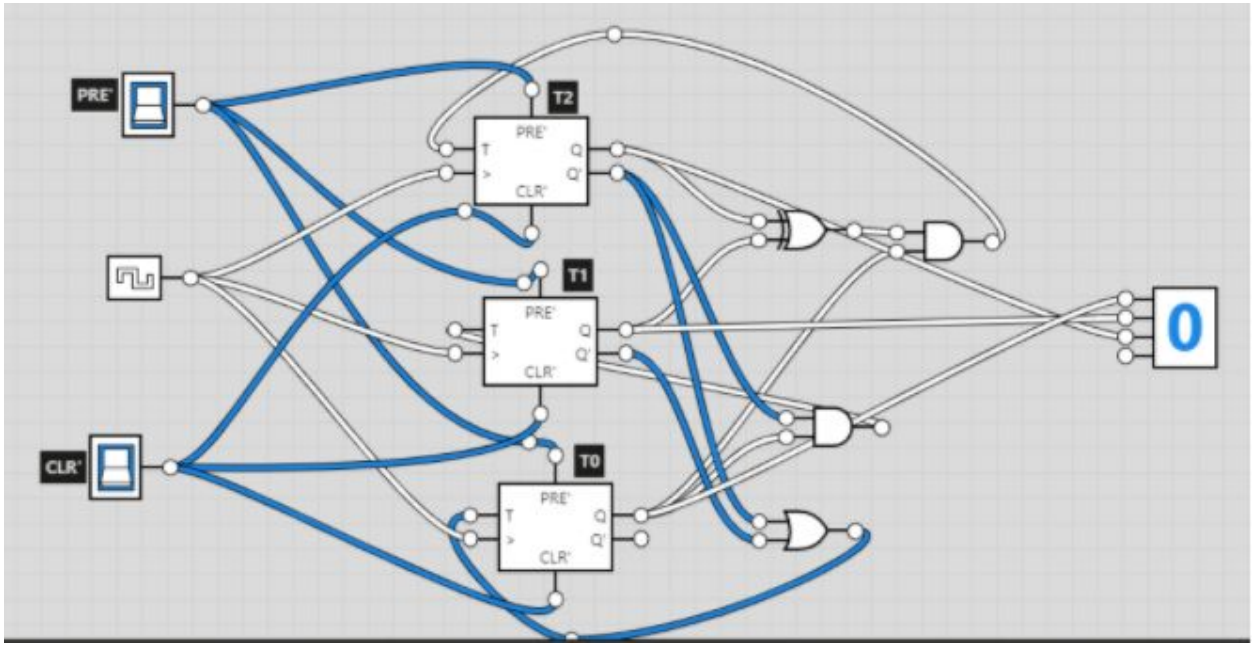
1	1	1	1
1	1	0	0

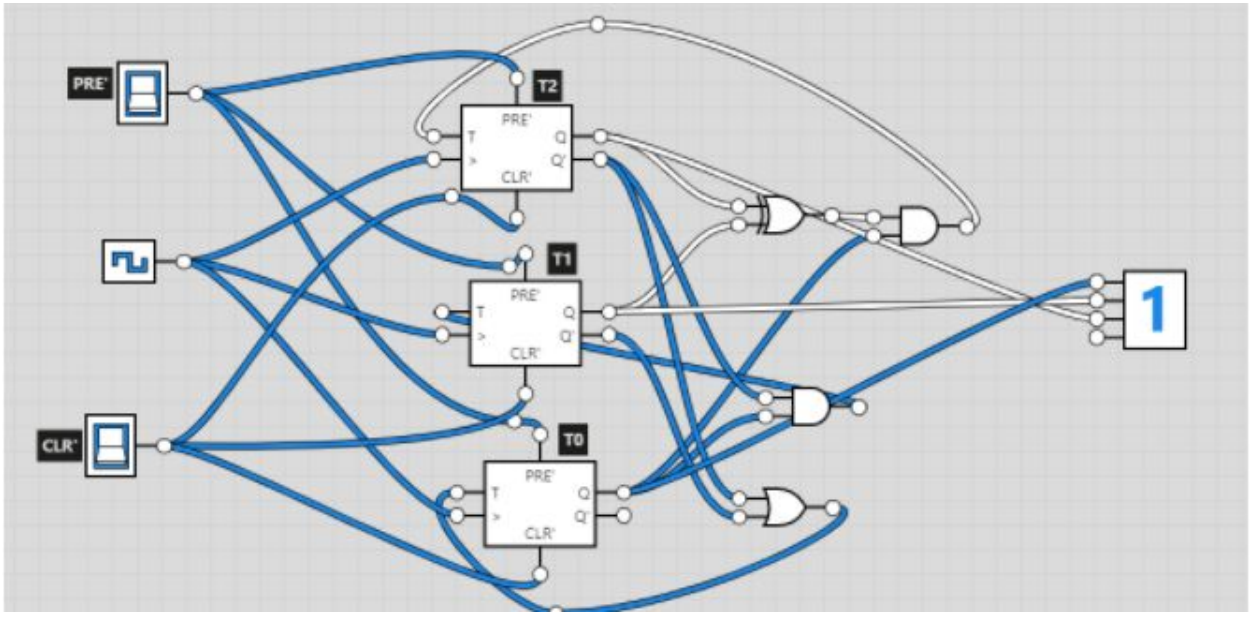
Combinational circuits for T_2 , T_1 , T_0

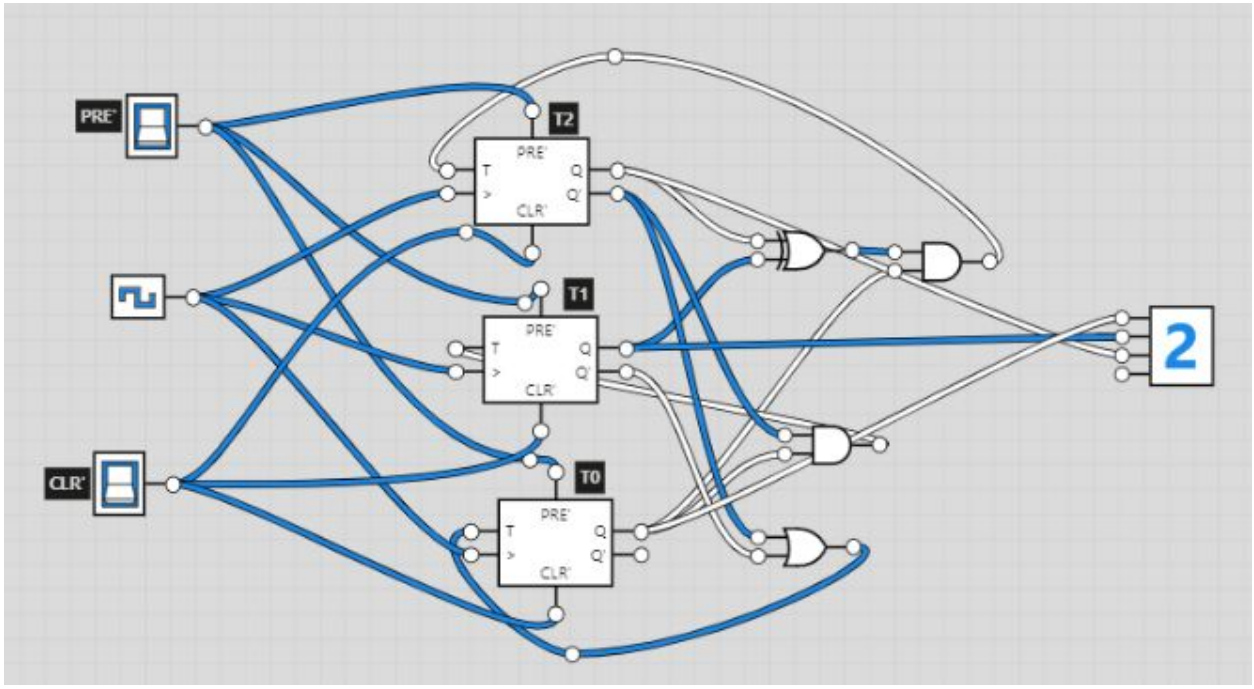


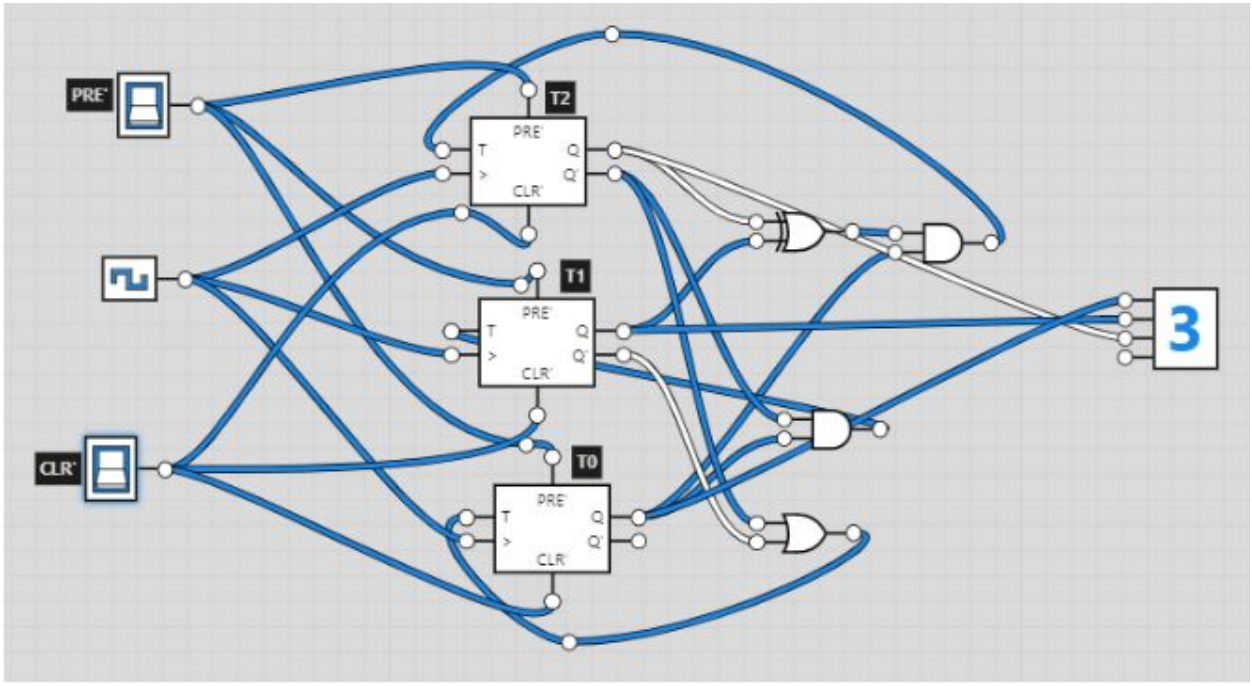


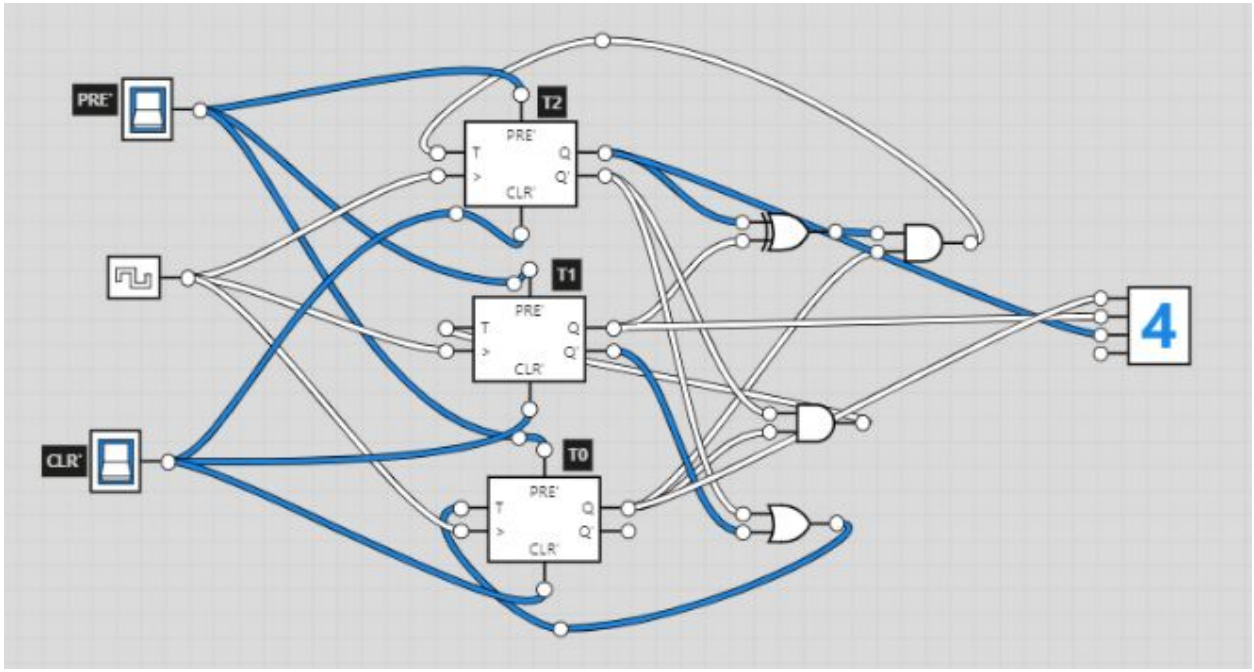
Here is the total circuit diagram of the sequence. I removed the input switches and NOT gates and I connected the circuit.

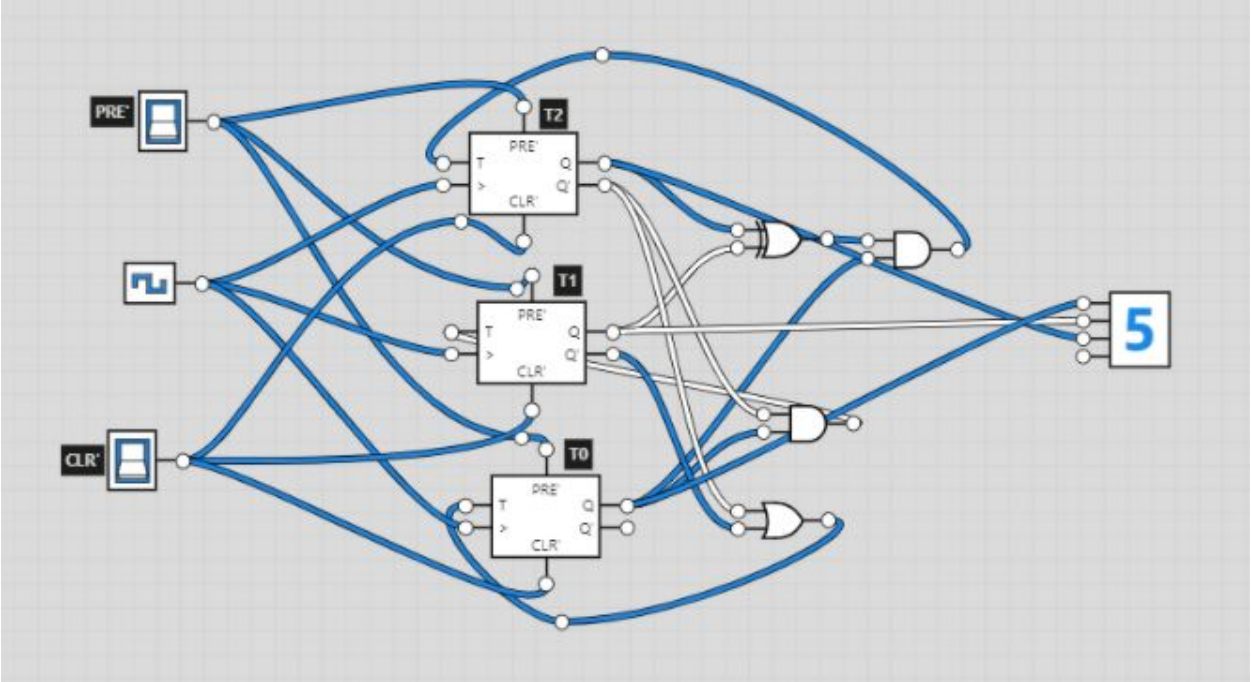



PRE'
CLR'
T2
T1
T0
PRE'
T
>
Q
Q'
CLR'
1


PRE'
CLR'
T2
T1
T0
PRE'
T
>
Q
Q'
CLR'
2


PRE'
CLR'
T2
T1
T0
PRE'
T
>
Q
Q'
CLR'
3


PRE'
CLR'
T2
T1
T0
PRE'
T
>
Q
Q'
CLR'
4



The sequence it is generating is 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, …