California State University, San Bernardino
CSE 3100 – 01, 02 – Digital Logic
SYLLABUS

Fall 2020

Due to Covid-19 the instruction of this class will be conducted strictly online. There will be no face-to-face meeting. Students will do the work individually.

Lectures: Lectures will be asynchronous and will be posted on Blackboard. It is the responsibility of the student to follow the lectures. Lectures and materials will be in different folders on Blackboard.

Labs: Labs make up 25% of the final grade. Labs and lab instructions will be posted on Blackboard.

Office Hours: 9:00 AM - 10:15 AM W, 1:00 PM - 2:15 PM Th and by appointment. All office hours will be conducted via email or Zoom. All Zoom meetings must be initiated by the student via email in advance.

Midterm Exam: Monday, October 12, 9:00 AM – 10:15 AM, Online. No make ups.

Final Exam: Wednesday, December 9, 9:00 AM – 11:00 AM, Online. No make ups.

Disabilities: If you are in need of an accommodation for a disability in order to participate in this class, please contact the instructor and the Services to Students with Disabilities at UH-183, (909) 537-5238. It is the student's responsibility to seek academic accommodations for a verified disability in a timely manner.

Student Learning Outcomes: This course introduces the principles of Digital Logic Design, that is the analysis and synthesis of various building blocks that exist in computers, starting from the abstraction level of binary states (0's and 1's). Specifically the objectives of the course are:

- To know number systems
- To know boolean algebra. Truth tables, canonical and standard forms, logic gates, gate level minimization, Karnaugh Maps
- To design and analyze combinational circuits. The outputs of such circuits are completely defined by their corresponding inputs. Adders, encoders, decoders, multiplexers
- To design and analyze sequential circuits. The outputs of such circuits depend on the internal states, as well as on the inputs. Latches, Flip-flops, registers, ripple counters, counters
- To program, analyze and use programmable components. RAM components, array logic, PLA, PAL, sequential programmable devices

Instructor: Professor Taline Georgiou

Email: tgeorgio@csusb.edu. Please include **CSE 3100** in the subject for filtering purposes.

Catalog Description: Diodes and transistors, Boolean algebra and logic simplification, design and analysis of combinational and sequential circuits, memory elements, counters, introduction to hardware description language and FPGA programming. Three hours lecture and three hours laboratory.

Prerequisites: Semester Prerequisite: CSE 2020 . Quarter Prerequisite: CSE 202 and MATH 272

Learning Management System: blackboard.csusb.edu.

Textbook (Required): *Digital Design* With an introduction to the Verilog HDL,VHDL, and System Verilog; 6th Edition, M. Morris Mano and Michael D. Ciletti, Prentice-Hall, 2017, ISBN: 9780134549897

Grading: Homework 20%, Labs 25%, Midterm 25%, Final 30%

Grade Scale:

A	93 – 100	C	73 – 76
A-	90 – 93	C-	70 – 73
B+	86 – 90	D+	66 – 70
B	83 – 86	D	63 – 66
B-	80 – 83	D-	60 – 63
C+	76 – 80	F	00 – 60

Attendance: It is expected that the student will follow all lectures and materials posted on Blackboard. The student is responsible for all material covered, and also for all announcements made through Blackboard or email.

Homework: Homework, four assignments, is to be done **individually**. It is due at the beginning of the class meeting on the due date. Homework must be neat, optionally typed. Sloppy or illegible homework will be penalized. **Problems must be in the right sequence with all work shown.** Points will be deducted for not following the rules. **Late homework will not be accepted.** Extenuating circumstances will be considered. Documentation may be asked. In such cases, the student must inform the instructor via email as soon as the problem arises or at least 3 days before the due day. **Homework will be uploaded on Blackboard. Students must have a way to scan or take clear pictures of the homework. Preferably the homework should be a single pdf file.**

Grading questions: All questions regarding a grade must be made within 7 calendar days from the day the grade has been posted on Blackboard. After that, the grade will be fixed and will not change.

Academic honesty: According to the CSUSB Catalog of Programs, plagiarism and cheating may result in penalties up to and including expulsion. Students are allowed and encouraged to discuss the material related to assignments, however writing down the solutions must be done individually. Exchanging solutions or parts of solutions is not allowed. When it comes to the attention of a student that possibly dishonest behavior took place, he or she should report it to the instructor. At the very least cheating on an assignment will result in a grade of zero.

University policies: The student is referred to "Academic Regulations and Procedures" in the CSUSB Bulletin of Courses for the university's policies on course withdrawal, cheating, and plagiarism.

Copyright of materials: All materials posted on Blackboard, including videos, slides, etc., are copyright of the Instructor, Publisher, and/or others. They are strictly for the student's educational use in this class, and it is prohibited to be shared with others or used in any other way.

Outline of Course: (Approximate and subject to change)

Week	Topic
1	Chap. 1, *Digital Systems and Binary Numbers,* Sect. 1-1 to 1-9
2, 3	Chap. 2, *Boolean Algebra & Logic Gates,* Sect. 2-1 to 2-9
4, 5	Chap. 3, *Gate-Level Minimization,* Sect. 3-1 to 3-9
6, 7	Chap. 4, *Combinational Logic,* Sect. 4-1 to 4-12
8	**Midterm Exam: Monday, October 12, 9:00 AM – 10:15 AM**, Online. No make ups.
8,9	Chap. 5, *Synchronous Sequential Logic,* Sect. 5-1 to 5-8
10, 11	Chap. 6, *Registers and Counters,* Sect 6-1 to 6-2
12, 13	Chap. 6, Sect. 6-3 to 6-6
14, 15	Chap. 7, *Memory and Programmable Logic,* Sect. 7-1 to 7-8
	Final Exam: Wednesday, December 9, 9:00 AM – 11:00 AM, Online. No make ups.