

Input File Format (Verilog Netlist)

1. The file begins with the “module” keyword followed by the module name and list of primary inputs and primary outputs within parenthesis and separated using ','.
Example: `module sample (N1,N2,N4);`
2. The primary inputs of a circuit are identified using the keyword “input” followed by list of inputs separated using ','.
Example: `input N1,N2;`
3. The primary outputs are designated with keyword “output” and the list of outputs follows.
Example: `output N4;`
4. The wires in the circuit are identified using the “wire” keyword.
Example: `wire N5;`
5. The architecture is then described using the gate types mentioned below.

Gate Types

Two-input, one-output gates or One-input, one-output gates as follows:

- AND2X1
- OR2X1
- NAND2X1
- NOR2X1
- XOR2X1
- INVX1
- BUFX1

6. A Gate definition includes a number of items separated by one or more spaces.

- 2-Input, 1-Output Gate:

Gate_Type Gate_name (.Y(Output_of_Gate),.A(Input_1),.B(Input_2));

Example: *AND2X1 AND_1 (.Y(N5),.A(N1),.B(N2));*

- 1-Input, 1-Output Gate:

Gate_Type Gate_name (.Y(Output_of_Gate),.A(Input_1));

Example: *INVX1 INV_1 (.Y(N4),.A(N5));*

7. All lines end with semicolon.

8. Comments are to be ignored when the file is being processed

//single line comment

/* Multi line

Comment*/

9. The definition of the module ends with the keyword “endmodule”.

Sample input file: mycircuit.v

```
module sample (N1,N2,N4);  
  
input N1,N2;  
output N4;  
wire N5;  
  
//Gates in the module  
AND2X1 AND_1 (.Y(N5),.A(N1),.B(N2));  
INVX1 INV_1 (.Y(N4),.A(N5));  
endmodule
```

This is the information regarding how the input netlist should look like that. As long as the netlist is in the given format, we will get the results. The logic gates can be from any of the six gates mentioned above.

RESULTS:

The results for given netlist in “source.txt” and inputs in “inputvector.txt” is shown below.

```
IPython console
Console 1/A

In [79]: runfile('J:/design_lab/compilecode8.py', wdir='J:/design_lab')
The input list of the circuit is ['N1', 'N2', 'N6', 'N7']

The level of this circuit is
3
For input vector of 1011 The values of all variables are
{'N1': '1', 'N2': '0', 'N6': '1', 'N7': '1', 'N5': '0', 'N8': '1', 'N4': '1', 'N9': '1'}

For input vector of 1100 The values of all variables are
{'N1': '1', 'N2': '1', 'N6': '0', 'N7': '0', 'N5': '1', 'N8': '0', 'N4': '0', 'N9': '0'}

For input vector of 0111 The values of all variables are
{'N1': '0', 'N2': '1', 'N6': '1', 'N7': '1', 'N5': '0', 'N8': '1', 'N4': '1', 'N9': '1'}

In [80]:
```

The circuit can be simulated for any number of gates. The circuit can be modified by changing the “source.txt” and inputs can be changed by changing “inputvector.txt”.