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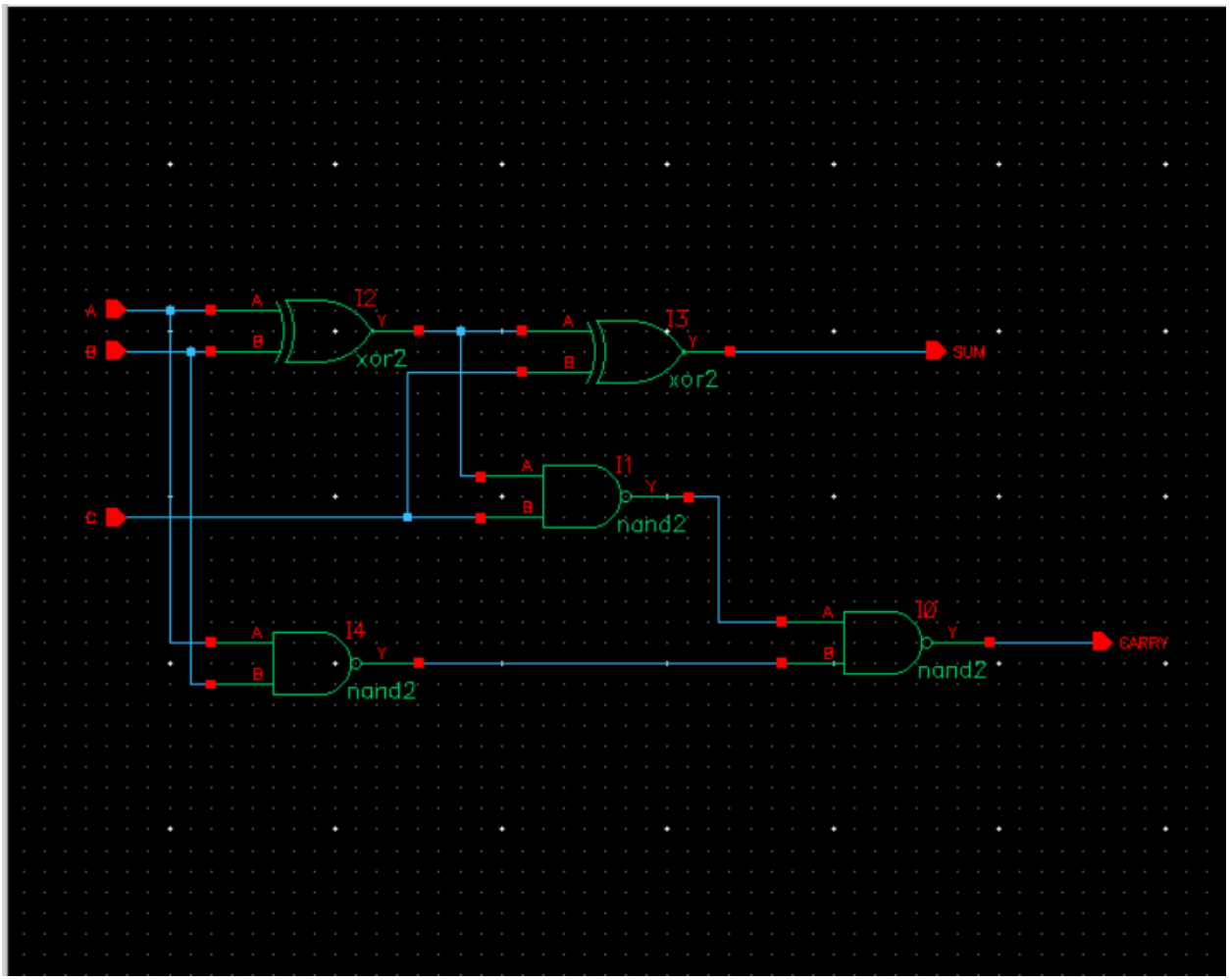
ECEN 454 Section 510

Lab date: 5 September 2024

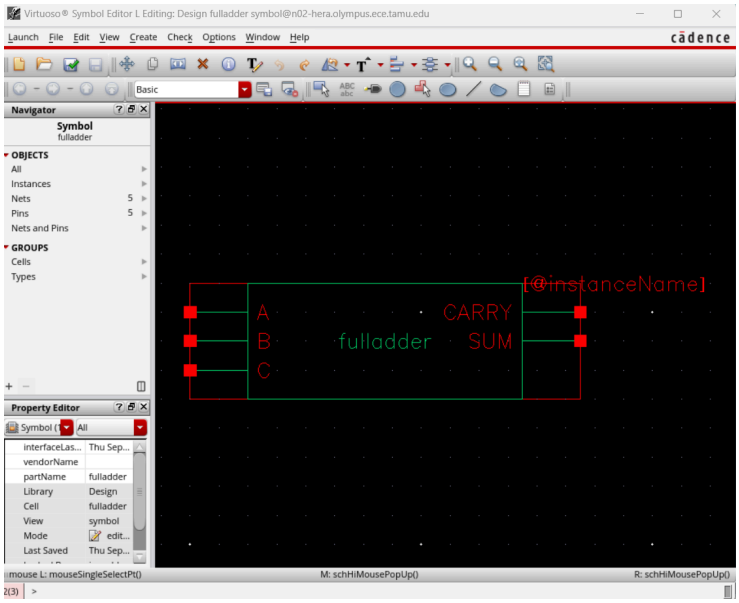
Due date: 14 September 2024

Lab 1: Introduction to Cadence Schematic Design & Simulation

1-bit Full Adder Schematic:



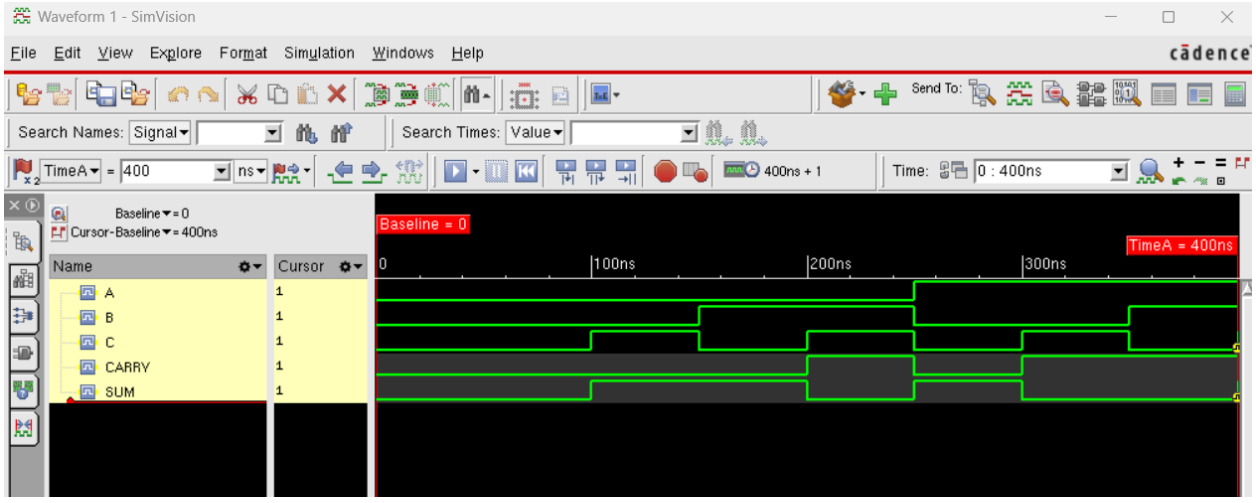
1-bit Full Adder Symbol:



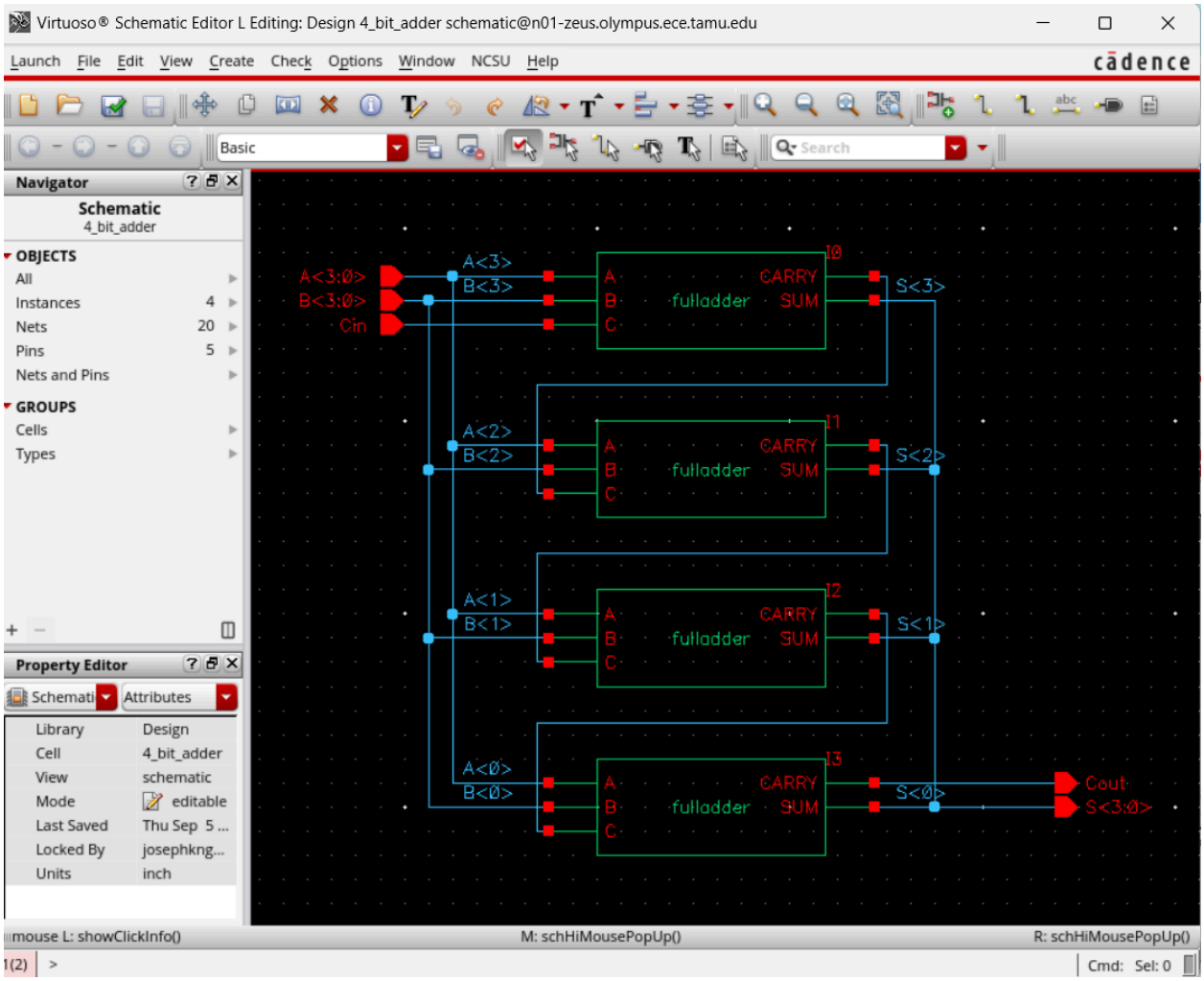
1-bit Full Adder Verilog:

```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.

initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);


initial
begin

   A = 1'b0;
   B = 1'b0;
   C = 1'b0;

#50 A=1'b0; B=1'b0; C=1'b1;             //ABC=001
#50 A=1'b0; B=1'b1; C=1'b0;             //ABC=010
#50 A=1'b0; B=1'b1; C=1'b1;             //ABC=011
#50 A=1'b1; B=1'b0; C=1'b0;             //ABC=100
#50 A=1'b1; B=1'b0; C=1'b1;             //ABC=101
#50 A=1'b1; B=1'b1; C=1'b0;             //ABC=110
#50 A=1'b1; B=1'b1; C=1'b1;             //ABC=111
end
```

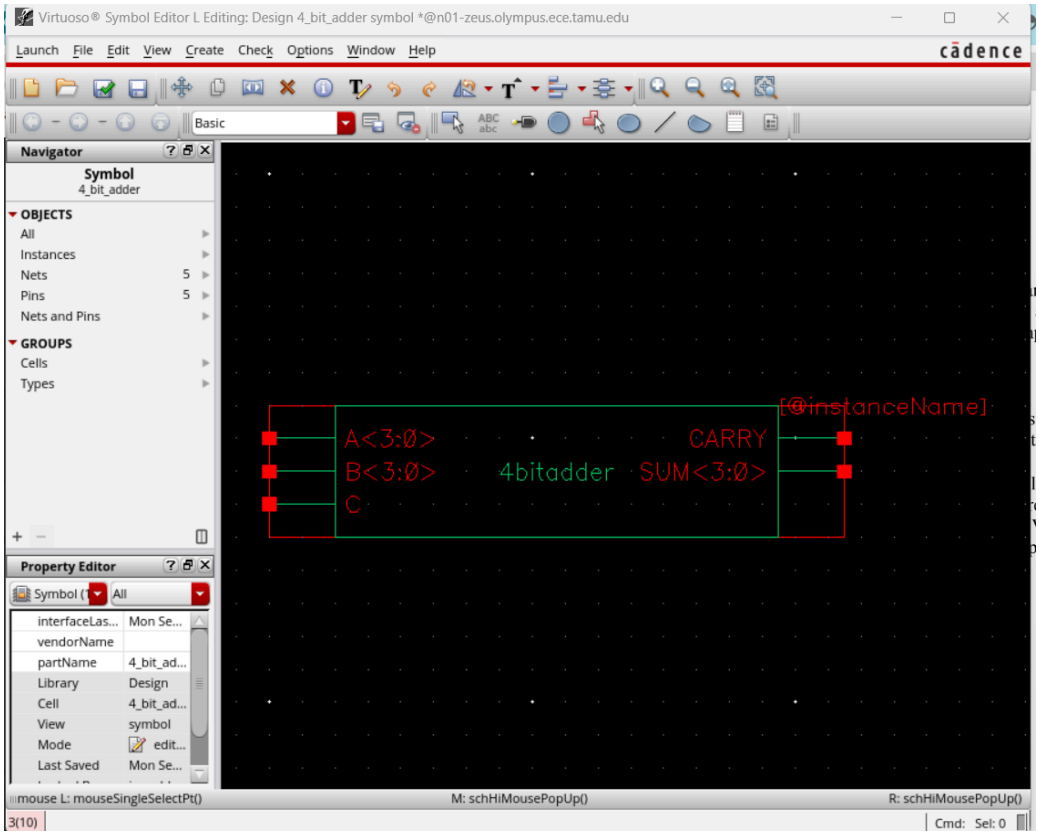
1-bit Full Adder Simulation Waveform:



4-bit Adder Schematic:



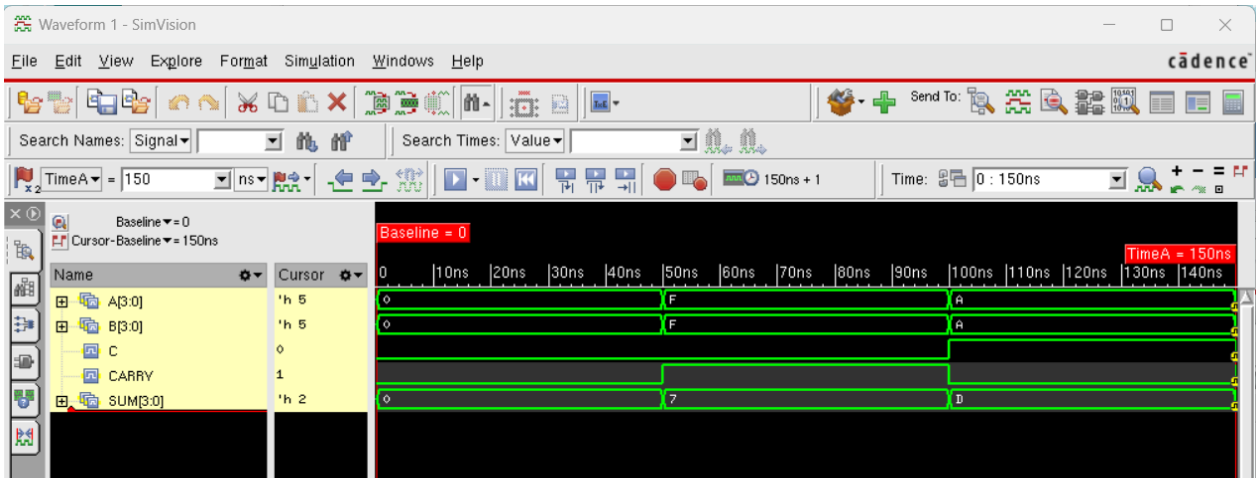
4-bit Adder Symbol:



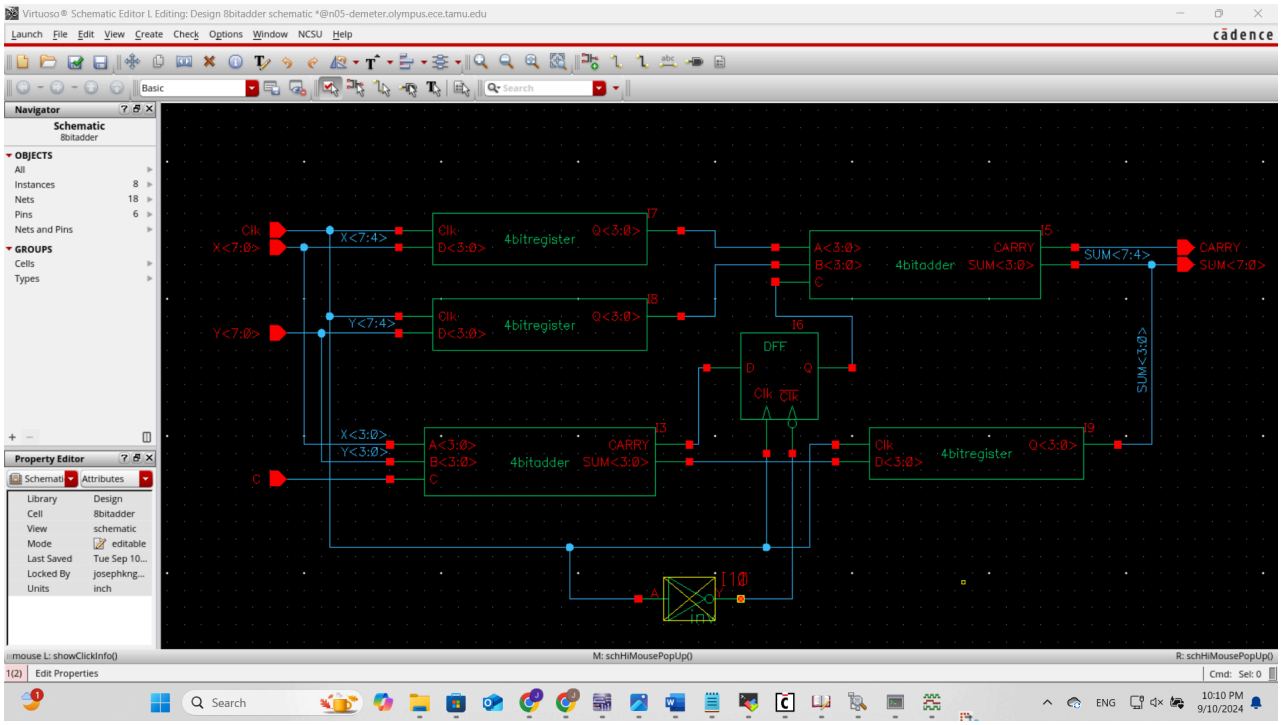
4-bit Adder Verilog:

```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.
initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);

initial
begin

   A[3:0] = 4'b0000;

   B[3:0] = 4'b0000;

   C = 1'b0;

#50 A=4'b1111; B=4'b1111; C=1'b0;              //ABC=111111110
#50 A=4'b1010; B=4'b1010; C=1'b1;              //ABC=101010101
#50 A=4'b0101; B=4'b0101; C=1'b0;              //ABC=010101010
end

initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);
initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);
initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);
```

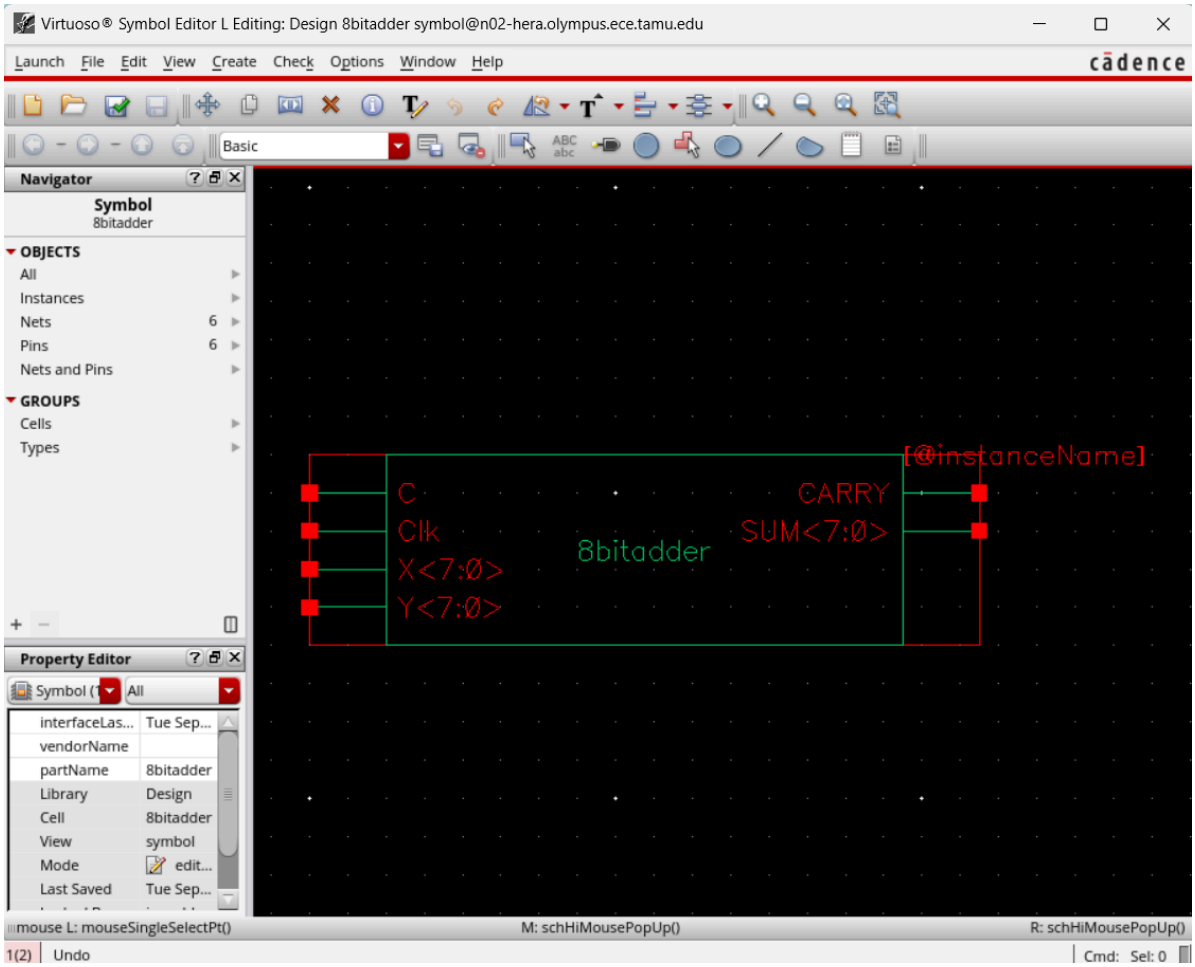
4-bit Adder Simulation Waveform:



8-bit Adder Schematic:



8-bit Adder Symbol:



8-bit Adder Verilog:

```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.

initial
begin

   C = 1'b0;
   Clk = 1'b0;
   X[7:0] = 8'b00000000;

   Y[7:0] = 8'b00000000;

#50 Clk=1'b1; X=8'b01111110; Y=8'b11100111; C=1'b0;
#50 Clk=1'b1; X=8'b11111111; Y=8'b00000000; C=1'b1;
#50 Clk=1'b1; X=8'b10101010; Y=8'b01010101; C=1'b0;
#50 Clk=1'b1; X=8'b10101010; Y=8'b01010101; C=1'b1;
#50 Clk=1'b1; X=8'b11001100; Y=8'b00110011; C=1'b0;
#50 Clk=1'b1; X=8'b11001100; Y=8'b00110011; C=1'b1;
end

initial
$monitor ($time," X=%b, Y=%b, C=%b, SUM=%b, CARRY=%b", X, Y, C, SUM, CARRY);
initial
$monitor ($time," X=%b, Y=%b, C=%b, SUM=%b, CARRY=%b", X, Y, C, SUM, CARRY);
initial
$monitor ($time," X=%b, Y=%b, C=%b, SUM=%b, CARRY=%b", X, Y, C, SUM, CARRY);
initial
$monitor ($time," X=%b, Y=%b, C=%b, SUM=%b, CARRY=%b", X, Y, C, SUM, CARRY);
initial
$monitor ($time," X=%b, Y=%b, C=%b, SUM=%b, CARRY=%b", X, Y, C, SUM, CARRY);
initial
$monitor ($time," X=%b, Y=%b, C=%b, SUM=%b, CARRY=%b", X, Y, C, SUM, CARRY);
```

8-bit Adder Simulation Waveform: