Joseph Nguyen

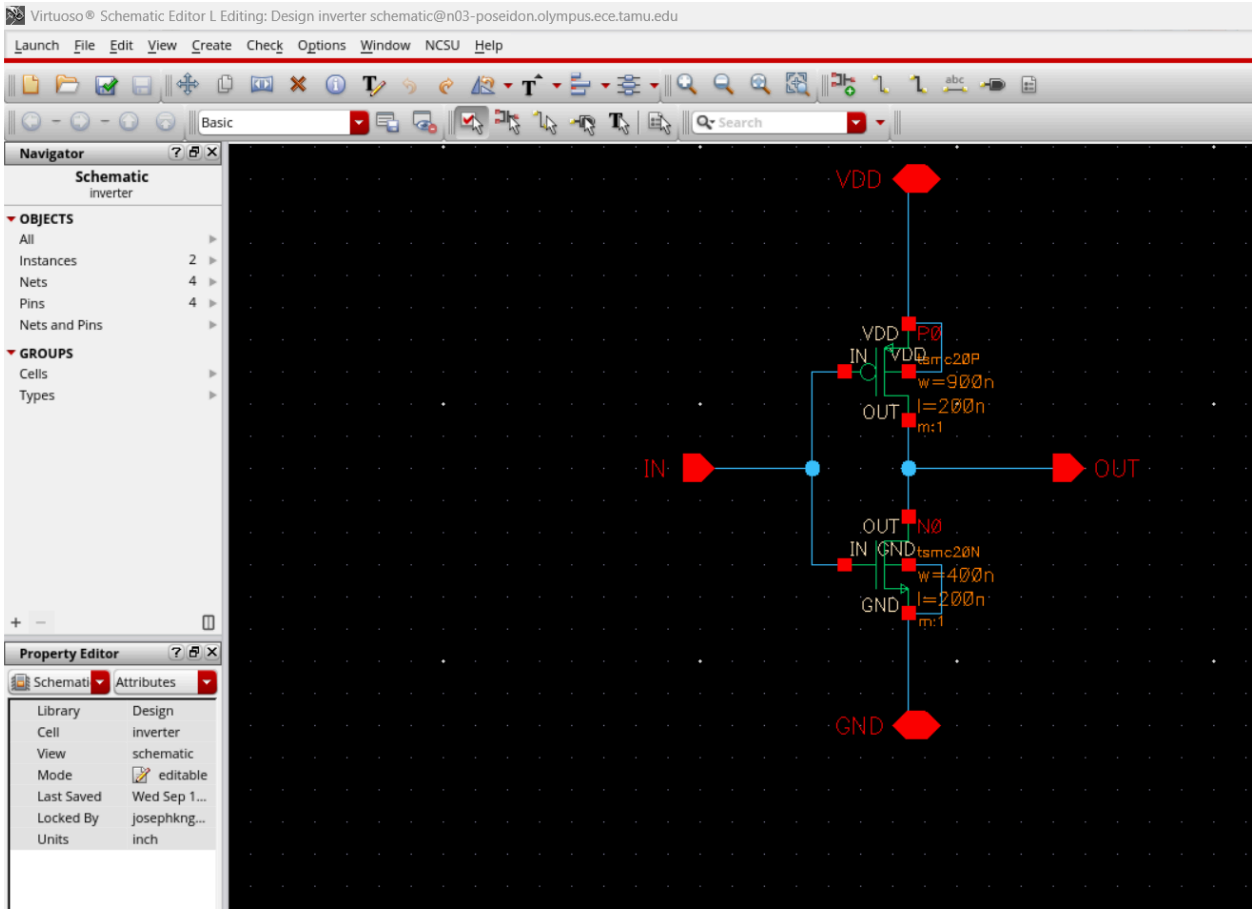
ECEN 454 Section 510

Lab date: 12 September 2024

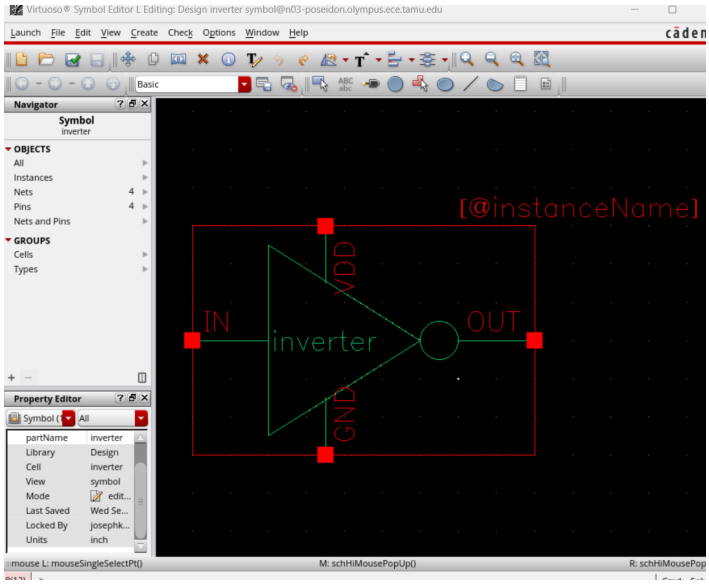
Due date: 18 September 2024

Lab 2: Cadence Custom layout: Design Rules, Extraction, and Verification

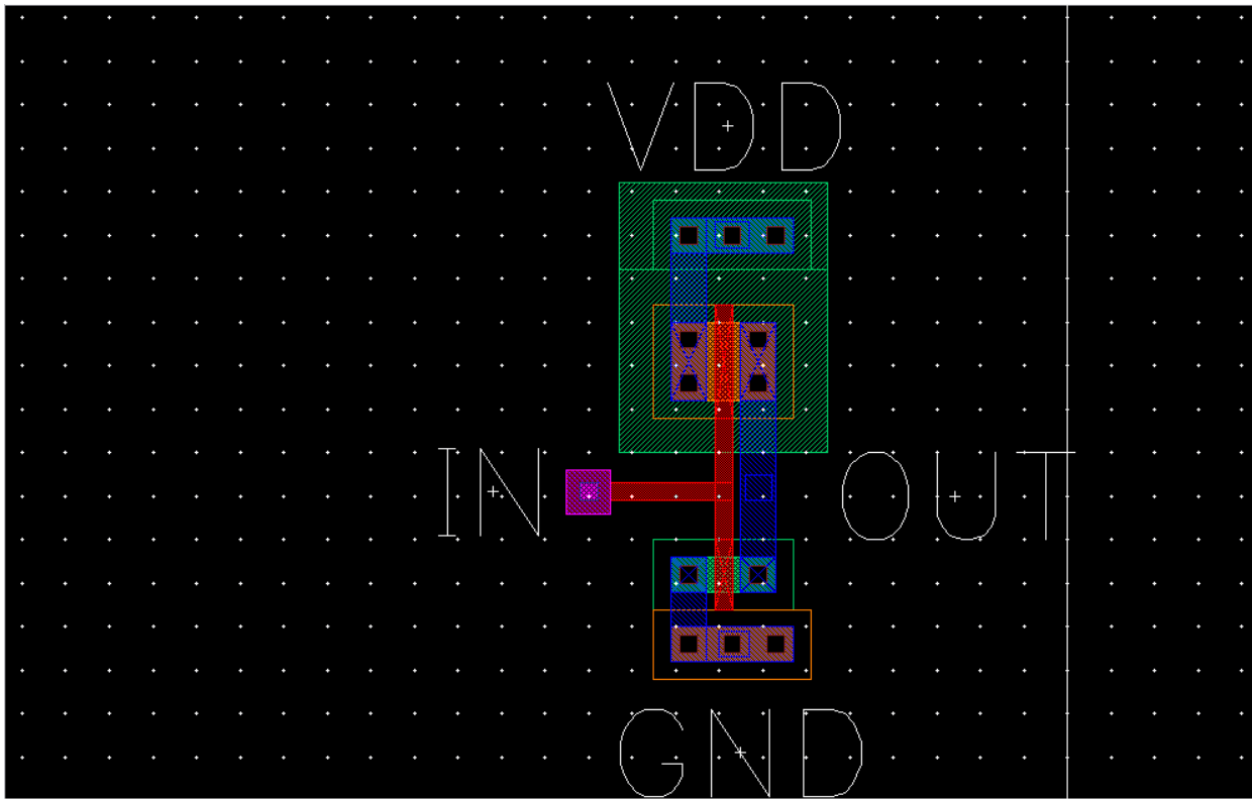
Inverter Schematic



Inverter Symbol:



Inverter layout:



Inverter LVS:

```
    Terminal correspondence points
    N0          N2          GND
    N2          N0          IN
    N1          N1          OUT
    N3          N3          VDD

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   2       2
        total                    2       2

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   4       4
        total                    4       4

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    4       4


Probe files from /home/ugrads/j/josephknguyen02/ecen454_714/LVS/schematic
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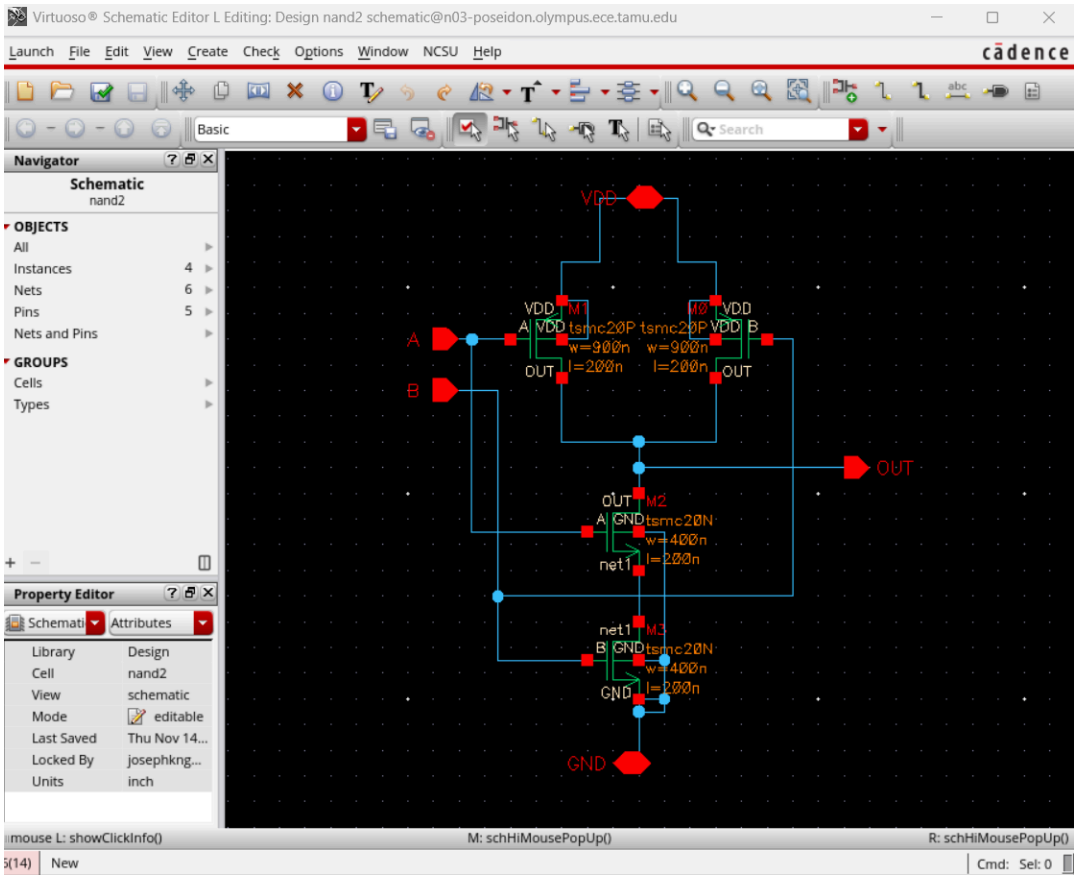
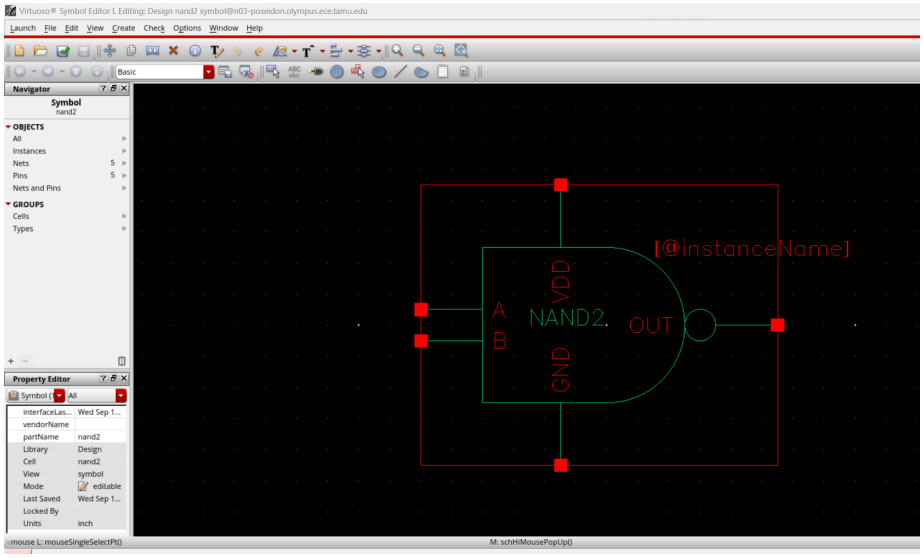
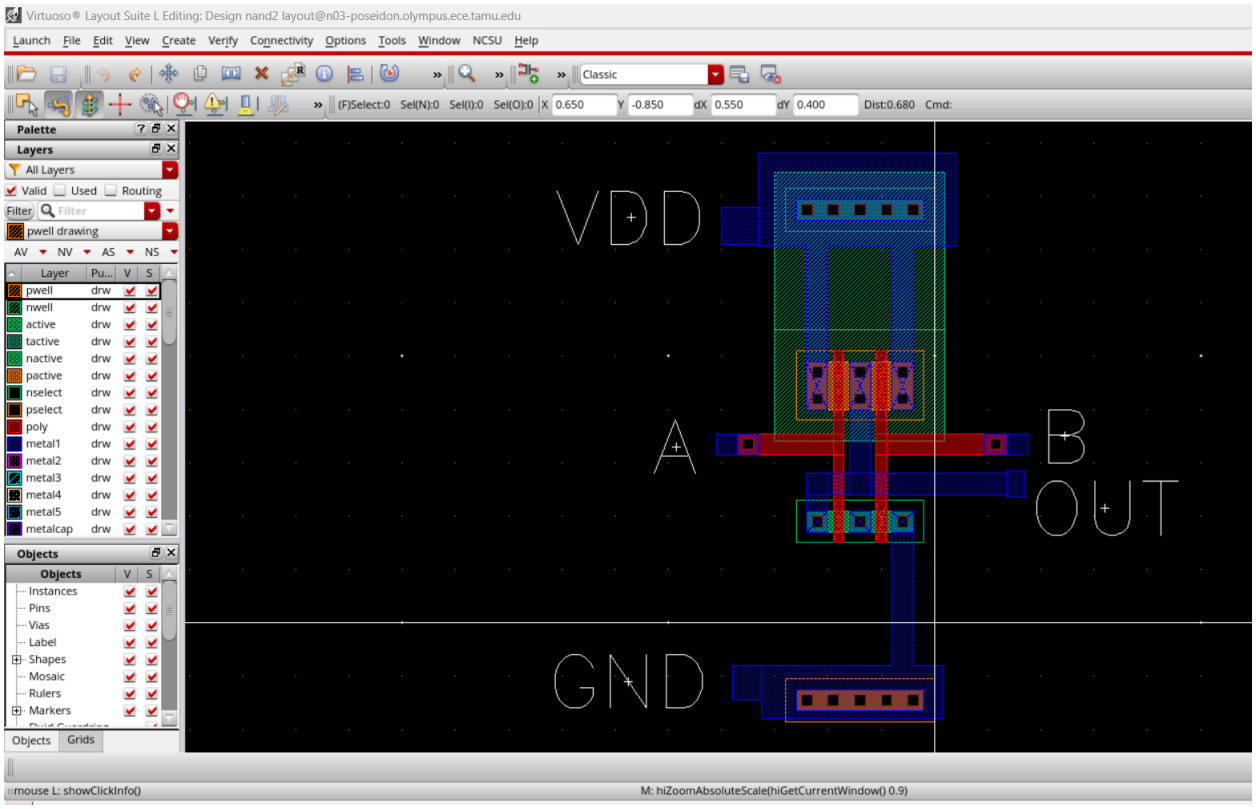
Nand2 schematic:



Nand2 symbol:



Nand2 layout:



Nand2 LVS:

```
    Terminal correspondence points
    N4          N2          A
    N3          N3          B
    N1          N1          GND
    N2          N4          OUT
    N5          N0          VDD

Devices in the netlist but not in the rules:
        pcapacitor pmos nmos

The net-lists match.

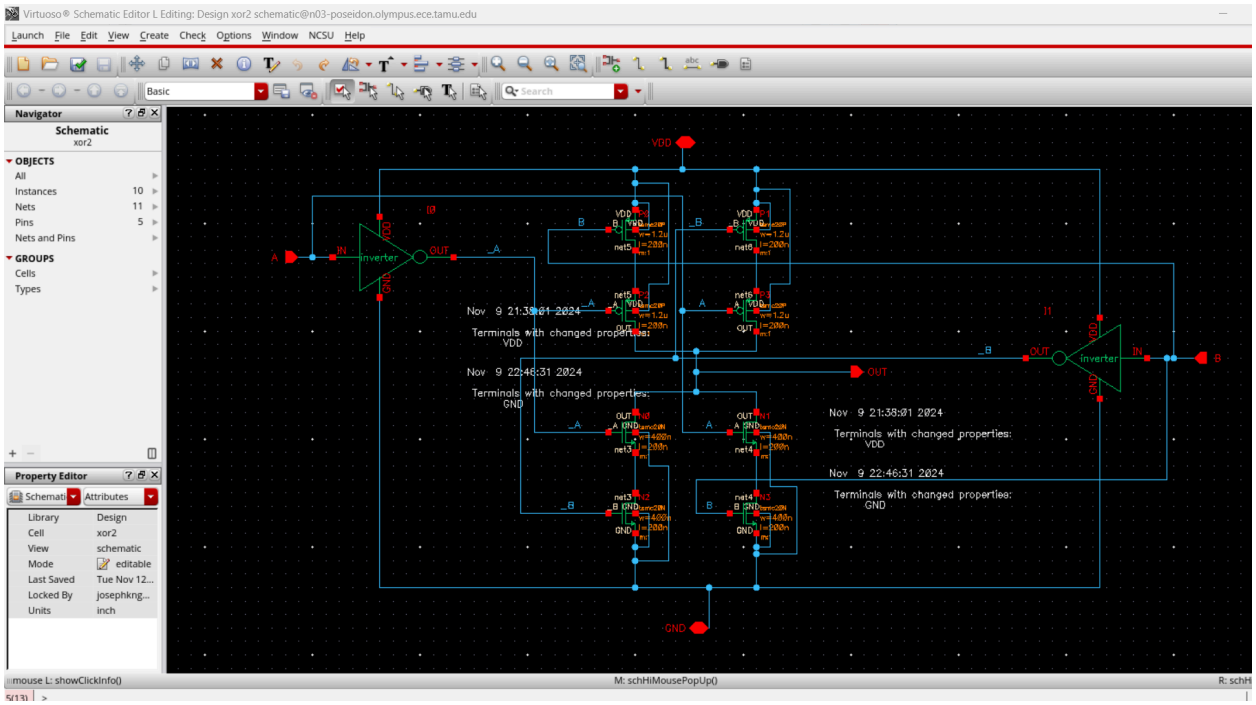
                              layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  6       6
        total                   6       6

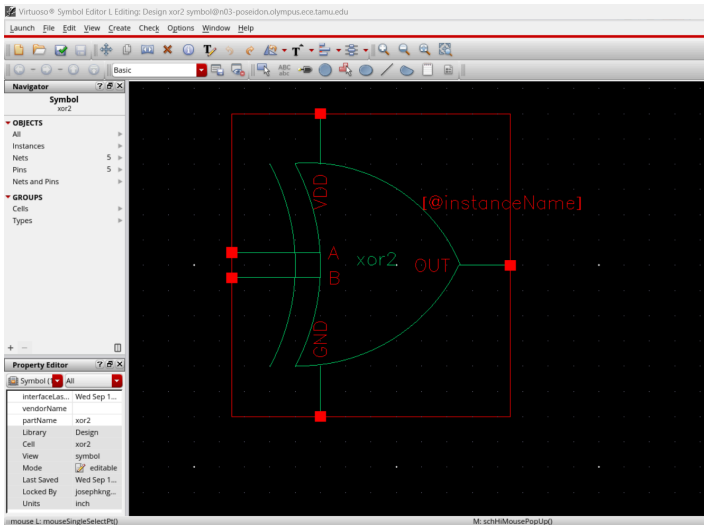
                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   5       5


Probe files from /home/ugrads/j/josephknguyen02/ecen454_714/LVS/schematic
```

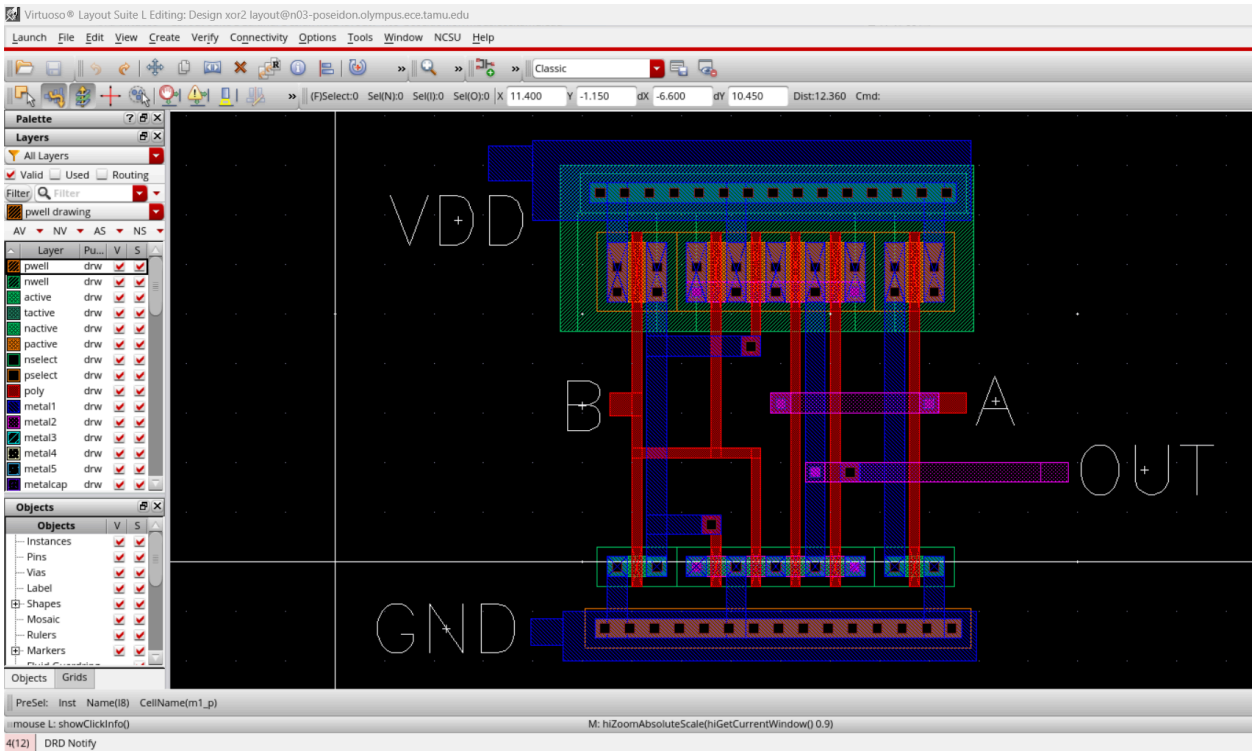
Xor2 schematic:



Xor2 symbol:



Xor2 layout:



Xor2 LVS:

/home/ugrads/j/josephknguyen02/ecen454_714/LVS/si.out@n03-poseidon.olympus.ece.tamu.ed

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```
    N9          N0          A
    N8          N1          B
    N6          N4          GND
    N7          N2          OUT
    N10         N3          VDD

Devices in the netlist but not in the rules:
        pcapacitor pmos nmos

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   12      12
        total                    12      12

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   11      11
        total                    11      11

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    5       5


Probe files from /home/ugrads/j/josephknguyen02/ecen454_714/LVS/schematic

devbad.out:

netbad.out:
```