Joseph Nguyen

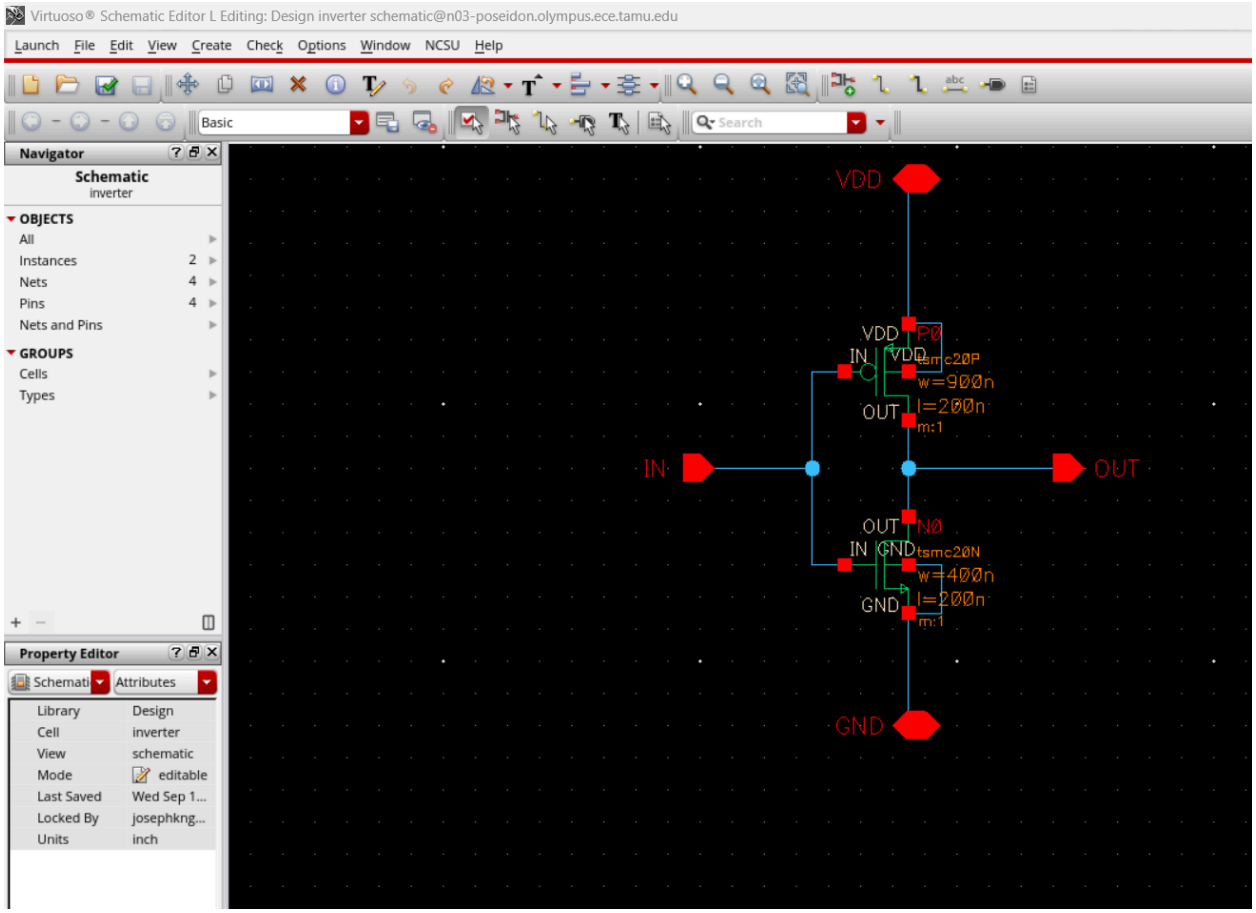
ECEN 454 Section 510

Lab date: 12 September 2024

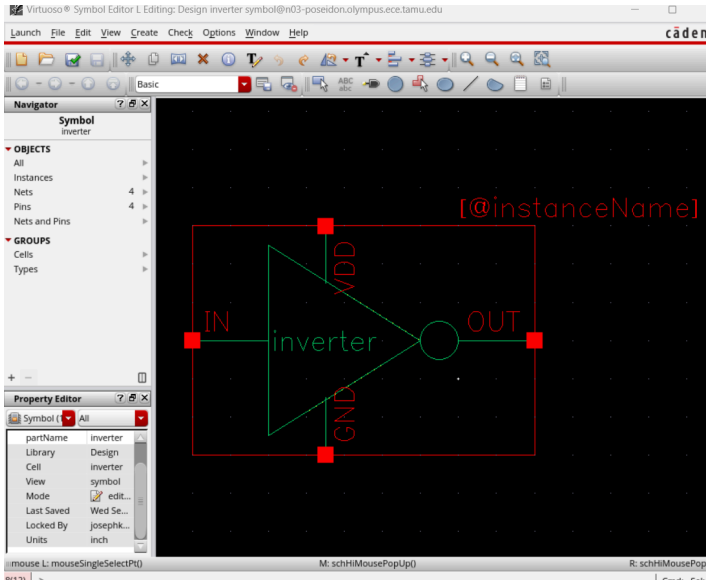
Due date: 18 September 2024

Lab 2: Cadence Custom layout: Design Rules, Extraction, and Verification

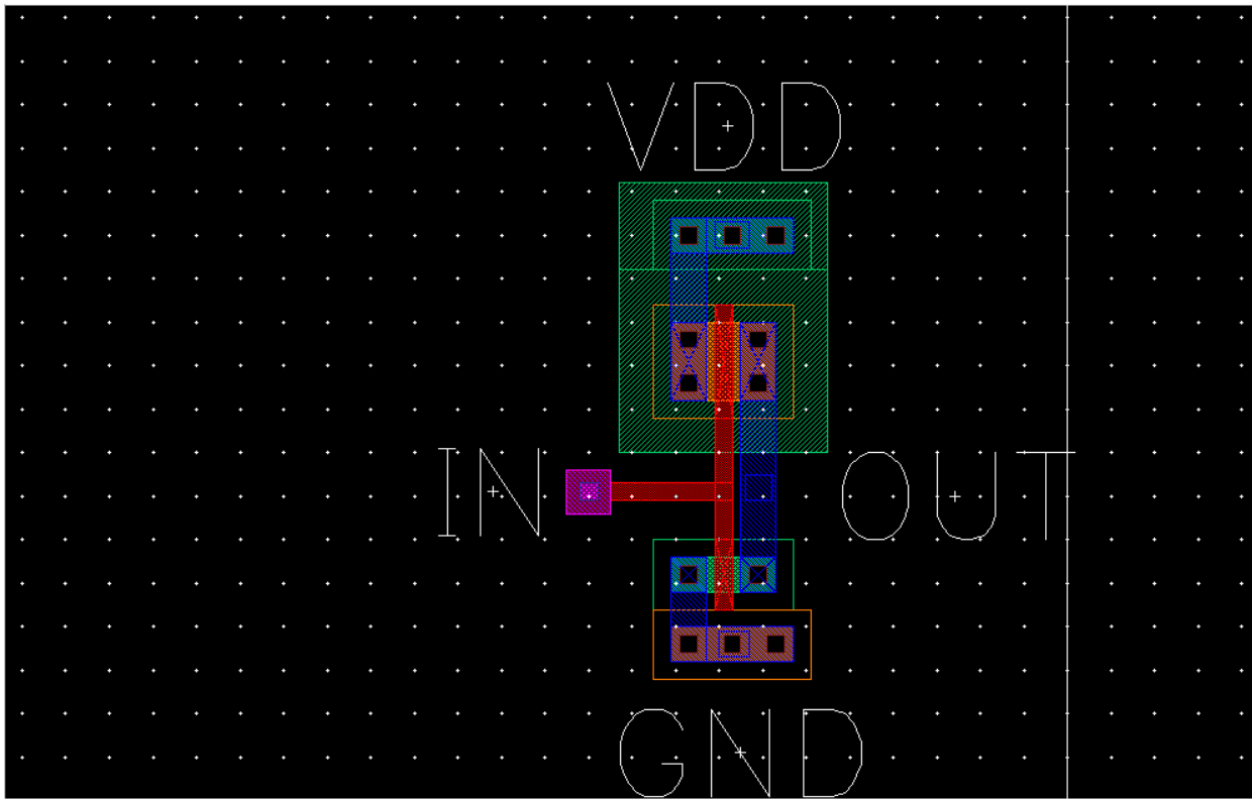
Inverter Schematic



Inverter Symbol:



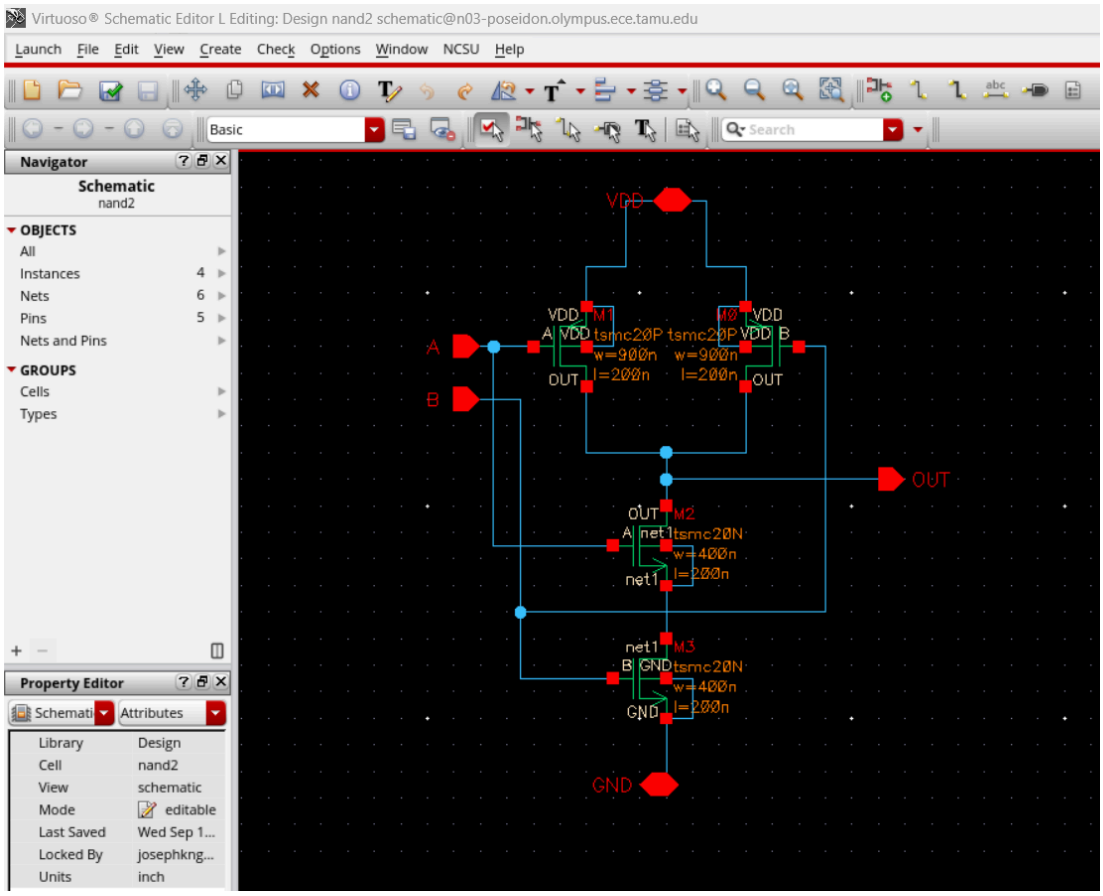
Inverter layout:



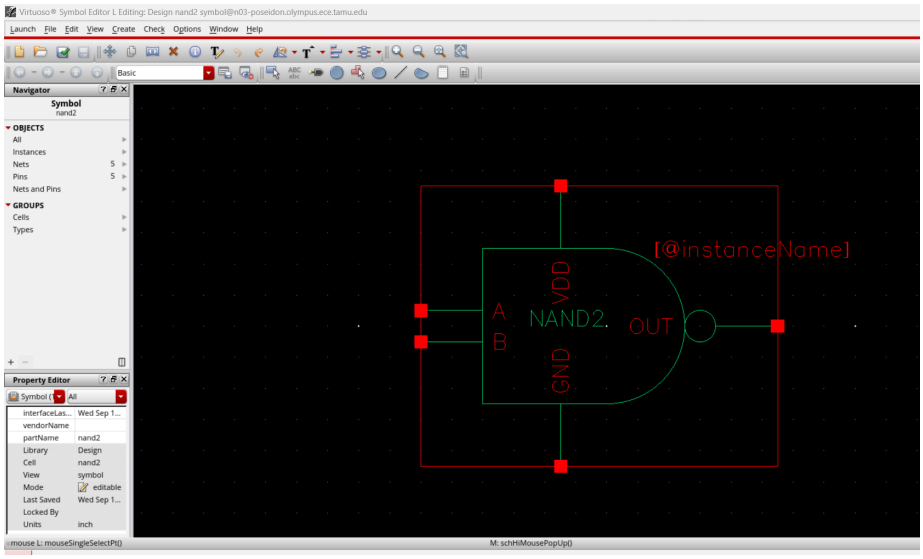
Inverter LVS:

```
    Terminal correspondence points
    N0          N2          GND
    N2          N0          IN
    N1          N1          OUT
    N3          N3          VDD

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   2       2
        total                    2       2

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   4       4
        total                    4       4

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    4       4


Probe files from /home/ugrads/j/josephknguyen02/ecen454_714/LVS/schematic
```

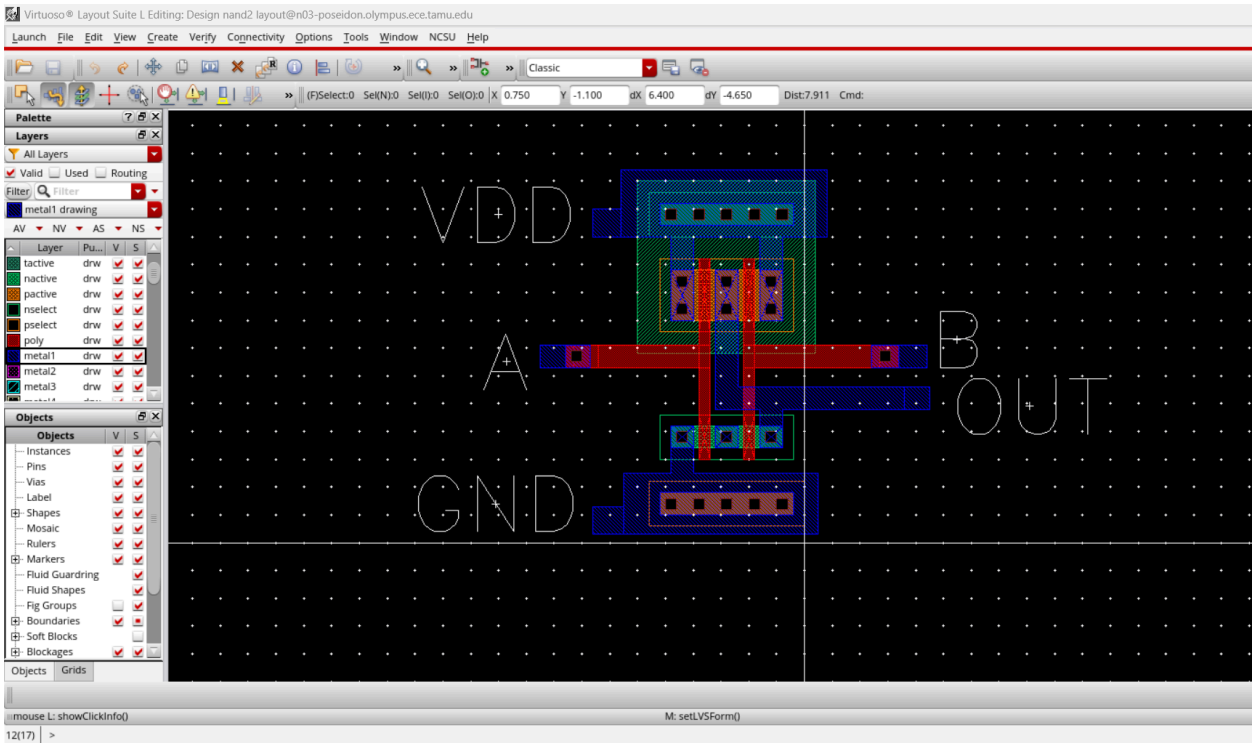
Nand2 schematic:



Nand2 symbol:



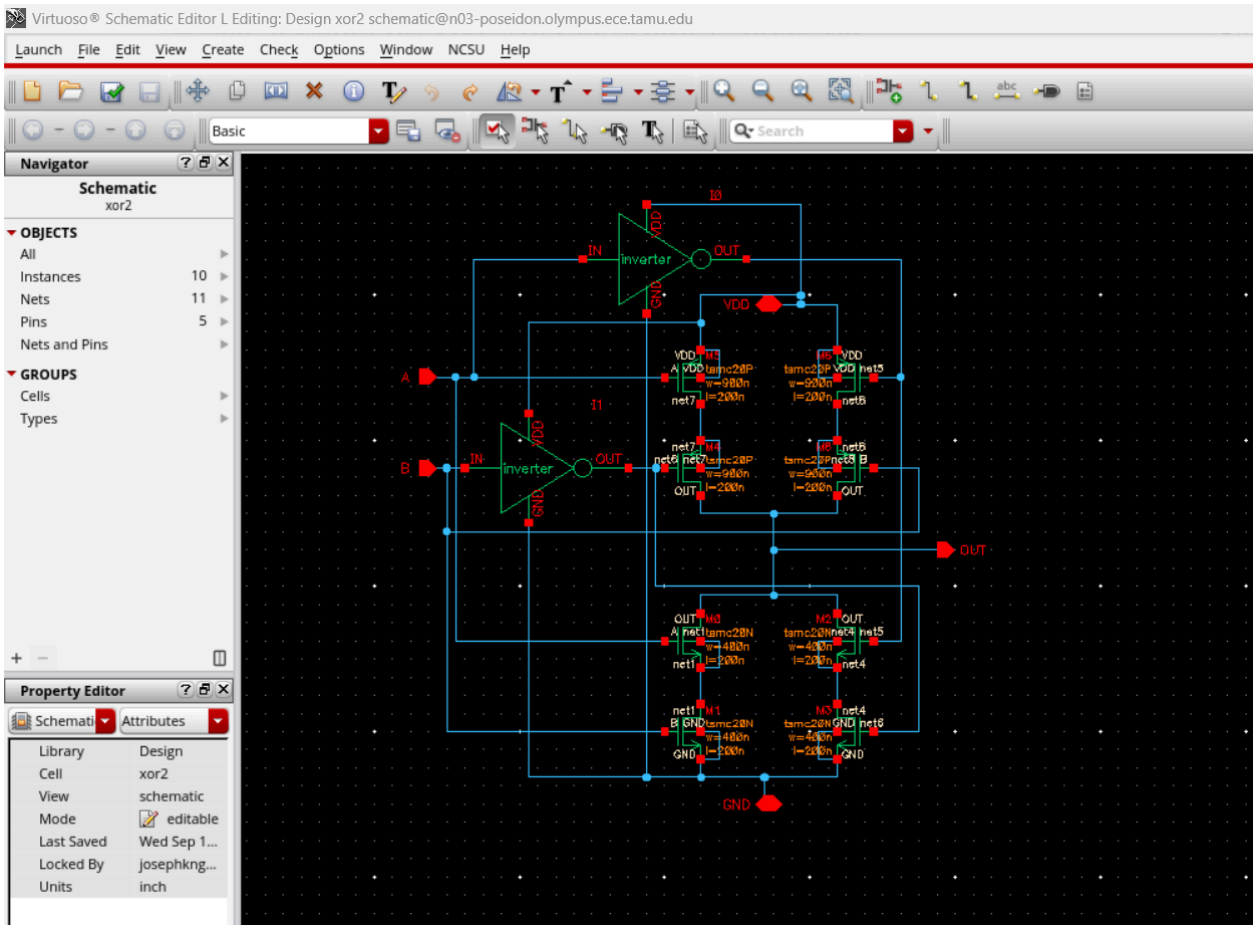
Nand2 layout:



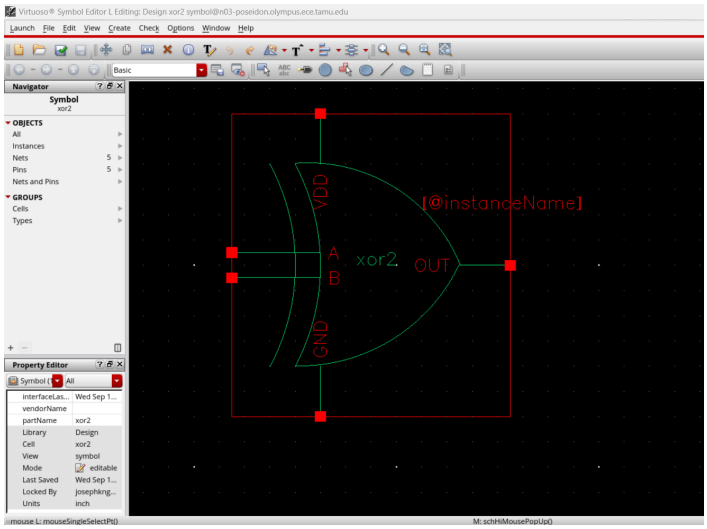
Nand2 LVS:

```
    Terminal correspondence points
    N0          N2          GND
    N2          N0          IN
    N1          N1          OUT
    N3          N3          VDD

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    2       2
        total                     2       2

                                  nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    4       4
        total                     4       4

                                terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     4       4


Probe files from /home/ugrads/j/josephknguyen02/ecen454_714/LVS/schematic
```

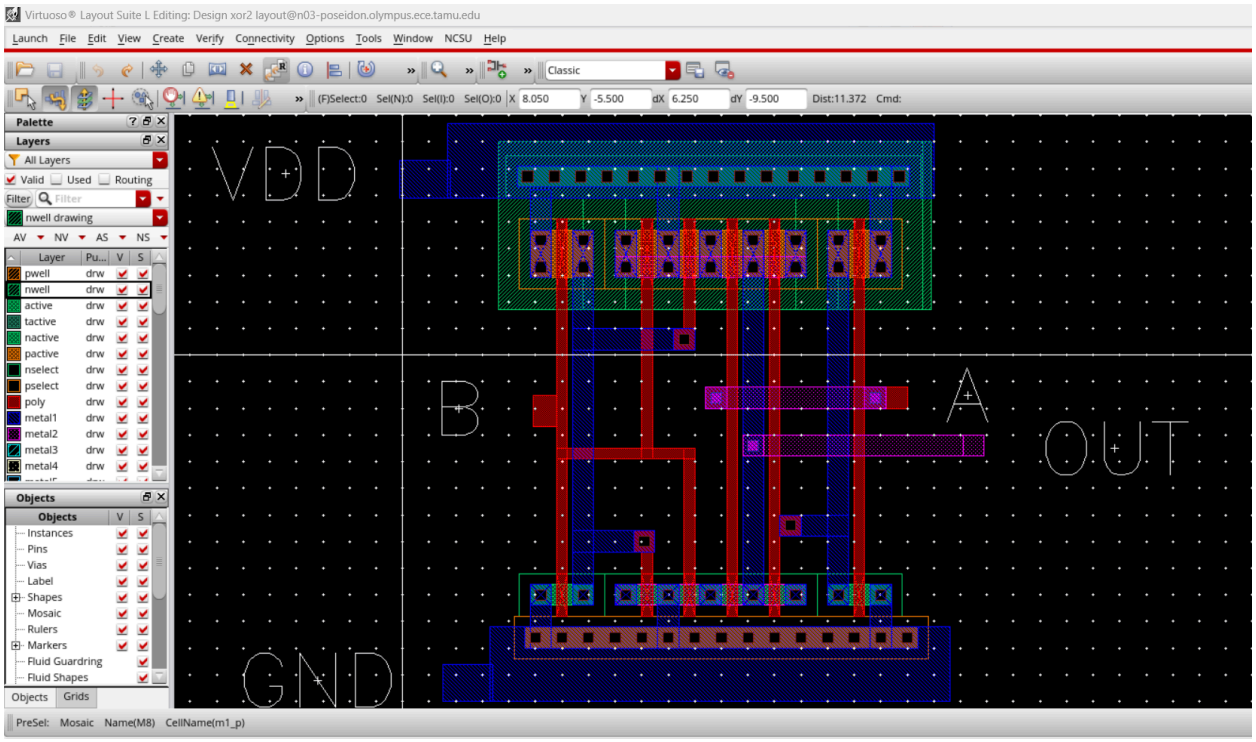
Xor2 schematic:



Xor2 symbol:



Xor2 layout:



Xor2 LVS:

```
    Terminal correspondence points
    N0          N2          GND
    N2          N0          IN
    N1          N1          OUT
    N3          N3          VDD

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    2       2
        total                     2       2

                                   nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    4       4
        total                     4       4

                                 terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     4       4


Probe files from /home/ugrads/j/josephknguyen02/ecen454_714/LVS/schematic
```