Joseph Nguyen

Troy Buhr

ECEN 325 Section 510

Lab date: 25 April 2024

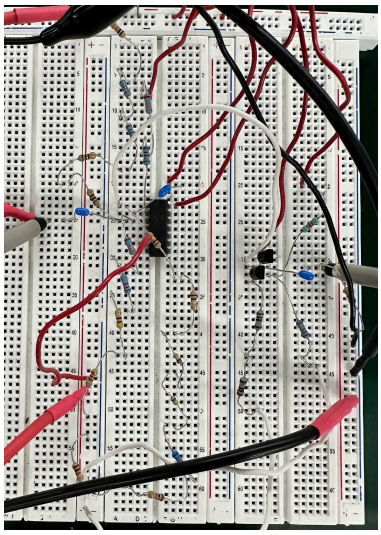
Due date: 30 April 2024

Lab 12: MOSFET Amplifier Design

Procedure:

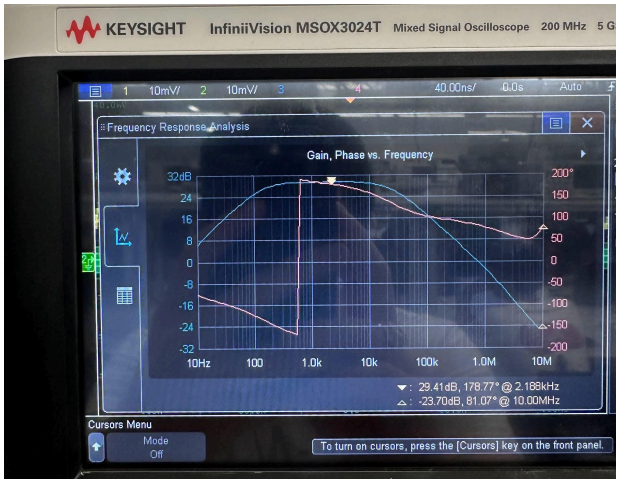
For the lab procedure, I started by building the two-stage amplifier circuit with the current source implementation. I then measured the DC operating point for the circuit and recorded all node voltages and branch currents. After verifying the recorded values, I measured the gain and input resistance of the circuit. Next, I applied a 5 kHz, 40 mV input signal to the circuit and obtained a time-domain waveform showing the output voltage with an amplitude at 2 V. Finally, I measured the THD of the circuit and obtained the output waveforms.

Two-stage MOSFET amplifier circuit:
Breadboard

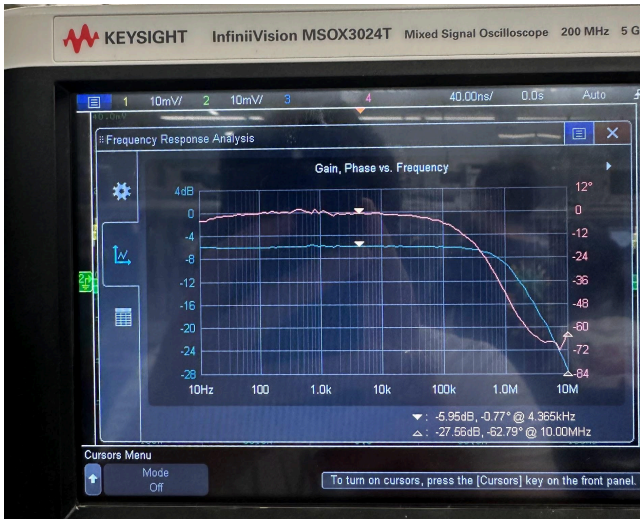


Bode Plots

Gain plot:

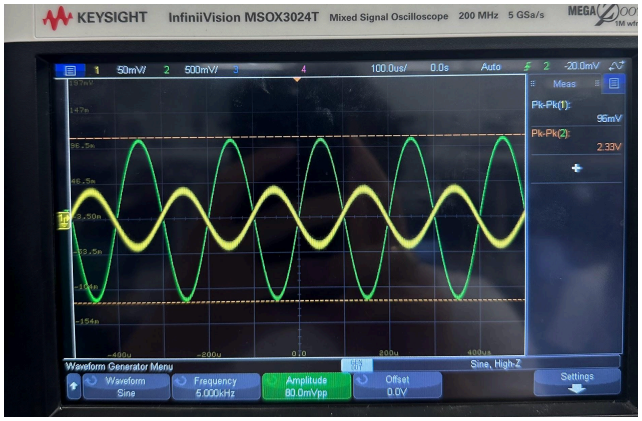


Ri plot:

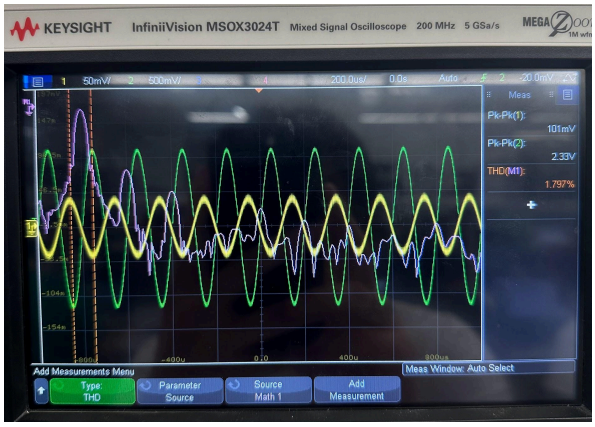


Time-domain and THD Waveforms

Transient waveform:



THD waveforms:



Data Tables and Results:

Table 1:

Below is a table for the calculated, simulated and measured component values.

	R_{G1} (kΩ)	R_{G2} (kΩ)	R_{G3} (kΩ)	R_{G4} (kΩ)	R_S (kΩ)	R_D (kΩ)	R_X (Ω)
Calculated	41.841	13.141	2.81	1.5	34.483	479.31	20
Simulated	41.8	13.1	2.81	1.5	34.5	480	20
Measured	41.8	13.1	4.7	2.2	34.5	480	20

When measuring the DC operating point, I found that the current for I_{D3} was off by about 10 mA. In order to compensate for this, I chose a smaller voltage at V_{G3} and changed the resistor values for R_{G3} and R_{G4}. This allowed for a more accurate value that was consistent with the calculated and simulated current value for I_{D3}.

Table 2:

Below is a table for the calculated, measured and simulated values for each circuit configuration.

	Node Voltages (V)	Branch Currents	A_V (V/V)	R_i (kΩ)	$V_{Out\text{-}(0\text{-}peak)}$ (V)	THD (%)
Calculated	V_{G1} = 2.609 V V_{S1} = 4.5 V $V_{D1} = V_{G2}$ = 1.95 V V_{D2} = 5V $V_{S2} = V_{D3}$ = -1 V V_{G3} = -1.52 V	I_{RG2} = 181.95 uA I_{RG4} = 2.32 mA I_{D1} = 14.52 uA I_{D2} = 25 mA I_{D3} = 25 uA	50	10	2	N/A

Simulated	V_{G1} = 2.61 V V_{S1} = 4.5 V $V_{D1} = V_{G2}$ = 1.98 V V_{D2} = 5V $V_{S2} = V_{D3}$ = -1 V V_{G3} = -1.52 V	I_{RG2} = 182.15 uA I_{RG4} = 2.32 mA I_{D1} = 14.52 uA I_{D2} = 24.56 mA I_{D3} = 24.56 mA	56.18	9.974	2.014	5.17
Measured	V_{G1} = 2.626 V V_{S1} = 4.475 V $V_{D1} = V_{G2}$ = 1.93 V V_{D2} = 5 V $V_{S2} = V_{D3}$ = -0.688 V V_{G3} = -1.798 V	I_{RG2} = 181.9 uA I_{RG4} = 1.543 mA I_{D1} = 14.94 uA I_{D2} = 25.5 mA I_{D3} = 25.5 mA	29.55	10.165	2.33	1.787

Here we can see that the calculated, simulated, and measured values are very similar to each other with the biggest difference being the gain that was measured during the lab. Due to the susceptible variation of the threshold voltage for the transistor used in the lab, this affects $V_{GS/SG}$ as well as the overdrive voltage for the transistor. As a result, this affects A_{V1} and reduces the overall gain from 50 to 29.55. The rest of the values however satisfy the design specifications and verifies the simulated and calculated values.