

Joseph Nguyen

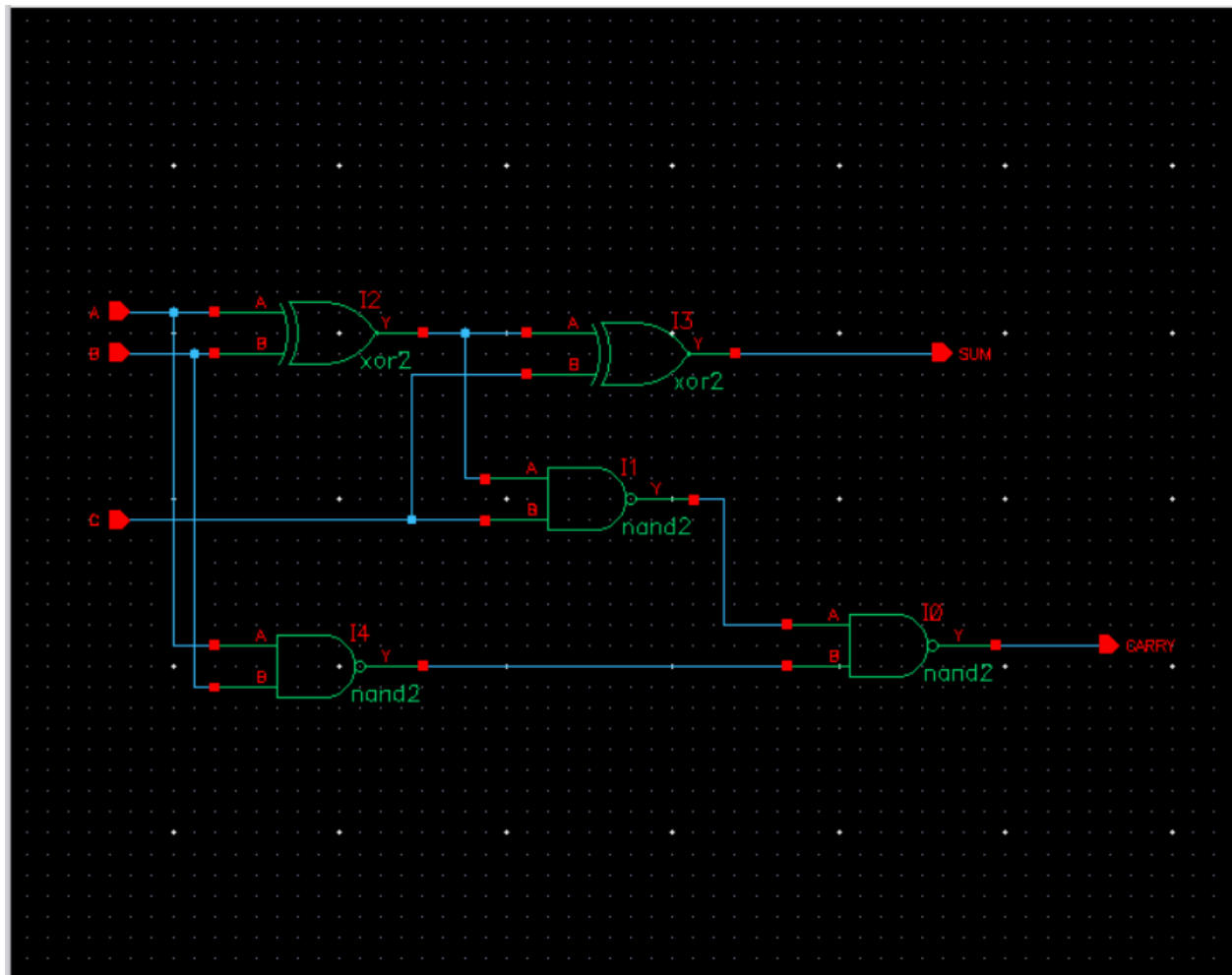
ECEN 454 Section 510

Lab date: 5 September 2024

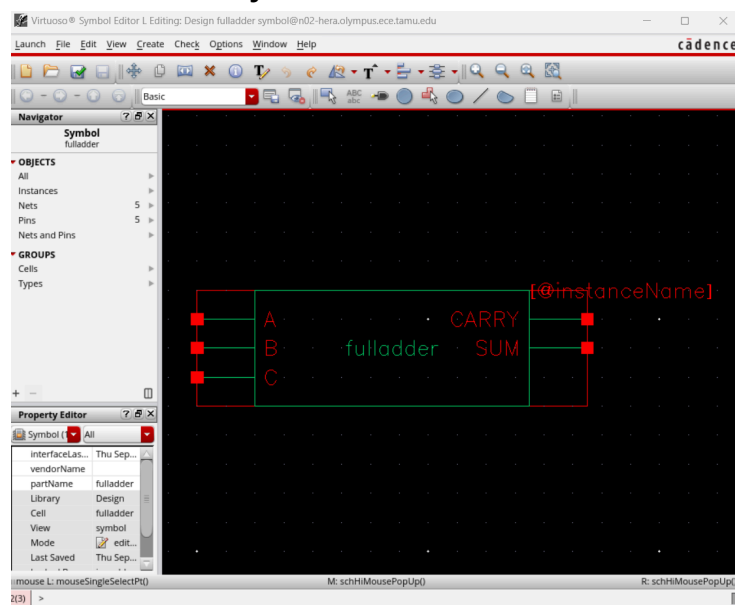
Due date: 14 September 2024

## **Lab 1: Introduction to Cadence Schematic Design & Simulation**

## 1-bit Full Adder Schematic:



## 1-bit Full Adder Symbol:



## 1-bit Full Adder Verilog:

```
// Verilog stimulus file.
// Please do not create a module in this file.

// Default verilog stimulus.

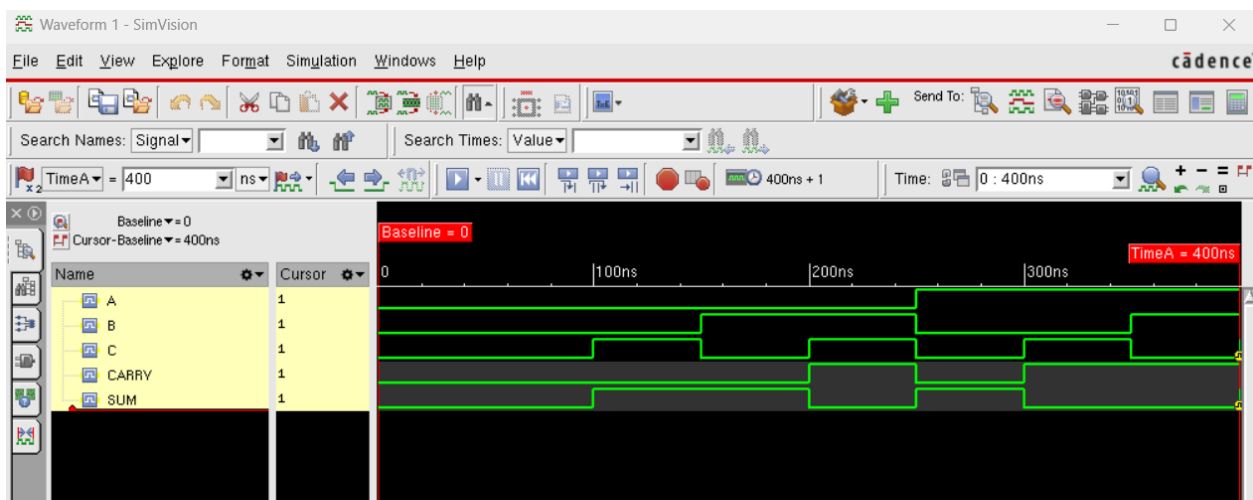
initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);

initial
begin

    A = 1'b0;
    B = 1'b0;
    C = 1'b0;

#50 A=1'b0; B=1'b0; C=1'b1;           //ABC=001
#50 A=1'b0; B=1'b1; C=1'b0;           //ABC=010
#50 A=1'b0; B=1'b1; C=1'b1;           //ABC=011
#50 A=1'b1; B=1'b0; C=1'b0;           //ABC=100
#50 A=1'b1; B=1'b0; C=1'b1;           //ABC=101
#50 A=1'b1; B=1'b1; C=1'b0;           //ABC=110
#50 A=1'b1; B=1'b1; C=1'b1;           //ABC=111
end
```

## 1-bit Full Adder Simulation Waveform:



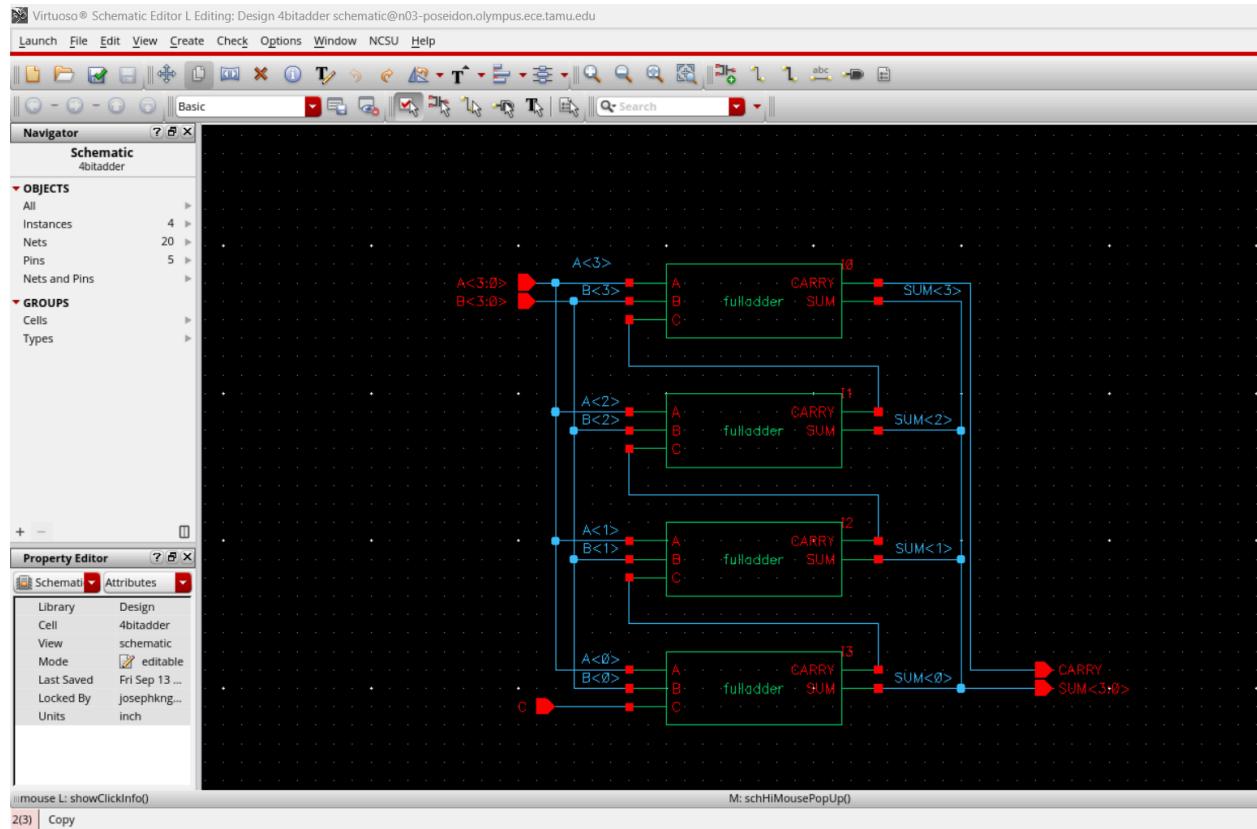
## 1-bit Full Adder Simout:

```
-----
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test -all -depth 1
Created probe 1
ncsim> run

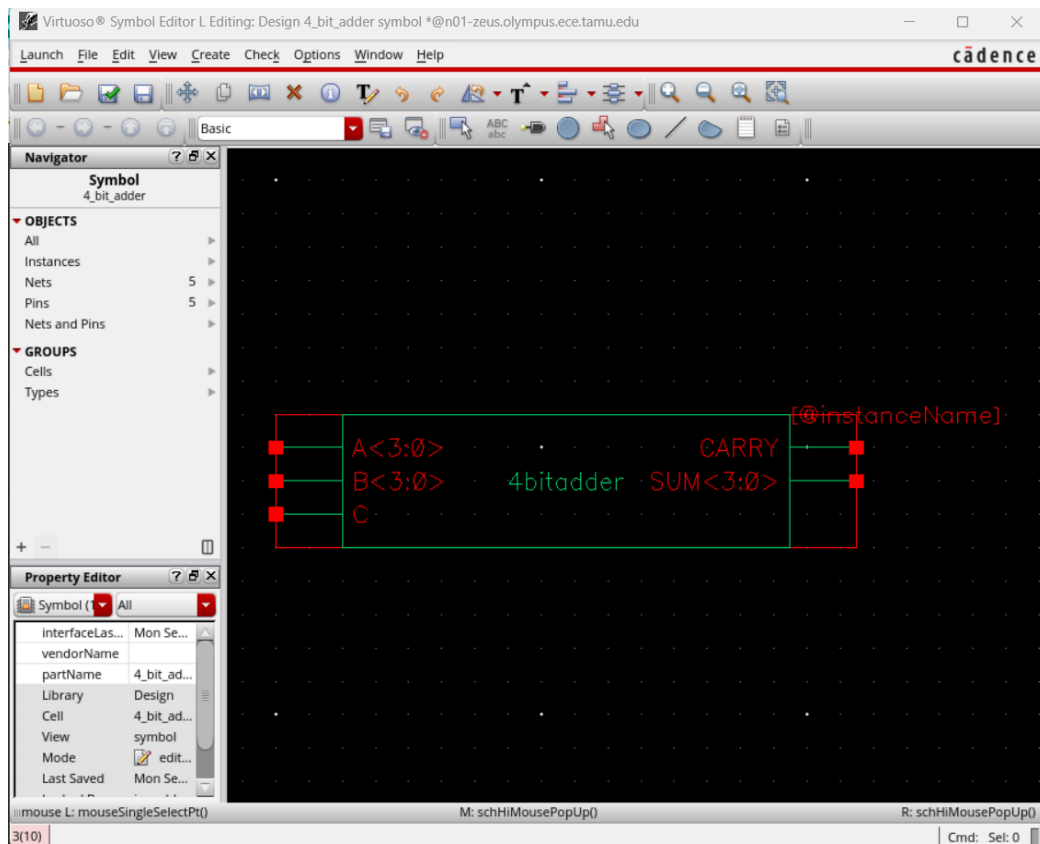
    0 A=0, B=0, C=0, SUM=0, CARRY=0
   100 A=0, B=0, C=1, SUM=1, CARRY=0
   150 A=0, B=1, C=0, SUM=1, CARRY=0
   200 A=0, B=1, C=1, SUM=0, CARRY=1
   250 A=1, B=0, C=0, SUM=1, CARRY=0
   300 A=1, B=0, C=1, SUM=0, CARRY=1
   350 A=1, B=1, C=0, SUM=0, CARRY=1
   400 A=1, B=1, C=1, SUM=1, CARRY=1

ncsim> run
ncsim> TOOL: ncx1mode 15.20-s086: Exiting on Sep 05, 2024
```

## 4-bit Adder Schematic:



## 4-bit Adder Symbol:



## 4-bit Adder Verilog:

```
// Verilog stimulus file.
// Please do not create a module in this file.

// Default verilog stimulus.
initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);

initial
begin

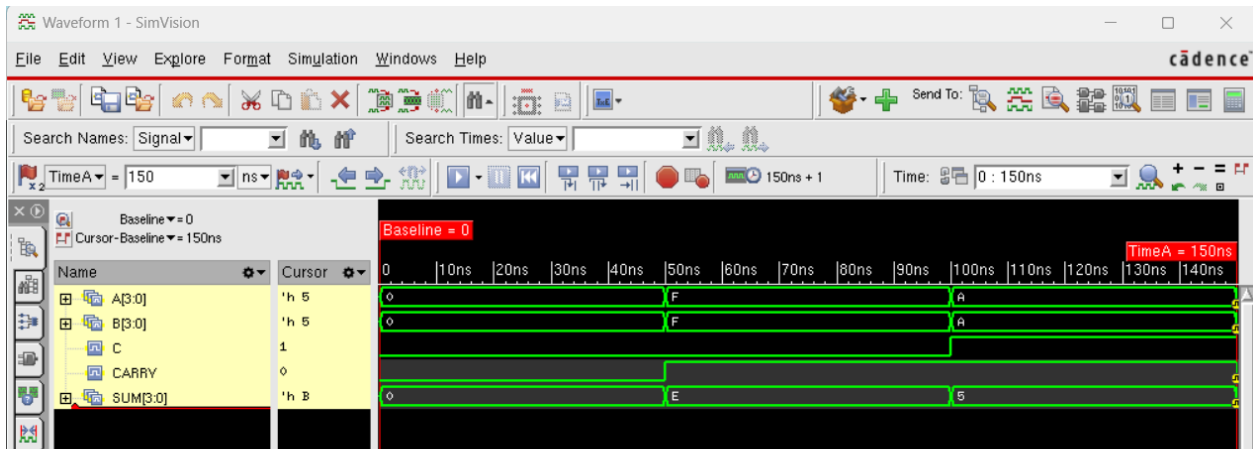
    A[3:0] = 4'b0000;

    B[3:0] = 4'b0000;

    C = 1'b0;
#50 A=4'b1111; B=4'b1111; C=1'b0;           //ABC=111111110
#50 A=4'b1010; B=4'b1010; C=1'b1;          //ABC=101010101
#50 A=4'b0101; B=4'b0101; C=1'b1;          //ABC=010101010
end

initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);
initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);
initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);
```

#### 4-bit Adder Simulation Waveform:



#### 4-bit Adder Simout:

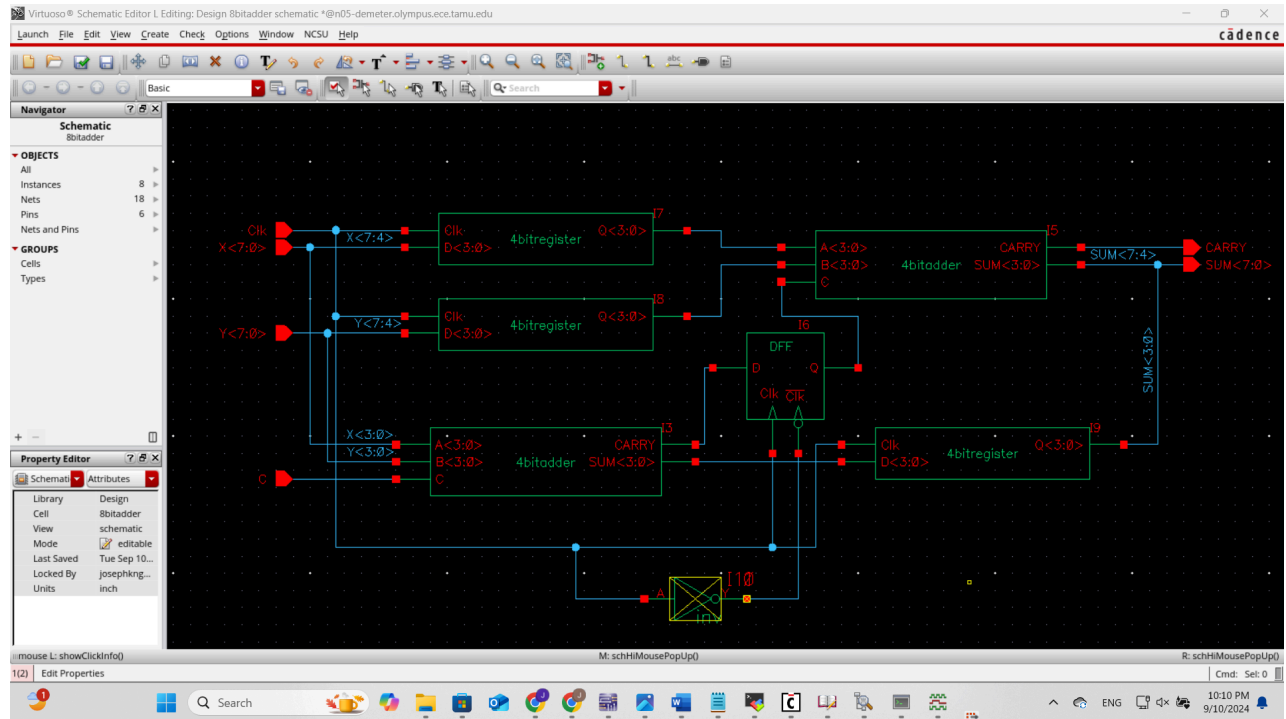
Relinquished control to SimVision...

```
nccsim>
nccsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/nccsimrc
nccsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
nccsim> probe -create -shm test -all -depth 1
Created probe 1
nccsim> run

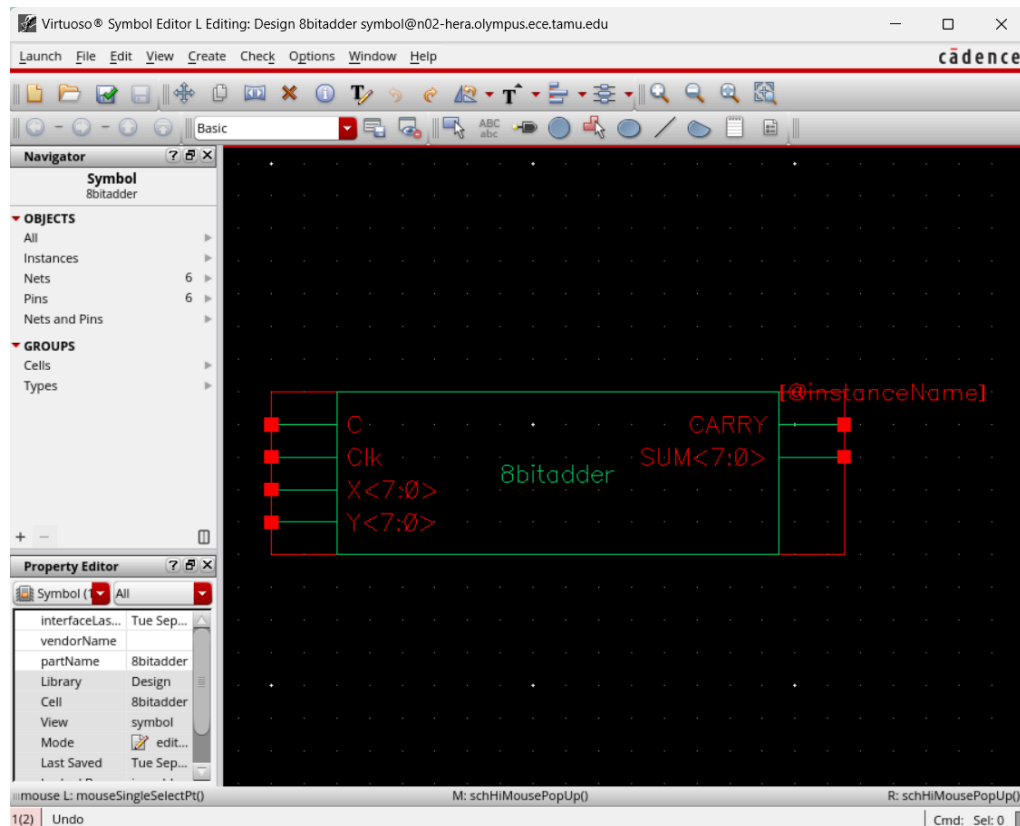
      0 A=0000, B=0000, C=0, SUM=0000, CARRY=0
     50 A=1111, B=1111, C=0, SUM=1110, CARRY=1
    100 A=1010, B=1010, C=1, SUM=0101, CARRY=1
    150 A=0101, B=0101, C=1, SUM=1011, CARRY=0

nccsim>
```

## 8-bit Adder Schematic:



## 8-bit Adder Symbol:

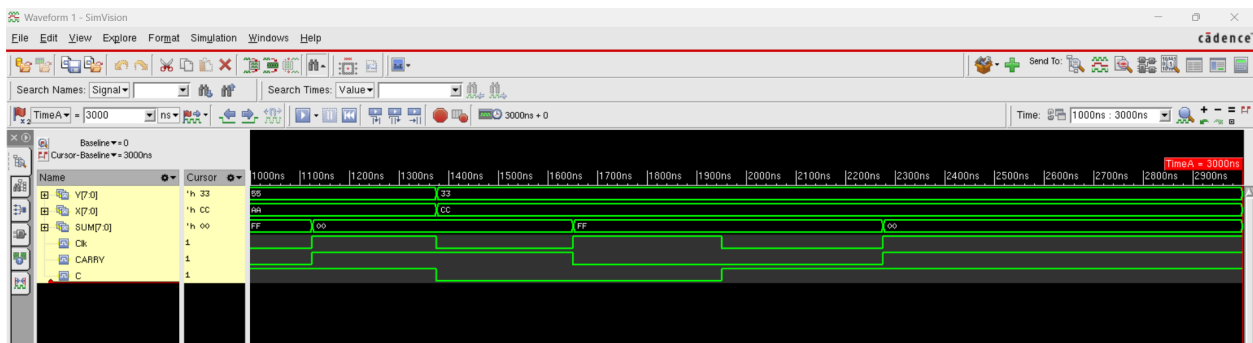
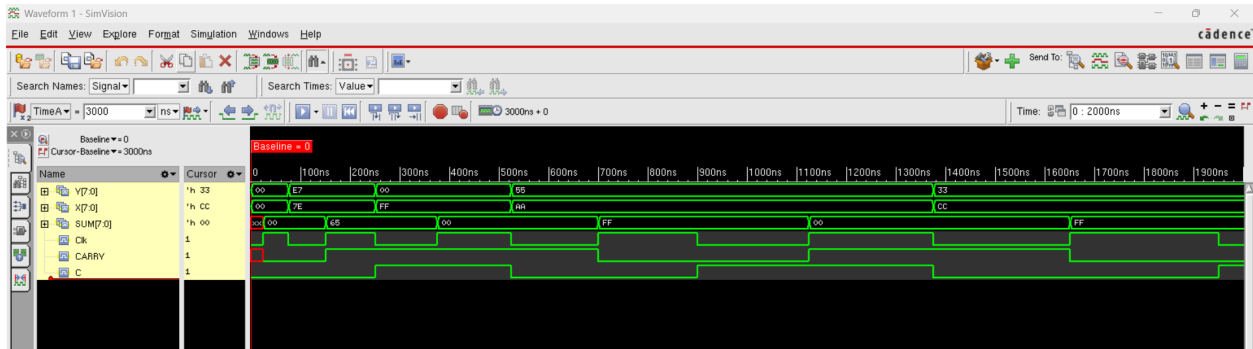


### 8-bit Adder Verilog:

[illegible]



## 8-bit Adder Simulation Waveforms:



## 8-bit Adder Simout:

```
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test -all -depth 1
Created probe 1
ncsim> run
      0 X=00000000, Y=00000000, C=0, SUM=xxxxxxxx, CARRY=x
     25 X=00000000, Y=00000000, C=0, SUM=00000000, CARRY=0
     75 X=01111110, Y=11100111, C=0, SUM=00000000, CARRY=0
    150 X=01111110, Y=11100111, C=0, SUM=01100101, CARRY=1
    250 X=11111111, Y=00000000, C=1, SUM=01100101, CARRY=1
    375 X=11111111, Y=00000000, C=1, SUM=00000000, CARRY=1
    525 X=10101010, Y=01010101, C=0, SUM=00000000, CARRY=1
    700 X=10101010, Y=01010101, C=0, SUM=11111111, CARRY=0
    900 X=10101010, Y=01010101, C=1, SUM=11111111, CARRY=0
   1125 X=10101010, Y=01010101, C=1, SUM=00000000, CARRY=1
   1375 X=11001100, Y=00110011, C=0, SUM=00000000, CARRY=1
   1650 X=11001100, Y=00110011, C=0, SUM=11111111, CARRY=0
   1950 X=11001100, Y=00110011, C=1, SUM=11111111, CARRY=0
   2275 X=11001100, Y=00110011, C=1, SUM=00000000, CARRY=1
Simulation complete via $finish(1) at time 3 US + 0
./testfixture.verilog:41 #375 $finish;
ncsim>
```