ECEN 489: Data Conversion Systems & Circuits

Lab 3: Data Conversion Figures of Merit

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https://github.com/josephknguyen02/ECEN489/tree/main

Lab Experiment:

For the lab experiment I began by building the comparator for part 1 in the lab manual shown below.

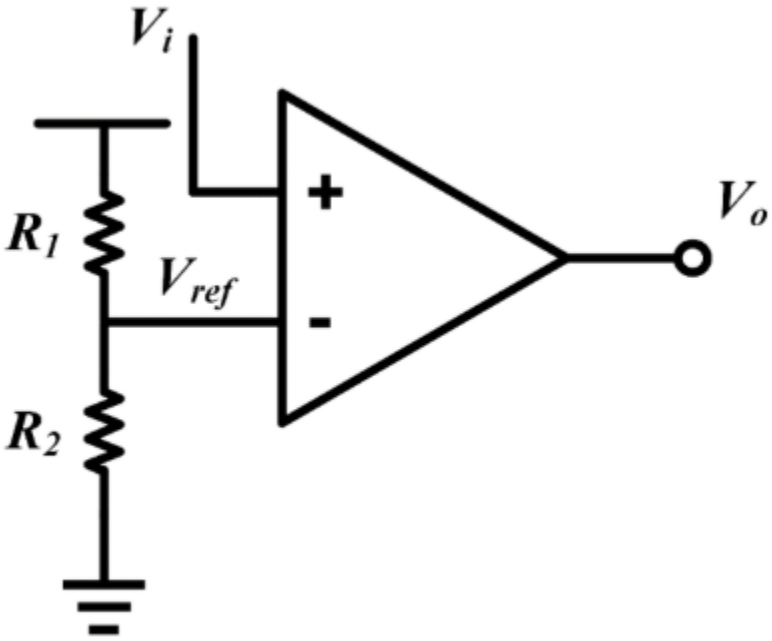
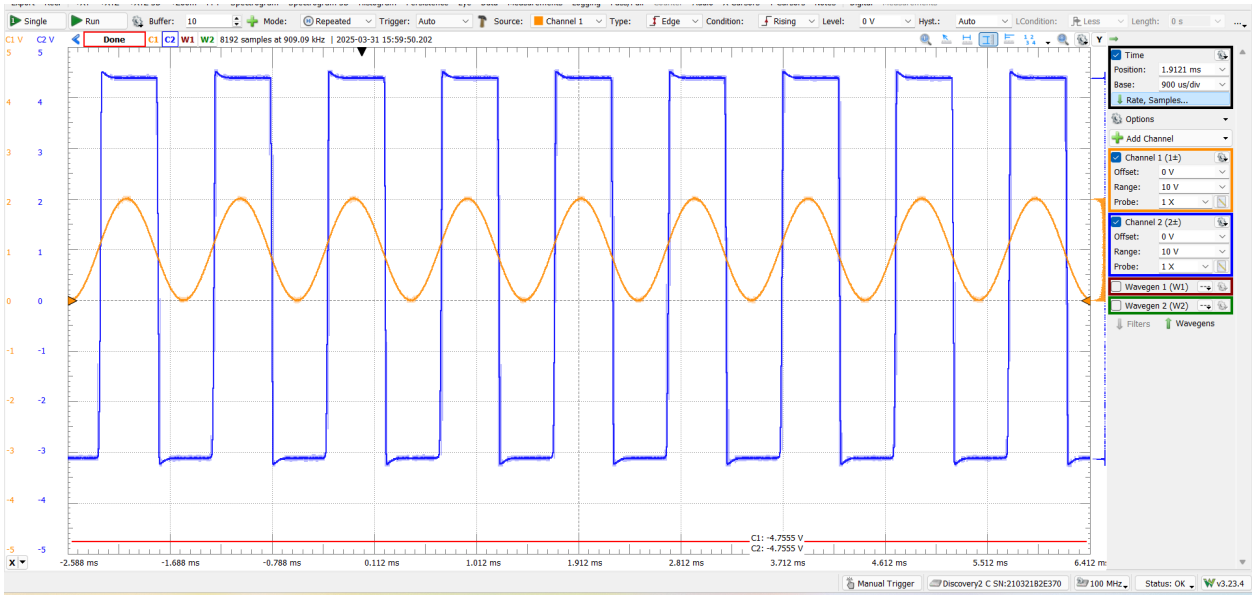


Figure 1: Block diagram of a simple comparator

Using 5V as Vdd, I used a 4k resistor for R_1 and a 1k resistor for R_2 in order to get a reference voltage of 1V. Using the AD2 to power the op-amp, I drove a 100kHz sine wave to the input and observed the output waveform which is shown below



As we can see the comparator behaves correctly showing the high/low outputs at around 1V.

For part 2, I proceeded by building the flash ADC architecture using 7 comparators.

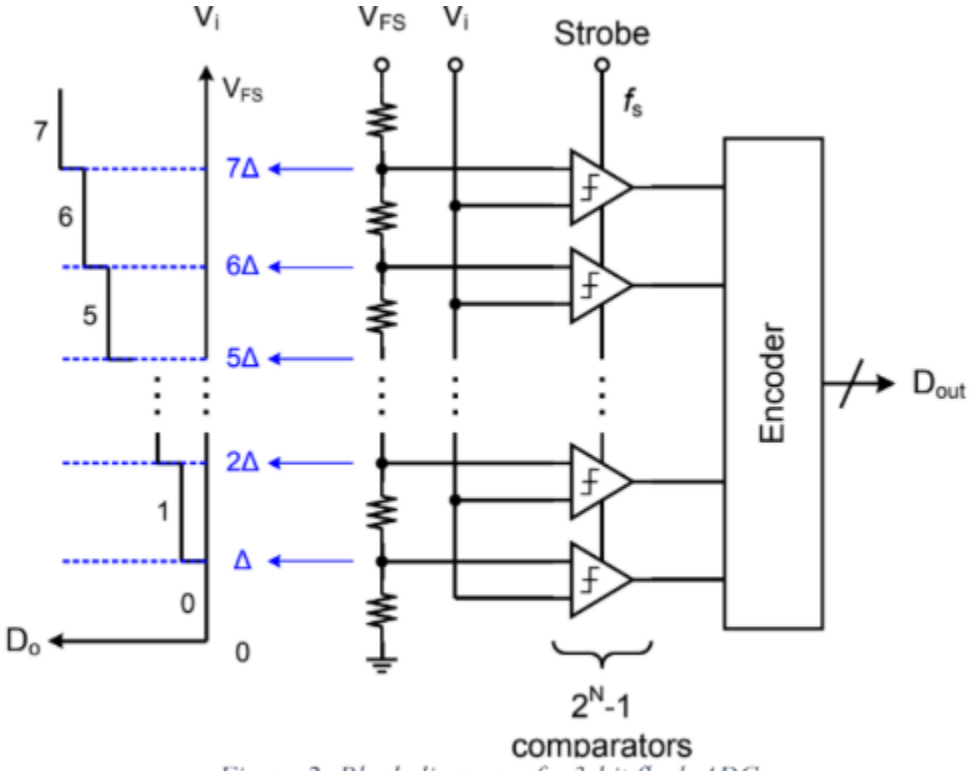
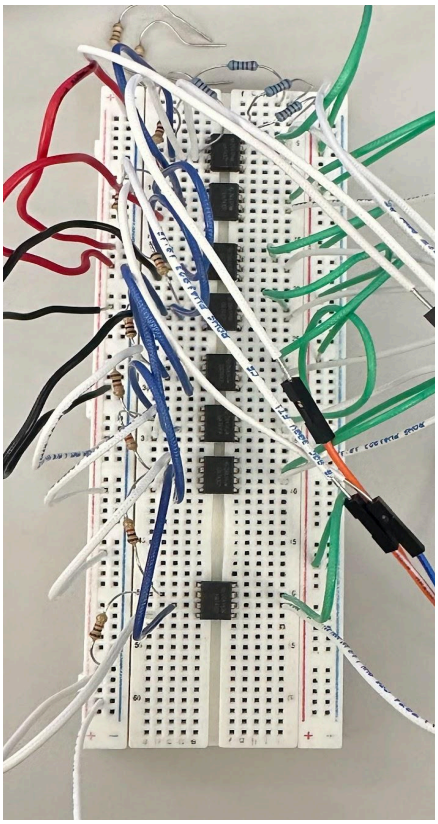
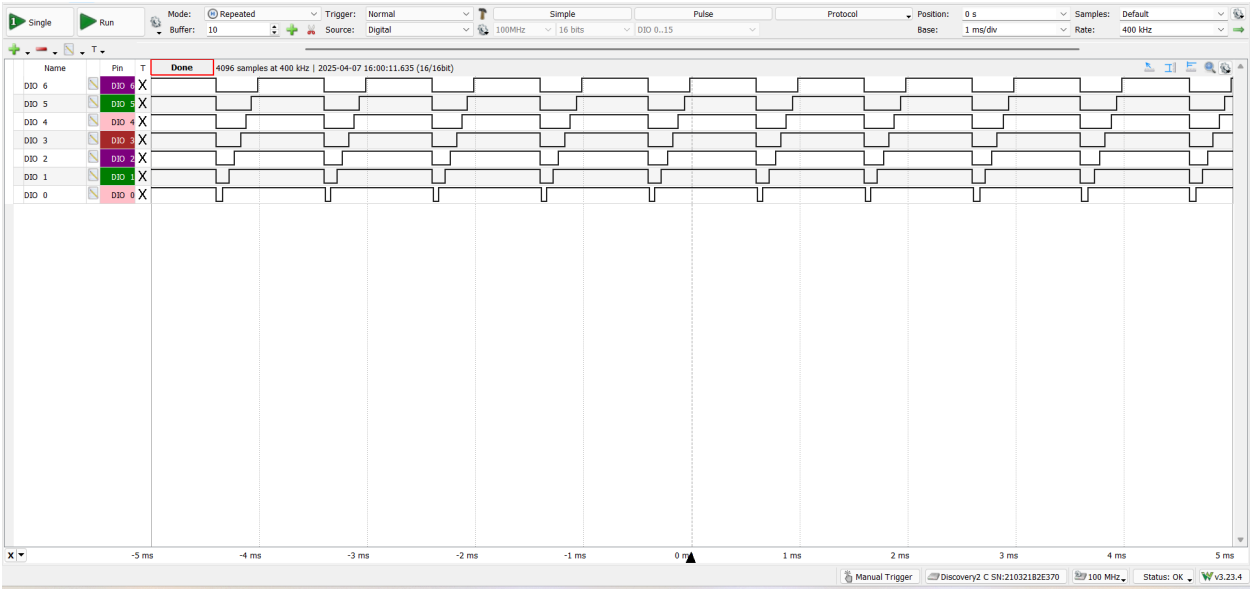


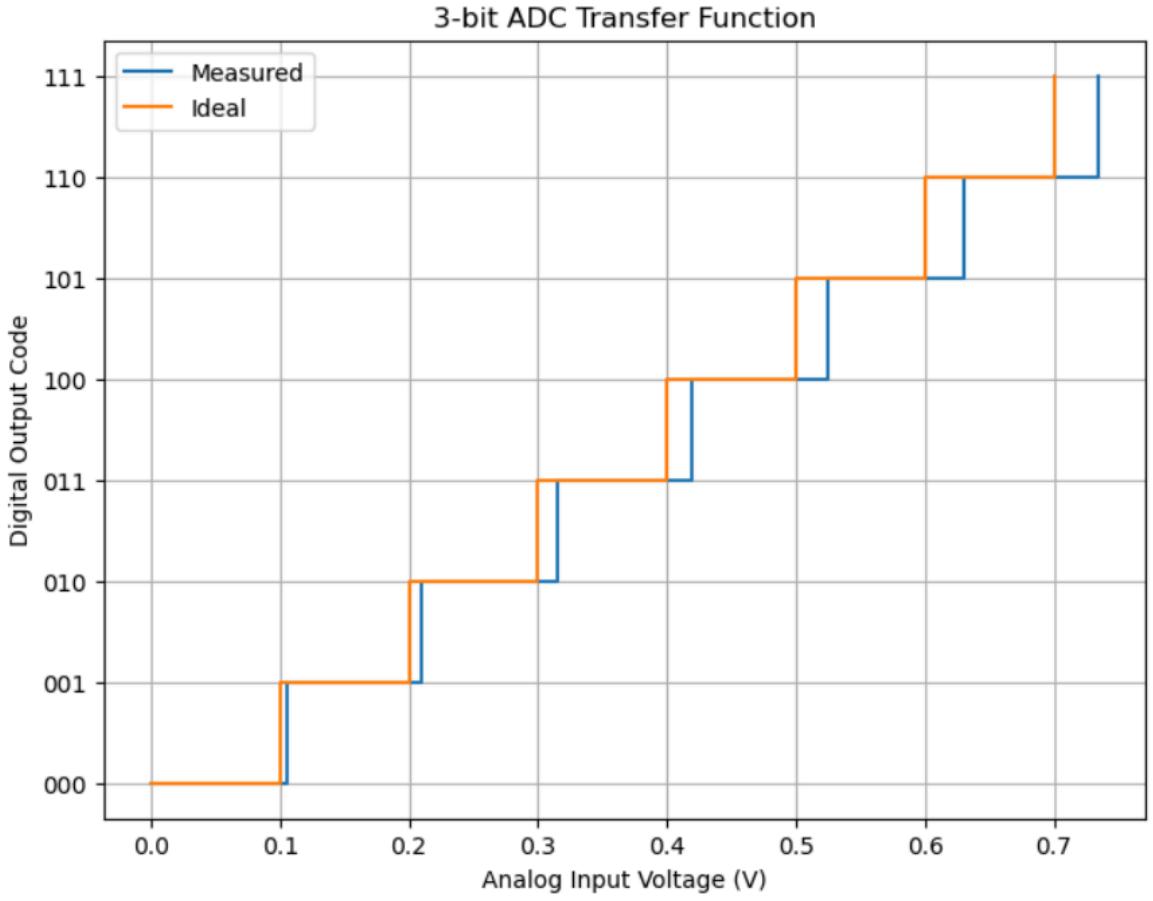
Figure 2: Block diagram of a 3-bit flash ADC



I then used the logic analyzer on the AD2 to capture the digital bits from the outputs of each of the comparators with a ramp as the input.



After exporting the data, I used python to plot the transfer function for the ADC and obtain the offset error, full-scale error, gain factor, DNL and INL.



```
offset_error = np.abs(Vref[1] - Vref_ideal[1])
fs_error = np.abs(Vref[-1] - Vref_ideal[-1])
gain_error = ((Vref[-1]+1) - (Vref_ideal[1])-1)/7

print(f"offset error = {offset_error:.3f}")
print(f"full-scale error = {fs_error:.3f}")
print(f"gain error = {gain_error:.3f}")
```

```
offset error = 0.005
full-scale error = 0.034
gain error = 0.091
```

```
step_sizes = np.diff(Vref)
DNL = (step_sizes / LSB) - 1
print("measured voltages:", Vref)
print("step sizes:", step_sizes)
print("DNL:", DNL)
```

```
measured voltages: [0.     0.1052 0.21   0.315  0.4198 0.5247 0.6298 0.734 ]
step sizes: [0.1052 0.1048 0.105  0.1048 0.1049 0.1051 0.1042]
DNL: [0.052 0.048 0.05  0.048 0.049 0.051 0.042]
```

```
INL = (Vref-Vref_ideal)/LSB
print("INL:", INL)
```

```
INL: [0.    0.052 0.1   0.15  0.198 0.247 0.298 0.34 ]
```