Single-Data Rate SDRAM Project
(Part No. MT48LC2M32B2)

Document Ver. 2
--/--/2021

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Objective

Set up a system to write/read data to/from multiple addresses on the SDRAM chip.

Components/Tools

- SDR SDRAM chip (part no. MT48LC2M32B2)
- 86-pin TSOP socket
- krtkl's snickerdoodle black FPGA Board
- Power supply
- Function generator

SDRAM Chip

Memory Organization

64 Mbit total memory

4 banks, 16 Mbit each

- 2^{11} rows $*$ 2^{8} columns $*$ 32 bits
- Address bits specify location at which operations take place, specific to the command issued (see A[10:0] in “Pinout” sub-section).

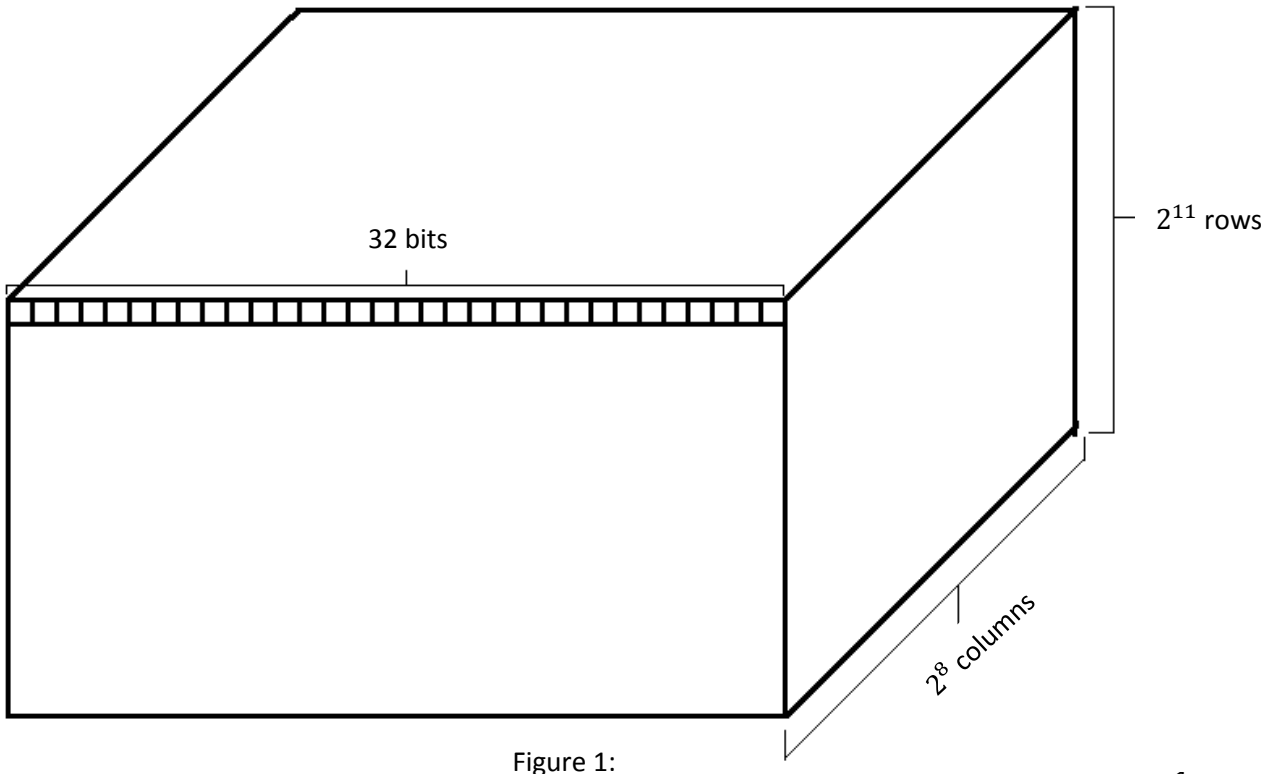


Figure 1:
Bank’s Memory Configuration

Pinout

Only included pinout description that is relevant to the current system's setup.

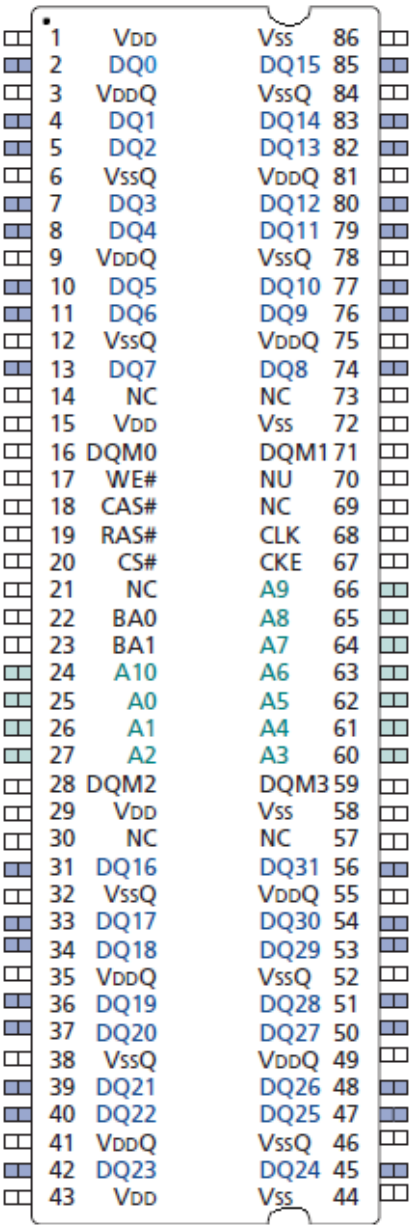


Figure 2:
TSOP Pinout

Pin	Type	Description
CLK	Input	Supplied clock signal. All SDRAM input is sampled on the rising edge.
CKE	Input	Clock enable; HIGH = enable CLK, LOW = disable CLK.
CS#	Input	Chip select; LOW = select SDRAM, HIGH = deselect SDRAM. All commands ignored when deselected.
CAS#, RAS#, WE#	Input	Command inputs (along with CS#) that determine the command being issued to the SDRAM.
DQM[3:0]	Input	DQ mask. Each DQM bit corresponds to 8 bits on DQ: DQM[3] → DQ[31:24], DQM[2] → DQ[23:16], DQM[1] → DQ[15:8], DQM[0] → DQ[7:0]. HIGH = high-Z, LOW = valid I/O (see Figure 3)
BA[1:0]	Input	Bank address; SDRAM has 4 banks. Defines which bank to issue command to. Also used for LMR command (see Figure 4).
A[10:0]	Input	Address bits. During ACTIVE command, A[10:0] = row address. During READ/WRITE command, A[7:0] = column address and A[10] enables (HIGH) or disables (LOW) auto-precharge. Also used for LMR command (see Figure 4).
DQ[31:0]	I/O	Data I/O to/from SDRAM.
V_{DDQ}	Supply	DQ power.
V_{SSQ}	Supply	DQ ground.
V_{DD}	Supply	SDRAM power.
V_{SS}	Supply	SDRAM ground.
NC	-	Not connected.
NU	-	Not used.

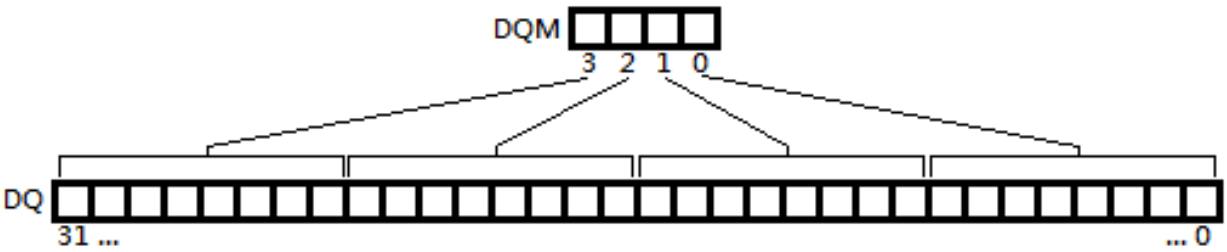


Figure 3:
DQM to DQ Relation

Mode Register

The mode register defines the operation of the SDRAM chip which involves the write-burst mode, the CAS latency (number of clock cycles between a READ and the data being output on DQ), the burst type, and the burst length.

The mode register is programmed with the LOAD MODE REGISTER (LMR) command and it must be done when all banks are idle (done with PRECHARGE command).

LMR command uses BA[1:0] as the most significant 2 bits and A[10:0] as the least significant 11 bits for the mode register.

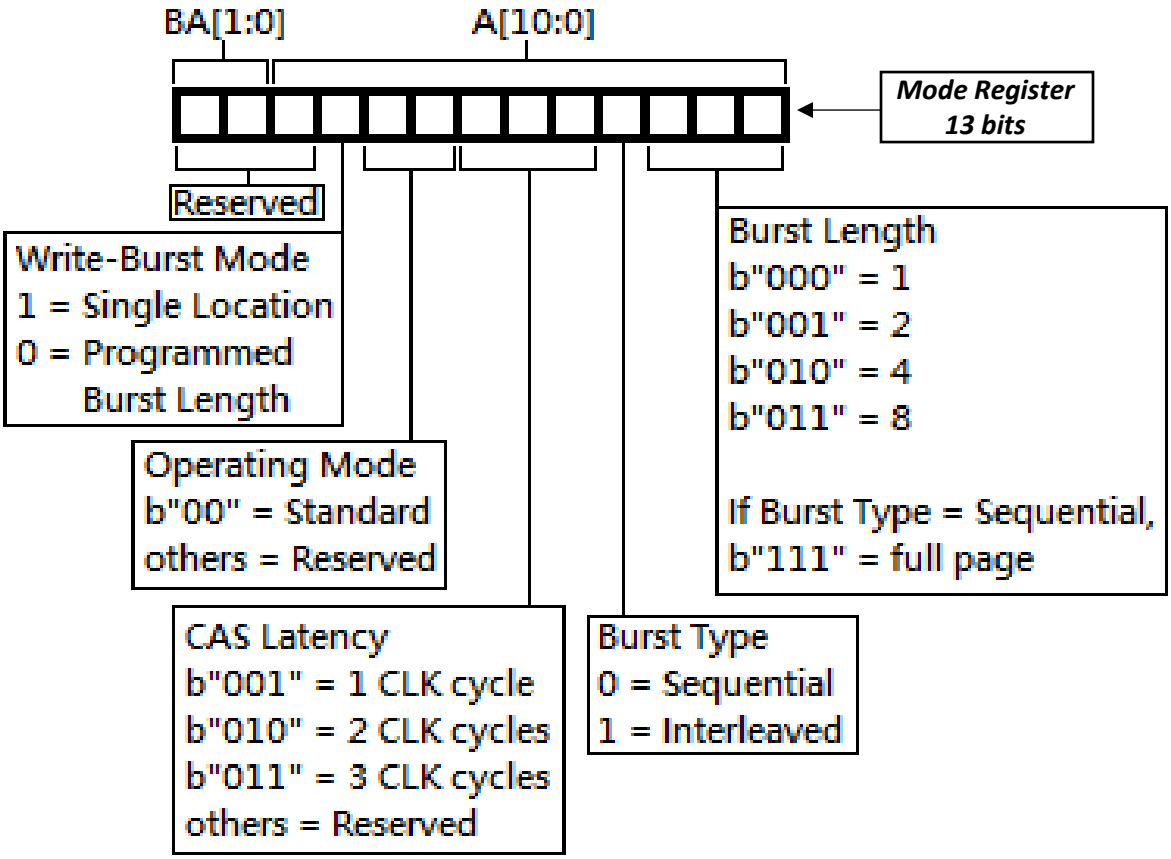


Figure 4:
Mode Register

Commands

Command Name	CS#	RAS#	CAS#	WE#	DQM	BA[1:0]	A[10:0]	DQ
COMMAND INHIBIT	H / 1	X	X	X	X	X	X	X
NO OPERATION	L / 0	H / 1	H / 1	H / 1	X	X	X	X
ACTIVE	L / 0	L / 0	H / 1	H / 1	X	Bank	Row	X
READ	L / 0	H / 1	L / 0	H / 1	L/H / 0/1	Bank	Column	Output
WRITE	L / 0	H / 1	L / 0	L / 0	L/H / 0/1	Bank	Column	Input
BURST TERMINATE	L / 0	H / 1	H / 1	L / 0	X	X	X	X
PRECHARGE	L / 0	L / 0	H / 1	L / 0	X	X	All/Single	X
REFRESH	L / 0	L / 0	L / 0	H / 1	X	X	X	X
LOAD MODE REGISTER	L / 0	L / 0	L / 0	L / 0	X	MR[12:11]	MR[10:0]	X
READ/WRITE Enable	X	X	X	X	L / 0	X	X	Valid
READ/WRITE Inhibit	X	X	X	X	H / 1	X	X	High-Z

Notes:

PRECHARGE
If A[10] = 1, precharge all banks (deactivate all rows).
If A[10] = 0, precharge bank determined by BA[1:0] (deactivate all rows in that specific bank).

REFRESH
If CKE = 1, REFRESH is AUTO REFRESH command and must be explicitly issued.
If CKE = 0, REFRESH is SELF REFRESH command and the SDRAM refreshes itself.

Timing

CAS Latency, CL

CAS – Column Address Strobe (deprecated term)

It is the number of clock cycles between sending a column address to the SDRAM and the data being available on DQ. [1, 2]

Can be set to 1, 2, or 3 clock cycles by programming the mode register.

Mode Register Delay, t_{MRD}

Delay between programming the mode register and issuing another command.

Row Active Time, t_{RAS}

The minimum number of clock cycles required between ACTIVE and issuing PRECHARGE. In SDRAM modules, this is t_{RCD} + CL. This is the time needed to internally refresh the row and overlaps with t_{RCD}. [1]

Row Cycle Time, t_{RC}

The minimum time in cycles it takes a row to complete a full cycle, which is $t_{RC} = t_{RAS} + t_{RP}$. If this is set too short it can cause corruption of data and if it is too high, it will cause a loss in performance, but increase stability. [3]

Row Address to Column Address Delay, t_{RCD}

The minimum number of clock cycles required between opening a row of memory (ACTIVE) and accessing columns within it (READ/WRITE). The time to read the first bit of memory from a DRAM without an active row is t_{RCD} + CL. [1]

Row Refresh Cycle Timing, t_{RFC}

Determines the number of cycles to refresh a row on a memory bank. If this is set too short, it can cause corruption of data and if it is too high, it will cause a loss in performance, but increased stability. [3]

Row Precharge Time, t_{RP}

The minimum number of clock cycles required between issuing PRECHARGE and opening the next row. (1)

Timings according to the datasheet:

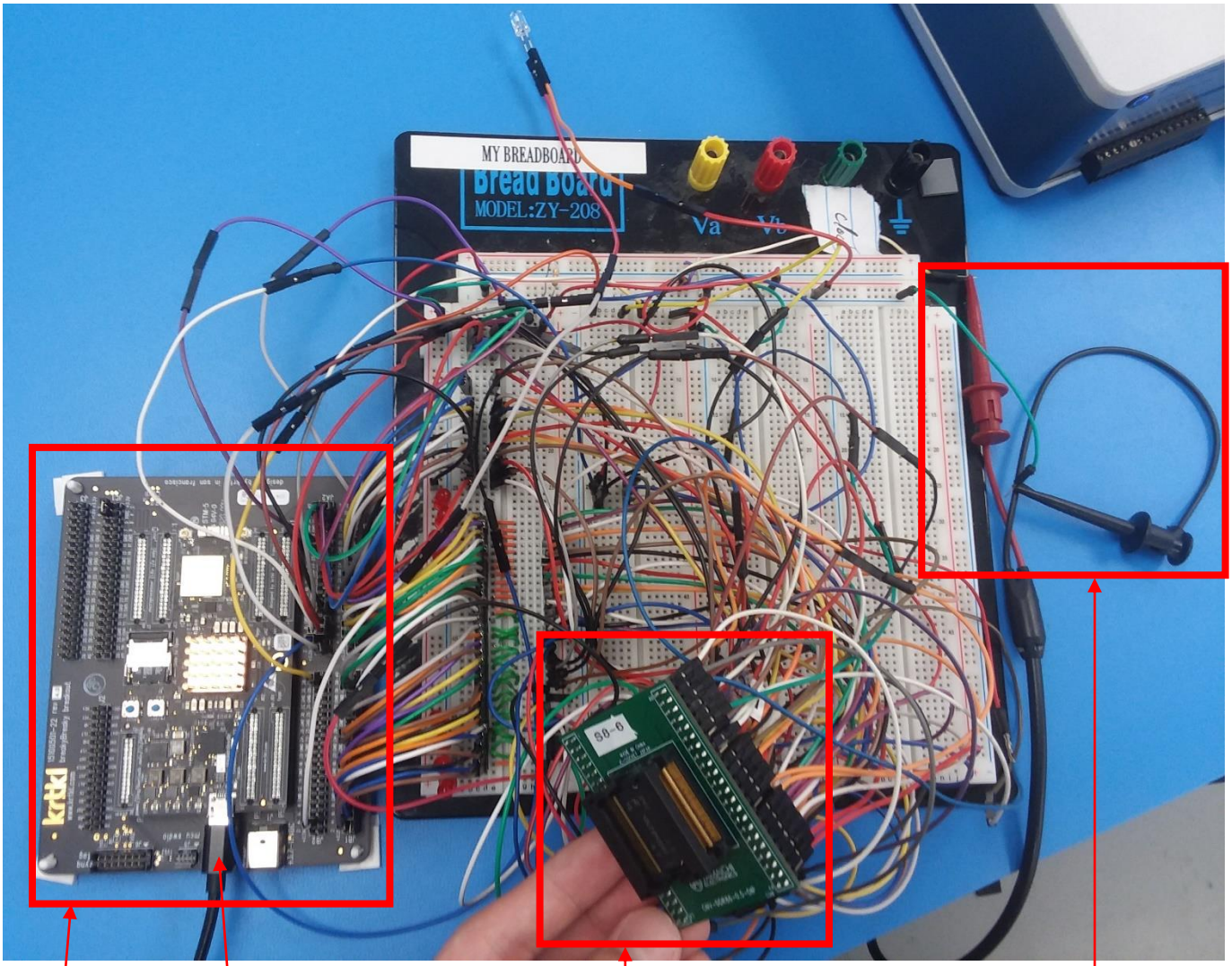
Parameter		143 MHz		167 MHz		167 MHz		183 MHz		200 MHz	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
ACTIVE to PRECHARGE	t_{RAS}	42	120k	42	120k	42	120k	38.7	120k	38.7	120k
Mode Register Delay	t_{MRD}	14	-	12	-	12	-	11	-	10	-
ACTIVE to ACTIVE	t_{RC}	70	-	60	-	60	-	55	-	55	-
ACTIVE to READ/WRITE Delay	t_{RCD}	20	-	18	-	18	-	16.5	-	15	-
AUTO REFRESH Period	t_{RFC}	70	-	60	-	60	-	60	-	60	-
PRECHARGE Period	t_{RP}	20	-	18	-	18	-	16.5	-	15	-

ns

System

Description

This system uses krtkl's snickerdoodle black FPGA board as a controller for the SDRAM. A function generator is used as the SDRAM's clock signal. A power supply, either USB or an external 5 V, is used to power the whole system. All signals to/from the snickerdoodle are 3.3 V.



Pin Mapping

The snickerdoodle black FPGA board has 180 general-purpose I/O pins available.

1 GPIO is used to power the SDRAM chip's V_{DD} and V_{DDQ} pins.
4 GPIO are used to issue commands to the SDRAM (CS#, RAS#, CAS#, and WE#).
1 GPIO is used for the SDRAM's clock enable pin, CKE.
2 GPIO are used for the SDRAM's bank address pins, BA[1:0].
11 GPIO are used for the SDRAM's address pins, A[10:0].
4 GPIO are used for the SDRAM's DQ mask pins, DQM[3:0].
32 GPIO are used for the SDRAM's data I/O pins, DQ[31:0].
1 GPIO is used for a push-button which starts the system.
1 GPIO is used for an LED that communicates whether the data written to the SDRAM is correct or not.

LEDs are connected to the least and most significant nibble of the DQ bus to visually verify written data.

A function generator will send a clock signal to both the FPGA and SDRAM chip.

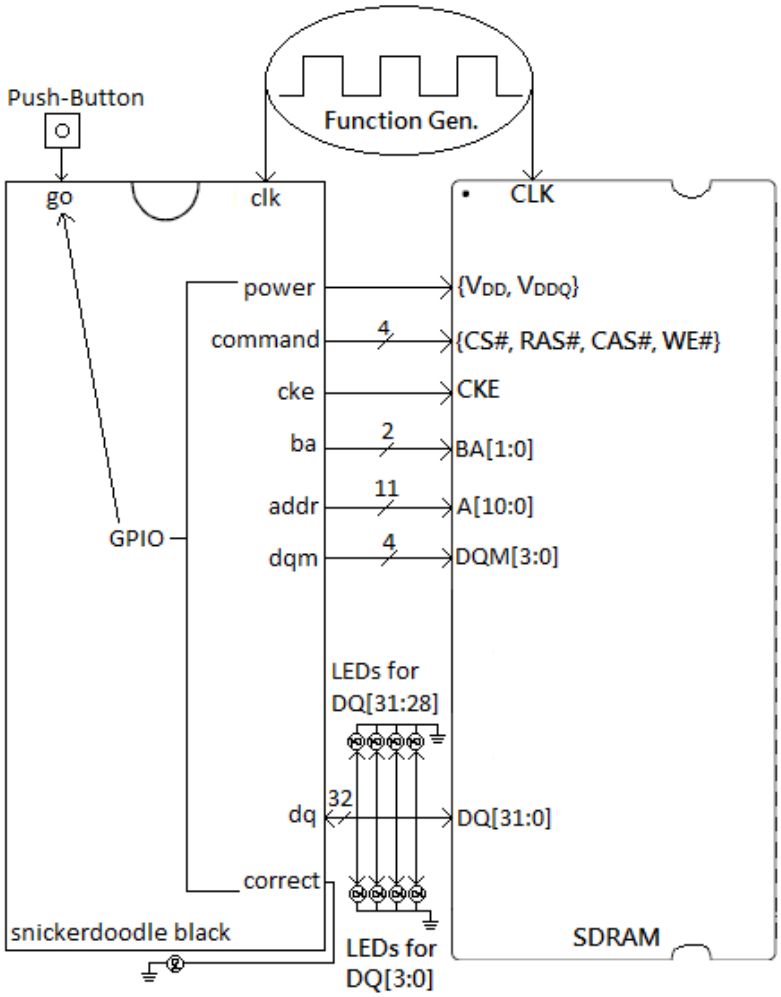


Figure 5:
System Diagram

Port Names – Input/Output		SDRAM Pin
clk	- Input	-
go	- Input	-
cke	- Output	CKE
power	- Output	{V_{DD}, V_{DDQ}}
command	- Output	{CS#, RAS#, CAS#, and WE#}
dqm	- Output	DQM[3:0]
ba	- Output	BA[1:0]
addr	- Output	A[10:0]
dq	- Input/Output	DQ[31:0]
correct	- Output	-

Timing

The previous version of this project involved using two PIC18F45K50 MCUs which introduced timing complications. Adapting the design from the previous version to the snickerdoodle black FPGA board removed those timing complications mainly because of the snickerdoodle's capability for receiving higher clock frequencies.

The commands the system is currently using that have timing constraints are PRECHARGE, AUTO REFRESH, LOAD MODE REGISTER, ACTIVE, READ, and WRITE.

Constraint	Requirement	Commands
t_{MRD}	2 cycles	LOAD MODE REGISTER
t_{RCD}	3 cycles	ACTIVE
t_{RFC}	2 cycles	AUTO REFRESH
t_{RP}	3 cycles	PRECHARGE, READ/WRITE (when auto PRECHARGE is enabled)

To fulfill these timing constraints, I made a timer architecture and instantiated an entity of it in the design. The design will match the timing constraint requirements, except for t_{RFC}. For increased data stability, t_{RFC} will be 10 cycles.

The SDRAM requires a REFRESH every 15.625 µs to maintain data integrity.

Code

[Code documentation omitted]

Design Corrections / Errors

Corrections:

- Unlike the previous version, all SDRAM pins (more notably DQM, BA, and A) are connected to an I/O pin on the FPGA board.

- The weak and jittery signals in the previous version were due to the enabled auto-precharge when issuing a READ command; READS are now done with 50 cycles and a separate PRECHARGE command issued afterwards.

- Design now works with a synchronous clock signal between the FPGA and SDRAM.

- Only 1 pin is used for powering the SDRAM as opposed to the 2 pins used in the previous version.

Errors:

- Design is made specifically for 5 MHz.

- Timer needs to be recoded:
  - Instead of 2 signals for starting and stopping, only 1 is necessary.
  - When timer is started, it starts its count at x”2” to make the waveform more precise, but it’s logically confusing.

- In the writing portion of the “Running” sys_state, there are no AUTO REFRESH commands issued; when testing all SDRAM addresses, design will need AUTO REFRESH commands in between writing to maintain the data integrity.

Miscellaneous

References

1.) **Memory Timings – Wikipedia**
https://en.wikipedia.org/wiki/Memory_timings#:~:text=The%20timing%20of%20modern%20synchronous,%2D8%2D8%2D24.

2.) **What Is CAS Latency in RAM? CL Timings Explained – Tom's Hardware**
https://www.tomshardware.com/reviews/cas-latency-ram-cl-timings-glossary-definition,6011.html

3.) **Memory Timings Explained – TechPowerUp**
https://www.techpowerup.com/articles/overclocking/AMD/memory/131/2