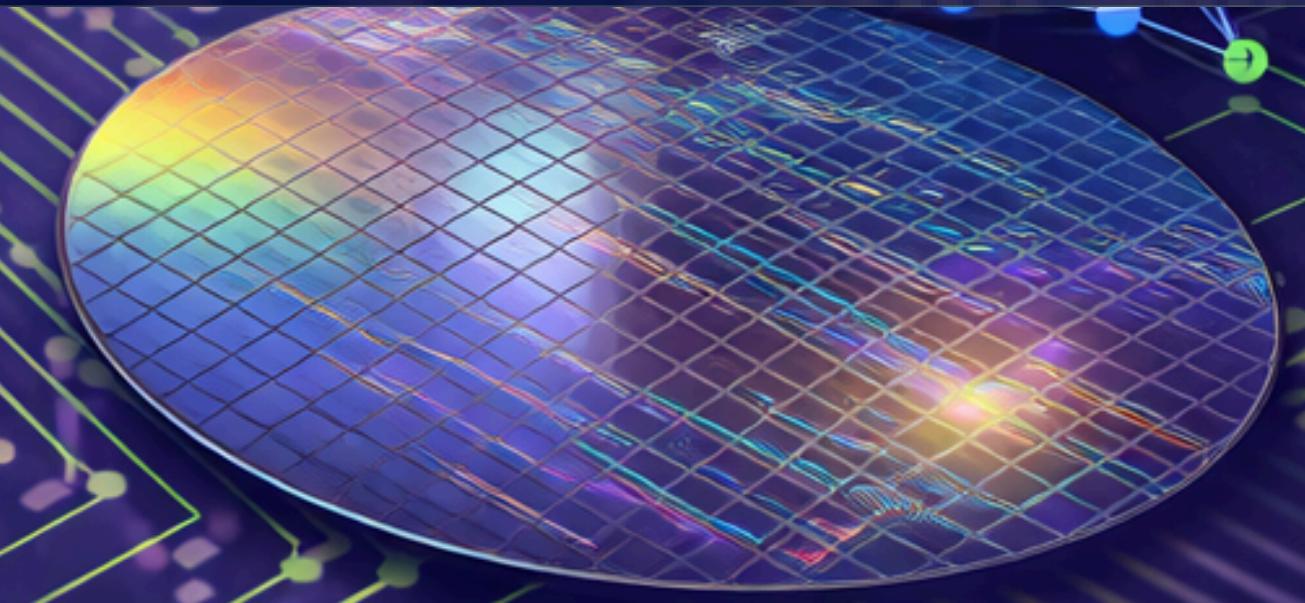


IESA DeepTech Hackathon

Idea Submission on

Edge-AI Defect Classification
for Semiconductor Images



Team Name

Robic Rovers --Silicon Simplified, Intelligence Amplified

Team Details

Team Name:

Robic Rovers

SR. NO	ROLE	NAME	ACADEMIC YEAR
1	Team Leader (Data Engineer)	Joseph Sam M (B.Tech AIDS)	2025 - 2026
2	Model Development Engineer	Nithish K (B.Tech AIDS)	2025 - 2026
3	Evaluation & Analysis Engineer	Raghul M (B.Tech AIDS)	2025 - 2026
4	Open Source Dataset Collection	Rupesh Nawin S (B.E ECE)	2025 - 2026
5	Wafer Defect Domain & Dataset	Suryaprasath S (B.E ECE)	2025 - 2026
6	Faculty Mentor(Professor)	Vijeyakumar K N (20+ years of R&D experience in ASIC design Flow)	

COLLEGE NAME

Sri Eshwar College of Engineering

TEAM LEADER CONTACT NUMBER

+91 8682045934

TEAM LEADER EMAIL ADDRESS

josephsam5934@gmail.com

Problem Statement Addressed



Edge-AI Defect Classification for Semiconductor Images

- As per Moore's Law, transistor count increases with technology scaling.
- Feature sizes shrink to deep nodes (≈ 2 nm), reducing channel width.
- Extreme miniaturization increases defect susceptibility, impacting yield & reliability.
- Wafer inspection generates large image volumes.
- Cloud/manual inspection faces latency, bandwidth, and scalability issues.

Need:

A lightweight Edge-AI defect classification system for fast, real-time on-device inspection

Idea Description



KEY CONCEPT & APPROACH

The proposed idea uses a **CNN-based image classification (supervised learning)** approach with the lightweight **SqueezeNet architecture** to automatically detect defects in semiconductor wafer images. The model processes **256×256 pixels grayscale images** and learns critical visual features such as

- **Bridge**
- **Crack**
- **LER (Line-edge roughness)**
- **Line Collapse**
- **LWV (Line Width Variant)**
- **Open**
- **Scratch**
- **Via**

SqueezeNet's efficient design enables accurate defect detection with low computational cost, making it suitable for real-time inspection.



Proposed Solution



Input:
256×256 grayscale wafer/SEM images are given as input to the CNN(convolutional neural network).

Convolution & Kernel Processing:
The images pass through multiple convolutional layers where learnable kernels slide over the image to extract low-level and high-level features such as edges, line breaks, cracks, line collapse, and surface irregularities.

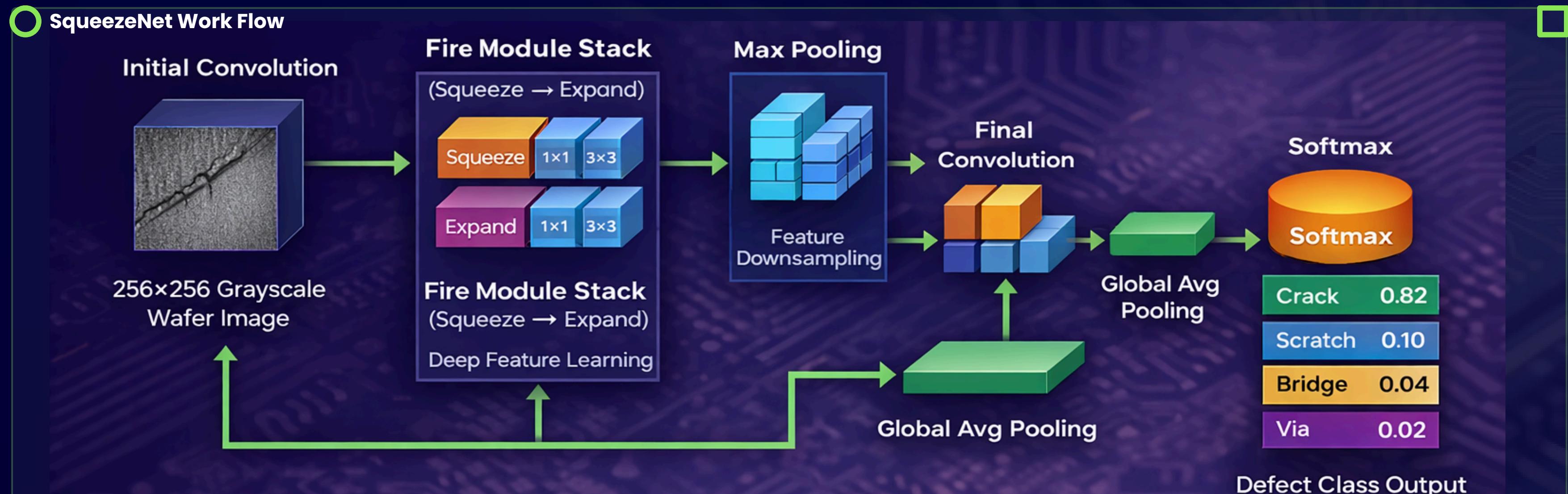
Output (Probability-Based Classification):
The final **softmax output layer** generates probability scores for each defect class. **The class with the highest probability indicates the detected defect among the 8 defined classes.**

SqueezeNet
Very small model size (< 2.5 MB)
Low memory & computation requirement
Suitable for real-time / edge deployment
Accuracy – 93% to 96%

Pooling Layer:
Pooling layers are applied after convolution to reduce spatial dimensions, suppress noise, and retain the most important defect features.

Fully Connected Layer:
The extracted features are flattened and passed to **fully connected layers (SqueezeNet classifier)** to learn defect-specific patterns.

Innovation and Uniqueness



KEY INNOVATION

- Grayscale SEM image processing
- Texture & structure feature learning
- Robust to lighting variations

COMPETITIVE ADVANTAGE

- Low memory & compute
- Fast real-time inference
- Industry deployment ready
- Reduces inspection cost

Impact and Benefits

Benefits

Why SqueezeNet is Selected ?

- Tested three CNN models: **EfficientNet, ResNet, and SqueezeNet**

SqueezeNet gave the best results :

- Accuracy: 94.8% ,Precision: 93.6% ,Recall: 92.9% ,F1-Score: 93.2% ,Model Size: < 2.5 MB ,Inference Time: < 50 ms per image**

Comparative Performance :

- SqueezeNet Accuracy: 94.8%**
- EfficientNet Accuracy: 92.1%**
- ResNet Accuracy: 90.7%**

+2-4% improvement over other tested CNN models

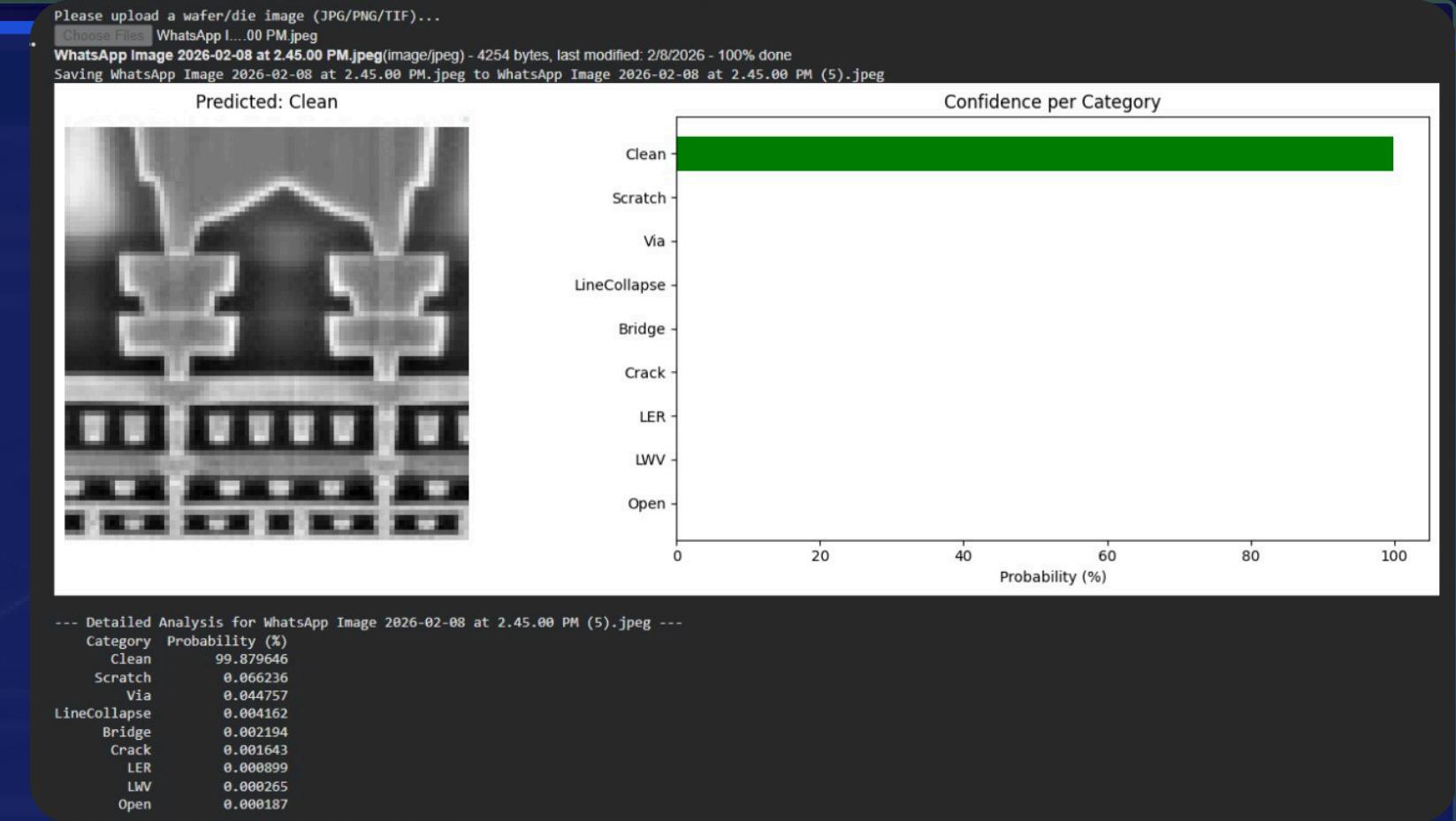
~70% smaller model size compared to ResNet

Conclusion:

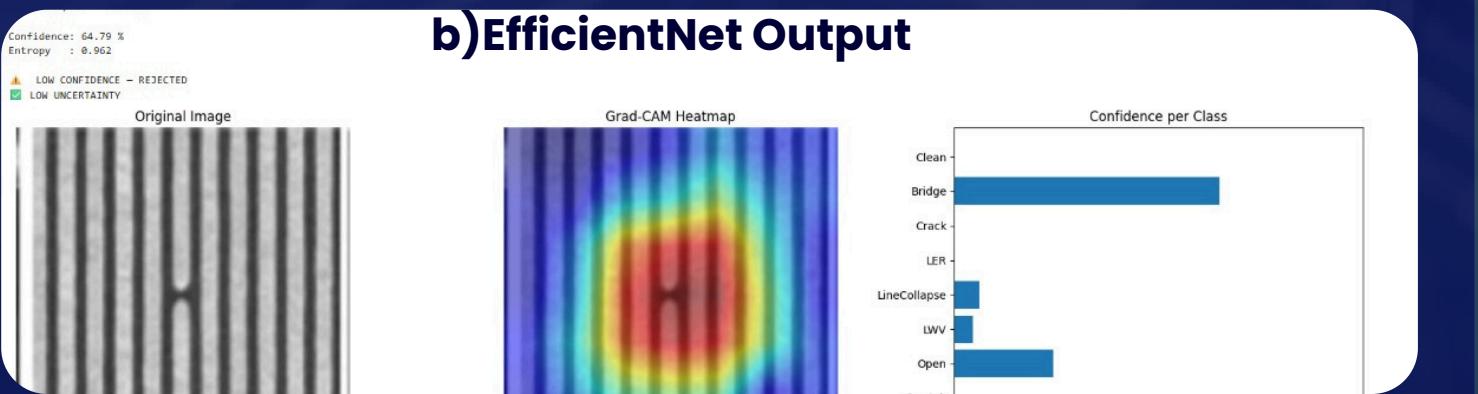
SqueezeNet provides the **best balance of accuracy + speed + model size, making it efficient for semiconductor defect detection.**

Quantifiable Outcomes

a) SqueezeNet Output More accuracy



b) EfficientNet Output



Technology & Feasibility



IMPLEMENTATION STRATEGY

Developed a CNN-based defect classification model using SqueezeNet, Optimized the model for 256×256 grayscale SEM images, Successfully trained and validated the model on curated wafer datasets, Achieved measurable performance improvements over other tested CNN models, Designed the system to run efficiently without requiring high-end GPUs for inference, A working, trained, and validated defect classification model is implemented.



Software Architecture

- End-to-End AI Pipeline
- Image Preprocessing & Augmentation
- Grayscale-Optimized SqueezeNet
- 8-Class Defect Classification
- Precision-Driven Performance Metrics



Hardware Components

- GPU-Based Model Training (Google Colab)
- CPU-Optimized Inference
- Lightweight & Memory Efficient Architecture
- Industrial System Compatibility
- No Specialized Hardware Requirement(phase-1)



Development Tools

- Python Programming Environment
- TensorFlow Deep Learning Framework
- OpenCV Image Processing Library
- NumPy & Matplotlib (Data Analysis & Visualization)
- Google Colab (GPU Training Platform)
- ONNX Model Export Support
- Docker Deployment Compatibility

GitHub & Video Link



GitHub Repository

☞ https://github.com/josephsamhub/Robic_Rovers_DeepTech_Hackathon_2026_AI_Enabled_Chip_Design



Prototype / Simulation Video

► https://drive.google.com/drive/folders/1jsIF_9jqQsUZddoIQnPxQ6A5OpX2QWFd?usp=sharing

Note:

We would like to inform that additional semiconductor wafer defect datasets are **expected to be received from industry sources after the current submission deadline.**

If our team is selected for Phase-2, we request permission to further train and **fine-tune the AI/ML model** using these industry datasets. Incorporating **real-time industrial data will help improve the model's learning capability** and **significantly increase the accuracy and reliability of defect detection.**

Research and References



Research Background

We attempted dataset collection from **Zenodo**, **Figshare**, **Hugging Face**, **SCL Semiconductor Laboratory**, and **IEEE DataPort**. Due to access and confidentiality limitations, only limited datasets were obtained, including some defect images extracted from IEEE research publications.



References & Citations

- 1) Pix2Pix-Based Generation of SEM Image in the ETCH Domain by SEM Image of LITHO Domain – Botong Zhao et al., 2023 International Workshop on Advanced Patterning Solutions (IWAPS), IEEE –<https://doi.org/10.1109/IWAPS60466.2023.10366092>.
- 2) Semiconductor SEM Image Defect Classification Using Supervised and Semi-Supervised Learning with Vision Transformers – Chien-Fu Huang et al., IBM Research –<https://arxiv.org/abs/2506.03345>.
- 3) SEM-CLIP: Precise Few-Shot Learning for Nanoscale Defect Detection in Scanning Electron Microscope Image – Qian Jin et al., arXiv, 2025 –<https://arxiv.org/abs/2502.14884>.