1. 128 words, 32-bits address
    a.

	CacheA	CacheB	CacheC	CacheD
# of bits for bytes displacement	7	6	4	6
# of bits for word displacement	5	4	2	4
# of bits in tag	23	24	25	26
# of sets in cache	2	2	3	0

2.
    a. 0x10010020
        i. TAG = 0001 0000 0000 0001 0000 000
        ii. Set = 00, offset = 010 0000
    b. 0x1001003c
        i. TAG = 0001 0000 0000 0001 0000 000 Hit
        ii. Set = 00, offset = 011 1100
    c. 0x10000128
        i. TAG = 0001 0000 0000 0000 0000 000
        ii. Set = 10, offset = 010 1000
    d. 0x10011016
        i. TAG = 0001 0000 0000 0001 0001 000
        ii. Set = 00, offset = 001 0110
    e. 0x10011017
        i. TAG = 0001 0000 0000 0001 0001 000 HIT
    f.

VALID	BLOCK#	TAG	CONTENT
1	0	0x80088	M[0x10011000 - 0x1001107f]
0	1		
1	2	0x80000	M[0x10000100 - 0x1000017f]
1	3		

3.

a. 0x10010020
    i. 100100 = TAG, 20 = 00(set) 100000
b. 0x1001003c
    i. 100100 = TAG, 3c = 00(set) 111100 , HIT
c. 0x10000128
    i. 100001 = TAG, 28 = 00(set) 101000
d. 0x10011016
    i. 100110 = TAG, 16 = 00(set) 010110
e. 0x10011017
    i. 100110 = TAG, 17 = 00(set) 010111 , HIT
f.

SET	VALID	DIRTY	TAG	CONTENT
SET0	1	1	100110	M[0x10011000- 0x1001103F]
	1	0	100001	M[0x10000100- 0x1000013F]
SET1	0			
	0			
SET2	0			
	0			
SET3	0			
	0			