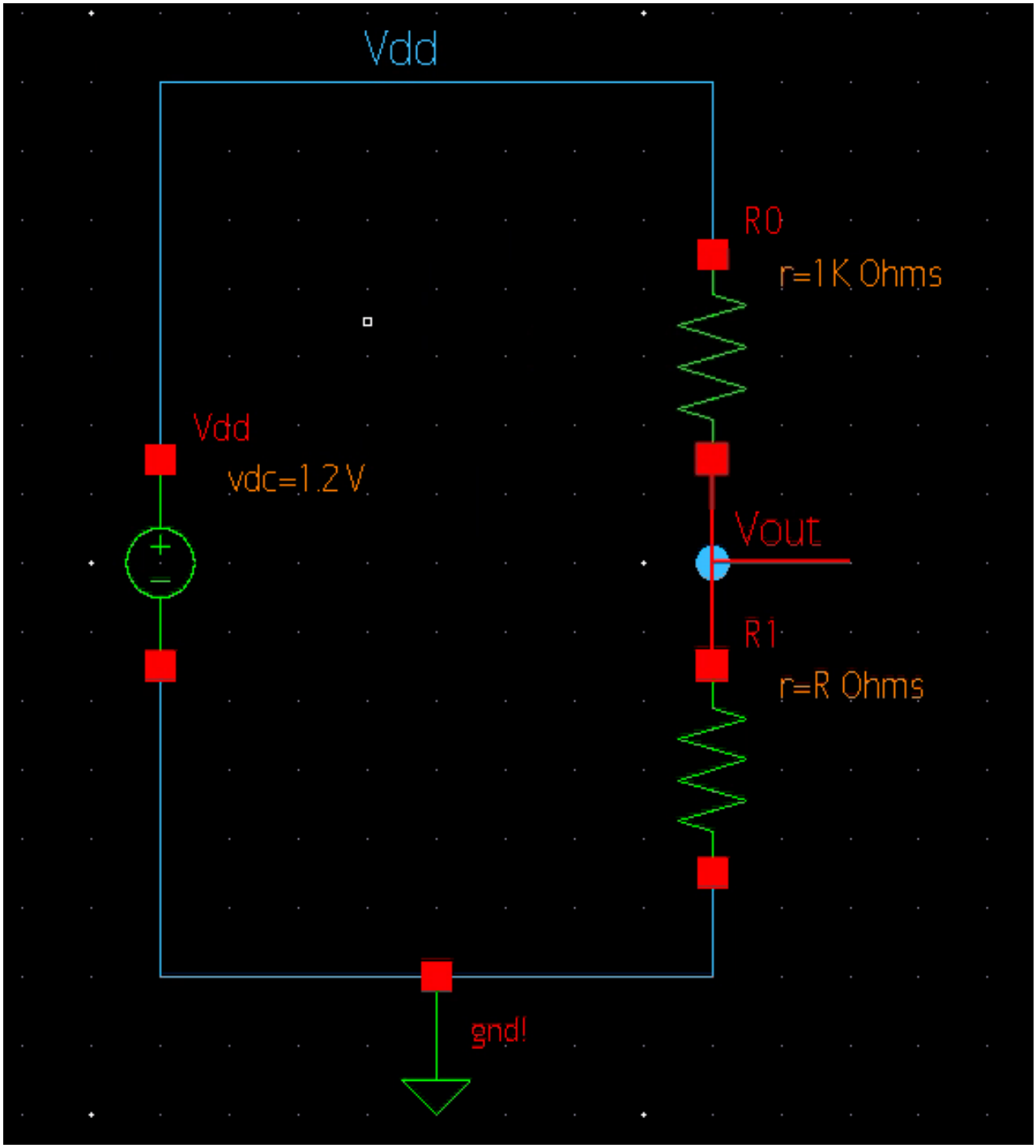
Lab 1: Introduction to Synopsys

by Joseph Yu

Procedure:

Part A: Complete!

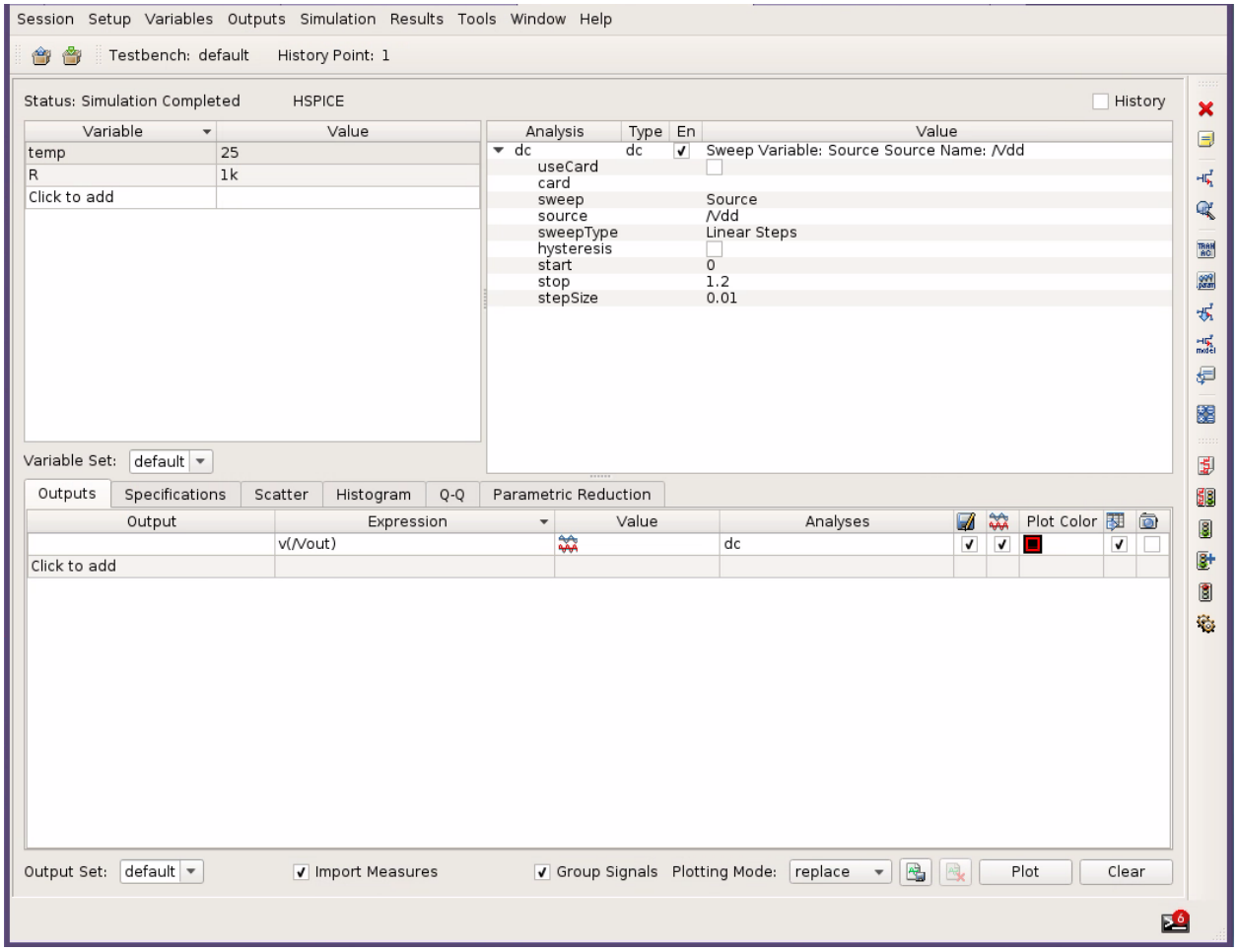
Part B:

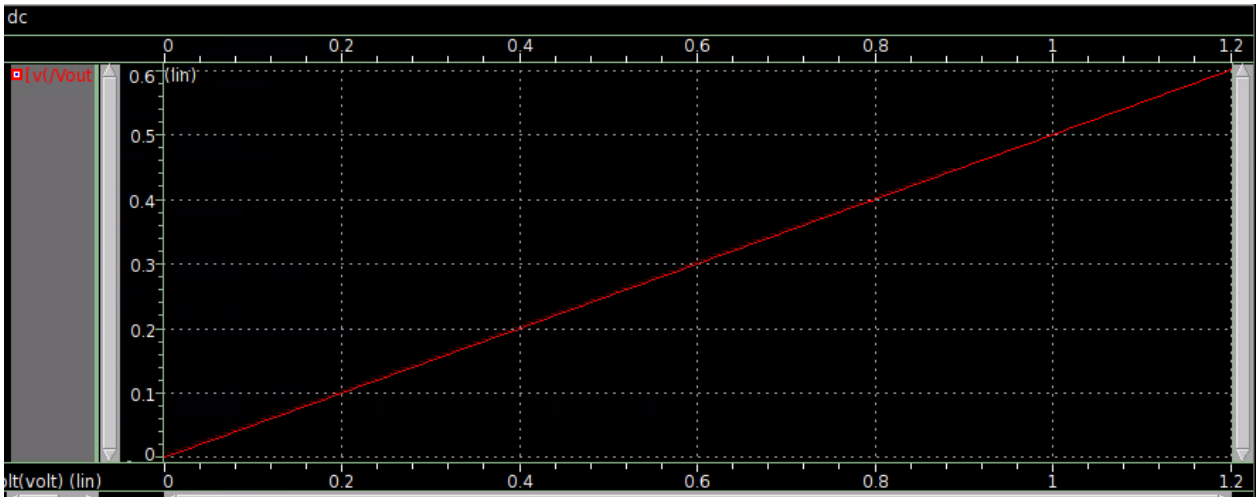


(Next Page)

Source Sweep:

"Vout" is equal to half of "Vdd" for all listed values.



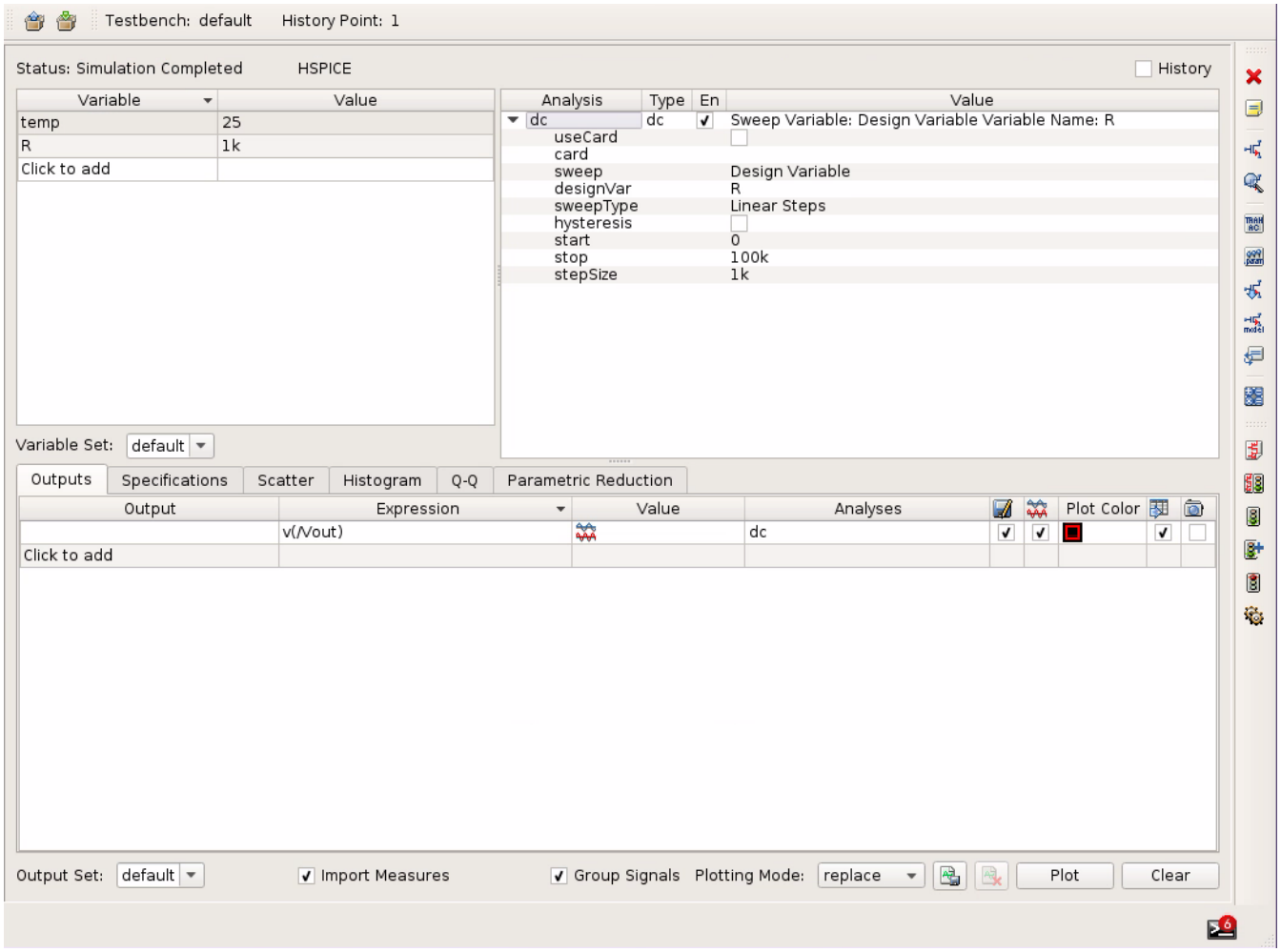


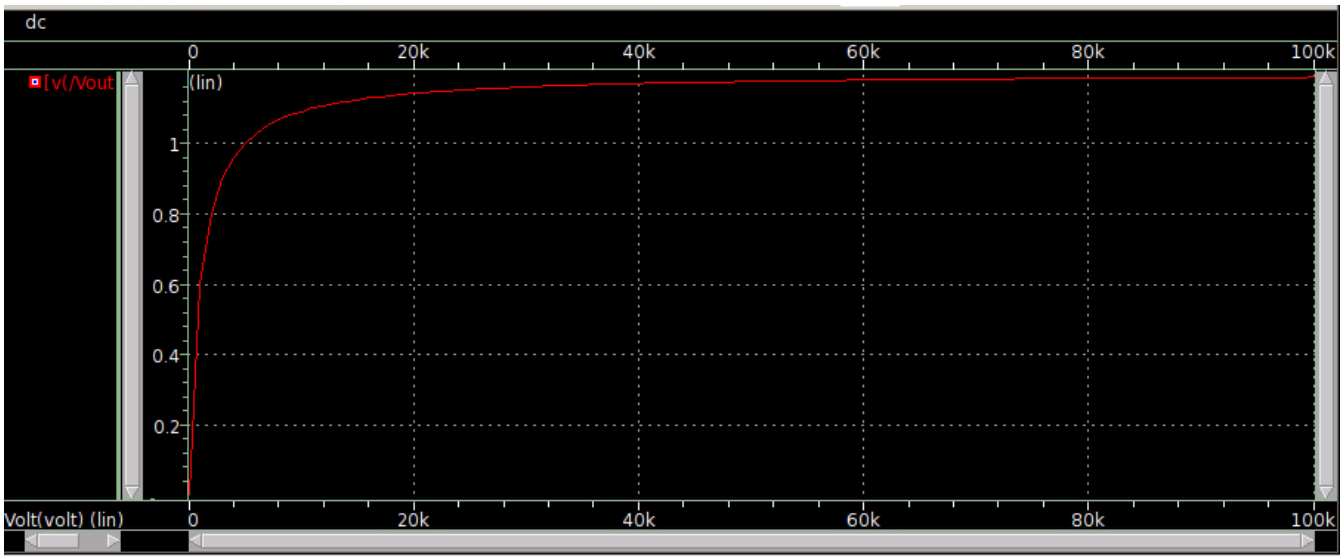
(Next Page)

Resistance Sweep:

When "R" is zero ohms, "Vout" is (apparently) zero volts.

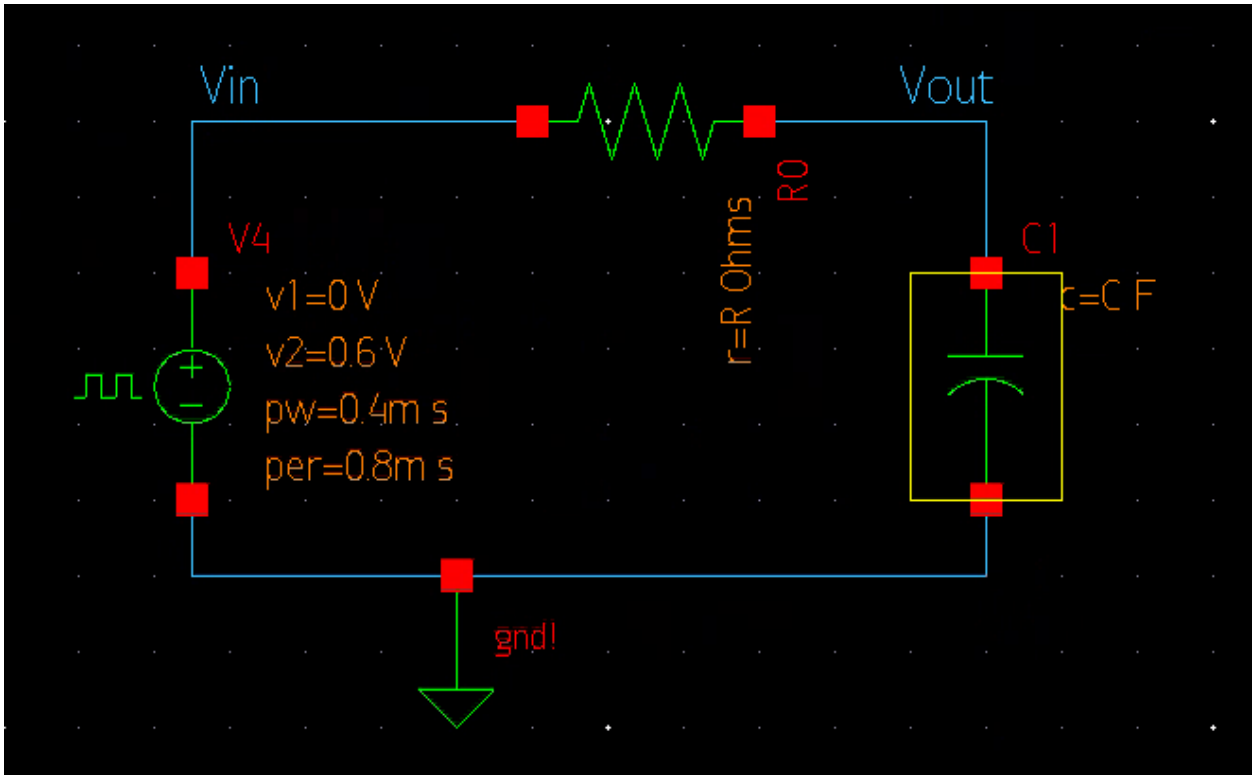
When "R" is 100k ohms, "Vout" is almost equal to the set "Vdd", which is 1.2 volts.





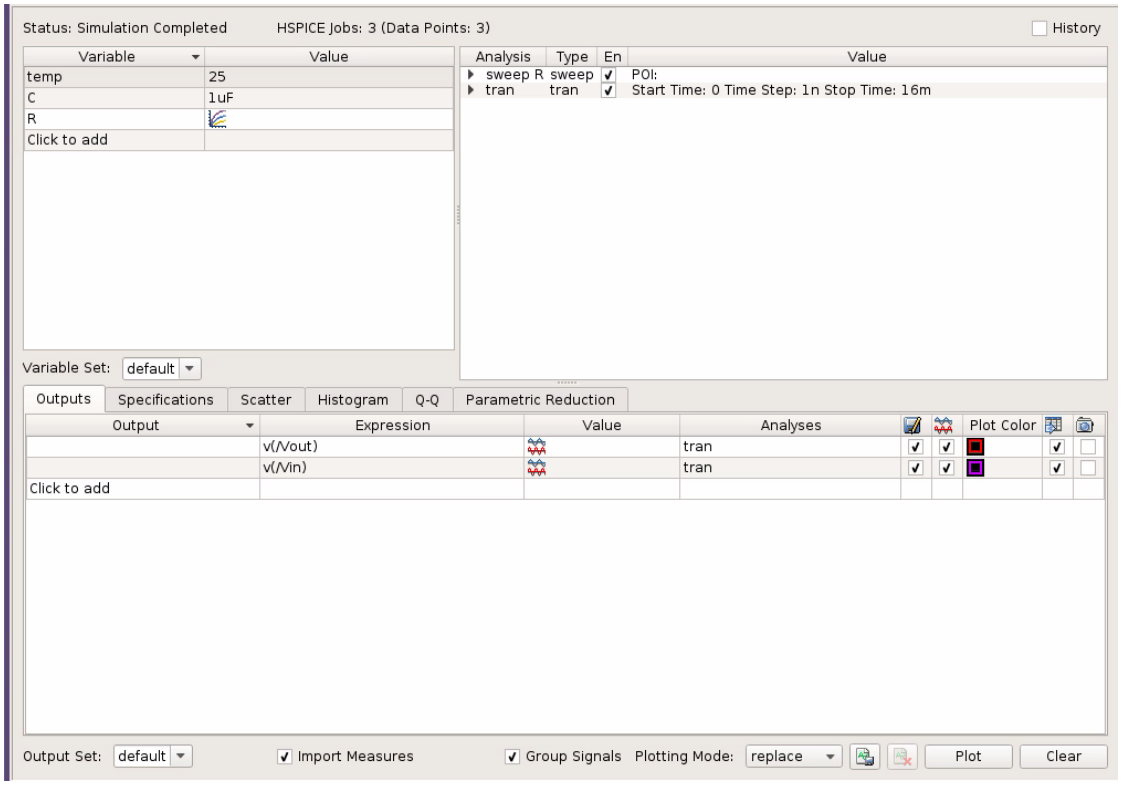
(Next Page)

Part C:

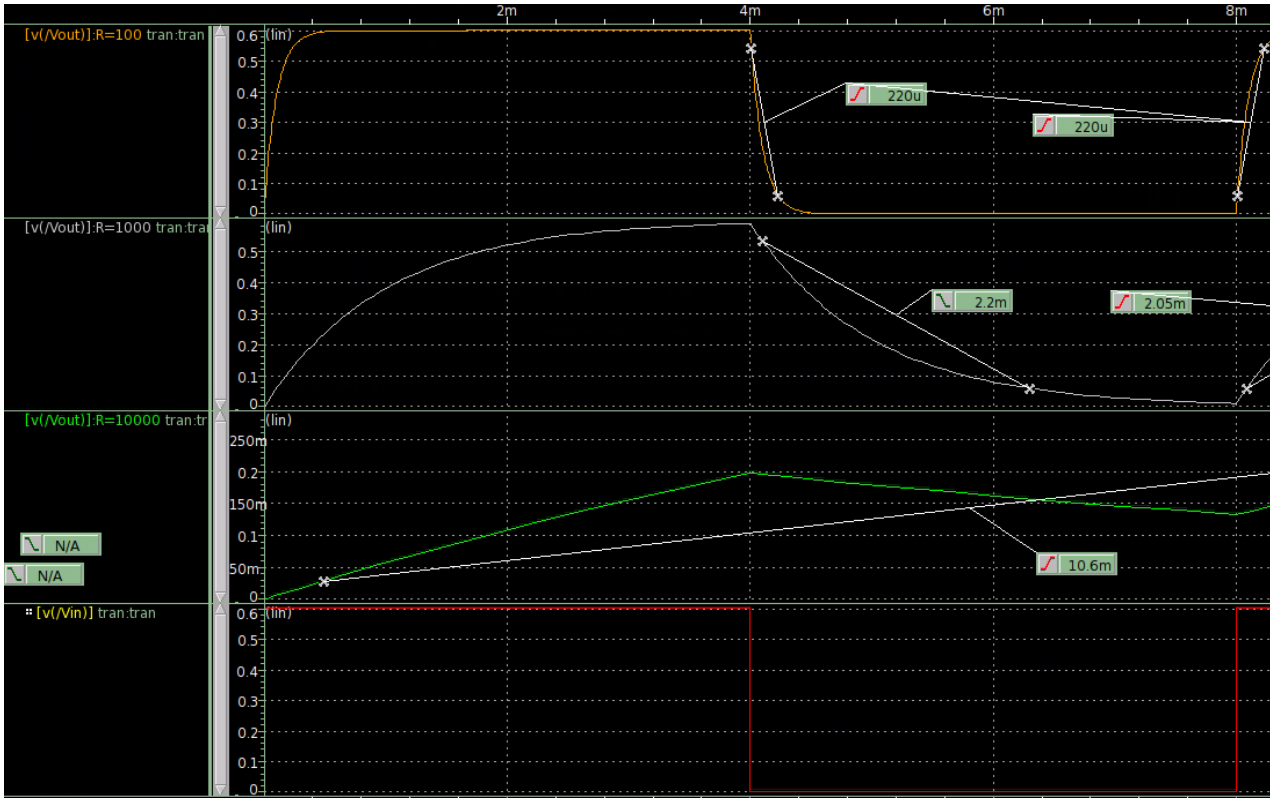


Resistance:

(Measure tool values should be in the graph on the next page.)



(Next Page)



Rise and fall time measures the amount of time it takes for a wave to deviate (through rising or falling) from 10% to 90% of the distance traveled.

In the third case (R = 10kΩ), the value never falls more than 90% of the height of the last wave, so the wave essentially continues to rise indefinitely. Therefore, the rise time is technically infinite, and the fall time doesn't exist.

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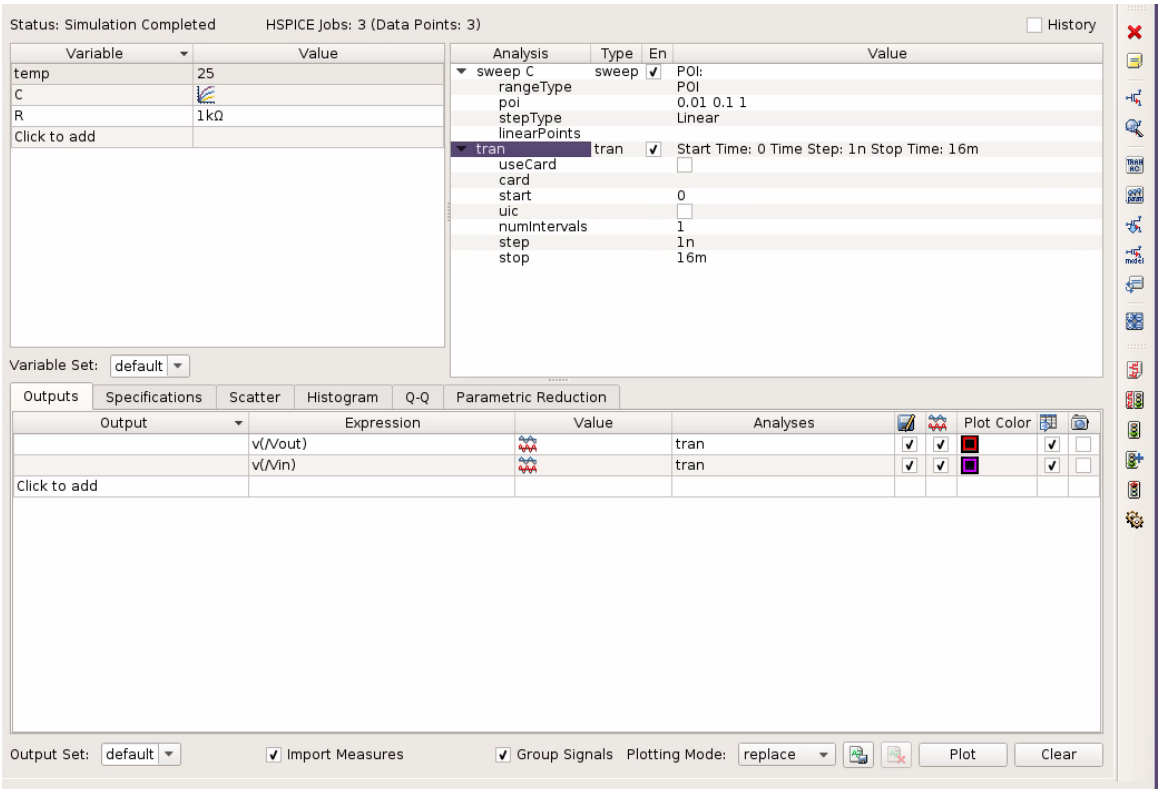
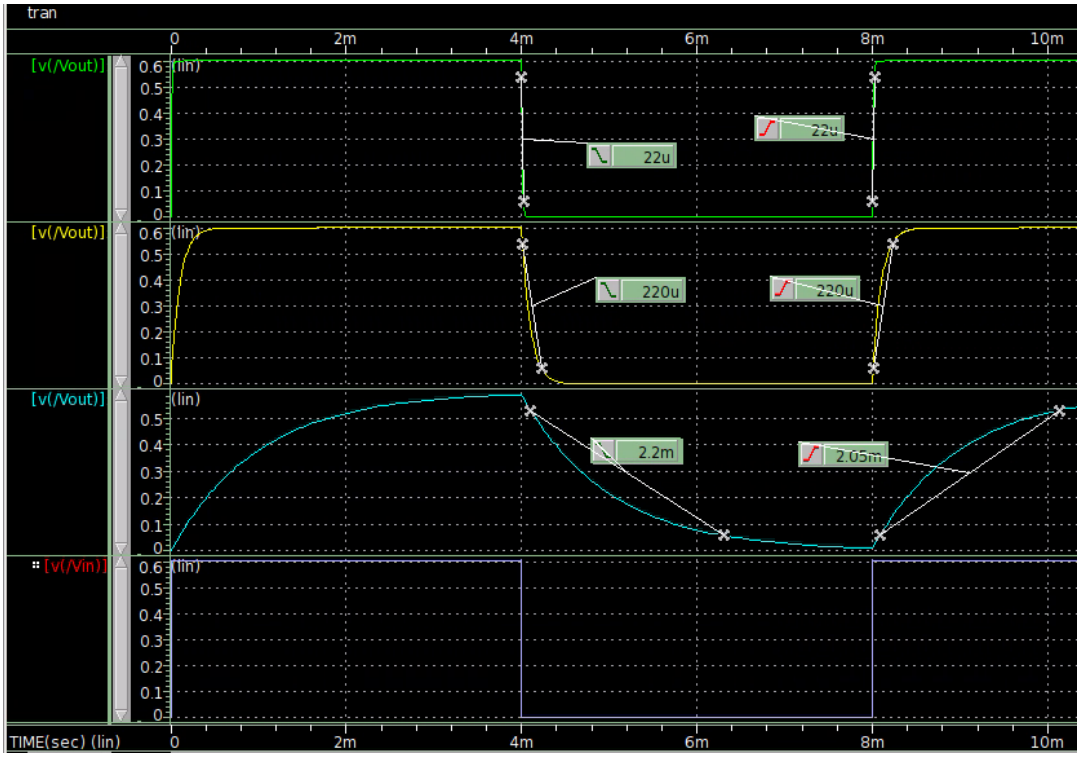
Capacitance:
(Measurements in the graph below).

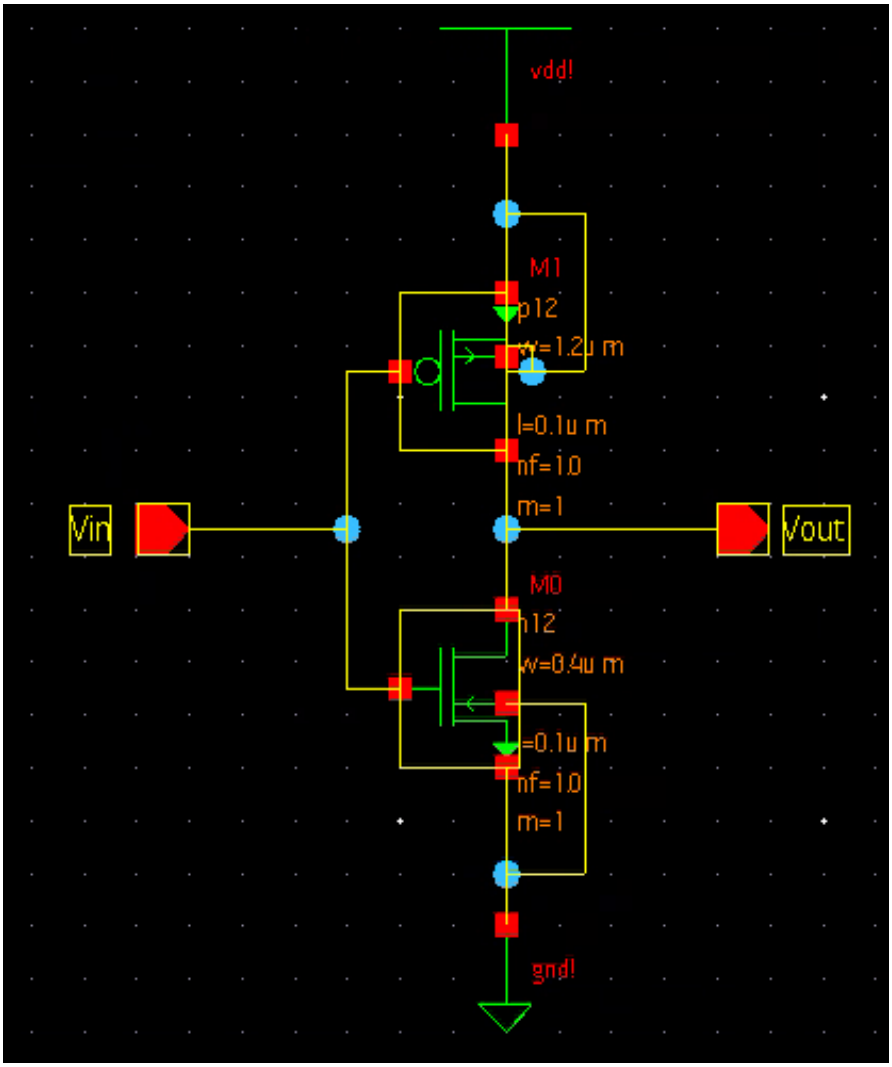


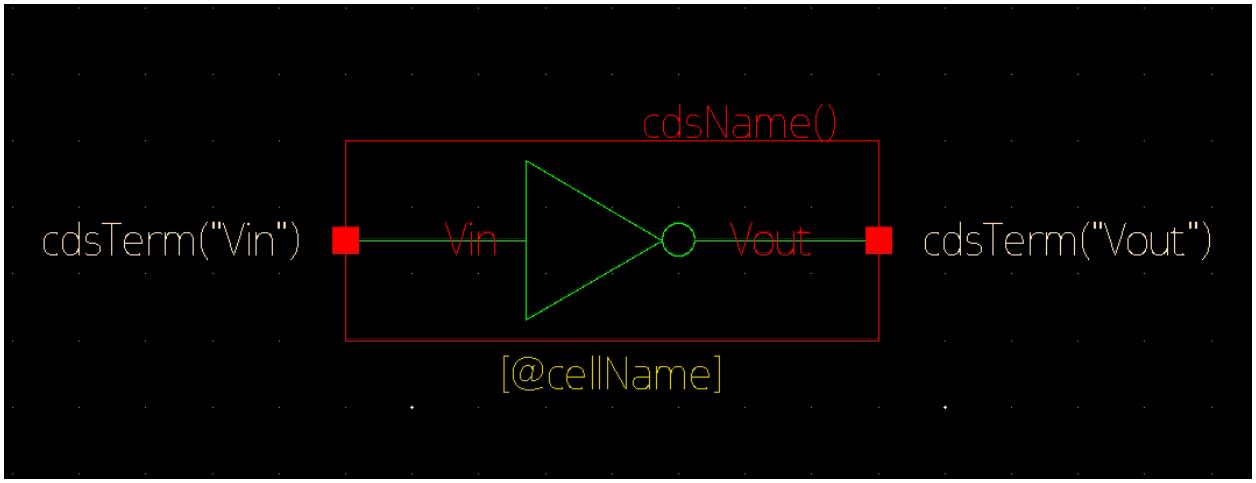


ELEN 153L Lab Report 2

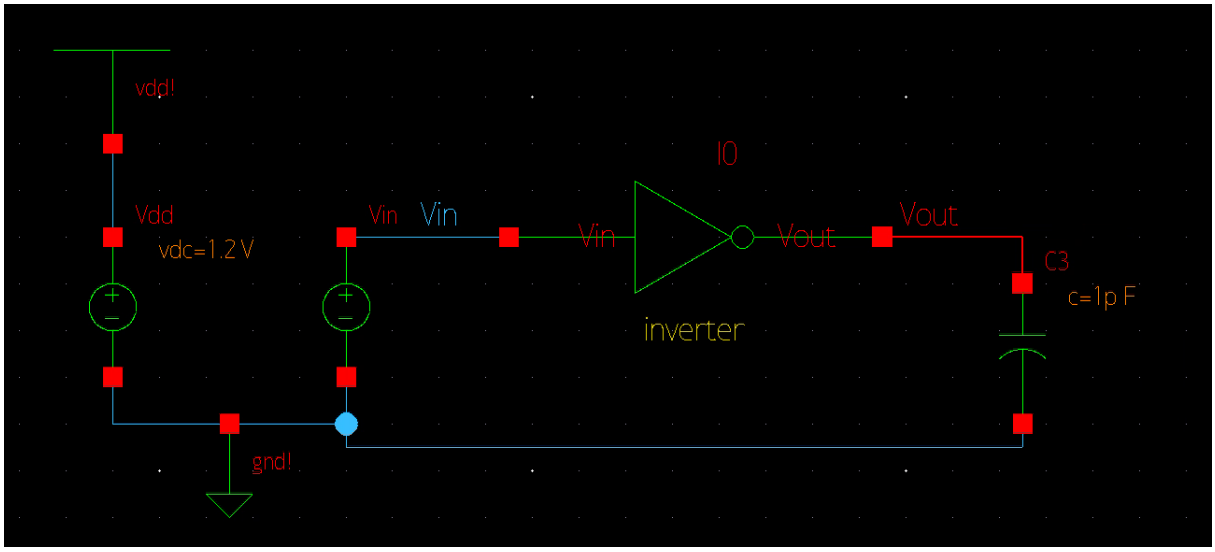
by Joseph Yu

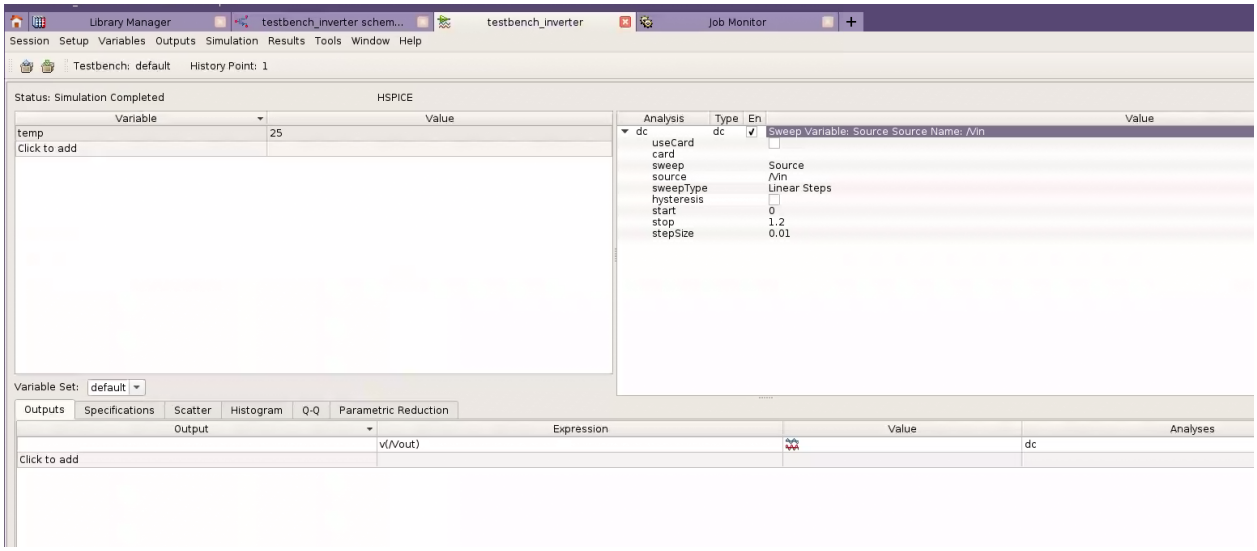
Inverter Schematic/ Symbol (Answers to Lab Questions on Page 6)

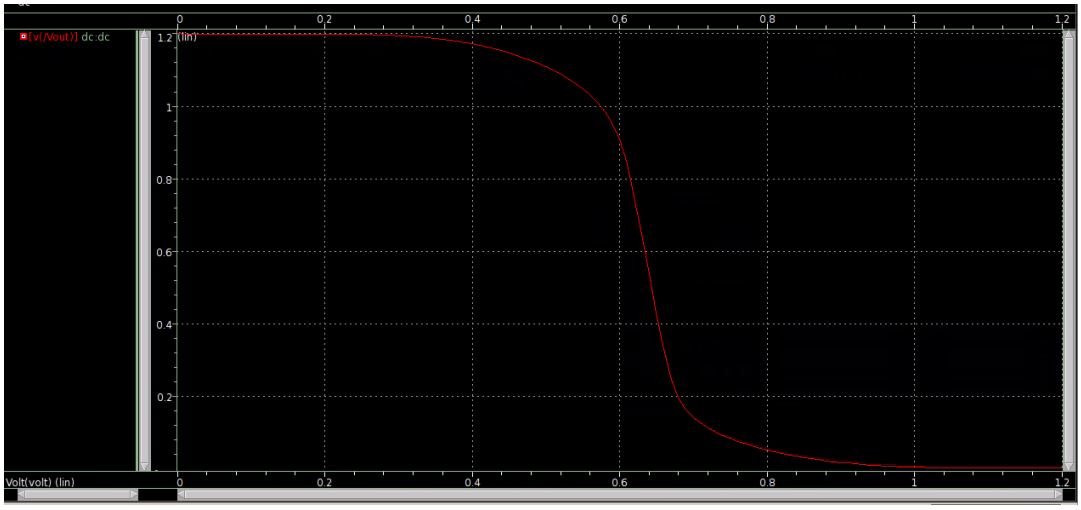




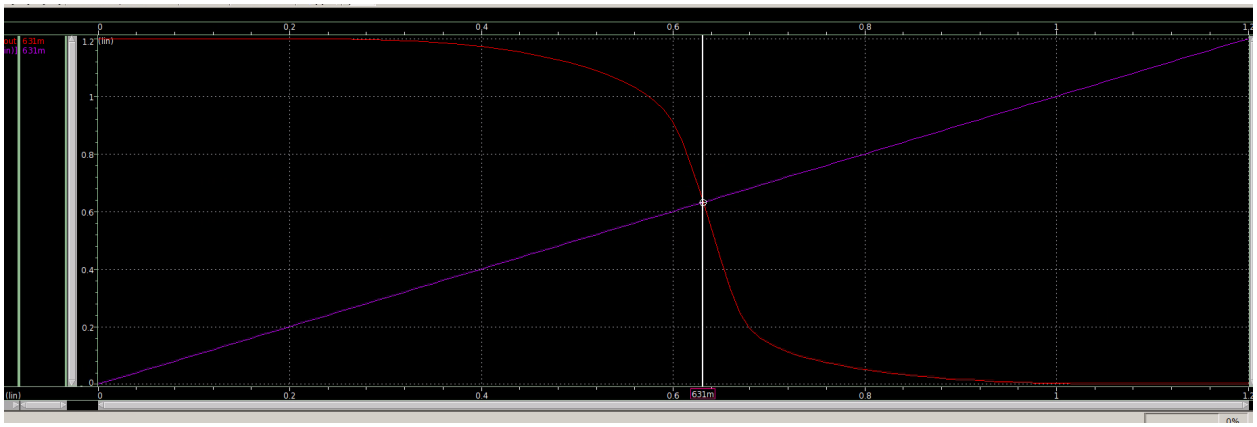
VTC

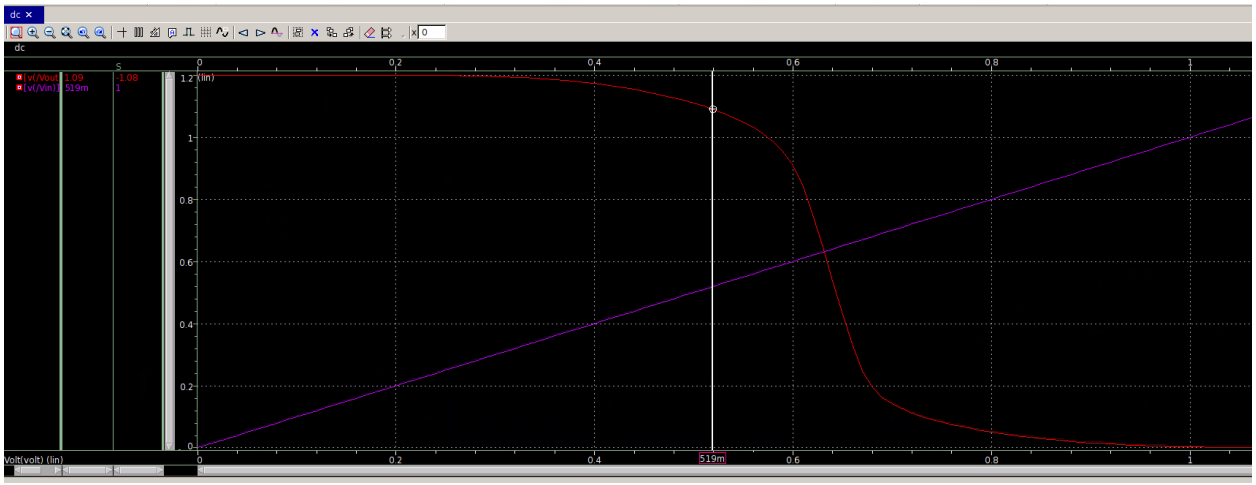

vdd!
Vdd
vdc=1.2 V
Vin
Vin
Vin
I0
Vout
Vout
C3
c=1p F
inverter
gnd!

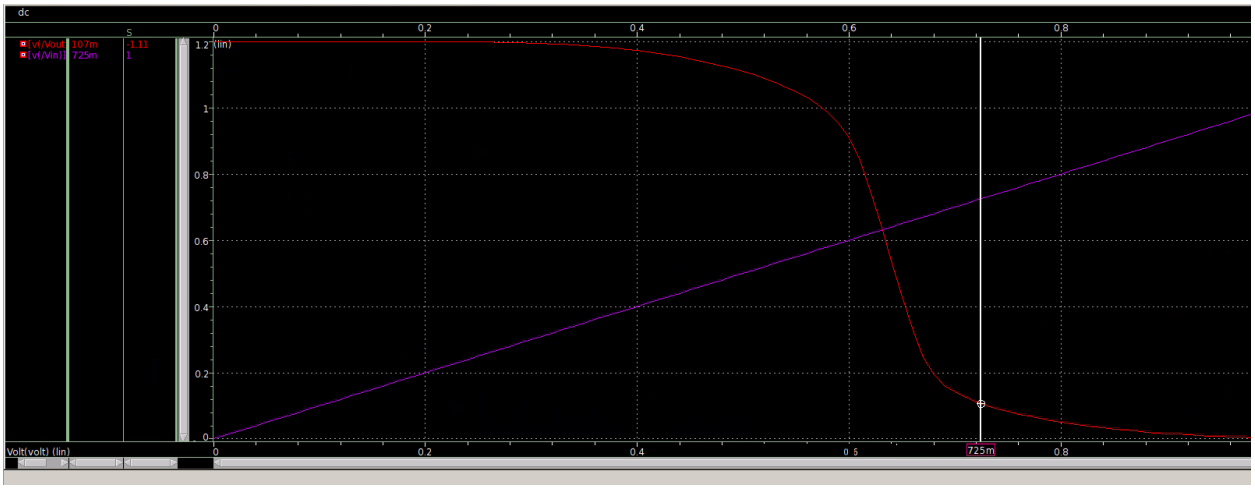

Library Manager
testbench_inverter schem...
testbench_inverter
Job Monitor
Session Setup Variables Outputs Simulation Results Tools Window Help
Testbench: default
History Point: 1
Status: Simulation Completed
HSPICE
Variable
Value
temp
25
Click to add
Analysis
Type
En
Value
dc
dc
Sweep Variable: Source Source Name: /Vin
useCard
card
sweep
Source
source
/Vin
sweepType
Linear Steps
hysteresis
start
0
stop
1.2
stepSize
0.01
Variable Set:
default
Outputs
Specifications
Scatter
Histogram
Q-Q
Parametric Reduction
Output
Expression
Value
Analyses
v(/Vout)
dc
Click to add

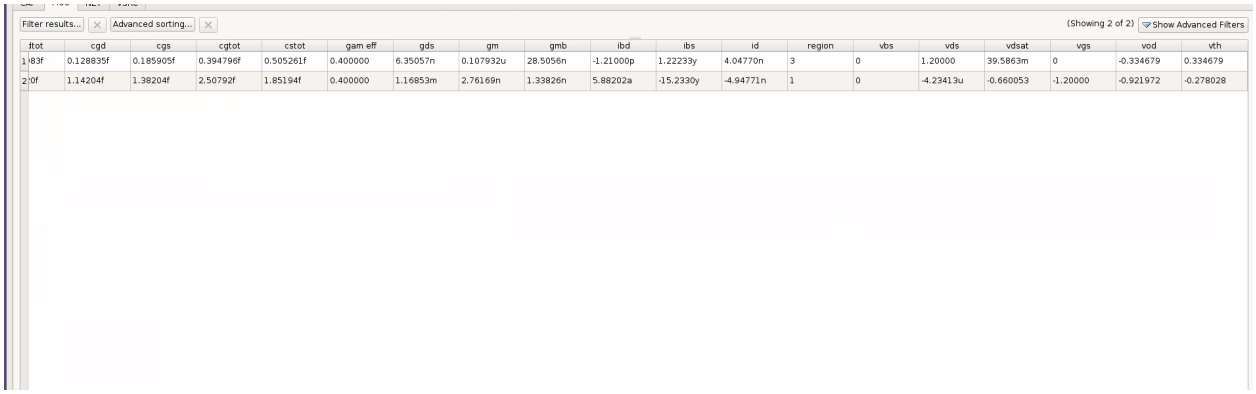

0
0.2
0.4
0.6
0.8
1
1.2
v(/Vout) dc:dc
1.2 (lin)
1
0.8
0.6
0.4
0.2
Volt(volt) (lin)

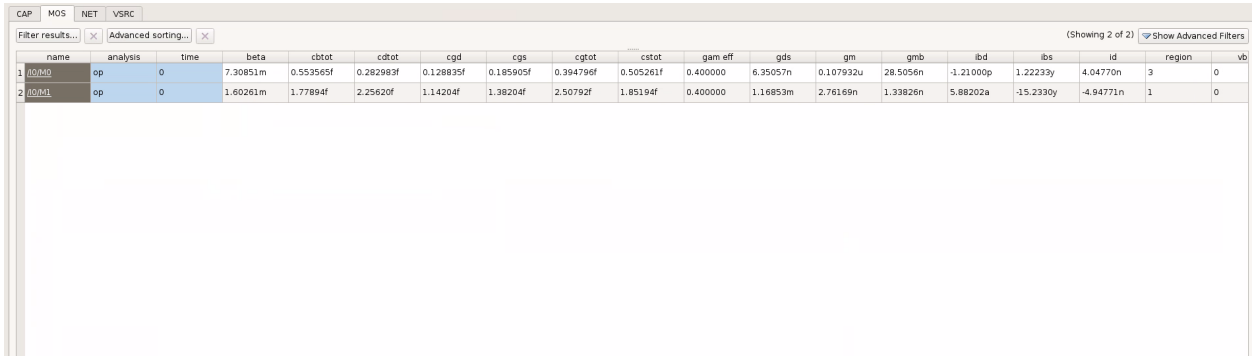
VTC OP


631m
631m
(lin)
631m


dc
dc
v(/Vout) 1.09 -1.08
v(/Vin) 519m 1
(lin)
519m
Volt(volt) (lin)


dc
v(/Vout) 107m 1.11
v(/Vin) 725m 1
(lin)
725m
Volt(volt) (lin)


Filter results...
Advanced sorting...
(Showing 2 of 2)
Show Advanced Filters
itot cgd cgs cgtot cstot gam eff gds gm gmb ibd ibs id region vbs vds vdsat vgs vod vth
1 83f 0.128835f 0.185905f 0.394796f 0.505261f 0.400000 6.35057n 0.107932u 28.5056n -1.21000p 1.22233y 4.04770n 3 0 1.20000 39.5863m 0 -0.334679 0.334679
2 0f 1.14204f 1.38204f 2.50792f 1.85194f 0.400000 1.16853m 2.76169n 1.33826n 5.88202a -15.2330y -4.94771n 1 0 -4.23413u -0.660053 -1.20000 -0.921972 -0.278028


CAP
MOS
NET
VSRC
Filter results...
Advanced sorting...
(Showing 2 of 2)
Show Advanced Filters
name analysis time beta cbtot cdtot cgd cgs cgtot cstot gam eff gds gm gmb ibd ibs id region vb
1 /I0/M0 op 0 7.30851m 0.553565f 0.282983f 0.128835f 0.185905f 0.394796f 0.505261f 0.400000 6.35057n 0.107932u 28.5056n -1.21000p 1.22233y 4.04770n 3 0
2 /I0/M1 op 0 1.60261m 1.77894f 2.25620f 1.14204f 1.38204f 2.50792f 1.85194f 0.400000 1.16853m 2.76169n 1.33826n 5.88202a -15.2330y -4.94771n 1 0

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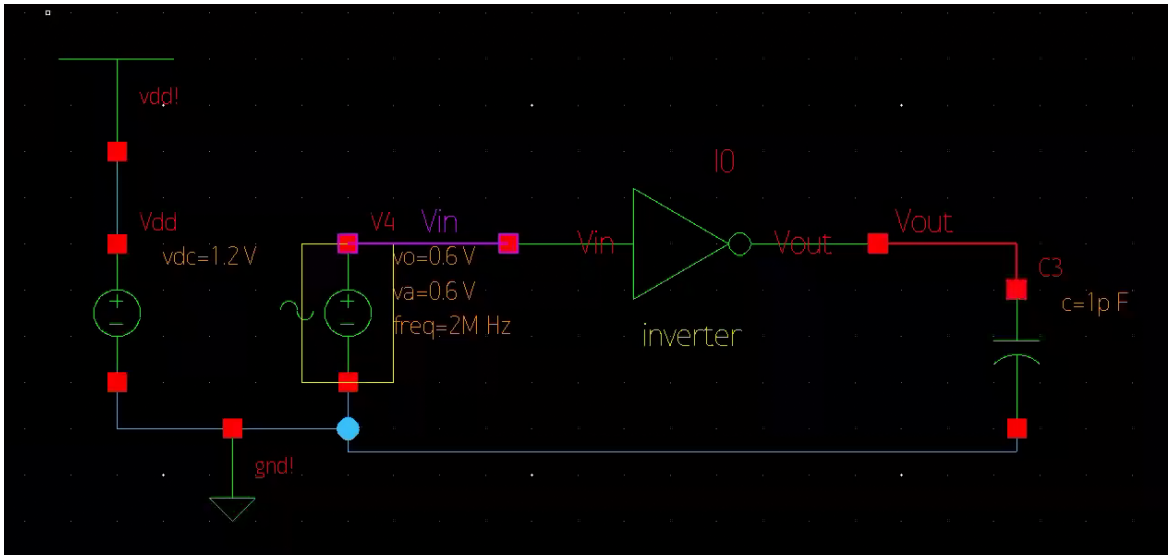
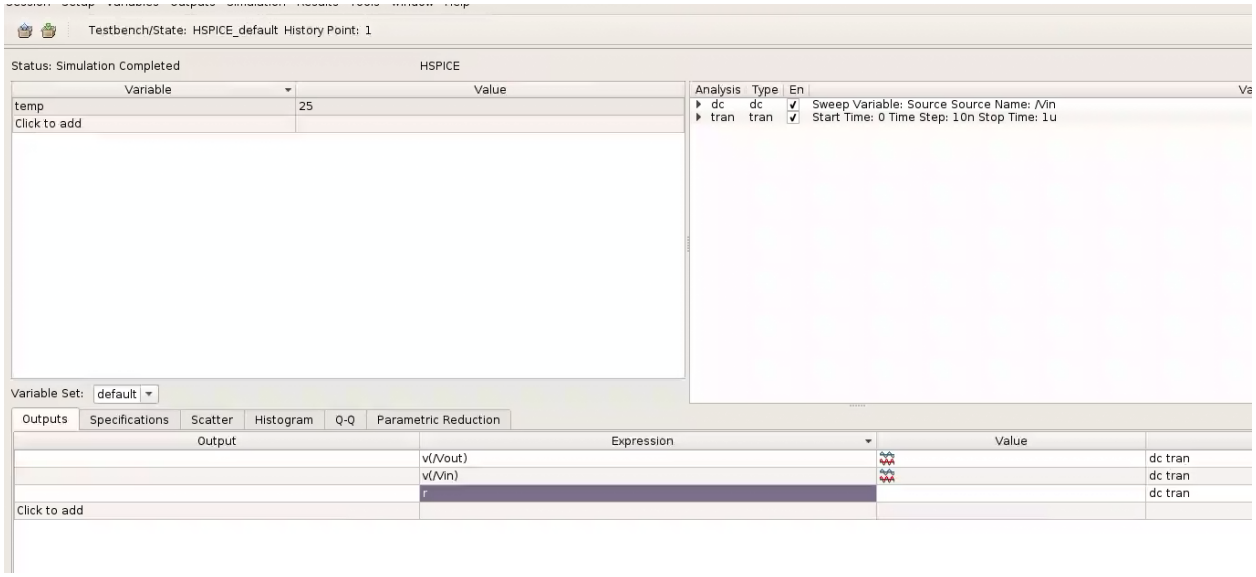
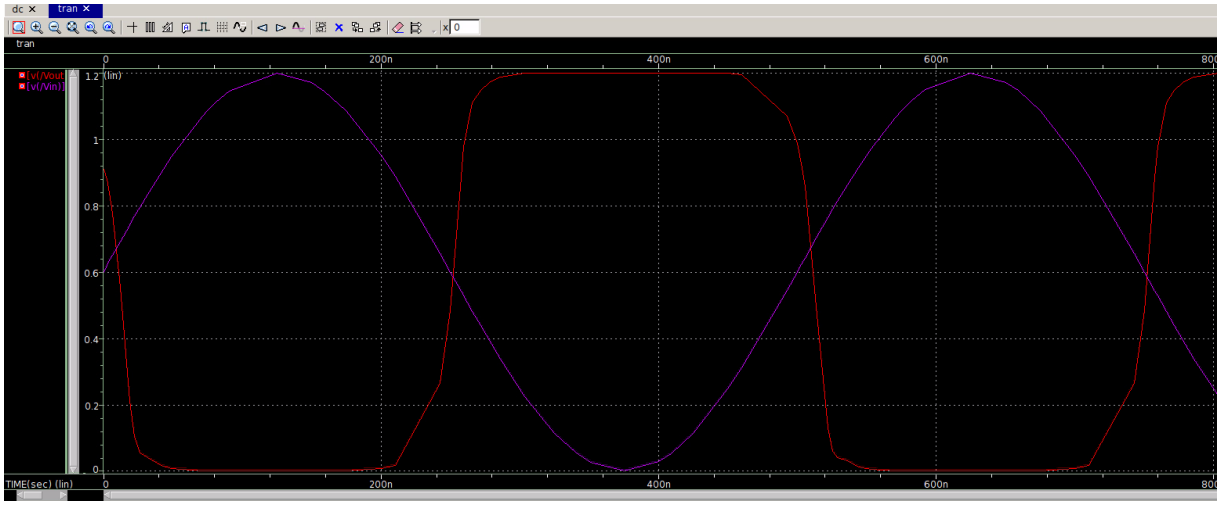
Transient


vdd!
Vdd
vdc=1.2 V
V4
Vin
vo=0.6 V
va=0.6 V
freq=2M Hz
Vin
I0
Vout
inverter
Vout
C3
c=1p F
gnd!


Testbench/State: HSPICE_default History Point: 1
Status: Simulation Completed
HSPICE
Variable
Value
temp
25
Click to add
Analysis
Type
En
dc
dc
Sweep Variable: Source Source Name: /Vin
tran
tran
Start Time: 0 Time Step: 10n Stop Time: 1u
Variable Set:
default
Outputs
Specifications
Scatter
Histogram
Q-Q
Parametric Reduction
Output
Expression
Value
v(/Vout)
dc tran
v(/Vin)
dc tran
dc tran
Click to add


dc
tran
tran
v(/Vout)
v(/Vin)
0
200n
400n
600n
1.2 (lin)
1
0.8
0.6
0.4
0.2
0
TIME(sec) (lin)

Lab Questions:

Step 3 in Lab Procedure:
> Vm = 0.631 V
> Vout = -1 → Vin = 0.519, 0.725

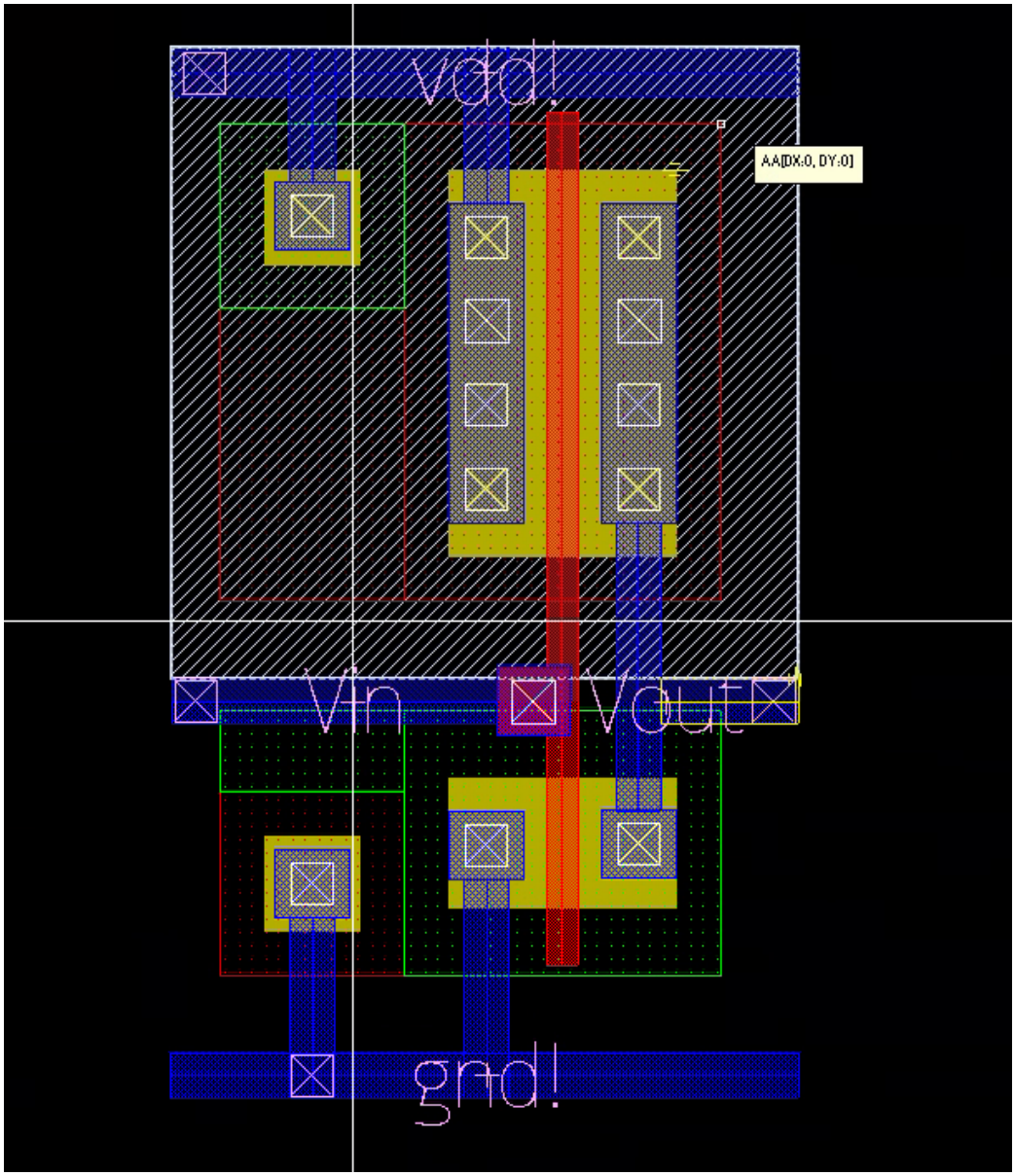
Questions concerning Lab Procedure:

a) NMOS: length = 0.1 um (micrometers), width = 0.4 um
   PMOS: length = 0.1 um, width = 1.2 um
b) Vm = 0.631 V
   Voh = 1.09 V
   Vil = 0.519 V
   Vol = 0.107 V
   Vih = 0.725 V
   (Screenshots on page 3)

Conclusions:
In this lab, we created a symbol for the logical negator using a PMOS and a NMOS in Synopsys Custom Compiler and performed some simulations (VTC and transient) using the new symbol. The intricacies and challenges that we faced during the lab allowed us to adapt to the new software and understand the relations between logical gates and the semiconductor transistors they are composed of.

[ELEN153L] Lab Report 3

by Joseph Yu



Procedure Step 1:

1.

NWELL: N-Well. NIMP: N+ Implantation PIMP: P+ Implantation DIFF: Diffusion PO: Poly Silicon	M1: Metal 1 M2: Metal 2 DIFFCON: Diffusion Contact POLYCON: Poly Contact

2. Length (Y-Axis) = 0.1 um
   PMOS, NMOS Width (X-Axis) = 1.2 um, 0.4 um

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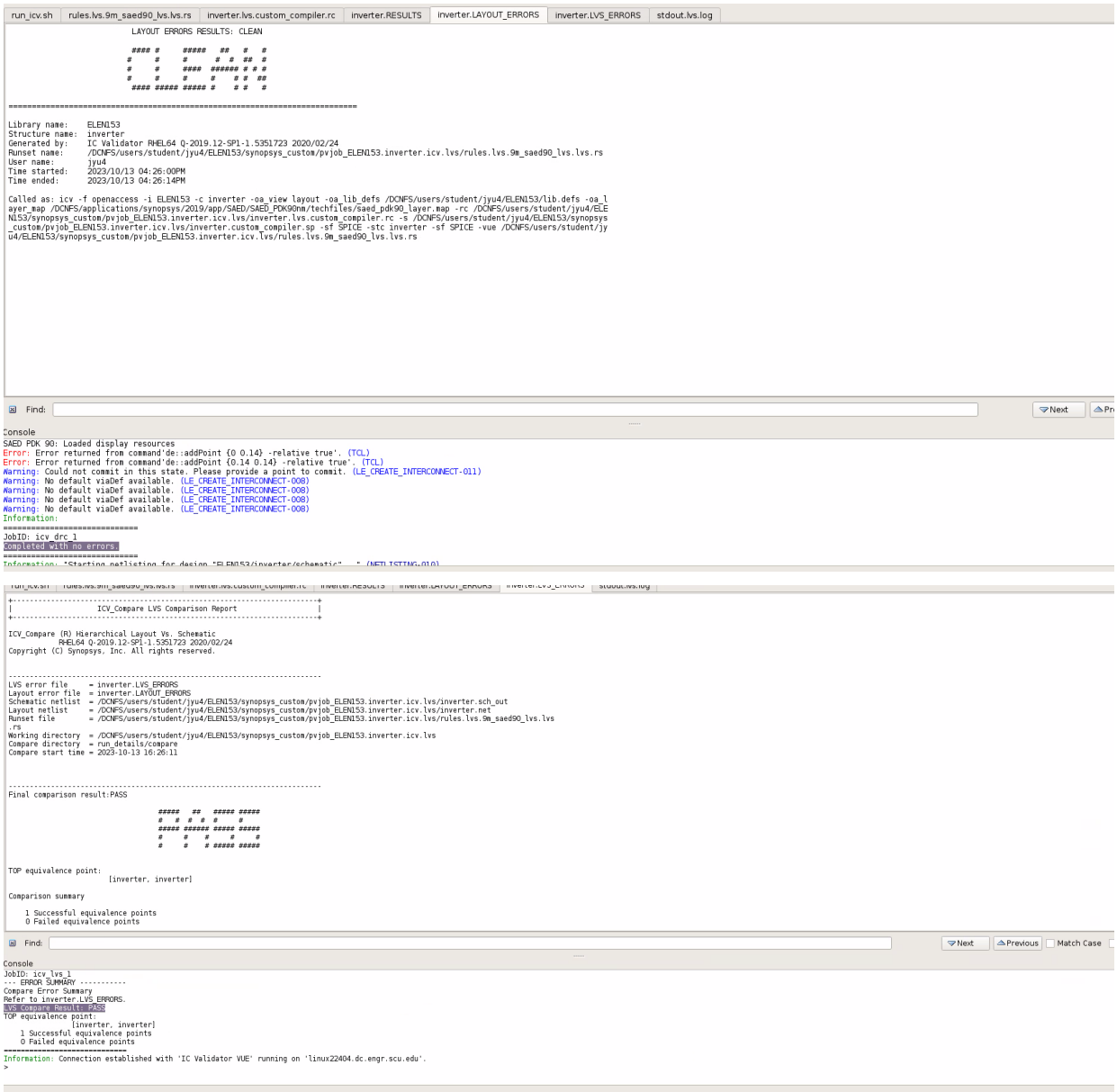
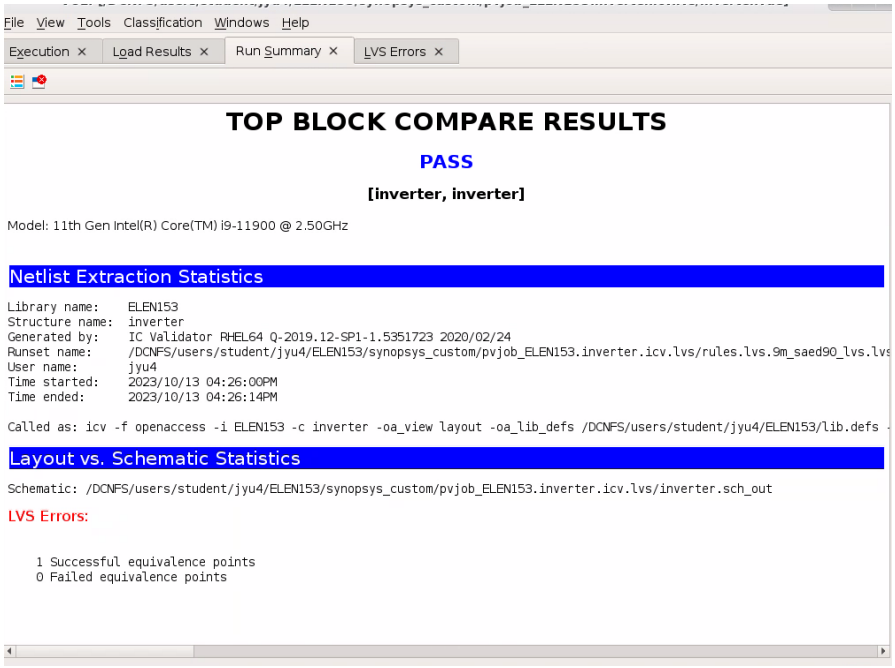

run_icv.sh
rules.lvs.9m_saed90_lvs.lvs.rs
inverter.lvs.custom_compiler.rc
inverter.RESULTS
inverter.LAYOUT_ERRORS
inverter.LVS_ERRORS
stdout.lvs.log
LAYOUT ERRORS RESULTS: CLEAN
Library name: ELEN153
Structure name: inverter
Generated by: IC Validator RHEL64 Q-2019.12-SP1-1.5351723 2020/02/24
Runset name: /DCNFS/users/student/jyu4/ELEN153/synopsys_custom/pvjob_ELEN153.inverter.icv.lvs/rules.lvs.9m_saed90_lvs.lvs.rs
User name: jyu4
Time started: 2023/10/13 04:26:00PM
Time ended: 2023/10/13 04:26:14PM
Called as: icv -f openaccess -i ELEN153 -c inverter -oa_view layout -oa_lib_defs /DCNFS/users/student/jyu4/ELEN153/lib.defs -oa_layer_map /DCNFS/applications/synopsys/2019/app/SAED/SAED_PDK90nm/techfiles/Saed_pdk90_layer.map -rc /DCNFS/users/student/jyu4/ELEN153/synopsys_custom/pvjob_ELEN153.inverter.icv.lvs/inverter.lvs.custom_compiler.rc -s /DCNFS/users/student/jyu4/ELEN153/synopsys_custom/pvjob_ELEN153.inverter.icv.lvs/inverter.custom_compiler.sp -sf SPICE -stc inverter -sf SPICE -vue /DCNFS/users/student/jyu4/ELEN153/synopsys_custom/pvjob_ELEN153.inverter.icv.lvs/rules.lvs.9m_saed90_lvs.lvs.rs
Find:
Next
Console
SAED PDK 90: Loaded display resources
Error: Error returned from command'de::addPoint {0 0.14} -relative true'. (TCL)
Error: Error returned from command'de::addPoint {0.14 0.14} -relative true'. (TCL)
Warning: Could not commit in this state. Please provide a point to commit. (LE_CREATE_INTERCONNECT-011)
Warning: No default viaDef available. (LE_CREATE_INTERCONNECT-008)
Warning: No default viaDef available. (LE_CREATE_INTERCONNECT-008)
Warning: No default viaDef available. (LE_CREATE_INTERCONNECT-008)
Warning: No default viaDef available. (LE_CREATE_INTERCONNECT-008)
Information:
JobID: icv_drc_1
Completed with no errors
Information: "Starting netlisting for design "ELEN153/inverter/schematic" ..." (NETLISTING-010)
ICV_Compare LVS Comparison Report
ICV_Compare (R) Hierarchical Layout Vs. Schematic
RHEL64 Q-2019.12-SP1-1.5351723 2020/02/24
Copyright (C) Synopsys, Inc. All rights reserved.
LVS error file = inverter.LVS_ERRORS
Layout error file = inverter.LAYOUT_ERRORS
Schematic netlist = /DCNFS/users/student/jyu4/ELEN153/synopsys_custom/pvjob_ELEN153.inverter.icv.lvs/inverter.sch_out
Layout netlist = /DCNFS/users/student/jyu4/ELEN153/synopsys_custom/pvjob_ELEN153.inverter.icv.lvs/inverter.net
Runset file = /DCNFS/users/student/jyu4/ELEN153/synopsys_custom/pvjob_ELEN153.inverter.icv.lvs/rules.lvs.9m_saed90_lvs.lvs.rs
Working directory = /DCNFS/users/student/jyu4/ELEN153/synopsys_custom/pvjob_ELEN153.inverter.icv.lvs
Compare directory = run_details/compare
Compare start time = 2023-10-13 16:26:11
Final comparison result:PASS
TOP equivalence point:
[inverter, inverter]
Comparison summary
1 Successful equivalence points
0 Failed equivalence points
Find:
Next
Previous
Match Case
Console
JobID: icv_lvs_1
--- ERROR SUMMARY ----------
Compare Error Summary
Refer to inverter.LVS_ERRORS.
LvsCompare Result1:PASS
TOP equivalence point:
[inverter, inverter]
1 Successful equivalence points
0 Failed equivalence points
Information: Connection established with 'IC Validator VUE' running on 'linux22404.dc.engr.scu.edu'.

(Next Page)

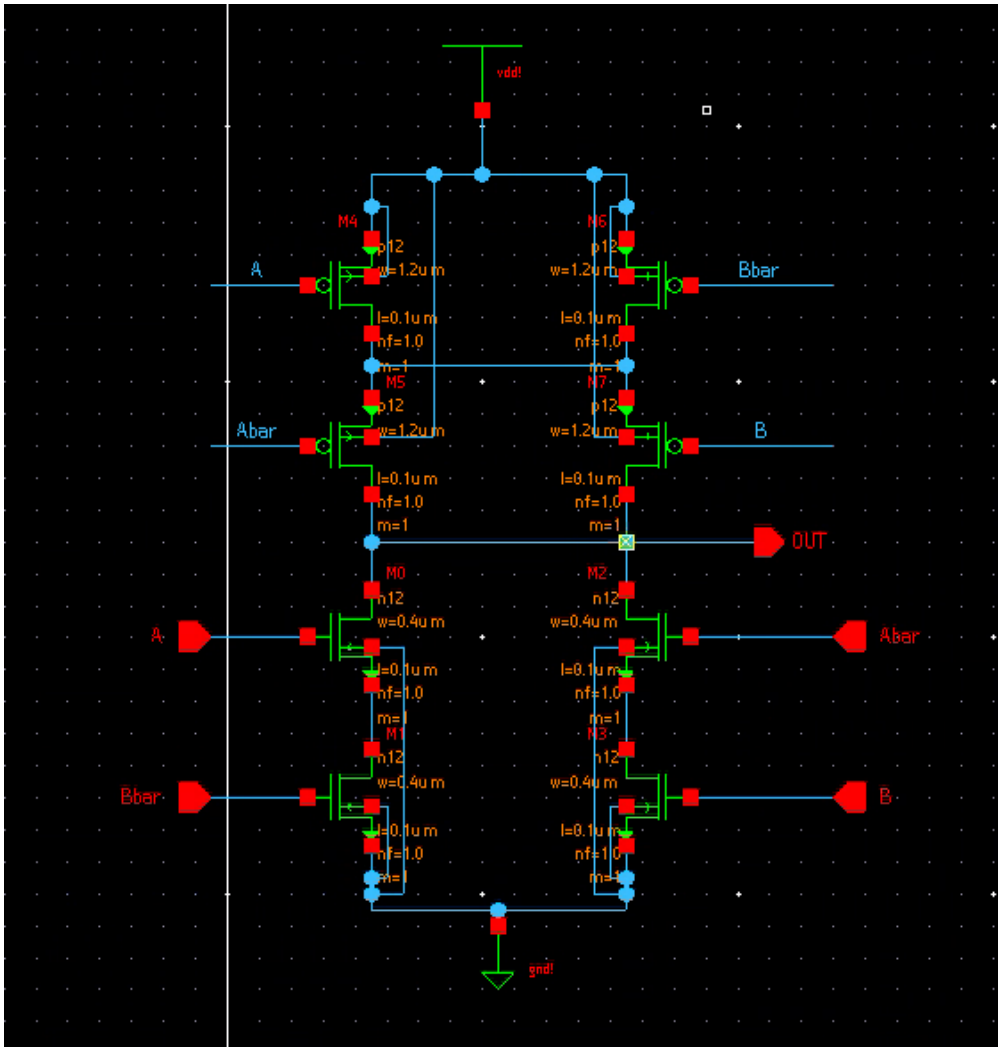


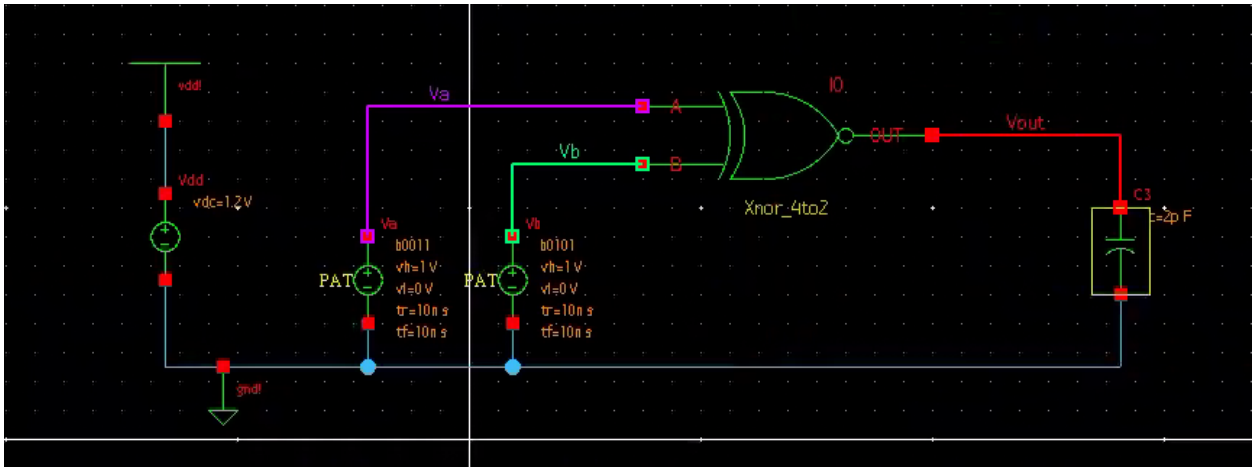
Conclusion:

Today, I was able to create the layout of an inverter in Synopsis Lab. It was able to pass all verification tests and further familiarize me with the inner workings of logical gates in relation to its metallic and transistor components. Nothing terrible happened.

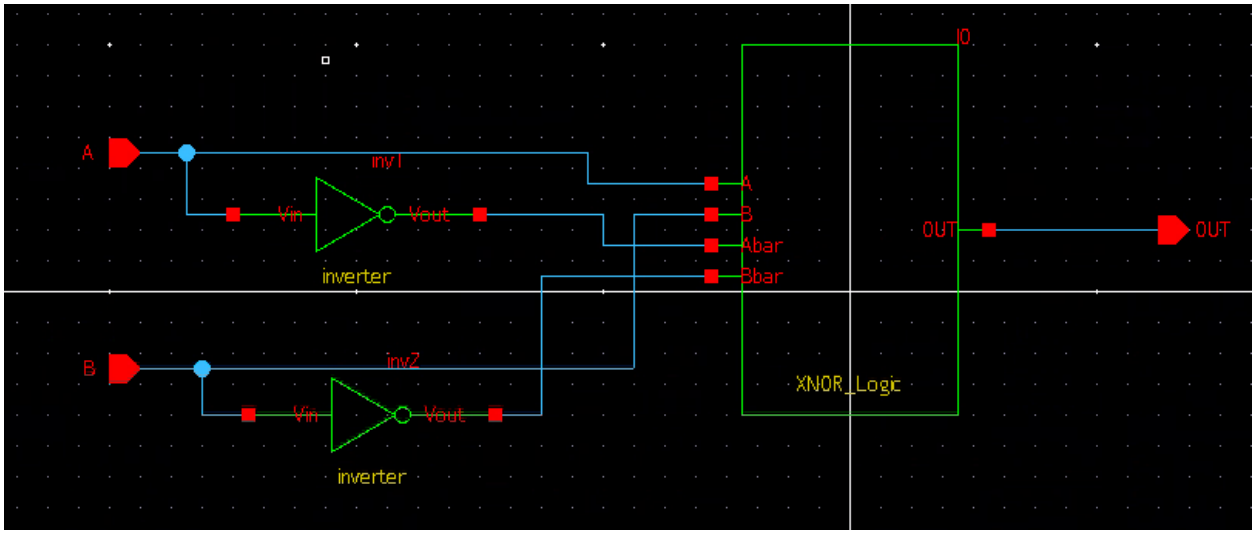
Lab 4 Report
by Joseph Yu

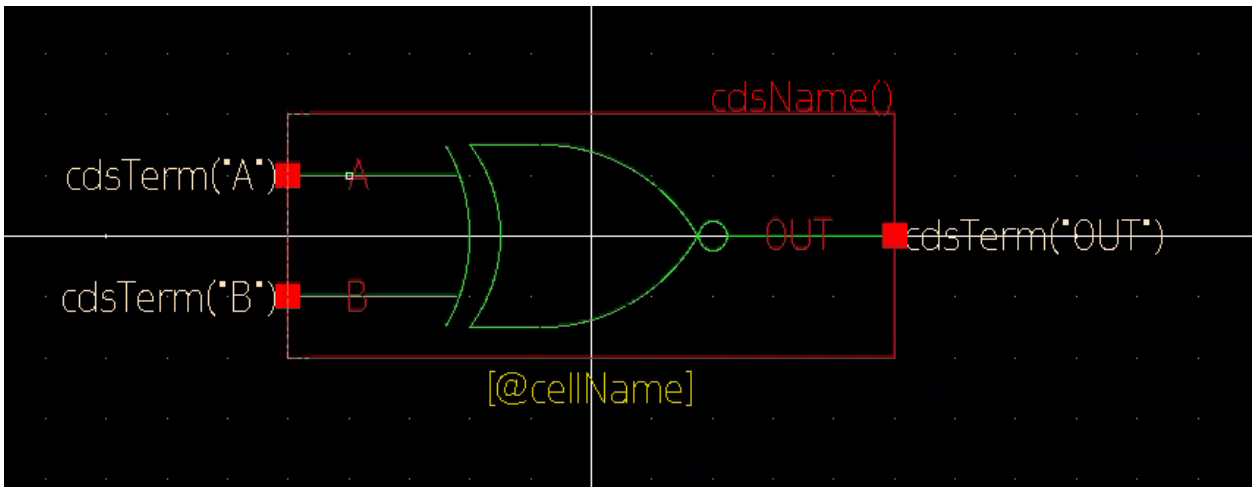
Pictures: (Answer to Procedure Questions on Page 4)

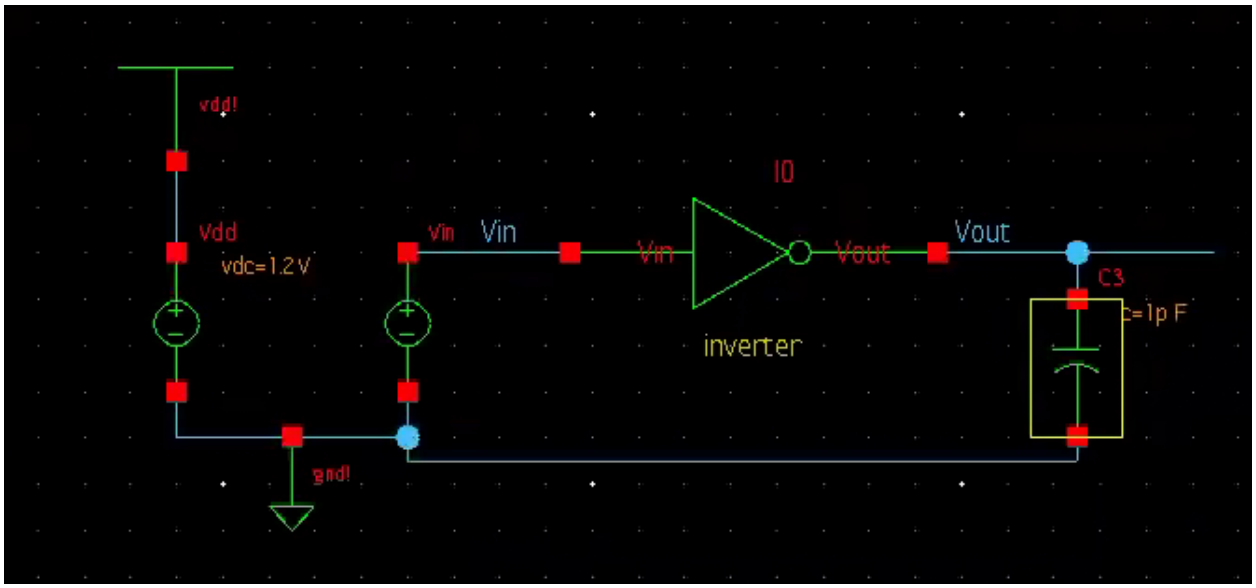




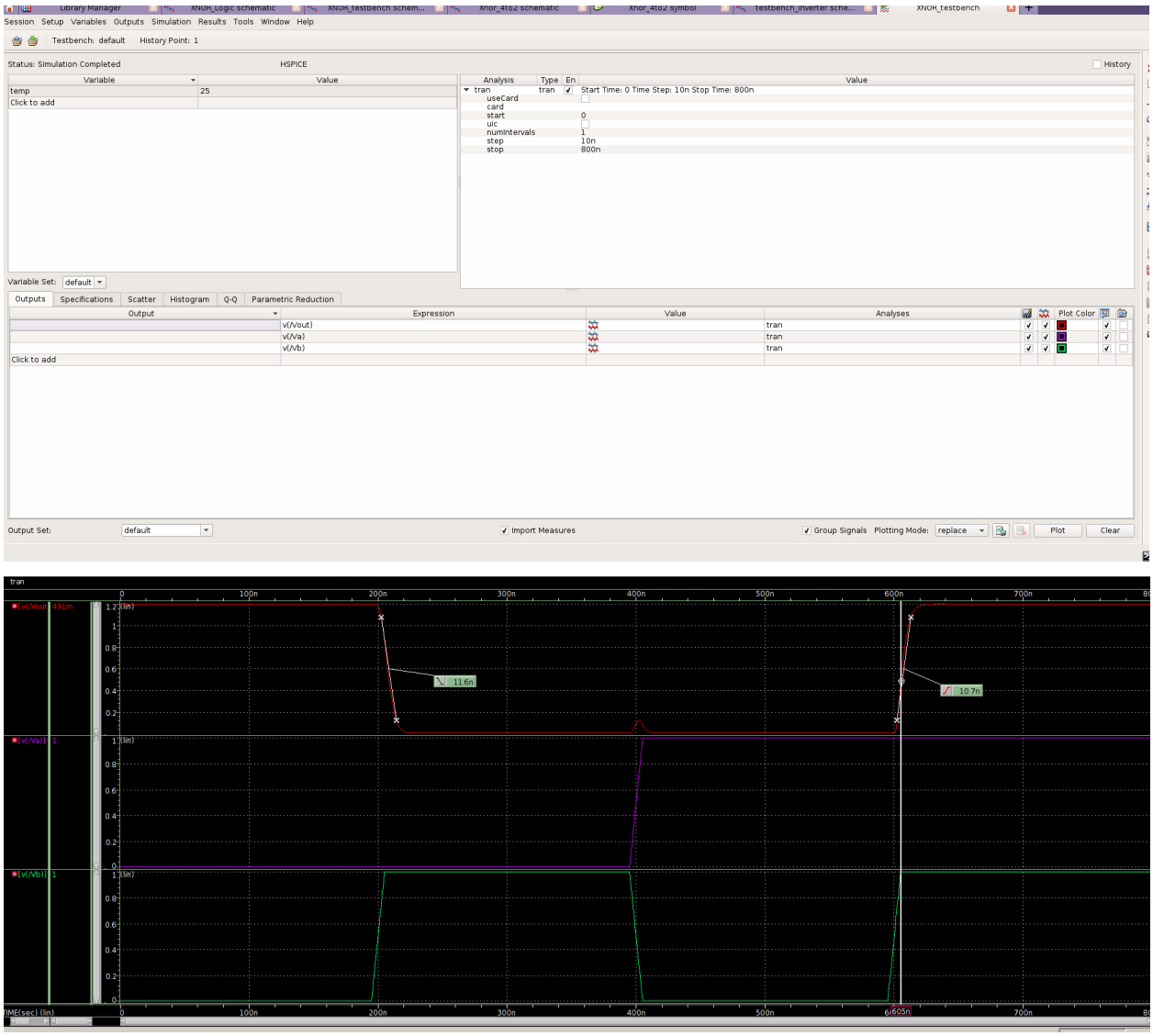
(Next Page)


A
inv1
Vin
Vout
inverter
B
inv2
Vin
Vout
inverter
I0
A
B
Abar
Bbar
XNOR_Logic
OUT
OUT


cdsName()
cdsTerm("A")
A
cdsTerm("B")
B
OUT
cdsTerm("OUT")
[@cellName]


vdd!
Vdd
vdc=1.2 V
gnd!
Vin
Vin
I0
Vin
Vout
inverter
Vout
C3

(Next Page)



(Caption: Above measurements depicted are 11.6 ns and 10.7 ns)

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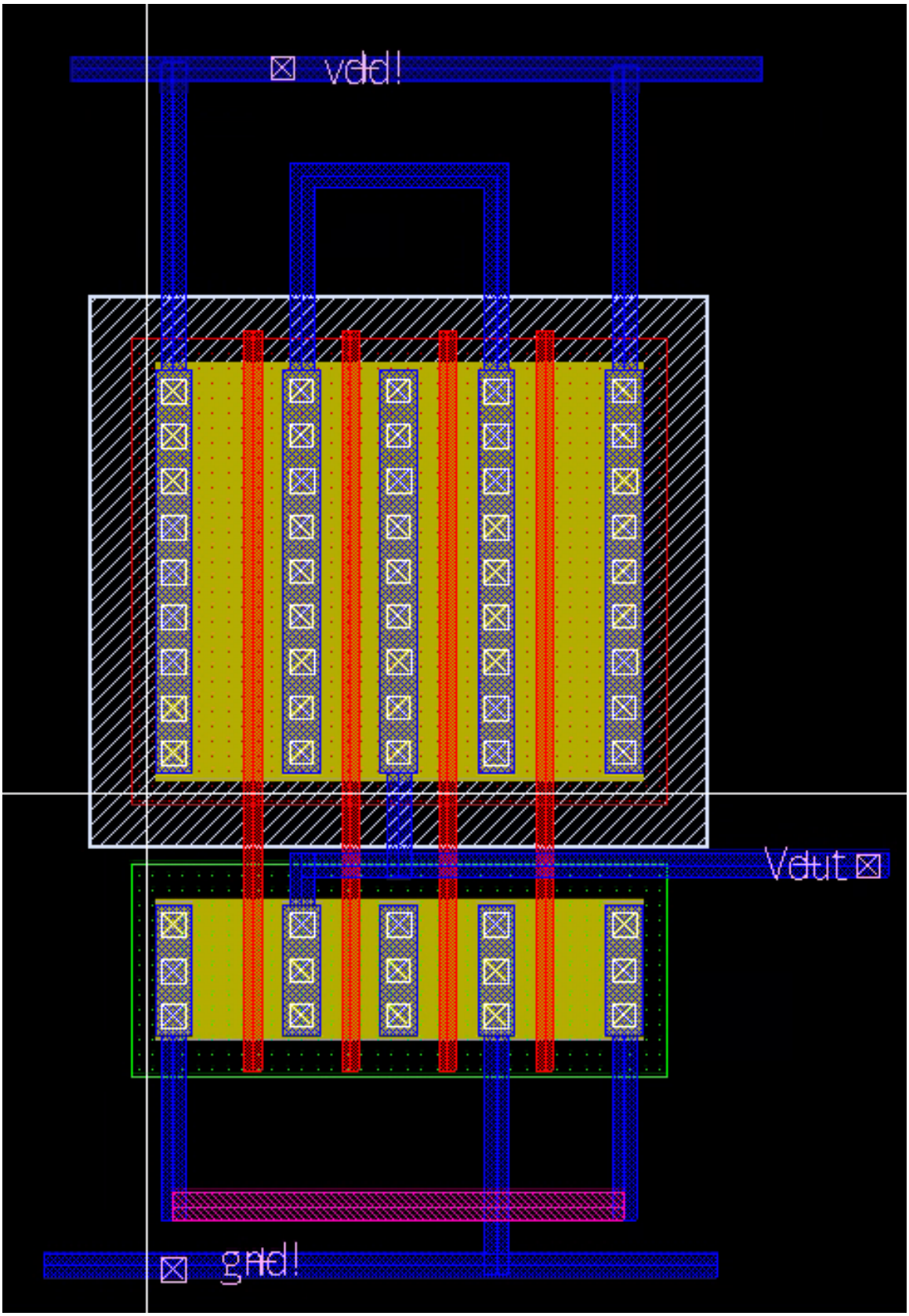
Questions:

Part C:

Fall: 11.6 ns

Rise: 10.7 ns (Refer to Page 3)

Lab 5 Report by Joseph Yu



run_icv.sh | rules.drc.9m_saed90_icv.drc.rs | XNOR_Logic.drc.custom_compiler.rc | XNOR_Logic.RESULTS | XNOR_Logic.LAYOUT_ERRORS

```
System Startup Time=0:00:00 User=0.00 Sys=0.02 Mem=0.437 GB


Command execution begins.  Details recorded in the summary and log files:
    /DCNFS/users/student/jyu4/ELEN153/synopsys_custom/pvjob_Lab4.XNOR_Logic.icv.drc/run_details/XNOR_Logic.sum
    /DCNFS/users/student/jyu4/ELEN153/synopsys_custom/pvjob_Lab4.XNOR_Logic.icv.drc/run_details/rules.drc.9m_saed90_icv.drc.dp.
g

Running ...
  ICV_Engine run is   1% complete.    Elapsed Time=0:00:00
  ICV_Engine run is   2% complete.    Elapsed Time=0:00:01
  ICV_Engine run is   3% complete.    Elapsed Time=0:00:03
  ICV_Engine run is   4% complete.    Elapsed Time=0:00:03
  ICV_Engine run is   5% complete.    Elapsed Time=0:00:03
  ICV_Engine run is  10% complete.    Elapsed Time=0:00:03
  ICV_Engine run is  15% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  20% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  25% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  30% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  35% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  40% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  45% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  50% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  55% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  60% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  65% complete.    Elapsed Time=0:00:04
  ICV_Engine run is  70% complete.    Elapsed Time=0:00:05
  ICV_Engine run is  75% complete.    Elapsed Time=0:00:05
  ICV_Engine run is  80% complete.    Elapsed Time=0:00:05
  ICV_Engine run is  85% complete.    Elapsed Time=0:00:05
  ICV_Engine run is  90% complete.    Elapsed Time=0:00:05
  ICV_Engine run is  95% complete.    Elapsed Time=0:00:06
  ICV_Engine run is 100% complete.    Elapsed Time=0:00:06

Completing error storage...
  Overall error storage time: None

Generating XNOR_Logic.LAYOUT_ERRORS...
  Generation Time=0:00:00  User=0.01 Sys=0.00 Mem=0.001 GB
```

Find:

Console

```
       1 First priority errors
       0 Second priority errors
============================
Information: Connection established with 'IC Validator VUE' running on 'linux22406.dc.engr.scu.edu'.
Information: Saving design 'Lab4 XNOR_Logic schematic'. (DESIGN_WINDOW-004)
Information: Connection closed with 'IC Validator VUE' running on 'linux22406.dc.engr.scu.edu'.
Information:
============================
JobID: icv_drc_2
Completed with no errors.
============================
>
```