



# PSMN013-30MLC

N-channel 30 V 13.6 mΩ logic level MOSFET in LPAK33 using NextPower Technology

23 February 2018

Product data sheet

## 1. General description

Logic level enhancement mode N-channel MOSFET in LPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

## 2. Features and benefits

- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

## 3. Applications

- DC-to-DC converters
- Load switching
- Synchronous buck regulator

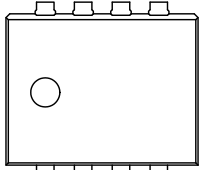
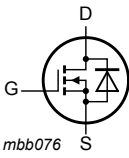
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-	30	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>		-	-	39	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	-	38	W
T <sub>j</sub>	junction temperature			-55	-	175	°C
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>		-	14.65	16.9	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>		-	11.8	13.6	mΩ
Dynamic characteristics							
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	1	-	nC
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	8	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		
			LFPAK33 (SOT1210)	

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN013-30MLC	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 8 leads	SOT1210

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN013-30MLC	M13C30

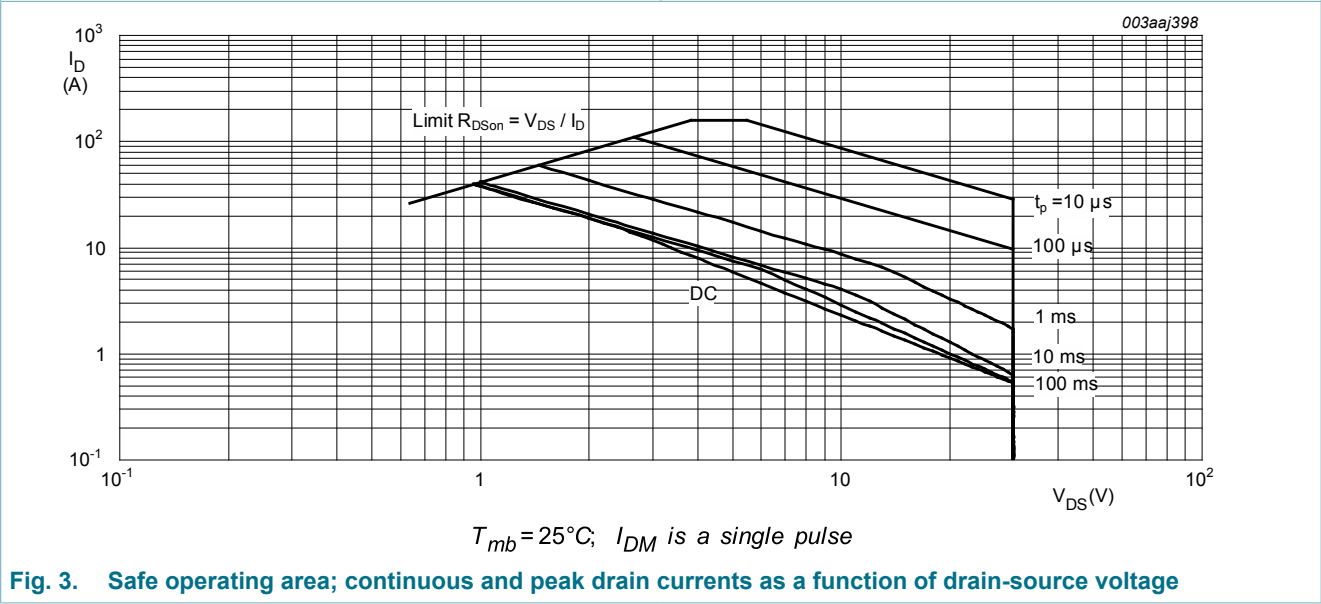
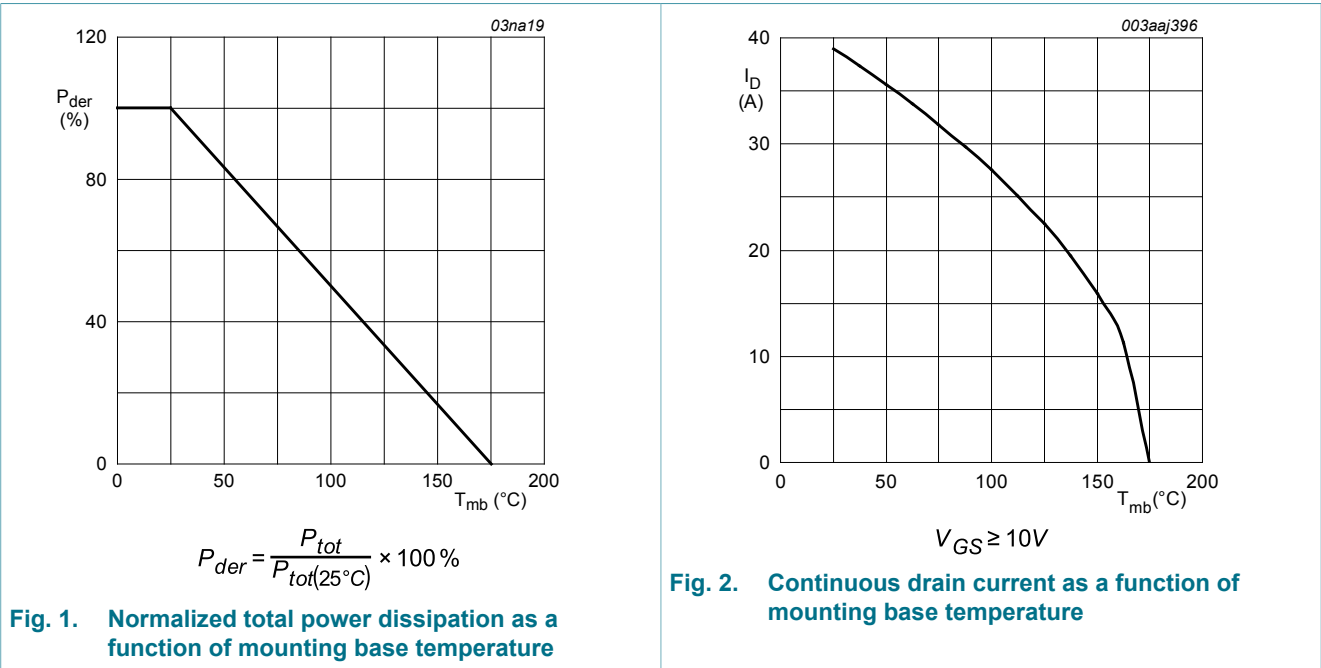
## 8. Limiting values

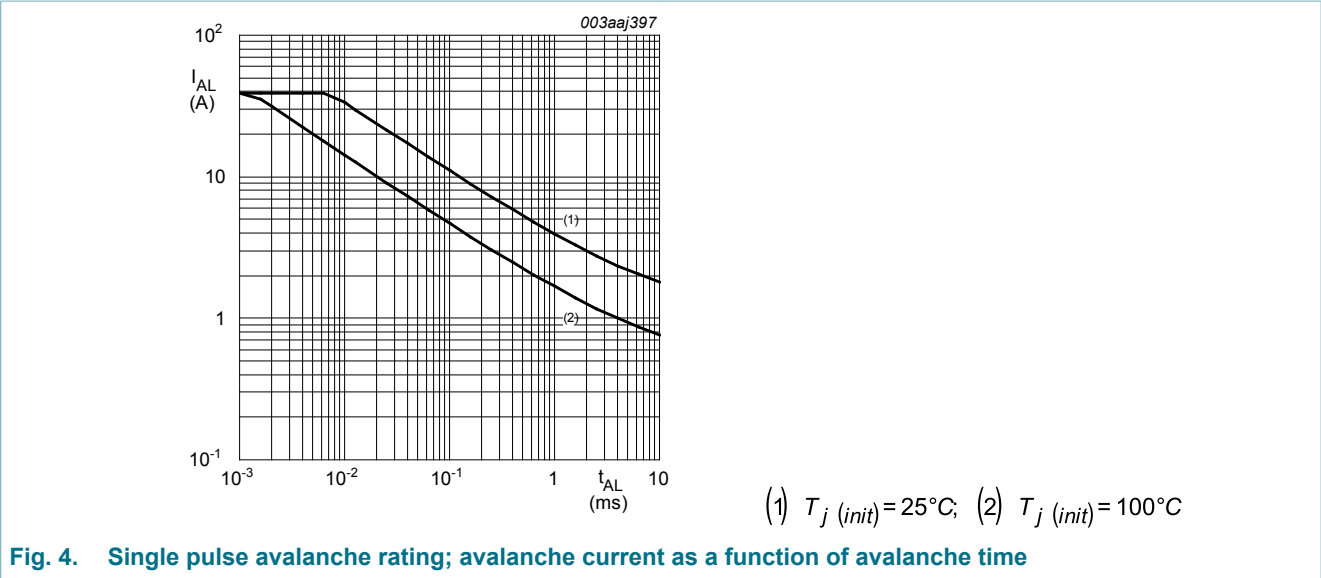
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1	-	38	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2	-	39	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; Fig. 2	-	28	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3	-	157	A
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>ESD</sub>	electrostatic discharge voltage	MM (JEDEC)		100	-	V
Source-drain diode						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	34	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	157	A
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 39 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; Fig. 4		-	5.6	mJ

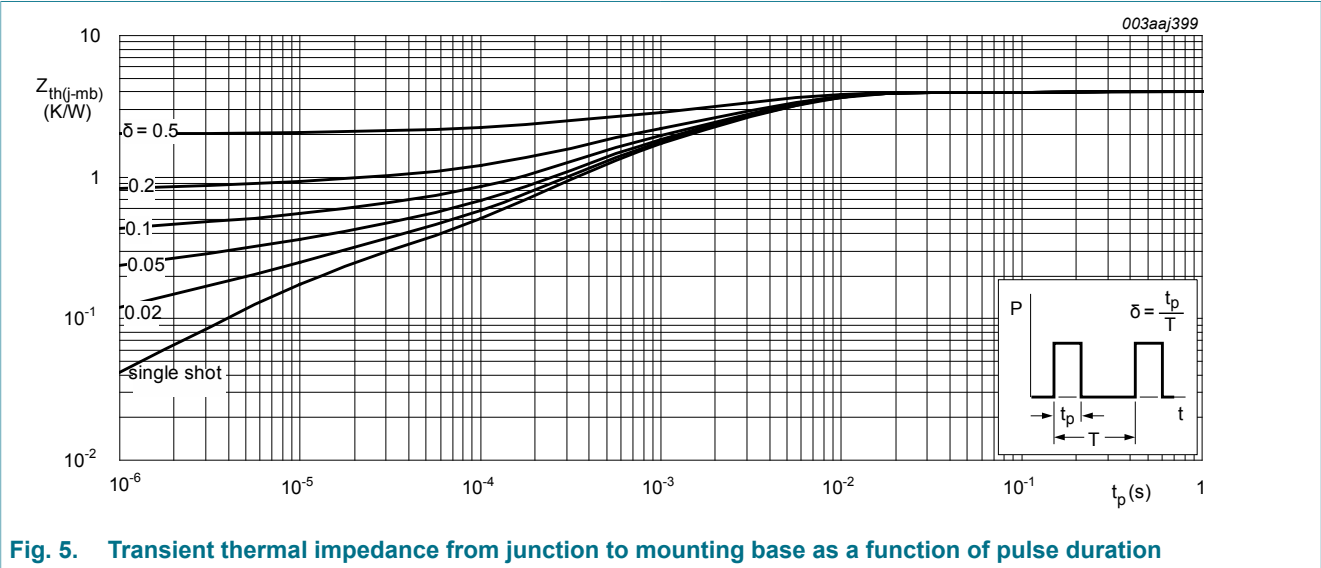




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	3.8	3.99	K/W

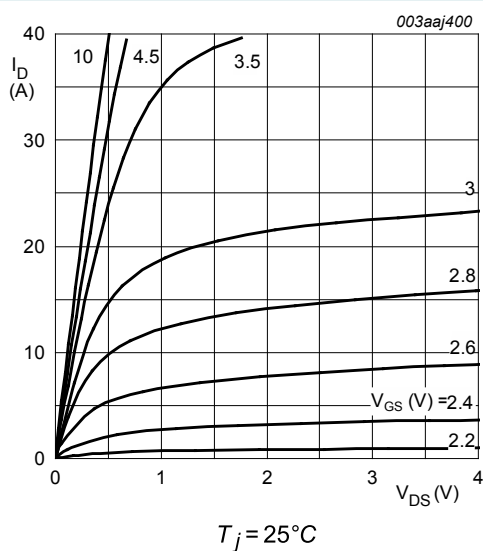


## 10. Characteristics

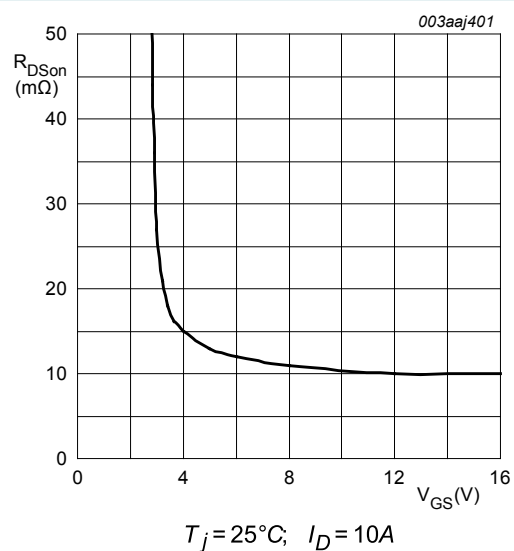
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$ ; $V_{GS} = 0\ V$ ; $T_J = 25\ ^\circ C$	30	-	-	V
		$I_D = 250\ \mu A$ ; $V_{GS} = 0\ V$ ; $T_J = -55\ ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$ ; $V_{DS} = V_{GS}$ ; $T_J = 25\ ^\circ C$	1.3	1.66	1.95	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature		-	-4	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 30\ V$ ; $V_{GS} = 0\ V$ ; $T_J = 25\ ^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 30\ V$ ; $V_{GS} = 0\ V$ ; $T_J = 150\ ^\circ C$	-	-	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16\ V$ ; $V_{DS} = 0\ V$ ; $T_J = 25\ ^\circ C$	-	-	100	nA
		$V_{GS} = -16\ V$ ; $V_{DS} = 0\ V$ ; $T_J = 25\ ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ V$ ; $I_D = 10\ A$ ; $T_J = 25\ ^\circ C$ ; <a href="#">Fig. 10</a>	-	14.65	16.9	mΩ
		$V_{GS} = 4.5\ V$ ; $I_D = 10\ A$ ; $T_J = 150\ ^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	-	28.75	mΩ
		$V_{GS} = 10\ V$ ; $I_D = 10\ A$ ; $T_J = 25\ ^\circ C$ ; <a href="#">Fig. 10</a>	-	11.8	13.6	mΩ
		$V_{GS} = 10\ V$ ; $I_D = 10\ A$ ; $T_J = 150\ ^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	-	22.95	mΩ
$R_G$	gate resistance	$f = 1\ MHz$	0.85	1.7	3.4	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 10\ A$ ; $V_{DS} = 15\ V$ ; $V_{GS} = 10\ V$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	8	-	nC
		$I_D = 10\ A$ ; $V_{DS} = 15\ V$ ; $V_{GS} = 4.5\ V$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	3.7	-	nC
		$I_D = 0\ A$ ; $V_{DS} = 0\ V$ ; $V_{GS} = 10\ V$	-	7.4	-	nC
$Q_{GS}$	gate-source charge	$I_D = 10\ A$ ; $V_{DS} = 15\ V$ ; $V_{GS} = 4.5\ V$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	1.2	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	0.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.4	-	nC
$Q_{GD}$	gate-drain charge		-	1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 10\ A$ ; $V_{DS} = 15\ V$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	2.6	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15\ V$ ; $V_{GS} = 0\ V$ ; $f = 1\ MHz$ ; $T_J = 25\ ^\circ C$ ; <a href="#">Fig. 14</a>	-	519	-	pF
$C_{oss}$	output capacitance		-	131	-	pF
$C_{rss}$	reverse transfer capacitance		-	37	-	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 1.5\ \Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\ \Omega$		-	7	-	ns
$t_r$	rise time			-	9.8	-	ns
$t_{d(off)}$	turn-off delay time			-	9.6	-	ns
$t_f$	fall time			-	5.5	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$		-	3.7	-	nC
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 15}$		-	0.86	1.1	V
$t_{rr}$	reverse recovery time	$I_S = 10\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}$		-	13.4	-	ns
$Q_r$	recovered charge			-	6.6	-	nC
$t_a$	reverse recovery rise time	$I_S = 10\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; \text{Fig. 16}$		-	8.6	-	ns
$t_b$	reverse recovery fall time			-	4.8	-	ns



**Fig. 6.** Output characteristics; drain current as a function of drain-source voltage; typical values



**Fig. 7.** Drain-source on-state resistance as a function of gate-source voltage; typical values

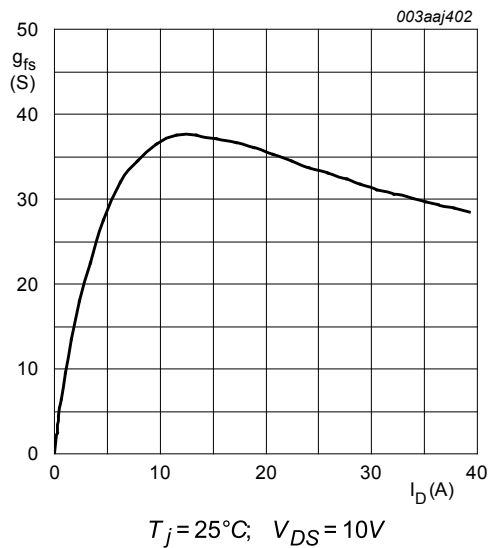


Fig. 8. Forward transconductance as a function of drain current; typical values

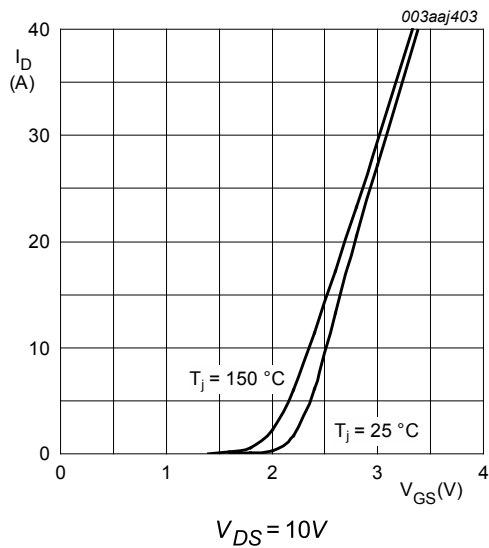


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

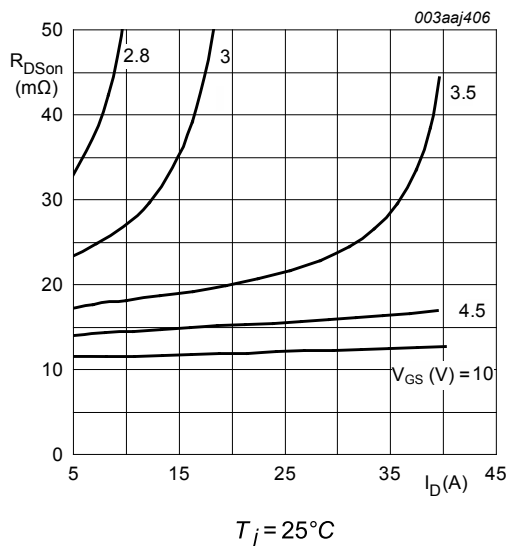


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

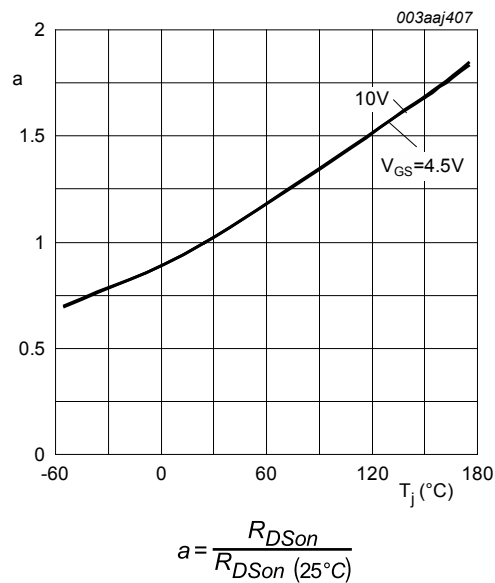


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

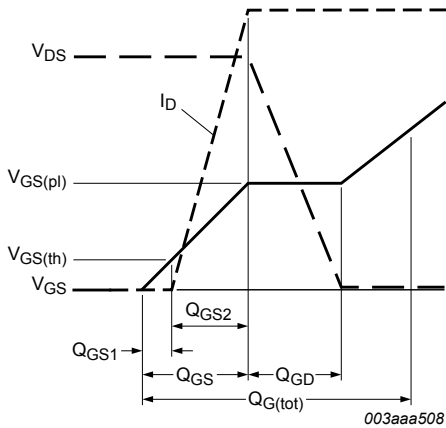


Fig. 12. Gate charge waveform definitions

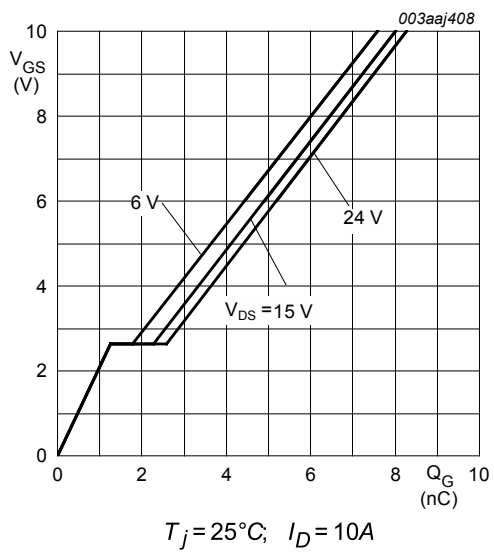


Fig. 13. Gate-source voltage as a function of gate charge; typical values

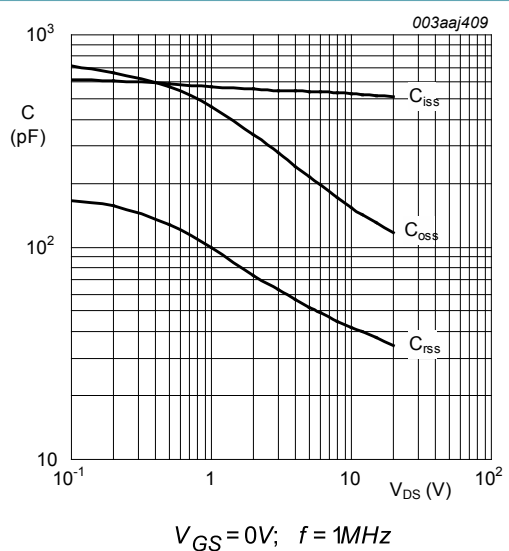


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

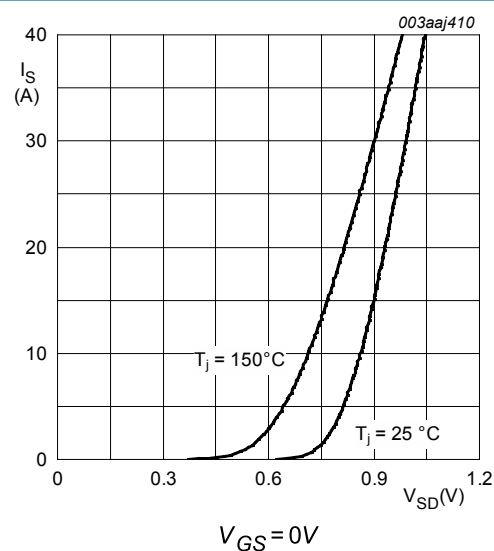


Fig. 15. Source current as a function of source-drain voltage; typical values



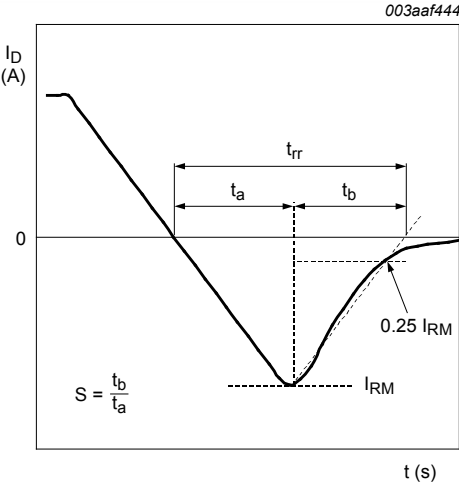


Fig. 16. Reverse recovery timing definition

11. Package outline

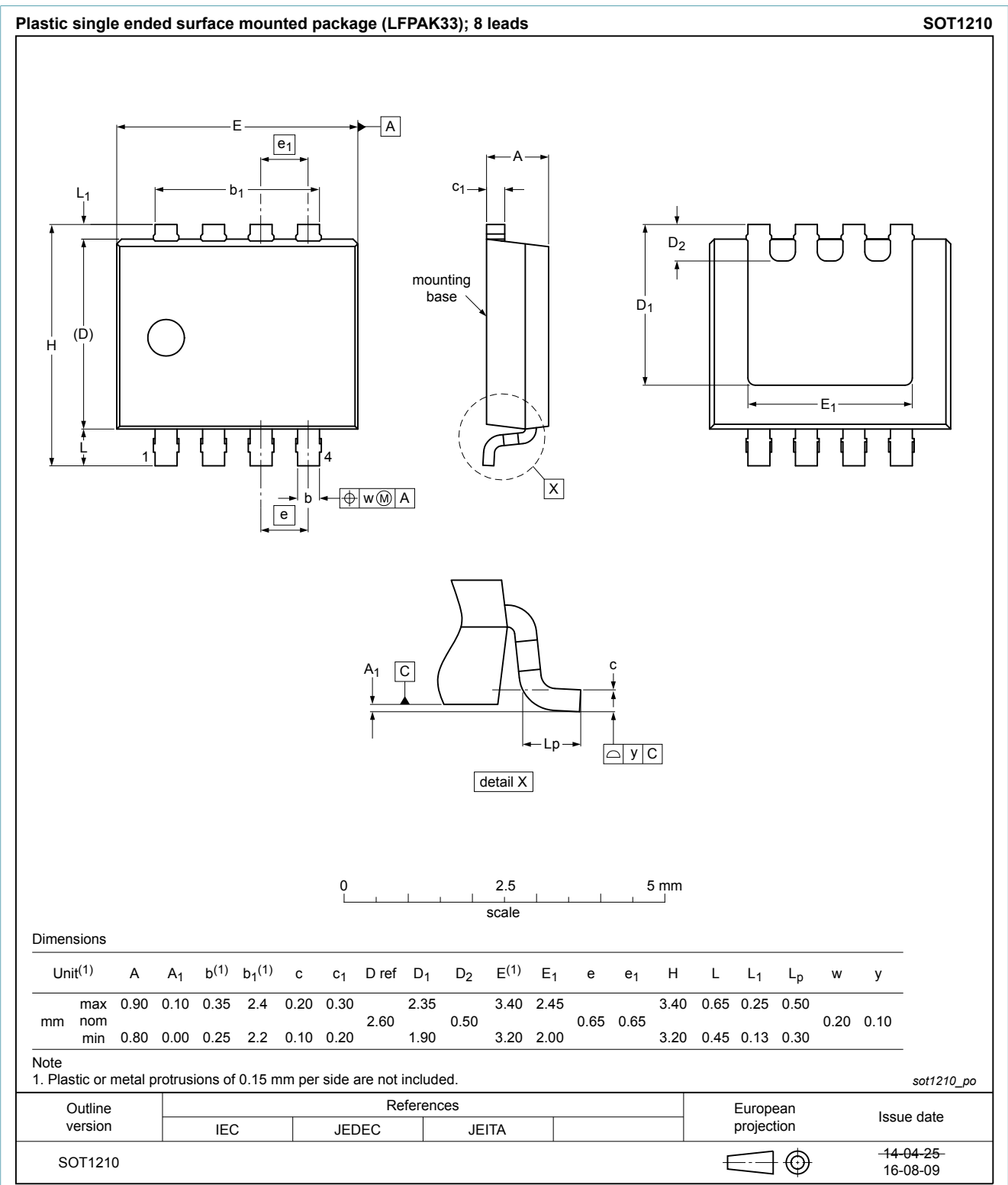
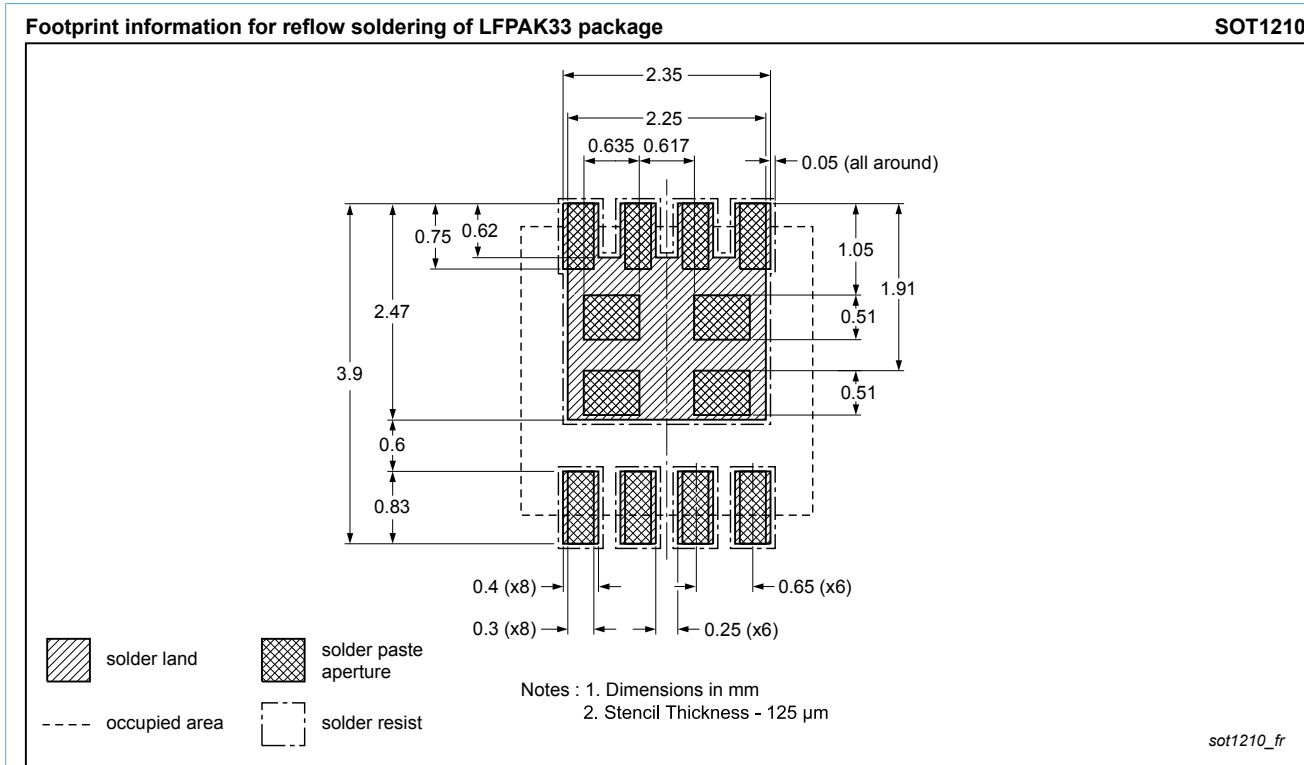


Fig. 17. Package outline LPAK33 (SOT1210)

## 12. Soldering



**Fig. 18. Reflow soldering footprint for LFPAK33 (SOT1210)**

## 13. Legal information

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