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CENTRO DE FORMACIÓN PROFESIONAL

Máster de Formación Permanente en Diseño Microelectrónico

UNIVERSITAT POLITÈCNICA DE VALÈNCIA

“A 22-nm FD-SOI Flip-Flop design”

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Resumen

La memoria del TFG/TFM empieza con un breve resumen de entre 150 y 200 palabras, escrito en castellano, valenciano e inglés. Estas páginas van sin numerar.

Resum

La memoria del TFG/TFM comença amb un breu resum d'entre 150 i 200 paraules, escrit en castellà, valencià i anglès. Aquestes pàgines van sense numerar.

Abstract

The thesis begins with a short abstract (between 150 and 200 words) written in Spanish, Valencian, and English. The cover page and the pages containing the three versions of the abstract are not numbered.

Agradecimientos

Este trabajo ha sido realizado con el apoyo de la *Cátedra Internacional UPV–VaSiC de Diseño Microelectrónico: Hacia el Campus Internacional de Semiconductores*, en el marco del Programa de Ayudas para la Creación de Cátedras Universidad–Empresa (Cátedras CHIP), financiado por la Unión Europea – *NextGenerationEU* y por la Secretaria de Estado de Telecomunicaciones e Infraestructuras Digitales del Ministerio para la Transformación Digital y la Función Pública, dentro del Plan de Recuperación, Transformación y Resiliencia (referencia **TSI-0691000-2023-0009**).

A su vez, agradecer al equipo de Bosch en especial Miguel/David por todo el apoyo técnico otorgado para la realización de este trabajo, sin la cual no hubiese sido posible.

RESUMEN EJECUTIVO

La memoria de TFM del Máster de Formación Permanente en Diseño Microelectrónico debe desarrollar en el texto los siguientes conceptos, debidamente justificados y discutidos, centrados en el ámbito del diseño microelectrónico.

CONCEPT	CONCEPTO	¿Cumple? (S/N)	¿Dónde? (páginas)
1. IDENTIFY:	1. IDENTIFICAR:		
1.1. Problem statement and opportunity	1.1. Planteamiento del problema y oportunidad		
1.2. Constraints (standards, codes, needs, requirements & specifications)	1.2. Toma en consideración de los condicionantes (normas técnicas y regulación, necesidades, requisitos y especificaciones)		
1.3. Setting of goals	1.3. Establecimiento de objetivos		
2. FORMULATE:	2. FORMULAR:		
2.1. Creative solution generation (analysis)	2.1. Generación de soluciones creativas (análisis)		
2.2. Evaluation of multiple solutions and decision-making (synthesis)	2.2. Evaluación de múltiples soluciones y toma de decisiones (síntesis)		
3. SOLVE:	3. RESOLVER:		
3.1. Fulfilment of goals	3.1. Evaluación del cumplimiento de objetivos		
3.2. Overall impact and significance (contributions and practical recommendations)	3.2. Evaluación del impacto global y alcance (contribuciones y recomendaciones prácticas)		

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Chapter 1. Introduction.

The continuing demand for higher performance and lower power consumption in integrated circuits has driven technology scaling into advanced process nodes. At the 22 nm node, Fully Depleted Silicon-On-Insulator (FD-SOI) technology is an attractive alternative to bulk CMOS for many applications because it mitigates short-channel effects, reduces parasitic capacitances, and offers body-biasing capability that can be used for dynamic performance-power tuning [1], [2]. This thesis focuses on the design and characterization of flip-flops implemented in a 22 nm FD-SOI process, with particular emphasis on device-level characterization and robustness across operating conditions (process, supply voltage, and temperature corners), and on design trade-offs for timing, area, and power.

Flip-flops are fundamental sequential building blocks used throughout digital systems, from microprocessors to communications interfaces [2]. In advanced technology nodes, flip-flop performance becomes increasingly sensitive to device variability and leakage, as well as to supply conditions and operating corners. FD-SOI provides additional design flexibility through back-bias capability [1]; however, in this work no back-bias sweeps are performed, and the evaluation is restricted to baseline operation across PVT corners. Designing flip-flops that remain robust under these conditions—while accounting for technology-specific device behaviour—is therefore an important practical and academic problem.

Objectives of this work:

- Design and evaluate three flip-flop topologies in a 22 nm FD-SOI process, targeting competitive timing, power, and area, and assessing their suitability for driving current-steering DAC control logic (IDACs).
- Characterize foundational devices and circuit primitives (from device options to transmission gates and inverters) to extract parameters relevant to flip-flop performance and robustness.
- Define test structures and simulation methodologies (from DC sweeps to consistent timing and noise measurements) to enable repeatable characterization of FD-SOI devices and flip-flops.
- Evaluate flip-flop behaviour across supply voltage, process corners, and temperature to quantify robustness and identify opportunities for optimization.

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This research combines device characterization, circuit design, and simulation:

- **Device and cell characterization:** Basic cells and device structures—including current mirrors, transmission gates, and inverters—are used to extract transistor-level metrics and to study performance trends in a 22 nm FD-SOI process.
- **Circuit design**: Based on these observations, three flip-flop topologies (two static latch-based flip-flop and one dynamic capacitor-based) are selected, sized, and simulated across PVT (process–voltage–temperature) corners.
- **Testing and simulation:** Tests and simulations are conducted under controlled bias and stimulus conditions to validate the designs and to quantify timing variation, leakage, and noise-related parameters.

This work provides an overview of how to design flip-flops suitable for controlling high-speed mixed-signal blocks such as IDACs. Given the role of IDACs in communication systems, and the semiconductor technology trends that impact their design, aligning flip-flop timing robustness with converter control requirements is an important practical consideration in high-quality implementations.

1.1 IDACs (Current-Steering DACs).

Digital-to-analog converters (DACs) translate digital binary codes into corresponding analog voltages or currents. In an ideal DAC, the digital codes map to analog levels that are uniformly spaced across the output range [3]. Current-steering DACs (CS DACs, also referred to as IDACs) are commonly used in high-speed mixed-signal systems because they can switch currents rapidly and scale well with advanced CMOS nodes [4].

A current-steering DAC typically consists of an array of matched unit current sources, switching elements that steer each unit current to one of two outputs, and an output summing network (e.g., a resistive or capacitive load). Each digital code selects the corresponding number of unit currents steered toward the positive output (with the remainder steered to the negative output), producing a differential output current [4], [5].

A typical DAC unit cell contains:

- An array of matched current sources (often implemented with cascode transistors to increase output impedance and reduce sensitivity to voltage variations at internal nodes).
- A differential switching quad (NMOS and/or PMOS switches) that steers the unit current to the output or to a dump/reference branch.
- Optional cascode devices above and/or below the switches to isolate the switching node and improve linearity and output impedance [6], [7].

Figure 1.1 illustrates a conceptual current-steering DAC unit cell in which a unit current is steered either to the output or to a dump branch.

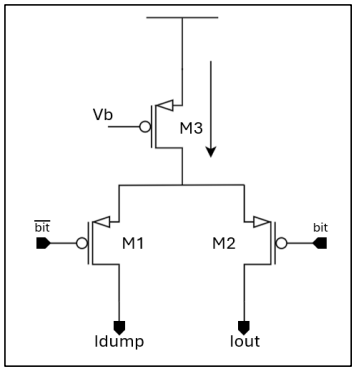

Figure 1.1: Conceptual current-steering DAC unit cell.

To achieve both high speed and high linearity, designers often use segmentation (a combination of thermometer coding and binary weighting). Thermometer-coded segments reduce switching glitch energy and mismatch sensitivity for the most significant bits, while binary weighting reduces area and complexity for the least significant bits. Static linearity in a current-steering DAC is primarily determined by matching among the unit current sources: device mismatch produces differential nonlinearity (DNL) and integral nonlinearity (INL) errors [3 - 8].

In high-speed IDACs, dynamic performance is also influenced by the alignment of switching events across unit elements. Timing skew and uncertainty in the digital control signals can increase glitch energy and degrade dynamic linearity. Therefore, when designing flip-flops for IDAC control logic in a 22 nm FD-SOI process, key considerations include timing accuracy, low clock-to-output variation across PVT, and layout-aware strategies (even at schematic level) that minimize coupling into sensitive switching nodes.

1.2 Advanced communication systems.

Modern applications in telecommunications and sensing increasingly require high-linearity waveform generation and high-speed data conversion. Advanced communication systems—including automotive radar, high-bandwidth wireless links, and sensor platforms for driver assistance—place stringent demands on mixed-signal hardware. In these systems, current-steering DACs (IDACs) are central building blocks because they enable high-speed, precise waveform synthesis and support wideband modulation schemes in which linearity and noise performance are critical.

Radar system-on-chip (SoC) implementations illustrate the broader trend toward higher integration and advanced process nodes: modern devices integrate millimetre-wave front ends together with substantial on-chip digital processing [9]. In this context, robust sequential cells remain important because they distribute timing and control signals to large arrays of mixed-signal unit elements. Even when the flip-flop is not the dominant performance limiter, its clock-to-output behaviour, sensitivity to operating conditions, and power consumption can still affect overall robustness and design margin.

This work was conducted with the support of Bosch Semiconductors. The preceding discussion of automotive radar and communication applications motivates the flip-flop design targets by linking them to realistic mixed-signal use cases in which timing robustness across operating conditions is critical.

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1.3 The technology.

Selecting the right technology involves understanding not only performance requirements but also design goals related to power, cost, and the target application domain. The demand for greater energy efficiency motivates the exploration of advanced nodes such as 22 nm for low-power and high-performance designs. At this node, FD-SOI platforms offer device characteristics that are advantageous for both digital and mixed-signal circuits, including reduced parasitic capacitances and improved electrostatic control compared with bulk CMOS [1].

FD-SOI technologies also provide the capability for forward and reverse back-biasing, which can be used as a post-fabrication knob to trade speed for leakage and to tune circuit behaviour across operating conditions [1]. However, since no back-bias sweeps are performed in this work, the analysis in this thesis focuses on baseline device and circuit behaviour under supply-voltage variation, process corners, and temperature variation.

In the following chapter, the 22 nm FD-SOI technology is introduced from a circuit designer's perspective, and the simulation environment and low-level characterization structures used in this thesis are described. These foundational results are then used to guide flip-flop design, sizing, and evaluation.

Chapter 2. Understanding 22-nm.

This chapter motivates the selection of a 22-nm FD-SOI technology (also referred to as 22FDX) and establishes the device-level basis used throughout this work. The flip-flop circuits analysed in the following chapters are constrained by transistor behaviour, including drive capability, leakage, intrinsic capacitances, and variability. For that reason, this chapter first summarizes the key characteristics of the 22-nm node that are relevant to high-speed mixed-signal operation. It then describes the simulation methodology and a set of baseline device tests (NFET/PFET), followed by a comparison between LVT and SLVT options. Finally, a Monte Carlo experiment using a current-mirror structure is used to quantify mismatch through the output-current standard deviation (σI_{OUT}) and histogram-based analysis.

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2.1 Why 22-nm for this work.

Selecting the technology node is a central design decision because it directly constrains the achievable speed, power, linearity, and robustness of the overall system. As CMOS nodes scale, switching energy can be reduced through lower supply voltages and smaller parasitic capacitances. However, maintaining performance at reduced supply voltage becomes increasingly challenging due to reduced voltage headroom and the growing sensitivity of delay to process and temperature variation. This fundamental trade-off between performance and energy efficiency motivates the exploration of advanced nodes for ultra-low-power implementations.

Submicron gate-length MOS transistors have historically enabled sample rates in the hundreds of MHz range, supporting the implementation of high-speed converters and fast-switching digital interfaces [7]. At 22 nm, these advantages are strengthened by reduced device capacitances and improved transistor transit frequency, which benefit timing-critical elements such as flip-flops and switching-intensive circuits such as current-steering DACs [2.3]. In addition, for systems that combine dense digital processing with precision analog or RF blocks (e.g., communications and sensing SoCs), these properties are especially relevant because they affect both power consumption and the predictability of device characteristics used in biasing and current generation [2.3 and 2.4].

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Comentado [JC6]: find

The choice of 22 nm is consistent with the goals of this work, which focuses on device and circuit characterization rather than on pushing an absolute technology limit. The circuits studied later depend heavily on (i) device drive capability (affecting timing), (ii) leakage (affecting static power), (iii) intrinsic capacitances (affecting dynamic power and switching transients), and (iv) mismatch (affecting current accuracy and DAC linearity). For this reason, this chapter establishes a device-level baseline in 22-nm FD-SOI through systematic NFET/PFET characterization over process corners and through a Monte Carlo mismatch experiment based on a current-mirror testbench.

In summary, the 22-nm node represents a practical point in the scaling roadmap where improved switching speed and reduced parasitic capacitances enable higher operating frequencies and lower dynamic energy per transition compared with older nodes. For timing-critical sequential cells such as flip-flops, these benefits translate into faster internal regeneration and reduced clock-to-Q delay for a given power budget. For current-steering architectures such as IDACs, reduced parasitics and improved electrostatics contribute to faster switching and can help preserve dynamic linearity by limiting unwanted charge injection and transient coupling at switching nodes.

2.2 Technology overview (22-nm FD-SOI device characteristics)

Technology scaling is widely used to improve energy efficiency; however, scaling is typically accompanied by a reduction in supply voltage to maintain device reliability and power density, which in turn pushes designs toward lower threshold voltages to preserve performance [10].

Within this context, 22 nm FD-SOI has gained attention as a planar technology option that supports continued performance scaling while improving energy efficiency, contributing to the extension of CMOS relevance for low-power and mixed-signal integration. Relative to conventional bulk CMOS, FD-SOI devices can exhibit reduced leakage and lower parasitic capacitances associated with source/ drain junctions. These properties benefit both dynamic power consumption and switching speed. They are directly relevant to this thesis because flip-flop timing and IDAC control quality depend on transistor drive current, leakage behaviour, intrinsic capacitances, and device-to-device variability.

FD-SOI devices are characterized by a thin silicon film on top of a buried oxide, which strengthens gate control over the channel and reduces junction-related parasitics compared with bulk CMOS. Figure 2-1 shows conceptual cross-sections comparing bulk CMOS and FD-SOI [11]. For the purposes of this thesis, the most relevant consequences at the circuit level are:

- **Electrostatic control and short-channel behaviour:** Improved channel control helps maintain predictable I–V behaviour in scaled devices, which is important when building timing-critical regenerative structures such as latches and flip-flops.
- **Reduced parasitic capacitances:** Lower parasitic capacitances reduce switching energy and can improve edge rates for a given drive current, affecting both flip-flop timing and the dynamic behaviour of IDAC switching networks.
- **Leakage and low-voltage operation:** Reduced leakage mechanisms (relative to comparable bulk nodes) support low-power operation and reduce static power consumption, which is relevant for always-on scenarios.
- **Device options (LVT/SLVT):** The PDK provides different threshold-voltage options, enabling explicit trade-offs between speed and leakage. This work compares LVT and SLVT devices using the same characterization methodology to guide later circuit choices.

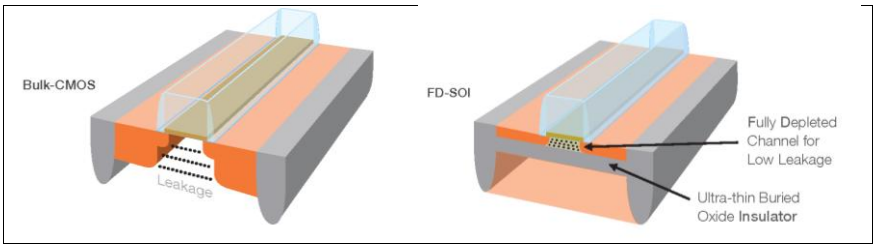


Figure 2-1: Bulk-CMOS and FD-SOI cross-section comparative.

FD-SOI technologies also offer the capability for forward and reverse back-biasing, which can be used to tune threshold voltage and trade off speed against leakage. However, no back-bias sweeps are performed in this work; therefore, the analysis in this thesis focuses on baseline behaviour under supply-voltage variation, process corners, and temperature. Back-bias exploration is outlined as a natural extension of this work in the Further work. section.

2.3 Simulation environment and methodology.

All device characterization results in this chapter are obtained using Cadence simulation tools and the 22 nm FD-SOI PDK. Unless otherwise stated, results are produced at the nominal supply voltage (V_{DD} = 0.8 V) and nominal temperature (T = 25 ºC).

The simulations are organized to extract a set of device metrics relevant to both timing-critical design and current-source accuracy through standardized testbenches:

- **DC characteristics:** I_D-V_{GS} and I_D-V_{DS} sweeps for NFET and PFET devices under defined bias conditions.

- **Small-signal parameters:** extraction of transconductance (g_m) and output conductance (g_{ds}) at representative operating points.
- **Threshold voltage extraction:** consistent method for estimating (V_{th}) across devices and conditions.
- **Leakage measurements:** off-state leakage current (I_{off}) under defined off-bias conditions.
- **Capacitances:** extraction of gate-related capacitances, specifically (C_{gg}) and (C_{gd}), which influence switching speed and dynamic power.

To ensure fair comparisons, NFET and PFET devices are characterized using identical sweep setups, and LVT/SLVT variants are evaluated with the same device dimensions and bias conditions. Process corners are evaluated to capture typical (TT) and extreme (SS/FF) variation. In addition, Monte Carlo simulations are used to assess local mismatch. All simulations are performed in Cadence Virtuoso Studio IC 23.1 using the GlobalFoundries 22-nm FD-SOI PDK obtained through EUROPRACTICE.

2.4 NFET and PFET characterization.

This section characterizes baseline NFET and PFET devices available in the technology to establish reference behaviour for later circuit analysis. The available device geometries span W = [0.08, 10] µm and L = [0.02, 8] µm). The testbenches used to characterize the NFET and PFET devices are shown in Figure 2-2. DC voltage sources are applied to the gate and drain terminals to perform the required sweeps. For each run, device width and length are configurable parameters, and the number of fingers is set to one.

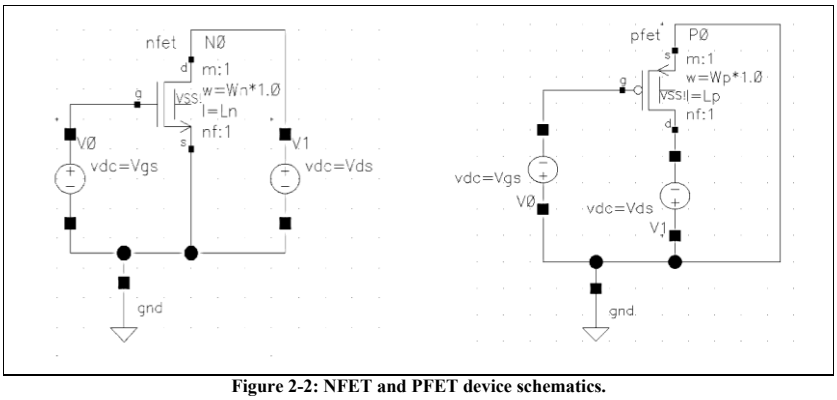


Figure 2-2: NFET and PFET device schematics.

2.4.1 $I_D - V_{GS}$ (transfer) characteristics.

The I_D–V_{GS} sweep is used to observe subthreshold conduction, the threshold transition region, and strong-inversion drive current. For the NFET, the transfer curve is obtained by sweeping V_{GS} from 0 to 0.9 V in steps of 0.05 V, while V_{DS} is held at representative values (V_{DS} = 0.05, 0.3, 0.6, 0.8, 0.9 V). The 0.9 V case is included as an extended-bias condition to highlight drain-induced effects.

Using multiple V_{DS} values allows visual inspection of DIBL (drain-induced barrier lowering), observed as an increase in subthreshold current and an apparent reduction in threshold voltage at higher V_{DS}. For the PFET, the same characterization is performed using the corresponding voltage polarities (sweeping V_{SG}) with fixed V_{SD} values). In both cases, the device dimensions are (W = 0.17 µm) and (L = 0.02µm). The resulting transfer characteristics are shown in the following figures:

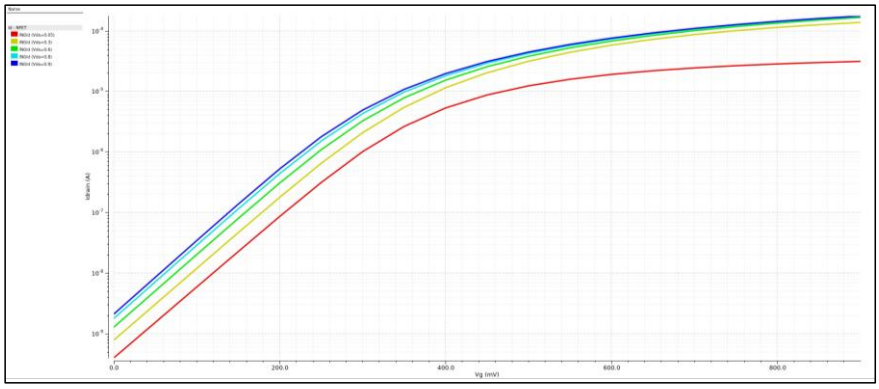


Figure 2-3: NFET transfer characteristic: I_D - V_{GS} with stepped drain bias.

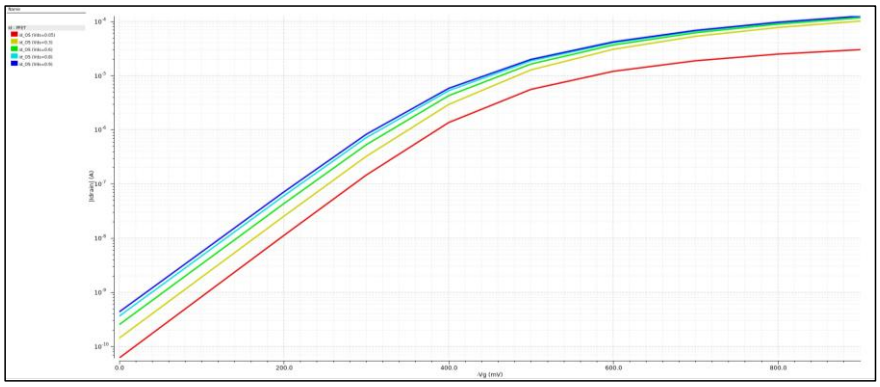


Figure 2-4: PFET transfer characteristic: I_D - V_{SG} with stepped drain bias.

As V_{DS} increases, the transfer curves shift upward (higher I_D for the same gate bias), particularly in the subthreshold region. This behaviour is consistent with drain-induced barrier lowering (DIBL), which increases subthreshold current and effectively reduces the apparent threshold voltage at higher V_{DS}.

2.4.2 I_D – V_{DS} (output) characteristics.

The I_D–V_{DS} sweep is used to observe the transition from the linear (ohmic) region to saturation and to evaluate channel-length modulation at higher drain bias. For the NFET, the output characteristics are obtained by sweeping V_{DS} from 0 to 0.9 V (ΔV_{DS} = 0.05 V) while V_{GS} is stepped through representative values (V_{GS} = 0.1 to 0.9 V in 0.1 V increments). At low V_{DS}, I_D increases approximately linearly with V_{DS}, whereas at higher V_{DS} the device approaches saturation. The remaining positive slope of I_D in the saturation region reflects channel-length modulation; that is, the effective channel length decreases with increasing V_{DS}, causing I_D to continue increasing.

As for the transfer curves, the device dimensions are fixed to (W = 0.17 µm) and (L = 0.02 µm) for both devices. For the PFET, the same characterization is performed using the corresponding voltage polarities (sweeping V_{SD} while stepping V_{SG}), producing an analogous family of output curves, as shown in the following figures:

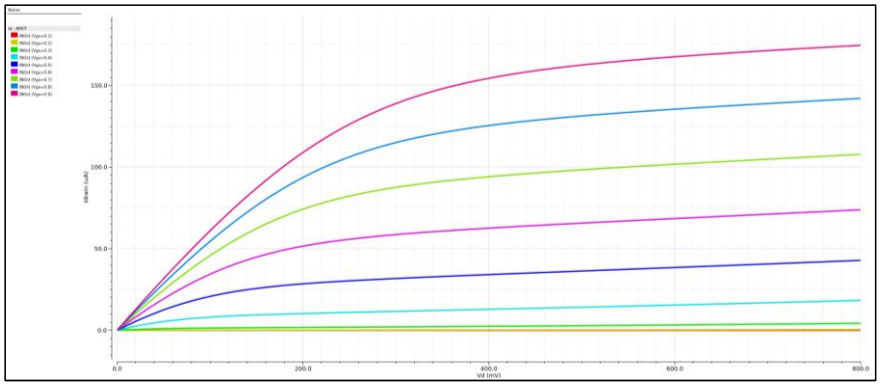


Figure 2-5:NFET output characteristic: I_D - V_{DS} with stepped gate bias.

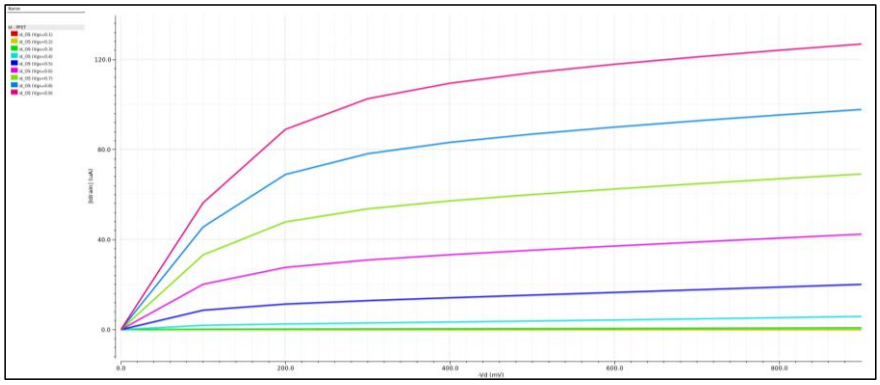


Figure 2-6: PFET output characteristic: I_D - V_{SD} with stepped gate bias.

2.4.3 Threshold voltage, I_d, I_{dOff}, g_m and g_{ds} extraction.

Section 2.4.3 reports extracted electrical parameters obtained from DC characterization testbenches for a discrete set of device geometries chosen to be representative of practical sizing and directly comparable to foundry characterization. To keep the discussion concise while still capturing geometry dependence, results are presented for the following (W/L) combinations: 0.17 µm/0.02 µm, 0.17 µm/0.024 µm, 0.5 µm/0.02 µm, 10 µm/8 µm, and 0.08 µm/0.02 µm.

This set spans the minimum-width, near-minimum-length device (0.08/0.02); a commonly used reference geometry for baseline comparison (0.17/0.02); a slightly longer channel to highlight short-channel sensitivity (0.17/0.024); a moderate-width, near-minimum-length device representative of a higher-drive sizing choice (0.5/0.02); and a large-width, long-channel device (10/8) that serves as a long-channel reference with reduced short-channel effects.

The same geometries are used for both NFET and PFET devices. Parameters are evaluated at the nominal temperature (T = 25 ºC) for the TT, FF, and SS process corners to enable consistent comparison across device type, geometry, and corner.

Small-signal parameters are extracted at operating points of interest following the GlobalFoundries (GF) characterization definitions. For PFET measurements, a negative supply is used and (V_{BS} = V_{DD}) is enforced; therefore, when (V_{DD} = -0.8 V) the PFET body is tied to (-0.8 V). For NFET measurements, GF specifies (V_{BS} = 0 V), so the NFET body is tied to the source (ground/reference), ensuring zero body bias during extraction.

In addition, operating points are selected using fixed drain-current references: ($I_{constant}$ = 300 nA) for NFETs and ($I_{constant}$ = 70 nA) for PFETs. The extracted small-signal parameters are presented in Table 2-1:

Parameter	Condition
$\mathbf{V_{thLin}}$	Vgs @ Iconstant, Vds = VddLin
$\mathbf{V_{thSat}}$	Vgs @ Iconstant, Vds = Vdd
$\mathbf{I_{dSat}}$	Id @ Vgs = Vdd, Vds = Vdd
$\mathbf{I_{dOff}}$	Id @ Vgs = 0V, Vds = Vdd
$\mathbf{g_m}$	$\frac{\partial Id}{\partial Vgs}$ @ Vgs = 0.1 + VthLin, Vds = Vdd/2
$\mathbf{g_{ds}}$	$\frac{\partial Id}{\partial Vds}$ @ Vgs = 0.1 + VthLin, Vds = Vdd/2

Table 2-1: Small signal evaluation conditions (GF definition).

The linear-region drain bias is set to ($V_{ds\ Lin}$ = +0.05 V) for NFETs and ($V_{ds\ Lin}$ = -0.05 V) for PFETs. The bias point (V_{gs} = 0.1 + V_{th}) is used to evaluate g_m and g_{ds} slightly above threshold, ensuring a consistent moderate-inversion operating condition across geometries and process corners and avoiding numerical sensitivity associated with extracting derivatives exactly at V_{th}. A brief description of each small-signal parameter is provided:

- $\mathbf{V_{thLin}}$ (linear-regime threshold voltage) is the gate voltage required to reach the reference current at low V_{DS}, and is commonly used to compare turn-on behaviour with minimal drain-induced effects.
- $\mathbf{V_{thSat}}$ (saturation-regime threshold voltage) is the gate voltage required to reach the reference current at nominal/high V_{DS}, reflecting threshold behaviour under a stronger lateral field and more representative on-state conditions.
- $\mathbf{I_{dSat}}$ (on-state drive current) is the drain current at maximum V_{GS} and V_{DS} and indicates the device current capability relevant for speed.
- $\mathbf{I_{dOff}}$ (off-state leakage current) is the drain current at (V_{GS} = 0) and nominal/high V_{DS}, and quantifies leakage in the nominal off condition (standby power).
- $\mathbf{g_m}$ (transconductance) indicates how effectively the device converts gate-voltage variations into drain current, relevant for switching speed and gain.
- $\mathbf{g_{ds}}$ (output conductance) reflects finite output resistance and impacts current-source accuracy, intrinsic gain, and mirror compliance.

For these measurements, 4-terminal devices are used to explicitly control the bulk connection Figure 2-7. The NFET bulk is tied to 0 V (ground), enforcing (V_{BS} = 0) during extraction. For the PFET, the bulk is tied to the negative supply rail (-V_{DD}), so that when (V_{DD} = 0.8 V) the body is at -0.8 V, ensuring a well-defined body potential and avoiding unintended body bias.

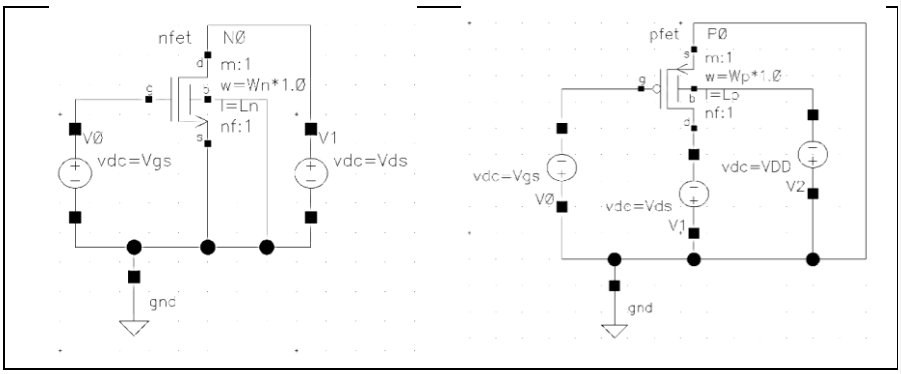


Figure 2-7: NFET and PFET devices with bulk connection schematics.

Parameter (units)	Width (µm)	Length (µm)	NFET - 22FDX-PLUS (T=25ºC)		
			TT	FF	SS
V_{thLin} *[mV]*	0.17	0.02	336.2	275.8	395.7
	0.17	0.024	342.6	286.3	398.1
	0.5	0.02	325.3	281.3	368.7
	10	8	387.2	358.6	415.0
	0.08	0.02	352.6	275.1	428.9
V_{thSat} *[mV]*	0.17	0.02	265	193	335.5
	0.17	0.024	286.3	222.1	349.3
	0.5	0.02	251.1	197.8	303.3
	10	8	377.9	349.5	405.5
	0.08	0.02	285.8	194.5	375.1
I_{dSat} *[µA/µm]*	0.17	0.02	836	1040.8	634.2
	0.17	0.024	776.5	959.9	595.2
	0.5	0.02	820.4	969.9	669.4
	10	8	5.34	6.55	4.32
	0.08	0.02	876.9	1147.2	611.7
I_{dOff} *[A/µm]*	0.17	0.02	9.68e-09	7.83e-08	1.22e-09
	0.17	0.024	3.03e-09	2.12e-08	4.48e-10
	0.5	0.02	1.41e-08	6.72e-08	2.99e-09
	10	8	6.77e-12	1.07e-11	1.46e-12
	0.08	0.02	5.50e-09	7.76e-08	4.08e-10
g_m *[µA/V/µm]*	0.17	0.02	1.29e+03	1.42e+03	1.14e+03
	0.17	0.024	1.19e+03	1.31e+03	1.06e+03
	0.5	0.02	1.24e+03	1.34e+03	1.12e+03
	10	8	5.53e+00	5.81e+00	5.26e+00
	0.08	0.02	1.39e+03	1.55e+03	1.19e+03
g_{ds} *[µA/V/µm]*	0.17	0.02	1.04e+02	1.40e+02	7.28e+01
	0.17	0.024	7.43e+01	9.77e+01	5.29e+01
	0.5	0.02	1.05e+02	1.32e+02	7.97e+01
	10	8	6.38e-03	6.83e-03	5.95e-03
	0.08	0.02	1.04e+02	1.48e+02	6.57e+01

Table 2-2: Extracted DC parameters for NFET device.

FD-SOI offers improved electrostatics compared to bulk CMOS, typically enabling higher transconductance (g_m) and lower output conductance (g_{ds}). These benefits stem from the fully depleted channel and the presence of a buried oxide (BOX), which reduce parasitic junction

capacitances and weaken drain-to-channel coupling. As a result, short-channel effects such as drain-induced barrier lowering (DIBL) are mitigated, helping to limit off-state leakage **¡Error! No se encuentra el origen de la referencia.**.

This trend is reflected in the extracted device metrics reported in Table 2-2 (NFET) and Table 2-3 (PFET), where both device types exhibit relatively high g_m and comparatively low g_{ds} across the evaluated geometries and TT/FF/SS process corners, indicating strong gate control and limited channel-length modulation.

Parameter (units)	Width (µm)	Length (µm)	PFET - 22FDX-PLUS (T=25ºC)		
			TT	FF	SS
V_{thLin} *[mV]*	0.17	0.02	-290	-234.5	-348
	0.17	0.024	-296.3	-244.9	-350.3
	0.5	0.02	-290.5	-250.9	-331.8
	10	8	-307	-279.8	-335.7
	0.08	0.02	-292.5	-219.6	-369.1
V_{thSat} *[mV]*	0.17	0.02	-221.7	-158.6	-288.3
	0.17	0.024	-241.2	-184.4	-301.3
	0.5	0.02	-219	-172.9	-267.4
	10	8	-298.7	-271.7	-327.2
	0.08	0.02	-228.7	-147.3	-315.1
I_{dSat} *[µA/µm]*	0.17	0.02	666.4	817.5	517.4
	0.17	0.024	607.6	738.7	476.9
	0.5	0.02	525.7	611.4	438.2
	10	8	3.154	3.943	2.508
	0.08	0.02	687.1	896.1	488.1
I_{dOff} *[A/µm]*	0.17	0.02	1.167e-08	5.98e-08	2.1e-09
	0.17	0.024	5e-09	2.272e-08	1.019e-09
	0.5	0.02	1.427e-08	4.579e-08	4.232e-09
	10	8	1.767e-10	1.097e-09	2.68e-11
	0.08	0.02	8.038e-09	7.221e-08	8e-10
g_m *[µA/V/µm]*	0.17	0.02	8.39e+02	9.14e+02	7.23e+02
	0.17	0.024	7.15e+02	7.81e+02	6.31e+02
	0.5	0.02	6.72e+02	71.5e+02	5.96e+02
	10	8	1.82e+00	2.04e+00	1.79e+00
	0.08	0.02	8.43e+02	9.59e+02	7.11e+02
g_{ds} *[µA/V/µm]*	0.17	0.02	5.43e+01	6.94e+01	3.88e+01
	0.17	0.024	3.49e+01	4.42e+01	2.61e+01
	0.5	0.02	4.55e+01	5.58e+01	3.46e+01
	10	8	2.52e-03	2.84e-03	2.59e-03
	0.08	0.02	5.26e+02	7.09e+02	3.57e+02

Table 2-3: Extracted DC parameters for PFET device.

2.4.4 Device capacitances.

To finalize this characterization, device capacitances are extracted to capture switching-relevant parasitics. The total gate capacitance (C_{gg}) determines input loading and directly impacts dynamic power, while the gate–drain capacitance (C_{gd}) is associated with Miller coupling, affecting edge rate, feedthrough, and timing. In addition to reporting (C_{gg}), the individual gate capacitance components (C_{gs}, C_{gd}, and C_{gb}) are also extracted to verify charge partitioning consistency, i.e. $C_{gg} \approx C_{gs} + C_{gd} + C_{gb}$.

Capacitances are evaluated at a representative on-state bias condition to reflect typical switching operation. For the NFET, values are extracted at ($V_{GS} = V_{DS} = V_{DD} = 0.8$ V); for the PFET, the

corresponding bias is used ($V_{GS} = V_{DS}$ = -0.8 V). Results are reported for the reference geometry (W/L = 0.17µm/0.02µm) across the TT, SS, and FF process corners at (T = 25 ºC).

In addition to the terminal capacitances, the total gate capacitance is further decomposed following the GF convention. The intrinsic gate-to-channel capacitance in inversion, ($C_{gc,\,INV}$), represents the portion of the gate capacitance associated with channel charge under strong inversion, while C_{ov} captures the largely geometry-driven overlap/fringing contribution that remains even when the device is biased off.

When overlap-only model terms are not directly available, these quantities can be estimated from two operating points. The overlap component is approximated from an off-state condition with minimal channel charge:

$$C_{ov} \approx C_{gg} : (V_{GS} = 0, V_{DS} = V_{DD})$$

Comentado [JC7]: numerar

and is reported as (C_{ov}/2) when using the GF unit convention of fF/µm/side. The intrinsic inversion component is then estimated from an on-state condition in the linear region (to avoid pinch-off):

$$C_{gc,INV} \approx C_{gg} : (V_{GS} = V_{DD}, V_{DS} = V_{DS,lin})$$

Comentado [JC8]: numerar

This decomposition is useful because C_{ov} sets a bias-insensitive lower bound on input loading and Miller coupling (particularly relevant for fast edges and small devices), whereas $C_{gc,\,INV}$ quantifies the inversion-charge-related capacitance and therefore tracks effective gate control and on-state charge storage. Together, these metrics help explain technology- and corner-dependent differences in delay and dynamic power beyond what is visible from C_{gg} alone.

Parameter (units)	NFET - 22FDX-PLUS (T=25ºC)		
	TT	FF	SS
C_{gg} *(aF)*	178.2	178.7	176.5
C_{gs} *(aF)*	122.8	125.6	118.9
C_{gd} *(aF)*	53.51	51.59	55.33
C_{gb} *(aF)*	1.836	1.535	2.241
$C_{gc,\,INV}$ *(fF/µm)*	1.201	1.188	1.212
C_{ov} *(fF/µm/side)*	0.331	0.324	0.339

Table 2-4: NFET capacitances.

Parameter (units)	PFET - 22FDX-PLUS (T=25ºC)		
	TT	FF	SS
C_{gg} *(aF)*	199.7	198.2	200.8
C_{gs} *(aF)*	132.4	132.7	131.4
C_{gd} *(aF)*	66.39	64.81	68.09
C_{gb} *(aF)*	0.953	0.683	1.294
$C_{gc,\,INV}$ *(fF/µm)*	1.263	1.247	1.277
C_{ov} *(fF/µm/side)*	0.407	0.399	0.416

Table 2-5: PFET capacitances.

Table 2-4 and Table 2-5 summarize the extracted NFET and PFET gate-capacitance components for the reference geometry across the TT, FF, and SS process corners. The relatively small drain/source-related parasitic capacitances (notably C_{gd} and C_{gs}) are consistent with improved high-frequency output impedance, which is beneficial in current-steering DACs by supporting higher linearity (reduced harmonic content), higher output impedance, and improved frequency response [12].

2.5 LVT vs. SLVT devices.

Designing in FD-SOI is largely similar to designing in bulk CMOS, but it benefits from improved substrate isolation. In FD-SOI, the channel formed under the gate-oxide is separated from the well (back-gate) by a thin buried oxide (BOX) layer, which reduces junction capacitances and enables electrostatic control of the channel through the back-gate. This architecture provides additional flexibility: parasitic capacitances (notably source/drain junction capacitances) are reduced, the effective threshold voltage can be tuned through the device option, and well configuration (conventional well vs. flip-well) is available [12].

Figure 2-8 from [13] illustrates the FD-SOI cross-section and the corresponding well arrangements for n-FET and p-FET devices, highlighting the buried oxide (BOX), the well regions, and the back-gate (BG) contact that enables body-bias tuning.

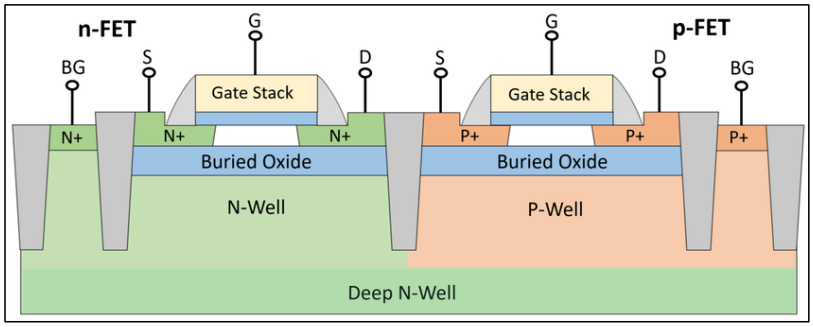


Figure 2-8: Cross section of the thin-oxide n-and p-MOSFETs in 22nm FDSOI.

In 22FDX, different device/well combinations are used to target specific speed–leakage trade-offs. In particular, flip-well devices place the transistor body in the opposite well type to enable stronger back-gate control and lower effective threshold voltage (e.g., SLVT options), whereas conventional-well devices use the standard well arrangement and are typically selected when lower leakage is prioritized:

- NMOS in N-well (flip-well) → super-low V_T (e.g. *slvtnfet*)
- PMOS in P-well (flip-well) → super-low V_T (e.g. *slvtpfet*)
- NMOS in P-well (conventional-well) → lower-leakage option (e.g. *nfet*)
- PMOS in N-well (conventional-well) → lower-leakage option (e.g. *pfet*)

Because low power is a primary design constraint in most practical applications, reduced-threshold devices are often selected to improve performance at low supply voltage, at the expense of increased leakage. The 22FDX PDK provides multiple threshold options; in this work, LVT (low-threshold-voltage) and SLVT (super-low-threshold-voltage) devices are evaluated.

Figure 2-9 from [14]summarizes the LVT/SLVT device options and associated well configurations used to realize LVT and SLVT transistors and to enable back-gate biasing through the well contacts. Conceptually, LVT devices rely on light channel doping and provide higher performance at the cost of increased leakage, while SLVT devices employ an (intrinsically) undoped channel and offer even higher speed, requiring careful thermal and leakage analysis. In the so-called flip-well construction, NFETs are implemented in an N-well (n-type back gate) and PFETs are implemented in a P-well (p-type back gate), strengthening back-gate control and enabling lower effective voltage threshold. Using identical dimensions and identical testbenches, LVT and SLVT devices are compared for both NFET and PFET in the following subsections.

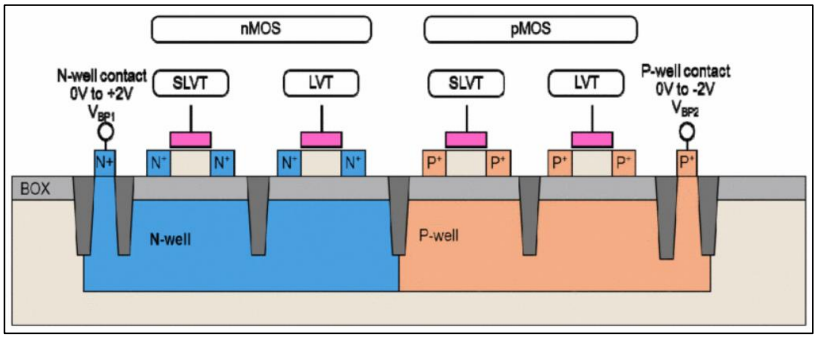


Figure 2-9: 22FDX flipped-well FET cross-section.

2.5.1 LVT vs. SLVT NFET characterization.

As in Section 2.4, this section characterizes and compares the LVT (*lvtnfet*) and SLVT (*slvtnfet*) NFET options using the same DC extraction methodology adopted for the baseline NFET. The testbenches used for the transfer and output characteristics are shown in Figure 2-10. Independent DC voltage sources bias the gate and drain terminals, while the source and bulk (body) terminals are tied to 0 V, enforcing (V_{BS} = 0 V). Device width (W) and length (L) are parameterized, and a single-finger configuration (nf=1) is used to keep the comparison consistent across device options.

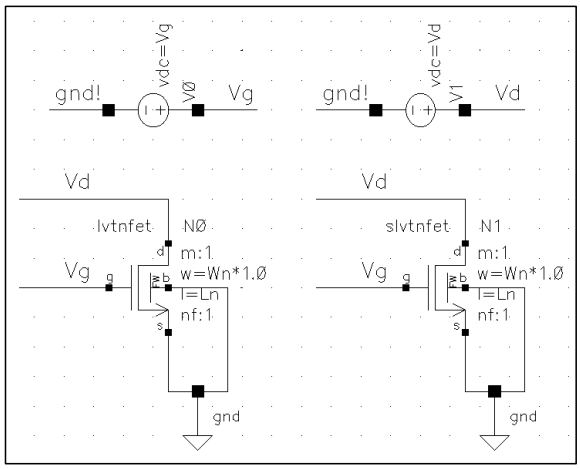


Figure 2-10: DC testbench schematic for LVT and SLVT NFET characterization.

To compare the behaviour of the LVT and SLVT devices, two standard DC sweeps are performed using the same bias sets as in Section 2.4, and the results are evaluated at several points of interest:

- **Transfer characteristic** (I_D - V_{GS}): V_{DS} equal to {0.05V, 0.3V, 0.6V, 0.8V, and 0.9V}.
- **Output characteristic** (I_D – V_{DS}): V_{GS} equal to {0.1V, 0.4V, 0.6V, 0.8V, and 0.9V}.

For all plots in this work, SLVT devices are shown with dash–dot–dot lines, while LVT devices are shown with solid lines. Unless otherwise stated, all graphs correspond to the reference geometry (W/L = 0.17µm/0.02µm); the baseline NFET is reported only in Section 2.4 to avoid overloading the figures.

Figure 2-11 plots the transfer characteristics and shows that the SLVT device conducts more current than the LVT device for the same V_{GS} across the entire sweep, with the largest differences observed in the subthreshold and moderate-inversion regions. This behaviour is consistent with SLVT's lower effective threshold voltage: the SLVT curves are shifted to lower V_{GS} (left) relative to LVT, indicating that a smaller gate voltage is required to reach the same drain current level.

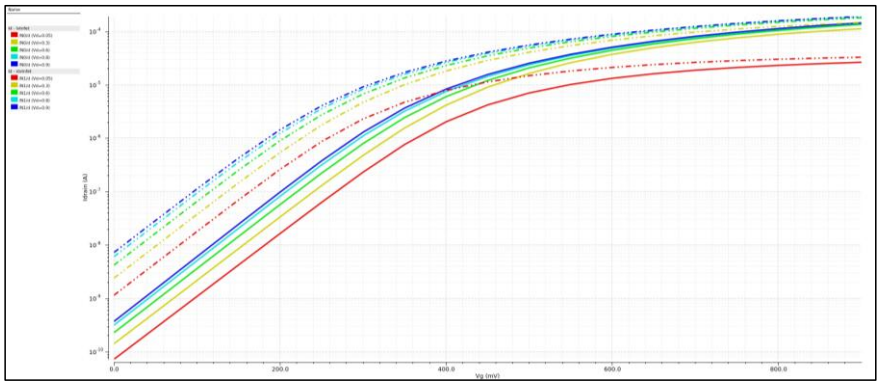


Figure 2-11: LVT and SLVT NFET transfer characteristic, I_D - V_{GS} with stepped drain bias.

Figure 2-12 plots the output characteristics and confirms the higher drive capability of the SLVT option. For any given V_{GS}, the SLVT curves exhibit higher drain current across the full V_{DS} range. In the low- V_{DS} region, this appears as a steeper slope (lower effective channel resistance), while at higher V_{DS} the SLVT device maintains a higher saturation current. These trends are consistent with SLVT being the higher-performance option and are reflected in the extracted I_{dSat} values.

Additionally, a finite slope of I_D versus V_{DS} is observed in saturation for both options, indicating channel-length modulation. Differences in this saturation-region slope correspond to differences in output conductance (g_{ds}) and thus intrinsic gain; this effect is quantified separately through g_m and g_{ds} extraction at a defined operating point.

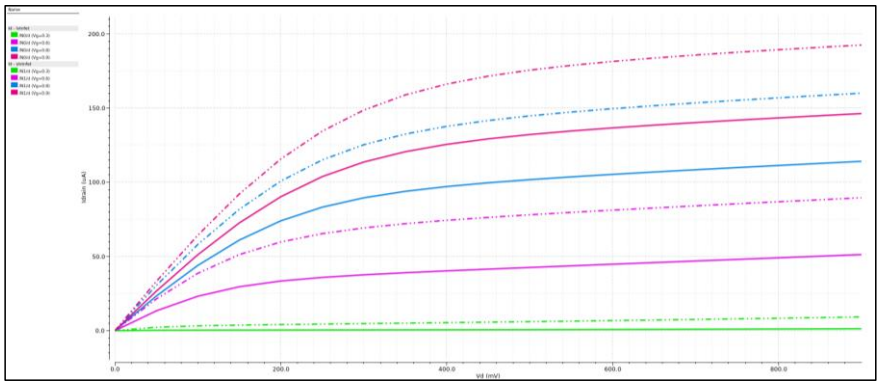


Figure 2-12: LVT and SLVT NFET output characteristic, I_D - V_{DS} with stepped gate bias.

To provide a compact numerical comparison, the same DC parameter-extraction flow described in Section 2.4 is applied to both LVT and SLVT devices. V_{thLin}, V_{thSat}, I_{dSat}, I_{doff}, g_m, and g_{ds} are extracted using identical bias definitions, enabling a direct, technology-consistent comparison between the two options.

Electrical Parameter	W (µm)	L (µm)	22FDX-PLUS (T=25°C)					
			LVTNFET			*SLVTNFET*		
			TT	**FF**	**SS**	**TT**	**FF**	**SS**
V_{thLin} *[mV]*	0.17	0.02	401.1	343	462.4	294	237.7	349
	0.17	0.024	405.9	350.5	463	297.4	244.3	348.8
	0.5	0.02	395	351.9	439.2	277.1	235.1	318.1
	10	8	479.7	452.8	506.3	336.9	311	362.4
	0.08	0.02	410.3	335.2	488.5	319.7	247.6	389.6
V_{thSat} *[mV]*	0.17	0.02	329.1	256.4	409.4	224.1	154.5	289.4
	0.17	0.024	347.7	282.6	418.5	243.4	181.8	301.9
	0.5	0.02	320	266.7	377.7	204.3	152.3	253.5
	10	8	468.6	441.8	495.1	328	302.1	353.4
	0.08	0.02	342.8	249.9	446.7	254.1	166.1	336.4
I_{dSat} *[µA/µm]*	0.17	0.02	655.1	848.1	451	923.5	1.111e3	732.4
	0.17	0.024	602.2	776	421.7	870.1	1.037e3	698.6
	0.5	0.02	648.6	785.1	501.8	926	1.052e3	787.4
	10	8	2.499	3.057	2.025	6.681	7.794	5.71
	0.08	0.02	680.2	943.4	408.9	924.2	1.176e3	676.6
I_{dOff} *[A/µm]*	0.17	0.02	1.70e-09	1.46e-08	1.60e-10	3.32e-08	2.47e-07	4.81e-09
	0.17	0.024	5e-10	3.72e-09	6.08e-11	1.07e-08	7.05e-08	1.77e-09
	0.5	0.02	2.19e-09	1.09e-08	3.82e-10	6.28e-08	2.76e-07	1.48e-08
	10	8	2.58e-12	7.24e-12	2.82e-13	6.35e-12	1.17e-11	6.32e-13
	0.08	0.02	1.16e-09	1.77e-08	6.36e-11	1.18e-08	1.63e-07	9.77e-10
g_m *[µA/V/µm]*	0.17	0.02	1.17e+03	1.30e+03	1.00e+03	1.25e+03	1.36e+03	1.12e+03
	0.17	0.024	1.07e+03	1.19e+03	9.26e+02	1.16e+03	1.26e+03	1.04e+03
	0.5	0.02	1.13e+03	1.21e+03	1.00e+03	1.19e+03	1.26e+03	1.10e+03
	10	8	4.55e+00	4.66e+00	4.39e+00	5.50e+00	5.66e+00	5.34e+00
	0.08	0.02	1.25e+03	1.42e+03	1.01e+03	1.32e+03	1.49e+03	1.15e+03
g_{ds} *[µA/V/µm]*	0.17	0.02	9.38e+01	1.30e+02	5.20e+01	1.00e+02	1.34e+02	7.21 e+01
	0.17	0.024	6.78e+01	9.15e+01	3.99e+01	6.95e+01	9.14e+01	5.12e+01
	0.5	0.02	9.41e+01	1.19e+02	6.46e+01	1.00e+02	1.23e+02	7.97e+01
	10	8	6.68e-03	6.98e-03	6.12e-03	6.69e-03	7.37e-03	6.09e-03
	0.08	0.02	9.40e+01	1.43e+02	3.83e+01	9.89e+01	1.45e+02	6.39e+02

Table 2-6: Extracted DC parameters for LVTNFET and SLVTNFET.

The extracted parameters in Table 2-6 confirm the trends observed in the transfer and output characteristics: compared to LVTNFET, SLVTNFET devices exhibit substantially lower threshold voltages and higher drive current, at expense of a significant increase in off-state leakage.

For the reference geometry (W/L = 0.17µm/0.02µm), the extracted saturation threshold voltage (V_{thSat}) decreases from 329.1/256.4/409.4 mV (LVT, TT/FF/SS) to 224.1/145.5/289.4 mV (SLVT, TT/FF/SS), corresponding to reductions of approximately 105 mV (TT), 111 mV (FF), and 120 mV (SS). A similar reduction is observed for V_{thLin}, indicating that SLVT consistently shifts the device characteristics toward lower-V_{GS} operation across drain-bias conditions.

This lower threshold translates into higher ON current. For the reference geometry (W/L = 0.17µm/0.02µm), I_{dSat} increases from 655.1/848.1/451 µA/µm (LVT, TT/FF/SS) to 923.5/1.111×10³/732.4 µA/µm (SLVT, TT/FF/SS), i.e., an increase of approximately +41% (TT), +31% (FF), and +62% (SS). The same trend is maintained across the additional geometries reported, with SLVT providing the highest drive current in all corners.

As expected, the performance benefit is accompanied by a strong leakage penalty. For the same geometry, the extracted off-state current (I_{doff}) rises from (1.70×10⁻⁹)/(1.46×10⁻⁸)/(1.60×10⁻¹⁰)

A/µm (LVT, TT/FF/SS) to $(3.32\times10^{-8})/(2.47\times10^{-7})/(4.81\times10^{-9})$ A/µm (SLVT, TT/FF/SS), corresponding to roughly ×19.5 (TT), ×16.9 (FF), and ×30 (SS) higher leakage. Therefore, while SLVT improves speed (higher I_{dSat}, lower V_T), it requires careful consideration of standby power, particularly in the FF and TT corners where I_{doff} is highest.

As a second reference point, the same comparison can be repeated for a wider device (W/L = 0.5µm/0.02µm), showing that the SLVT-LVT trends are maintained beyond the minimum-width case. For this geometry, the extracted V_{thSat} decreases from 320/266.7/377.7 mV (LVT, TT/FF/SS) to 204.3 mV/152.3/253.5 mV (SLVT, TT/FF/SS), corresponding to a reduction of approximately 116 mV (TT), 114 mV (FF), and 124 mV (SS). A similar shift is observed for V_{thLin}, confirming a consistent threshold shift across drain-bias conditions.

This threshold reduction produces a clear increase in ON current. The extracted I_{dSat} increases from 648.6/785.1/501.8 µA/µm (LVT, TT/FF/SS) to $926/1.052\times10^{3}/787.4$ µA/µm (SLVT, TT/FF/SS), i.e., approximately +43% (TT), +34% (FF), and +57% (SS).

The leakage penalty remains significant. For (W/L = 0.5µm/0.02µm), the extracted off-state current (I_{doff}) increases from $(2.19\times10^{-9})/(1.09\times10^{-8})/(3.82\times10^{-10})$ A/µm (LVT, TT/FF/SS) to $(6.28\times10^{-8})/(2.76\times10^{-7})/(1.48\times10^{-8})$ A/µm (SLVT, corresponding to roughly ×28.7 (TT), ×25.3 (FF), and ×38.7 (SS) higher leakage. Overall, these wide-device results reinforce that SLVT consistently improves drive strength and reduces threshold voltage, but at the cost of a significant increase in off-state current across all corners.

Comentado [JC9]: Es el motivo por el que utilizamos lvt entonces?

2.5.1.1 LVT vs. SLVT NFET capacitances.

To complete the LVTNFET–SLVTNFET comparison, gate-related capacitances are extracted to quantify switching-relevant parasitics. In particular, C_{gg} captures the dominant input loading, while C_{gd} accounts for Miller coupling and can affect edge rate, feedthrough, and timing. The individual components (C_{gs}, C_{gd}, and C_{gb}) are also reported to confirm consistent gate-capacitance partitioning:

$$C_{gg} \approx C_{gs} + C_{gd} + C_{gb}$$

Capacitances are evaluated at the same ON-state operating point used in Section 2.4.4, (V_{GS} = V_{DS} = V_{DD} = 0.8 V), (V_{BS} = 0 V). Results are reported for the reference geometry (W/L = 0.17µm/0.02µm) across TT, FF, and SS corners at 25ºC.

Parameter [Unit]	22FDX-PLUS (T=25ºC)					
	LVTNFET			*SLVTNFET*		
	TT	**FF**	**SS**	**TT**	**FF**	**SS**
C_{gg} *[aF]*	176	176.1	174.7	179.9	180.2	179.1
C_{gs} *[aF]*	121.4	123.6	117.5	122.2	125	118.9
C_{gd} *[aF]*	52.35	50.65	54.54	55.89	53.75	57.83
C_{gb} *[aF]*	2.26	1.92	2.71	1.81	1.42	2.29
$C_{gc\ INV}$ *[fF/µm]*	1.188	1.176	1.198	1.202	1.184	1.218
C_{ov} *[fF/µm/side]*	0.328	0.321	0.336	1.338	0.330	0.348

Table 2-7: Parasitic capacitances for LVT and SLVT NFET devices.

The extracted capacitances Table 2-7 indicate that SLVTNFET exhibits a slightly larger total gate capacitance than LVTNFET across all corners. Specifically, C_{gg} increases from 176.0–174.7 aF (LVT, TT–SS) to 179.9–179.1 aF (SLVT, TT–SS), i.e., a modest ~2–3% increase.

Looking at the partitioned capacitances, the increase is mainly associated with C_{gd}, which rises from 52.35–54.54 aF (LVT) to 55.89–57.83 aF (SLVT), while C_{gs} remains of comparable magnitude (differences of a few aF depending on corner). The back-gate component C_{gb} is comparatively small in all cases (≈1–3 aF), but shows some corner dependence. The reported values also satisfy the expected consistency, i.e., ($C_{gg} \approx C_{gs} + C_{gd} + C_{gb}$) within rounding error.

Overall, SLVTNFET achieves the expected performance gain but with a small capacitive penalty: C_{gg} increases by only ~2–3%, largely driven by a higher C_{gd} (Miller component), while the inversion-related term $C_{gc\ INV}$ remains similar between options. The extracted C_{ov} is also higher for SLVT across corners, suggesting increased overlap/fringing contribution, which is consistent with the observed C_{gd} increase. In practice, this added input/Miller loading can slightly reduce speed gains in heavily loaded nodes and marginally increase dynamic power.

Comentado [JC10]: •That's a big problem in our architecture.

If the flip-flops are heavily loaded (large clock tree, large fanout, or they directly drive sizable gate loads such as big switch gates, thermometer decoders, or retiming chains), the higher **input capacitance** (clock/data pin capacitance) and especially higher **Miller-related effects** can:

•
•increase **clock dynamic power** (clock toggles every cycle),
•slow down edges (more load for the same driver),
•increase **clock-to-Q / setup time** slightly if internal node capacitances are also higher. In this case, SLVT's higher (I_{D,sat}) often still improves speed, but the gain can be **smaller than expected**, and clock power can rise.
•**If leakage/standby power matters** (battery/always-on, long idle, stringent static power budget), SLVT is often the bigger issue because (I_{off}) can rise by **orders of magnitude**. A bank of SLVT flops can dominate standby power, especially in FF/TT corners and at high temperature.
•**If the flip-flops are not the critical path** (DAC settling dominated by analog switch RC, output buffer, reference settling, or mismatch/noise limits), then SLVT in flops may bring little benefit while still costing leakage and clock power—so it's usually not the best trade.

Practical guidance (common in mixed-signal IDACs):

•Use **LVT (or even RVT)** for most state-holding logic and clocked storage if standby power matters.
•Use **SLVT only where you truly need speed**, e.g., a small subset of timing-critical flops on the fastest clock boundary.
•Consider **body-bias** (if available in your flow) to tune (V_T): forward body-bias for speed in active mode, reverse body-bias for leakage in standby.

2.5.2 LVT vs. SLVT PFET characterization.

This section extends the threshold-option comparison to PFET devices by characterizing and contrasting the LVT (*lvtpfet*) and SLVT (*slvtpfet*) variants using the same DC methodology described in Section 2.4 and previously applied to NFET options in Section 2.5.1. The testbench topology is presented in Figure 2-13: independent DC sources bias the gate and drain terminals, while the source and bulk are tied to the well potential (for PFET, ($V_{SB} = V_{DD}$), i.e., (VSB = -0.8 V). Device geometry (W/L) is parameterized, and a single-finger configuration (nf=1) is used to keep the comparison consistent across device options.

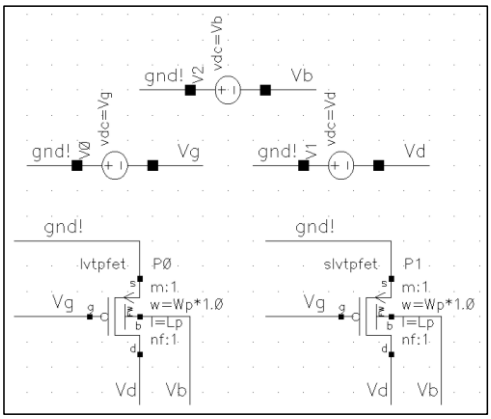


Figure 2-13: DC testbench schematic for LVT and SLVT PFET characterization.

Two sweeps are performed to capture the main operating regions:

- **Transfer characteristic ($I_D - V_{GS}$):** the gate bias is swept while V_{DS} is stepped across the same set of values used previously. Figure 2-14 shows the expected shift between threshold options for the reference geometry (W/L = 0.17µm/0.02µm): for the same V_{GS} at fixed V_{DS}, the SLVTPFET exhibits a higher drain current than the LVTPFET, indicating a lower effective threshold-voltage magnitude for the SLVT option. As V_{GS} increases toward V_{DD}, the separation between the curves reduces and both devices approach similar strong-inversion behaviour, although SLVT remains the higher-current device.

  The stepped-V_{DS} curves also highlight drain-bias sensitivity near threshold: increasing V_{DS} increases I_D for a given V_{GS}, with a more pronounced separation at lower V_{GS}. This behaviour is consistent with drain-induced barrier lowering (DIBL), which is typically more evident in lower-V_{th} options.

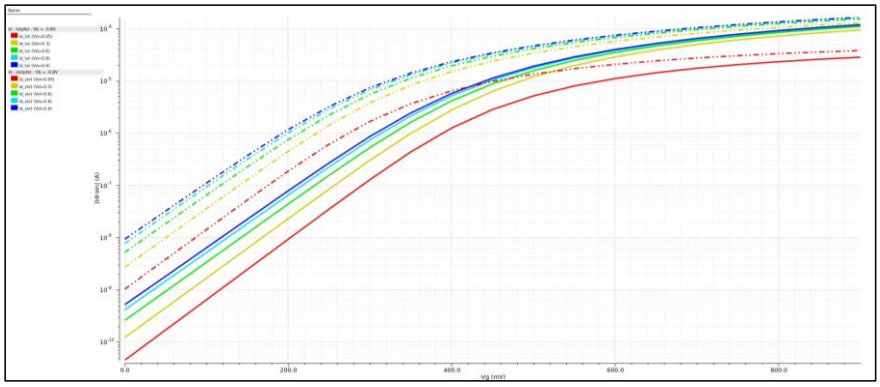


Figure 2-14: LVT and SLVT PFET transfer characteristic, I_D – V_{GS} with stepped drain bias.

- **Output characteristic (I_D – V_{DS}):** the drain bias is swept while V_{GS} is stepped up to the nominal supply magnitude. Figure 2-15 confirms the increased drive capability of SLVTPFET. For each stepped V_{GS}, SLVT delivers higher $|I_D|$ across the full V_{DS} range. In the low- V_{DS} region, SLVT exhibits a steeper slope, indicating a lower effective channel resistance at the same gate bias. As V_{DS} increases both devices transition toward saturation while maintaining a consistent current offset in favour of SLVT. These trends are reflected in the extracted I_{dSat} values. In addition, the finite slope in the saturation region motivates the subsequent comparison of g_{ds} (output conductance) extracted at the defined operating point.

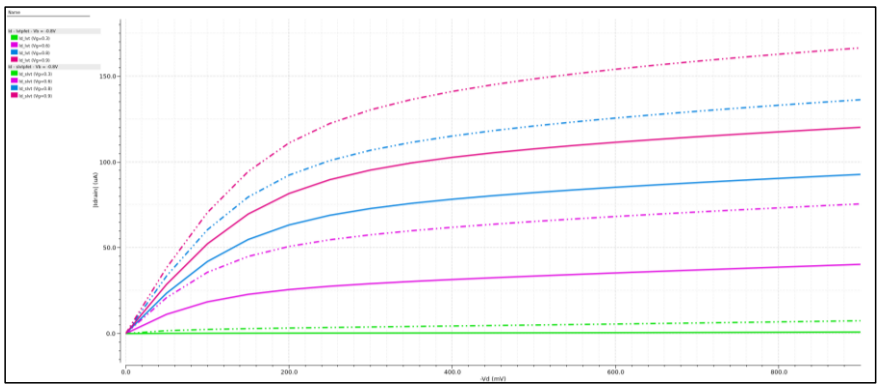


Figure 2-15: LVT and SLVT PFET output characteristic, I_D – V_{DS} with stepped gate bias.

Table 2-8 summarizes the extracted DC parameters for LVTPFET and SLVTPFET devices across TT, FF, and SS corners at 25 ºC. The reported metrics include V_{thLin} and V_{thSat}, the ON-state drive current (I_{dSat}), the off-state leakage (I_{doff}), and the small-signal parameters g_m, and g_{ds}. Results are provided for multiple (W, L) geometries to capture sizing dependence and to enable a consistent LVT–SLVT comparison under identical bias definitions.

Electrical Parameter	W (µm)	L (µm)	22FDX-PLUS (T=25ºC)					
			LVTPFET			*SLVTPFET*		
			TT	**FF**	**SS**	**TT**	**FF**	**SS**
V_{thLin} *[mV]*	0.17	0.02	-358.5	-302.8	-418.4	-243.7	-185.3	-303.3
	0.17	0.024	-364.1	-312.2	-420.2	-251.4	-197.6	-306.9
	0.5	0.02	-359.2	-319.6	-401.3	-239.5	-197.9	-282.9
	10	8	-380.9	-347.1	-416.4	-246.8	-215.4	-280.6
	0.08	0.02	-361.9	-288.5	-441.6	-264	-188.9	-340.4
V_{thSat} *[mV]*	0.17	0.02	-285.9	-219.8	-359.5	-172.2	-107.8	-240.4
	0.17	0.024	-305.8	-246.7	-371.1	-194.4	-134.2	-256
	0.5	0.02	-284.9	-237.3	-336.9	-166.3	-94	-217.6
	10	8	-374.2	-340.6	-409.4	-240.9	-209.7	-274.5
	0.08	0.02	-292.2	-206.2	-388.7	-195	-109.5	-281.3
I_{dSat} *[µA/µm]*	0.17	0.02	532.4	687	368.3	783.6	948.7	622
	0.17	0.024	479	612.7	337.3	719.3	862.7	575.7
	0.5	0.02	425.6	512	327.7	654.7	770.2	543.1
	10	8	1.92	2.53	1.42	4.45	5.76	3.34
	0.08	0.02	549.9	771.5	339	839.4	1070.2	607.6
I_{dOff} *[A/µm]*	0.17	0.02	2.25e-09	1.26e-08	3.4e-10	4.27e-08	2.43e-07	7.32e-09
	0.17	0.024	8.97e-10	4.33e-09	1.62e-10	1.66e-08	8.44e-08	3.18e-09
	0.5	0.02	2.76e-09	9.32e-09	7.41e-10	5.42e-08	1.92e-07	1.47e-08
	10	8	2.79e-10	2.15e-09	3.59e-11	9.67e-11	4.52e-10	1.29e-11
	0.08	0.02	1.49e-09	1.52e-08	1.21e-10	2.06e-08	2.04e-07	2.02e-09
g_m *[µA/V/µm]*	0.17	0.02	6.56e+02	7.42e+02	5.52e+02	7.12e+02	7.79e+02	6.32e+02
	0.17	0.024	5.71e+02	6.44e+02	4.88e+02	6.36e+02	6.97e+02	5.63e+02
	0.5	0.02	5.39e+02	5.88e+02	4.73e+02	5.89e+02	6.44e+02	5.28e+02
	10	8	1.58e+00	1.69e+00	1.47e+00	1.86e+00	2.03e+00	1.69e+00
	0.08	0.02	6.45e+02	7.56e+02	5.29e+02	7.55e+02	8.65e+02	6.37e+02
g_{ds} *[µA/V/µm]*	0.17	0.02	5.24e+01	6.88e+01	3.43e+01	5.58e+01	6.97e+01	4.35e+01
	0.17	0.024	3.59e+01	4.58e+01	2.49e+01	3.87e+01	4.76e+01	3.08e+01
	0.5	0.02	4.32e+01	5.32e+01	3.19e+01	4.70e+01	5.83e+01	3.74e+01
	10	8	4.55e-03	4.80e-03	4.30e-03	2.16e-03	2.29e-03	2.02e-03
	0.08	0.02	5.42e+01	7.53e+01	3.26e+01	6.23e+01	8.07e+01	4.63e+01

Table 2-8: Extracted DC parameters for LVTPFET and SLVTPFET.

The extracted parameters in Table 2-8 confirm the qualitative trends observed in the transfer and output characteristics: compared to LVTPFET, SLVTPFET devices exhibit a reduced threshold-voltage magnitude and higher drive current, with a large penalty in off-state leakage.

For the reference geometry (W/L = 0.17µm/0.02µm), the extracted saturation threshold voltage (V_{thSat}) shifts from (-285.9/-219.8/-359.5) mV (LVT, TT/FF/SS) to (-172.2/-107.8/-240.4) mV (SLVT, TT/FF/SS). In terms of threshold magnitude, this corresponds to a reduction of approximately 114 mV (TT), 112 mV (FF), and 119 mV (SS). A similar shift is observed for V_{thLin}, indicating a consistent threshold reduction under both linear and saturation drain-bias conditions.

This threshold reduction increases ON current. For the same geometry, I_{dSat} increases from 532.4/687.0/368.3 µA/µm (LVT, TT/FF/SS) to 783.6/948.7/622.0 µA/µm (SLVT, TT/FF/SS), i.e., approximately +47% (TT), +38% (FF), and +69% (SS).

As expected, leakage increases substantially. The extracted off-state current (I_{doff}) rises from 2.25×10^{-9}/1.26×10^{-8}/3.4×10^{-10} A/µm (LVT, TT/FF/SS) to 4.27×10^{-8}/2.43×10^{-7}/7.32×10^{-9} A/µm (SLVT, TT/FF/SS), corresponding to roughly ×19.0 (TT), ×19.3 (FF), and ×21.5 (SS) higher

leakage. Therefore, while SLVT PFET options provide a clear performance advantage (higher (I_{dSat}) and lower ($|V_{th}|$)), they also require careful management of standby power.

2.5.2.1 LVT vs. SLVT PFET capacitances.

To complete the LVTPFET-SLVTPFET comparison, Table 2-9 summarizes the extracted PFET gate capacitances at 25ºC for the reference geometry (W/L = 0.17µm/0.02µm) across TT, FF, and SS corners. C_{gg} is reported as the primary input-loading metric, together with its partitioned components C_{gs}, C_{gd} (Miller), and C_{gb}. The component values satisfy $C_{gg} \approx C_{gs} + C_{gd} + C_{gb}$ within rounding error, confirming extraction consistency.

Parameter [Unit]	22FDX-PLUS (T=25ºC)					
	LVTPFET			*SLVTPFET*		
	TT	**FF**	**SS**	**TT**	**FF**	**SS**
C_{gg} *[aF]*	195.4	194.2	196	199.2	197.6	200.4
C_{gs} *[aF]*	127.9	128.9	126.3	130.9	131.1	130.2
C_{gd} *[aF]*	66.18	64.35	68.24	67.4	65.8	69.03
C_{gb} *[aF]*	1.22	0.96	1.54	0.90	0.69	1.16
$C_{gc\ INV}$ *[fF/µm]*	1.239	1.224	1.251	1.251	1.233	1.267
C_{ov} *[fF/µm/side]*	0.408	0.399	0.418	0.412	0.404	0.420

Table 2-9: Parasitic capacitances for LVT and SLVT PFET devices.

Overall, Table 2-9 shows that SLVTPFET has a modestly higher total gate capacitance (C_{gg}) than LVTPFET across all corners: LVTPFET (C_{gg} ≈ 195.4/194.2/196.0) aF (TT/FF/SS) versus SLVTPFET (C_{gg} ≈ 199.2/197.6/200.4) aF, i.e. an increase of ~2.1% (TT), ~1.8% (FF), and ~2.2% (SS). This is consistent with the partitioned values: C_{gg} increases slightly (127.9/128.9/126.3 → 130.9/131.1/130.2 aF), while C_{gd} also rises in TT and SS (66.18/64.35/68.24 → 67.40/65.80/69.03 aF), implying a minor increase in both input loading and Miller coupling. The body component C_{gb} remains small for both options (≈0.7–1.5 aF) and does not materially affect the comparison.

Using the model-decomposed terms, the inversion-related width-normalized capacitance ($C_{gc,\,INV}$) is only slightly higher for SLVT (1.251/1.233/1.267 fF/µm) than for LVT (1.239/1.220/1.251 fF/µm), indicating that the intrinsic strong-inversion gate-channel contribution is broadly similar between threshold options. By contrast, C_{ov} is consistently higher for SLVT (0.412/0.404/0.420 fF/µm/side vs. 0.408/0.399/0.418 for LVT), suggesting a small but systematic increase in overlap/fringing parasitics.

In summary, SLVT improves drive strength and g_m but substantially increases I_{doff}, while capacitance penalties remain modest. These extracted trends directly impact current-mirror performance through output resistance g_{ds}, bias efficiency g_m, and leakage, motivating the mirror and mismatch study in Section 2.6.

2.6 Current mirror, mismatch characterization.

To conclude Chapter 2, a current mirror is implemented and simulated to quantify device mismatch in the 22FDX technology. Current mirrors are widely used as bias generators in analog and mixed-signal circuits, and their accuracy is fundamentally limited by random mismatch between nominally identical transistors. Evaluating current-mirror mismatch therefore provides a practical circuit-level measure of matching performance, complementing the single-device DC characterization presented in the previous sections.

In addition to the large-signal and small-signal device characterization, random mismatch is a key limitation in high-precision analog design and often trades off with other performance parameters such as speed, leakage, and area. Even when two transistors are designed with identical geometry and placed in close proximity, microscopic process variations introduce random deviations in electrical parameters. As discussed in standard analog design literature, these imperfections

manifest primarily as device mismatch and—together with nonlinearity—are among the main non-idealities that bound achievable accuracy in practical circuits (e.g., current sources, bias networks, and data converters) **¡Error! No se encuentra el origen de la referencia.**.

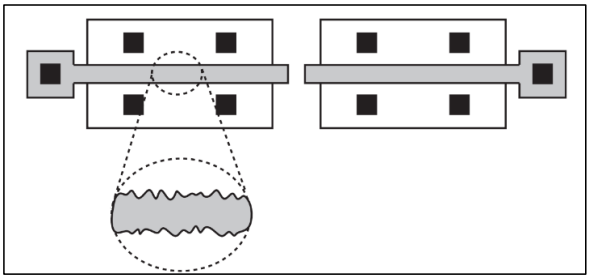


Figure 2-16: Random mismatches due to variations in device dimensions.

As illustrated in Figure 2-16 (reproduced from [15]), microscopic variations in device dimensions and material properties lead to random parameter deviations even for adjacent, identically drawn transistors. Accurate current matching is fundamental for IDAC unit elements and bias networks[16]; in current-steering DACs, unit-current mismatch directly increases DNL/INL and therefore limits achievable static linearity [7]. Although increasing device area improves matching, it increases parasitic capacitances and can limit high-frequency performance. As a common rule of thumb, quadrupling transistor area improves matching by roughly one bit, illustrating why extremely high-resolution matching requirements are impractical to satisfy by sizing alone [17].

A widely used insight is that larger device area reduces random mismatch through statistical averaging. In particular, Pelgrom's model relates the standard deviation of threshold mismatch between two closely spaced, identically laid out transistors to device area [12]:

$$\sigma(\Delta V_{TSat}) \approx \frac{A_{\Delta V_{thSat}}}{\sqrt{W \cdot L}}$$

Where $\sigma(\Delta V_{tSat})$ is the standard deviation of the threshold-voltage mismatch (expressed using the V_{thSat} definition), W and L are the transistor dimensions, and $A_{\Delta V_{thSat}}$ is the Pelgrom coefficient (units: V·m). The key design insight is therefore:

- Larger device area (W·L) yields lower mismatch, approximately scaling as $(1/\sqrt{(W \cdot L)})$.
- Smaller ΔV_{thSat} means better intrinsic matching technology, since less area is required to reach a given mismatch target.

Published GlobalFoundries data indicates that 22FDX exhibits lower V_{thSat} mismatch (lower ΔV_{thSat}) compared with common industry reference nodes (e.g., 28 nm HKMG and 40 nm LP), supporting its suitability for analog blocks that rely on well-matched devices (e.g., current sources and mirror arrays).

Finally, the operating point also influences how threshold mismatch translates into current error. In saturation, I_D depends strongly on the effective overdrive (V_{GS} - V_{TH}); therefore, operating with larger gate overdrive reduces the relative sensitivity of the drain current to random V_{th} variations and improves current-source matching [7]. For these reasons, current sources in high-accuracy DACs are typically implemented with longer-channel devices and biased in saturation [5].

2.6.1 Testbench description.

To quantify mismatch at circuit level, a basic two-transistor current mirror is implemented. One transistor is diode-connected to establish the reference current I_{REF}, and the second, nominally

identical transistor generates the mirrored current I_{OUT}. The devices use identical geometry (same W, L, and number of fingers) and are biased in saturation with sufficient compliance voltage to ensure proper operation. In the ideal case, $I_{OUT} = I_{REF}$; in practice, random mismatch introduces a mirror gain error between the two currents. In this work, the testbench is implemented for LVTNFET and LVTPFET devices, and the same procedure is repeated for SLVT options to assess how reduced Vth impacts matching and leakage.

Figure 2-17 shows the current-mirror testbench used in this work for both NFET (left) and PFET (right) devices. An ideal DC current source (I_{DC}) forces the reference current into the diode-connected device (N0/P0), whose gate and drain are shorted to generate the bias voltage (V_G) such that ($I_{REF} \approx I_{DC}$). The same gate node is then applied to a second, nominally identical device (N1/P1), producing the mirrored current (I_{OUT}).

To ensure both transistors operate under comparable drain bias, a unity-gain VCVS is used to enforce ($V_{D_0} \approx V_{D_1}$) (with the VCVS output limited to 0.8 V to maintain compliance). With both devices sharing the same (V_{GS}) and approximately the same (V_{DS}), deviations between IOUT and IREF are primarily attributed to random device mismatch.

Device dimensions W and L are parameterized, with a single finger (nf=1). The bulk is tied to the source for NFET ($V_B = 0$ V) and tied to V_{DD} for PFET, consistent with the biasing used throughout this chapter.

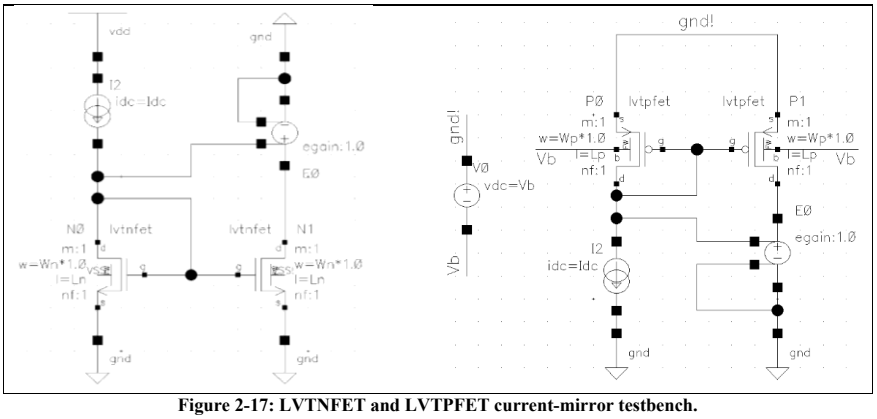


Figure 2-17: LVTNFET and LVTPFET current-mirror testbench.

2.6.2 Monte Carlo reports.

In this work, current-mirror mismatch is quantified using the standard deviation of the mirrored output current. For each Monte Carlo run, the drain current of the output device; N1 for NFET or P1 for PFET is recorded. For every (W, L) geometry and each (I_{DC}) bias point, 200 Monte Carlo samples are simulated. The simulator uses the standard Monte Carlo method with the variation option set to "All," so that all enabled statistical variability mechanisms provided by the PDK are included in the runs.

Table 2-10 and Table 2-11 report the standard deviation obtained for NFET current-mirror devices (LVT and SLVT options) at nominal temperature (25 ºC), for an I_{DC} sweep from 100 µA to 500 µA in 50 µA steps, and for progressively larger geometries while keeping the aspect ratio (W/L) constant (from 1 µm/20 nm to 16 µm/320 nm). In general, the results follow the expected trends: the absolute spread (σI_{OUT}) increases with I_{DC}, whereas the relative deviation (σ (%)) decreases as I_{DC} increases (i.e., the mirror becomes relatively more accurate at higher bias). In addition, increasing device area from 1 µm/20 nm to 8 µm/160 nm reduces mismatch, consistent with Pelgrom-type behaviour.

However, the largest device (16 µm/320 nm) does not continue this improvement and shows higher σ than the 8 µm/160 nm case. Since this size exceeds the PDK's recommended maximum device width, the result should be treated with caution: it likely reflects operation outside the model's intended geometry range rather than a true reversal of Pelgrom scaling. In this setup and bias range, the apparent non-monotonic behaviour may also be influenced by secondary effects such as operating-point sensitivity, non-idealities in the enforced V_D matching condition, or model/extraction limits for very large geometries.

	LVTNFET *(W / L)*									
I_{DC}	**1µm/20nm**		**2µm/40nm**		**4µm/80nm**		**8µm/160nm**		**16µm/320nm**	
[µA]	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)
100	14.49	14.49	9.50	9.5	7.17	7.17	6.85	6.85	7.87	7.87
150	18.10	12.06	12.13	8.09	9.27	6.18	8.89	5.93	10.23	6.82
200	20.93	10.46	14.30	7.15	11.06	5.53	10.64	5.32	12.26	6.13
250	23.28	9.31	16.14	6.45	12.63	5.05	12.19	4.87	14.07	5.62
300	25.29	8.43	17.75	5.91	14.05	4.68	13.60	4.53	15.71	5.23
350	27.07	7.73	19.18	5.48	15.34	4.38	14.90	4.25	17.23	4.92
400	28.66	7.16	20.46	5.11	16.53	4.13	16.10	4.02	18.65	4.66
450	30.11	6.69	21.63	4.8	17.63	3.91	17.22	3.82	19.98	4.44
500	31.46	6.29	22.71	4.54	18.66	3.73	18.28	3.65	21.24	4.24

Table 2-10: LVTNFET current-mirror output-current mismatch.

	SLVTNFET *(W / L)*									
I_{DC}	**1µm/20nm**		**2µm/40nm**		**4µm/80nm**		**8µm/160nm**		**16µm/320nm**	
[µA]	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)
100	11.21	11.21	8.36	8.36	6.45	6.45	6.23	6.23	7.27	7.27
150	13.86	9.24	10.62	7.08	8.34	5.56	8.11	5.41	9.49	6.33
200	15.89	7.95	12.43	6.22	9.93	4.97	9.72	4.86	11.41	5.71
250	17.51	7.00	13.95	5.58	11.32	4.53	11.14	4.46	13.11	5.24
300	18.86	6.29	15.25	5.08	12.55	4.18	12.42	4.14	14.65	4.88
350	20.00	5.71	16.38	4.68	13.66	3.9	13.60	3.89	16.07	4.59
400	21.00	5.25	17.39	4.35	14.68	3.67	14.68	3.67	17.40	4.35
450	21.87	4.86	18.29	4.06	15.61	3.47	15.70	3.49	18.64	4.14
500	22.66	4.53	19.10	3.82	16.47	3.29	16.65	3.33	19.81	3.96

Table 2-11: SLVTNFET current-mirror output-current mismatch.

Looking at Table 2-11 for the same (W/L) and I_{DC}, SLVT NFETs exhibit slightly lower σ I_{OUT} and σ (%) than the LVT option, indicating marginally improved current matching over the bias range considered. The same non-monotonic behaviour is still observed for the 16 µm/320 nm case, which is outside the recommended geometry range and is therefore treated cautiously.

To complete this section, PFET current-mirror mismatch results are summarized in Table 2-12 and Table 2-13 for LVT and SLVT devices at (25 ºC). The PFET mirrors show the same dependence on bias current and device area observed for NFETs (|σ I_{OUT}|) increasing with I_{DC} and relative σ (%) decreasing with I_{DC}. Comparing LVT and SLVT PFET options at identical (W/L) and I_{DC} further highlights the impact of threshold-voltage option on current matching.

PFET mirror mismatch results follow the same general behaviour observed for NFETs. Increasing device area reduces mismatch up to the 8 µm/160 nm geometry, consistent with Pelgrom-type scaling, whereas the 16 µm/320 nm case again shows non-monotonic behaviour and is treated cautiously since it exceeds the recommended maximum width range.

	LVTPFET *(W / L)*									
IDC	**1µm/20nm**		**2µm/40nm**		**4µm/80nm**		**8µm/160nm**		**16µm/320nm**	
[µA]	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)
100	10.19	10.19	6.95	6.95	5.70	5.70	6.33	6.33	8.02	8.02
150	12.57	8.38	8.59	5.73	7.30	4.87	8.18	5.45	10.39	6.93
200	14.61	7.3	9.86	4.93	8.62	4.31	9.75	4.88	12.39	6.19
250	16.60	6.64	10.83	4.33	9.75	3.9	11.13	4.45	14.17	5.67
300	18.59	6.20	11.73	3.91	10.63	3.54	12.36	4.12	15.78	5.26
350	20.53	5.87	12.57	3.59	11.41	3.26	13.51	3.86	17.29	4.94
400	21.87	5.47	13.45	3.36	12.08	3.02	14.47	3.62	18.63	4.66
450	23.44	5.21	14.14	3.14	12.68	2.82	15.38	3.42	19.85	4.41
500	25.19	5.04	14.85	2.97	13.13	2.63	16.23	3.25	21.02	4.20

Table 2-12: LVTPFET current-mirror output-current mismatch.

	SLVTPFET *(W / L)*									
I_{DC}	**1µm/20nm**		**2µm/40nm**		**4µm/80nm**		**8µm/160nm**		**16µm/320nm**	
[µA]	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)	σ (µA)	σ (%)
100	8.92	8.92	6.48	6.48	4.89	4.89	5.23	5.23	6.56	6.56
150	10.62	7.08	7.97	5.31	6.30	4.20	6.77	4.51	8.49	5.66
200	12.02	6.01	9.06	4.53	7.45	3.73	8.09	4.05	10.16	5.08
250	13.13	5.25	9.90	3.96	8.43	3.37	9.26	3.70	11.65	4.66
300	14.07	4.69	10.67	3.56	9.27	3.09	10.29	3.43	13.04	4.35
350	14.94	4.27	11.14	3.18	9.99	5.85	11.24	3.21	14.23	4.07
400	15.76	3.94	11.63	2.91	10.64	2.66	12.11	3.03	15.37	3.84
450	16.53	3.67	12.07	2.68	11.13	2.47	12.90	2.87	16.44	3.65
500	17.38	3.48	12.47	2.49	11.58	2.32	13.63	2.73	17.44	3.49

Table 2-13: SLVTPFET current-mirror output-current mismatch.

To finish, Figure 2-18 and Figure 2-19.plot the relative current-mirror mismatch for all evaluated device pairs, expressed as (σ (%)), as a function of the imposed reference current (I_{DC}). Each curve corresponds to one geometry (constant (W/L) while scaling area), and compares LVT (solid) versus SLVT (dashed) options for the same dimensions. The plots provide a compact visualization of the main trends extracted from Table 2-10 to Table 2-13: σ (%) decreases with increasing I_{DC} (improved fractional matching at higher bias), and mismatch generally improves with increasing device area up to the 8 µm/160 nm case, while the 16 µm/320 nm geometry shows the same non-monotonic behaviour discussed previously.

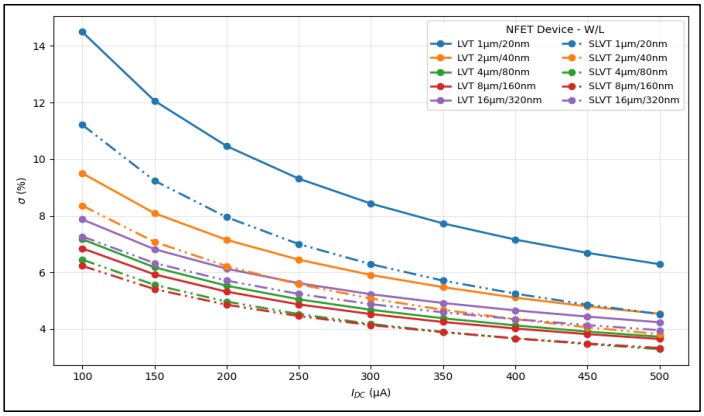


Figure 2-18: NFET current-mirror relative mismatch for LVT and SLVT devices.

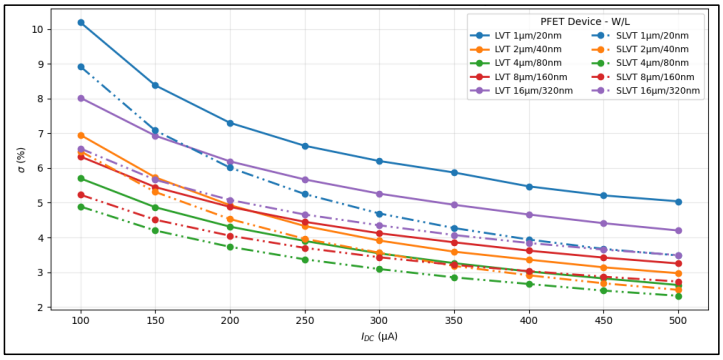


Figure 2-19: PFET current-mirror relative mismatch for LVT and SLVT devices.

This chapter links the extracted mismatch statistics to their circuit-level impact. In IDAC arrays, unit-current mismatch directly limits achievable static linearity by increasing DNL/INL. In bias networks, mismatch reduces bias accuracy and can shift device operating points, indirectly affecting timing margins and overall performance. The chapter concludes by assessing whether the observed mirror gain error is primarily dominated by random device mismatch at the selected geometries and bias conditions.

For additional context, and to close the chapter, GlobalFoundries reports Pelgrom-style mismatch metrics for 22FDX that are improved relative to a 40LP reference node for both NFET and PFET devices (Figure 2-20) [12]. The reported values suggest lower intrinsic threshold-related mismatch in 22FDX, consistent with the qualitative trends discussed in this chapter. This comparison is included as a benchmark; the absolute mismatch observed in this work also depends on the chosen device geometry, bias point, and the specific Monte Carlo/statistical options enabled in the simulator.

AΔvtsat (mV-µm)			
	40LP	22fdx	Diff
N	4.45	1.65	-63%
P	2.89	1.61	-44%

σ(Δvtsat) (mV)			
	40LP	22fdx	Diff
N	42	23.6	-44%
P	28	23.1	-18%

AΔidsat (%-µm)			
	40LP	22fdx	Diff
N	0.94	0.47	-50%
P	0.77	0.49	-36%

σ(Δidsat)/idsat (%)			
	40LP	22fdx	Diff
N	9.2	6.16	-33%
P	7.5	6.87	-8%

Figure 2-20: Vendor-reported 22FDX FET mismatch comparison versus a 40LP reference node.

Chapter 3. Flip-Flop design.

This chapter presents the main work of this thesis: the design, device-level characterization, and circuit-level simulation and verification of three flip-flop topologies in 22FDX technology. Flip-flops are fundamental sequential elements used in digital logic and in timing and synchronization blocks. Conceptually, a flip-flop can be interpreted as a one-bit memory element whose state is updated under clock control. Because sequential circuits inherently require storage, the selection and implementation of flip-flop structures directly impact speed, power consumption, robustness, and sensitivity to process and mismatch variability.

Memory elements can be classified according to the physical mechanism used to store information. In static storage, data is retained through bistability created by positive feedback (typically using cross-coupled CMOS inverters), enabling indefinite retention as long as the supply is present. In dynamic storage, information is stored as charge on a capacitance; this approach can reduce area and sometimes improve speed, but retention time is limited by leakage and noise and therefore depends on process, voltage, and temperature (PVT) conditions. A basic example is shown in Figure 3-1, which illustrates a capacitor-based storage cell from [18].

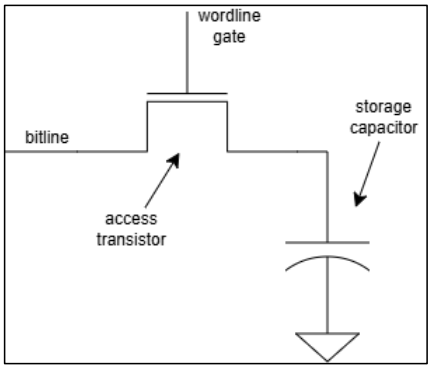


Figure 3-1: Storage capacitor.

The chapter is organized as follows. Section 3.1 reviews latch operation, establishing the intuition needed to interpret timing and robustness limitations. Section 3.2 introduces the basic circuit elements used throughout the designs—transmission gates and CMOS inverters—and discusses their role in signal transfer and state retention. Section 3.3 discusses registers/flip-flops from both static and dynamic storage perspectives and then presents the three implemented flip-flop topologies, describing their internal nodes and operation across clock phases. Finally, Section 3.4 details the simulation methodology and characterization metrics used in this work, including PVT analysis, clock-to-Q delay, setup/hold time, jitter sensitivity, metastability/MTBF, and power consumption.

Comentado [JC11]: Review cuando termines el capítulo

3.1.1 Latches as the building block.

Flip-flop architectures are most easily understood from a latch perspective. Most practical flip-flops are built from latches, with edge-triggered behaviour commonly obtained using a master–slave architecture: two latches are cascaded and controlled by complementary clock phases so that data is sampled in one phase and transferred to the output in the other. For this reason, understanding latch operation—transparency, regeneration, and the conditions that lead to metastability—is essential to analyse key flip-flop metrics such as clock-to-Q delay, setup/hold time, jitter sensitivity, and metastability robustness **¡Error! No se encuentra el origen de la referencia.**. In the following sections, the latch-level building blocks used in the implemented

designs are introduced, followed by a description of each flip-flop topology and its operation across clock phases.

Latches can be classified according to the active level of the enable (clock) signal into active-high and active-low latches. A latch operates in two modes: transparent and opaque (hold). When the latch is transparent, the output follows the input, i.e., (Q ≈ D). When the latch is opaque, the sampling path is disabled and the latch retains the last value of D captured during the active phase, thereby behaving as a memory element.

¡Error! No se encuentra el origen de la referencia. illustrates both cases. An active-high latch is transparent when (CLK = 1) and opaque when (CLK = 0). Conversely, an active-low latch is transparent when (CLK = 0) and opaque when (CLK = 1). The timing diagrams show the corresponding input–output behaviour for each latch type.

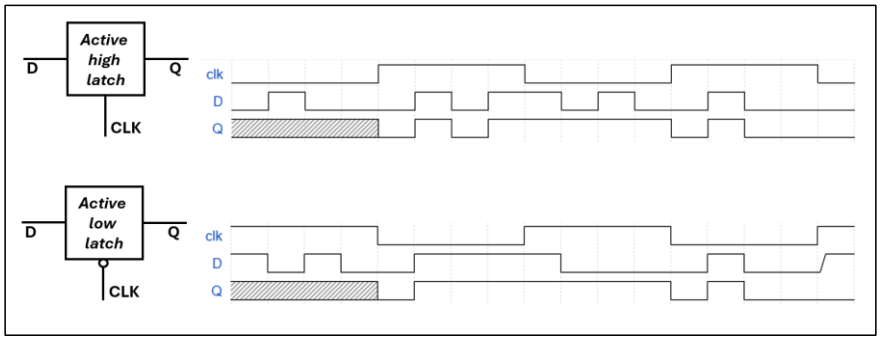


Figure 3-2: Active-high and active-low latch behaviour.

A level-sensitive latch can be conveniently interpreted as a 2:1 multiplexer with feedback, where the select line is the clock (or enable) signal. For an active-high latch, when (CLK = 1) the latch is transparent and the multiplexer selects the data input D, so (Q ≈ D). When (CLK = 0), the latch enters the hold phase and the multiplexer selects the feedback path, recycling the previously stored output value (Q_{old}) so that the output is maintained.

In a practical circuit, this "memory" action cannot be implemented with a passive wire alone, because during the hold phase the stored node must be actively driven to a valid logic level in the presence of leakage and noise. Robust static storage is therefore obtained using two cross-coupled CMOS inverters, which form a bistable element through positive feedback, as illustrated in Figure 3-3.

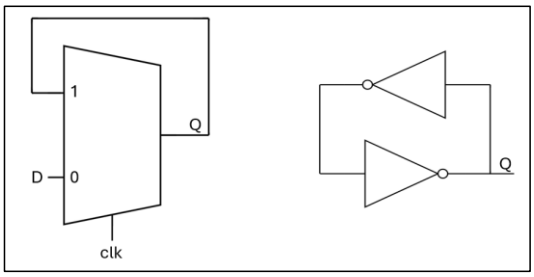


Figure 3-3: Latch interpretation using (left) a 2:1 multiplexer with feedback and (right) a static storage element implemented with cross-coupled inverters.

To make the latch transparent when (CLK = 1), the input D is conditionally connected to the internal storage node through an input switch S_1 (Figure 3-4). If the feedback path were left

enabled during this phase, the input driver would contend with the cross-coupled inverter pair, increasing effective loading, slowing transitions, and potentially preventing the internal node from being overwritten. To avoid this contention, a second switch, S_2, is inserted in the feedback path and driven by the complementary clock ($\overline{clk}$), so that the feedback is disabled when the latch is transparent and enabled during hold.

An additional inverter is placed before S_1 to preserve a non-inverting transfer characteristic at the latch level ((Q ≈ D) when transparent), while also buffering the input as it forces the bistable core to a new state.

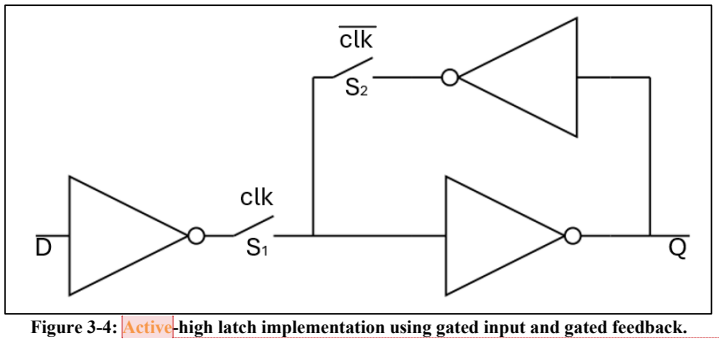


Figure 3-4: Active-high latch implementation using gated input and gated feedback.

Comentado [JC12]: Understand well how to design a active-low. Only changing the clokcs??

As a result, the latch operates in two non-overlapping configurations:

- Transparent mode (CLK = 1): S_1 ON and S_2 OFF, so the input path is enabled and Q tracks D. The corresponding equivalent circuit is show in Figure 3-5 (a).
- Hold mode (CLK = 0): S_1 OFF and S_2 ON, so the input is isolated and the cross-coupled inverters preserve the last stored value. The corresponding equivalent circuit is shown in Figure 3-5 (b).

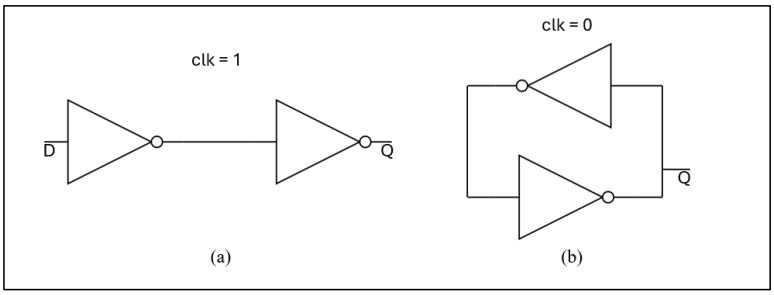


Figure 3-5: Equivalent circuits of an active-high latch in (a) transparent mode and (b) hold mode.

The ideal switches (S_1) and (S_2) are implemented using MOS devices (NMOS, PMOS, or CMOS transmission gates). The next section discusses switch implementations and motivates the use of transmission gates to ensure full-swing signal transfer.

3.2 Basic structures inside a latch.

At the circuit level, latches and flip-flops can be decomposed into two fundamental building blocks: switching elements that control when data is sampled, and restoring elements that preserve and regenerate logic levels. Although a switch can be implemented using a single NMOS or PMOS device, practical latch designs commonly employ CMOS transmission gates to pass both logic '0' and logic '1' with reduced signal degradation and improved noise margin. The storage

function is typically implemented using CMOS inverters, either as a static bistable element (cross-coupled inverters) or as a restoring stage associated with a dynamic storage node.

3.2.1 Transmission gate (T-gate) as a switch.

A MOS switch can be implemented using a single NMOS or PMOS device; however, a single pass transistor does not transfer full logic swing. An NMOS-only pass device conducts a strong logic '0', but when passing a logic '1' the output typically saturates around ($V_{DD} - V_{th,n}$), because the channel turns off as V_{GS} approaches $V_{th,n}$. Conversely, a PMOS-only pass device conducts a strong logic '1', but degrades a logic '0' and may stop near ($|V_{th,p}|$) above ground [2]. This threshold-drop behaviour can be observed in Figure 3-6.

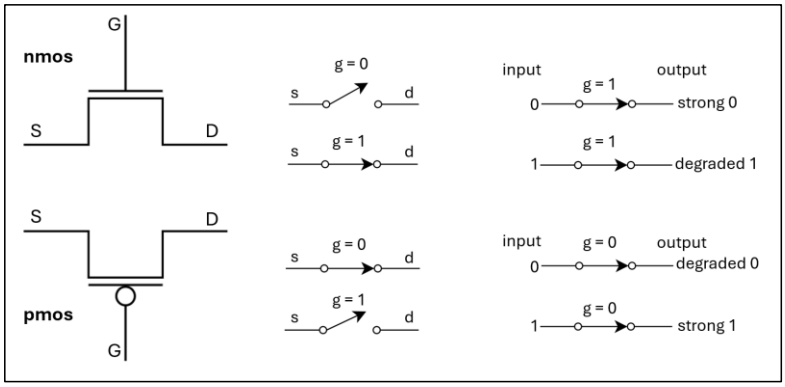


Figure 3-6: Pass transistor strong and degraded outputs.

To avoid this threshold-drop limitation, latches commonly use a CMOS transmission gate (T-gate), formed by an NMOS and PMOS in parallel. When enabled, the NMOS provides low resistance path for low-level transmission, while the PMOS provides a low resistance path for high-level transmission. As a result, the internal node can be driven close to both rails (0 and V_{DD}) reducing signal degradation and improving noise margins.

Proper operation requires complementary control signals (CLK) and ($\overline{CLK}$), ensuring that the NMOS and PMOS are either both ON or both OFF simultaneously. In master–slave and feedback-based latch structures, clock generation typically enforces non-overlap between complementary phases to prevent unintended transparent windows and to avoid momentary contention paths between the input and the feedback network. The complementary gating and full-swing transfer provided by a transmission gate are illustrated in Figure 3-7.

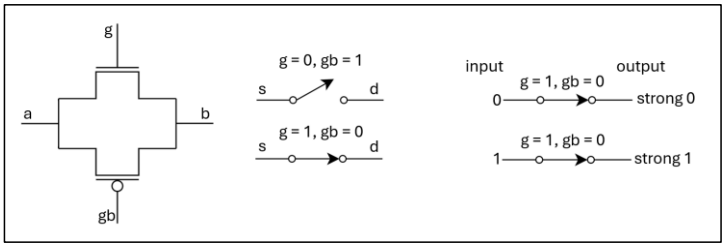


Figure 3-7: Transmission gate outputs.

Finally, although NMOS devices typically provide higher electron mobility (and therefore lower on-resistance for a given size), they also tend to exhibit stronger sensitivity to process and mismatch variations. Using both NMOS and PMOS devices in a transmission gate exploits the

complementary conduction strengths of each device polarity and helps preserve full-swing operation across PVT.

3.2.2 The inverter inside a latch.

The CMOS inverter is the fundamental restoring element in latch and flip-flop design. While the transmission gate controls when a node is sampled, the inverter determines how that node is regenerated to a valid logic level, provides gain for noise suppression, and ultimately sets key timing parameters such as propagation delay.

A CMOS inverter, illustrated in Figure 3-8, is formed by a PMOS pull-up device and an NMOS pull-down device connected in series between V_{DD} and ground, with a common input gate and a common output node. For a low input voltage ($V_{IN} \approx 0$), the PMOS is ON and the NMOS is OFF, so the output is pulled up to (V_{DD}). For a high input voltage ($V_{IN} \approx V_{DD}$), the NMOS is ON and the PMOS is OFF, so the output is discharged toward ground. In steady state, one of the two devices is ideally OFF, which leads to (approximately) zero DC static current, making CMOS inverters well-suited for storage elements that must retain state indefinitely in static latches [2].

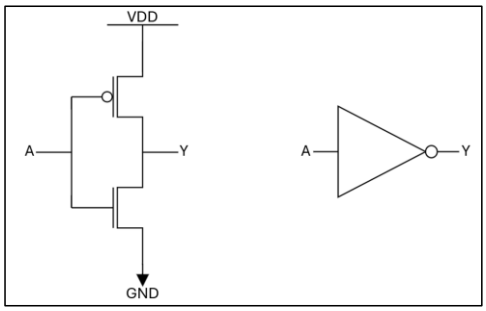


Figure 3-8: CMOS inverter schematic (left) and symbol (right).

In latch topologies, inverters appear both as buffers (to restore signal levels after a switch) and as storage cores when two inverters are cross-coupled to create bistability and static state retention. The voltage transfer characteristic (VTC), ($V_{OUT}(V_{IN})$), of an inverter captures their regenerative property, which exhibits a high-gain transition region where small input variations produce large output changes. This gain is the key mechanism that "cleans up" degraded or noisy internal nodes and improves robustness.

A key parameter of the VTC is the switching threshold (V_M) (often defined at ($V_{IN} = V_{OUT}$), which depends on the relative strength of the NMOS and PMOS devices. By sizing the PMOS wider than the NMOS (to compensate for lower hole mobility), designers typically target a near-symmetric VTC with ($V_M \approx V_{DD}/2$), which improves noise margins and balances rising and falling delays. If the sizing ratio is skewed, V_M shifts away from mid-supply, trading noise margin and timing symmetry for a preferred switching direction—sometimes useful in latch optimization, but generally undesirable for nominal logic robustness. This effect is illustrated in Figure 3-9, which presents a near-symmetric inverter transfer characteristic ($V_M \approx V_{DD}/2$) with a skewed sizing case where V_M is shifted away from mid-supply.

Device sizing therefore impacts latch behaviour in two ways: it sets the inverter strength ratio (and thus the switching threshold V_M and noise margins), and it also determines the effective drive strength and the capacitance presented to the previous stage. Increasing device widths reduces the pull-up/pull-down on-resistance and can improve speed for a fixed load, but it simultaneously increases gate and diffusion capacitances, raising the load seen by upstream nodes and increasing dynamic power. Consequently, inverter sizing involves a trade-off between robustness, delay, and switching energy—particularly important in flip-flops, where internal nodes and the clock network are heavily loaded. In the next subsections, these inverter properties are used to justify the chosen device sizing and to interpret timing and robustness trends observed in the implemented flip-flop topologies.

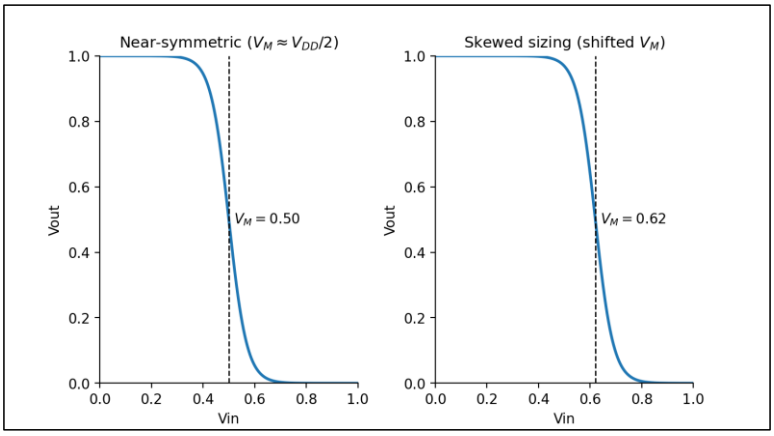


Figure 3-9: Representative CMOS inverter DC transfer characteristics.

3.3 Flip-flop designs.

In Section 3.1.1 latches were introduced as level-sensitive storage elements, and Section 3.2 reviewed the two key circuit primitives that implement them: the transmission gate (switching) and the CMOS inverter (restoring/storage). Building on these concepts, a flip-flop can be defined as a clocked storage element that samples its input only at discrete instants of time, typically on a clock edge, and holds the sampled value at its output for the remainder of the clock period.

Comentado [JC13]: Other options??

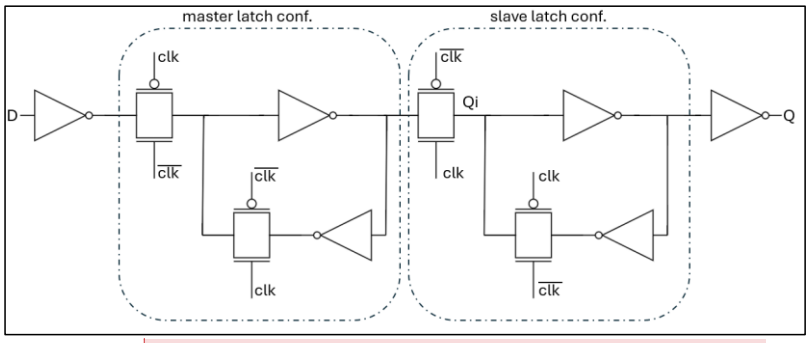


Figure 3-10: Master-slave flip-flop implemented by cascading two transmission-gate latches.

A common implementation of an edge-triggered flip-flop is the master–slave configuration, obtained by cascading two level-sensitive latches that are enabled on opposite clock phases. In Figure 3-10, when (clk = 1) the master latch is transparent and tracks D while the slave latch is in hold, isolating the output. When (clk = 0), the master enters hold and the slave becomes transparent, transferring the previously stored value at Q_i to the output Q. With complementary (and ideally non-overlapping) clocking, the two latches are never transparent at the same time, preventing race-through and yielding edge-triggered behaviour at Q.

Comentado [JC14]: REVIEW

Figure 3-11 illustrates the timing of a master–slave flip-flop, showing how D is first sampled onto the internal node (Q_i) during the master-transparent phase (blue-shaded region), and then transferred to the output (Q) during the slave-transparent phase (orange-shaded region) under complementary clocking (clk and clkb).

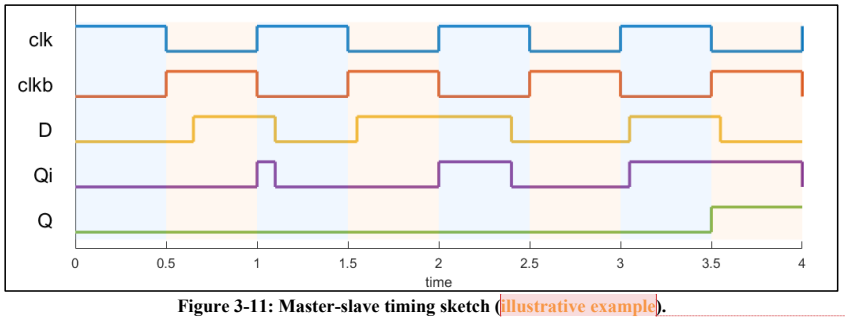


Figure 3-11: Master-slave timing sketch (illustrative example).

Comentado [JC15]: Review is well designed.

As we have seen in Section 3.1.1, latches are level-sensitive: when their enable or clock signal is active, they are transparent and the output (Q) follows the input (D). This transparency can be beneficial in synchronous systems by allowing time borrowing, which can relax setup requirements across clock boundaries. However, it also demands careful control of enable periods and clock signals to prevent race-through, where unintended changes in (D) can propagate to (Q) during the transparent interval.

In contrast, a flip-flop is edge-triggered: the output (Q) updates only at a specific clock transition, typically the rising or falling edge. This edge-triggered characteristic greatly simplifies timing analysis and closure in synchronous designs, since signal sampling occurs at a well-defined instant. However, implementing flip-flops generally requires higher area, increased power consumption, and greater clock loading compared to a single latch, since flip-flops are often built from two level-sensitive latch stages or equivalent internal circuitry. [Add]

Comentado [JC16]: If space allows. Draw a timing sketch showing difference as D-latch and fipflop output.
Althoug can be the same as figure 3.11

Flip-flops can also be classified by their storage mechanism:

- **Static storage:** The state is held by positive feedback, typically using cross-coupled CMOS inverters (e.g., Figure 3-4 and Figure 3-10). The stored value can be retained indefinitely as long as power is applied, and the node remains actively driven to a valid logic level. Static designs are generally more robust to leakage and noise, at the cost of increased transistor count and larger internal capacitance.
- **Dynamic storage:** The state is stored as charge on a capacitance at an internal node, usually through a clocked switch (e.g., a transmission gate). Dynamic structures can be more compact and can achieve high speed due to reduced transistor count and smaller internal nodes. However, the stored charge is gradually lost due to leakage currents, so the state can only be held reliably for a limited time; dynamic nodes are also more sensitive to noise, charge sharing, and clock feedthrough. Figure 3-12 illustrates a dynamic master-slave latch concept in which data is stored temporarily as charge on internal capacitances.

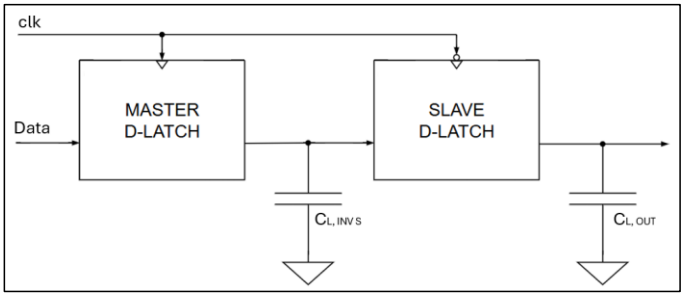


Figure 3-12: Master-slave C2MOS D-flip-flop block-level, adapted from [21].

These are only a few examples of latch and flip-flop designs. Different flip-flop topologies exist to meet specific speed, power, and robustness requirements, and the choice often depends on clock frequency, allowable clock loading, supply voltage, and noise/leakage constraints of the technology. In the following subsections, the flip-flop architectures considered in this work are presented and compared. Building on the latch-level concepts discussed above (transparency/hold behaviour, static vs. dynamic storage, and complementary clocking), each topology is analysed using a consistent simulation methodology and a common set of figures of merit, highlighting its operating principle (static or dynamic), clocking requirements, and the expected trade-offs in delay, power, and signal integrity across PVT corners.

3.3.1 Conventional transmission-gate flip-flop (TGFF).

A conventional transmission-gate flip-flop (TGFF) is an edge-triggered structure obtained by cascading two level-sensitive transmission-gate latches (master–slave). Each latch includes a static storage element implemented by a pair of cross-coupled CMOS inverters. This cross-coupled inverter pair forms a bistable feedback loop: once an internal node is driven to a valid logic level, the positive feedback continuously reinforces that state. In the ideal case (no leakage and perfect noise margins), the stored value is retained indefinitely as long as power is applied, since the inverters actively drive the storage nodes to either (0) or (V_{DD}). Figure 3-13 illustrates and example of this architecture, being the same structure as presented in Figure 3-10.

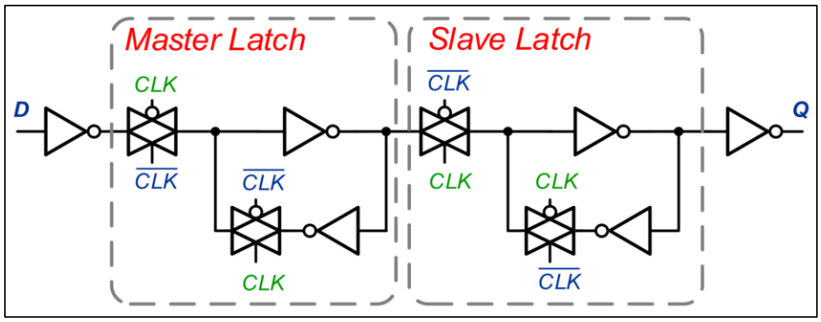


Figure 3-13: Schematic diagram of conventional TGFF, from ¡Error! No se encuentra el origen de la referencia..

This static storage mechanism provides important advantages for robust digital operation. First, because the storage node is always regenerated by a low-impedance CMOS path, static latches and flip-flops exhibit good noise margins and are generally less sensitive to leakage-induced voltage droop than dynamic nodes. Second, the full-swing restoration provided by the inverter pair improves immunity to signal degradation across PVT corners, which is particularly relevant at low supply voltages where reduced headroom can otherwise compromise logic levels.

However, these benefits come at a cost. Static latch-based structures require a larger number of transistors (transmission gates plus the cross-coupled inverter pair and associated buffers), which increases cell area and internal capacitance. The larger transistor count increases the total capacitance seen by the input and clock signals (mainly MOS gate capacitances) and also increases the capacitance of internal storage nodes (diffusion and gate loading). As a result, the clock network must charge/discharge a larger total gate capacitance every cycle, increasing dynamic power, and internal nodes may switch more slowly and dissipate more energy when they toggle.

In this work, the conventional TGFF is used as a baseline static topology, and its timing and power performance are compared against reduced-transistor and dynamic alternatives. The conventional structure is widely described as a reference design in standard reviews of CMOS flip-flops and low-power latch-based sequential elements.

3.3.2 Static C²MOS latch-based flip-flop.

A useful way to introduce the C²MOS latch is to begin from the concept of a clock-gated inverter: when the enable signal is active, the inverter evaluates and propagates the input, while in the inactive phase the signal path is disabled and the state is preserved by the inverter's regenerative behaviour. Figure 3-14 illustrates this idea and its compressed CMOS realization

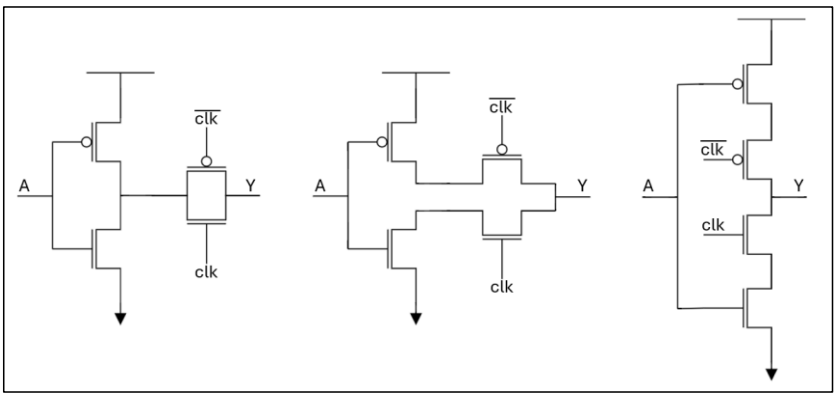


Figure 3-14: Clock-gated inverter concept and condensed realization, adapted from [2].

Figure 3-15 shows the static C²MOS latch implementation. In this structure, the clocked transistors are embedded in the pull-up and pull-down paths of an inverter such that, during the active clock phase, the latch is transparent and the output follows (D), whereas during the complementary phase the storage node is isolated, and the logic level is maintained by static regeneration. Because the stored value is held by an actively driven CMOS path rather than by charge on a floating capacitor, the latch is robust to leakage-induced droop and provides good noise margins. Figure 3-15 also highlights an important implementation constraint: the clocked devices must be arranged to correctly isolate the storage node during hold; an incorrect placement can lead to weak isolation or an undesired conduction path (illustrated by the "bad" configuration).

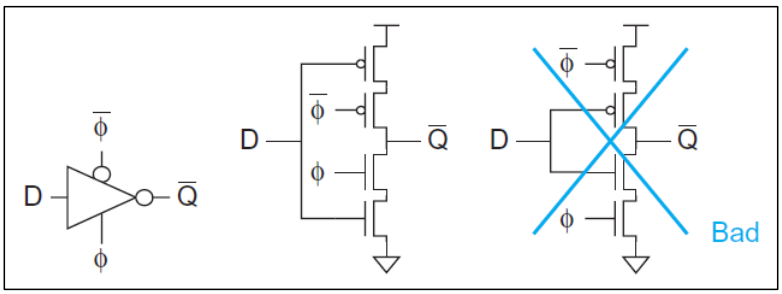


Figure 3-15: Static C²MOS latch; symbol (left), correct (middle) and wrong (right) implementations.

By cascading two C²MOS latches driven by complementary clock phases, an edge-triggered flip-flop can be obtained, as shown in Figure 3-16. The master latch samples the input during one phase, and the slave latch transfers the stored value to the output during the opposite phase. With complementary (and ideally non-overlapping) clocking, both latches are not transparent at the same time, preventing race-through and yielding edge-triggered behaviour at (Q). Building on this clocked-latch viewpoint, the same concept can be extended to dynamic high-speed sequential styles in which the state is stored primarily as charge on internal capacitances, enabling reduced transistor count and lower clock loading at high frequency.

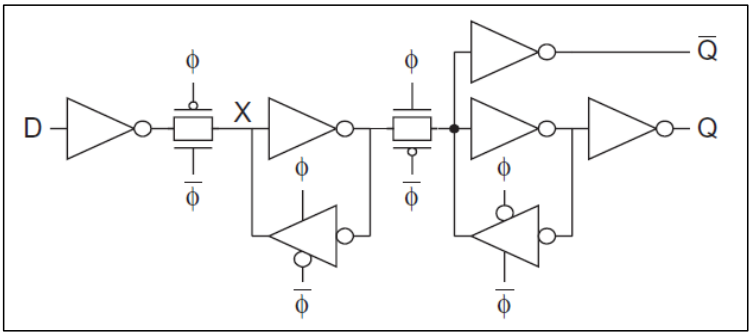


Figure 3-16: Master-slave flip-flop constructed from two C²MOS latches with complementary clocking [2].

3.3.3 Dynamic C²MOS capacitor-based flip-flop.

In a dynamic C²MOS-style flip-flop, the logic state is stored primarily as charge on the capacitance of internal nodes, rather than being maintained by a continuously active regenerative feedback loop. During sampling, clock-controlled devices update an internal node; during hold, the node becomes high-impedance, and the state is retained as charge on an effective capacitance. The master and slave sections operate on complementary clock phases, enabling edge-triggered behaviour in a master–slave arrangement while relying on dynamic node storage.

The effective storage capacitance is typically not an explicit capacitor but the sum of parasitics at the storage node, including drain diffusion (junction) capacitances of the transistors connected to the node, the gate capacitance of the following stage, and interconnect capacitance. As shown in Figure 3-17, the master latch samples the input onto an internal dynamic node (X), and the slave latch transfers the stored value to the output on the opposite clock phase; hence, the capacitances at node (X) and at the output strongly influence both retention time and switching speed.

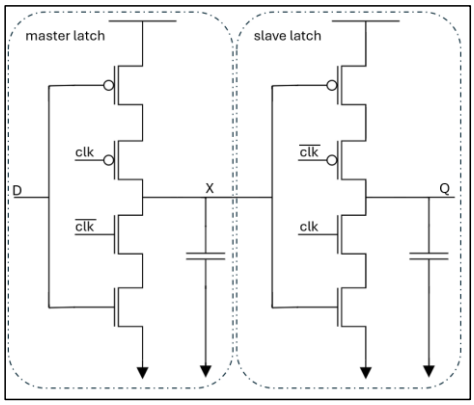


Figure 3-17: Dynamic C²MOS capacitor-based flip-flop.

A key limitation of dynamic storage is finite retention time: since the logic level is represented by charge on the node capacitance, leakage gradually causes the stored voltage to drift. Therefore, dynamic C²MOS flip-flops must be clocked so that the dynamic nodes are refreshed frequently enough to preserve correct logic levels under worst-case PVT conditions (notably low (V_{DD}) and cold temperature). Moreover, because the storage node is high impedance during hold, correct operation benefits from careful sizing and well-controlled clock transitions to mitigate disturbances such as capacitive coupling, charge sharing, and clock feedthrough/charge injection.

3.4 Architecture tests.

Once the flip-flop topologies for this work have been introduced in Sections 3.3.1 to 3.3.3, the discussion moves from a qualitative architectural comparison to a quantitative evaluation based on circuit simulation. The following subsections define the target specifications and describe the simulation testbenches and metrics used in this work. First, transmission-gate and inverter characterization is performed to parameterize technology- and sizing- dependent behaviour (including LVT vs. SLVT options). Then, the complete flip-flops are evaluated under the operating conditions of Table 3-1 to verify correct functionality across PVT variations and high-speed operation, and to assess suitability for the IDAC control logic under the required frequency and loading constraints.

Parameter	Min	Typ	Max	*Units*
Supply	0.76	0.8	0.84	V
Temperature	-40	25	150	ºC
F_{CLK}	3	-	7	GHz
C_{LOAD}	-	-	10	fF

Table 3-1: Test parameters description.

Table 3-1 summarizes the simulation conditions used throughout this chapter. The flip-flops are evaluated at a nominal supply voltage of (V_{DD} = 0.8 V) with a ± 5% variation, corresponding to a range of 0.76-0.84 V. The temperature sweep spans −40°C to 150°C to cover extended-temperature operation. A clock frequency range of 3–7 GHz is considered, and a 10 fF capacitive load is used at the output node to emulate the expected fanout and to enable a consistent comparison between architectures.

Comentado [JC17]: The point is, the output of a flip-flop does not drive an ideal wire, usually drives the gate capacitance of the next logic stage, some interconnect wire capacitance or possibly multiple gates (this is called fanout).

All of these effects can be modeled as a capacitance connected to the output node.

Parameter	Max	*Units*
Power down Current	1	µA
Current Consumption	500	µA
Clock2Q	80	ps
Setup Time	10	ps
Hold Time	10	ps
Clock2Q$_{mismatch}$ (rms)	0.4	ps
MTBF	5.00E+00	Years
Jitter(rms)	0.2	pSec
Rising Time	5	ps
Falling Time	5	ps
Duty Cycle	50 4%	%

Table 3-2: Flip-Flop metric's requirements.

Comentado [JC18]: Check, defined as same setup time.

Comentado [JC19]: Why this notation

Change to ps??

Table 3-2 lists the target limits adopted to compare the flip-flop implementations. Timing requirements are expressed in terms of clock-to-Q delay, setup and hold constraints, and the mismatch (rms) between clock-to-Q delay. Power targets include both active current consumption and power-down (leakage) current. To ensure that results are comparable across topologies and representative of the intended clocking environment, constraints on clock duty cycle and input transition time are also specified. Unless stated otherwise in each testbench, "active current" is measured with the clock running at the specified frequency and with a defined switching activity at the data input, while "power-down current" is measured with the circuit placed in its inactive

Comentado [JC20]: Input transition time is the time it takes for a signal to transition, from low (high rise time), from high (low fall time)

state (clock disabled and inputs held constant) so that the reported current reflects leakage-dominated operation.

Comentado [JC21]: Check

3.4.1 T-Gate characterization.

A transmission gate is used throughout the latch and flip-flop topologies presented in Section 3.3 as the sampling/feedback switch. Since flip-flop timing and power are strongly influenced by the transmission gate on-resistance and by any residual signal attenuation near the rails, this subsection characterizes a standalone T-gate under the operating conditions defined in Table 3-1.

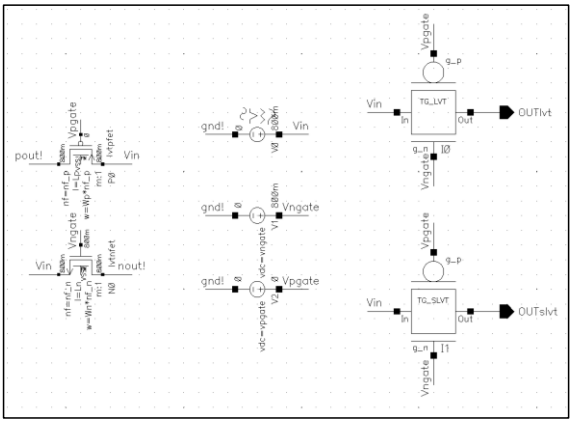


Figure 3-18: T-gate characterization testbench (single pass devices and TG implementations).

The characterization is performed using the basic two-terminal configuration, presented previously in Figure 3-7, with the NMOS and PMOS driven by complementary control signals (CLK and $\overline{CLK}$). Two clock states are considered: enabled (CLK = 1, $\overline{CLK}$ = 0) and disabled. (CLK = 0, $\overline{CLK}$ = 1). In the enable state, both devices conduct and the T-gate behaves as a low-resistance bidirectional switch, ideally yielding ($V_{OUT} \approx V_{IN}$). In the disabled state, both devices are off and the output node is isolated from the input.

Figure 3-18, shows the testbench used for the initial characterization. The left part illustrates the behaviour of single NMOS/PMOS pass devices and motivates the use of the complementary T-gate structure. The right part shows the two transmission-gate instances implemented in this work, using LVT and SLVT devices, respectively. For this initial test, both implementations use the same reference geometry (W/L = 0.17µm/0.02µm) and are driven by ideal complementary control levels (NMOS gate at (V_{DD}) and PMOS gate at 0 V in the enabled state).

To evaluate signal transfer under dynamic operation, (V_{in}) is driven by a 0–(V_{DD}) square wave while the transmission gate is held enabled, and the resulting (V_{OUT}) waveforms are recorded for each device option. Figure 3-19 shows a representative transient example at 7 GHz, highlighting the differences in output tracking between the LVT and SLVT transmission gates and the behaviour of single NFET and PFET pass transistors.

Comentado [JC22]: Repeat

After this transient evaluation, (V_{in}) is defined as a DC input and swept from 0 V to (V_{DD}) to extract the static transfer characteristic (V_{out} (V_{in})) of the LVT and SLVT transmission gates. The corresponding results are shown in Figure 3-20, where (V_{out}) closely follows (V_{in}) across the full input range under DC conditions. In practical clocked operation, however, the achievable tracking depends on the available ON time and on the timing relationship between complementary control signals, which must provide sufficient conduction time while avoiding unintended overlap during transitions.

While Figure 3-19 and Figure 3-20 verify correct signal transfer in transient and DC conditions, the next step is to quantify the effective on-resistance of the transmission gate, since this parameter directly sets the RC time constant when driving capacitive nodes and therefore impacts delay and dynamic power in the flip-flop architectures.

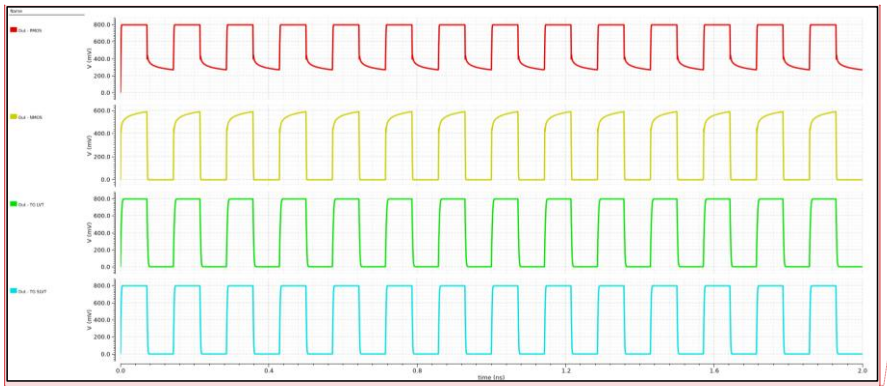


Figure 3-19: Transient signal output at 7 GHz, for NFET/PFET as pass devices and LVT/SLVT T-Gates.

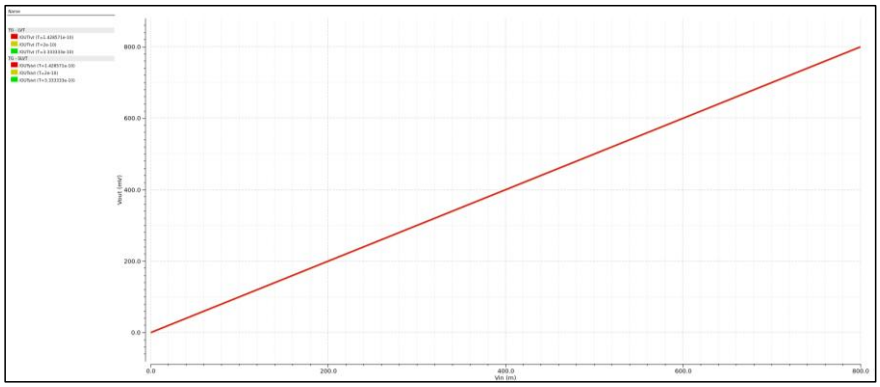


Figure 3-20: DC transfer characteristic of the transmission gate for LVT and SLVT implementations.

Finally, the effective conduction strength of the enabled transmission gate is summarized by extracting on-resistance. Practically, the enabled transmission gate can be modelled as a voltage-dependent on-resistance ($R_{on}(V)$) between (V_{in}) and (V_{out}). Since the NMOS and PMOS devices provide parallel conduction paths, the equivalent resistance can be interpreted as the parallel combination of both channel resistances:

$$R_{on} \approx R_{on,n} || R_{on,p} = \left(\frac{1}{R_{on,n}} + \frac{1}{R_{on,p}} \right)^{-1}$$

For each device, being in saturation:

$$R_{on} \approx R_{out} \approx \frac{1}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})} \approx \frac{1}{g_{ds}}$$

From the equations, it is straightforward to see that increasing device width reduces the effective resistance, while increasing channel length increases it. Therefore, both devices are kept at

Comentado [JC23]: Change graph, each signal different colour

Comentado [JC24]: enumerar

Comentado [JC25]: enumerar

Comentado [JC26]: Linkar la equation??

minimum channel length ($L_n = L_p = L_{min}$) to minimize R_{on} and avoid unnecessary parasitic capacitance. Because the transmission gate is used as a high-speed sampling switch, low R_{on} is desirable to reduce the RC time constant when driving capacitive internal nodes.

Table 3-3 and Table 3-4 summarize the extracted maximum (R_{on}) values for the LVT and SLVT transmission gates across the main PVT conditions considered in Table 3-1. For each corner, ($R_{on}(V)$) is firsts obtained as a function of (V_{in}), and the worst-case (peak) value over the sweep is reported as ($R_{on,\,max}$) to provide a conservative metric for timing analysis. In terms of switch conduction, the worst-case condition corresponds to the SS process corner combined with low supply voltage ($V_{DD} = 0.76$ V) and cold temperature ($T = -40°C$). Across all evaluated conditions, the SLVT option consistently exhibits a lower ($R_{on,\,max}$) than the LVT implementation.

T-Gate $R_{on,\,max}$ - LVT device				
Temperature	**V_{DD}**	**$R_{ON,\,TT}$**	**$R_{ON,\,FF}$**	**$R_{ON,\,SS}$**
-40 ºC	*0.76 V*	76.49 K	14.55 K	570 K
	0.8 V	41.31 K	9.306 K	285.8 K
	0.84 V	23.56 K	2.172 K	145.4 K
25 ºC	*0.76 V*	25.73 K	8.229 K	112.3 K
	0.8 V	17.11 K	6.11 K	68.38 K
	0.84 V	11.85 K	1.021 K	42.69 K
150 ºC	*0.76 V*	8.532 K	4.423 K	19.88 K
	0.8 V	6.934 K	3.714 K	15.36 K
	0.84 V	1.338 K	1.067 K	12.11 K

Table 3-3: Extracted maximum transmission-gate on-resistance ($R_{on,\,max}$) for the LVT implementation across supply voltage, temperature, and process corners.

T-Gate $R_{on,\,max}$ - SLVT device				
Temperature	**V_{DD}**	**$R_{ON,\,TT}$**	**$R_{ON,\,FF}$**	**$R_{ON,\,SS}$**
-40 ºC	*0.76 V*	5.489 K	2.302 K	18.87 K
	0.8 V	4.073 K	1.886 K	11.94 K
	0.84	3.158 K	1.585 K	8.091 K
25 ºC	*0.76 V*	4.142 K	2.076 K	10.13 K
	0.8 V	3.336 K	1.773 K	7.503 K
	0.84	2.732 K	1.541 K	5.759 K
150 ºC	*0.76 V*	2.942 K	1.805 K	5.287 K
	0.8 V	2.538 K	1.63 K	4.497 K
	0.84	2.19 K	1.486 K	3.875 K

Table 3-4: Extracted maximum transmission-gate on-resistance ($R_{on,\,max}$) for the SLVT implementation across supply voltage, temperature, and process corners.

The ($R_{on,\,max}$) values reported in Table 3-3 and Table 3-4 are extracted from the same ($R_{on}(V)$) DC sweep shown in the following figures: for each PVT condition, (V_{in}) is swept from 0 to (V_{DD}), ($R_{on}(V_{in})$) is computed point-by-point, and the peak value over the sweep is recorded as ($R_{on,\,max}$).

Figure 3-21 shows ($R_{on}(V)$) as a function of (V_{in}) for the LVT transmission gate in the TT corner at 25ºC, comparing (V_{DD} = {0.76, 0.8, 0.84} V). A clear peak is observed around mid-supply, where neither device is strongly overdriven; increasing (V_{DD}) improves gate overdrive and reduces the overall resistance, lowering the peak value and improving conduction over the full input range. As (V_{DD}) changes, the location of the resistance peak also shifts slightly along the (V_{in}) axis, remaining close to mid-supply (approximately ($V_{in} \approx V_{DD}/2$). In this testbench the NMOS and PMOS devices in the transmission gate are sized with the same (W) and (L); therefore, the peak occurs near the point where their effective overdrives become comparable—set primarily

by (V_{DD} - V_{in}) for the NMOS conduction contribution and by (V_{in}) for the PMOS contribution—so the minimum combined conductance ($R_{on,\,max}$) scales with the supply voltage.

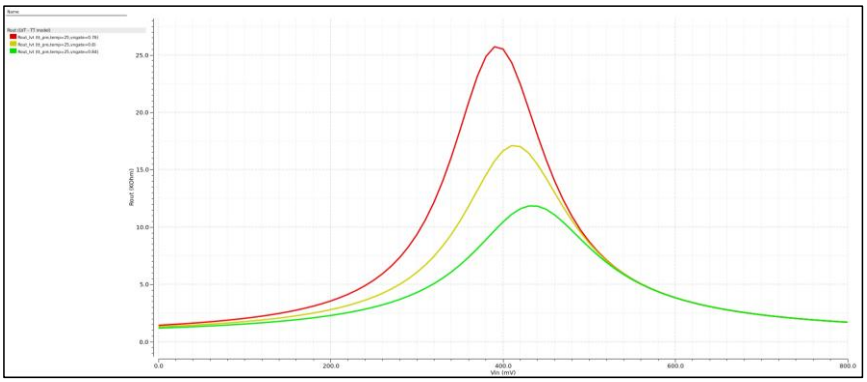


Figure 3-21: R_{on} vs V_{in} for the TT corner at 25 ºC, comparing V_{DD} = 0.76 V, 0.8 V, and 0.84 V.

Figure 3-22 repeats (R_{on}(V)) extraction for the LVT transmission gate in the TT corner at (V_{DD} = 0.8 V) for three different temperatures (T = -40 ºC, 25 ºC, and 150 ºC). The resistance increases at cold temperature due to reduced carrier mobility and weaker effective drive, while higher temperature reduces (R_{on}) even though leakage increases elsewhere in the design. This trend motivates the use of low-temperature conditions as a key contributor to the worst-case delay corner for switch-limited paths.

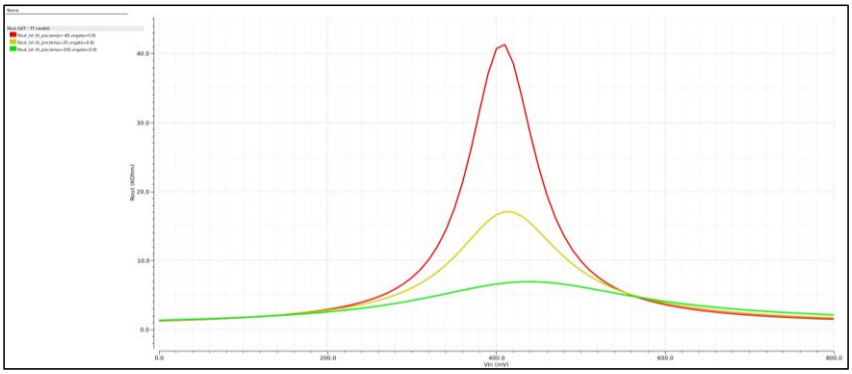


Figure 3-22: R_{on} vs V_{in} at V_{DD} = 0.8 V and TT corner for three temperatures (-40 ºC, 25 ºC, and 150 ºC).

Figure 3-23 compares LVT and SLVT transmission gates under the worst-case conduction conditions (SS process corner, low voltage supply (V_{DD} = 0.76 V), and cold temperature (T = -40 ºC)). As expected, SLVT provides a lower (R_{on}) due to its reduced threshold voltage, which improves overdrive at low supply voltage.

Figure 3-24 then illustrates the impact of transmission-gate width scaling on the extracted on-resistance by sweeping the common device width while keeping the remaining parameters constant. In this sweep the NMOS and PMOS are scaled together (W_n = W_p), and the results are shown for both LVT and SLVT transmission-gate implementations.

The sweep is performed from minimum to maximum width; across the full range, SLVT consistently exhibits a lower (R_{on}) than LVT for the same width, consistent with its reduced threshold voltage and higher effective overdrive (higher conduction strength). As the common

width increases, (R_{on}) decreases due to the higher channel conductance. This sizing study can therefore be used to select a practical switch width that reduces (R_{on}) without excessively increasing area and dynamic power.

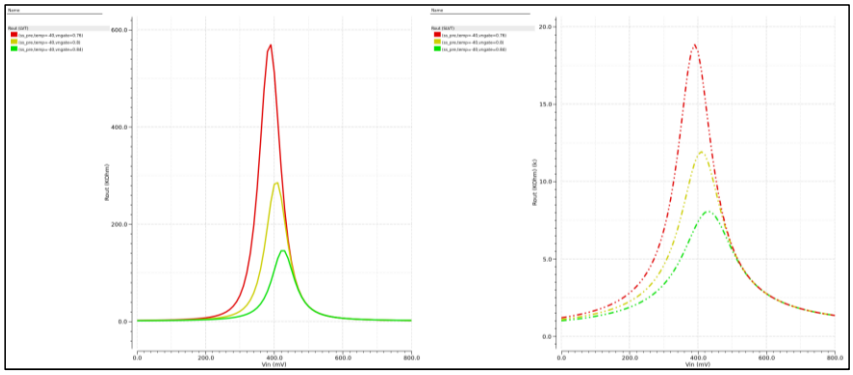


Figure 3-23: Worst-case corner R_{on}(V) comparison between LVT and SLVT transmission gates at SS corner, V_{DD} = 0.76 V, and T = -40 °C.

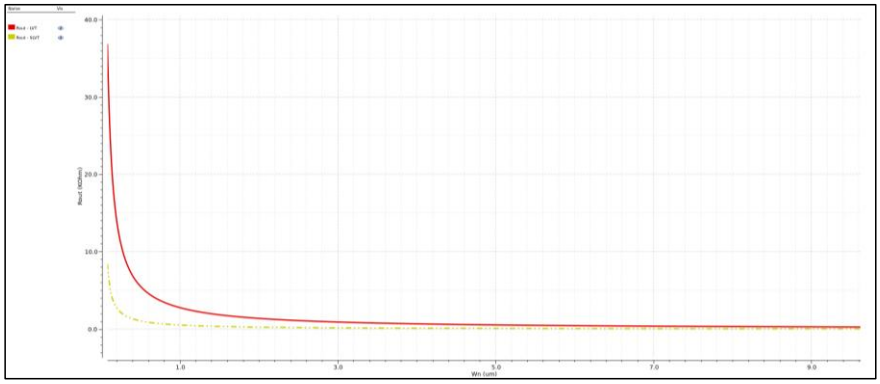


Figure 3-24: Transmission-gate on-resistance versus common switch width ($W_n = W_p$) for LVT and SLVT implementations.

Overall, the transmission-gate characterization confirms that (R_{on}) is strongly dependent on the input operating point and worsens under the SS/low-V_{DD}/cold condition, while SLVT devices consistently reduce (R_{on}) at the cost of the leakage penalties discussed in Chapter 2. These results provide a quantitative basis for selecting switch sizing and device option in the flip-flop implementations. With the switching element characterized, the next subsection focuses on the second key latch primitive, the CMOS inverter, by extracting its transfer characteristic and delay under comparable PVT conditions, since inverter regeneration strength and noise margins ultimately determine the robustness and timing of the complete flip-flop.

Comentado [JC27]: Review all the section, understand how to choose the correct size for the flipflop.

3.4.2 Inverter characterization.

The CMOS inverter is the fundamental regenerative element inside the latch and flip-flop architectures analysed in this work. In contrast to the transmission gate, which primarily determines sampling resistance and RC time constants, the inverter sets logic restoration strength, noise margins, and regeneration speed. Its static transfer characteristic determines robustness against noise and charge loss, while its dynamic response directly influences clock-to-Q delay and overall internal timing closure. For these reasons, the inverter is characterized under the same

PVT conditions as the transmission gate, using consistent sizing and bias definitions, and its behaviour is explicitly linked to the flip-flop results presented in Section 3.4.3.

A reference inverter is first implemented using minimum channel length devices ($L_n = L_p = 0.02$ µm) with an initial width ($W_n = 0.17$ µm). The PMOS width is then selected relative to the NMOS (i.e., ($W_p = r \cdot W_n$)) to achieve a switching point close to mid-supply, targeting ($V_M \approx V_{DD}/2$). This sizing provides a near-symmetric voltage transfer characteristic and balances rising and falling delays, which is desirable for robust latch regeneration and for clock buffering.

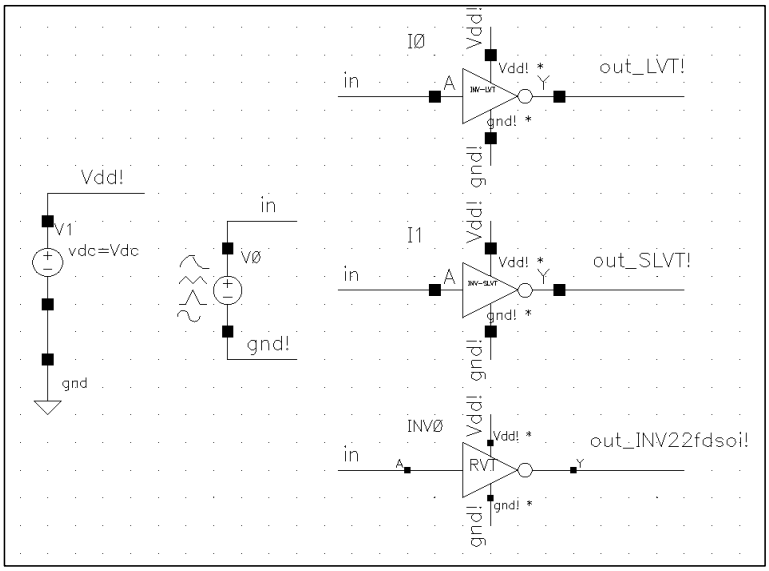


Figure 3-25: Inverter characterization testbench: three inverter variants (LVT, SLVT, and 22FDX PDK reference) with a common input and supply.

Figure 3-25 illustrates the initial testbench used for inverter characterization. Two inverter instances are implemented using LVT and SLVT devices, while a third instance, based on the 22FDX PDK standard cell (INV0), was included to provide a reference and ensure consistency of extracted results. The voltage transfer characteristic, ($V_{out}(V_{in})$), was obtained by sweeping the input from 0 to (V_{DD}), across three supply voltages (V_{DD} = {0.76, 0.8, 0.84} V). For each configuration the switching point (VM) was extracted and used to validate and optimize the (Wp/Wn) ration selection.

, the inverter switching point (VM) is evaluated when (Vin = Vdd/2) and is used to validate the chosen (Wp/Wn) ratio. Same sweep is repeated for the three supply voltages used throughout this chapter (V_{DD} = {0.76, 0.8, 0.84} V).

A first sweep with (r = {1, 1.2, 1.4, 1.6, 1.8, 2}) showing the best results for (r = 1.6) so a second sweep is performed with closer values (r = {1.5, 1.55, 1.6, 1.65, 1.7}). Table 3-5 shows the results obtained for all the ratio values tested, although values as (r=1.4) show really good results for (VDD = 0.84) with an error of 9.043mV the overall performance for all the (VDD) evaluated is worst; being the best result for all the VDD options obtained for (r=1.6), minimizes the worst-case deviation (\max_{V_{DD}}|V_M-V_{DD}/2|) across (V_{DD}={0.76,0.8,0.84}) V.". Finally, Figure 3-26 shows the output obtained for the ratio (r = 1.6) evaluated for each VDD option. [Note for all this values only LVT values are reported]

	E(r) max for LVT devices
	r values for (Wp = Wn*r)

V_{DD}	1	1.2	*1.4*	1.5	1.55	1.6	1.65	1.7	1.8	2
0.76	140.4 mV	105.3 mV	74.76 mV	59.62 mV	52.26 mV	44.62 mV	36.76 mV	29.44 mV	14.93 mV	13.17mV
0.8	186.8 mV	106.4 mV	38.87 mV	8.922 mV	5.245 mV	19.66 mV	34.16 mV	46.95 mV	71.29 mV	115.5 mV
0.84	83.37 mV	32.38 mV	9.043 mV	26.97 mV	35.38 mV	44.07 mV	52.91 mV	60.48 mV	74.93 mV	101.7 mV

Table 3-5: xx

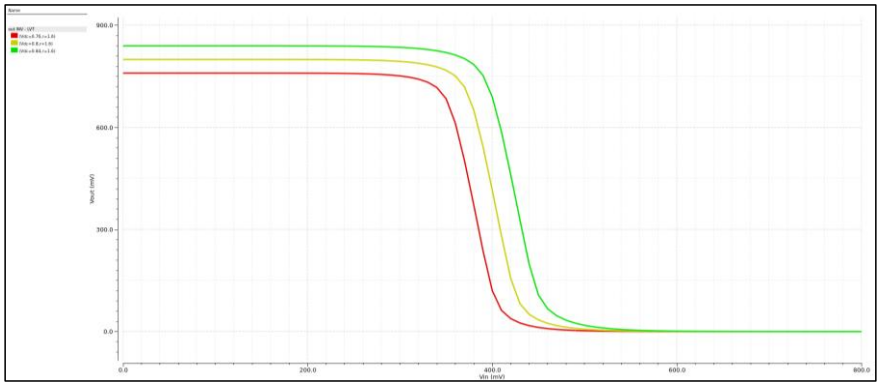


Figure 3-26: Vout(Vin) characteristic for (VDD = {0.76, 0.8, 0.84} V, and r = 1.6).

After selecting the inverter sizing ratio, the remaining characterization focuses on dynamic behaviour. Using this nominal sizing, transient simulations are then performed to (i) extract propagation delay as a function of load capacitance, representative of internal latch nodes, and (ii) evaluate waveform integrity under high-frequency excitation, representative of clock buffering (CLK/CLKB generation), where insufficient drive can lead to reduced output swing and distorted edges at multi-GHz operation.

A three-stage inverter chain is used to characterize clock buffering under capacitive loading. The first inverter is driven by an ideal clock source (V1), while the third inverter drives a purely capacitive load (C_L) that models the total gate capacitance of the transmission gates connected to the clock net. Using a short chain avoids measuring an unrealistically ideal source-driven transition and provides inverter-driven edges representative of actual clock distribution within the sequential blocks. Propagation delays (t_{pHL}) and (t_{pLH}) are extracted using the 50%–50% convention, and output rise/fall times are measured using the 10–90% definition.

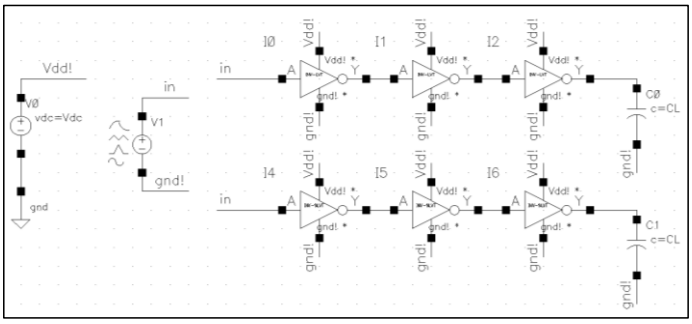


Figure 3-27: Testbench chain of inverters for LVT and SLVT configurations.

Inverter delay is measured using a representative capacitive load to emulate the loading conditions encountered inside latches and flip-flops. This approach avoids optimistic unloaded delays and ensures that the extracted timing values are representative of realistic sequential operation.

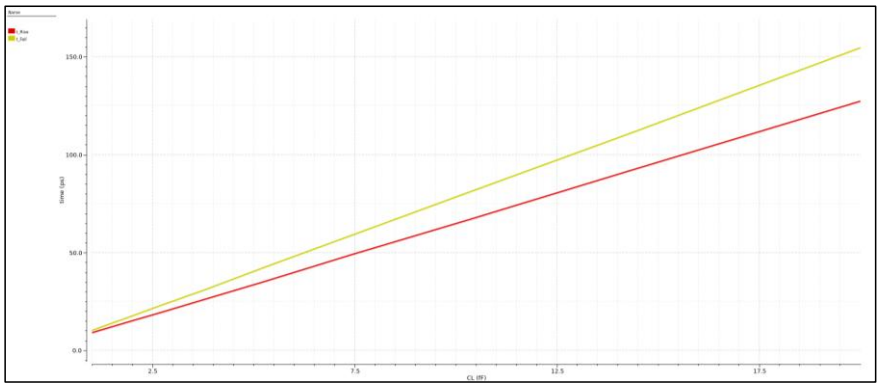
To ensure that the extracted propagation delay and transition times reflect only the capacitive load dependence (and are not limited by incomplete settling at higher frequencies), the delay-versus-(C_L) characterization uses an input period of (T = 625 ps) (corresponding to 1.6 GHz). This choice guarantees that, across the full evaluated load range (1–20 fF), the slowest output transitions—measured at (C_L = 20 fF)—complete well within each half-clock cycle. For instance, the maximum measured output fall time is approximately 155 ps, giving a margin of over 2× relative to the half-period (T/2 = 312.5 ps). This ensures each edge reaches its full logic level before the next switching event, so the reported delays and slopes are not impacted by frequency-limited behaviour.

	CL									
$t_{p\ avg}$	**1**	**1.39**	***1.94***	**2.71**	**3.78**	**5.28**	**7.36**	**10.28**	**14.34**	**20**
INV1 to INV2	5.60	5.62	5.63	5.64	5.65	5.66	5.66	5.67	5.67	5.68
INV2 to INV3	8.26	9.75	11.77	14.54	18.39	23.73	31.18	41.49	56.01	75.97

$$t_{pHL} = t(V_1 \uparrow 50\%) \rightarrow t(V_2 \downarrow 50\%)$$

$$t_{pLH} = t(V_1 \downarrow 50\%) \rightarrow t(V_2 \uparrow 50\%)$$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$



As expected, increasing (C_L) increases delay approximately proportionally, while increasing device widths reduces delay at the expense of higher input capacitance and dynamic power in the driving stage.

These results establish the intrinsic delay and slew scaling of the inverter for a wide range of transmission-gate loading. The ability of the inverter to maintain sufficient output swing and

correct timing at multi-GHz clock rates, representative of practical flip-flop operation, is evaluated in the subsequent frequency-domain characterization.

Although SLVT inverters provide lower intrinsic delay due to higher drive current, the associated increase in leakage and gate capacitance makes them less attractive for widespread use inside flip-flop structures. Since inverters in latches are permanently connected to the supply rails and continuously contribute to static power, excessive leakage can dominate standby consumption. For this reason, unless the inverter lies on a critical timing boundary, LVT devices provide a more balanced trade-off between speed, robustness, and power. This consideration motivates the device choices used in the flip-flop implementations analysed in Section 3.4.3.

Frequency-domain robustness (inverter chain). Finally, to identify the operating-frequency limit at which the inverter can no longer restore full logic swing, a short chain of three inverters is simulated while sweeping input frequency. A pass/fail criterion is defined using output levels and timing: correct inversion is considered valid when the output maintains acceptable logic levels, quantified using 10–90% output swing (or equivalently ensuring (V_{OH}) and (V_{OL}) remain sufficiently close to (V_{DD}) and 0 V). This test is particularly relevant for CLK/CLKB generation: at very high frequency the inverter delay and finite drive strength can prevent the output from reaching the rails within half a period, producing reduced swing and waveform distortion that can degrade transmission-gate control and sequential timing.

The inverter results obtained in this subsection are used in the following sections to (i) select a practical (W_p/W_n) ratio for robust regeneration, (ii) determine realistic internal-node delay and energy trends versus load, and (iii) justify the maximum clock frequency used in the flip-flop verification campaign.

- **Next section: Frequency capability / waveform integrity (3–7 GHz and beyond)** There you fix a representative (C_L) (e.g., based on expected TG fanout) and sweep frequency, showing when VOH/VOL and slew degrade.

Inverter, variation of the load capacitance leads to a change in the delay and dynamic power, and the technology scaling results in an increase of delay; however, with a decrease in the dynamic power values [18].

Fmin of all the circuits is going to be limited by the inverter.

Increase W or number of fingers at p device

Look clkb and clk signals, sometimes the inverter can't lead with the speed of the original clock so the signal doesn't reach the max and min voltage levels, also the shape of the signal can look different.

Also we can change from lvt to slvt, BUT, when we perform T tests, the current leakage for the slvt is bigger so the device is going to have a increase in power consumption.

Point to f = 10GHz

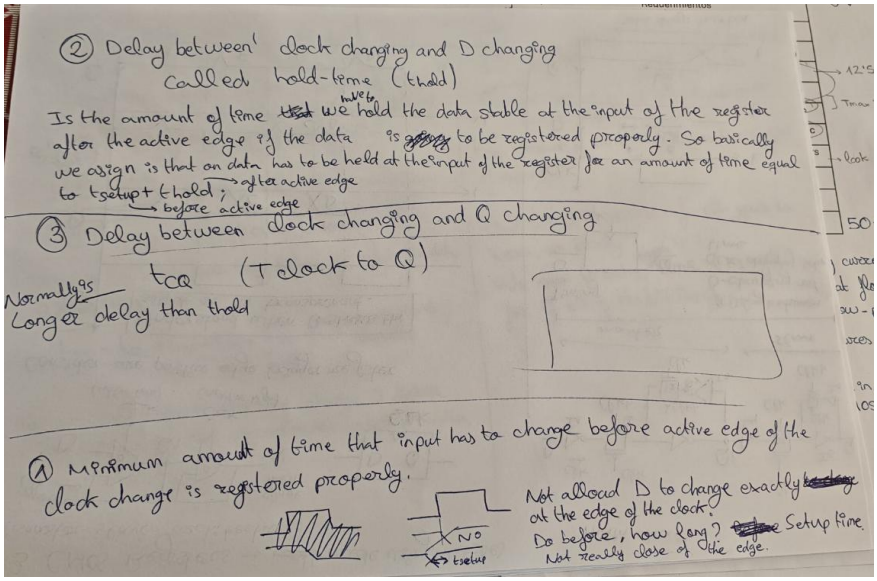
New schematic with a chain of three inverters (our design) and the INV of the technology. The point is to perform a frequency sweep and look for the point where the output doesn't invert the input correctly.

The inverter characterization results confirm that inverter sizing and device-option selection strongly influence both static robustness and dynamic timing. A near-mid-supply switching point provides balanced noise margins and regeneration strength, while delay scales with both drive capability and output loading. Although SLVT devices reduce intrinsic delay, their higher leakage and capacitive loading make LVT inverters a more appropriate default choice for latch feedback and state-holding paths in this work. These observations directly inform the flip-flop implementations evaluated in the next section, where clock-to-Q delay, setup time, and power are analysed at the architectural level.

3.4.3 Flip-flops characterization.

Characterization includes delay, leakage, , and noise margins. Corners (SS,TT,FF) and temperatures (-40ºC to 125ºC) are evaluated.

Dynamic: Conventional and advanced. And static using caps.



3.4.3.1 Power down current and current consumption.

Static and dynamic current consumption are evaluated, including sleep-mode leakage measurements.

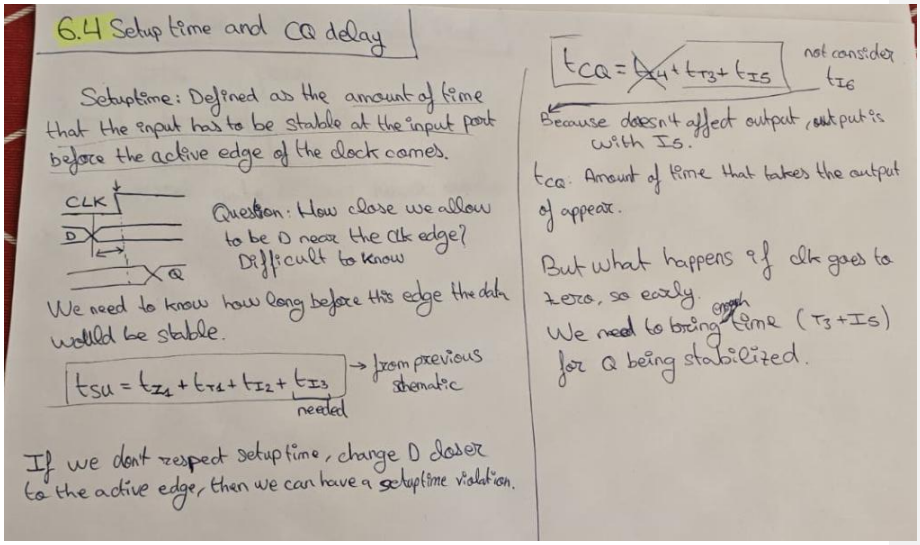
3.4.3.2 Jitter noise

Clock-to-Q delay defines the response time of a flip-flop to a clock edge, while jitter introduces uncertainty in timing.

3.4.3.3 Clock2Q - SetupTime and hold time.

"Clock to q" se refiere a la retraso de propagación (delay) entre un flanco de reloj y el cambio en la salida (Q) de un biestable (flip-flop). Este tiempo es crucial para analizar la velocidad máxima de operación de circuitos digitales y para garantizar que los datos se propaguen correctamente a través de cascadas de biestables.

Defined as the amount of time that the input hast to be stable at the input port before the active edge of the clock comes, in other words determines how early data must be stable before the clock edge to ensure proper capture.



3.4.3.4 MTBF

Look source: Impulse Sensitivity Function Analysis of Periodic Circuits.

Mean Time Between Failure quantifies metastability robustness. Higher clock frequencies and small setup margins degrade MTBF.

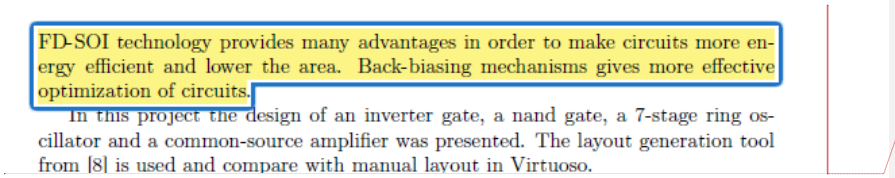
3.4.3.5 Corners and nominal. PVT. Understand how temperature can affect the performance of the devices.

Impact of process, supply voltage, and temperature variations are analysed. Higher temperatures increase leakage and delay.

Chapter 4. Conclusions.

This report outlines the fundamentals of IDAC architecture, device behavior at the 22nm node, flip-flop design concepts, and key testing methodologies. The performance and reliability of high-speed mixed-signal circuits depend strongly on device selection, layout strategy, and thorough PVT testing.

First point of the DAC design accomplished, next steps assembly the full architecture. [J]


FD-SOI technology provides many advantages in order to make circuits more energy efficient and lower the area. Back-biasing mechanisms gives more effective optimization of circuits.

In this project the design of an inverter gate, a nand gate, a 7-stage ring oscillator and a common-source amplifier was presented. The layout generation tool from [8] is used and compare with manual layout in Virtuoso.

Comentado [JC28]: TFM 22nm FDSOI

As summary, and based on the extracted DC figures of merit in this chapter, ID, gm, or gds values are consistent with the general trends highlighted in the GlobalFoundries 22FDX analog workshop. In that context, 22FDX FD-SOI is commonly reported to offer several advantages for analog design as:

- It can provide drive current and gm/ID efficiency comparable to high performance 28 nm bulk nodes.
- A reduction in gds (often reported up to ~1.8×) can improve output resistance.
- Transition frequency (fT) is reported to be competitive with the best 28 nm bulk results.
- Higher intrinsic voltage gain (gm/gds) is frequently observed, in some cases exceeding 2× depending on device option and biasing.
- The planar FD SOI structure is associated with relatively low source/drain and gate resistances (RSD and RG), which can be beneficial for high speed and low noise analog blocks.

4.1 Further work.

Body biasing capabilities in FDSOI opens a variety of opportunities such as achieving lower threshold voltages for the devices and lower power, and it can also be used for compensating process variations in a cell. [TFM 22nm FDSOI]

Adding new functions (LSI designs requires FFs having additional functions like scan, reset, and set. The performance and cell area for these cells are also important [21])

Explore new latch architectures ECL, etc.

Start with Layout, build the full architecture. Explore body biasing options from the technology.

Explore calibration techniques [3,4,11] calibration techniques allows us to reduce the parasitic capacitance significantly, enabling the DAC to achieve superior dynamic linearity at high frequency. So we don't need to increase area thanks to calibration.

Talk about power, needs to be limited to allow practical thermal management?

Large-area current source arrays are widely used in current-steering digital-to-analog converters(DACs) to statically maintain a required level of matching accuracy between the current sources. This not only results in large die size but also in significant degradation of dynamic range for high-frequency signals. For this, calibration techniques can be presented which

effectively compensates for current source mismatch and achieves high linearity with small die size and low power consumption [10].

Cascode is widely used to enhance the output impedance of current sources and improve dynamic linearity, nut low supply voltages make it impractical to use cascaded current sources. In these calibration techniques become even more attractive [10]

These techniques consume less power and do not introduce noise or spurs during normal operation [12].

Some works use body biasing for the NMOS transistors in the Latch to make the design more robust [BachThesis].

Back-gate control, allows for a Vt reduction, enables smaller switches due lower Ron/W and Ron·C. Smaller Ron/W stands for smallers switches, smaller layout, reduced parasitic and even smaller switches. These advantages can be utilized to realize architectures that would be inefficient or unrealistic in bulk.

22FDX, uses back-gate biasing to control current mirror VTH directly, being excellent for multi-channel ADC drivers, analog SoC front ends, and precision references.

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