

Introduction to analog design with open source tools

Using the SkyWater PDK and Efabless platform



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SVP Analog & Platform



efabless
efabless.com



Open Circuit Design
opencircuitdesign.com



Google Cloud
google.com



SkyWater sky130 open PDK
skywatertechnology.com

The SkyWater Open PDK

Public repository



Documentation

<https://skywater-pdk--136.org.readthedocs.build>

Efabless design repositories

<https://github.com/efabless/caravel>

https://github.com/efabless/caravel_user_project_analog

Community



slack

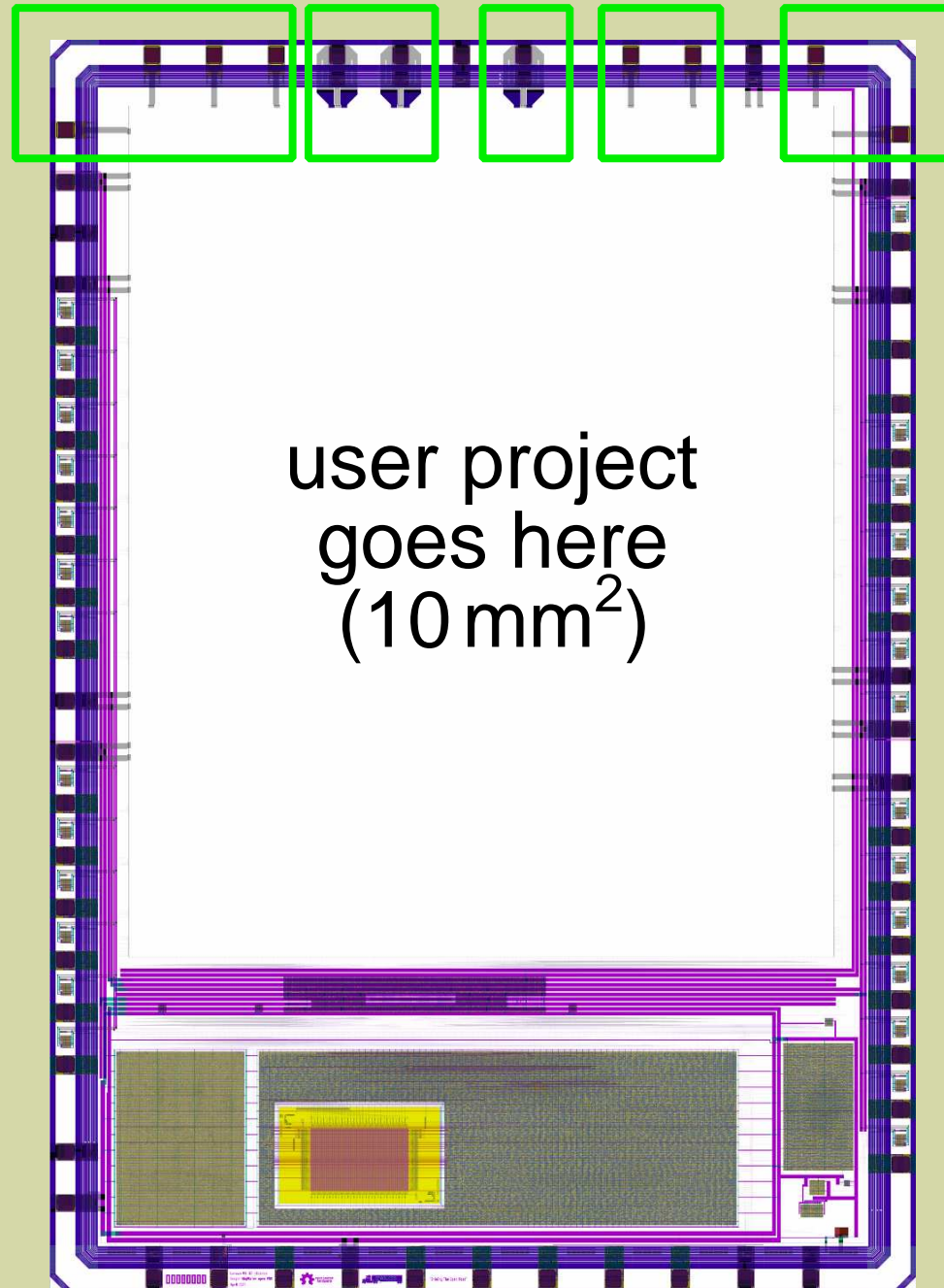
<https://join.skywater.tools>

#analog-design

#xschem

#magic

“Caravan” analog project harness



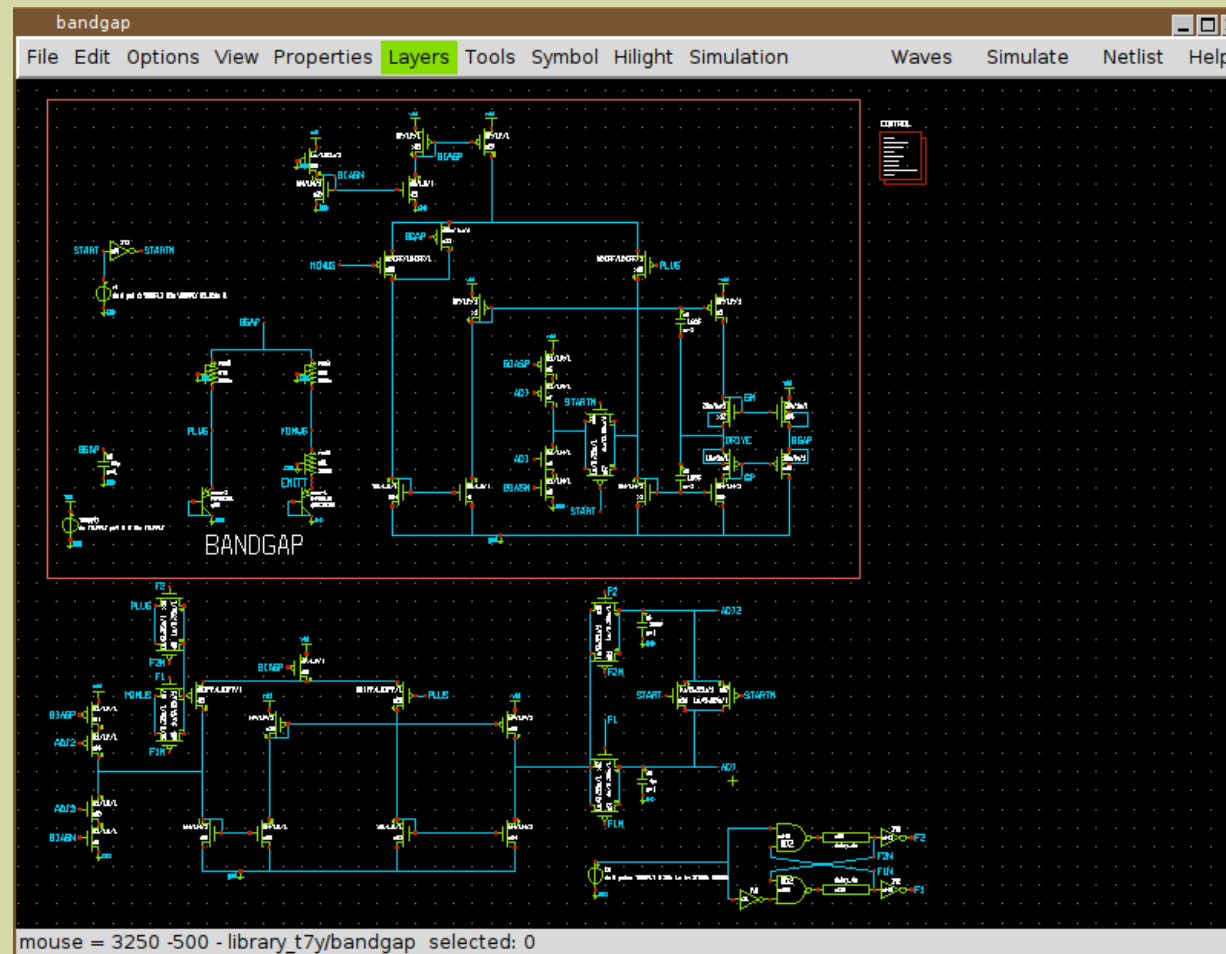
- ← These pads on the top have been repurposed for analog (11 pads)
- ← GPIO for the rest (27 pads)
 - analog signals can be connected to the GPIO pads (except lower 7)
 - additional 3.3V digital GPIO inputs available to the user area.
 - No digital power rings; project connects directly to wrapper pins
- ← Same RISC-V management SoC and support circuitry as Caravel

Open-Source EDA Tools

Tools Currently Supported by the open PDK

Xschem

<https://github.com/StefanSchippers/xschem>




Open-Source EDA Tools

Tools Currently Supported by the open PDK

Ngspice

<https://ngspice.sourceforge.net>



**MIXED MODE - MIXED LEVEL
CIRCUIT SIMULATOR**
BASED ON BERKELEY'S SPICE3F5

NGSPICE SUMMARY

[Home](#) | [News](#) | [Screenshots](#) | [Download](#) | [Documentation](#) | [Extras/Options](#) | [Applications](#) | [Development](#) | [Simulation Environments](#) | [Recipes](#)

Ngspice Home

[Home](#)
[What is ngspice ?](#)
[Features, Extras & Options](#)
[FAQ](#)
[Tutorials](#)
[Sourceforge Developer Pages](#)

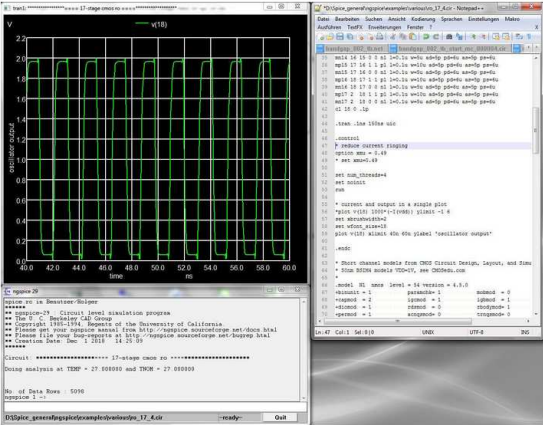
ngspice - open source spice simulator

ngspice is the open source spice simulator for electric and electronic circuits.

Such a circuit may comprise of JFETs, bipolar and MOS transistors, passive elements like R, L, or C, diodes, transmission lines and other devices, all interconnected in a netlist. Digital circuits are simulated as well, event driven and fast, from single gates to complex circuits. And you may enter the combination of both analog and digital as a mixed-signal circuit.

ngspice offers a wealth of device models for active, passive, analog, and digital elements. Model parameters are provided by the semiconductor manufacturers. The user add her circuits as a netlist, and the output is one or more graphs of currents, voltages and other electrical quantities or is saved in a data file.

ngspice does not provide schematic entry. Its input is command line or file based. There are however [third party](#) interfaces available.



The screenshot shows the ngspice simulation interface. The main window displays a plot of voltage V(t) over time, showing a square wave oscillating between approximately 1.8V and 0.2V. The x-axis represents time in milliseconds (ms) from 40.0 to 60.0. The y-axis represents voltage in Volts (V) from 0.0 to 2.0. Below the plot, there is a command window showing the simulation setup and results. The command window displays the netlist, simulation parameters, and the output of the simulation, including the time step and the number of data points.

ngspice is SPICE compatible. You may apply PSPICE or LTSPICE device model parameters and netlists for simulating discrete circuits. ngspice will also read HSPICE device libraries from semiconductor foundry PDKs for simulating integrated circuits.

ngspice builds on many operating systems. The source code and binaries for MS Windows and macOS are available for download on our [sourceforge download page](#). All popular Linux distributions, [Cygwin](#) or [FreeBSD](#) offer ngspice as well. The [FAQ](#), and [documentation](#) pages provide a lot of information, a detailed [manual](#) is available. [Mailing lists](#), [discussion forums](#) and a [bug tracker](#) are offered.

If you are new to Spice and ngspice, don't hesitate to give it a try, if you are a professional user, you will benefit from its robustness and flexibility.

 SOURCEFORGE

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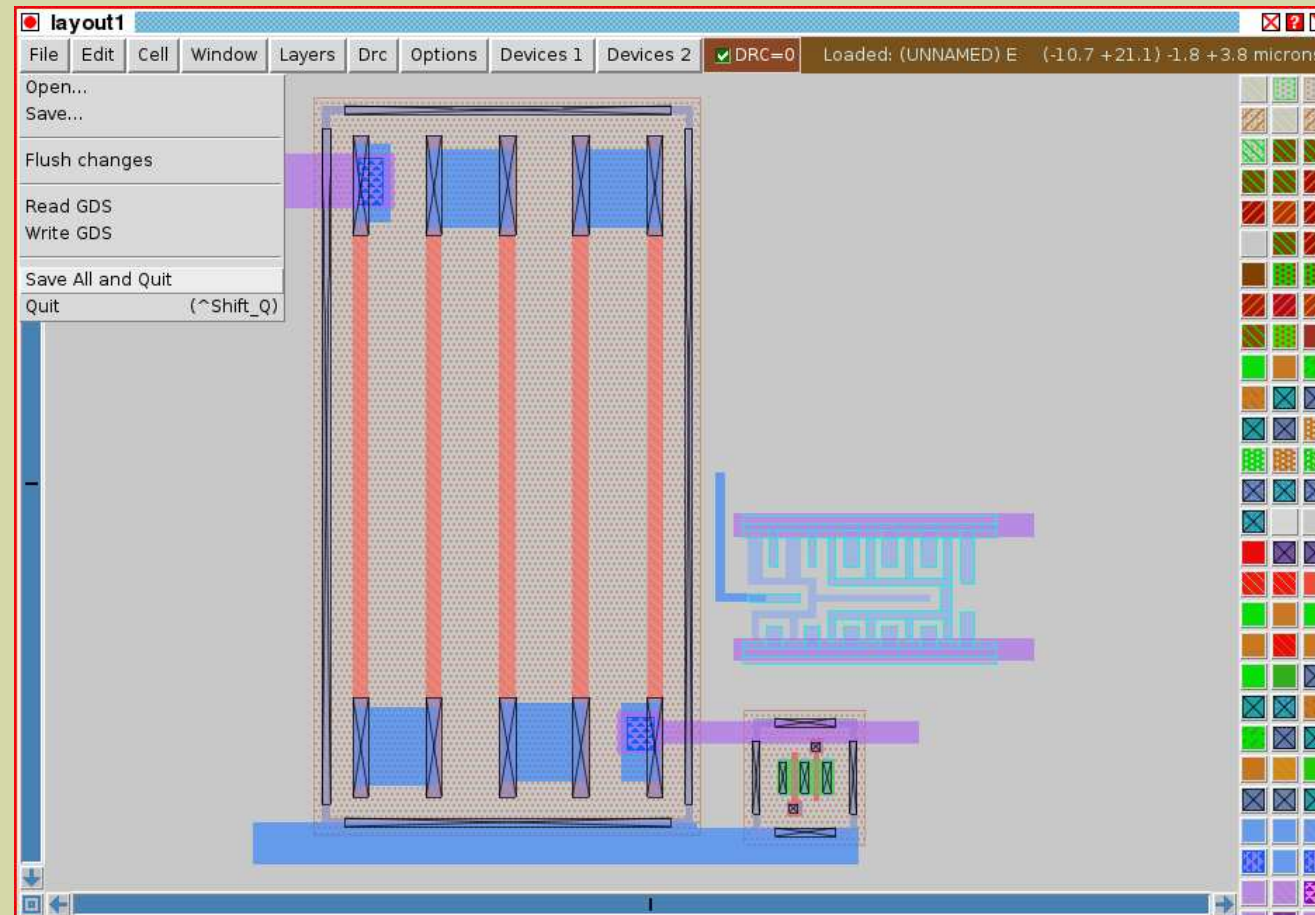


Open-Source EDA Tools

Tools Currently Supported by the open PDK

Magic

<http://opencircuitdesign.com/magic>

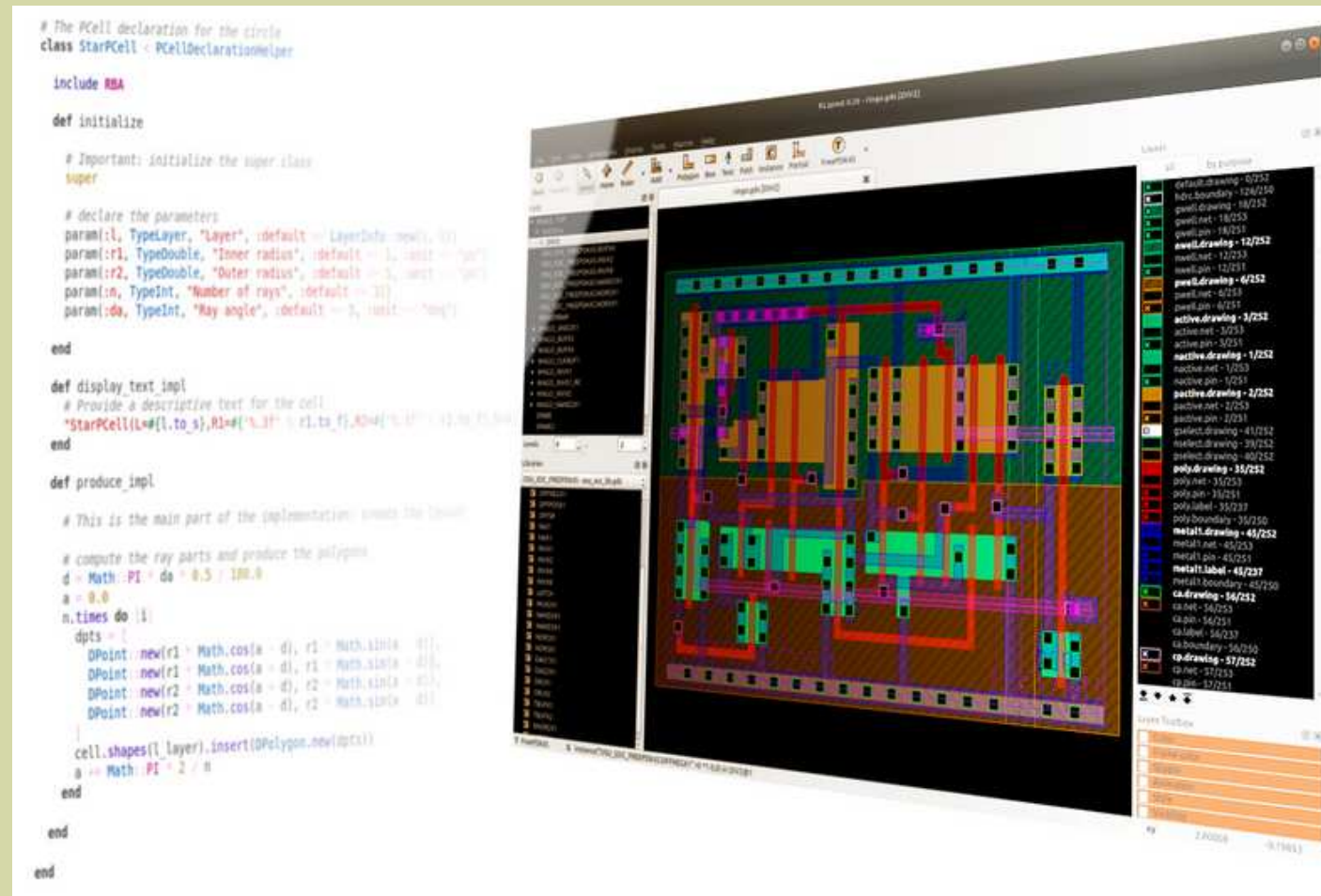


Open-Source EDA Tools

Tools Currently Supported by the open PDK

Klayout

<https://www.klayout.de>

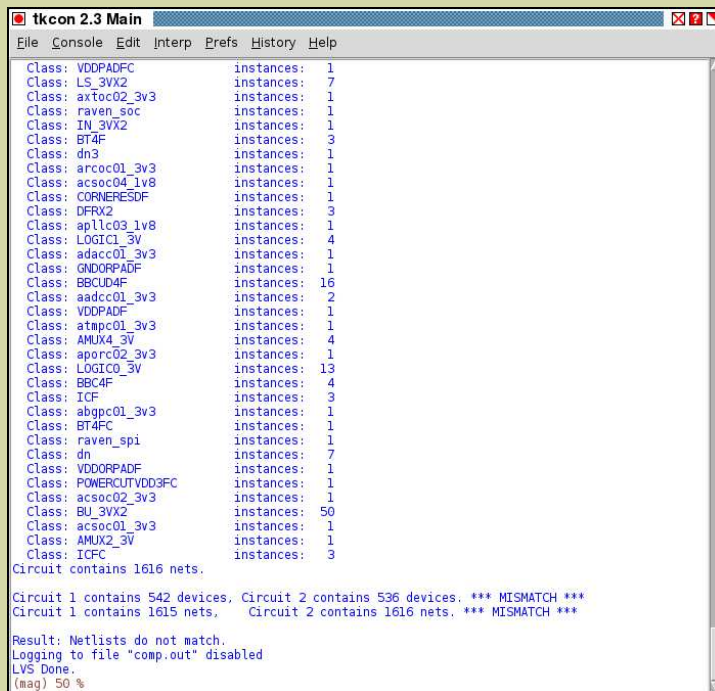


Open-Source EDA Tools

Tools Currently Supported by the open PDK

Netgen

<http://opencircuitdesign.com/netgen>



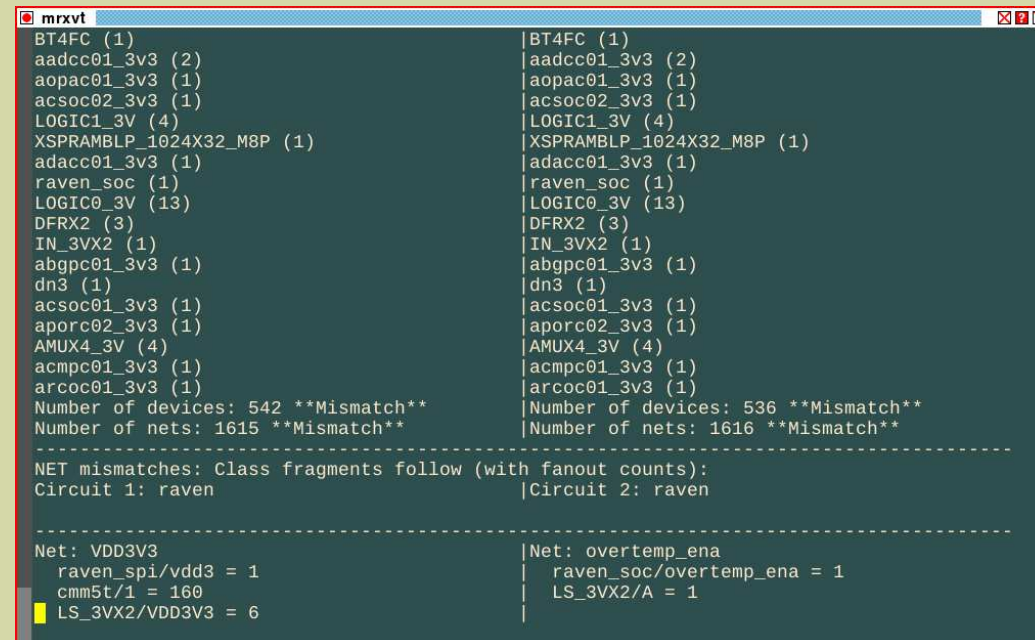
```
tkcon 2.3 Main
File Console Edit Interp Prefs History Help

Class: VDDPADCFC instances: 1
Class: LS_3VX2 instances: 7
Class: axToc02_3v3 instances: 1
Class: raven_soc instances: 1
Class: IN_3VX2 instances: 1
Class: BT4F instances: 3
Class: dn3 instances: 1
Class: arcoc01_3v3 instances: 1
Class: acsoc04_1v8 instances: 1
Class: CORNERESDF instances: 1
Class: DFRX2 instances: 3
Class: ap11c03_1v8 instances: 1
Class: LOGIC1_3V instances: 4
Class: adacc01_3v3 instances: 1
Class: GNDORPADF instances: 1
Class: BBCUD4F instances: 16
Class: aadcc01_3v3 instances: 2
Class: VDDPADCFC instances: 1
Class: atmpc01_3v3 instances: 1
Class: AMUX4_3V instances: 4
Class: aporc02_3v3 instances: 1
Class: LOGIC0_3V instances: 13
Class: BBC4F instances: 4
Class: ICF instances: 3
Class: abgpc01_3v3 instances: 1
Class: BT4FC instances: 1
Class: raven_spi instances: 1
Class: dn instances: 7
Class: VDDORPADF instances: 1
Class: POWERCLUTVDD3FC instances: 1
Class: acsoc02_3v3 instances: 1
Class: BU_3VX2 instances: 50
Class: acsoc01_3v3 instances: 1
Class: AMUX2_3V instances: 1
Class: ICF instances: 3

Circuit contains 1616 nets.

Circuit 1 contains 542 devices, Circuit 2 contains 536 devices, *** MISMATCH ***
Circuit 1 contains 1615 nets, Circuit 2 contains 1616 nets, *** MISMATCH ***

Result: Netlists do not match.
Logging to file "comp.out" disabled
LVS Done.
(mag) 50 %
```



```
mrxvt

BT4FC (1) | BT4FC (1)
aadcc01_3v3 (2) | aadcc01_3v3 (2)
aopac01_3v3 (1) | aopac01_3v3 (1)
acsoc02_3v3 (1) | acsoc02_3v3 (1)
LOGIC1_3V (4) | LOGIC1_3V (4)
XSPRAMBLP_1024X32_M8P (1) | XSPRAMBLP_1024X32_M8P (1)
adacc01_3v3 (1) | adacc01_3v3 (1)
raven_soc (1) | raven_soc (1)
LOGIC0_3V (13) | LOGIC0_3V (13)
DFRX2 (3) | DFRX2 (3)
IN_3VX2 (1) | IN_3VX2 (1)
abgpc01_3v3 (1) | abgpc01_3v3 (1)
dn3 (1) | dn3 (1)
acsoc01_3v3 (1) | acsoc01_3v3 (1)
aporc02_3v3 (1) | aporc02_3v3 (1)
AMUX4_3V (4) | AMUX4_3V (4)
acmpc01_3v3 (1) | acmpc01_3v3 (1)
arcoc01_3v3 (1) | arcoc01_3v3 (1)
Number of devices: 542 **Mismatch** | Number of devices: 536 **Mismatch**
Number of nets: 1615 **Mismatch** | Number of nets: 1616 **Mismatch**

-----
NET mismatches: Class fragments follow (with fanout counts):
Circuit 1: raven | Circuit 2: raven

-----
Net: VDD3V3 | Net: overtemp_ena
  raven_spi/vdd3 = 1 | raven_soc/overtemp_ena = 1
  cmm5t/1 = 160 | LS_3VX2/A = 1
  LS_3VX2/VDD3V3 = 6 |
```


Open-Source EDA Tools

SkyWater SKY130 Libraries

1. Digital standard cells

sky130_fd_sc_hd sky130_fd_sc_hdll
sky130_fd_sc_hs sky130_fd_sc_ms sky130_fd_sc_ls
sky130_fd_sc_lp sky130_fd_sc_hvl

2. Primitive devices / analog

sky130_fd_pr

3. I/O cells

sky130_fd_io

4. 3rd-party libraries

sky130_ml_xx_hd
sky130_sram_macros

Understanding the SkyWater PDK

Libraries

primitive devices and models

sky130_fd_pr • primitives

foundry •

MOSFET transistors (1.8V and 3.3–5.0V)

Bipolar transistors

Resistors

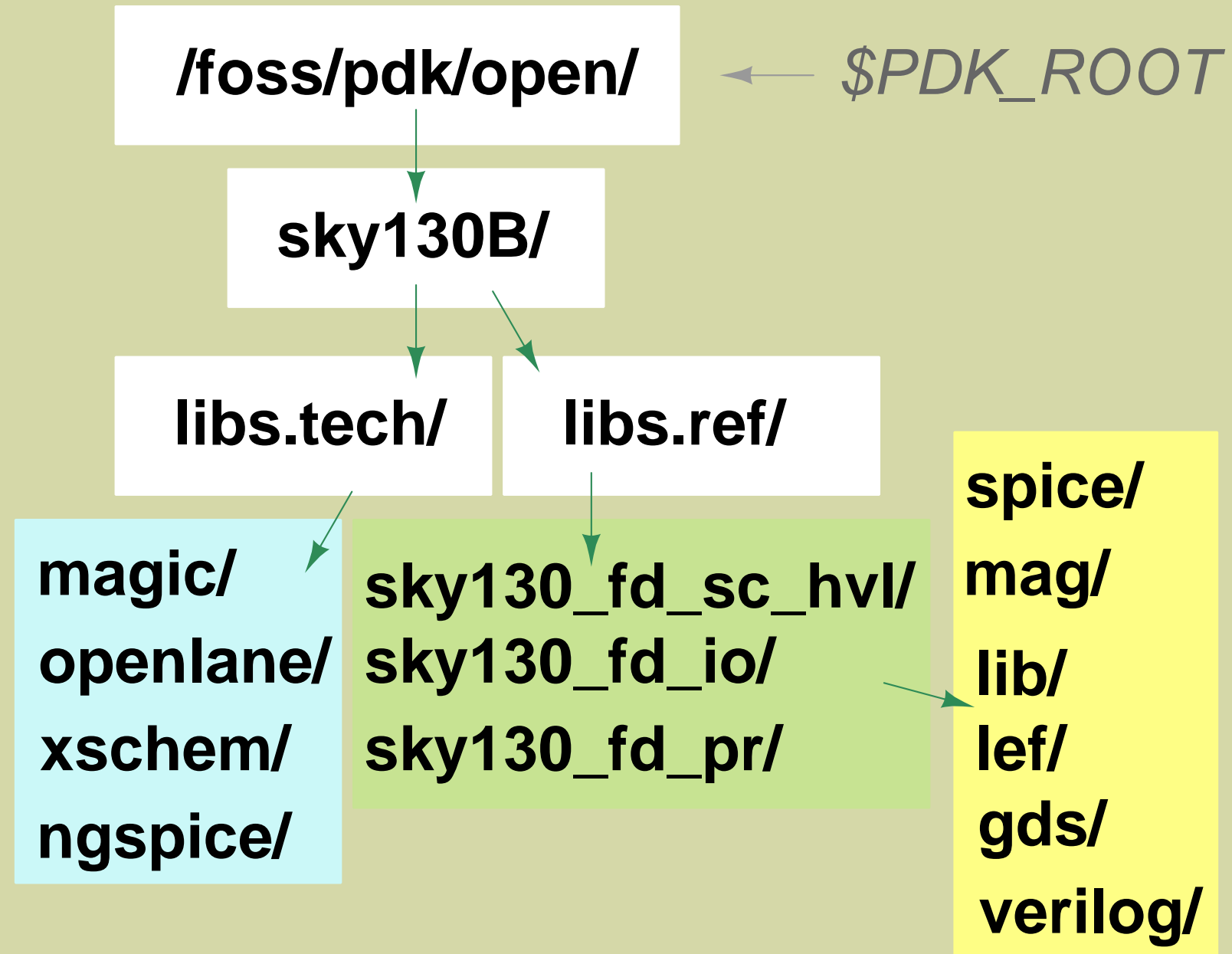
Capacitors

Diodes

Varactors

Open-Source EDA Tools

SkyWater SKY130 Installed Filesystem Structure



Open-Source EDA Tools

Open PDKs Project Filesystem Structure

caravel_user_project_analog/

← cloned git repository

macros/

macro_name/

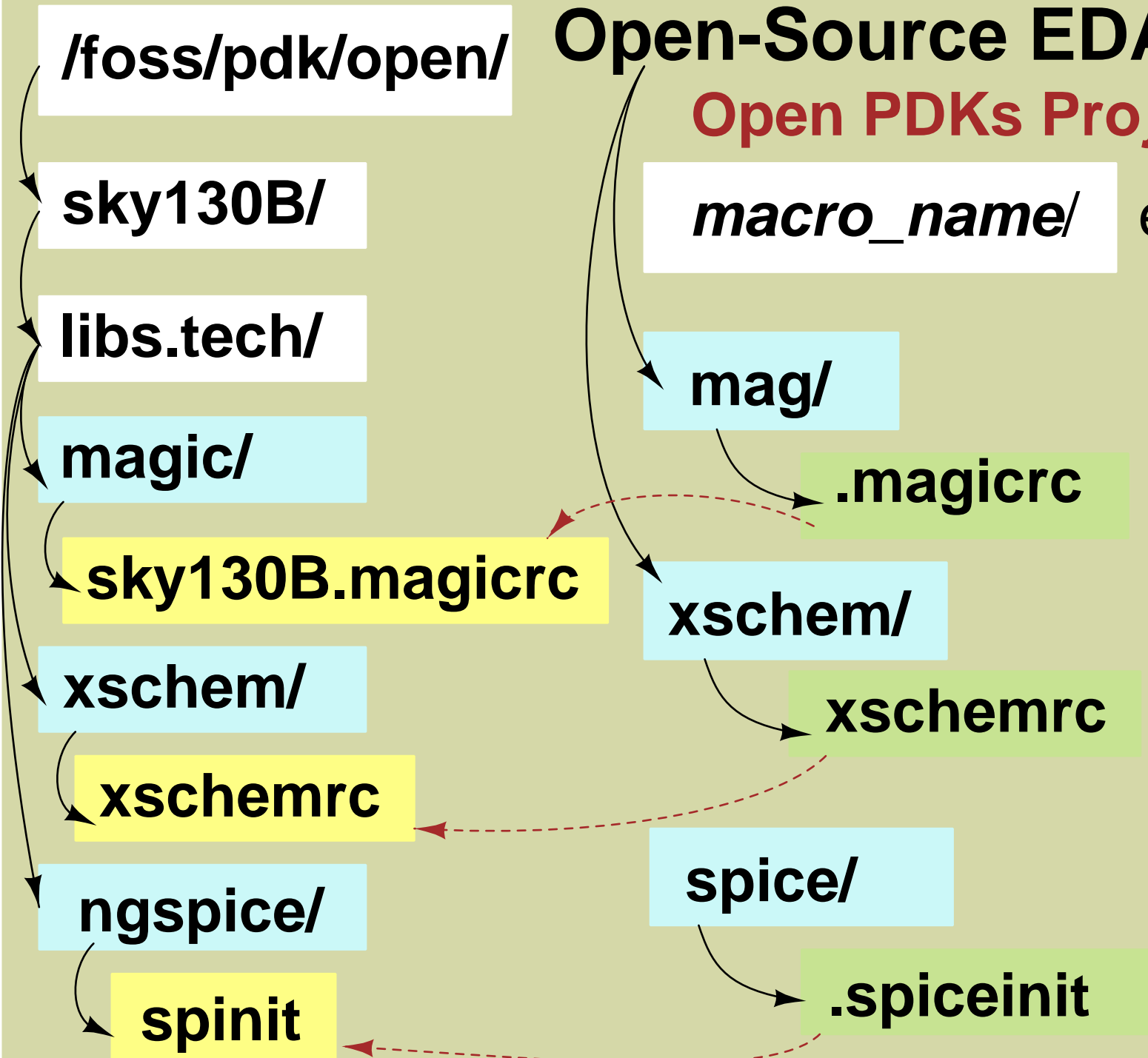
e.g., "sample_and_hold"

**xschem/
spice/
mag/
openlane/
verilog/**

Open-Source EDA Tools

Open PDKs Project Filesystem Structure

macro_name/ e.g., "sample_and_hold"

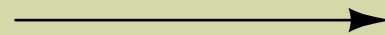


Open Source Tools and Flows

A simple manual design flow

Schematic

xschem

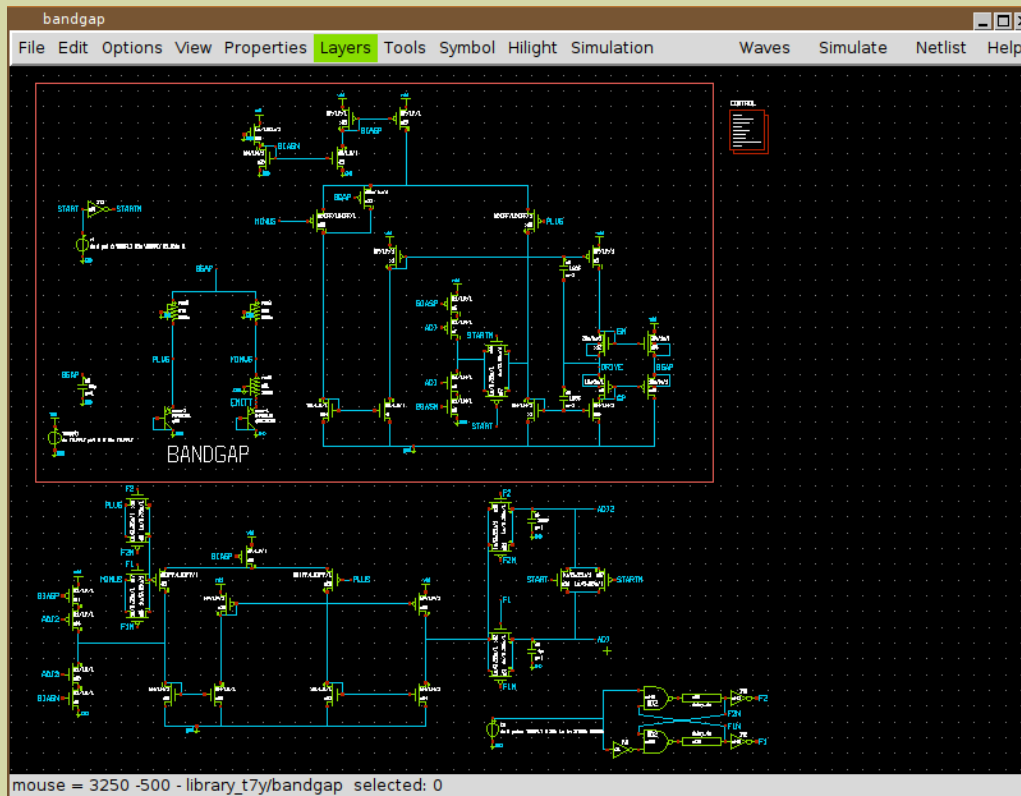


netlist
(SPICE format)

ngspice (analog simulation,
waveform viewing)

magic (layout)

netgen (LVS)

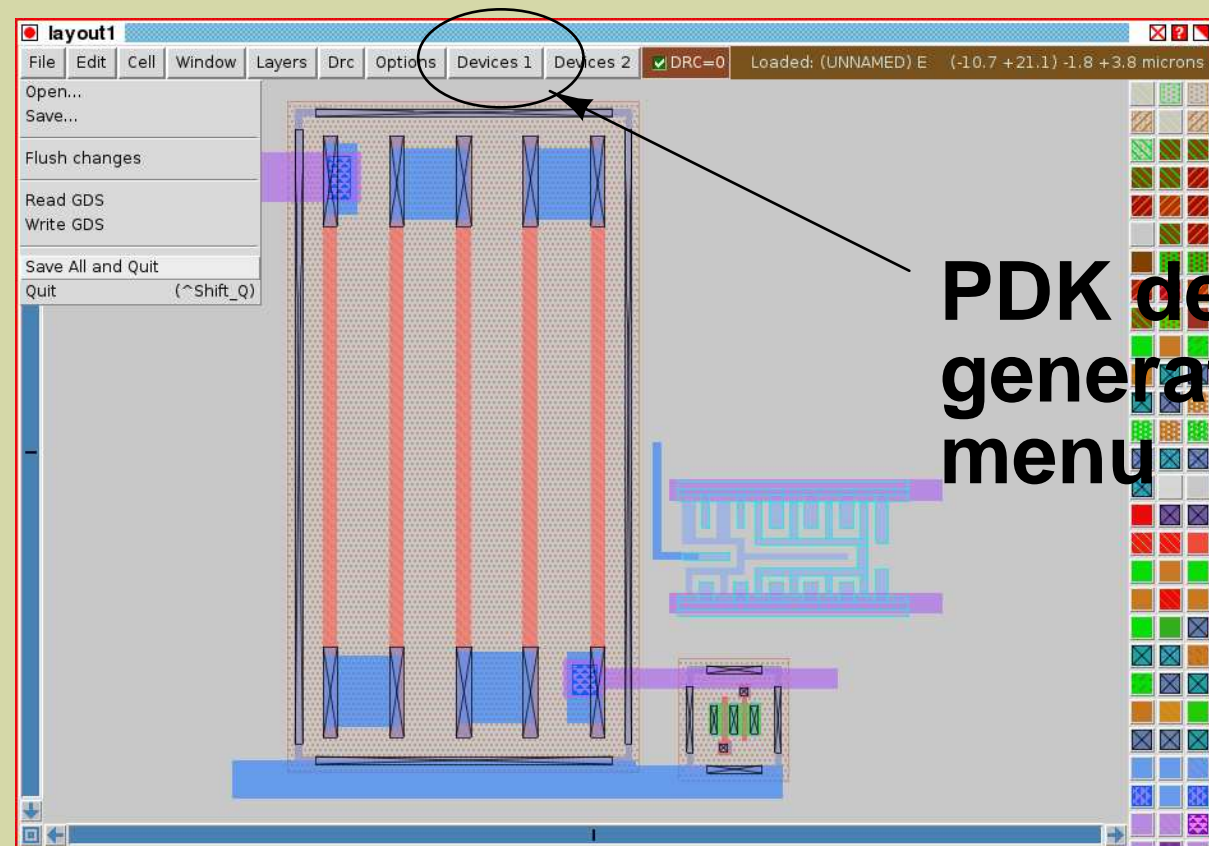


Open Source Tools and Flows

A simple manual design flow

Layout

Parameterized devices in magic

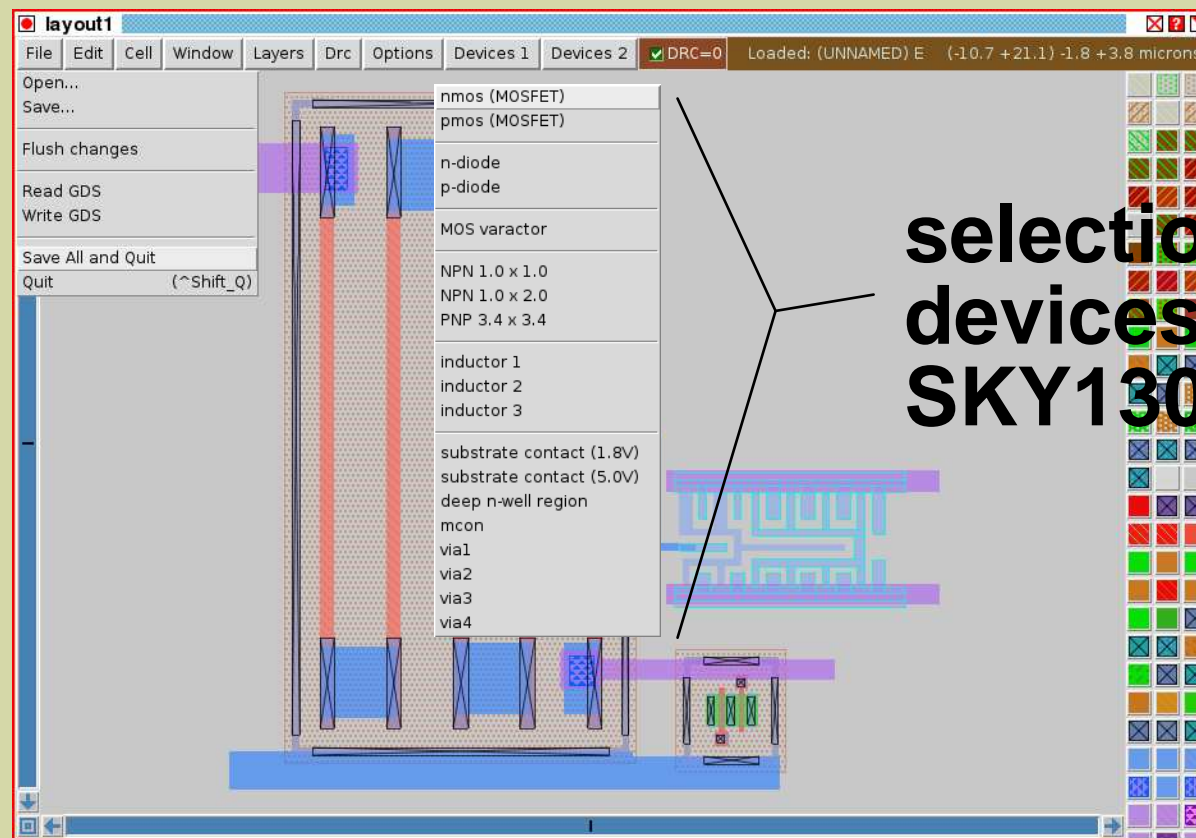


**PDK device
generation
menu**

Open Source Tools and Flows

A simple manual design flow

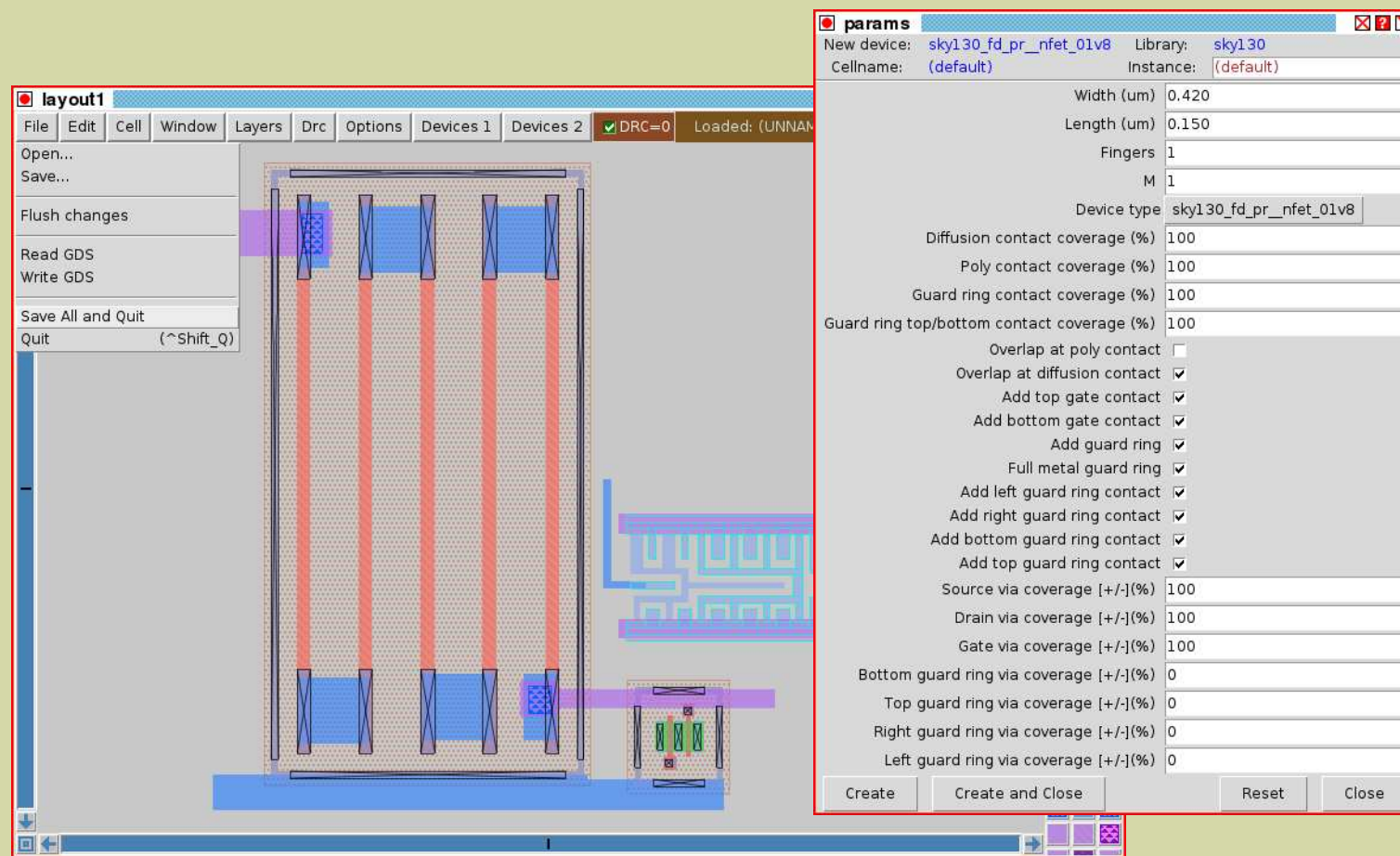
Parameterized devices in magic



Open Source Tools and Flows

A simple manual design flow

Parameterized devices in magic

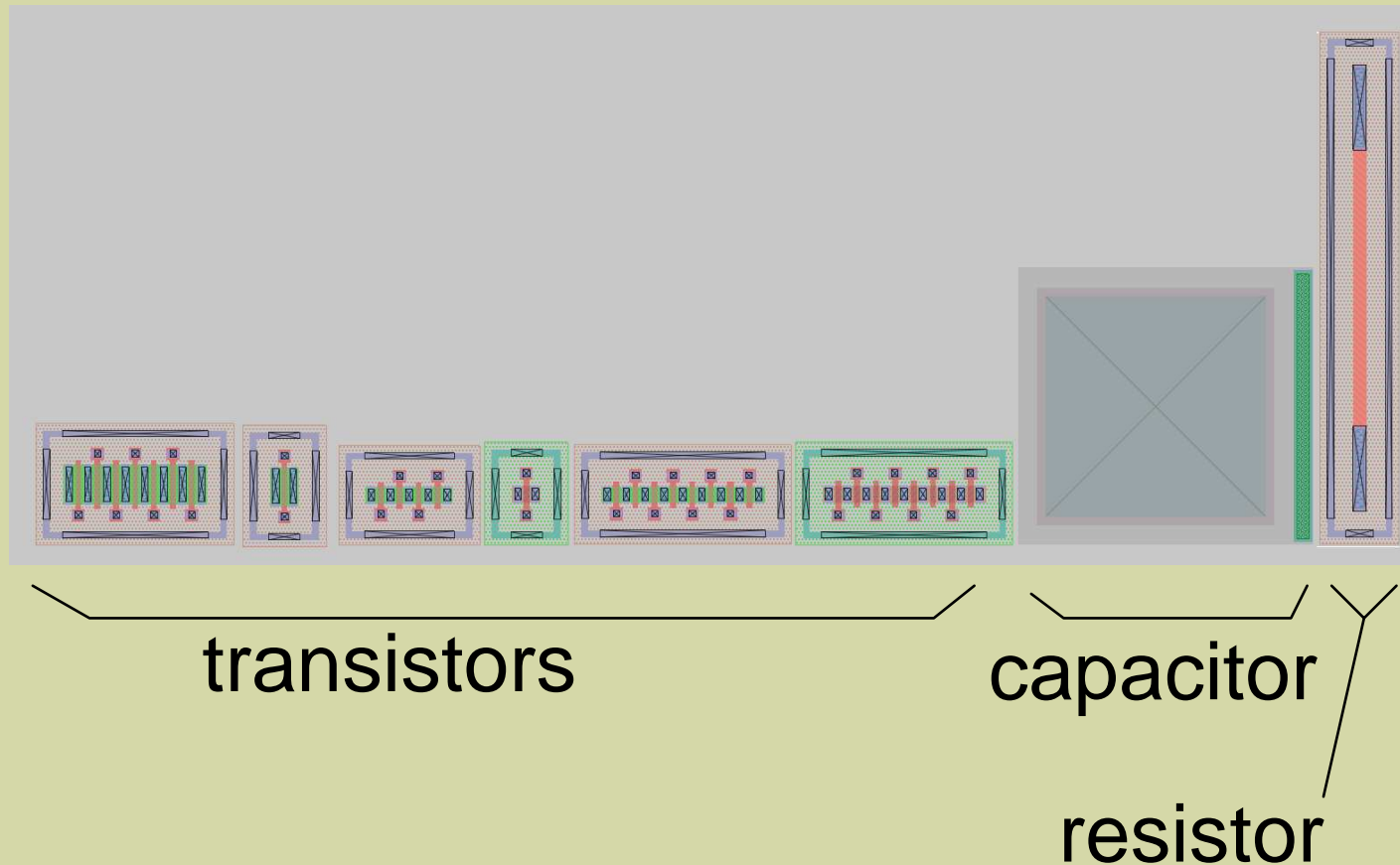


parameter selection
window

Open Source Tools and Flows

A simple manual design flow

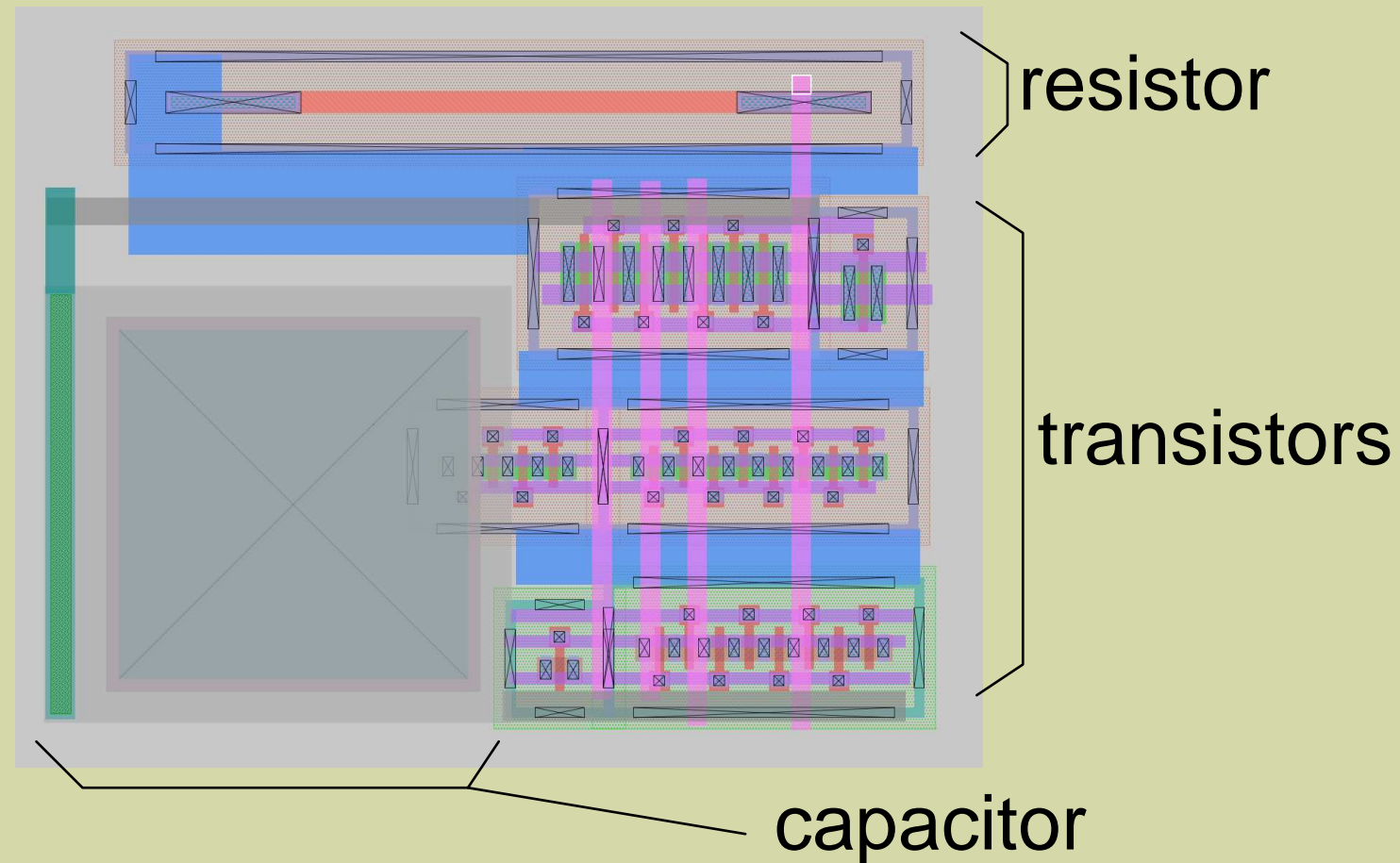
Example initial layout of devices in magic,
imported from schematic



Open Source Tools and Flows

A simple manual design flow

Analog example layout
work in progress in magic



Open Source Tools and Flows

A simple manual design flow

1. Schematic

export →

netlist
(SPICE format)



LVS (netgen)

2. Layout

export →

netlist
(SPICE format)



Analog design flow summary

1. **xschem** **Create a schematic, netlist extraction**
2. **ngspice** **Simulation validation**
3. **magic** **Layout, netlist extraction, DRC validation**
4. **netgen** **LVS validation**