

# Further PCB Design and Manufacturing

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# FPGA Workshop?

My proposal is:

- Two workshops
  - WTFpga - Implementing a 7 segment decoder at your own pace
  - LED Matrix / UART / Simulation / FPGA Theory
  - Verilog only (no SystemVerilog / VHDL)
- Requires Linux / Mac, may work on windows.
  - Will provide untested instruction for windows which may require different workflow - pull requests welcomed
- FPGA hardware will be \$50
  - iCE-40 FPGA in feather form factor
  - 7 Segment / DIP switch board
  - 6\*6 LED Matrix / Buttons
  - Feather to dual PMOD (bare PCB)
  - Want to assemble your own? Can be organised!
- Will get hardware to everyone before next meetup, so you can install toolchains / get to blinky at your own leisure

# Overview

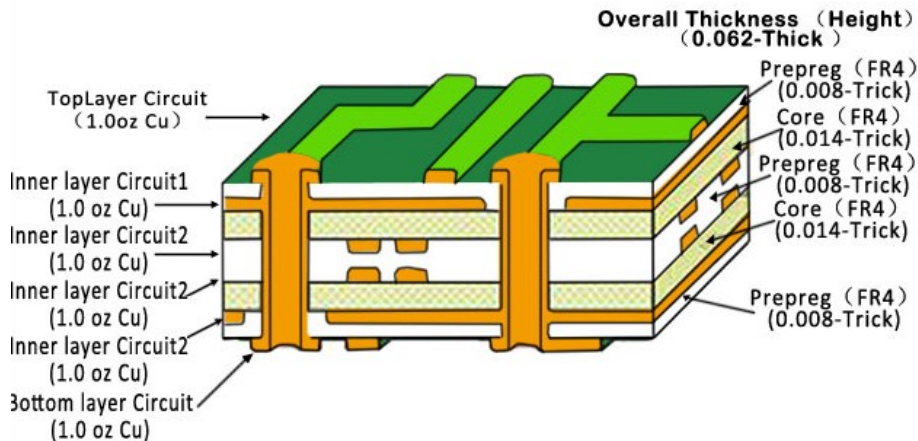
- Multilayer PCBs
- Impedance control
- Differential Pairs
- Cutting edge processes
- Panellisation
- Random KiCad things
- Layout Tips
- Layout Review

# Multilayer PCBs

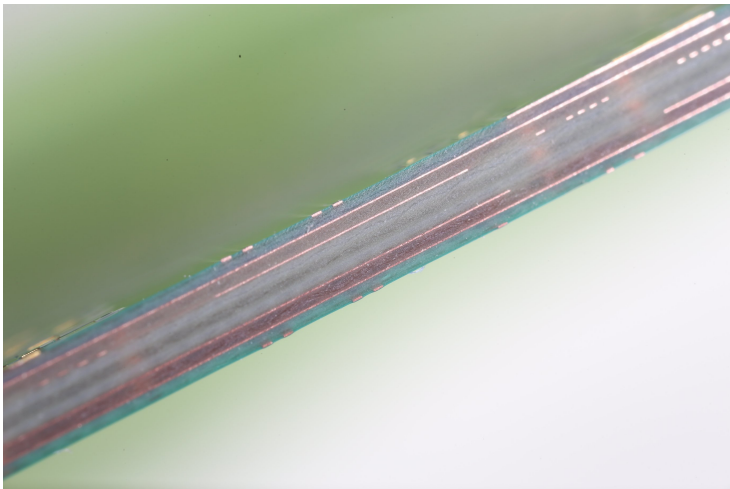
PCBs are often 2 or 4 layers, but 8-16 is common for phones / motherboards / GPUs etc. Why?

- Dedicated power / ground planes
  - Allows for low impedance supply and return of currents
  - Not only required for function of devices, but to pass emissions testing
  - Many different stackups, both material, spacing, and layer assignment (signal / gnd / power)
- More layers to route signals
- Required for BGA fanout
- Impedance control

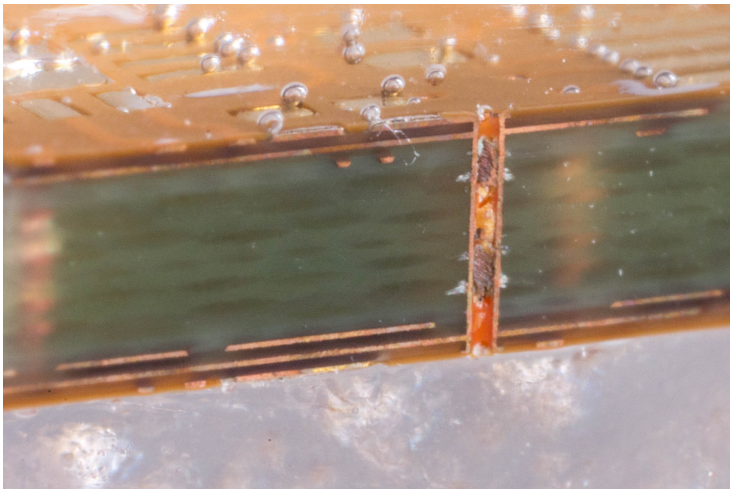
# PCB Stackup



# PCB Stackup


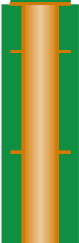






# PCB Stackup



# Via Technology

## Via Options

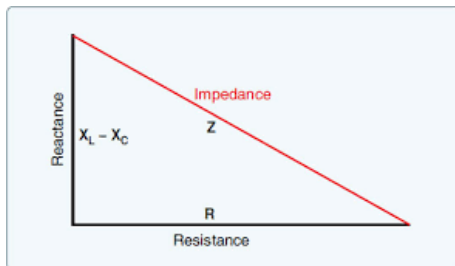
Cost	Standard	Standard	+\$	++	+++	+++
Duration	Standard	Standard	+⌚	+⌚	+⌚⌚	+⌚⌚
Type	Through Via 	Tented Via 	Blind Via 	Buried Via 	Stacked Via 	Via in Pad 



# Impedance Controlled Traces

What is impedance?

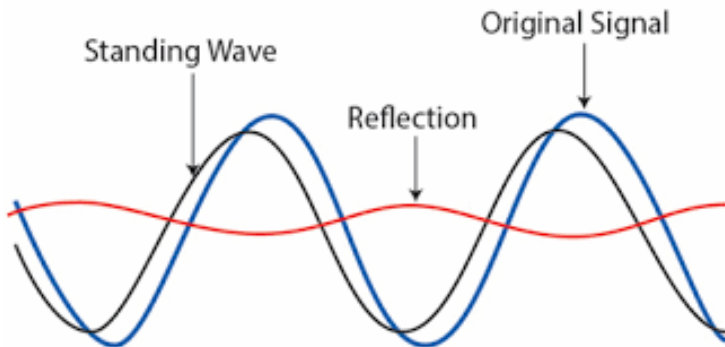
- the effective resistance of an electric circuit or component to alternating current, arising from the combined effects of ohmic resistance and reactance



# Impedance Controlled Traces

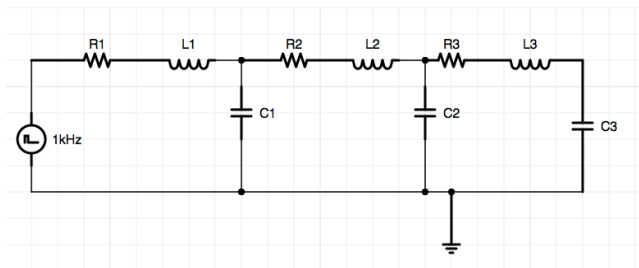
Why do we care?

- Impedance mismatch results in reflections, which causes power loss and signal degradation
- Mismatches caused by incorrect track width, stubs, lack of termination resistors



# Impedance Controlled Traces

## Transmission line model

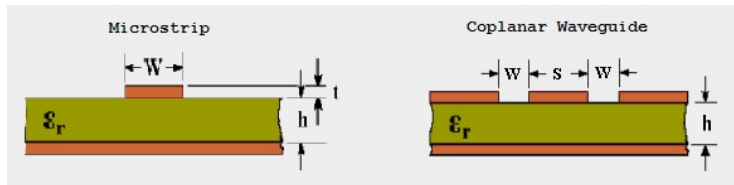


## Characteristic Impedance

$$Z_0 = \sqrt{\frac{L}{C}}$$

# Impedance Controlled Traces

## PCB transmission line



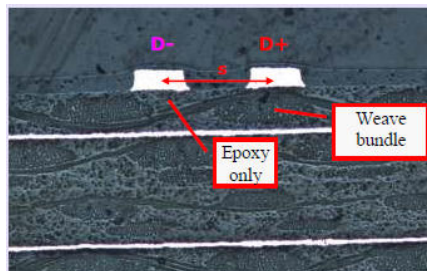
To calculate, use tools such as TXLine or Saturn PCB Toolkit

At higher frequencies, (above 2GHz) FR4 has high loss

Materials such as PTFE, Rogers 4003C / 4350B (glass reinforced hydrocarbon/ceramics) are better suited to higher frequency applications

Packing and orientation of glass weave can also play a part, along with surface roughness due to skin effect

# Glass Weave



106



1080



2113



2116



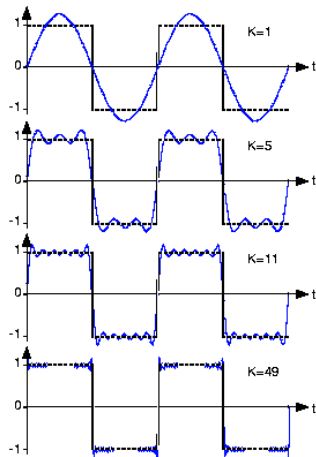
1652



7628

# Impedance Controlled Traces

I'm designing a digital board, so I don't have to worry about this?

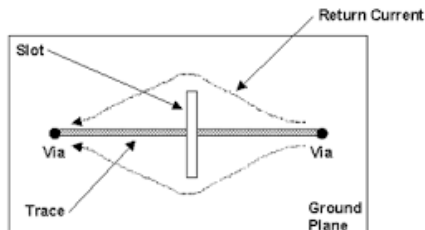


- Bandwidth =  $\frac{0.34}{t_{rise}}$
- Dependent on rise / fall times, not frequency (although higher frequencies do require faster edges)

# Impedance Controlled Traces

## Return current?

- Impedance controlled traces must be referenced to an unbroken plane (can be ground or power)
- As return current takes path of least impedance, follows path of outbound current!
- Slots, gaps, cut outs all result in return current taking a long path and emitting EMI



**SLOTTED GROUND PLANE**

# Path of least impedance

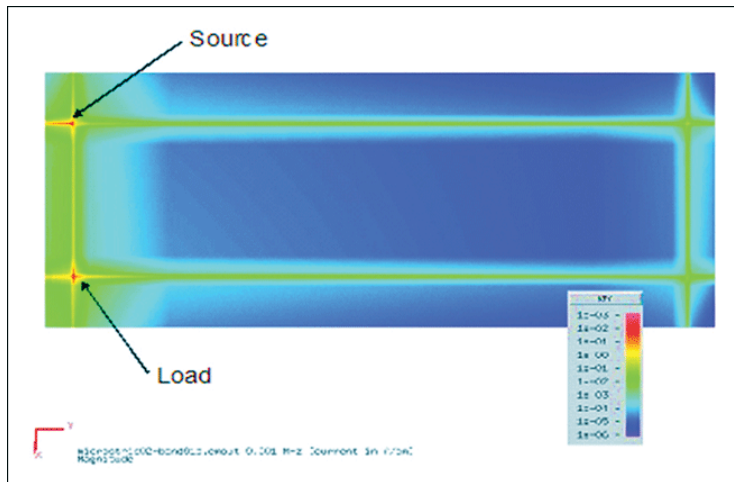
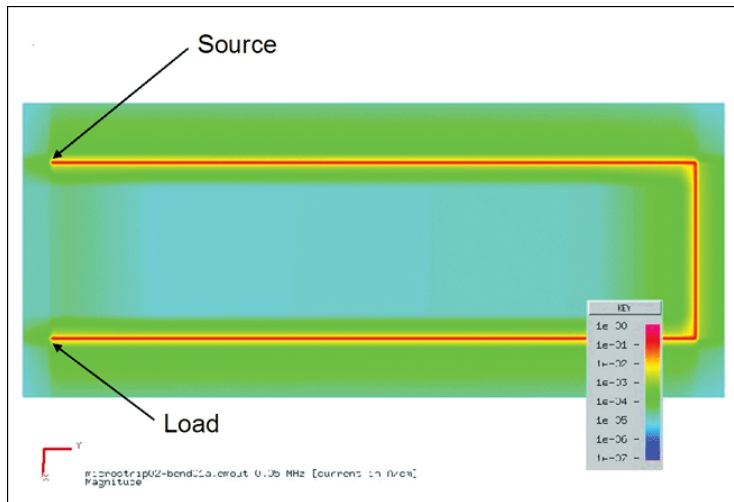


Figure: Currents for a 1kHz signal flow. The ground current primarily flows directly from the load to the source in a straight line, as indicated by the narrow yellow line.

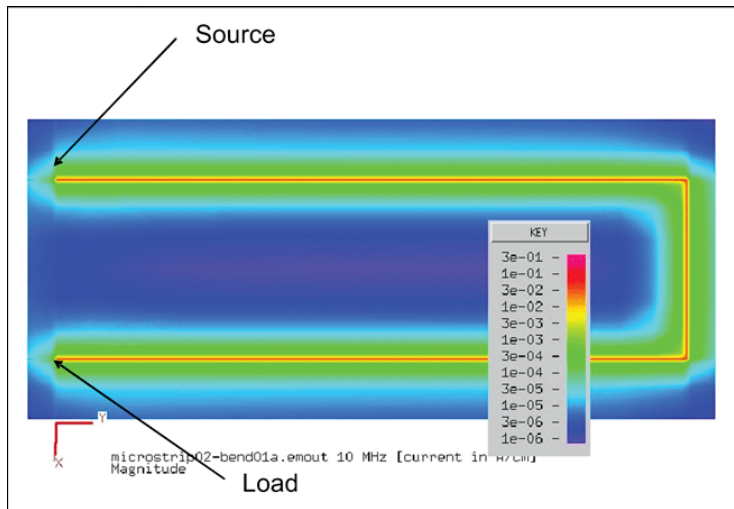


# Path of least impedance



**Figure:** Current for a 50kHz signal flowing primarily along the signal trace and, to a lesser extent, directly from load to source.

# Path of least impedance

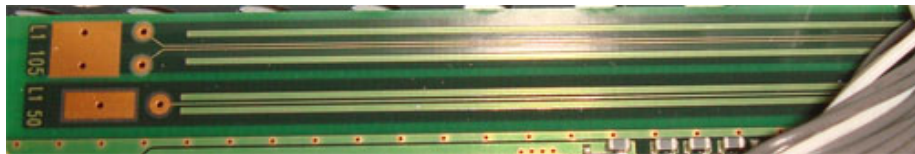


**Figure:** Current paths with a 1MHz signal. Virtually all the return ground current is flowing along the path of the signal trace

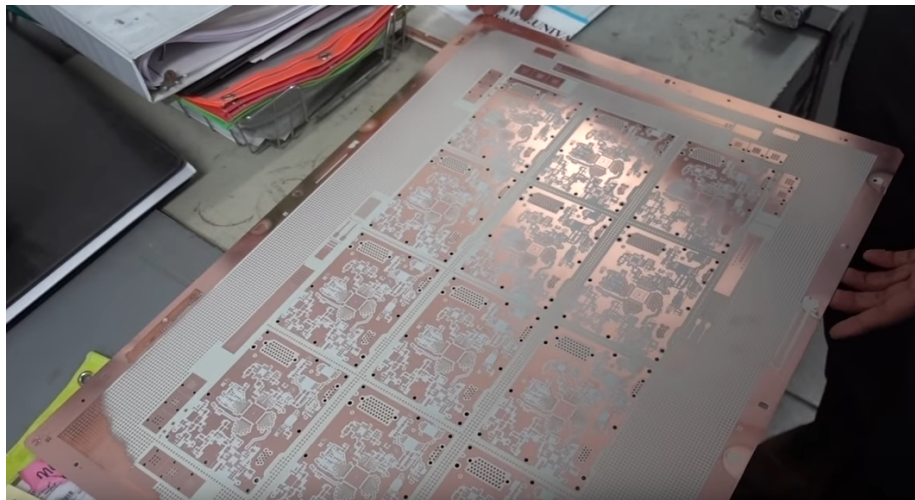
# Impedance Controlled Traces

## Confirming correct Impedance?

- Follow fabricators guidelines (NOT TXLine etc) they know their process best
- Board houses do what is known as 'Etch Compensation' to ensure traces stay at required impedance
- They can also make a test coupon, and measure with a TDR to ensure correct dimensions



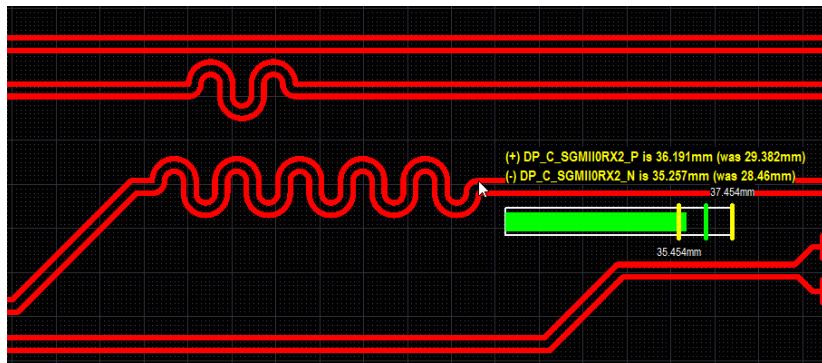
# Test Coupons



# Differential Pairs

Used on most high speed signals. Why?

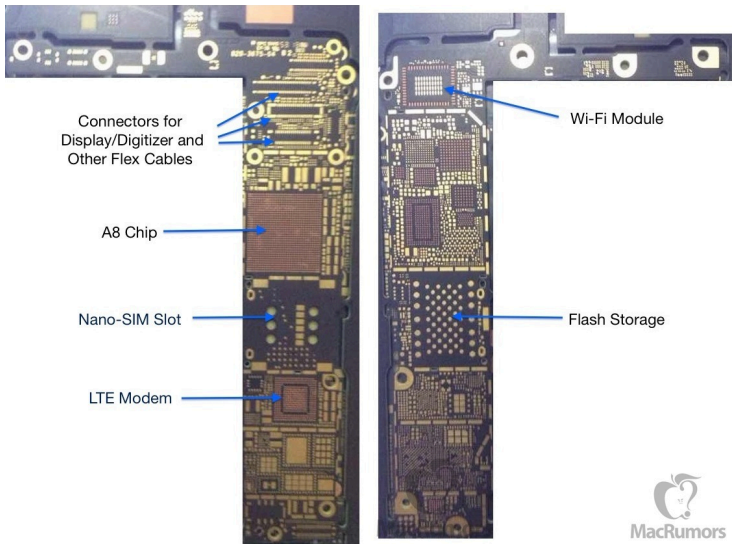
- Minimise crosstalk
- Better functioning in noisy environments
- Reduce electromagnetic interference
- Improvement in SNR
- Isolation from power supplies

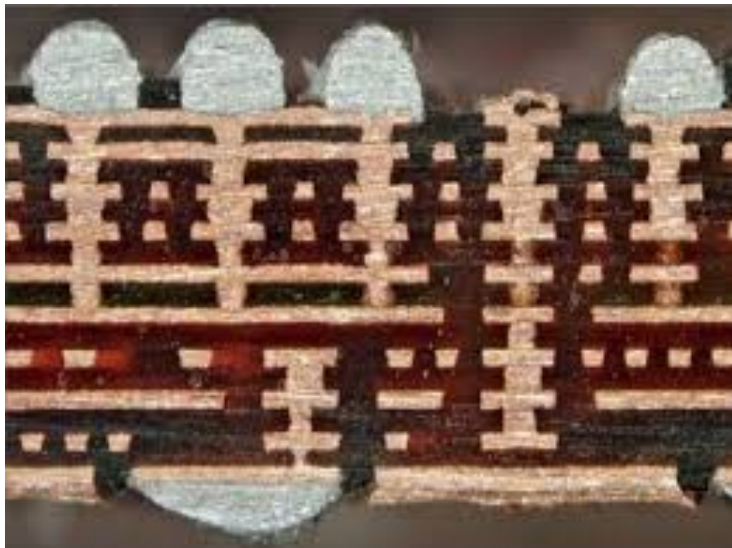


# Cutting edge processes

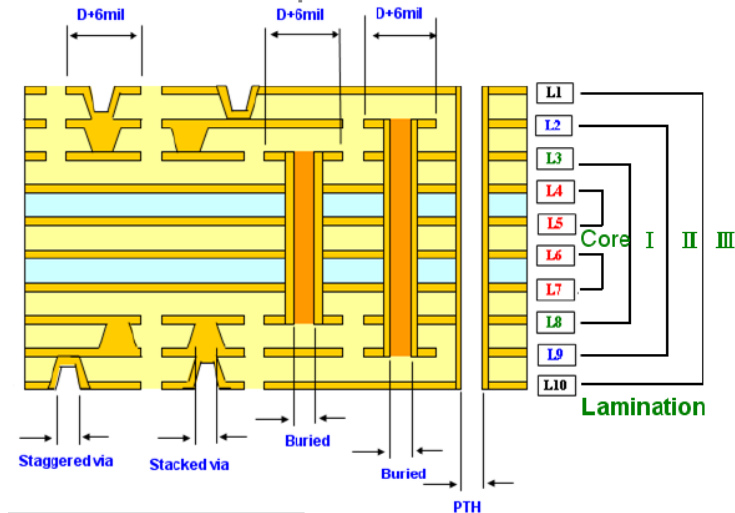
- Blind and buried vias
- Stacked microvias
- Filled and capped vias
- 2 thou (0.05 mm) trace and space
- High density interconnect (HDI)
- Greater than 10:1 aspect ratio vias (6:1 typical)
- Up to 20oz copper (700um, compared to typical 35um)
- Flex and rigid flex
- Distributed element filters
- Embedded passives

# iPhone

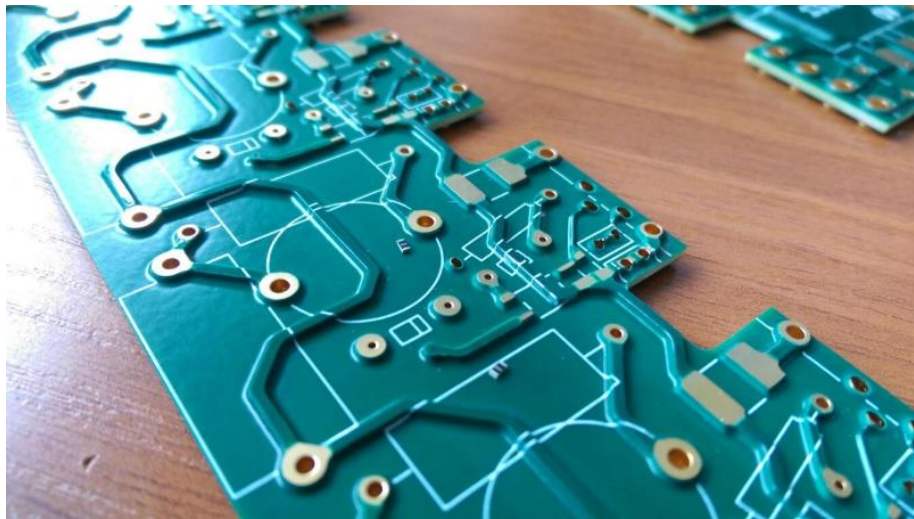




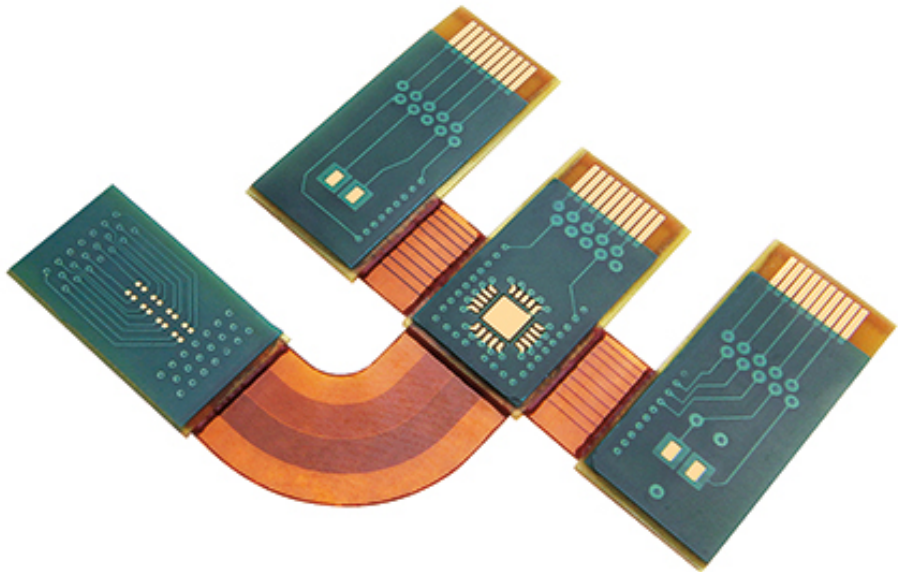




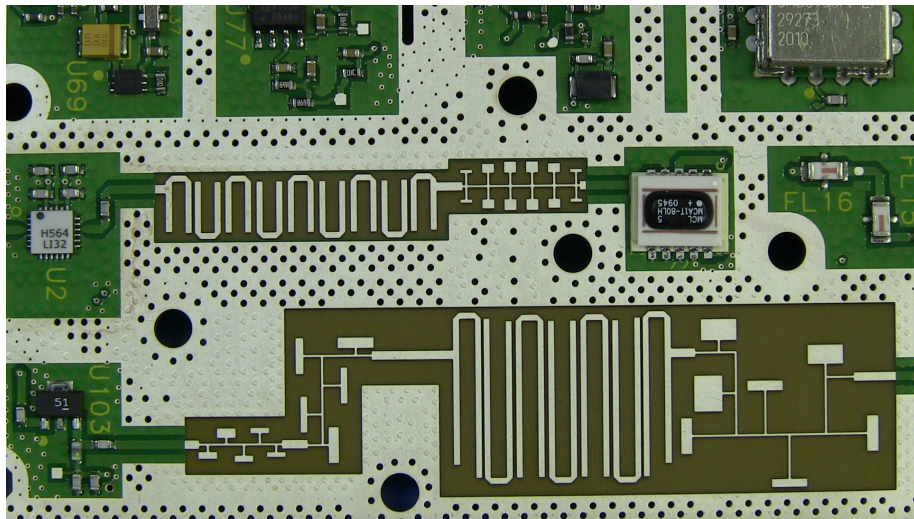
# High copper thickness



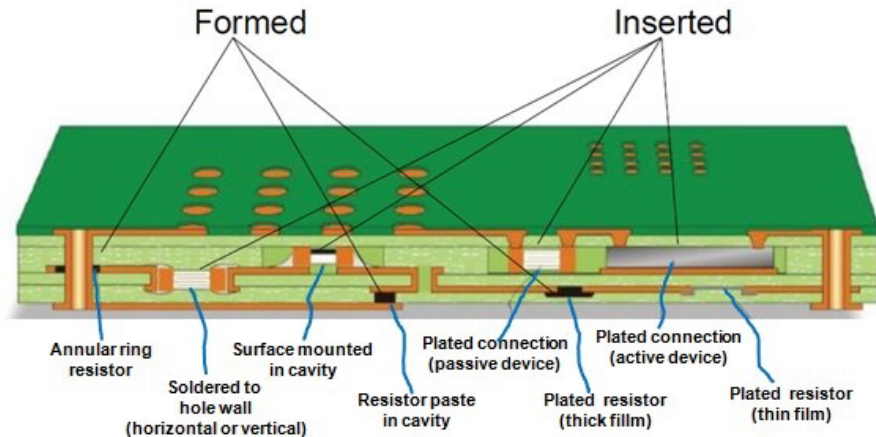
# Rigid Flex



# Distributed Element Filters



# Embedded Passives



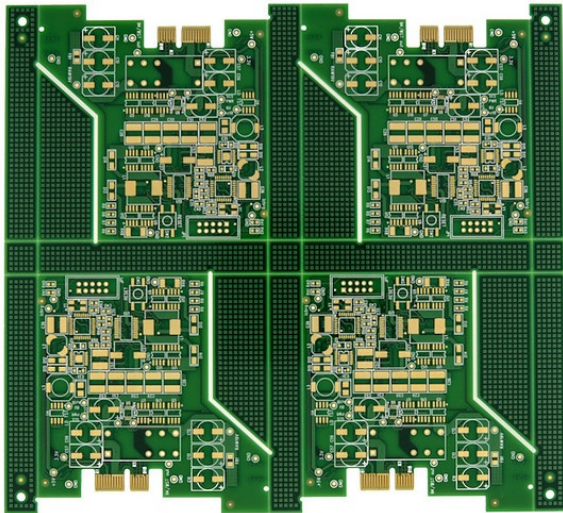
## Why do we panellise boards?

- To aide assembly - odd shaped or small boards cannot make it through a SMT line
- To aide programming and test - boards can be gang programmed / tested
- To get more boards for your money - either through sharing tooling charge between multiple people, or getting more boards under a dimension price break

## How to break boards out?

- V-Scoring
- Tab and route
- Combination of both

# Panellisation



# Random KiCad Things

- Library Management
- Panellisation using kicad-util
- Interactive HTML BOM



# Layout Tips

- Layout is 80% placement, 20% routing
- Don't push design rules because you can - bigger is better
- Place mounting holes and components first
- Use polygons where practicable
- Keep traces as short as possible
- Route key signals first
- Snake tracks - point to point is not more efficient
- Place decoupling caps close to power pins, smaller value closer
- Series termination resistors close to driver
- Tracks run into center of pads
- No acute angles on traces
- Multiple vias to stitch higher current nets
- Ensure ground / power plane is not cut up, stitch multiple planes together with vias

# Layout Review

- 2 layer Keyboard (mechanical constraints)
- 4 layer VNA (RF)
- 4 layer FPGA (somewhat dense)

# The End

FPGA Workshop Thoughts?

Say Hello!

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Project Files: [github.com/joshajohnson/CBRhardware](https://github.com/joshajohnson/CBRhardware)