furtherPCB

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12/8/2019

FPGA Workshop?

My proposal is:

- Two workshops
  - WTFpga - Implementing a 7 segment decoder at your own pace
  - LED Matrix / UART / Simulation / FPGA Theory
  - Verilog only (no SystemVerilog / VHDL)
- Requires Linux / Mac, may work on windows.
  - Will provide untested instruction for windows which may require different workflow - pull requests welcomed
- FPGA hardware will be $50
  - iCE-40 FPGA in feather form factor
  - 7 Segment / DIP switch board
  - 6*6 LED Matrix / Buttons
  - Feather to dual PMOD (bare PCB)
  - Want to assemble your own? Can be organised!
- Will get hardware to everyone before next meetup, so you can install toolchains / get to blinky at your own leisure

Overview

- Multilayer PCBs
- Impedance control
- Differential Pairs
- Cutting edge processes
- Random KiCad things
- Layout review

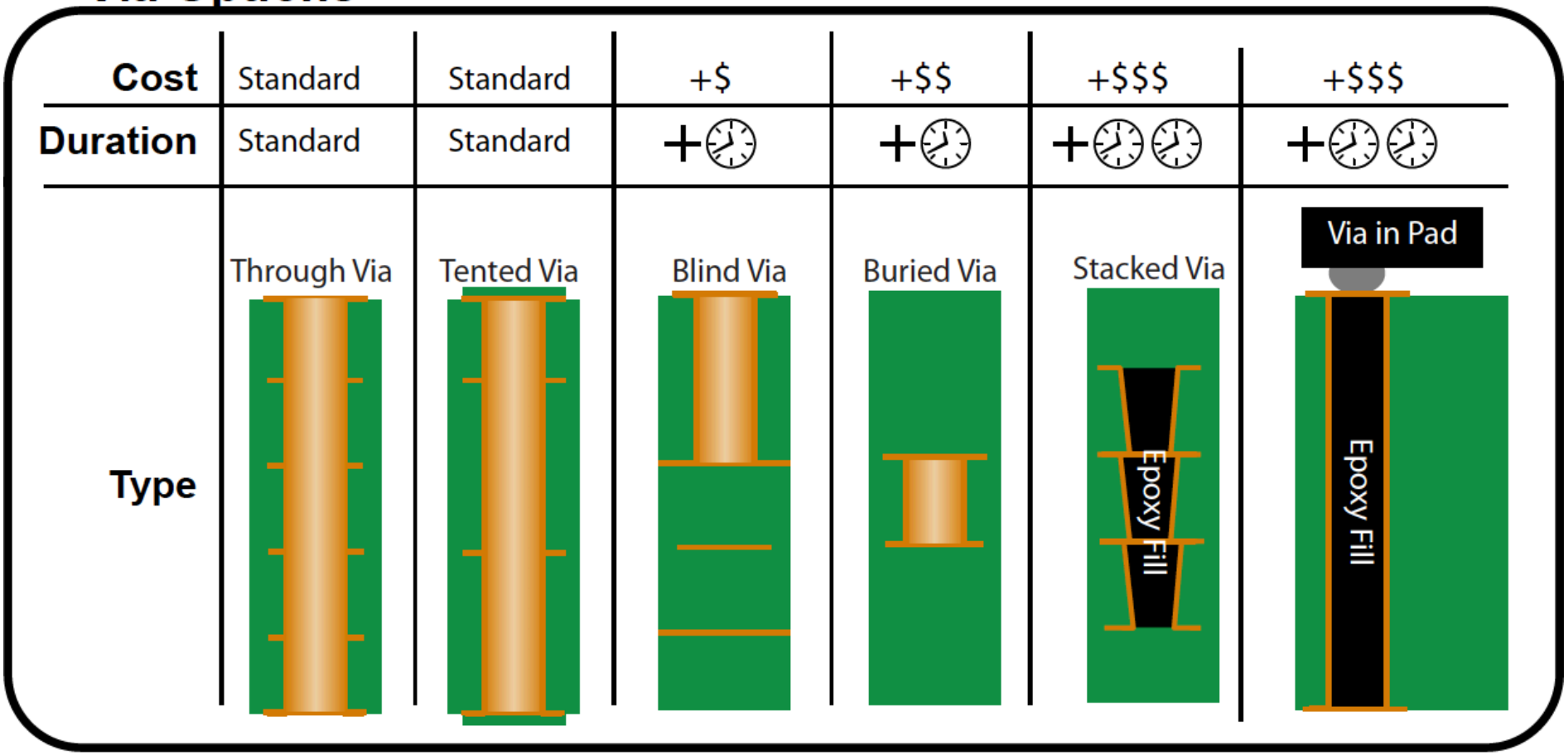
Multilayer PCBs

PCBs are often 2 or 4 layers, but 8-16 is common for phones / motherboards / GPUs etc. Why?

- Dedicated power / ground planes
  - Allows for low impedance supply and return of currents
  - Not only required for function of devices, but to pass emissions testing
  - Many different ways to design multilayer boards, will be shown later
- More layers to route signals
- Required for BGA fanout
- Impedance control

Via Technology

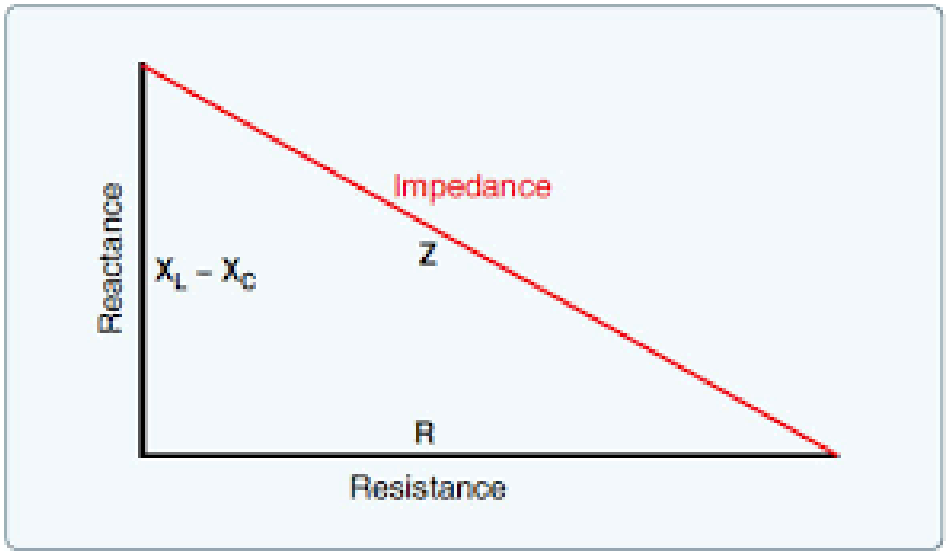
Via Options



Impedance Controlled Traces

What is impedance?

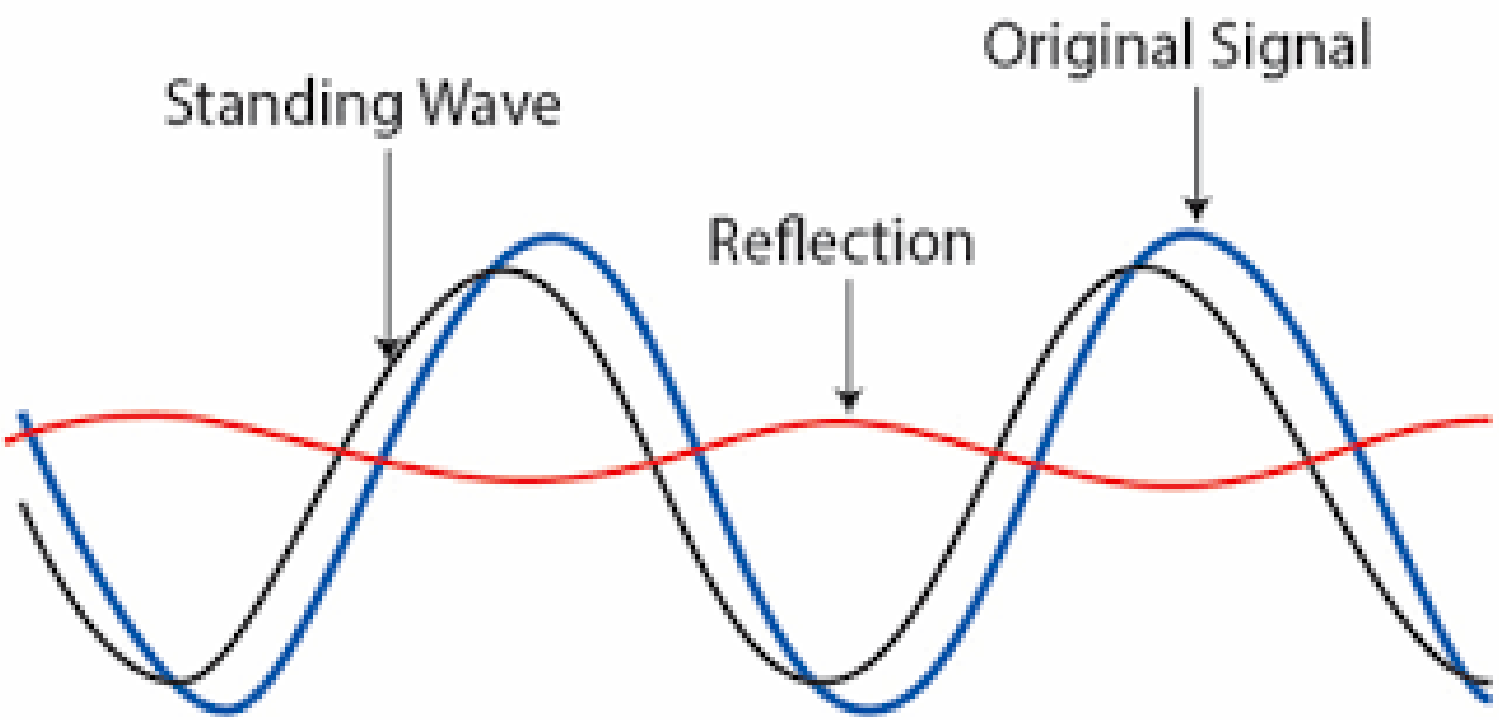
- the effective resistance of an electric circuit or component to alternating current, arising from the combined effects of ohmic resistance and reactance



Impedance Controlled Traces

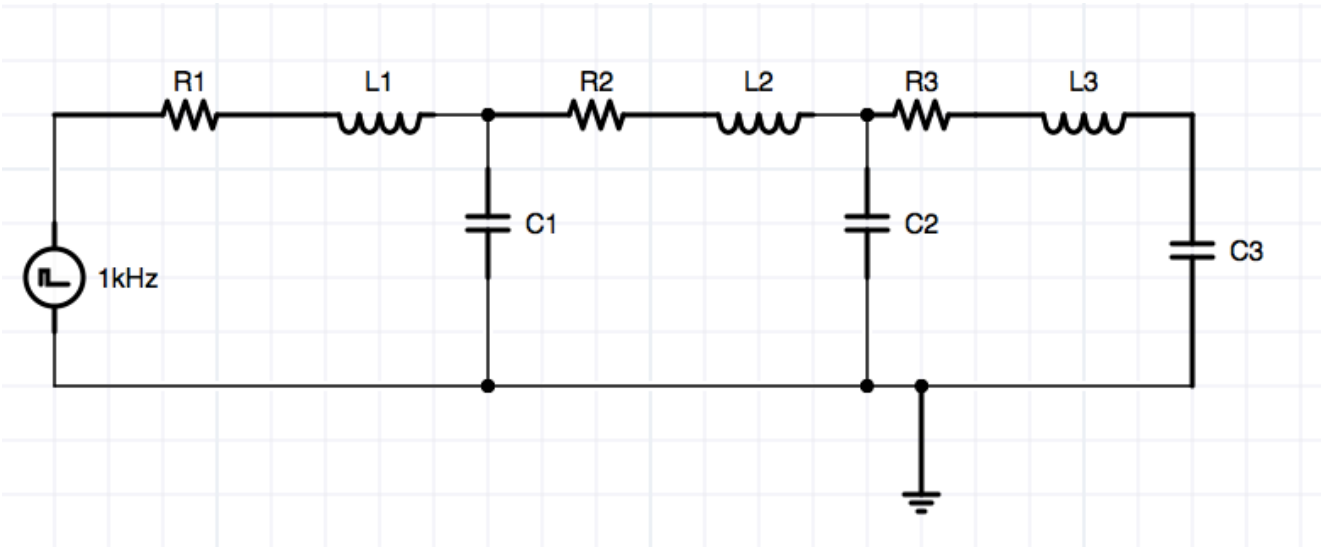
Why do we care?

- Impedance mismatch results in reflections, which causes power loss and signal degradation
- Mismatches caused by incorrect track width, stubs, lack of termination resistors



Impedance Controlled Traces

Transmission line model

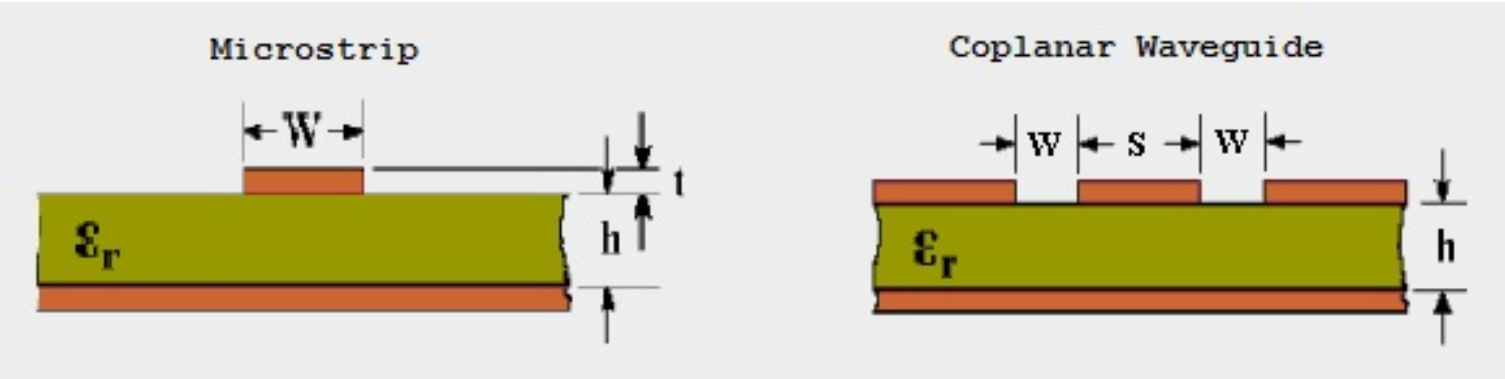


Characteristic Impedance

$$Z_0 = \sqrt{\frac{L}{C}}$$

Impedance Controlled Traces

PCB transmission line

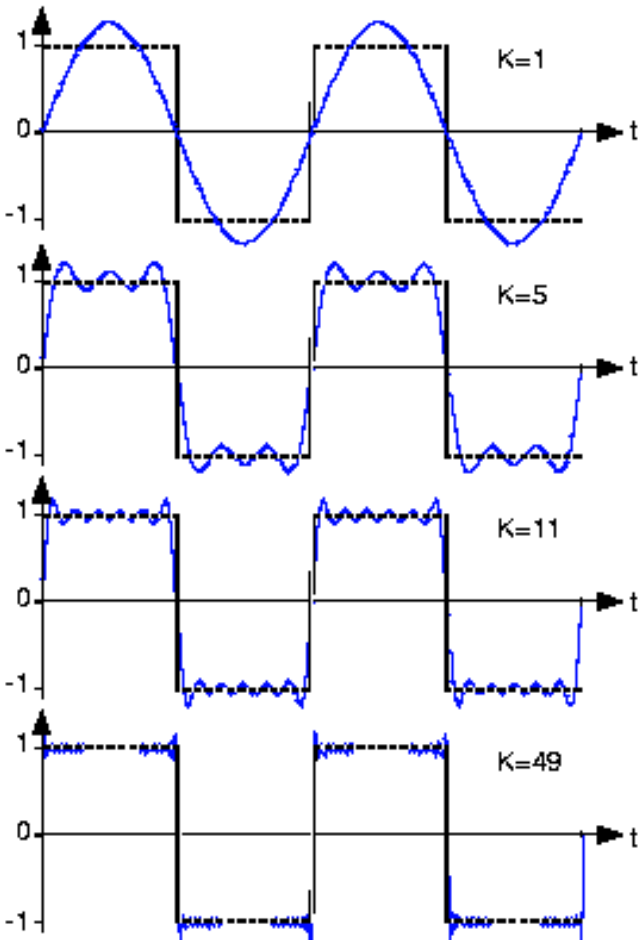


To calculate, use tools such as TXLine or Saturn PCB Toolkit

At higher frequencies, ($>$ 2GHz) FR4's dialectic constant changes + has high loss
Materials such as PTFE, Rogers (glass reinforced hydrocarbon/ceramics) are better suited to higher frequency applications
Packing and orientation of glass weave can also play a part

Impedance Controlled Traces

I'm designing a digital board, so I don't have to worry about this?

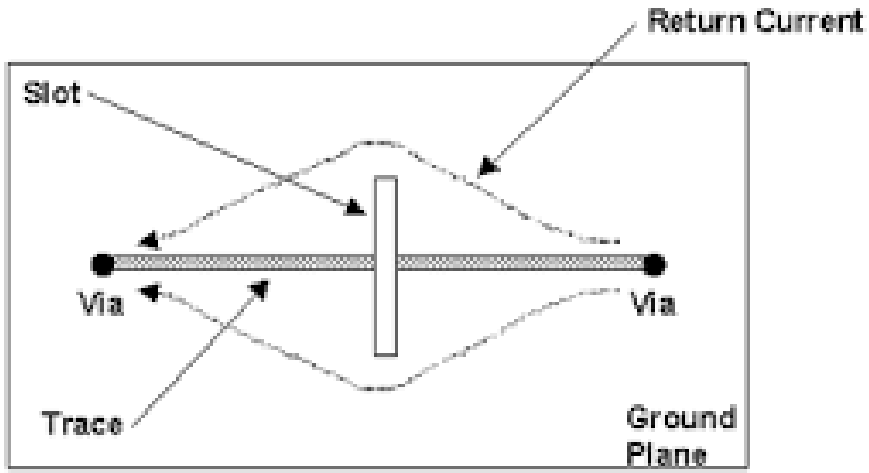


- Bandwidth $= \frac{0.34}{t_{rise}}$
- Dependent on rise / fall times, not frequency (although higher frequencies do require faster edges)

Impedance Controlled Traces

Return current?

- Impedance controlled traces must be referenced to an unbroken plane (can be ground or power)
- As return current takes path of least impedance, follows path of outbound current!
- Slots, gaps, cut outs all result in return current taking a long path and emitting EMI

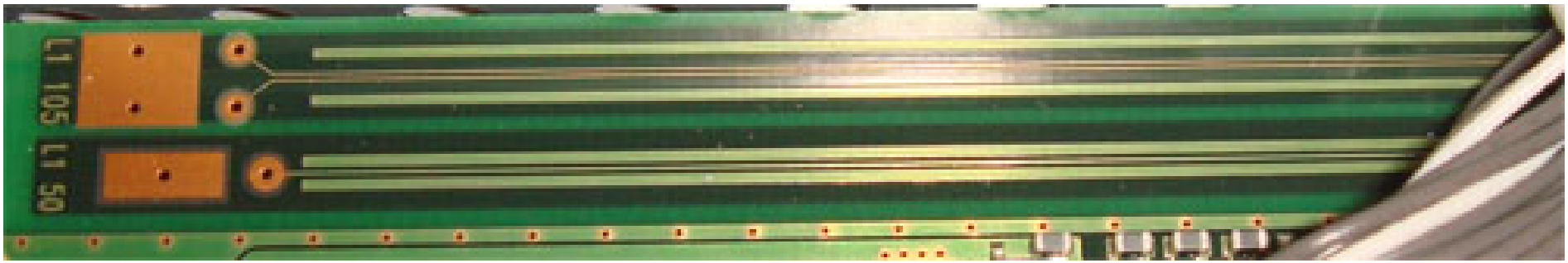


SLOTTED GROUND PLANE

Impedance Controlled Traces

Confirming correct Impedance?

- Follow fabricators guidelines NOT TXLine etc tools - they know their process best
- Board houses do what is known as 'Etch Compensation' to ensure traces stay at required impedance
- They can also make a test coupon, and measure with a TDR to ensure correct dimensions



The End

Say Hello!
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Project Files: `github.com/joshajohnson/CBRhardware`