FPGA102: More FPGA

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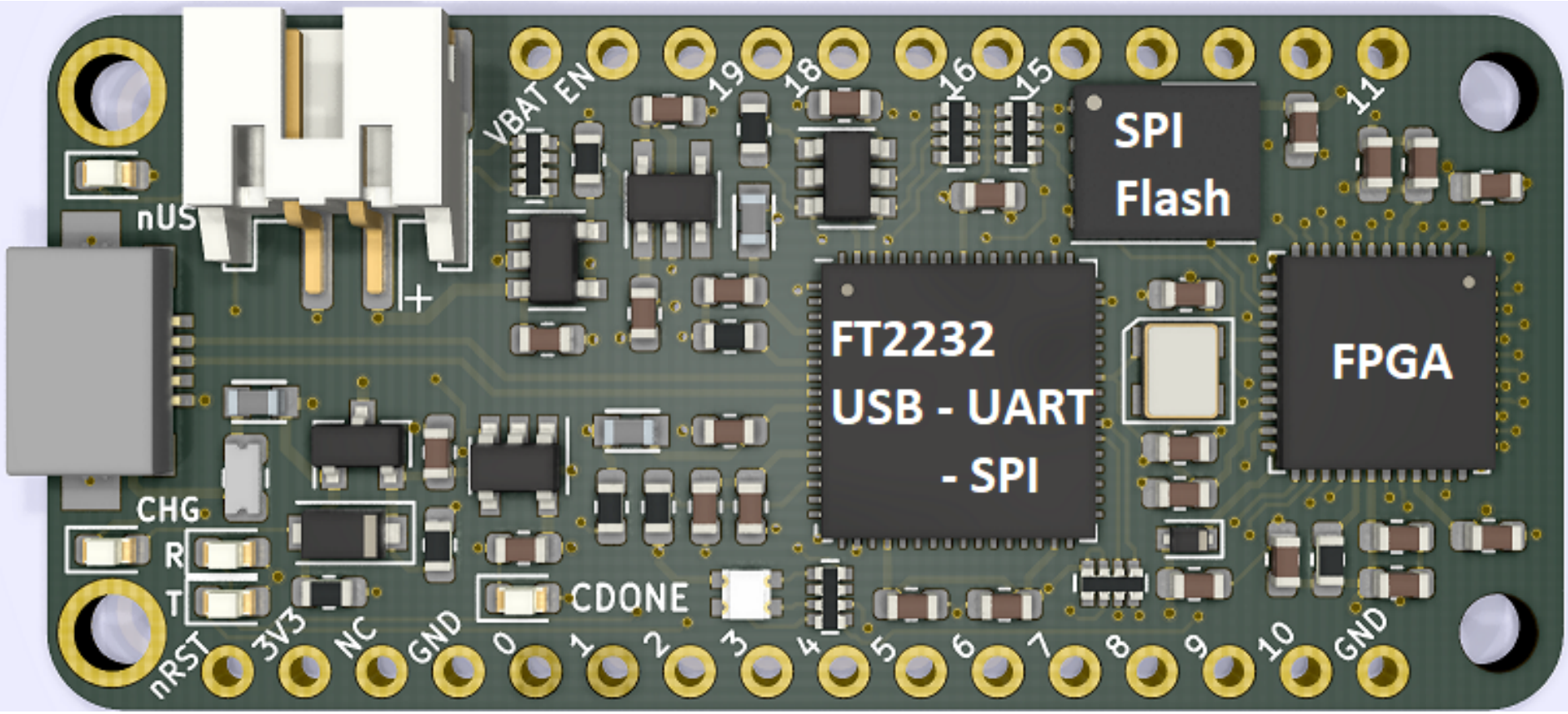
Overview

- Schematic / PCB Design
- Silicon Level
- Toolchain
- Demo time
  - PWM x 3
  - UART TX, RX
  - Dot

Project Files: `github.com/joshajohnson/CBRhardware`
Also on the memory stick being passed around

Schematic / PCB Design



Following slides stolen from Dave Shah

OSHUG - Open FPGA Toolchains

From Past to Present

David Shah
@fpga_dave
Symbiotic EDA

Slides: fpga.dev/oshug.pdf

Symbiotic EDA

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FPGA?

- Field Programmable Gate Array
- Chip containing **user-programmable** digital logic
- Can be (re)programmed “in the field” - older devices programmed once by literally burning fuses

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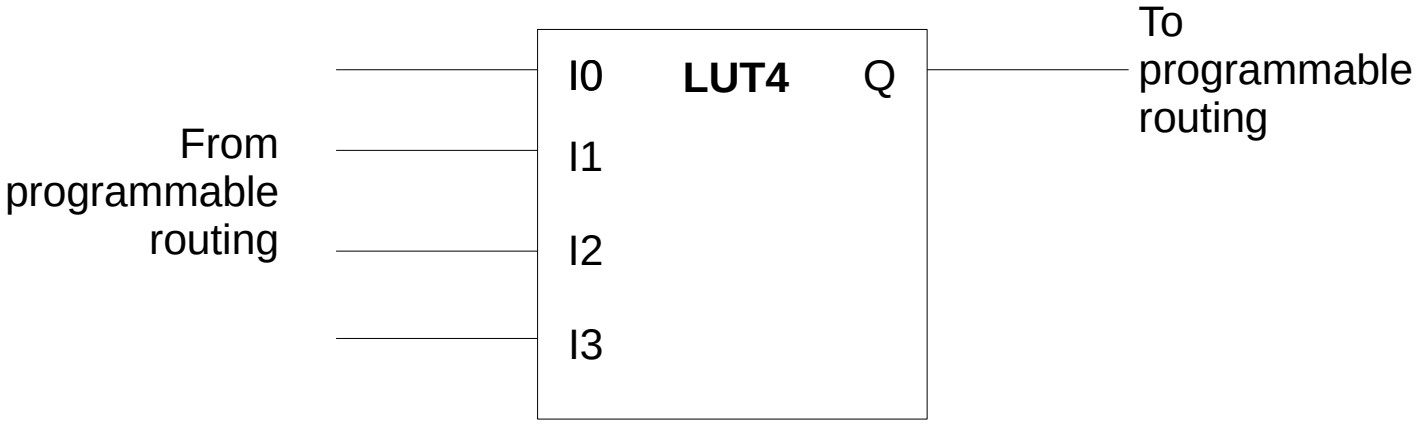
FPGA Logic



Look Up Table (LUT) – basic logic element of an FPGA

a K-input LUT has 2^K bits of memory storing its **function**
e.g. 4-input AND: `1000 0000 0000 0000`
4-input OR: `1111 1111 1111 1110`

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FPGA Logic

D-type flip flop (DFF) – basic storage element of an FPGA

D is stored at the rising or falling edge of **CLK**

Combine DFFs and LUTs to build sequential logic such as state machines, counters, CPUs, ...

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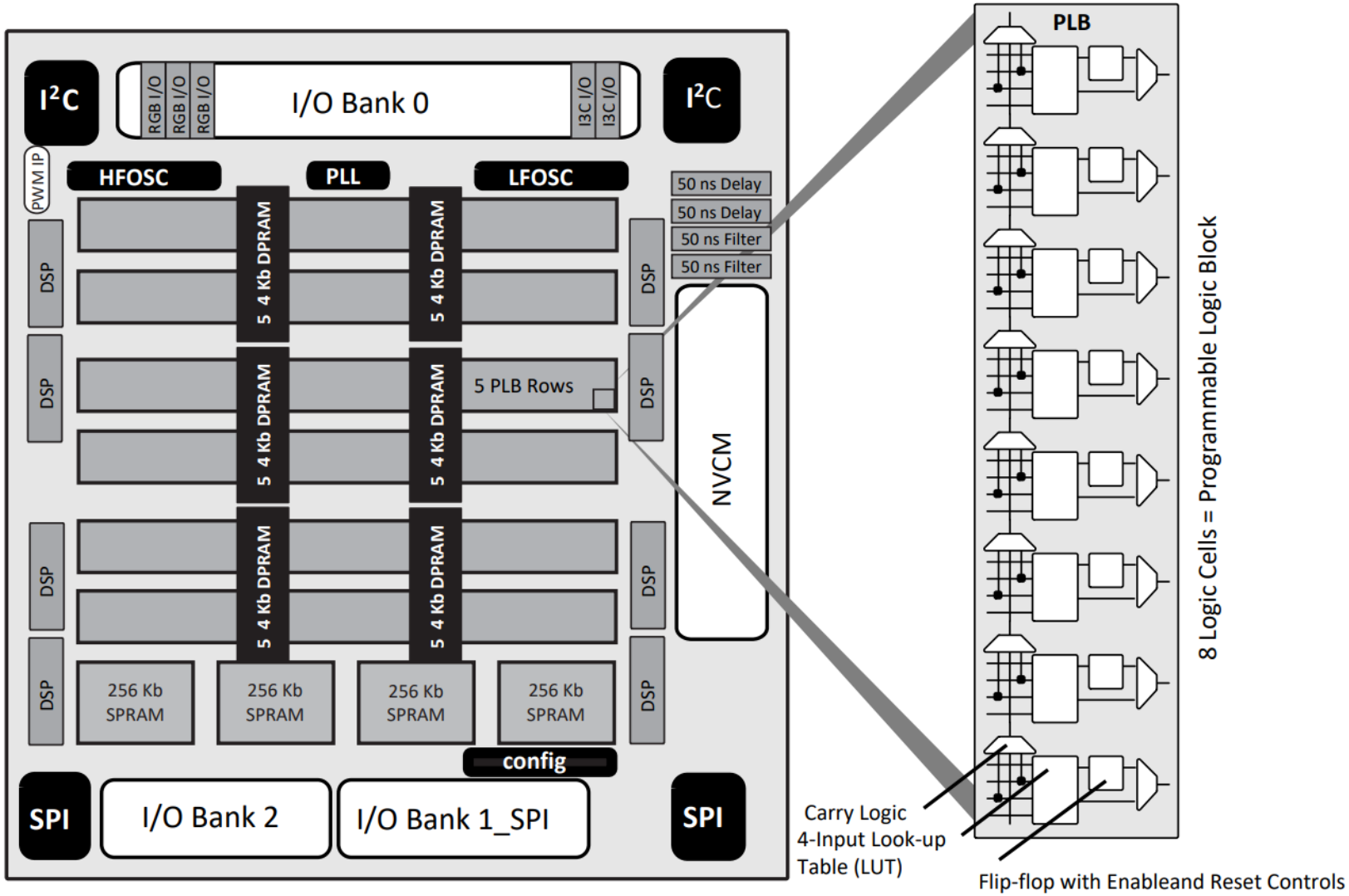
Silicon Level



Silicon Level

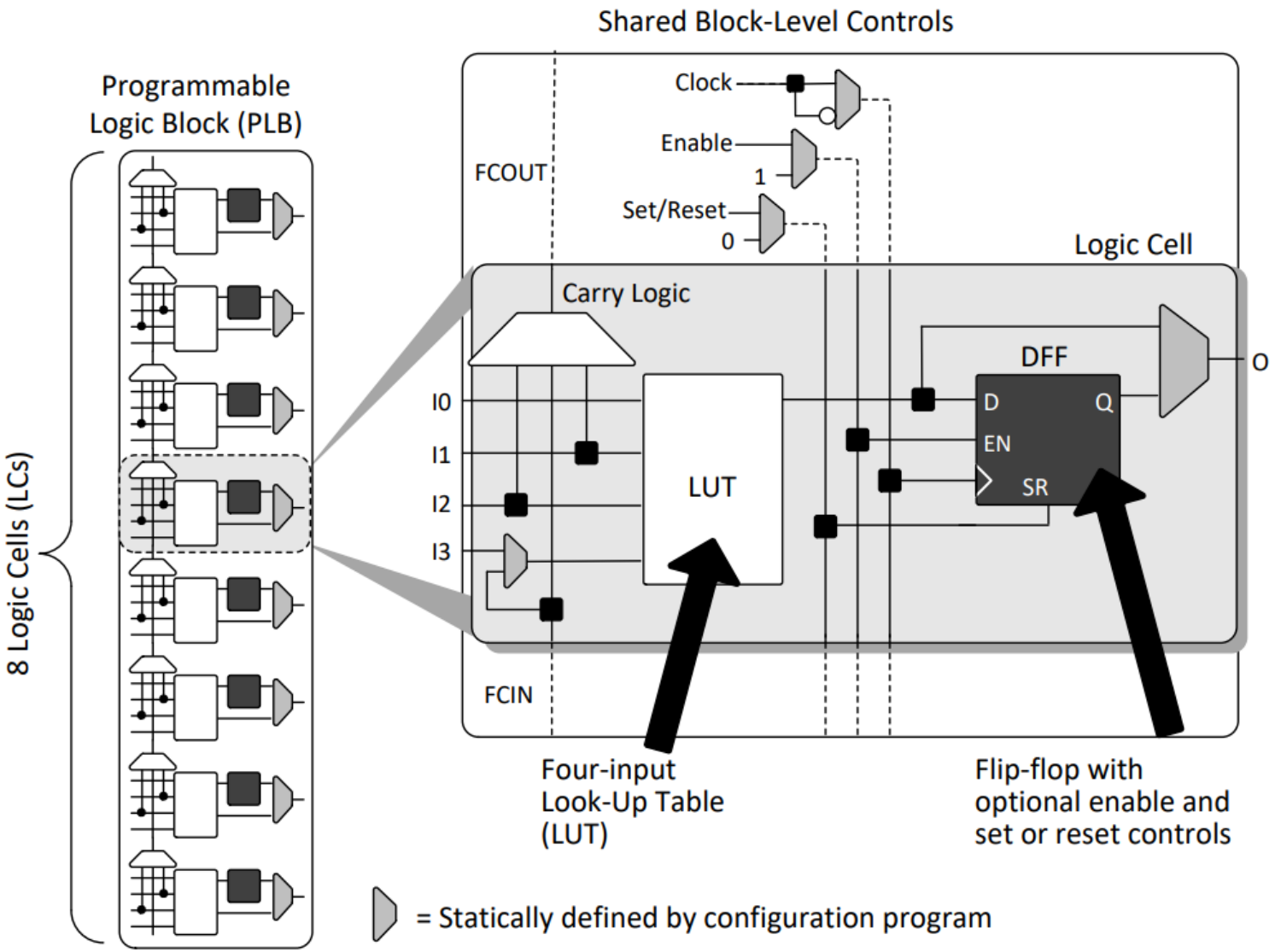
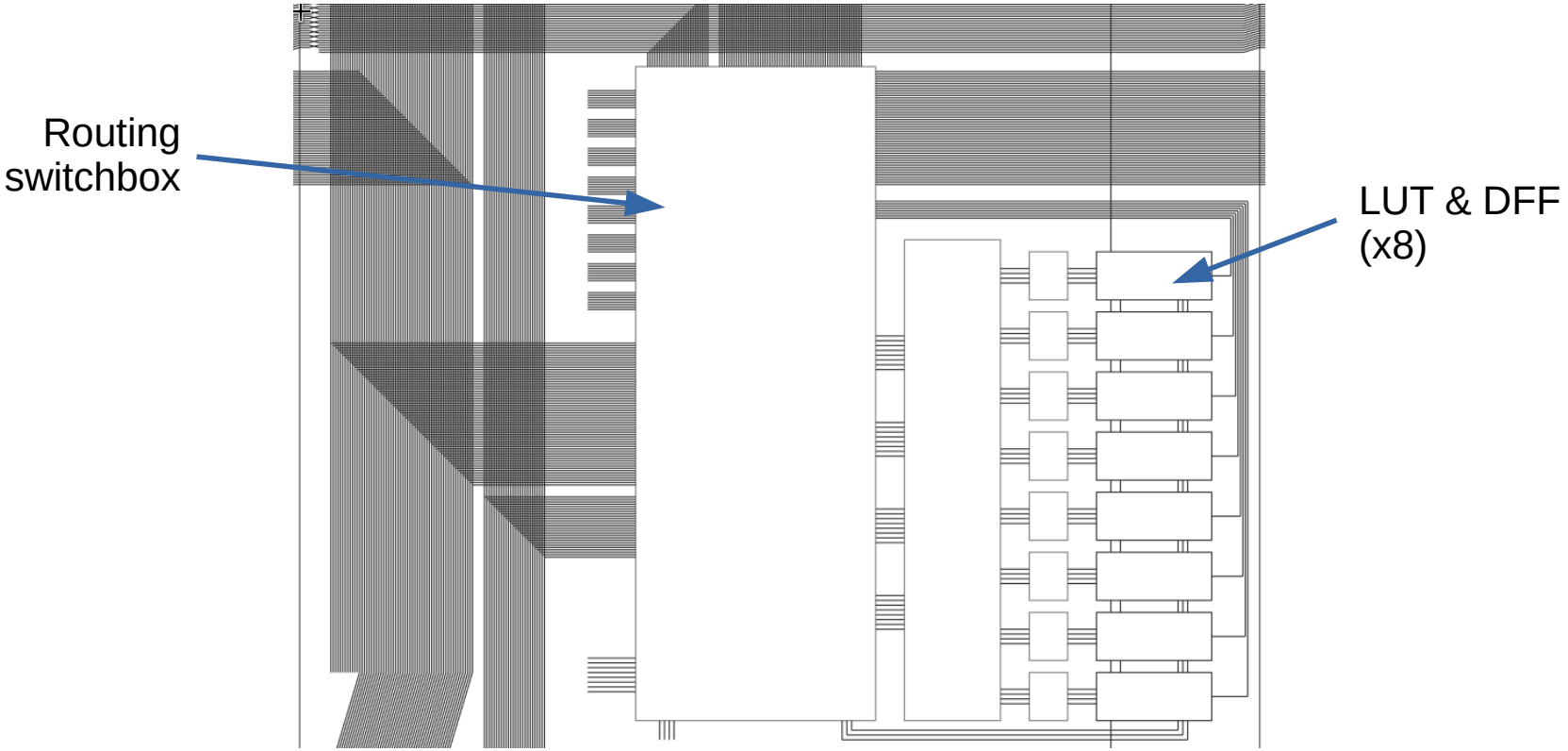


Figure 3.2. PLB Block Diagram

FPGA Structure



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FPGA Structure

- Modern FPGAs aren't just LUTs and DFFs!
- Block RAM: dual port SRAM, usually 4-36 kbit
- DSP: multiplier and adders
- High speed IO blocks for DDR memory, HDMI, PCI Express, etc
- Even CPUs! (Zynq ARM cores, Virtex-II Pro PPC)

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Toolchain

Steps required to turn Verilog into working hardware.

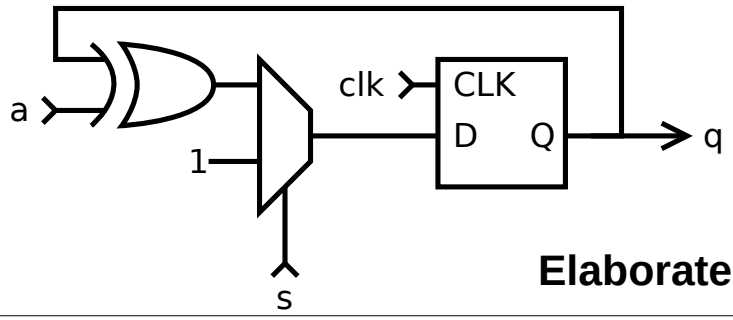
- Synthesis: Verilog to logic gates (Yosys)
- Place and Route: Physically connect LUTs in FPGA (nextPNR)
- Programming: Load bitstream onto FPGA (iceStorm)

Watch this for more info:
https://www.youtube.com/watch?v=A5AHglpfdtQ

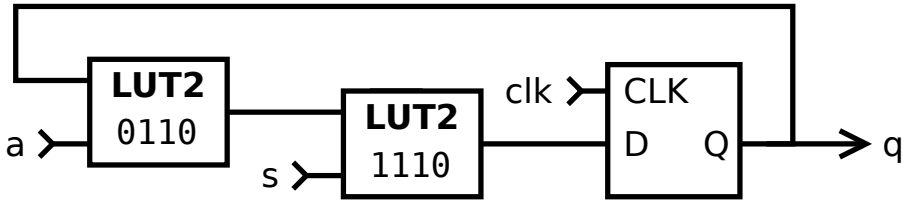
Synthesis

```
module top(
    input clk,
    input a, s,
    output reg q
);

always @(posedge clk)
    if (s)
        q <= 1;
    else
        q <= q ^ a;

endmodule
```

Verilog Source



Elaborated Circuit



Mapped to 2-input LUTs

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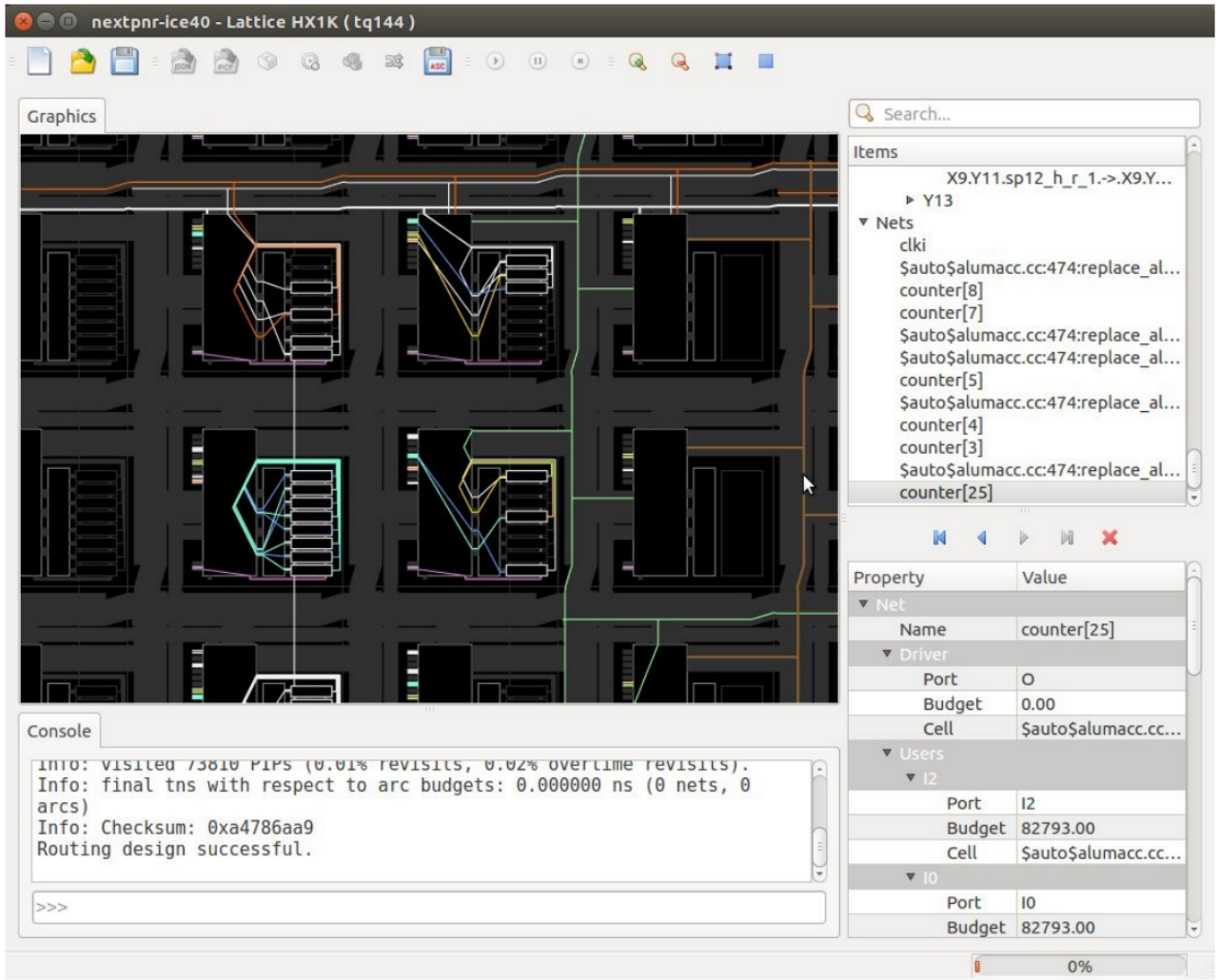
nextpnr


nextpnr-ice40 - Lattice HX1K (tq144)
Graphics
Search...
Items
X9.Y11.sp12_h_r_1.->.X9.Y...
Y13
Nets
clki
$auto$alumacc.cc:474:replace_al...
counter[8]
counter[7]
$auto$alumacc.cc:474:replace_al...
$auto$alumacc.cc:474:replace_al...
counter[5]
$auto$alumacc.cc:474:replace_al...
counter[4]
counter[3]
$auto$alumacc.cc:474:replace_al...
counter[25]
Property
Value
Net
Name
counter[25]
Driver
Port
O
Budget
0.00
Cell
$auto$alumacc.cc...
Users
I2
Port
I2
Budget
82793.00
Cell
$auto$alumacc.cc...
I0
Port
I0
Budget
82793.00
Console
Info: final tns with respect to arc budgets: 0.000000 ns (0 nets, 0 arcs)
Info: Checksum: 0xa4786aa9
Routing design successful.
>>>
0%

Demo Time - PWM

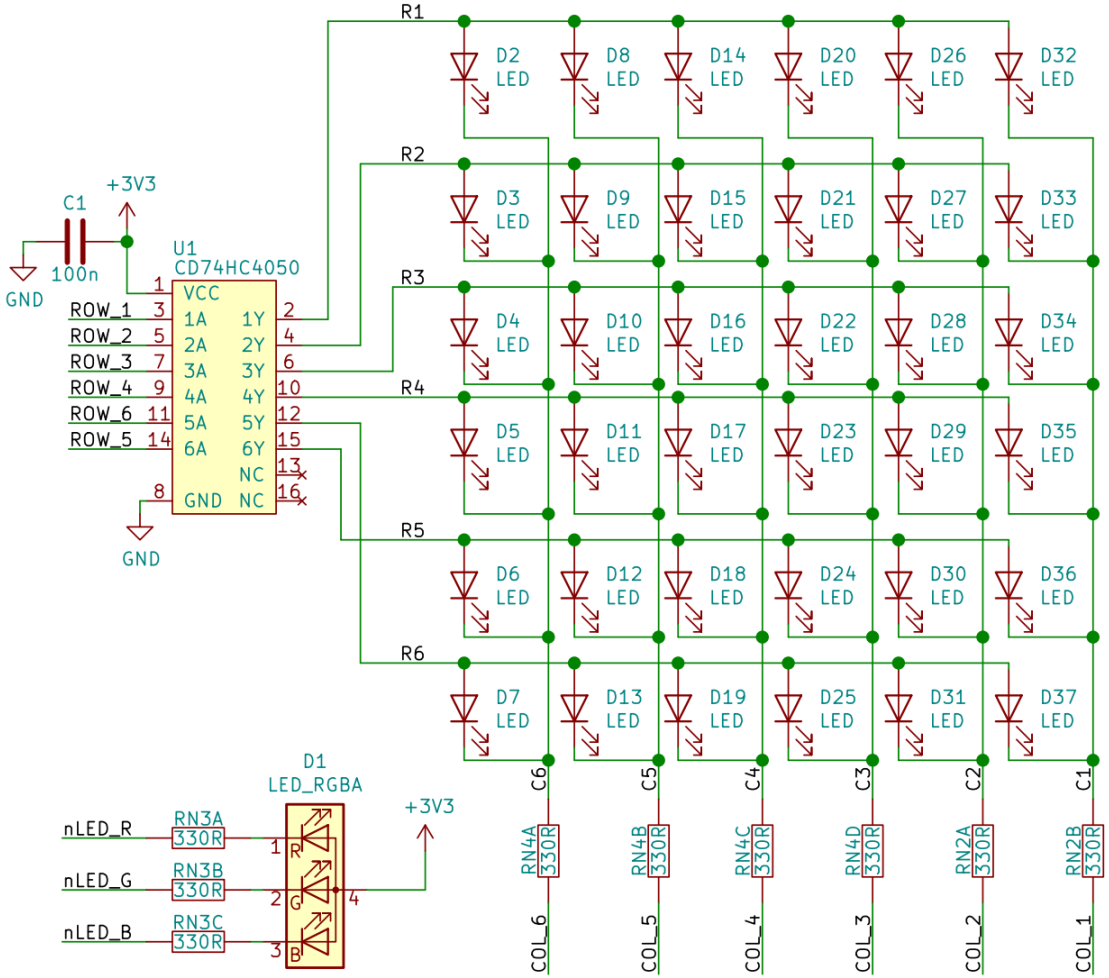
Three Demos showing how to PWM a LED

- Basic linear fade up / down
- Above but with three bugs - how to debug / setup simulation
- Gamma corrected PWM

Simulation Setup

- Install GTKwave and Icarus Verilog
- Create `fileName_tb.v` test bench and add required code
- Alternatively, can run `make new NAME="newName"` to copy from blink example with all files names changed
- Run `make simulate` to simulate and view waveforms
- Upon setting up GTKwave, go `file->write save file` to save current display
- Wayne has documented the process (see resources)
- Easier if I just show you...

LED Matrix



Yes (0,0) is top right corner (there is a reason for this!)

UART

Standard UART frame: 9600 Baud, 1 start bit (low), 8 data bits, LSB first, 1 stop bit (high).
To transmit: set pin as required.
To receive: sample half way through bit period

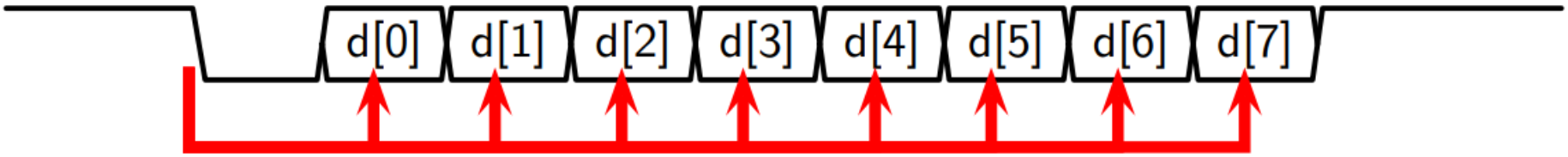


Image stolen from ZipCPU

The End

Links to resources: `fpga102/README.md`

Next month (11/11/19)
Unprepared talk on Electronic Test and Measurement, highlighting what tool is right for the job, limitations of equipment, along with how to do things on the cheap, and an overview of the VNA I built.

Future Months
I won't be here - talk to Silvio if you want to run the meetup

Say Hello!
BSidesCbr Slack: josh
Twitter: @_joshajohnson
Email: josh@joshajohnson.com

Project Files: `github.com/joshajohnson/CBRhardware`