Design of a Low Cost Vector Network Analyser

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This thesis contains no material which has been accepted for the award of any other degree or diploma in any university. To the best of the author's knowledge, it contains no material previously published or written by another person, except where due reference is made in the text.

Josh Johnson

30 September 2019

Abstract

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Glossary

ADC - Analog to Digital Converter.

ASIC - Application Specific Integrated Circuit.

COTS - Commercial Off-The-Shelf.

dB - Decibel.

dBm - Decibel power ratio with reference to 1 mW.

DDS - Direct Digital Synthesis.

DSP - Digital Signal Processing.

DUT - Device Under Test. With reference to a VNA, the device connected to VNA's ports being measured.

FPGA - Field Programmable Gate Array.

ISM - Industrial Scientific Medical.

IP3 - Third Order Intermodulation Product.

I/Q - In-phase / Quadrature. Used in DSP to represent two sinusoids which are 90 degrees out of phase.

LO - Local Oscillator.

P1dB - 1 dB Compression Point.

PA - Power Amplifier.

PCB - Printed Circuit Board.

PCBA - Printed Circuit Board Assembly.

PLL - Phase Locked Loop.

RF - Radio Frequency.

RFIC - Radio Frequency Integrated Circuit

S-parameters - Scattering Parameters. Elements of a scattering matrix which describe the behaviour of linear electrical networks.

S_{MN} - S-paramater describing the relationship between ports M and N in an electrical system. Common s-parameters are S_{11} which represents the reflected power incident on port one, and S_{21}, which represents the gain of a DUT between ports 2 and 1.

SPDT - Single Pole Double Throw switch.

SP4T - Single Pole 4 Throw switch.

VCO - Voltage Controlled Oscillator.

VNA - Vector Network Analyser. Electronic test and measurement instrument which measures s-parameters of electrical networks.

VSWR - Voltage Standing Wave Ratio

1 Introduction

1.1 Background

A Vector Network Analyser is a radio frequency test and measurement instrument which measures the s-parameters of a device under test. VNAs are used extensively in the design of RF devices as they allow the gain and phase response of RF components such as antennas, filters, amplifiers, and mixers to be characterised over the their operating frequencies, which is crucial for successful design and manufacturing of RF devices.

Vector network analysers work by generating a reference frequency which is passed into a device under test (DUT), and through comparing the incident and reflected RF signals from ports of the DUT the change in waveform caused by the DUT can be determined. Through sweeping the frequency, the response at each port of the VNA can be determined over a frequency range, and through signal processing the gain and phase response of each port of the DUT can be determined. From this data, S-paramater, VSWR, along with Smith chart and polar plots are able to be generated, which allows analysis of the DUT along with informed decisions regarding the function of the DUT to be made, which is required for the engineering of modern devices.

Given that VNAs are intricate pieces of engineering and are sold in low volume to engineering firms, their price represents this high level of performance and niche market, with VNAs typically ranging from tens of thousands to millions of dollars. Given this pricing is prohibitively expensive for teaching in educational institutions and far more than most electronics hobbyists have to spend, this limits the scope of projects and learning experiences which can be accessed outside of professional engineering environments.

1.2 Aim

The aim of this thesis is design and build a VNA which is significantly cheaper than the commercial offerings, as this will lower the barrier of entry to RF engineering and enable more hobbyists and educators to build or purchase a VNA which fits their needs. Whilst this VNA will not have the frequency and dynamic range, accuracy, UI, or speed of a commercial VNA, it will still be able to provide indicative measurements which are sufficiently accurate for home or educational use, along with providing an interesting learning exercise in the areas of radio frequency and embedded engineering.

1.3 Previous Work

Numerous people have attempted to make their own VNAs with varying specifications and architectures, and the work outlined in this thesis has been heavily inspired by many of these projects.

Henrik Forsten has designed two VNAs, both of which cost less than $1000 and operate upto 6 GHz. His first design [1] utilised printed microstrip couplers to couple the RF, along with a microcontroller with a 12 bit ADC sampling at 10 MSPS to sample downconverted RF. This design worked, however due to port to port leakage, variances with coupling over the frequency range, and slow processing due to the microcontroller struggling to keep up with the ADC sampling speed required.

Forsten's second design [2] replaced the microcontroller with an FPGA and external 14 bit, 40 MSPS ADC, which allowed both data capture and signal processing to be completed in real time. He also designed resistive bridge couplers which had significantly better performance over the required frequency range, and whilst this design preformed significantly better, the extra components resulted in an increased BOM and the couplers took up significant space. He did however show that a feature complete VNA could be manufactured for significantly less than commercial offerings, using processes and components which can be easily acquired by hobbyists.

Other architectures have utilised a dedicated RFIC in the form of Analog Devices' AD8302 gain and phase detector, which handles all of the gain and phase detection in silicon, and allows for low frequency sampling of two analogue outputs to determine gain and phase. This results in a significant decrease in signal processing required, allowing for lower cost embedded processors being utilised in the design.

One such design [3] utilised an AD8302 and COTS components in the form of development boards to prototype a VNA. That project showed that an AD8302 based VNA was practicable, however due to the use of development board for each functional block the cost came out to roughly $2000, significantly higher than the target for this project. The design also ran into issues regarding zero crossings of phase due to long conformance errors in the AD8302, however it was noted that this is likely correctable with sufficient signal processing.

Another design based around the AD8302 [4] utilised a direct digital synthesis IC with I and Q outputs to feed two AD8302 ICs, which enabled them to work around the zero crossing issue outlined above. However, due to the inherit limitations of DDS architecture, they were limited to 5 - 80 MHz, significantly less than the bandwidth of most VNAs.

1.4 Overview

Chapter 2 - Requirements, Constraints, and Specifications details the requirements and constraints of the VNA, and will enable the design scope and device specifications to be determined.

Chapter 3 - Design covers design of the VNA. Resulting from theory of operation and research of other low cost VNAs, the high level architecture along with detailed design was undergone and though testing candidate components were validated and selected.

Chapter 4 - Implementation and Assembly details printed circuit board layout along with assembly of the PCB. Furthermore, mechanical design of an enclosure along with firmware and software implementation is discussed.

Chapter 5 - Calibration and Testing covers calibration of the VNA, comparison of measurements to commercial VNAs, along with a discussion of the results and proposes future avenues for improvement of the VNA.

2 Requirements, Constraints and Specifications

2.1 Requirements

To be useful the VNA must be able to measure the gain and phase response of a DUT over a given frequency range, and have industry standard features including plotting and file handling which would allow it to replace a commercial VNA in certain situations.

2.2 Constraints

There are an number of constraints acting upon the project which will constrain the design and function of the device. The desire of the project is to build the most performant VNA that can be designed within the below constraints.

- **Cost -** as outlined in the introduction, the major goal of this project is to build a VNA at a significantly lower price than commercial offerings. As such, there will be a large number of trade-offs required to bring the price down, and as a result the accuracy, dynamic range, bandwidth, and numerous other performance characteristics will be traded off in an attempt to reach the desired price point.
- **Component Selection -** in an attempt to decrease the cost of low volume manufacture, along with the engineering time and resources required, all components in the design must be commercial off-the-shelf, as this will reduce the cost and time required during development and manufacturing.
- **Resources -** due to a number of factors including skill level of the designer, limited time frame, monetary resources available, and the lack to access to test gear and industry specific tools such as Keysight's Advanced Design System and CST Microwave Studio, the complexity of the project needs to be limited to ensure that a minimum viable product is able to be produced within the given time frame.

2.3 Specifications

Taking the above outlined requirements and constraints into consideration, specifications for the VNA can be determined. Given that there are no hard numbers specified, and that the goal for the VNA is one which is as performant and feature complete as possible given the constraints, many of the exact specifications of the VNA will be determined during the design process. This allows cost to be a key factor during the architecture design and components selection, as small decreases in performance are able to be made to save significant cost, which would not be possible if the system requirements were highly specified. In saying this, there are some key minimum specifications and high level architectural choices which will help narrow the design scope:

- **Bandwidth -** the VNA should have at least 1GHz of bandwidth, as this will allow both the 433MHz and 915 MHz ISM bands to be within the frequency span, and as such enable testing of components which can be utilised without a amateur radio licence.

- **Interface -** controlling the VNA from a computer will not only remove the need for a display on device which will lower cost, but also significantly reduce the embedded compute power required whilst allowing for use of tools such as Python's NumPy and scikit-rf for data processing and VNA calibration, along with Qt and Matplotlib to provide a user interface with a much lower time investment than developing the required functionality from scratch on embedded hardware.

- **Ports -** whilst most modern VNAs allow for all S-parameters of a DUT to be measured, this requires extra hardware for the routing of signals around the board which drives up cost and complexity. Given that the majority of measurements only involve S_{11} and S_{21}, through only measuring these two parameters the complexity and cost of the VNA can be reduced whilst not significantly impeding function of the device. If S_{22}, S_{12}, or a DUT with more than two ports is required to be measured, external connections to the DUT can be altered to allow these measurements to take place.

- **Licencing -** the VNA should be able to be designed, manufactured, programmed, and operated using solely free tools, and where practicable open source tools. This ensures the VNA is able to be operated without any expenses other than the cost of hardware, whilst also ensuring that the hardware, firmware, and software is able to be viewed and modified by anyone without having to purchase proprietary tools, which may be prohibitively expensive and become obsolete, preventing access to the source files used during design.

3 Design

Design of the VNA takes place in two steps: high level architectural design where the functional blocks of the system are determined, followed by detailed design where specific components are chosen to meet the needs of each functional block.

3.1 Architecture

A VNA has four main functional blocks as shown in Figure 1: source for stimulus, signal separation, receiving / detecting, and processing / display. Each of these functional blocks plays a key role in the function of a VNA and will be discussed below.

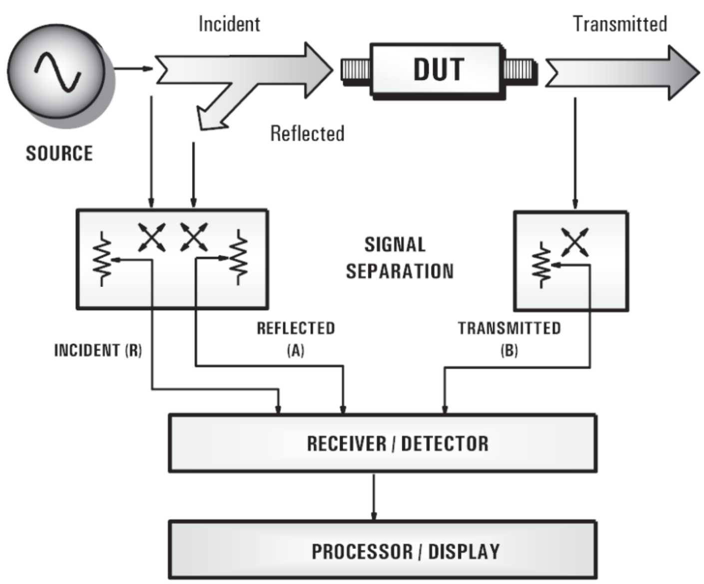

Figure 1: Generalised Network Analyser Block Diagram [5]

3.1.1 Signal Source

The signal source is the first functional block in the signal path of a VNA, and is responsible for providing the stimulus used for the test system. This source is typically swept over frequency, but can also be swept over power to measure the required parameters. Two primary considerations for the signal source are the phase noise of the signal, which can cause issues with narrow bandwidth measurement if it is too large, and the spectral purity of the signal, which can result in incorrect frequency response measurements if there are spurious tones or harmonics in the output spectrum.

Typically the signal sources utilise a voltage controller oscillator, which is able to generate continuous wave signals over a wide bandwidth through the use of a PLL to multiply a reference clock to the required frequency. Single chip solutions are available which contain a PLL and multiple VCOs to enable a wide frequency range with only a few external passives, and whilst these PLLs are easy to implement and control, they typically have increased phase noise, harmonics, and spurs compared to a PLL which uses multiple discrete components to close the loop, which is seen on higher end devices where the quality of the output spectrum is key.

To allow control over the output power level, a power amplifier, programmable attenuator, and power detector can be utilised to provide closed loop control over the output power level. Key features of the source levelling components are that they can provide the required power level over the frequency range being swept, along with not distorting the signal being output by the source.

3.1.2 Signal Separation

Signal separation is the next functional block in the system, and is utilised to measure a portion of the source for analysis in the receiver / detector subsystem. They are used to measure both the power being output by the source, along with the incident and reflected waves at connections to the DUT. The latter two measurements require directional couplers, as both the incident and reflected waves are on the same PCB trace whilst travelling in opposing directions, and as such high directivity is required to ensure that only the signal travelling in the desired direction is being measured.

The three most common methods for coupling signals are resistive dividers, which are broadband but lack directivity and have high loss, directional couplers, which have low loss however their coupling and directivity are limited in bandwidth, and directional bridges, which are broadband, can have high directivity, and have lower loss than restive dividers.

3.1.3 Receiver / Detector

Most vector network analysers utilise a tuned narrowband detector where the RF incident upon the DUT is downconverted to an intermediate frequency, where an ADC samples the signal and digital signal processing is then preformed to determine the gain and phase of the IF signal. This design results in high sensitivity and dynamic range, along with good harmonic and spurious tone rejection, and a significantly lower noise floor than other methods. However due to the high sample rates of the ADC required to meet the Shannon-Nyquist sampling frequency of the signal, this method requires a fast sampling ADC, and the corresponding amount of computing power to preform the signal processing to determine the amplitude and phase of the signal, which is comparatively expensive to other methods.

In scalar network analysers, diode based detectors are often used as they provide a cost effective solution to measuring power. However they are broadband which can result in spurious measurements at unintended frequencies, do not have the sensitivity and dynamic range of a tuned detector, and are only able to measure gain, not phase of a signal. As such they are not suitable for use in a vector network analyser where phase measurements are required.

A third potential receiver utilises the AD8302 from Analog Devices, which is a RF / IF Gain and Phase Detector. [6] The AD8302 contains dual demodulating log amplifiers and a phase detector, which generates two analog voltages which correspond to the gain and phase difference between the input RF signals. This design has the same issues as a diode detector due to utilising diode detectors internally for gain detection, however it resolves the phase measurement issue due to generating phase difference as a second output. There are however some signal processing challenges which need to be overcome with the phase detection, as the output can not differentiate between positive and negative phase, and also has non insignificant log conformance error at small phase differences and higher frequencies. However, given that its cost is between the two other solutions outlined above, it may be a cost effective solution to gain and phase detection if high dynamic range is not required.

3.1.4 Processor / Display

The final functional block in a VNA is the processing and display of the received data, and this is where the raw data measured by the receiver is transformed and displayed in various ways which enable the user to make informed decisions about the measurements being taken.

Depending on the amount of processing required, the compute requirements may vary from multiple custom ASICs for the digital signal processing combined with a Windows install, touch screen, and physical buttons for the application layer, all the way through to a Cortex M0 microcontroller with a small TFT display which handles both the signal processing and display to the user. In recent years, companies such as Tektronix have been rolling out 'headless' devices which utilise the user's computer to handle the application layer, enabling smaller and cheaper test and measurements devices as they no longer require a screen along with the user interface on device.

3.1.5 Chosen Architecture

Taking into account the constraints and specifications in combination with the common architectures outlined above, the desired architecture for the device can be decided so that the scope can be narrowed for detailed design.

- **Signal Source -** a single chip PLL with integrated VCO would be well suited for the VNA, as the benefits from a single chip solution which is cheaper, takes up less board space, and is easier to configure than a PLL made of discrete components far outweighs the loss of performance which will result the single chip solution.
- **Signal Separation -** whilst a directional bridge would be ideal as it has high directivity whilst working over a wide frequency range, the desire for all components to be COTS rules this out, as they are typically designed into the PCB and as such would require extensive simulation and testing, even if a reference design such as the work of of N. Drobotun and P. Mikheev in their paper "A 300khz-13.5ghz directional bridge" [7] was to be implemented. As such a directional coupler will be the best option, with the main limitation being the availability of broadband directional couplers in the desired frequency range.
- **Receiver / Detector -** whilst a tuned narrowband detector would be ideal, the cost of a high sample rate ADC along with a FPGA to do the signal processing would exceed

the desired BOM of the VNA. As such, the AD8302 from Analog Devices will form the receiver as it has sufficient performance characteristics whilst being significantly cheaper than a digital front end.

- **Processor / Display -** given the use of an AD8302 for gain and phase detection, a microcontroller will have sufficient processing power and can be utilised to keep costs low. Furthermore, offloading data processing and visualisation to a host computer will allow for further reduction in cost due to not requiring the extra processing power, display, or user interface controls to be added to the device.

3.2 Detailed Design

With the architecture of the VNA outlined and constraints which influence component selection documented, detailed design of the VNA can begin. The following section outlines key considerations in component choice, low level design details, along with some of the testing and characterisation which was done prior to finalising the first schematic. A block diagram of the system can be found in Figure 2, with the full schematic for the VNA in Appendix A.

3.2.1 LO Generation

The first part of the RF chain begins with the LO, as it generates the signal used throughout the VNA. As outlined in the architecture section, a single chip solution is desired and resulting from research two primary options were found: ADF4351 from Analog Devices, and the MAX2871 from Maxim. The below table summaries their specifications.

Table 1: Comparison of LO generation ICs

	MAX2871	**ADF4351**
Frequency Range MHz	23.5 - 6000	35 - 4400
Fractional / Integer N	Fractional	Fractional
Max Output Power dBm	5	5
Cost ($ at Quantity 1)	17	23
Example Code	No	Yes

As can be seen from Table 1, the MAX2871 has a wider frequency range, whilst having a lower cost and having the same maximum output power and Fractional-N PLL as the AD4351. The only downside of it for our application is that there is no example code provided by Maxim, and this combined with it's poor data sheet may result in extended firmware development time, whereas Analog Devices provides example code along with an extremely well documented data sheet and application notes. Given there is no cost associated with firmware development and that the goal for the device is to have the widest frequency band at the lowest cost possible, the MAX2871 was chosen due to it's superior specifications.

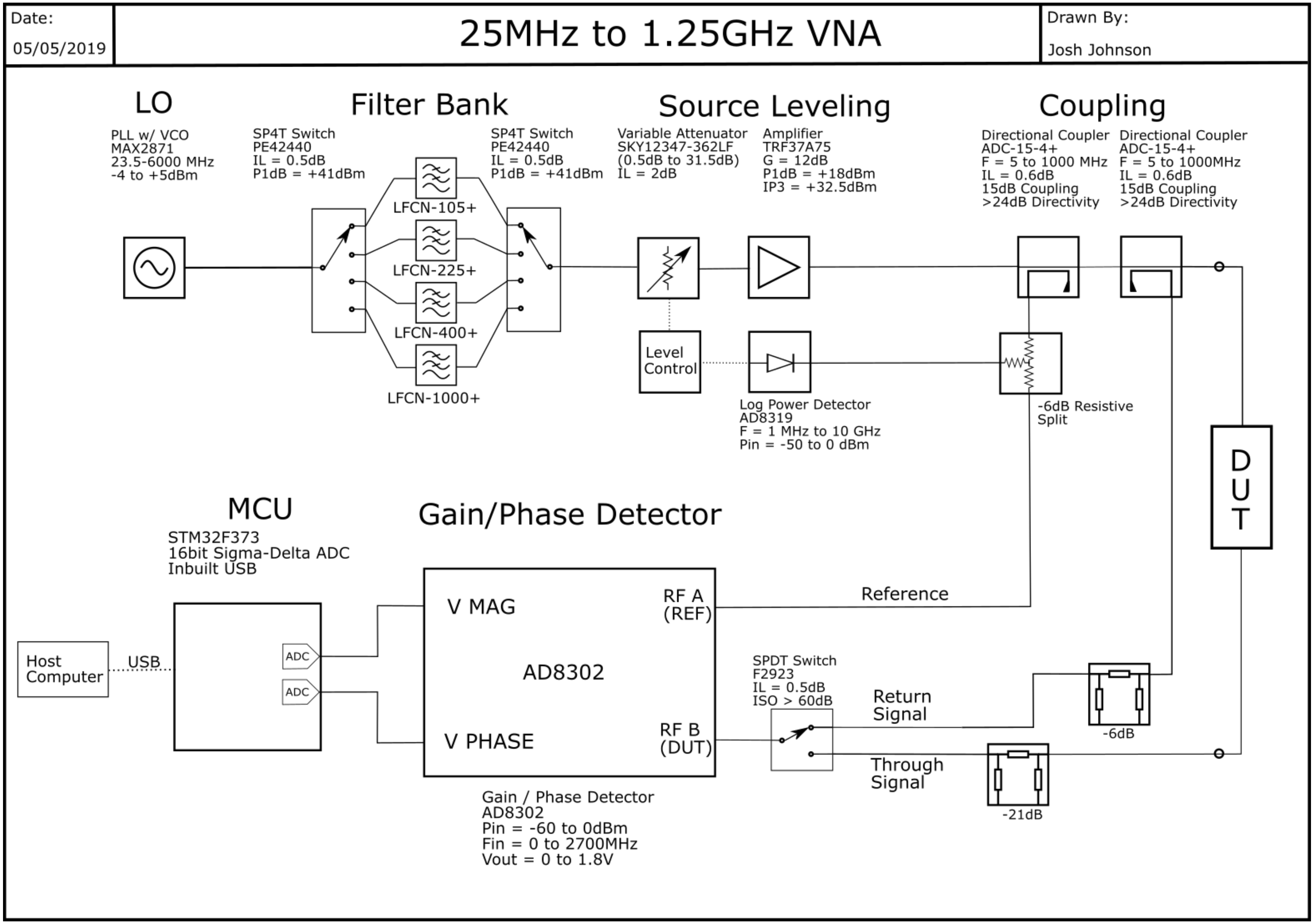

Figure 2: Functional Block Diagram of VNA

3.2.2 LO Filtering

Due to the LO utilising a divided down output for frequencies below 3 GHz, there are significant harmonics in the output signal which need to be filtered out. As will be discussed later, the directional couplers chosen operate up to 1 GHz, and as such filters need to be chosen which operate up to this frequency. Four filters from Mini-Circuits's LFCN series were chosen, with the goal of only frequencies below the second harmonic of a signal being able to pass through, as this would remove most of the unwanted harmonics. In an ideal world this would prevent all harmonics from a fundamental greater than 50 MHz from passing through the RF chain, however due to the roll off of the filter, along with some poor decisions resulting from not paying enough attention to the data sheets and not fully understanding of the importance of an harmonic free output, the filter selection resulted in issues which will be discussed in §4. The chosen filters are tabulated below, along with the frequencies at which 1, 3, and 40 dB of attenuation are measured.

Table 2: Selected Filters

	LFCN-105+	**LFCN-225+**	**LFCN-400+**	**LFCN-1000+**
1 dB IL (MHz)	125	250	410	1100
3 dB IL (MHz)	180	350	560	1300
40 dB IL (MHz)	265	510	680	1800

During the design of the VNA, filters were chosen based off their 1 dB attenuation, as that is the headline figure which Mini-Circuits names their products by. At the time of choosing, the amplitude and number of harmonics in the output were unknown, along with the significance of a harmonic free output. In hindsight, now knowing the importance of harmonics being attenuated by more than the ~ 35 dB of dynamic range of the VNA, filters would be chosen based upon their frequency at with 40 dB of attenuation is measured, as shown by the bottom row of Table 2.

For the filters to be switched in and out of the signal path, two SP4T switches capable of functioning down to 25 MHz were required. The PE42440 from pSemi was chosen due to it's flat insertion loss across the frequency band of interest, along with low price.

3.2.3 LO Levelling

With the hardware described above a signal can be generated over a broad frequency range, however other than the 3 dB steps programmable from the MAX2871, there is no control over the output power. A flat power profile is required as a DUTs performance may vary as a function of power, and as such being able to keep the output power at a constant value is crucial. This is implemented through the use of a programmable attenuator and power amplifier to set a given output power, and a logarithmic power detector and firmware to measure and provide closed loop control over the output power.

With the desired programmable attenuator having a flat insertion loss from 25 MHz to 1 GHz and fine power control, the PE43711 from pSemi was chosen as it allowed for 0.25 dB attenuation steps up to 31.75 dB whilst having a flat frequency response throughout. A HMC313 from Hittite was chosen as the PA, once again due to it's flat frequency response across the operating frequencies. Finally, an AD8319 log power detector was chosen to provide the power sensing, as it's logarithmic output would allow for easy measurement of the logarithmic RF power from an analog pin on the host microcontroller.

A test board was designed with the above components interfacing with an external microcontroller to implement the control algorithm, and through testing was shown to work. However, during testing it was noticed that at power levels above 0 dBm there were significant harmonics in the spectrum, and due to this varying with power it was identified that the issue was non-linearities in the amplifier causing the unwanted tones. As such a new test board based around the TRF37A75 from Texas Instruments was designed, and through testing it was shown that the higher P1dB and IP3 was sufficient for the power levels required for the source levelling block. One downside of the TRF37A75 is that the gain drops off steeply below 40 MHz, however due to the programmable attenuator being situated in series with the PA this can be compensated for by decreasing the attenuation at the lower frequencies. The key differences between the HMC313 and TRF37A75 are highlighted in Table 3.

Table 3: Comparison of Power Amplifiers

	HMC313	**TRF37A75**
Frequency Range (MHz)	DC - 6000	40 - 6000
Gain (dB)	17	12
P1dB (dBm)	14	18
IP3 (dBm)	27	32.5
Current Draw (mA at 5V)	50	80
Cost ($ at Quantity 1)	6	2.5

3.2.4 Directional Couplers

Directional couplers are one of the key components in a VNA, as they set the frequency and dynamic range of the device. A wide frequency range, flat coupling, high directivity, along with low insertion and return loss are all key measurements which play a role in determining the performance of the instrument. Whilst it would have been preferable to design a resistive directional bridge which has superior characteristics for the above parameters, due to the desire for solely COTS products to be utilised the ADC-15-4+ from Mini-Circuits is the best fit, and it's key features are outlined in Table 4.

Table 4: Key Parameters of the ADC-15-4+ Directional Coupler

	ADC-15-4+
Frequency Range (MHz)	5 - 1000
Insertion Loss (dB)	0.4 - 0.8
Coupling (dB)	15
Directivity (dB)	24 - 35
Return Loss (dB)	>25

During qualification of the ADC-15-4+, the directivity was measured out to 2000 MHz and it was noted that whilst it decreased after 1000 MHz, directivity stayed above 24 dB until 1300 MHz, and coupling was also flat out to that frequency. As such the operational range of the coupler can be increased to 5 - 1300 MHz for our use in the VNA.

3.2.5 Gain and Phase Detection

With the AD8302 by Analog Devices being chosen for gain and phase detection, there is little design work do be done due to reference designs being available. However there are a few challenges which need to be overcome to successfully transform it's outputs to gain and phase values, and understanding these will be key to selecting the correct processor to sample and process the information. Figure 3 highlights the Functional Block Diagram of the AD8302 which may assist with understanding the function of the device.

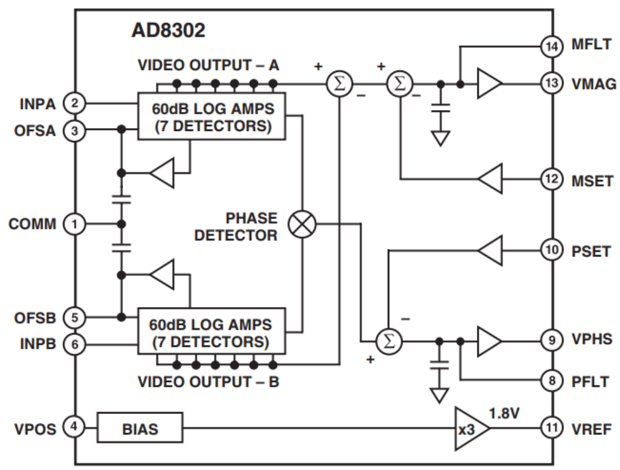

Figure 3: Functional Block Diagram of AD8302

Given RF inputs on INPA and INPB, the AD8302 outputs two analog signals ranging from 0 to 1.8V on VMAG and VPHS which correspond to the gain and phase difference between the two RF signals. However these outputs are not perfect, and as such there are various considerations which need to be taken into account to ensure that the gain and phase differences are represented accurately.

VMAG Log Conformance Error

The VMAG output of the AD8302 shown in Figure 4, which represents the magnitude ratio of the two RF inputs, has decreased linearity towards the ends of its span. Although this could be compensated for through using a non linear model for the voltage to gain conversion, given that the error exceeds 0.5 dB at ±27 dB, which is not only enough dynamic range for many measurements but only 3 dB from the limits of the output, it will not be compensated for due to the limited time available for this project.

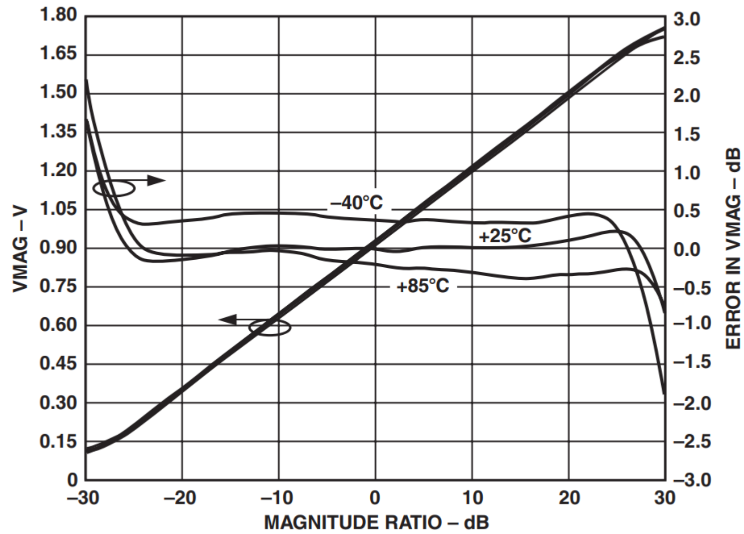

Figure 4: VMAG Log Conformance Error

VPHS Sign Ambiguity

As shown in Figure 5, the output voltage representing the phase difference is unable to differentiate between positive and negative phase, due to the output voltage being symmetrical around zero phase difference. It should however be noted that the gradient between -180 and 0 phase is different to 0 to +180 degrees, and as such by looking at how the phase changes as a function of frequency the sign of phase can be determined. The implementation of the signal processing required to make this determination will be explained in §4.

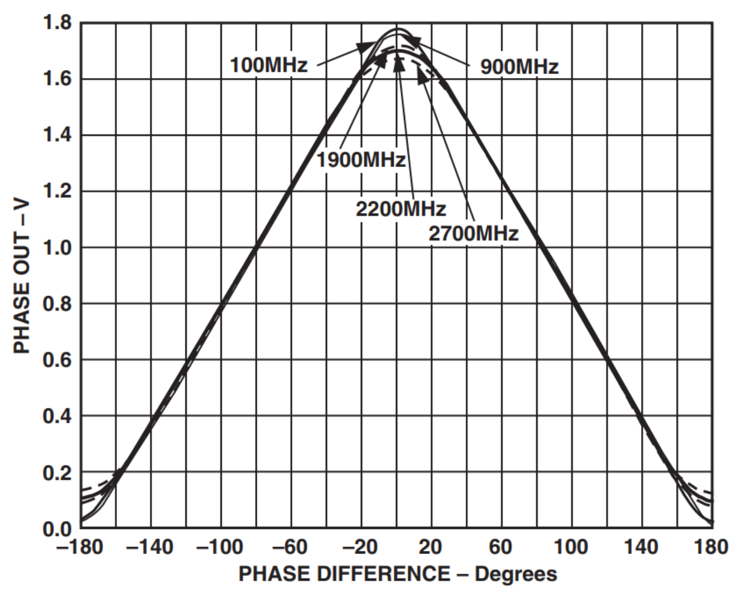

Figure 5: VPHS Output over Frequency and Phase

VPHS Log Conformance Error

Like VMAG, VPHS has log conformance errors at the limits of the internal detectors, which manifest in increased errors when the phase difference is small between the two signals. This is highlighted in Figure 6, which shows the phase error at 900 MHz can be up to 8 degrees when comparing the actual voltage output to the ideal linear fit. Measuring this flattening out of the output voltage and ensuring that the resolution of the sampling ADC is sufficiently high that it can detect the difference at low phase difference values is crucial, as this would allow reconstruction of the actual phase output with sufficient signal processing, which will be outlined in §4.

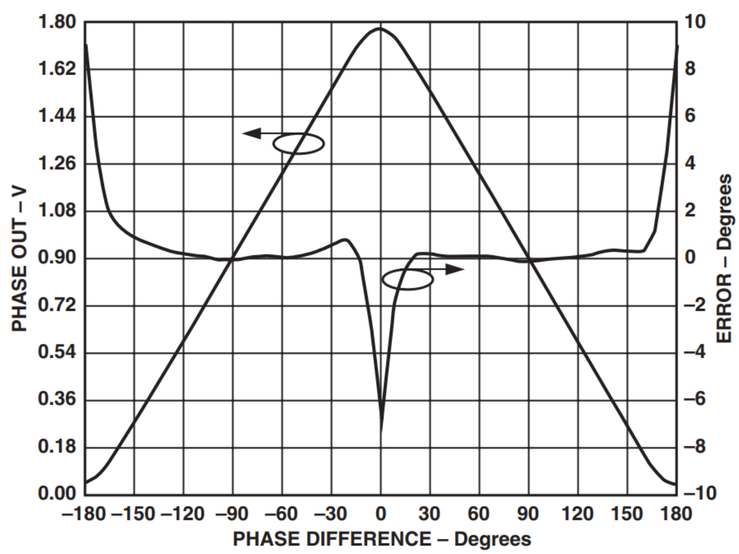

Figure 6: VPHS Log Conformance Error at 900 MHz

VPHS Frequency Dependence

It should also be noted that as shown in Figure 5, the log conformance error increases as a function of frequency. This will need to be compensated for in addition to the error increasing at small phase differences, and this will be covered in §4.

3.2.6 Processor

Sampling of the ADC, control of all onboard devices, along with communications with the host machine will require an embedded processor. As such, a microcontroller with sufficient pins and peripherals to connect to all required hardware, along with inbuilt USB and DSP instructions would be ideally suited to the task. Furthermore, an integrated ADC with at least 12 bits would be ideal, as this would ensure that sampling of the AD8302 could be done with the accuracy required. The STM32F373 series from STMicroelectronics is a great fit for this, as the line-up has 16 bit sigma-delta ADCs with programmable gain, a Cortex-M4 core which has DSP instructions capable of floating point add, multiply, and subtraction in a single clock, along with 64 to 256 Kbytes of flash, and packages with between 48 and 100 pins which will allow the hardware to scale once final specifications and code size are determined.

3.3 Firmware and Software

4 Implementation and Assembly

5 Calibration and Testing

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A VNA Design Files

All files used in the design of the VNA can be found at https://github.com/joshajohnson/vna. Some of the files, such as the schematic, images of the PCB, and functional block diagrams are included either in the body of this thesis, or in the following pages.

Schematics for the test boards, ECal unit, along with the code written for the VNA is not included in the thesis, as there are numerous schematics and thousands of lines of code and as such appending them would not be reasonable. The below dot points link through to the GitHub repository where the files can be found if desired.

Hardware

- Hardware Folder
  - KiCad Design Files for VNA
  - VNA Gerbers
  - Renders and Screenshots of PCBA
  - Functional Block Evaluation Boards
  - ECal Hardware Design

Firmware

- Firmware Files for VNA
  - MAX2871 Programming
  - MAX2871 Register Configuration
  - Transmit Chain Control
  - AD8302 Measurement and Initial Phase Correction
  - Command Parsing and VNA Control
- Firmware Targeting Development Boards

Software

- Software Folder
  - VNA Control Software
  - Phase Correction Jupyter Notebook
  - Calibration Jupyter Notebook
  - Python Implementation of PLL Configuration

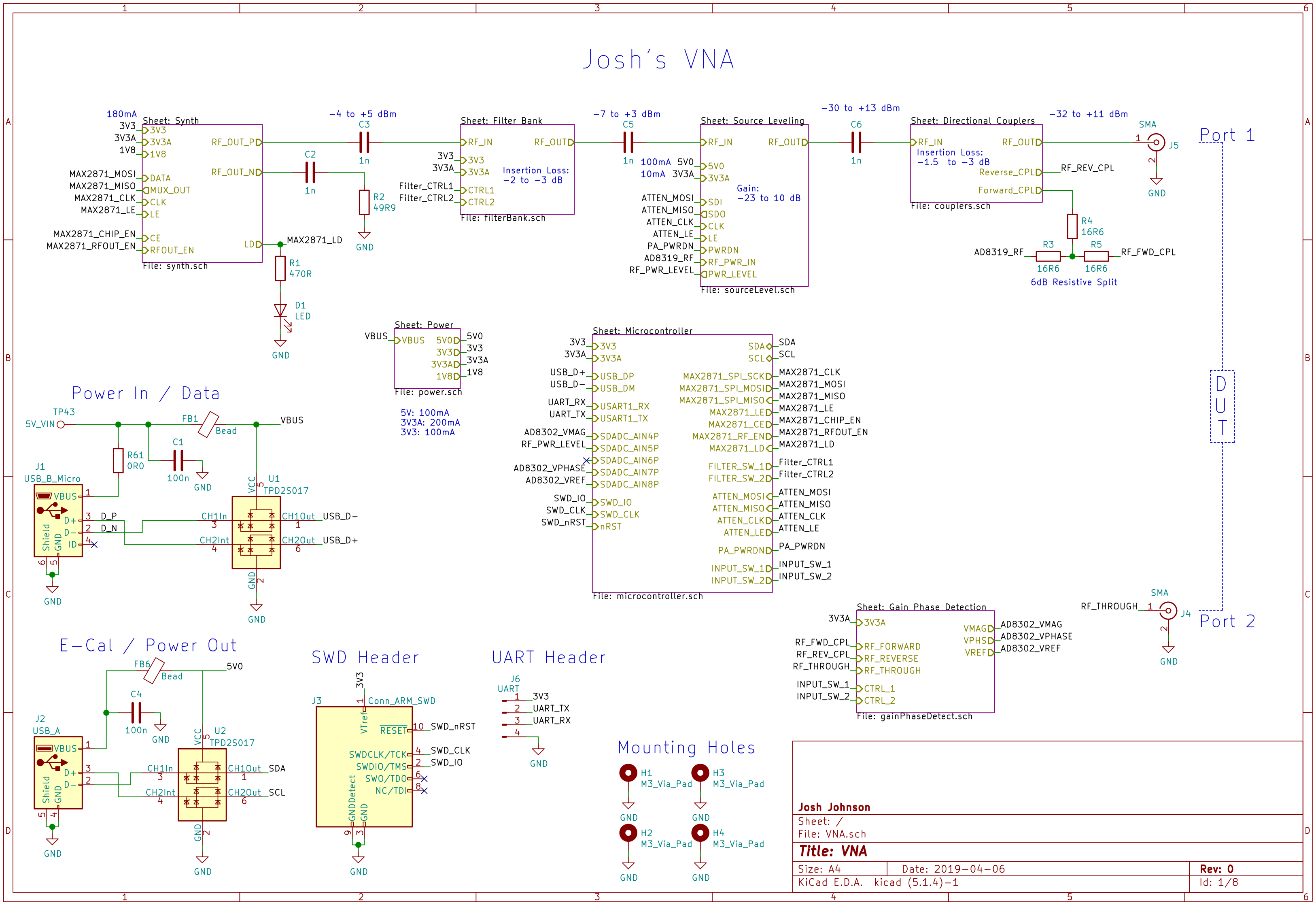

Figure 7: VNA Schematic - Overview

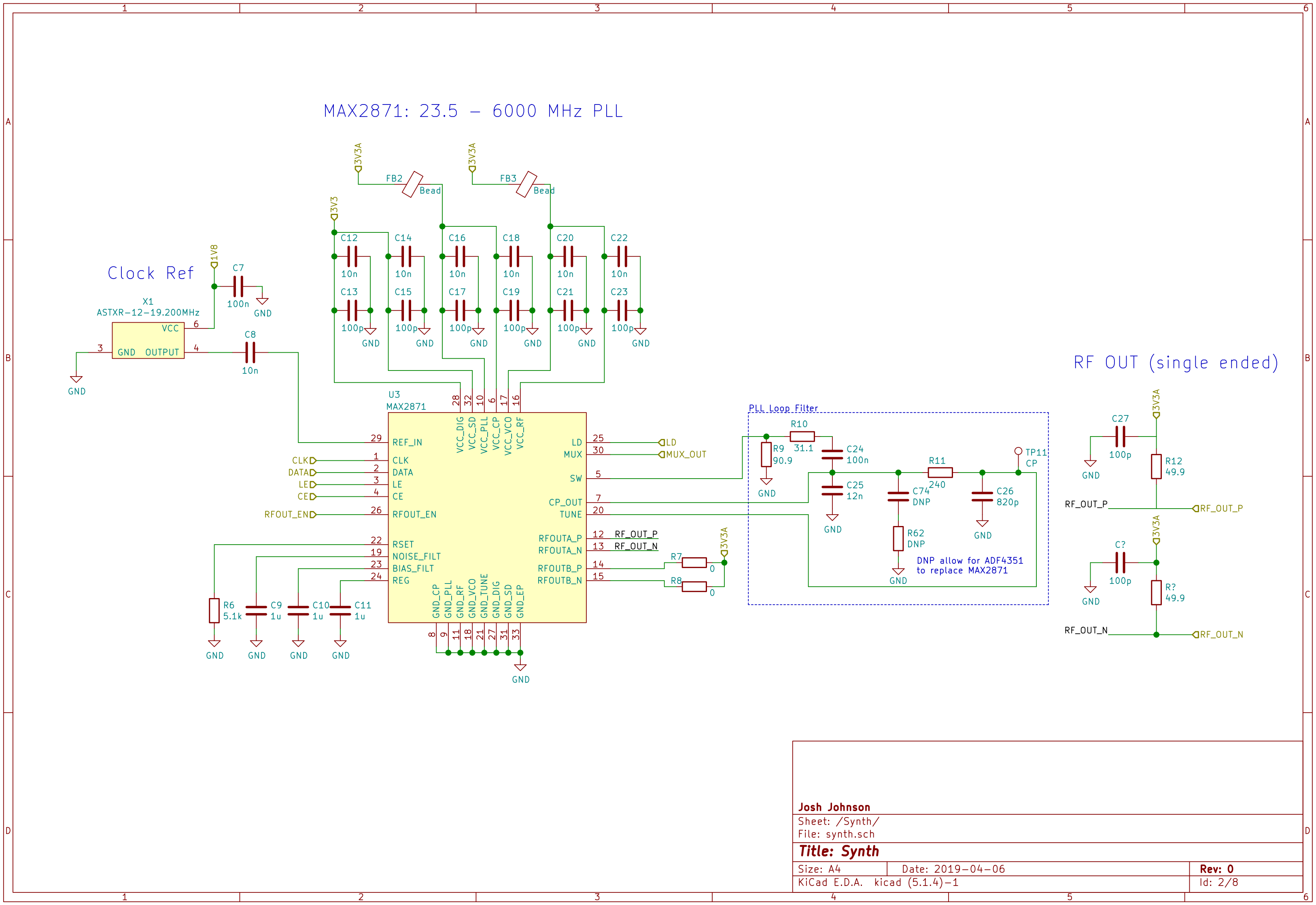

Figure 8: VNA Schematic - LO Generation

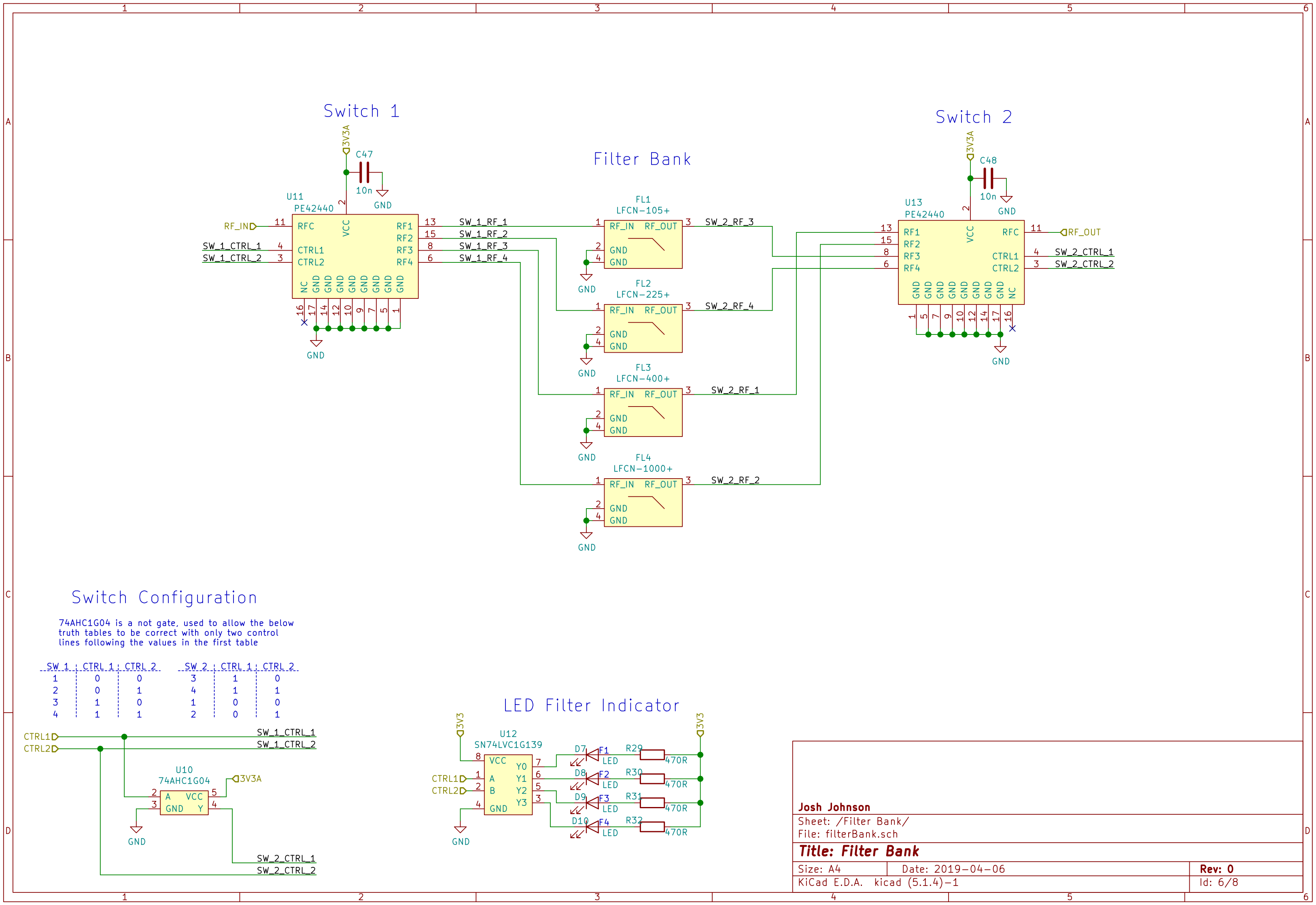

Figure 9: VNA Schematic - Filter Bank

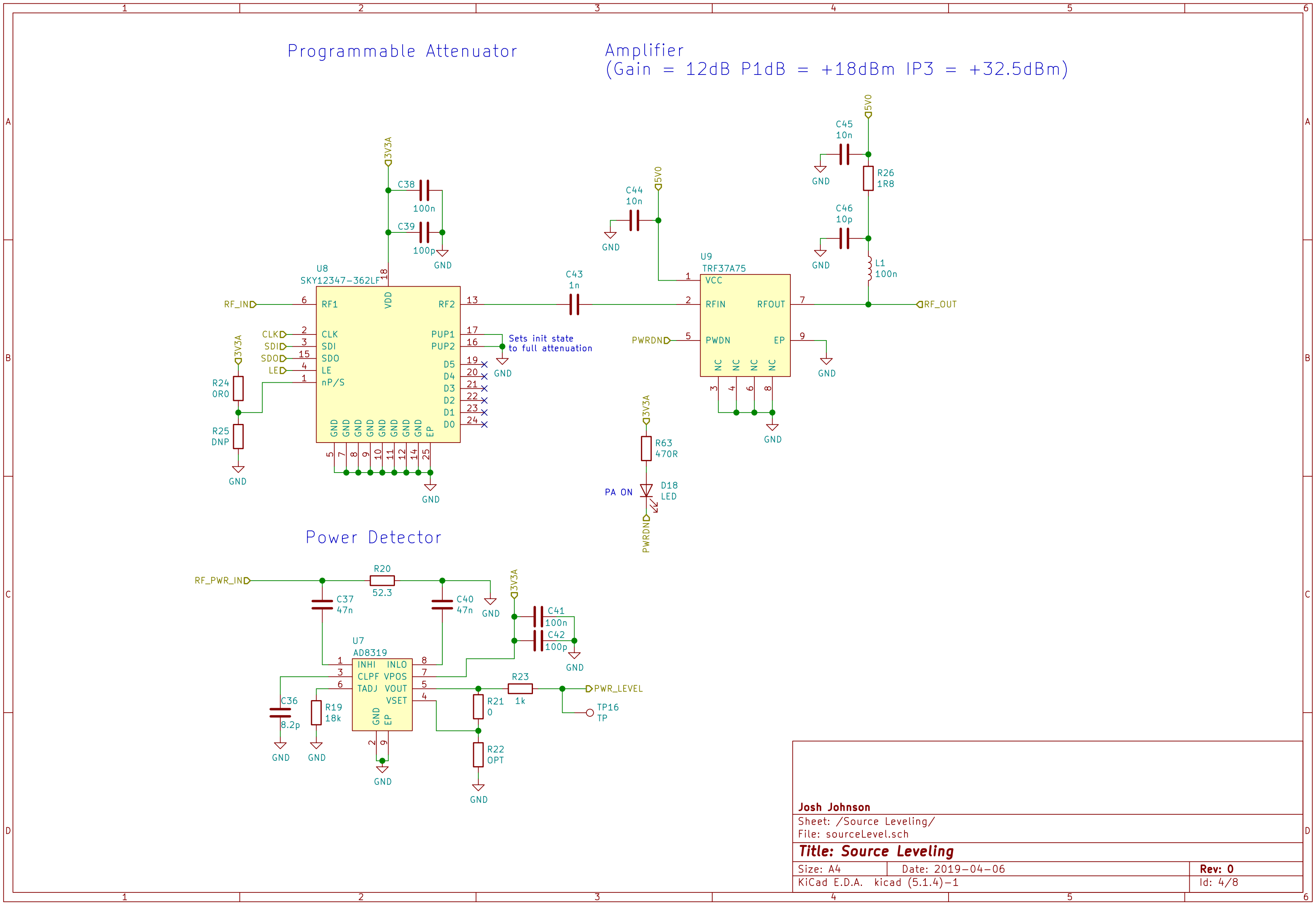

Figure 10: VNA Schematic - Source Levelling

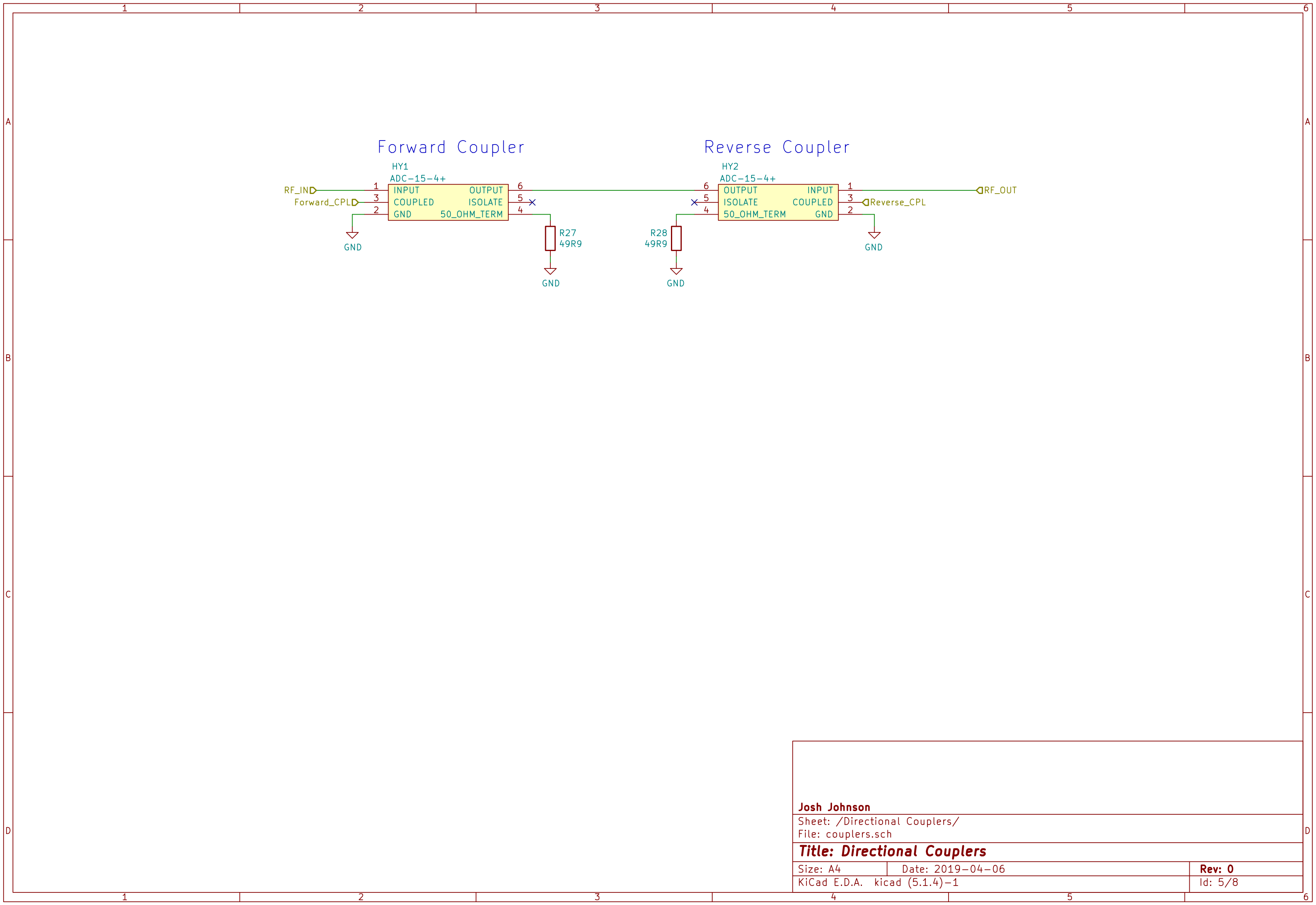

Figure 11: VNA Schematic - Coupling

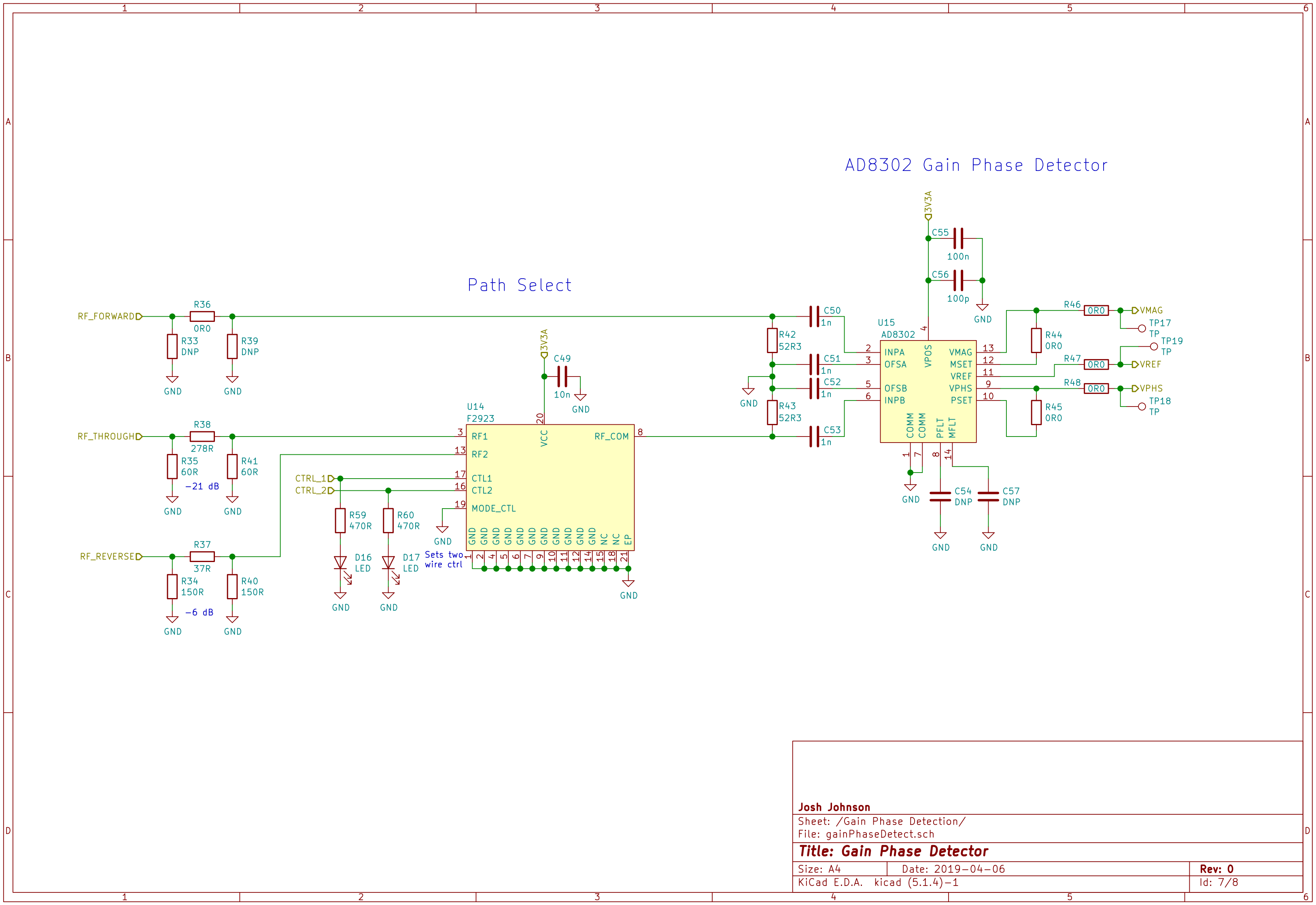

Figure 12: VNA Schematic - Gain and Phase Detection

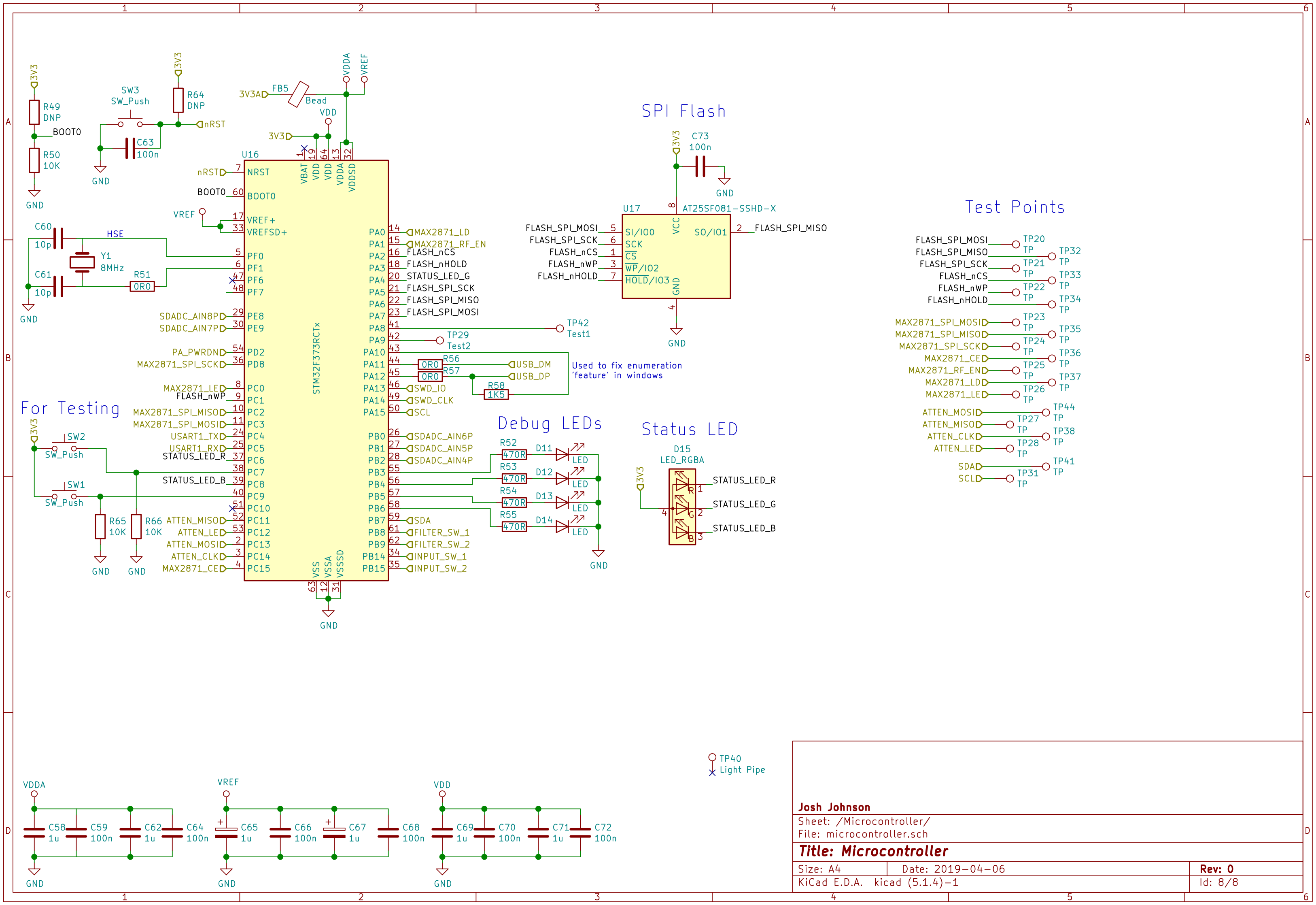

Figure 13: VNA Schematic - Microcontroller

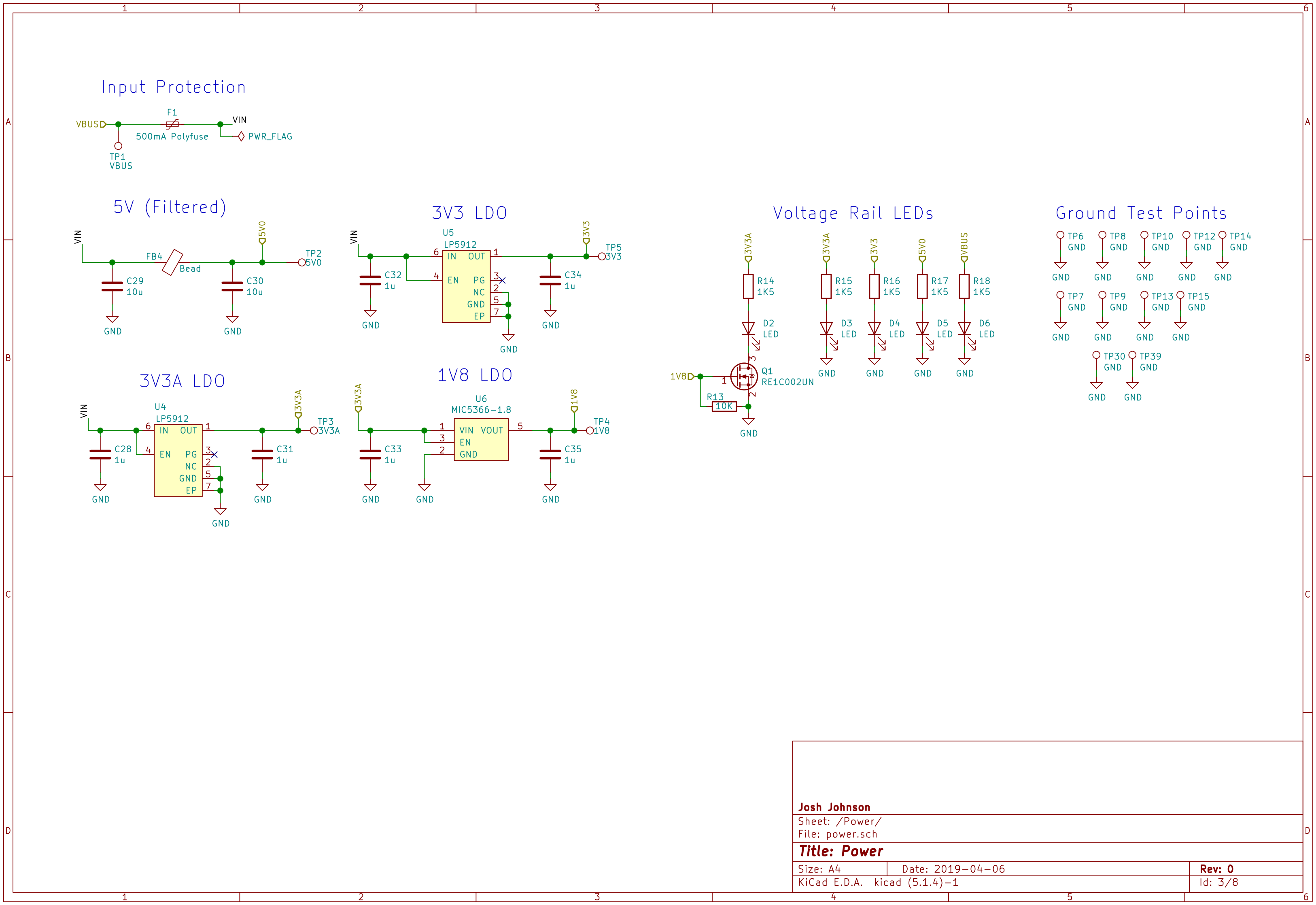

Figure 14: VNA Schematic - Power