

Integrated Load Switches versus Discrete MOSFETs

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Drivers and Load Switches

ABSTRACT

The most common approach to load switching solutions is to use a Power MOSFET surrounded by discrete resistors and capacitors; however, in most cases using a fully integrated load switch has significant advantages. While both discrete and integrated load switching solutions perform the same basic function (turn on and turn off), distinctions exist, such as the transient behavior and total solution size. This application report highlights many drawbacks and limitations of a discrete switching solution and discusses how they can be overcome with an integrated load switch.

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1 Summary of Load Switching

A typical system involves a power supply and multiple loads which require various load currents. In most cases, the system must independently control which loads are on, when they are turned on, and how quickly they turn on. As previously mentioned, this power switching, as [Figure 1](#) shows, can be implemented using a discrete MOSFET circuit or an integrated load switch.

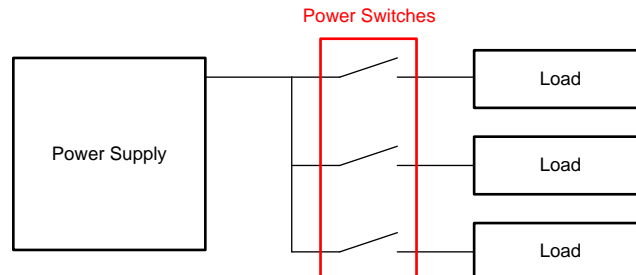


Figure 1. Power Switching

A discrete MOSFET circuit contains several components to control the turnon and turnoff of a discrete power MOSFET. These circuits can be enabled or disabled by using a GPIO signal from a microcontroller. [Figure 2](#) shows several of these circuits.

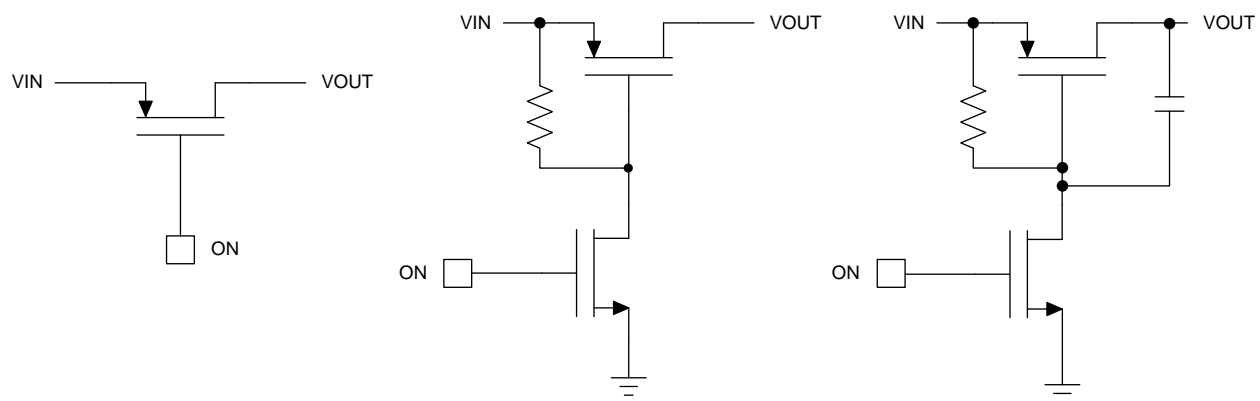


Figure 2. PMOS Discrete Circuits

Load switches can also be used to open and close the connection between the power rail and the corresponding load. These integrated devices have several benefits and features while they are enabled, disabled, or even switching between the two states. [Figure 3](#) shows a load switch circuit.

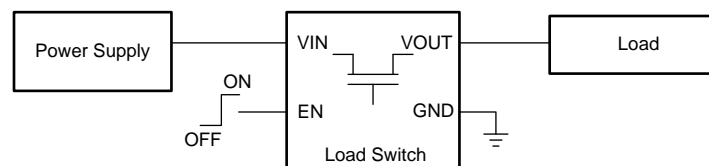


Figure 3. Load Switch Circuit

The following sections use switching waveforms to show and compare the discrete circuits and integrated load switches when used for power switching.

2 PMOS Discrete Circuit #1

The simplest discrete circuit that can be used for power switching is a PMOS transistor whose gate is driven by a GPIO.

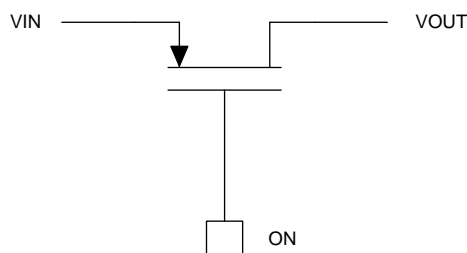


Figure 4. PMOS Discrete Circuit #1

The benefit of this solution is simplicity. Only one component is required and the operation is simple—when the GPIO is high the PMOS is turned off, and when the GPIO is pulled low the PMOS is turned on.

2.1 Performance

The performance of the PMOS solution is evaluated by looking at the way the PMOS transistor is able to switch on with a load attached. For the purpose of this application report, a resistive load of 1 Ω and capacitive load of 4.7 μF are used. Figure 5 shows this type of circuit.

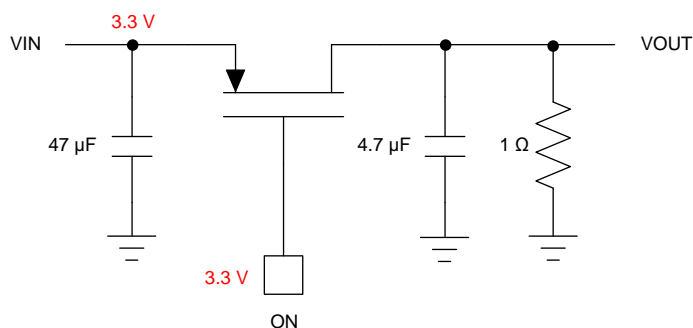


Figure 5. PMOS Discrete Circuit #1 with a Resistive and Capacitive Load

The input capacitance was chosen to be 10 times higher than the output capacitance to show a solution with strong compensation for transient currents seen during start up. Figure 6 shows the typical turn on behavior of this circuit.

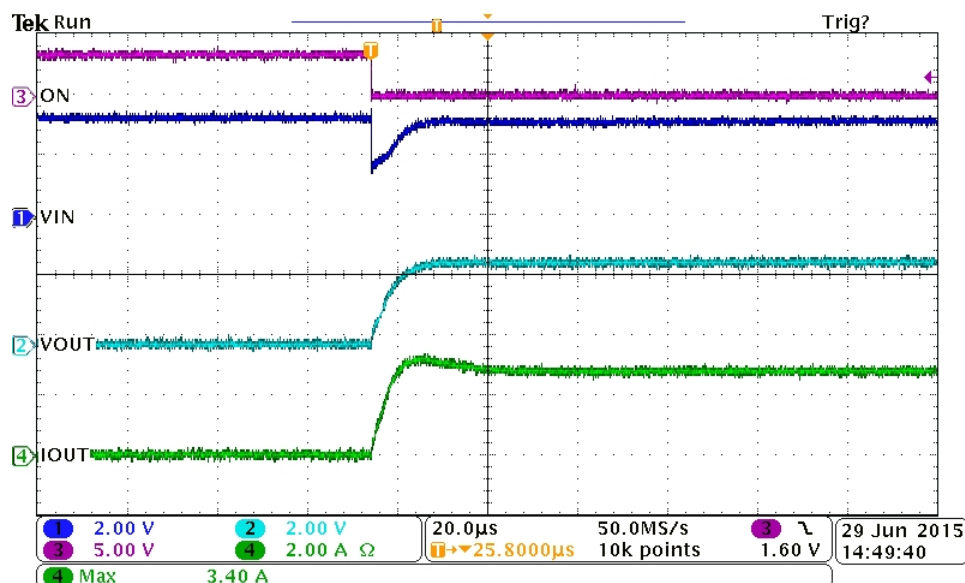


Figure 6. Turn on Behavior for PMOS Discrete Circuit #1

When the GPIO signal (ON) is brought low, the PMOS transistor is turned on and its load is connected to the power supply (VIN). Because the PMOS has no controlled turn on, the voltage on the power supply decreases heavily due to the sudden demand for current. As the current ramps up to its final value, the voltage on VIN stabilizes. Figure 7 shows the stabilizing behavior of the PMOS Discrete circuit.

The resistive load is removed and the capacitive load is left on the output when observing the magnitude of the inrush current.

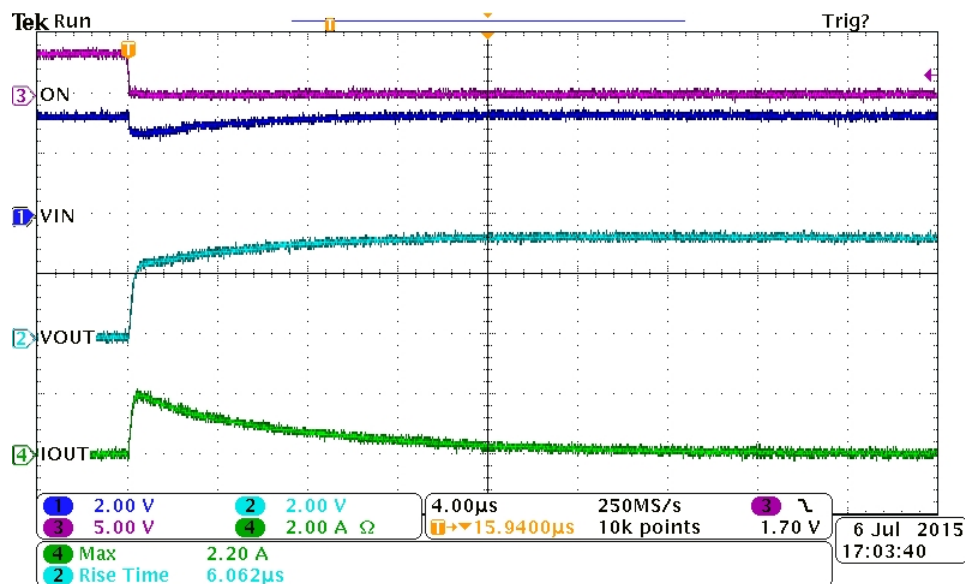


Figure 7. Inrush Current for PMOS Discrete Circuit #1

With only a small capacitance of 4.7 µF, the uncontrolled turnon manages to generate over 2 A of inrush current. As the output capacitance increases, the inrush current also increases at the same rate. Use Equation 1 to calculate inrush current.

$$I_{\text{INRUSH}} = C_{\text{LOAD}} \times \frac{dV}{dt}$$

where

- I_{INRUSH} = amount of inrush current caused by a capacitance
- C_{LOAD} = total capacitance
- dV = change in voltage during ramp up
- dt = rise time (during voltage ramp up)

(1)

This current could lead to input voltage decreases, power supply failure, or PCB trace damage. If the input voltage at the load switch becomes lower than expected, such as in the case of the MOSFET startup, then other modules or subsystems on the same power rail may reset because of a low input voltage and which transitions the system into an undesired state. For more information on the negative effects of inrush current, see the [Managing Inrush Current](http://www.ti.com/loadswitch) application note found at www.ti.com/loadswitch.

2.2 Adding a Resistor to Slow the Output Rise Time

A resistor is added to the gate of the PMOS to help slow down the rise time of the output voltage (and reduce the inrush current). This additional resistor will limit the amount of current that charges or discharges the gate and turns the PMOS off or on.

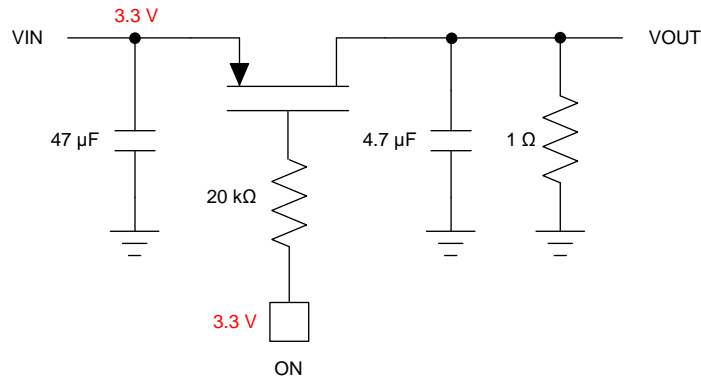


Figure 8. PMOS Discrete Circuit #1 with a 20-kΩ Resistor on the PMOS Gate

Figure 9 shows the effect of a 20-kΩ resistor on the gate of the PMOS.

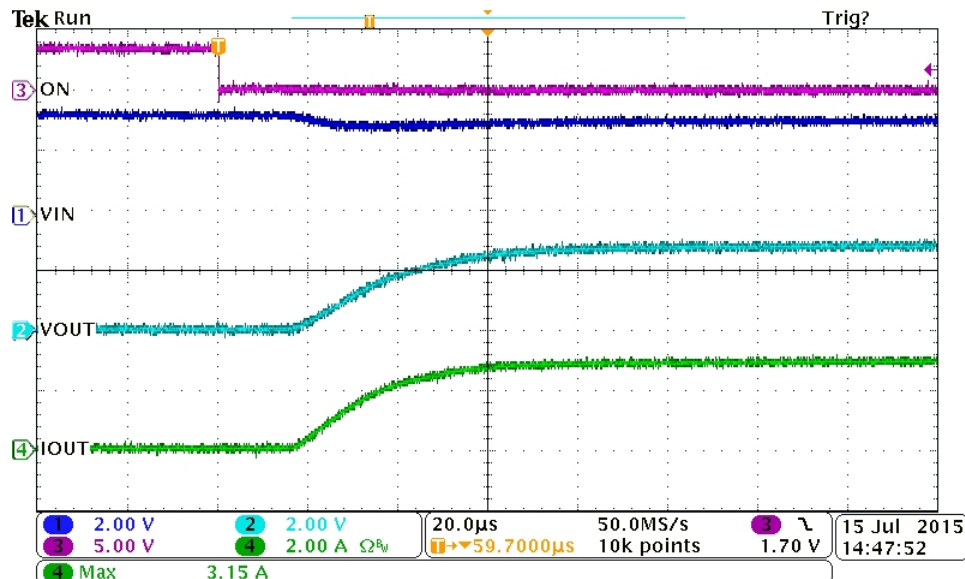


Figure 9. Turnon Behavior of PMOS Discrete Circuit #1 with a 20-kΩ Resistor on the PMOS Gate

With the 20-k Ω resistor added, the rise time increases. The power supply is now able to manage the inrush current without any significant voltage drop. While this resistance may work for the 4.7- μ F load, a higher output capacitance would require a higher rise time and therefore more resistance on the gate.

While adding resistance to the gate of the PMOS helps in increasing the rise time of the output, it also increases the fall time when the PMOS is turned off. **This** can be a disadvantage for systems which need the output load discharged quickly for faster system operation.

2.3 V_{th} Voltage Disadvantage

Aside from the decreasing voltage on the input power rail, this circuit has a few additional disadvantages. One disadvantage is the restriction on the input voltage range of the circuit. This is limited by the V_{th} turn on threshold of the MOSFET. The maximum input voltage which can be applied to the MOSFET is the V_{OH} voltage of the GPIO added to the V_{th} voltage of the MOSFET. If the voltage is any higher than this, then the PMOS will stay on even when the GPIO toggles high.

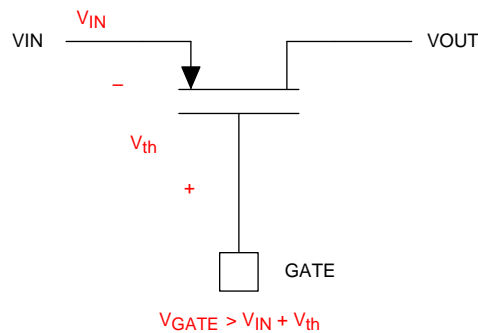


Figure 10. VIN and GPIO Voltage Requirements for PMOS Discrete Circuit #1

The minimum input voltage that can be applied to the PMOS is determined by the desired MOSFET performance. In general, a higher V_{GS} voltage will yield a lower on-resistance across the PMOS and cause less of a voltage drop from V_{IN} to V_{OUT} . While this is desired, it is difficult to implement in this circuit with a low V_{IN} voltage because the GPIO cannot be pulled any lower than 0 V and the V_{GS} voltage will be the value of V_{IN} . Additionally, many times the GPIO voltage will be higher than 0 V because of GPIO variance and the inability to pull the pin all the way down to 0V, resulting in a higher on-resistance and more voltage drop across the PMOS.

2.4 Active Low Disadvantage

Another disadvantage is that the GPIO signal from the microprocessor must always be present to prevent the PMOS from turning on. This means that the microprocessor cannot be powered off or put to sleep to save power for the rest of the system. Also, if the input of the MOSFET comes up before the microprocessor has had a chance to power up and pull its GPIO control high, then the MOSFET circuit will allow power to pass through, even if this behavior is not desired. If the discrete circuit is being controlled by a power good signal instead, then this signal must be active low.

3 PMOS Discrete Circuit #2

The next circuit which will be investigated involves an additional resistor and NMOS transistor.

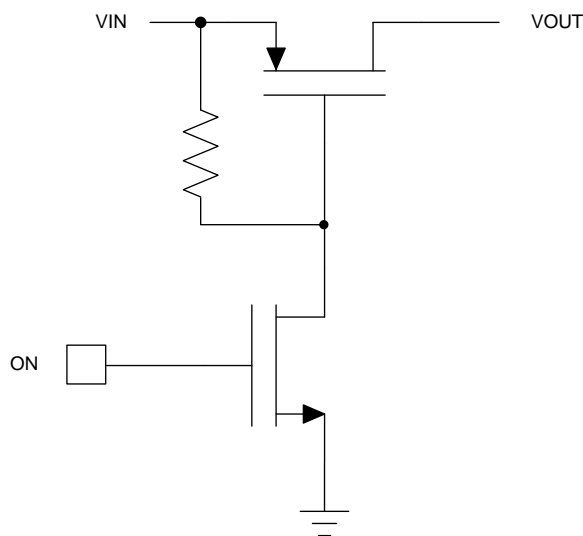


Figure 11. PMOS Discrete Circuit #2

With this circuit, the GPIO pulls the gate of the NMOS high and connects the gate of the PMOS transistor to ground. This turns on the PMOS and allows power to flow from VIN to VOUT. When the GPIO signal pulls the gate of the NMOS low, V_{IN} pulls the gate of the PMOS high and prevents power from flowing through the MOSFET. Rather than using an NMOS transistor to drive the PMOS, an NPN BJT can also be used.

3.1 Performance

Once again, performance is evaluated by observing the switching characteristics of the circuit. Figure 12 shows how this circuit is evaluated with the same input and output conditions as the first discrete solution.

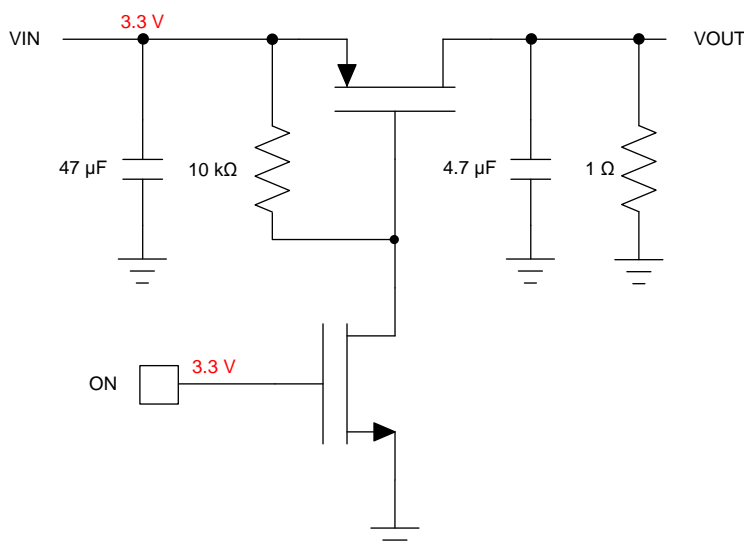


Figure 12. PMOS Discrete Circuit #2 with a Resistive and Capacitive Load

Figure 13 shows the turn on performance of this circuit.

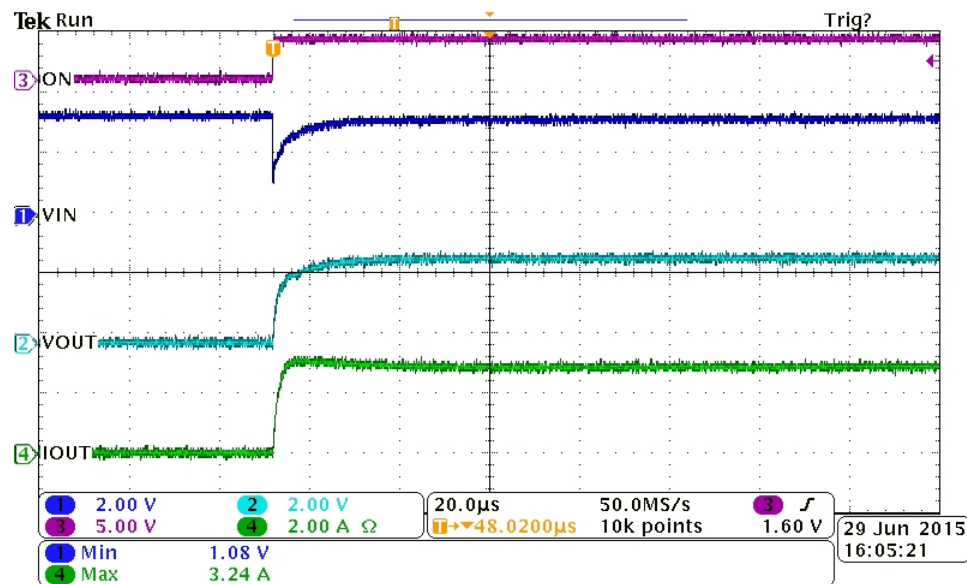


Figure 13. Turn on Behavior for PMOS Discrete Circuit #2

Although the voltage on VIN drops in the same way as the first circuit, this drop does not last as long and is less severe. The inrush current can be observed in Figure 14.

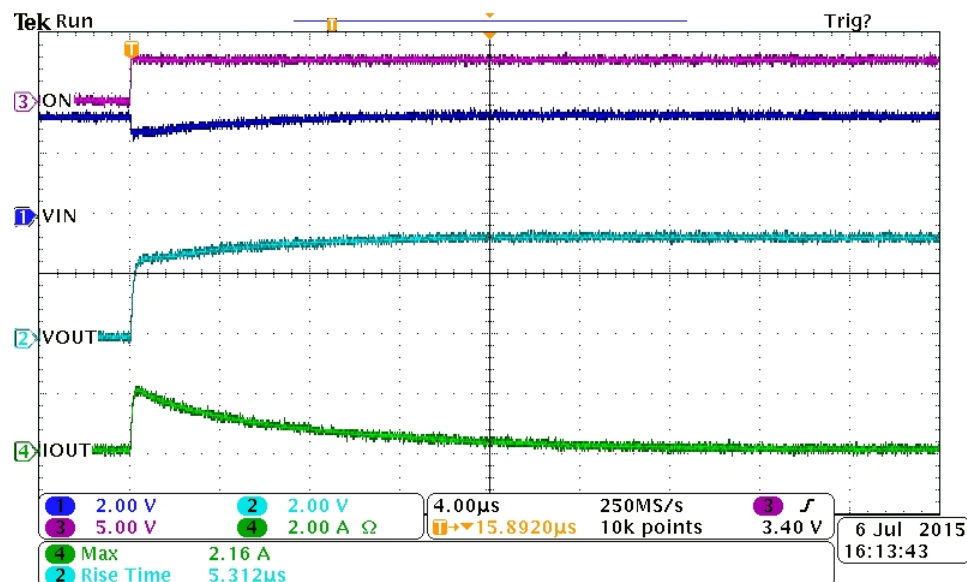


Figure 14. Inrush Current for PMOS Discrete Circuit #2

Once again, over 2 A of inrush current is measured on turn on.

Overall, this circuit solves several problems that the first circuit had. Because an NMOS transistor is being driven, the logic is active high and does not require a constant GPIO voltage to prevent power from passing through to the load. The maximum bound on the VIN voltage is also removed since the gate of the PMOS is coupled to VIN when the PMOS is turned off instead of the GPIO voltage. This circuit also improves the on-resistance performance of the PMOS because the variance in the GPIO signal voltage no longer affects the gate of the PMOS. However, for low values of V_{IN} , the V_{GS} of the circuit would still be small during turn on and would lead to a large on-resistance and voltage drop across the PMOS.

3.2 VIN Leakage Disadvantage

One disadvantage with this circuit is a VIN leakage path that is present when the PMOS is turned on. Because the NMOS is enabled, current is able to flow from VIN, through the resistance from source to gate, and down to ground.

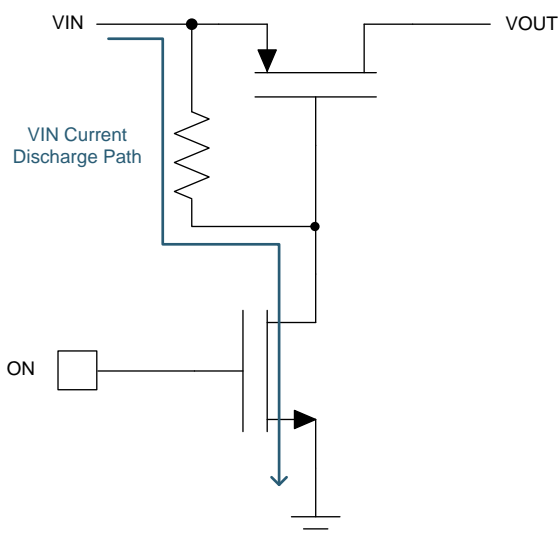


Figure 15. PMOS Discrete Circuit #2 VIN Leakage Path

Leakage is an issue for power conscious designs because it reduces the efficiency of the switch solution and adds additional power dissipation to the rest of the system.

3.3 Adding a Resistor to Slow the Output Rise Time

Once again, a 20-k Ω resistor is added to the gate of the PMOS to slow down the charge of the gate and increase the rise time of the output. Figure 16 shows the 20-k Ω resistor when applied to the PMOS discrete circuit.

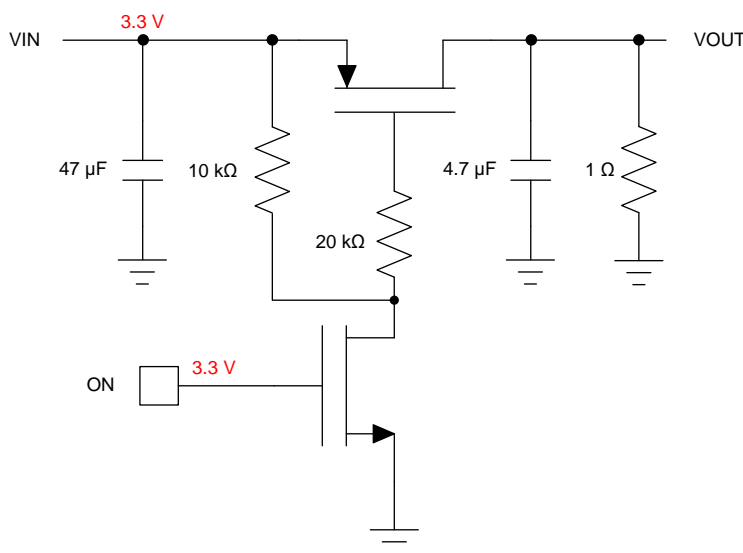


Figure 16. PMOS Discrete Circuit #2 with a 20-k Ω Resistance on the PMOS Gate

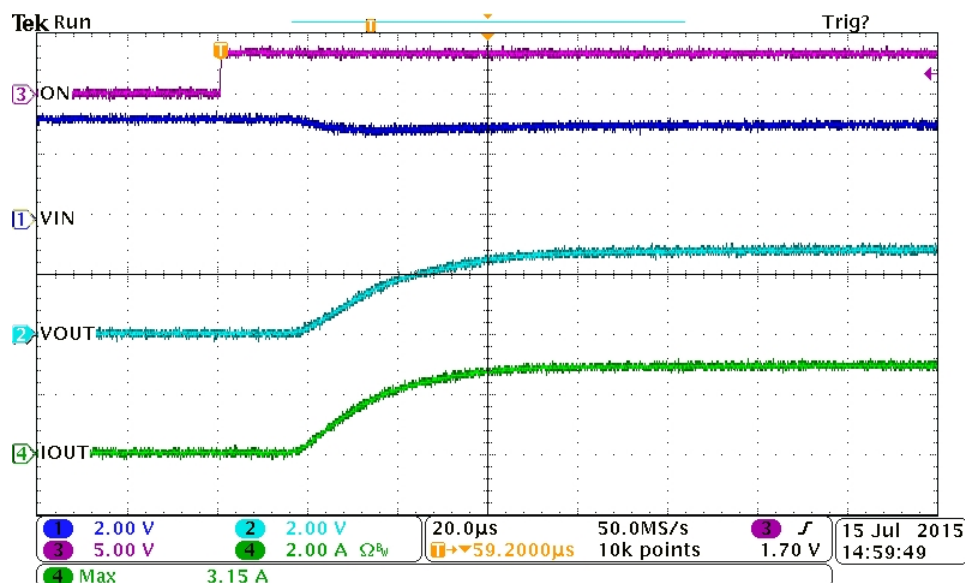


Figure 17. Turn on Behavior of PMOS Discrete Circuit #2 with a 20-k Ω Resistance on the PMOS Gate

With the 20-k Ω resistance added, the rise time is increased and the power supply is able to manage the inrush current without any significant voltage dip. Again, a higher output capacitance would require more resistance on the gate to slow the rise time of the output. As with circuit #1, the slower rise time also leads to a slower fall time which may not be desirable for the system.

4 PMOS Discrete Circuit #3

Despite all of the improvements the second discrete circuit made over the first, the power supply still suffers from a decrease in voltage when there is no resistance present on the gate of the PMOS. The decrease is because of the quick turn on of the PMOS transistor and the inrush current which is generated by the load capacitance. An additional capacitor can be added to help control the turnon.

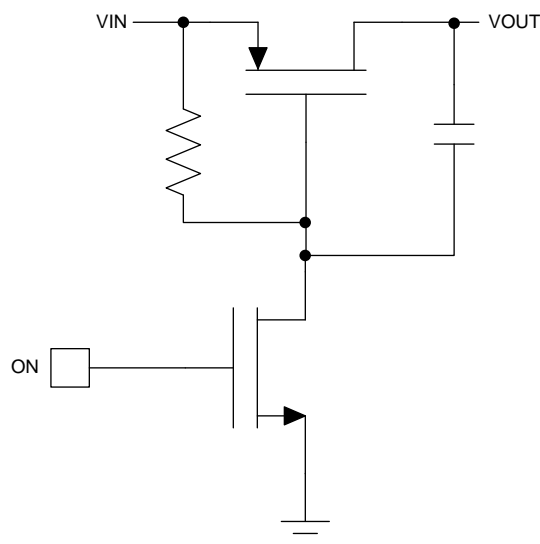


Figure 18. PMOS Discrete Circuit #3

The additional capacitor slows the discharge of the PMOS gate and provides a controlled rise time on VOUT that limits the inrush current and helps prevent changes in the input voltage during switching. Again, a BJT can be used in place of the NMOS transistor.

4.1 Performance

For evaluation, the following input and output conditions were used.

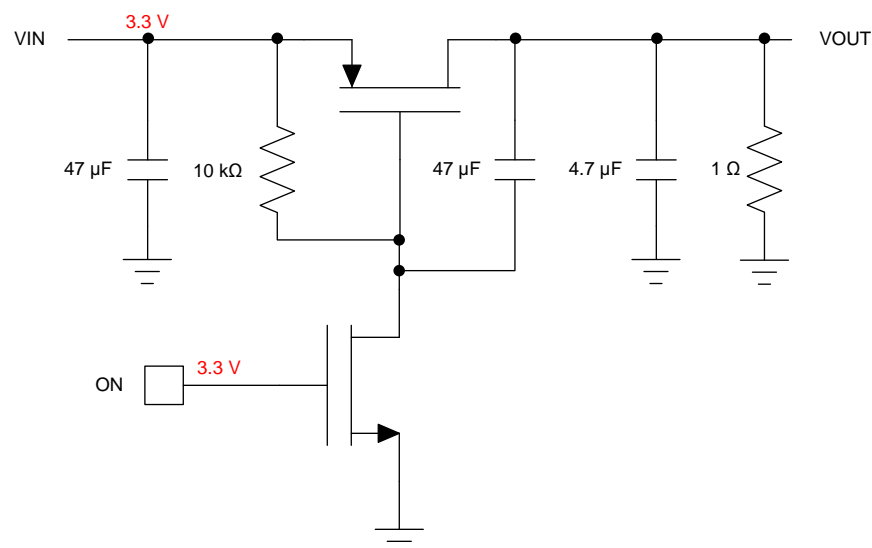


Figure 19. PMOS Discrete Circuit #3 with a Resistive and Capacitive Load

Figure 20 shows the turn on behavior of the discrete solution.

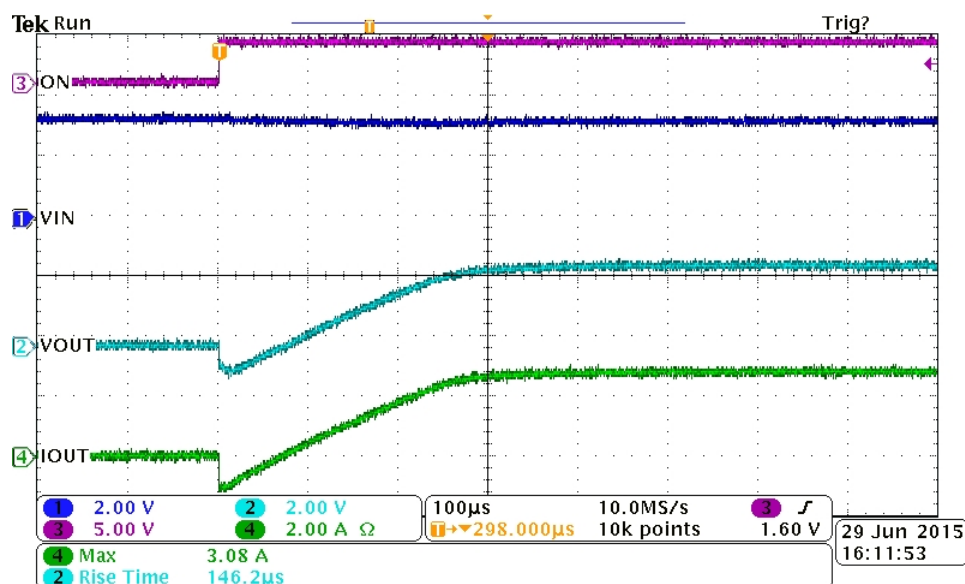


Figure 20. Turn on Behavior for PMOS Discrete Circuit #3

In contrast to the first and second circuits, the PMOS discrete circuit does not suffer from a VIN voltage dip and can control the amount of inrush current generated by the load. The downside here is the negative voltage and current decrease seen at the output.

When VIN is applied to the circuit and ON is low, the capacitor between the gate and drain of the PMOS becomes charged to the value of VIN. When ON goes high and the circuit is turned on, the gate of the PMOS is pulled down from VIN to ground. Because the voltage across the capacitor cannot change instantaneously, the voltage on the output of the PMOS is also pulled down, which results in a negative voltage on VOUT. Once the gate of the PMOS has been discharged, the output voltage is able to ramp up to the value of VIN.

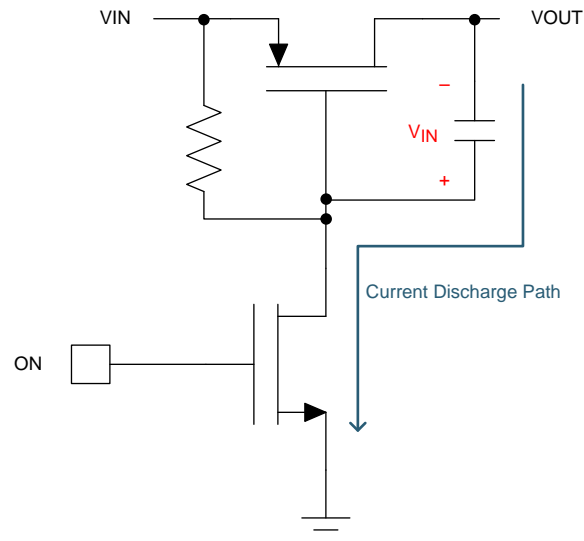


Figure 21. Negative Voltage and Current on PMOS Discrete Circuit #3

A smaller capacitance will lead to smaller negative currents and voltages, but it will also decrease the ability of the circuit to handle inrush current by reducing its rise time. The negative voltage could not only damage the devices downstream of the load switch, but could also lead to latch up and ESD issues for the components in the system.

As with circuit #2, this circuit also has a discharge path from VIN to ground that causes current to leak from VIN when the PMOS is turned on.

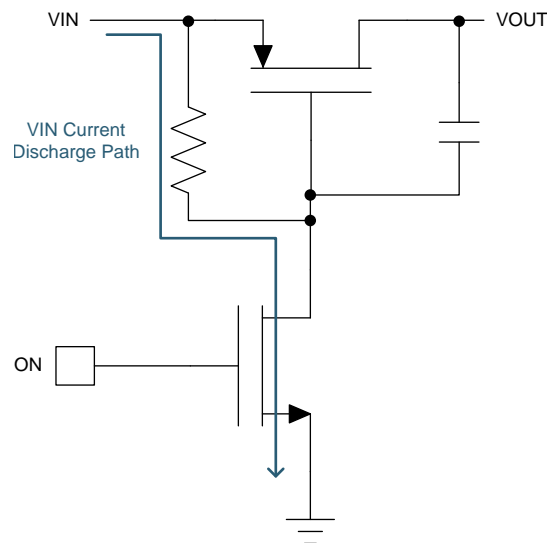


Figure 22. PMOS Discrete Circuit #3 VIN Leakage Path

4.2 Disadvantage when Applying V_{IN}

Another unique disadvantage to this circuit is the behavior when V_{IN} is first applied to the circuit. Before V_{IN} is present, the gate of the PMOS will be a high impedance node.

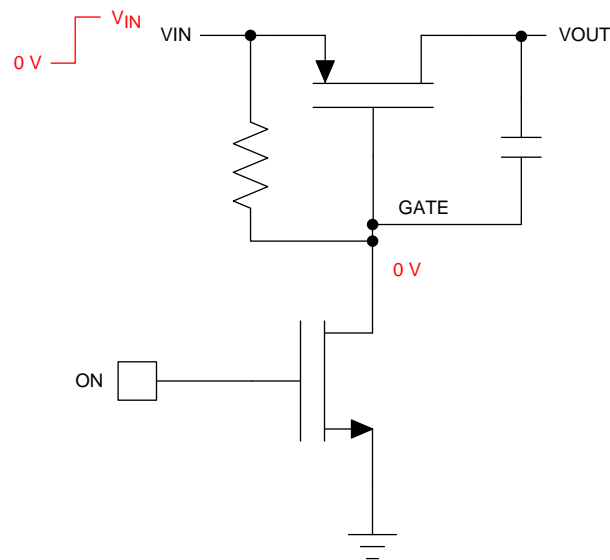


Figure 23. VIN Voltage step causes VOUT Voltage before PMOS gate can charge to VIN

The moment VIN is applied, a negative V_{GS} immediately appears across the PMOS causing it to turn on even when the GPIO control signal is low. As the bulk gate capacitance slowly charges up to VIN, the switch will eventually turn off. Once the gate is charged, the GPIO control signal can be used normally to turn the switch on and off with inrush current control. However, when VIN is first applied, the PMOS will turn on without inrush current control and without regards to the GPIO control signal. Figure 24 shows a screenshot of this behavior.

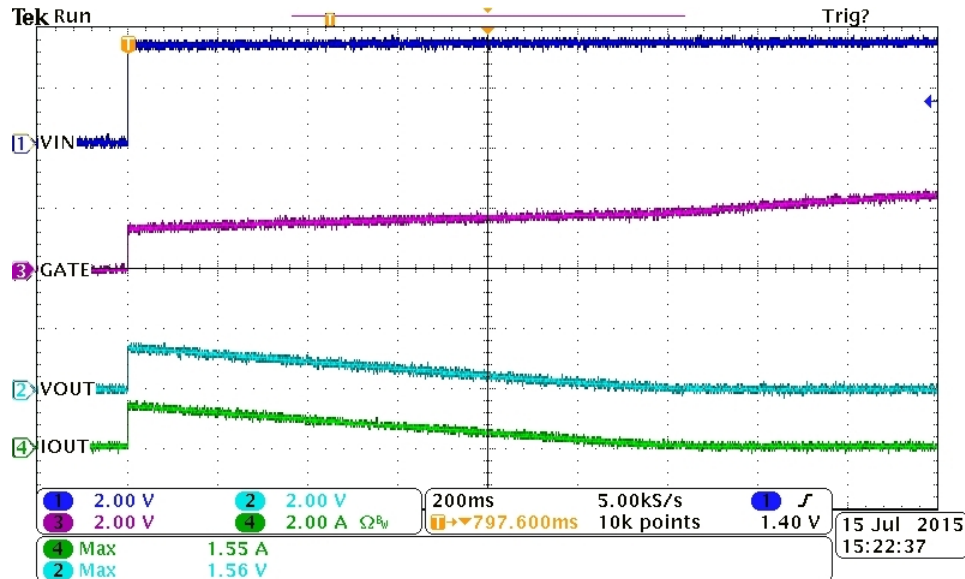


Figure 24. VIN Voltage step Behavior for PMOS Discrete Circuit #3

As VIN goes high, the gate voltage cannot keep up due to the delay caused by the gate capacitance and capacitor between the gate and drain. Therefore, the PMOS is able to turn on briefly before the gate can reach a voltage high enough to turn the PMOS off. This causes a significant amount of inrush current and output voltage which can potentially turn on undesired loads and cause stress on the power supply. This event is especially prevalent in systems with a replaceable battery since putting in a new battery can cause VIN to go from 0 V to the battery voltage very quickly.

5 NMOS Discrete Circuits

A discrete power switching solution can also be put together by using an NMOS as the main pass FET. With an NMOS, the voltage on the gate needs to be higher than the input voltage to turn it on. This means that lower voltages can be switched without requiring a large voltage on the gate. For example, an NMOS transistor with a V_{GS} turn on requirement of 1 V could have a 3.3 V GPIO controlling the gate and switch low voltage rails such as 1.8 V, 1.2 V, or even 0.8 V.

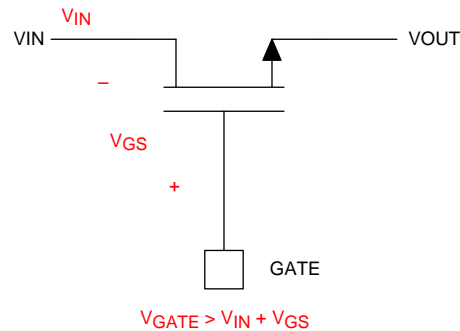


Figure 25. NMOS V_{GS} Requirements for Turn on

While these voltages can be switched, a higher gate voltage may be desired for a higher V_{GS} voltage and lower on-resistance. To switch a high voltage rail (5 V or above), an even higher voltage rail needs to be available in the system to switch the gate of the NMOS. If one is not available, a discrete charge pump can be used to drive the voltage up to an appropriate level for that transistor.

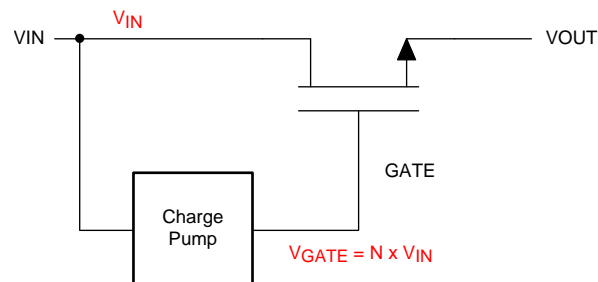


Figure 26. NMOS Charge Pump Circuit

With a charge pump, a high V_{GS} for the NMOS can be achieved, and this will drive the on-resistance of the circuit lower. However, this comes at the cost of a larger solution size, increased BOM count, and higher cost when compared to the PMOS solution.

6 Load Switches

After evaluating several discrete circuits for load switching, a comparison can be made to the integrated load switch solution.

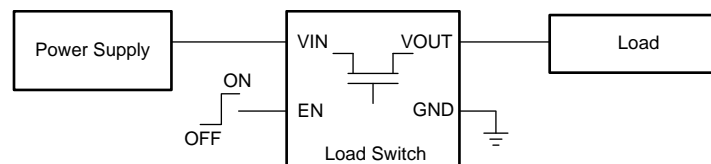


Figure 27. Load Switch Circuit

One clear advantage for using a load switch is the reduced complexity. There is only one device needed that incorporates the advantages of all the above circuits. A load switch is able to provide a lower input voltage range, can utilize low voltage GPIO signals, and uses a controlled rise time to manage the inrush current.

6.1 Performance

Figure 28 shows the TPS22969 load switch configured with a 1-Ω, 4.7-μF load.

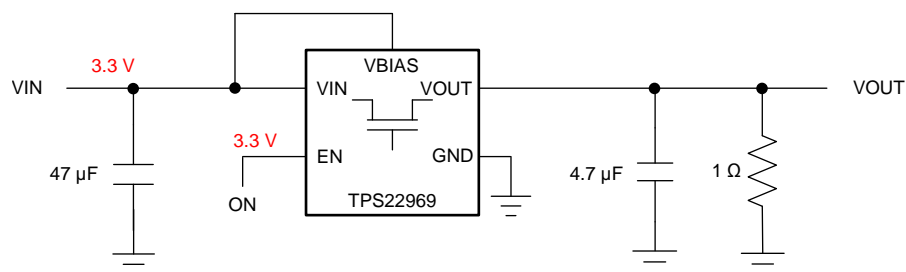


Figure 28. TPS22969 with Resistive and Capacitive Load

The screenshot in Figure 29 was taken using the configuration from Figure 28.

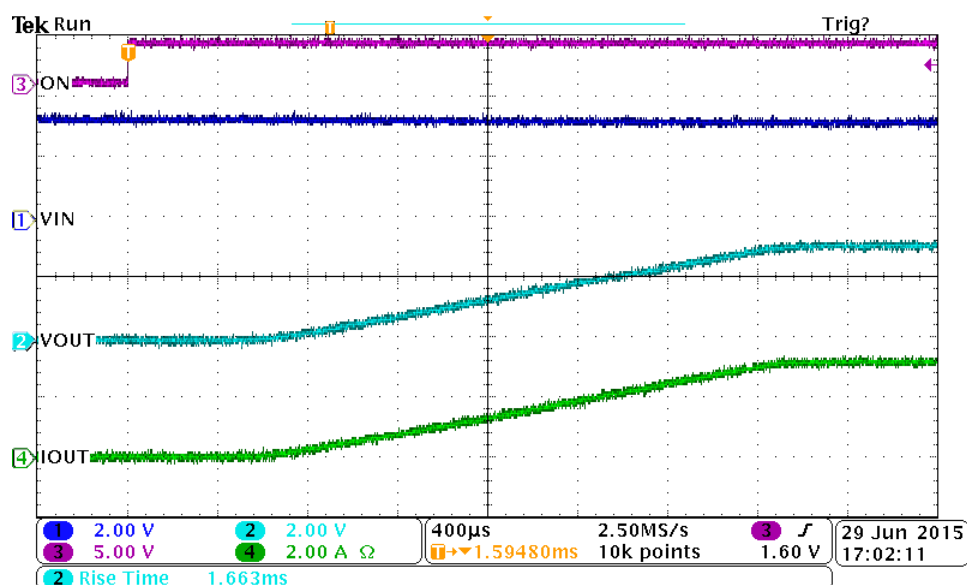


Figure 29. Turn on Behavior for TPS22969

The controlled rise time ensures a lower inrush current and no voltage dip on the input without any external components needing to be used. Figure 30 shows that the controlled rise time of the TPS22969 limits the inrush current generated from the 4.7 μF output capacitor to about 12 mA.

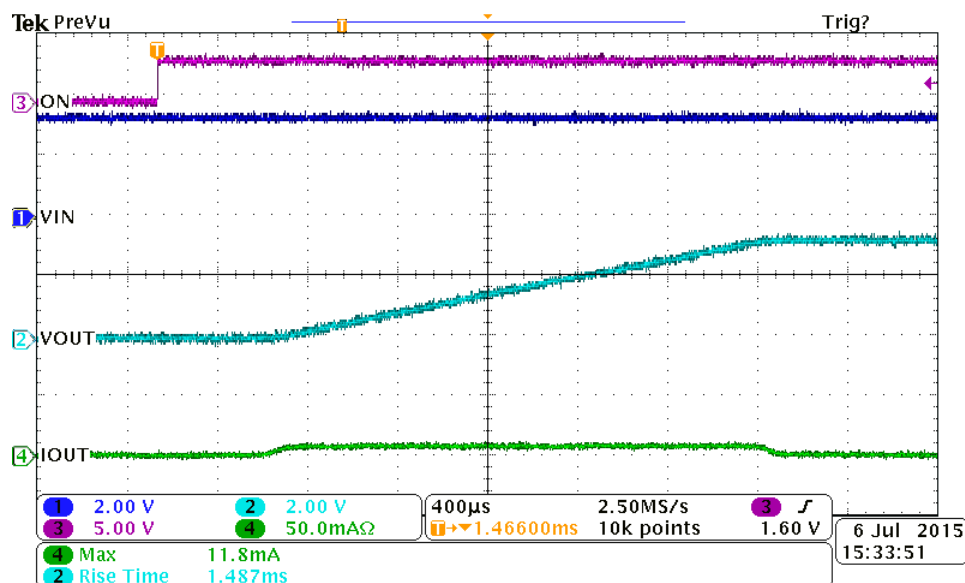


Figure 30. Inrush Current for TPS22969

When observing VIN ramping up on the third PMOS circuit, there was both a voltage and current which was allowed to pass through to VOUT. When VIN is applied to the TPS22969 load switch, there is no effect on VOUT. Figure 31 shows VIN applied to the TPS22969

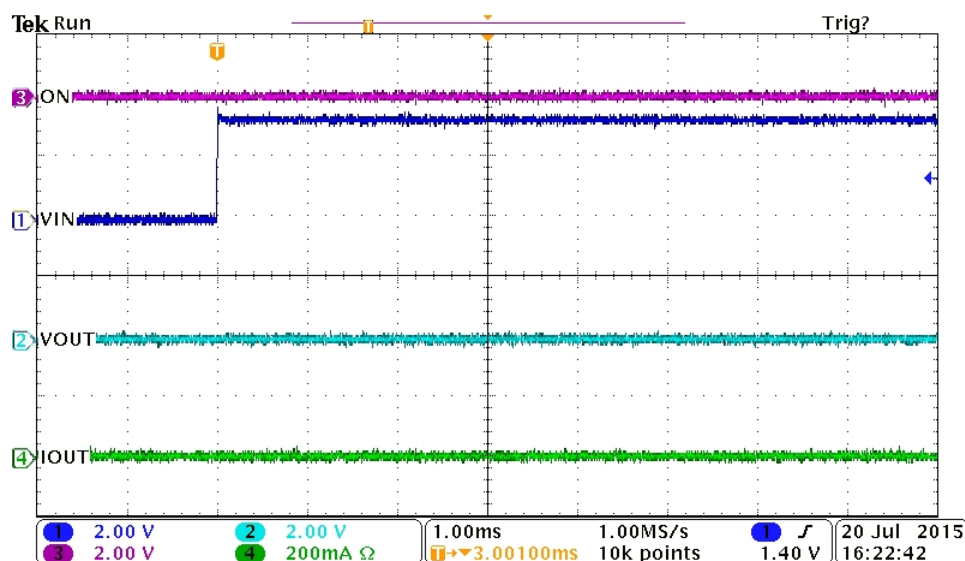


Figure 31. VIN Step on TPS22969

6.2 Size Advantage

Another advantage of using a load switch solution is the reduced number of components and solution size. Load switches are designed to integrate all of these components into packages that can be smaller than even the MOSFETs by themselves. Figure 32 shows a to scale comparison of a PMOS solution and an equivalent load switch.

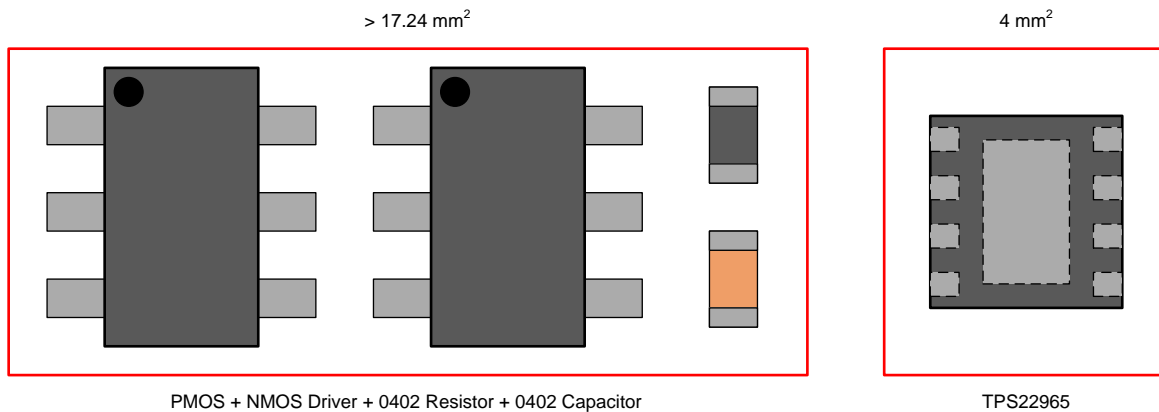


Figure 32. Size Comparison between the TPS22965 and an Equivalent Discrete Solution

6.3 Feature Advantages

There are several features which are integrated into load switches that are not found in any of the above discrete circuits. To add *reverse current blocking* to a discrete solution, an additional MOSFET would be needed to create a back to back configuration. The TPS22953 and TPS22963 are just two examples from Texas Instruments' load switch portfolio which come with this feature already built in.

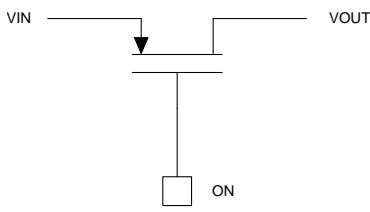
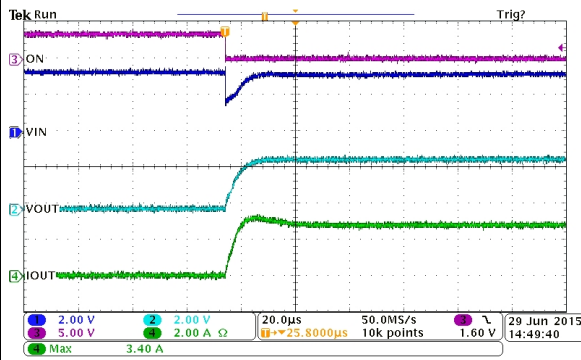
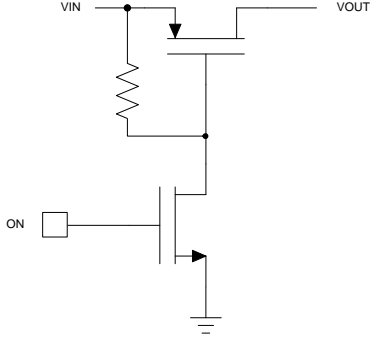
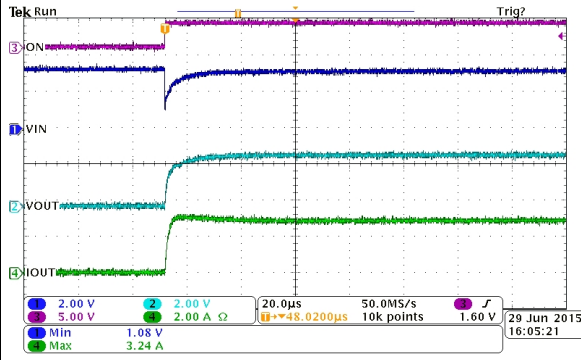
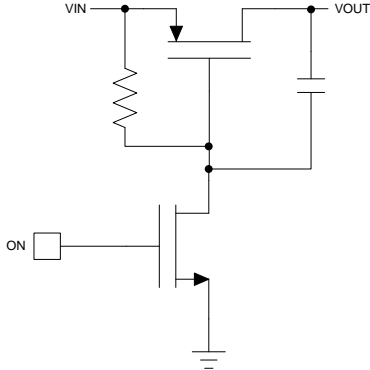
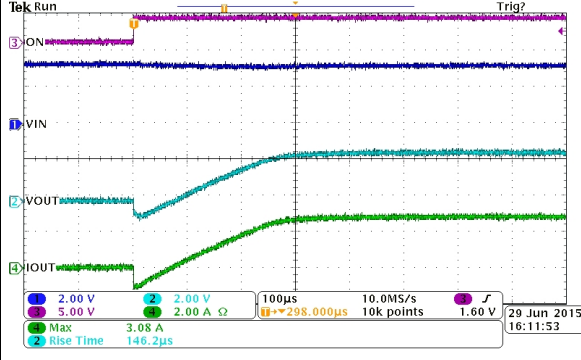
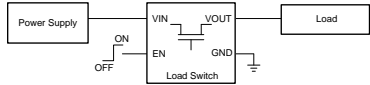
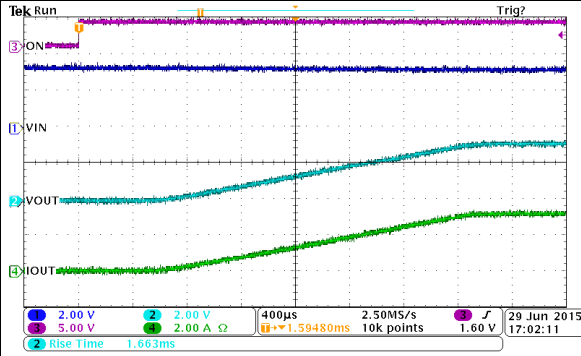
Quick output discharge is a load switch feature which discharges VOUT through an internal path to ground when the switch is disabled. This provides a known state on the output and ensures that all loads have been discharged and are turned off.

The TPS22953 and TPS22954 implement a *power good* feature which can provide a signal to the user when VOUT has charged to 90% of the final value. This signal can be fed to the enable pin of downstream modules so that they can turn on when the load switch has provided power. This feature can also be used for power sequencing, allowing the user to enable one load switch and have multiple rails come up in a specific order.

7 Conclusion

While a discrete MOSFET solution can be used for power switching, it can also cause a high amount of inrush current, a negative voltage on the output, or an undesired output voltage on system startup. A load switch provides a controlled rise time (and therefore less inrush current), a smaller solution size, a wider range on VIN, and several additional features which can benefit the desired application. [Table 1](#) summarizes all of the circuits evaluated and shows their turnon behavior.

Table 1. Turn on Behavior Comparison Table

Circuit	Turn on Behavior	Summary
		Advantages <ul style="list-style-type: none"> - Simple Disadvantages <ul style="list-style-type: none"> - No inrush current control - V_{GS} concerns - Active Low
		Advantages <ul style="list-style-type: none"> - Expands VIN range Disadvantages <ul style="list-style-type: none"> - No inrush current control - V_{GS} concerns - Leakage path through the source to gate resistor
		Advantages <ul style="list-style-type: none"> - Inrush current control Disadvantages <ul style="list-style-type: none"> - Negative voltage on VOUT - VOUT voltage on VIN startup - V_{GS} concerns - Leakage path through the source to gate resistor
		Advantages <ul style="list-style-type: none"> - Inrush current control - Wide VIN range - Small solution, low BOM count - No VOUT voltage on VIN startup

8 References

1. TPS22969 5.5-V, 6-A, 4.4-mΩ On-Resistance Load Switch ([SLVSCJ7](#))

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