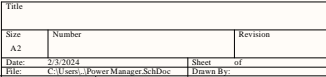
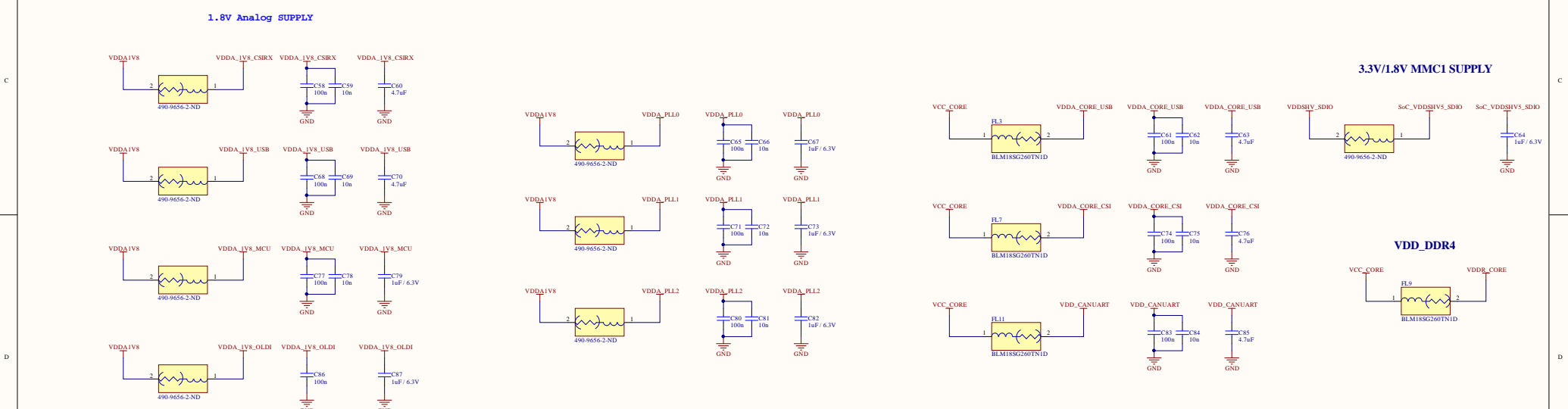
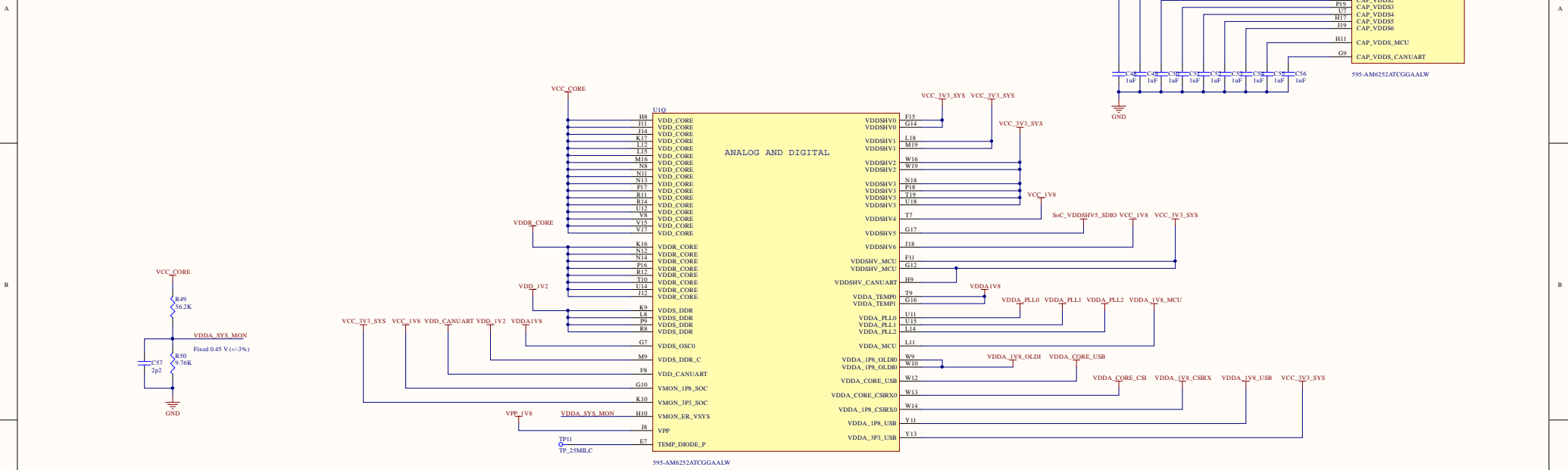


PMIC POWER MANAGER

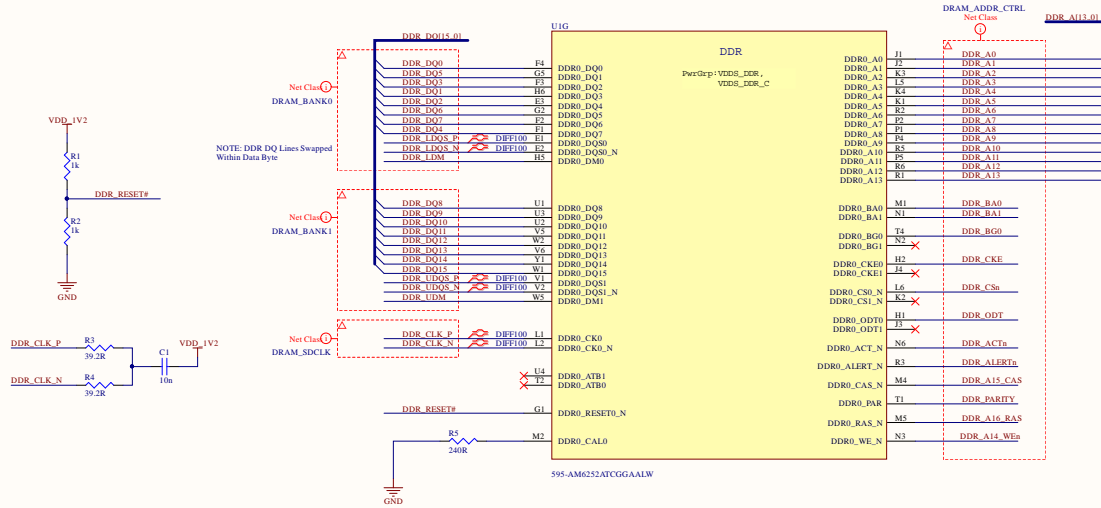


SOC POWER

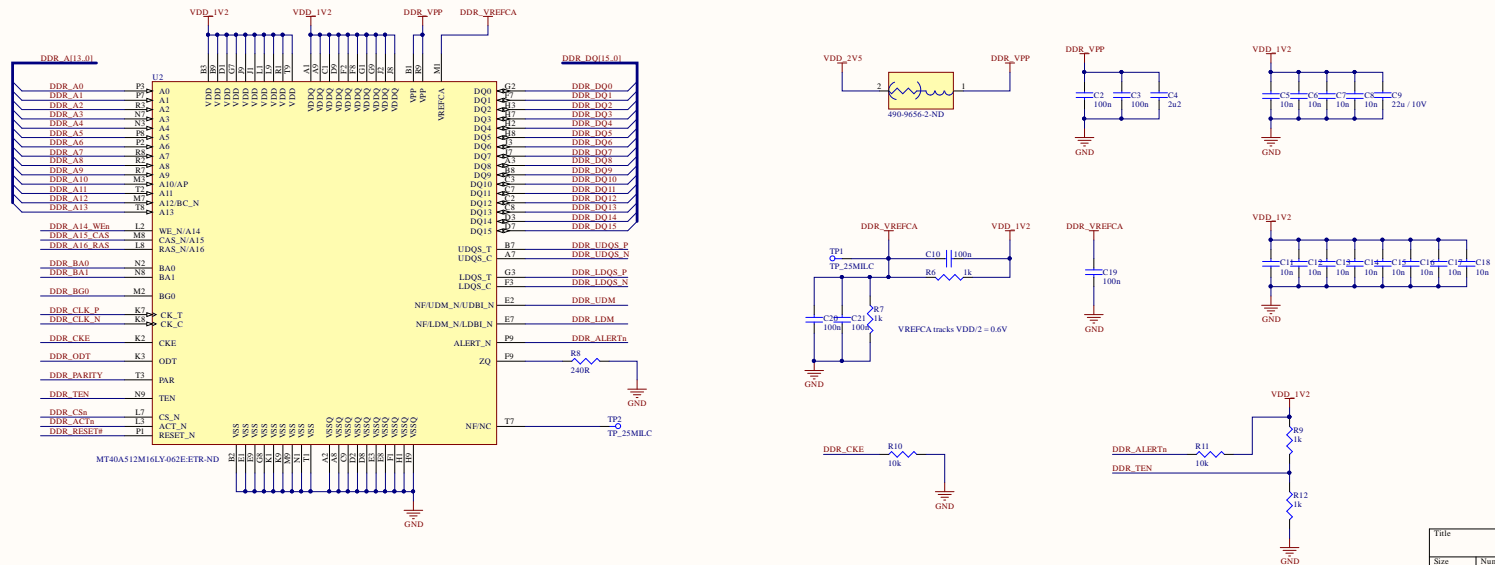


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SOC DDR INTERFACE

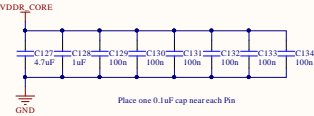
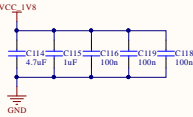
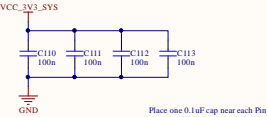
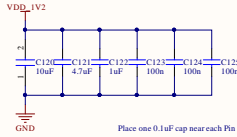
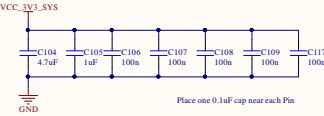
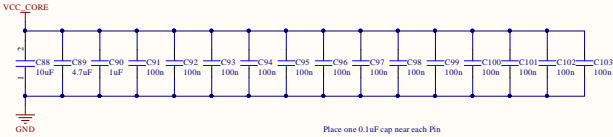


DDR4 DEVICE

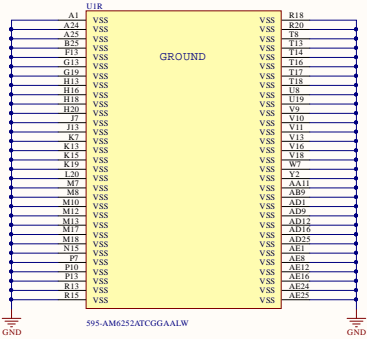


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SOC POWER DECAPS

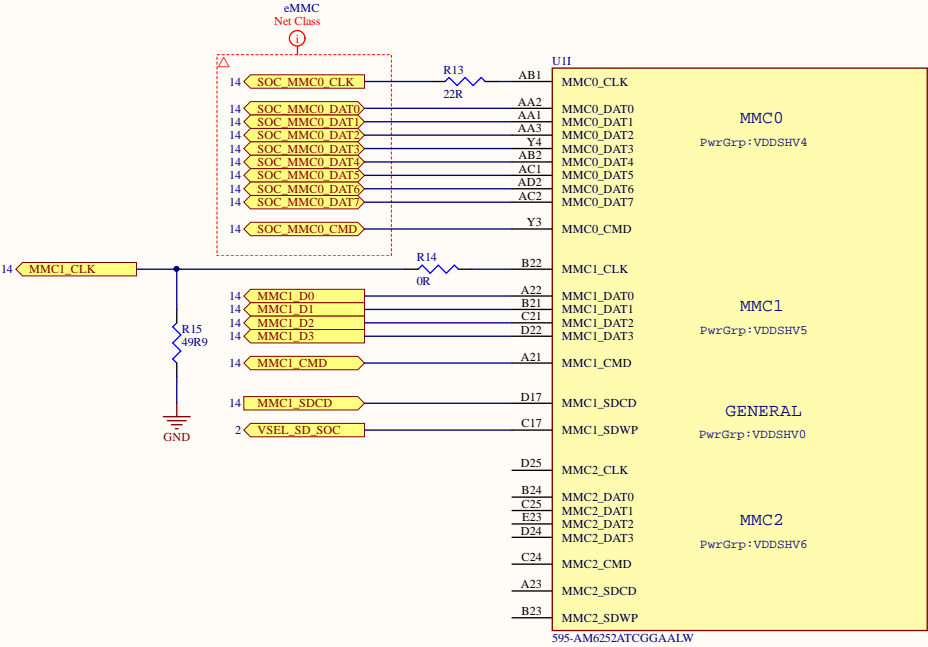


SOC POWER DECAPS



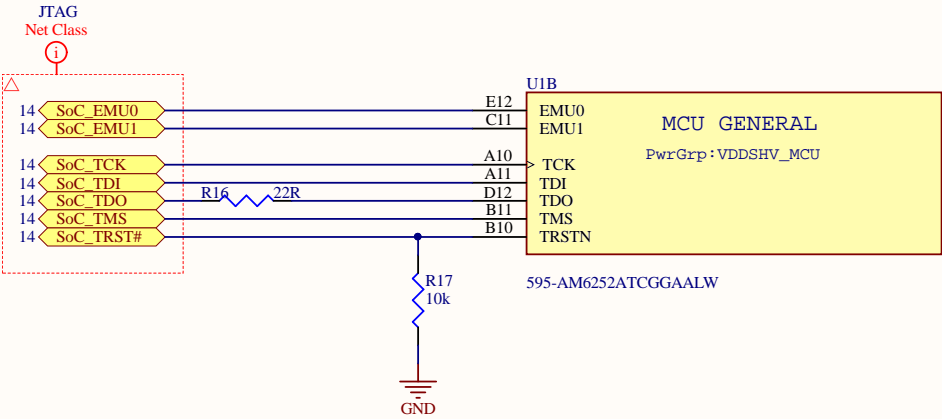
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SOC - MMC Interface

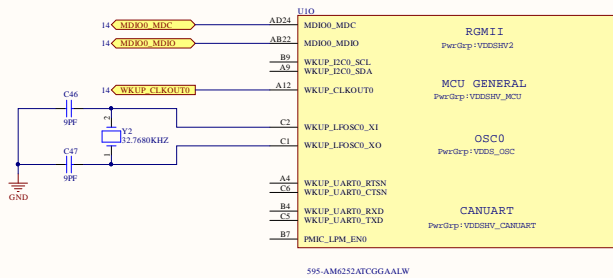
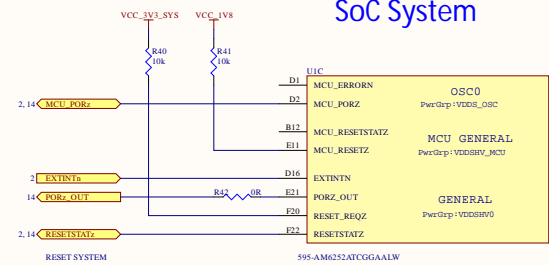
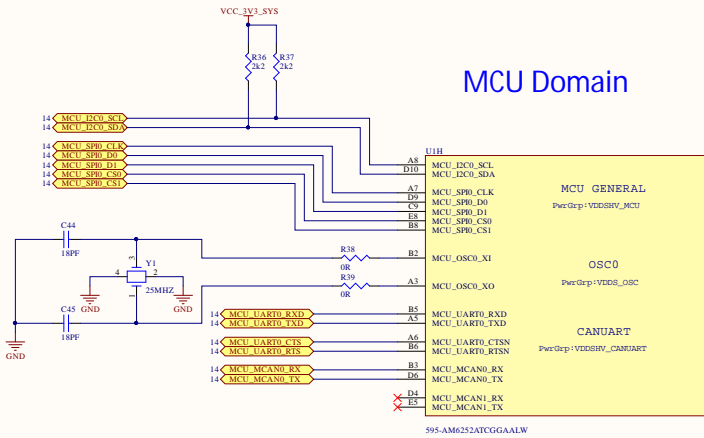


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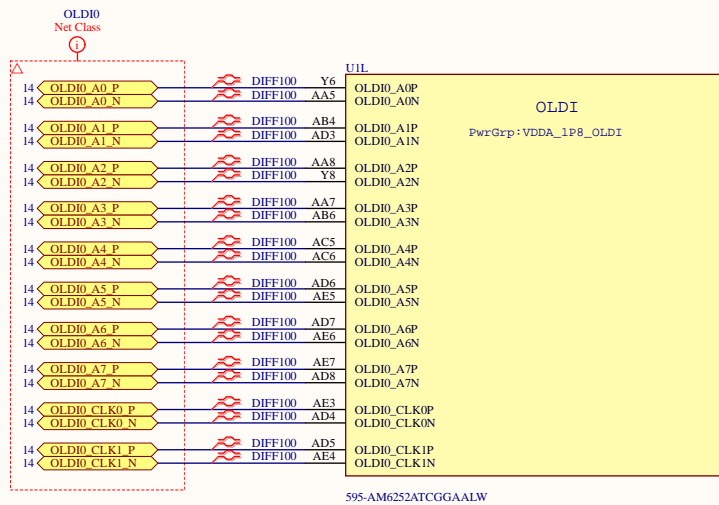
JTAG SOC SECTION



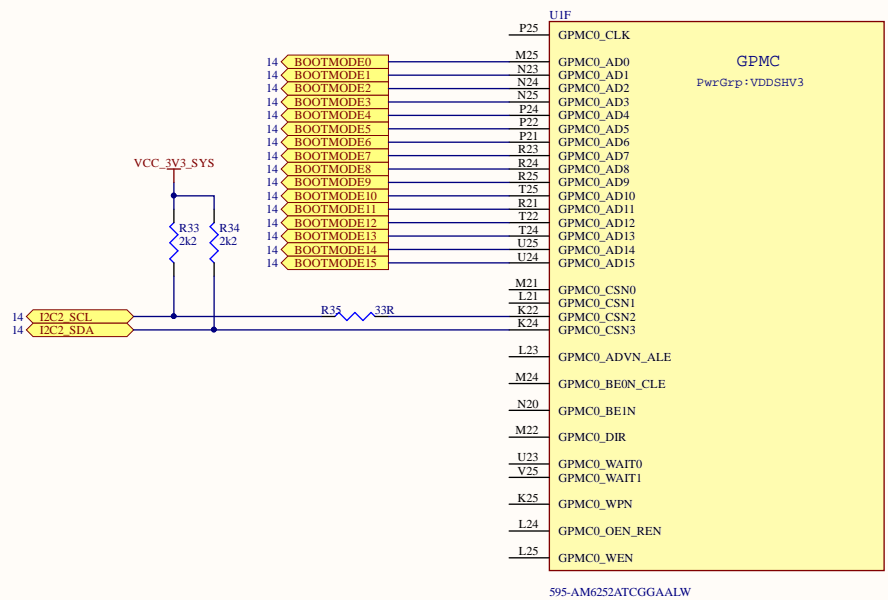
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Title		
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Bootstrap/GPIO 1.8V

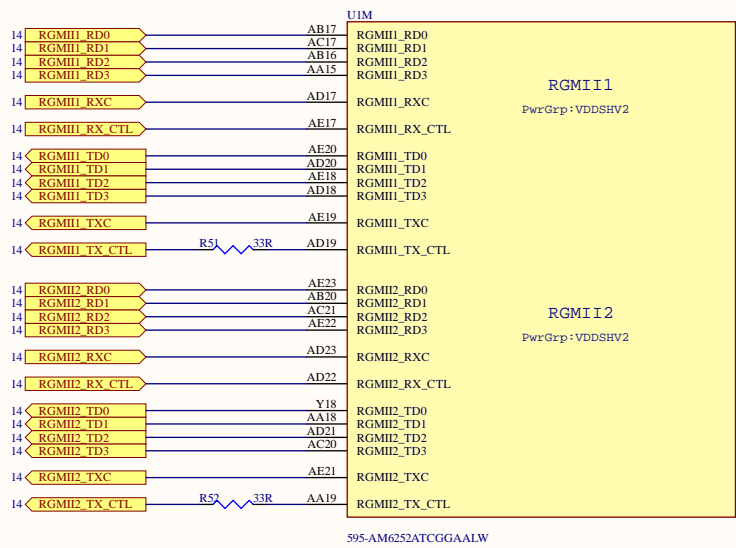


Note for AM625 Boot pin configuration by Switch

1. PLL Config B[2:0] = 0b011 : Ref Clock -> 25MHz
2. Primary Boot B[9:3] = 0b1001001 : eMMC Boot
3. Backup Boot B[13:10] = 0b1011 : UART Boot
4. Primary Boot B[9:3] = 0b1001000 : SDCard FS Boot
5. Backup Boot B[13:10] = 0b0001 : USB Dfu Boot

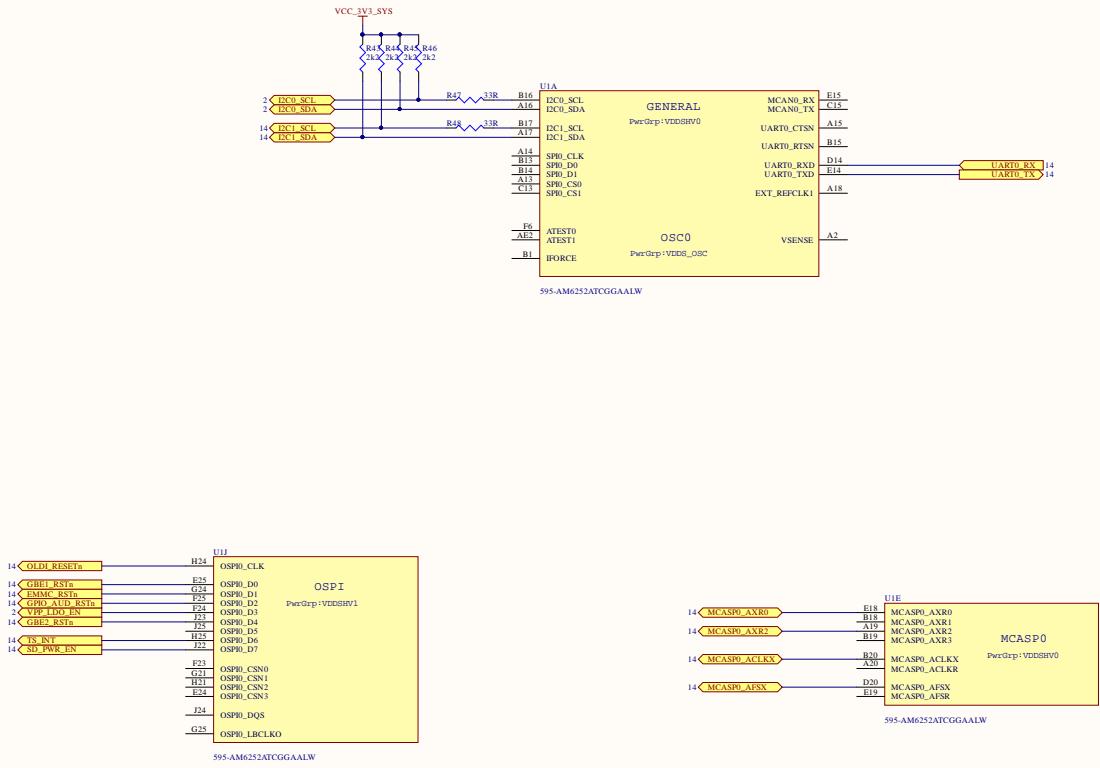
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SoC RGMII 1.8V

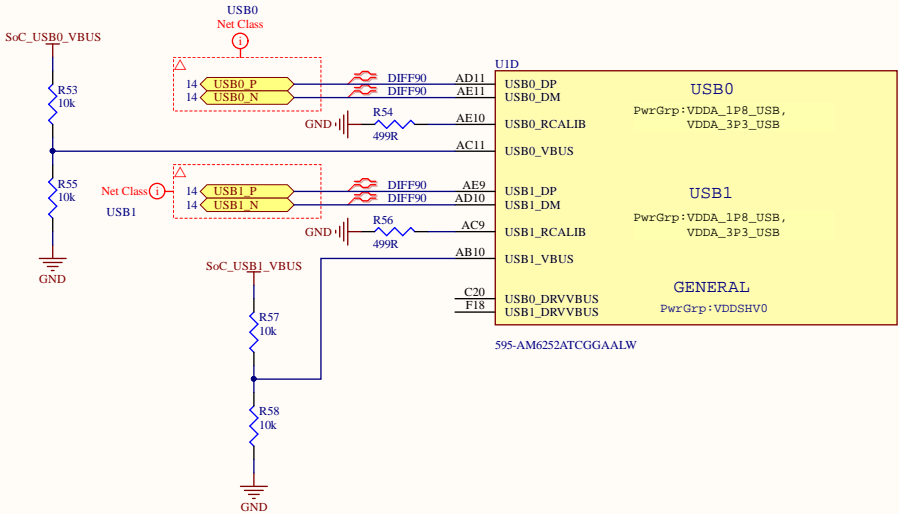


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SoC GPIO 3.3V

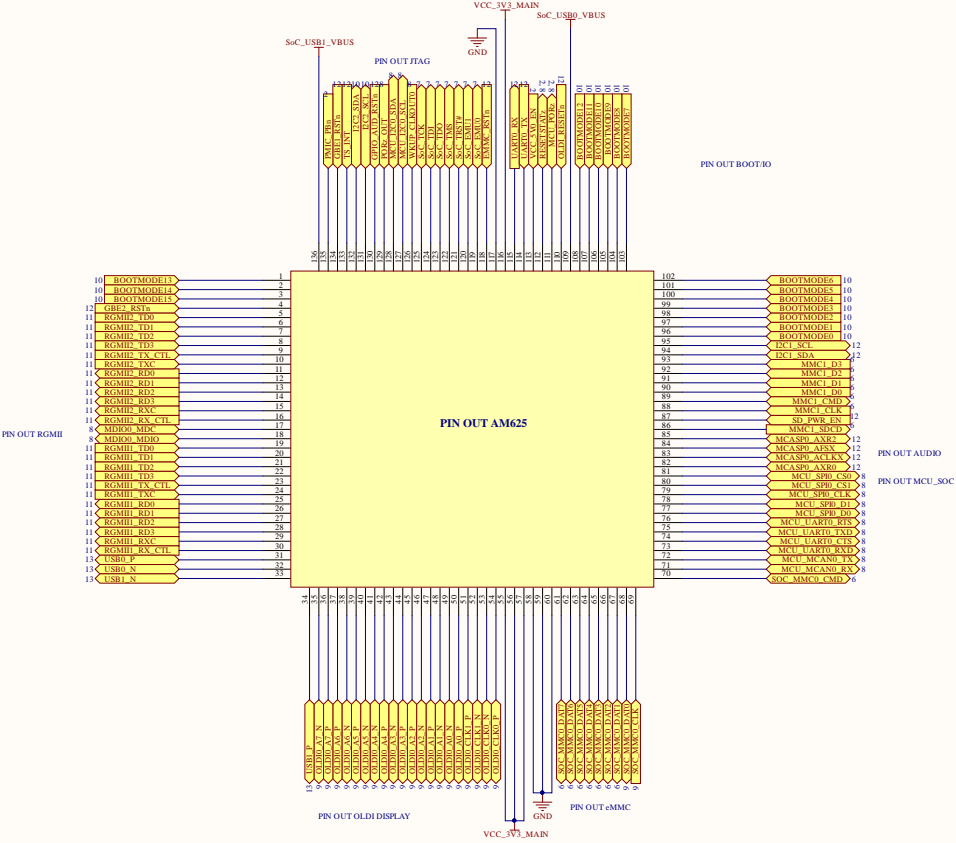


USB0/2.0

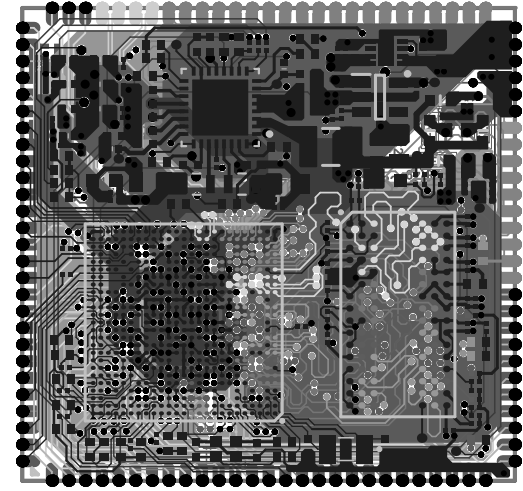


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SoC Pin_Out



Title		
Size	Number	Revision
A2		
Date:	2/1/2024	Sheet of
File:	C:\Users\SOE_PinOut_SchDoc	Drawn By:



Board S