

# **phyCORE®-AM62xx**

## **Hardware Manual**

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## 2 SOM Features

The phyCORE-AM62xx offers the following features:

- Insert-ready, small (43 mm x 32 mm) System on Module (SOM) subassembly in low EMI design, achieved through advanced SMD technology
- Populated with the Texas Instruments AM62xx SoC (13 x 13 mm, 0.5 mm pitch BGA)
- Single supply voltage of 5V with on-board power management IC
- Up to 4GB DDR4 RAM
- Up to 128GB on-board eMMC
- 1x Octal/Quad SPI Flash Subsystem connected to a 64MB NOR Flash
- 1x Gigabit Ethernet PHY (signals brought out to connector as diff pairs)
- 1x 4KB I<sup>2</sup>C EEPROM
- 1x On-board RTC
- 2x 0.5mm pitch 2x60 pin Samtec connectors (BSH-060-01-L-D-A-TR) that expose the following interfaces:
  - 2x MMC/SDIO modules
  - 2x USB 2.0 Ports
  - 1x 10/100/1000 Mbit Ethernet (signals brought out as RGMII)
  - 3x MCAN with CAN-FD support
  - 10x UART
  - 6x I<sup>2</sup>C
  - 1x JTAG debug port
  - 4x SPI
  - 3.3V/1.8V GPIOs
  - 4x EPWM (Enhanced Pulse Width Modulator) modules
  - 4x ECAP (Enhanced Capture) modules
  - 3x EQEP (Enhanced Quadrature Encoder Pulse) modules
  - 1x GPMC (General Purpose Memory Controller) module
  - 1x TRC (Trace) module
  - 1x CPTS (Common Platform Time Sync) module
  - 12x Timer modules
  - 1x CSI (Camera Serial Interface) module
  - 3x McASP (Multichannel Audio Serial ports) modules
  - 1x OLDI/LVDS (4 lanes - 2x) display module
  - 1x 24-bit RGB parallel display module

**NOTE:**

Some of the features listed are not available simultaneously due to the multiplexing options of the various processor pins. Refer to the sections 5 – 12 of the manual for further information on available multiplexing options and the pinout of signals.

# 3 Conventions, Abbreviations and Acronyms

This hardware manual describes the PCM-071 System on Module, henceforth referred to as phyCORE-AM62xx. The manual specifies the phyCORE-AM62xx's design and function. Precise specifications for the Texas Instruments AM62xx SoC can be found in the [AM62xx Technical Reference Manual](#).

We refrain from providing detailed part specific information within this manual which can be subject to changes. This is due to the continuous maintenance of our products. Please read section [13.4 Product Change Management](#) for more information.

The BSP delivered with the phyCORE-AM62xx includes drivers and/or software for controlling all components such as interfaces, memory, etc. Therefore, programming close to the hardware (at the register level) is not necessary in most cases. For this reason, this manual contains no detailed description of the processor's registers, or information relevant for software development. Please refer to the [AM62xx Technical Reference Manual](#) if such information is needed.

## 3.1 Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n" or end in z (e.g.: nRD or RDz), are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I<sup>2</sup>C devices always represent the 7 most-significant bits (MSB) of the address byte. The correct value of the least-significant bit (LSB) will depend on the desired command (read (1) or write (0)) and must be added to get the complete address byte. E.g. given the address in this manual 0x41 => the complete address byte = 0x83 reads from the device and 0x82 to writes to the device
- Text in *blue italics* indicate a cross-reference to an internal section of this Document. Click these links to quickly jump to the applicable part, chapter, table, or figure.
- Text in underlined in blue indicate an external link. Click these links to quickly jump to the applicable URL.
- References made to the phyCORE-Connector always refer to the high density Samtec connectors on the undersides of the phyCORE-AM62xx System on Module.

## 3.2 Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

**Table 1 Abbreviations and Acronyms used in this Manual**

Abbreviation	Definition
--------------	------------

BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Linux) preinstalled on the module and Development Tools)
CB	Carrier Board; used in reference to the phyCORE Development Kit Carrier Board
DDR	Double data rate
DRAM	Dynamic random access memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FSI	Fast Serial Interface
GPIO	General-Purpose Input/Output
GPT	General-Purpose Timer
J	Solder Jumper: these types of jumpers require solder equipment to remove and place
JP	Solderless Jumper: these types of jumpers can be removed and placed by hand with no special tools
JTAG	Joint Test Action Group (a serial bus protocol usually used for test purposes)
LCD	Liquid Crystal Display
PCB	Printed circuit board
PCI	Peripheral Component Interconnect
PCIe	PCI express
PCM	Product Change Management
PCN	Product Change Notification
PDI	PHYTEC Display Interface; defined to connect PHYTEC display adapter boards, or custom adapters
PEB	PHYTEC Expansion Board
PMIC	Power management IC
POR	Power-on reset
PRU	Programmable Realtime Unit
PWM	Pulse-width Modulation
RTC	Real-time clock
SD	Secure Digital
SMT	Surface mount technology
SOC	System on Chip
SOM	System on Module; used in reference to the BOARD DESIGNATOR/ SOM BOARD NAME module
SPI	Serial Peripheral Interface
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the Carrier Board
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

### 3.3 Types of Signals

Different types of signals are brought out at the phyCORE-Connector. *Table 2* below lists the abbreviations used to specify the type of a signal.

**Table 2 Signal Types Used in this Manual**

Signal Type	Description	Abbreviation
Analog	Analog	A
Power	Supply voltage input	PWR_I
Input	Digital input	I
Output	Digital output	O
IO	Bidirectional input/output	I/O
OD-Bidir PU	Open drain input/output with pull up	OD_BI
OD-Output	Open drain output without pull-up, requires an external pull-up	OD
5V Input PD	5 V tolerant input with pull down	5V_PD
LVDS Input	Differential line pairs 100 Ω LVDS level input	LVDS_I
LVDS Output	Differential line pairs 100 Ω LVDS level output	LVDS_O
USB IO	Differential line pairs 90 Ω USB level bidirectional input/output	USB_I/O
ETHERNET Input	Differential line pairs 100 Ω Ethernet level input	ETH_I
ETHERNET Output	Differential line pairs 100 Ω Ethernet level output	ETH_O
ETHERNET IO	Differential line pairs 100 Ω Ethernet level bidirectional input/output	ETH_I/O
PCIe Input	Differential line pairs 100 Ω PCIe level input	PCIe_I
PCIe Output	Differential line pairs 100 Ω PCIe level output	PCIe_O
MIPI CSI-2 Input	Differential line pairs 100 Ω MIPI CSI-2 level input	CSI-2_I

## 4 Introduction



Figure 1. phyCORE-AM62xx SOM

The phyCORE-AM62xx belongs to PHYTEC's phyCORE System on Module family. The phyCORE boards integrate all core elements of a SoC on a single module and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

The phyCORE-AM62xx is a small (43mm x 32mm) insert-ready System on Module populated with the Texas Instrument's AM62xx SoC. Its universal design enables its insertion in a wide range of embedded applications. Most of the SoC signals and ports extend from the SoC to the high-density pitch (0.5 mm) connectors aligning two sides of the board, allowing it to be plugged directly into a target application.

Implementing a phyCORE-AM62xx SOM as the "core" of your embedded design allows for increased focus on hardware peripherals and firmware without expending resources to "re-invent" microprocessor circuitry or other commonly used circuitry that has already been implemented on the phyCORE-AM62xx including a DDR RAM, an eMMC, an OSPI Flash, a power distribution network, an Ethernet PHY, an RTC, and an EEPROM. Production-ready board support packages (BSPs), design services for our hardware, and lifecycle maintenance of our parts will further reduce development time, risk, and allows for increased focus on product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution, new ideas can be brought to market in the most timely and cost-efficient manner.

Precise specifications for the processor populating the board can be found in the applicable processor reference manual or datasheet. The descriptions in this manual are based on the Texas Instrument's AM62xx. No descriptions of compatible SoC derivative functions are included; these are not relevant for the basic functioning of the phyCORE-AM62xx.

## Block Diagram

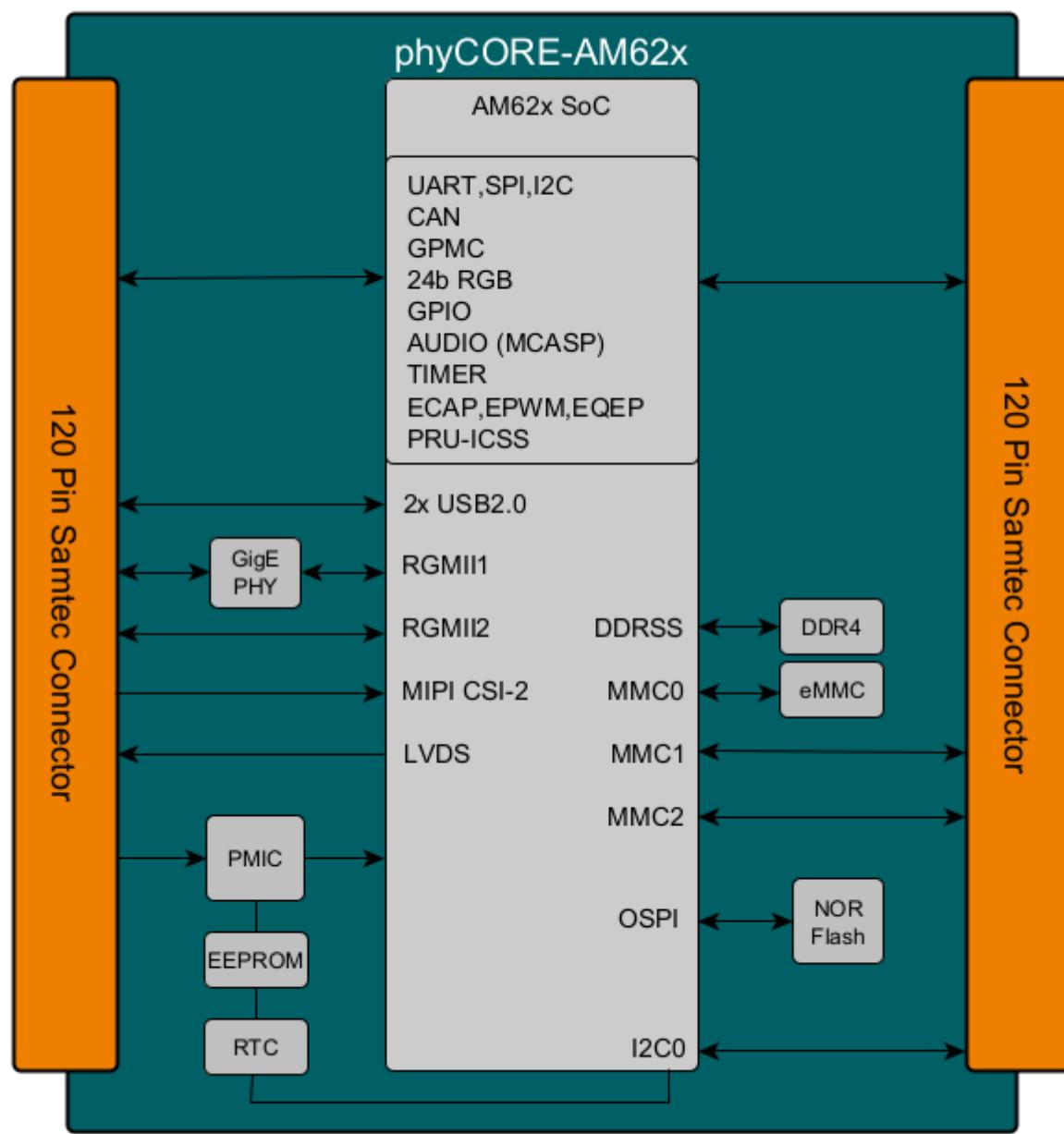


Figure 2. phyCORE-AM62xx Block Diagram

## 4.1 Physical Dimensions

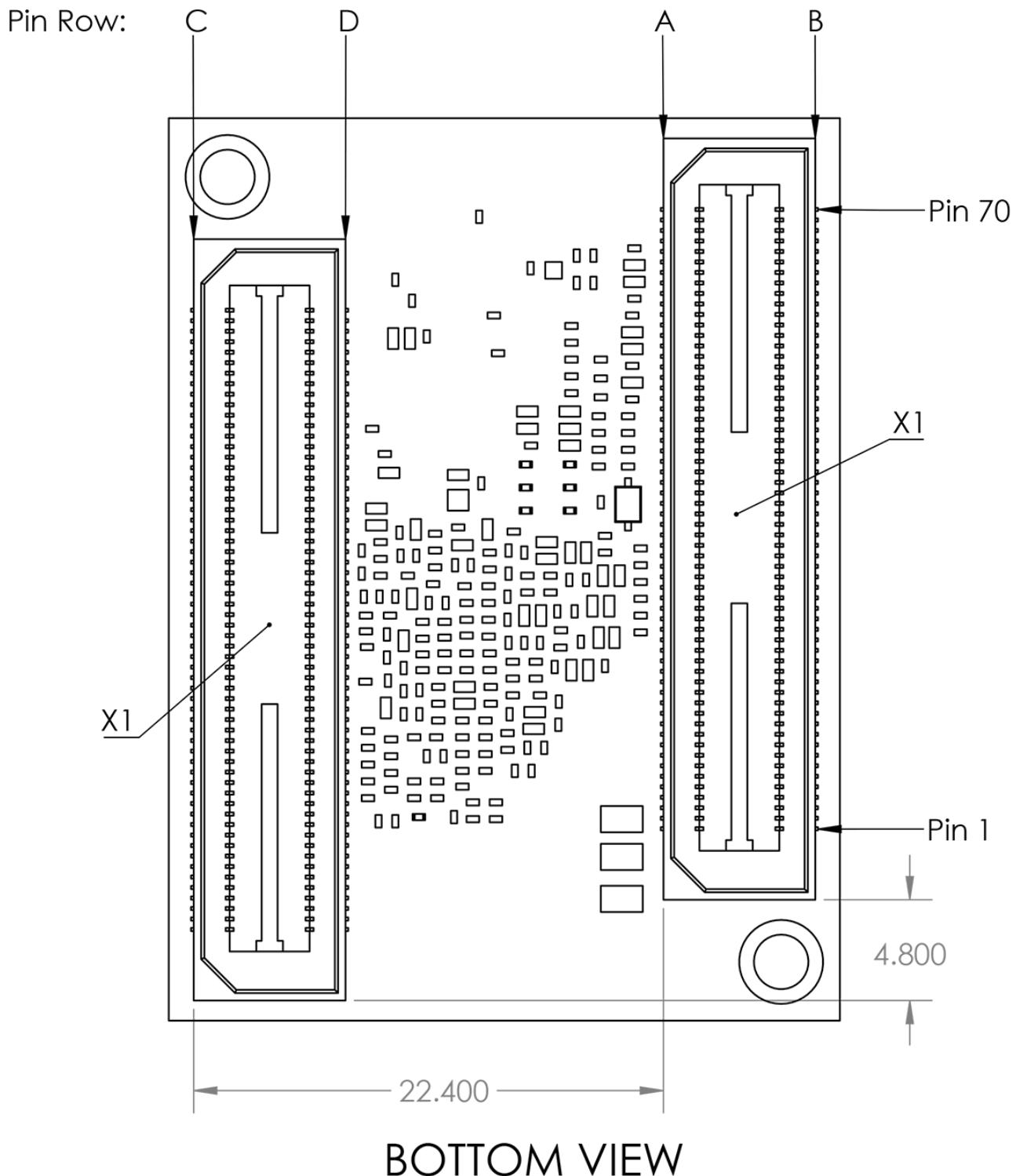


Figure 3. phyCORE-AM62xx Dimensions Top View

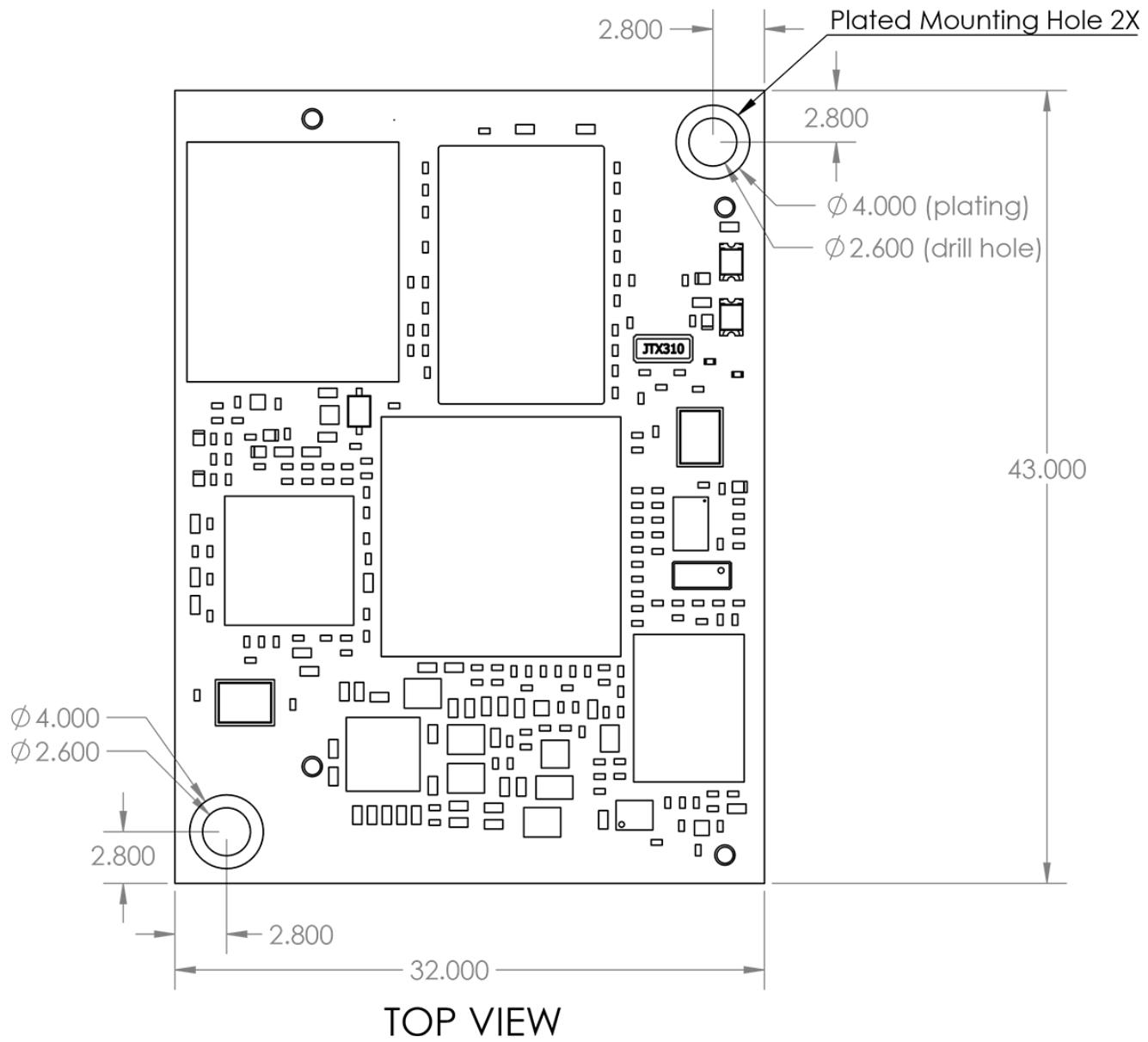


Figure 4. phyCORE-AM62xx Dimensions Bottom View

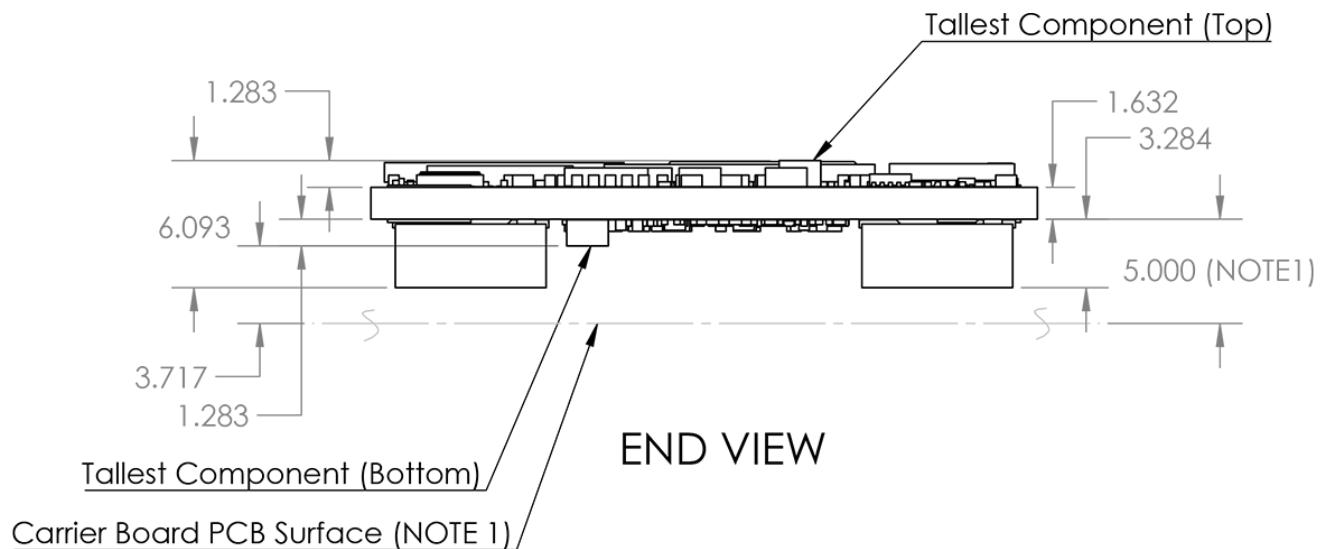


Figure 5. phyCORE-AM62xx Dimensions End View

## 4.2 Connector Alignment for Mating to Carrier Boards

The phyCORE-AM62xx has two mounting holes in the lower left and upper right corner sized for M2.5 screws/components.

It is recommended to use the following mounting hardware to secure the SOM to a mating carrier board:

- 2x M2.5x5mm Female-Female Standoffs
- 4x M2.5x4mm Screws
- 4x M2.5 Washers

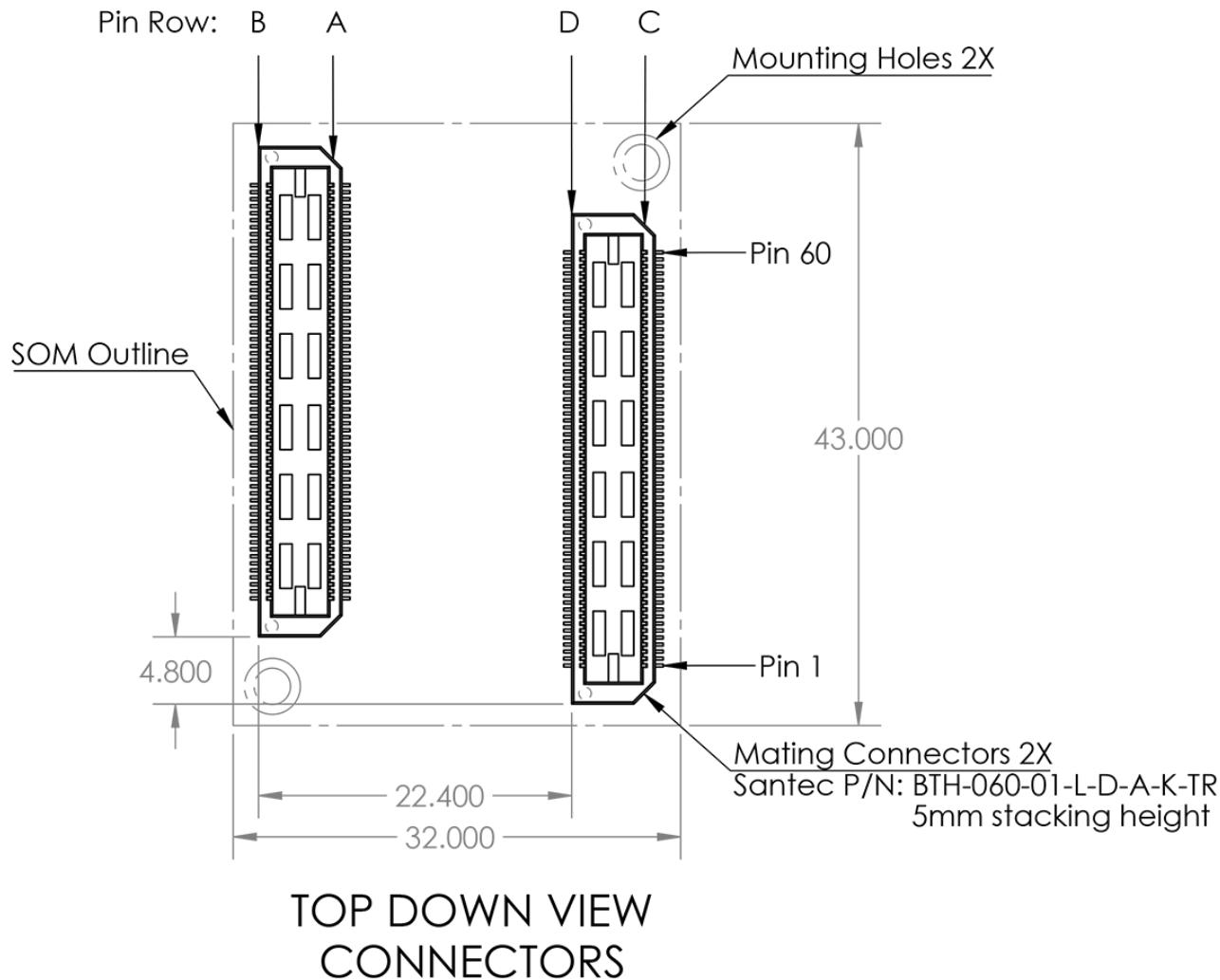


Figure 6. Top Down View of Mating Connectors

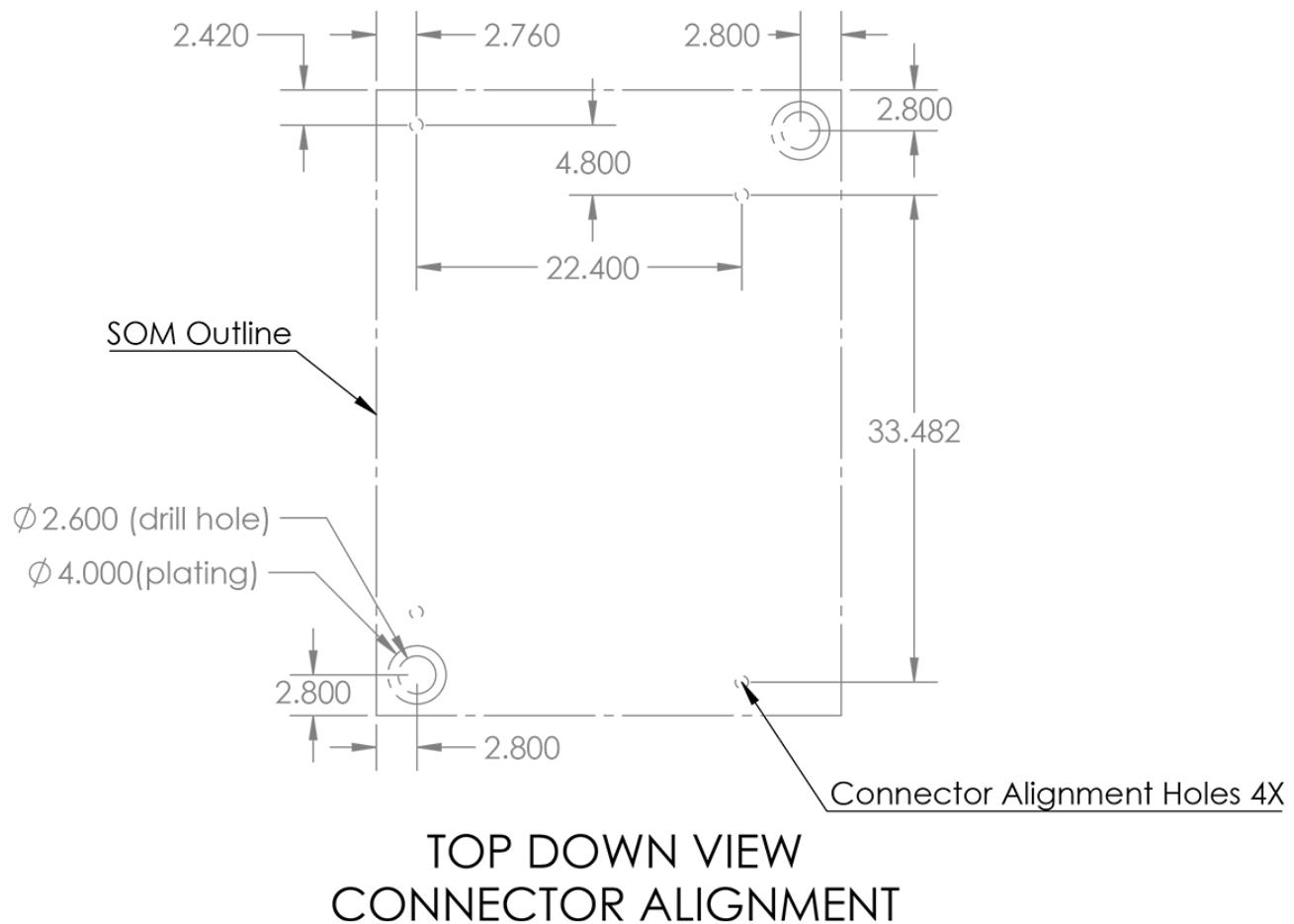
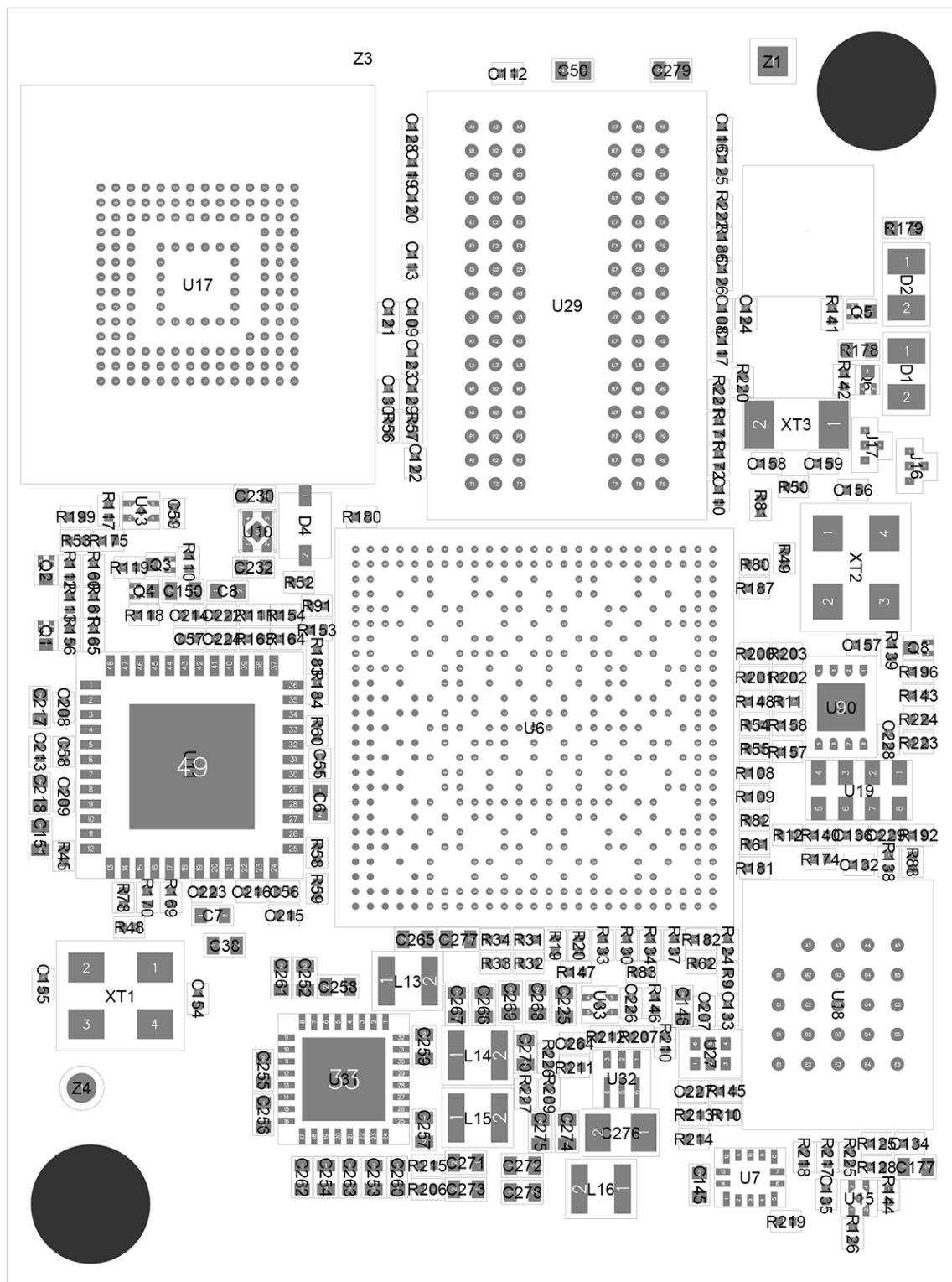


Figure 7. Carrier Board Alignment Hole Placement

## 4.3 Component Placement Diagram



**Figure 8. phyCORE-AM62xx Component Placement (processor side)**

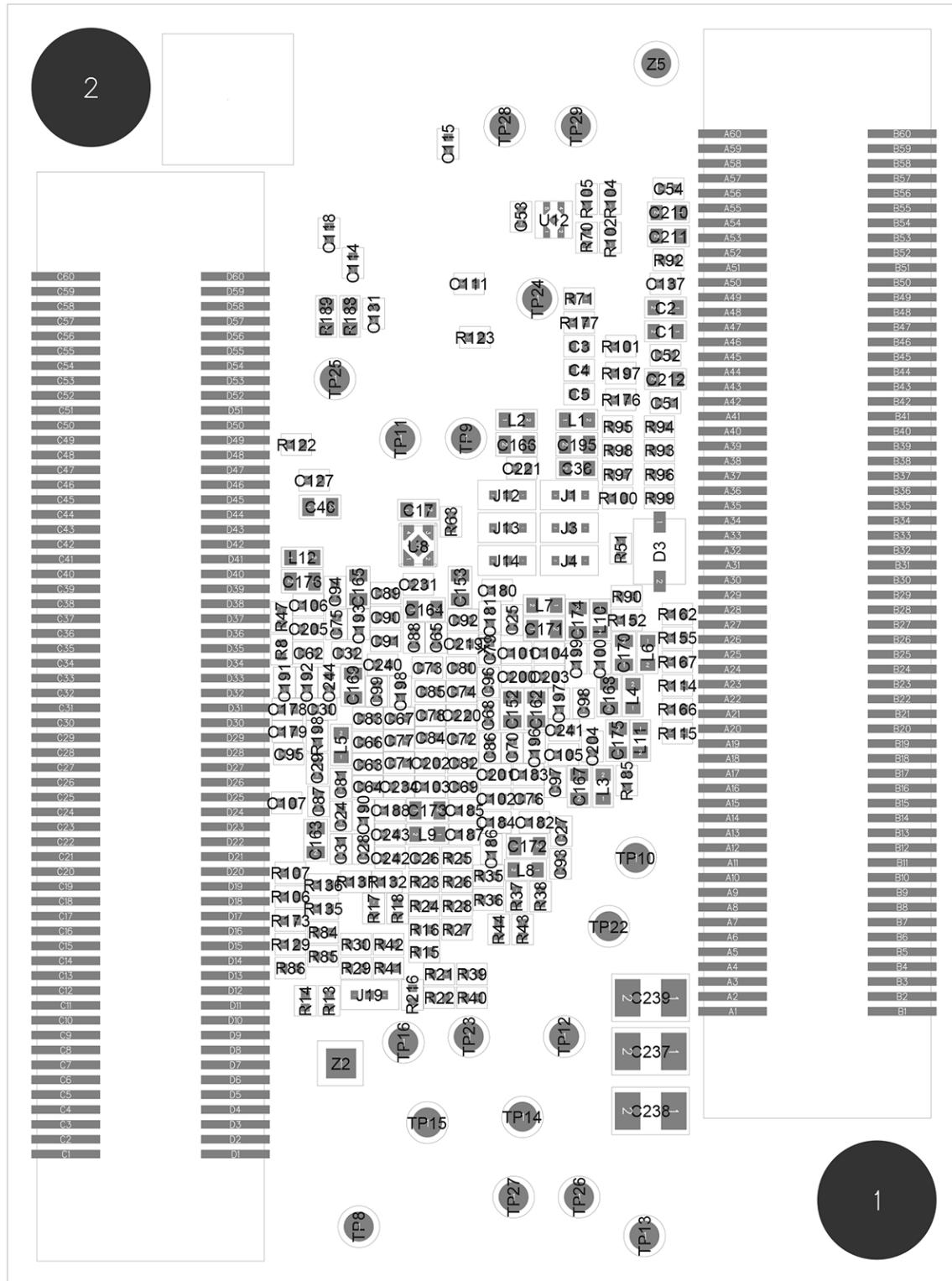


Figure 9. phyCORE-AM62xx Component Placement (connector side)

A searchable pdf of the phyCORE-AM62xx component placement can be found [here](#).

## 4.4 Technical and Electrical Specifications

**Table 3 Technical Specifications**

<b>Specification</b>	
Dimensions	43 mm x 32 mm x 3.8 mm
Mass	~9.3g
Storage Temperature	-40C to +85C
Operating Temperature	-40C to +85C
Typical Idling Power Consumption <sup>1</sup>	1.47W <sup>1</sup>

<sup>1</sup> Calculated from idle  $I_{VCC}$  in [Table 4](#)

**Table 4 Recommended Operating Conditions for the Input and Output Power Domains**

<b>Symbol</b>	<b>Description</b>	<b>Conditions</b>	<b>Min</b>	<b>Typical</b>	<b>Max</b>	<b>Unit</b>
VIN	5V SOM input voltage		4.5	5	5.5	VDC
VBAT	Backup battery for RTC		1.2	3	5.5	VDC
$I_{VIN}$	5V SOM operating current	Idle in Linux with external interfaces down/disconnected (except for Serial RS-232 and SD card)	-	293	-	mA
		Measured while device was under load <sup>1</sup>	-	490	-	mA
$I_{VBAT}$	RTC operating current		-	40	-	nA

<sup>1</sup> The load included the following interfaces/commands: the “memtester 500M” command was run, ETH0 was plugged in with iperf3 running, and two instances of the following command were run (yes > /dev/null &), [The Yes Command](#)

## 4.5 Minimum Requirements for Operation

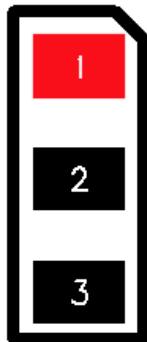
PHYTEC recommends the following minimum requirements for basic operation of the phyCORE-AM62xx SOM:

- Mount the SOM into the mating carrier board using two BTH-060-01-L-D-A-K-TR 0.5mm 2x60 Samtec connectors. Symbols/cells for the connectors are discussed in [Section 13.1 Integration](#).
- Connect all available 5V input pins to a power supply on a custom carrier board that provides at least 1000 mA.
- Connect all ground pins to ground.
- Implement a power sequencing circuit to avoid driving external power to the I/O pins of the PHYCORE-AM62xx SOM before the module is fully powered up. More details on this can be found in section [5.4 Power Sequencing](#).
- Implement at least one of the supported boot devices to support loading and executing application software. Refer to section [6.3 System Boot Configuration](#) for more details regarding supported boot modes. The phyCORE-AM62xx SOM provides an on-board eMMC, but it is recommended to support another boot source for development and debugging. PHYTEC suggests SD boot for which an example circuit can be seen in section [6.2.2.3 MMC Reference Circuit](#)

- Strap the boot signals to the desired levels at POR to configure the required boot mode for your application (i.e. using a DIP switch). This is required on the carrier board to override the default boot mode set on the SOM. Refer to section [6.3 System Boot Configuration](#) for more information.
- Implement a serial debug port (such as via UART0) to interface with the module for development. An example can be found in section [11.3 UART0](#).
- Implement a reset button for easy reset of the module.

## 4.6 Solder Jumpers

For configuration purposes the phyCORE-AM62xx SOM has several solder jumpers. [Figure 10](#) illustrates the numbering of the solder jumper pads, while [Figure 11](#) and [Figure 12](#) indicate the location and the default configuration of the solder jumpers on the board. [Table 5](#) provides a functional summary of the solder jumpers which can be changed to adapt the phyCORE-AM62xx SOM to specific design needs. It shows their default positions, possible alternative positions, type, and functions. The jumpers are a 0201 package size with a 1/16W or higher power rating.



**Figure 10. 3-Position Solder Jumper Pad Numbering Scheme**

**Table 5 Solder Jumper Settings**

Jumper	Position	Description	Type
<b>J1</b>	<b>1+2</b>	Sets the VDDSHV0 domain to 3.3V	0 Ω
	2+3	Sets the VDDSHV0 domain to 1.8V	
<b>J3</b>	<b>1+2</b>	Sets the VDDSHV2 domain to 3.3V	0 Ω
	2+3	Sets the VDDSHV2 domain to 1.8V	
<b>J4</b>	<b>1+2</b>	Sets the VDDSHV3 domain to 3.3V	0 Ω
	2+3	Sets the VDDSHV3 domain to 1.8V	
<b>J12</b>	<b>1+2</b>	Sets the VDDSHV6 domain to 3.3V	0 Ω
	2+3	Sets the VDDSHV6 domain to 1.8V	
<b>J13</b>	<b>1+2</b>	Sets the VDDSHV_MCU domain to 3.3V	0 Ω
	2+3	Sets the VDDSHV_MCU domain to 1.8V	
<b>J14</b>	<b>1+2</b>	Sets the VDDSHV_CANUART domain to 3.3V	0 Ω
	2+3	Sets the VDDSHV_CANUART domain to 1.8V	

Jumper	Position	Description	Type
J16	1+2	Sets pin D43 to X_CPSW_ETH0_GPIO_0	0 Ω
	2+3	Sets pin D43 to X_CPSW_ETH0_nINT	
	<b>2+4</b>	<b>Sets pin D43 to X_EMU0</b>	
J17	1+2	Sets pin D44 to X_RTC_EVI	0 Ω
	2+3	Sets pin D44 to X_VPP_EN	
	<b>2+4</b>	<b>Sets pin D44 to X_EMU1</b>	
J19	<b>1+2</b>	<b>Connect GPMC0_CLK to X_GPMC0_CLK</b>	
	2+3	Connect GPMC0_CLK to SD_VSEL The state of SD_VSEL determine the voltage level of SoC_VDDSHV5_SDIO.	

**NOTE:**

Jumper settings show the default position in **bold, blue text**. Pin 1 is highlighted with an alternate color in *Figure 10* and the solder jumper locations *Figure 11* / *Figure 12*.

Some of the phyCORE-AM62xx power domains can be configured for 1.8V or 3.3V operation via the solder jumpers in the table above. This allows for configuring the voltage levels of the associated I/O signals under these domains to meet application requirements. These domains are detailed in the table below:

**Table 6 Voltage Domain Configurations**

Voltage Domain	Jumper	Associated Signals
VDDSHV_MCU	J13	EMU0, EMU1, TCK, TDI, TDO, TMS, TRSTN, MCU_I2C0_SCL, MCU_I2C0_SDA, MCU_SPI0_CLK, MCU_SPI0_D0, MCU_SPI0_D1, MCU_OSC0_XI, MCU_OSC0_XO, MCU_SPI0_CS0, MCU_SPI0_CS1, WKUP_I2C0_SCL, WKUP_I2C0_SDA, WKUP_CLKOUT0, MCU_RESETSTATZ, MCU_RESETZ
VDDSHV_CANUART	J14	WKUP_UART0_RXD, WKUP_UART0_TXD, WKUP_UART0_CTSN, WKUP_UART0_RTSN, MCU_UART0_RXD, MCU_UART0_TXD, MCU_UART0_CTSN, MCU_UART0_RTSN, MCU_MCAN0_RX, MCU_MCAN0_TX, MCU_MCAN1_RX, MCU_MCAN1_TX, PMIC_LPM_ENO
VDDSHV0	J1	MMC1_SDWP, MMC1_SDCD, USBO_DRVVBUS, USB1_DRVVBUS, MCASPO_AXR0, MCASPO_AXR1, MCASPO_AXR2, MCASPO_AXR3, MCASPO_ACLKX, MCASPO_ACLKR, MCASPO_AFSX, MCASPO_AFSR, I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, SPI0_D0, SPI0_D1, SPI0_CS0, SPI0_CS1, SPI0_CLK, MCAN0_RX, MCAN0_TX, UART0_CTSN, UART0_RTSN, UART0_RXD, UART0_TxD, EXT_REFCLK1, PORZ_OUT, RESET_REQZ, RESETSTATZ, EXTINTN
VDDSHV2	J3	RGMII1_RD0, RGMII1_RD1, RGMII1_RD2, RGMII1_RD3, RGMII1_RXC, RGMII1_RX_CTL, RGMII1_TD0, RGMII1_TXC, RGMII1_TX_CTL, RGMII1_TD1, RGMII1_TD2, RGMII1_TD3, RGMII2_RD0, RGMII2_RXC, RGMII2_RX_CTL, RGMII2_TD0, RGMII2_TXC, RGMII2_TX_CTL, RGMII2_TD1, RGMII2_TD2, RGMII2_TD3, RGMII2_TD1, RGMII2_TD2, RGMII2_TD3, MDIO0_MDC, MDIO0_MDIO
VDDSHV3	J4	GPMC0_AD0, GPMC0_AD1, GPMC0_AD2, GPMC0_AD3, GPMC0_AD4, GPMC0_AD5, GPMC0_AD6, GPMC0_AD7, GPMC0_AD8, GPMC0_AD9, GPMC0_AD10, GPMC0_AD11, GPMC0_AD12, GPMC0_AD13, GPMC0_AD14, GPMC0_CLK, GPMC0_ADVN_ALE, GPMC0_OEN_RN, GPMC0_WEN, GPMC0_BEON_CLE, GPMC0_BE1N, GPMC0_WAIT0, GPMC0_WAIT1, GPMC0_WPN, GPMC0_DIR, GPMC0_CS0, GPMC0_CS1, GPMC0_CS2, GPMC0_CS3, GPMC0_AD15, VOUT0_DATA0, VOUT0_PCLK, VOUT0_DE, VOUT0_VSYNC, VOUT0_HSYNC, VOUT0_DATA1, VOUT0_DATA2, VOUT0_DATA3, VOUT0_DATA4, VOUT0_DATA5, VOUT0_DATA6, VOUT0_DATA7, VOUT0_DATA8, VOUT0_DATA9, VOUT0_DATA10, VOUT0_DATA11, VOUT0_DATA12, VOUT0_DATA13, VOUT0_DATA14, VOUT0_DATA15
VDDSHV6	J12	MMC2_CLK, MMC2_DAT0, MMC2_DAT1, MMC2_DAT2, MMC2_DAT3, MMC2_SDWP, MMC2_SDCD, MMC2_CMD

If manual jumper modification is required, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Follow the instructions carefully for whatever method of removal is used.

**CAUTION:**

If any modifications to the module are performed, regardless of their nature, the manufacturer warranty is voided.

**Figure 11. Jumper Locations (Processor side)**

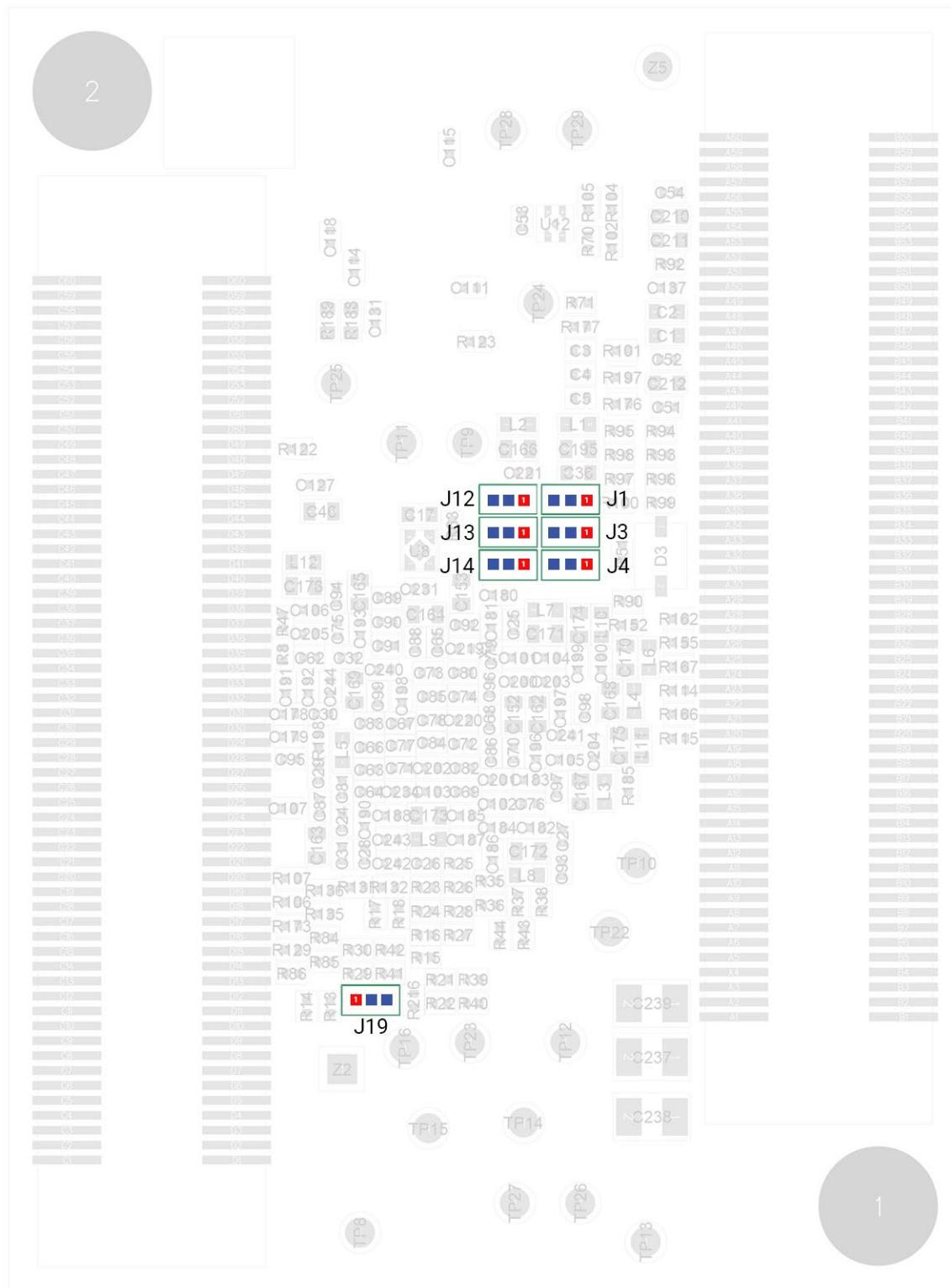
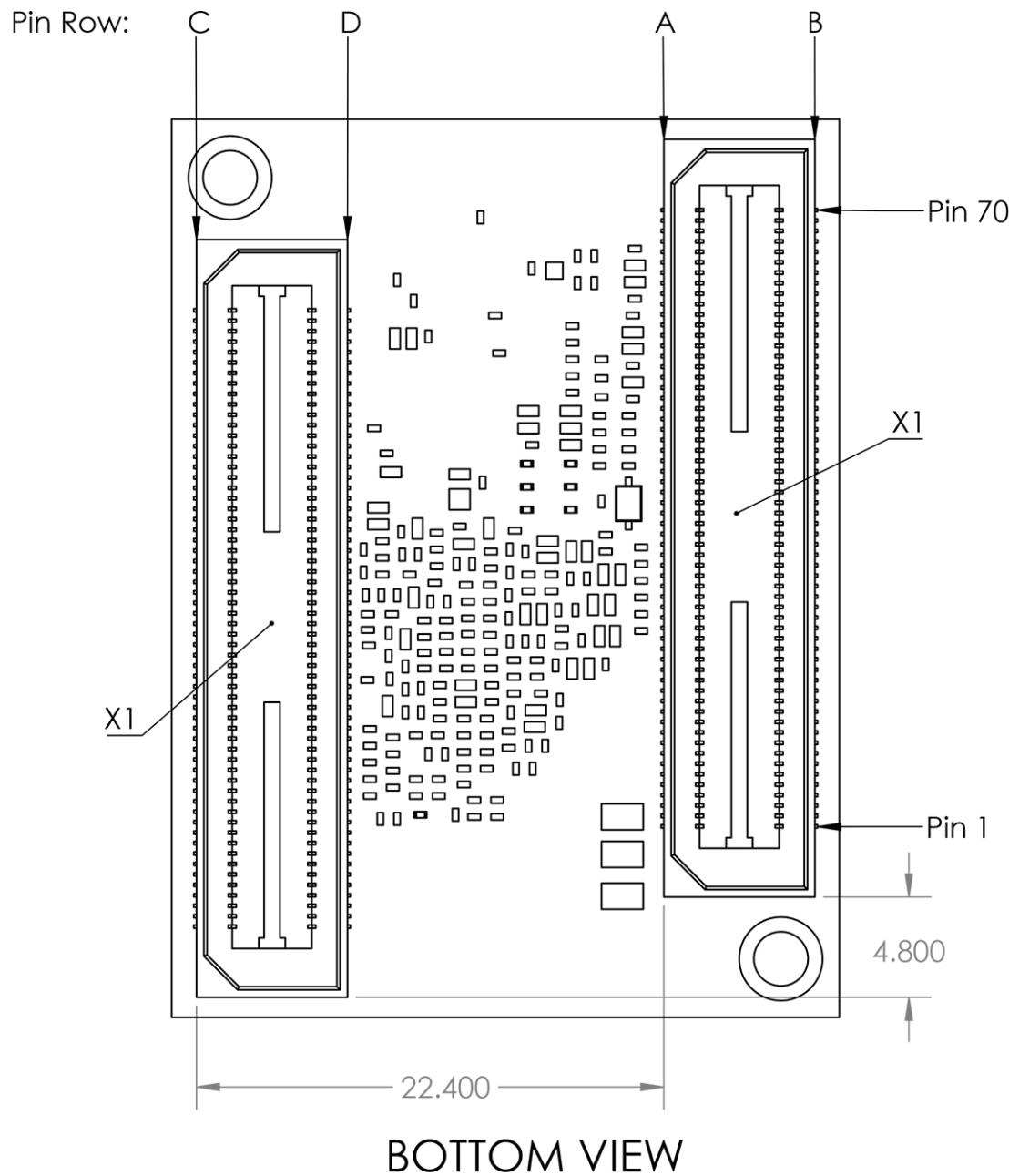


Figure 12. Jumper Locations (Connector side)

## 4.7 Pin Descriptions

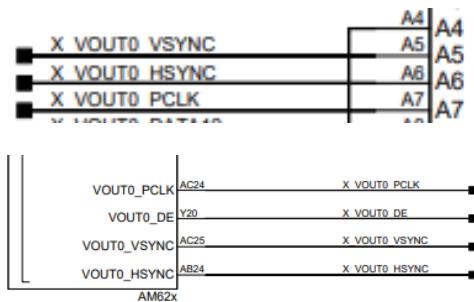
Most of the processor signals extend to the Samtec Connectors (0.5mm) lining two sides of the module (referred to as the phyCORE-Connector). The numbering scheme for the phyCORE-Connector is based on a two-dimensional matrix in which column positions are identified by a letter and row position by a number. [Figure 13](#) illustrates the numbered matrix system. It shows a bottom view of the phyCORE-AM62xx SOM with phyCORE-Connectors on its underside.



**Figure 13. Pinout of the phyCORE-Connector**

Tables 7-10 provide an overview of the pinout of the phyCORE-Connector with signal names and descriptions specific to the phyCORE-AM62xx SOM as well as the processor ball it connects to, if any. An example of how this information

translates to our schematic is shown in *Figure 14*. The tables also discuss the appropriate voltage domain, signal type, and a description of the functionality. The signal type also includes information about the signal direction.



**Figure 14.** Pinout example using X\_VOUT0\_SYNC, top phyCORE-Connector, bottom the AM62xx SoC symbol

Most of the processor pins have multiple multiplexed functions. As most of these pins are connected directly to the phyCORE-Connector, the alternative functions are available by using the phyCORE-AM62xx SOM's pin multiplexing options. Signal names and descriptions in the following tables 7-10, however, are in regards to the specification of the phyCORE-AM62xx SOM schematic and may not line up with the functionality defined in the BSP. For information about pin multiplexing contact [PHYTEC Support](#). Please refer to the pinout tables in sections 5-12 to learn about alternative functions. To utilize a specific pin's alternative function, the corresponding registers must be configured within the appropriate driver of the BSP.

Some of the signals which are brought out on the phyCORE-Connector are used to configure the boot mode for specific boot options. These signals should not be driven by any device on the baseboard during reset unless that device is specifically being used to configure the boot pins. The signals that affect the boot configuration are labeled with "BOOTMODE" in the signal name. Details regarding these signals can be found under section [6.3 System Boot Configuration](#).

#### CAUTION:

The Texas Instruments AM62xx is a multi-voltage operated SoC and as such, special attention should be paid to the interface voltage levels to avoid unintentional damage to the SoC and other on-board components. Please ensure that all module connections do not exceed their expressed maximum voltage/current or drive power before the SOM is fully powered as damage from improper connections varies according to use and application.

**It is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.**

Please refer to the pinout tables at the end of this section as well as in the various interface sections [5-12](#) for more information about the operating characteristics. Refer to section [5.4 Power Sequencing](#) for more information about preventing damage from powering up too early.

## 4.8 Pinout Table

Table 7 phyCORE-AM62xx Connector X1, Column A Pinout

X1, Column A					
Pin	SOM Signal Name	Type	Level	Processor Ball	Description
A1	VIN	PWR_I	5.0V	-	Main Power Supply Input
A2	VIN	PWR_I	5.0V	-	Main Power Supply Input
A3	VIN	PWR_I	5.0V	-	Main Power Supply Input
A4	GND	-	-	-	Ground
A5	X_VOUT0_VSYNC	I/O	3.3V <sup>1</sup>	AC25	Video Output Vertical Sync
A6	X_VOUT0_HSYNC	I/O	3.3V <sup>1</sup>	AB24	Video Output Horizontal Sync
A7	X_VOUT0_PCLK	I/O	3.3V <sup>1</sup>	AC24	Video Output Pixel Clock Output
A8	X_VOUT0_DATA12	I/O	3.3V <sup>1</sup>	AB25	Video Output Data
A9	GND	-	-	-	Ground
A10	X_VOUT0_DATA13	I/O	3.3V <sup>1</sup>	AA24	Video Output Data
A11	X_VOUT0_DATA11	I/O	3.3V <sup>1</sup>	AA23	Video Output Data
A12	X_VOUT0_DATA14	I/O	3.3V <sup>1</sup>	Y22	Video Output Data
A13	X_VOUT0_DATA15	I/O	3.3V <sup>1</sup>	AA21	Video Output Data
A14	GND	-	-	-	Ground
A15	X_VOUT0_DE	I/O	3.3V <sup>1</sup>	Y20	Video Output Data Enable
A16	X_VOUT0_DATA10	I/O	3.3V <sup>1</sup>	V20	Video Output Data
A17	X_CPSW_RGMII2_RX_CTL	I/O	3.3V <sup>1</sup>	AD22	RGMII Receive Control
A18	X_CPSW_RGMII2_RXC	I/O	3.3V <sup>1</sup>	AD23	RGMII Receive Clock
A19	GND	-	-	-	Ground
A20	X_CPSW_RGMII2_RD3	I/O	3.3V <sup>1</sup>	AE22	RGMII Receive Data 3
A21	X_CPSW_RGMII2_RD2	I/O	3.3V <sup>1</sup>	AC21	RGMII Receive Data 2
A22	X_CPSW_RGMII2_RD1	I/O	3.3V <sup>1</sup>	AB20	RGMII Receive Data 1
A23	X_CPSW_RGMII2_RD0	I/O	3.3V <sup>1</sup>	AE23	RGMII Receive Data 0
A24	GND	-	-	-	Ground
A25	X_CPSW_RGMII2_TXC	I/O	3.3V <sup>1</sup>	AE21	RGMII Transmit Clock
A26	X_CPSW_RGMII2_TX_CTL	I/O	3.3V <sup>1</sup>	AA19	RGMII Transmit Control
A27	X_CPSW_RGMII2_TD0	I/O	3.3V <sup>1</sup>	Y18	RGMII Transmit Data 0
A28	X_CPSW_RGMII2_TD1	I/O	3.3V <sup>1</sup>	AA18	RGMII Transmit Data 1
A29	GND	-	-	-	Ground
A30	X_CPSW_RGMII2_TD2	I/O	3.3V <sup>1</sup>	AD21	RGMII Transmit Data 2
A31	X_CPSW_RGMII2_TD3	I/O	3.3V <sup>1</sup>	AC20	RGMII Transmit Data 3
A32	GND	-	-	-	Ground
A33	X_CSIO_RXP1	I	Differential	AE14	CSI Differential Receive Input (positive)
A34	X_CSIO_RXN1	I	Differential	AD14	CSI Differential Receive Input (negative)
A35	X_CSIO_RXP0	I	Differential	AC15	CSI Differential Receive Input (positive)
A36	X_CSIO_RXN0	I	Differential	AB14	CSI Differential Receive Input (negative)
A37	GND	-	-	-	Ground
A38	X_USB0_DM	I/O	Differential	AE11	USB 2.0 Differential Data (negative)
A39	X_USB0_DP	I/O	Differential	AD11	USB 2.0 Differential Data (positive)
A40	X_USB0_VBUS	A/I	5V	AC11	USB Level-shifted VBUS Input (resistor/diode network on SOM)
A41	X_USB0_DRVVBUS	I/O	3.3V <sup>1</sup>	C20	USB VBUS control output (active high)
A42	GND	-	-	-	Ground
A43	X_OLDIO_CLK0P	I/O	Differential	AE3	OLDI Differential Clock (positive)
A44	X_OLDIO_CLK0N	I/O	Differential	AD4	OLDI Differential Clock (negative)
A45	GND	-	-	-	Ground
A46	X_OLDIO_A2P	I/O	Differential	AA8	OLDI Differential Data (positive)

X1, Column A					
Pin	SOM Signal Name	Type	Level	Processor Ball	Description
A47	X_OLDIO_A2N	I/O	Differential	Y8	OLDI Differential Data (negative)
A48	X_OLDIO_A3P	I/O	Differential	AA7	OLDI Differential Data (positive)
A49	X_OLDIO_A3N	I/O	Differential	AB6	OLDI Differential Data (negative)
A50	GND	-	-	-	Ground
A51	X_OLDIO_A1N	I/O	Differential	AD3	OLDI Differential Data (negative)
A52	X_OLDIO_A1P	I/O	Differential	AB4	OLDI Differential Data (positive)
A53	X_OLDIO_A0N	I/O	Differential	AA5	OLDI Differential Data (negative)
A54	X_OLDIO_A0P	I/O	Differential	Y6	OLDI Differential Data (positive)
A55	GND	-	-	-	Ground
A56	X_WKUP_UART0_CTSN	I/O	3.3V <sup>1</sup>	C6	UART Clear to Send (active low)
A57	X_MCU_MCAN0_TX	I/O	3.3V <sup>1</sup>	D6	MCAN Transmit Data
A58	X_MCU_MCAN0_RX	I/O	3.3V <sup>1</sup>	B3	MCAN Receive Data
A59	X_MCU_MCAN1_TX	I/O	3.3V <sup>1</sup>	E5	MCAN Transmit Data
A60	X_MCU_MCAN1_RX	I/O	3.3V <sup>1</sup>	D4	MCAN Receive Data

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

Table 8 phyCORE-AM62xx Connector X1, Column B Pinout

X1, Column B					
Pin	Signal Name	Type	Level	Processor Ball	Description
B1	SoC_VDDSHV5_SDIO <sup>2</sup>	PWR_IO	3.3V	-	SD IO voltage
B2	VBAT	PWR_I	3.0V	-	Battery Backup Supply Input for RTC
B3	GND	-	-	-	Ground
B4	X_VOUT0_DATA2	I/O	3.3V <sup>1</sup>	W25	Video Output Data
B5	X_VOUT0_DATA3	I/O	3.3V <sup>1</sup>	W24	Video Output Data
B6	X_VOUT0_DATA1	I/O	3.3V <sup>1</sup>	V24	Video Output Data
B7	X_VOUT0_DATA4	I/O	3.3V <sup>1</sup>	Y25	Video Output Data
B8	GND	-	-	-	Ground
B9	X_VOUT0_DATA7	I/O	3.3V <sup>1</sup>	AA25	Video Output Data
B10	X_VOUT0_DATA5	I/O	3.3V <sup>1</sup>	Y24	Video Output Data
B11	X_VOUT0_DATA6	I/O	3.3V <sup>1</sup>	Y23	Video Output Data
B12	X_VOUT0_DATA0	I/O	3.3V <sup>1</sup>	U22	Video Output Data
B13	GND	-	-	-	Ground
B14	X_VOUT0_DATA9	I/O	3.3V <sup>1</sup>	W21	Video Output Data
B15	X_VOUT0_DATA8	I/O	3.3V <sup>1</sup>	V21	Video Output Data
B16	X_MDIO0_MDC	I/O	3.3V <sup>1</sup>	AD24	MDIO Clock (1.5K pullup on SOM)
B17	X_MDIO0_MDIO	I/O	3.3V <sup>1</sup>	AB22	MDIO Data (1.5K pullup on SOM)
B18	GND	-	-	-	Ground
B19	X_CPSW_ETH0_D-	I/O	Differential	-	Ethernet Data D Negative
B20	X_CPSW_ETH0_D+	I/O	Differential	-	Ethernet Data D Positive
B21	X_CPSW_ETH0_C-	I/O	Differential	-	Ethernet Data C Negative
B22	X_CPSW_ETH0_C+	I/O	Differential	-	Ethernet Data C Positive
B23	GND	-	-	-	Ground
B24	X_CPSW_ETH0_B-	I/O	Differential	-	Ethernet Data B Negative
B25	X_CPSW_ETH0_B+	I/O	Differential	-	Ethernet Data B Positive
B26	X_CPSW_ETH0_A-	I/O	Differential	-	Ethernet Data A Negative
B27	X_CPSW_ETH0_A+	I/O	Differential	-	Ethernet Data A Positive
B28	GND	-	-	-	Ground
B29	X_CPSW_ETH0_LED_LINK	O	3.3V	-	Ethernet LED Link Signal
B30	X_CPSW_ETH0_LED_ACTIVITY	O	3.3V	-	Ethernet LED Activity Signal
B31	X_CSIO_RXCLKP	I	Differential	AE15	CSI Differential Receive Clock Input (positive)

X1, Column B					
Pin	Signal Name	Type	Level	Processor Ball	Description
B32	X_CSIO_RXCLKN	I	Differential	AD15	CSI Differential Receive Clock Input (negative)
B33	GND	-	-	-	Ground
B34	X_CSIO_RXP2	I	Differential	AE13	CSI Differential Receive Input (positive)
B35	X_CSIO_RXN2	I	Differential	AD13	CSI Differential Receive Input (negative)
B36	X_CSIO_RXP3	I	Differential	AC13	CSI Differential Receive Input (positive)
B37	X_CSIO_RXN3	I	Differential	AB12	CSI Differential Receive Input (negative)
B38	GND	-	-	-	Ground
B39	X_USB1_DM	I/O	Differential	AD10	USB 2.0 Differential Data (negative)
B40	X_USB1_DP	I/O	Differential	AE9	USB 2.0 Differential Data (positive)
B41	X_USB1_VBUS	A/I	5V	AB10	USB Level-shifted VBUS Input (resistor/diode network on SOM)
B42	X_USB1_DRVVBUS	I/O	3.3V <sup>1</sup>	F18	USB VBUS control output (active high)
B43	GND	-	-	-	Ground
B44	X_OLDIO_A7N	I/O	Differential	AD8	OLDI Differential Data (negative)
B45	X_OLDIO_A7P	I/O	Differential	AE7	OLDI Differential Data (positive)
B46	X_OLDIO_A6P	I/O	Differential	AD7	OLDI Differential Data (positive)
B47	X_OLDIO_A6N	I/O	Differential	AE6	OLDI Differential Data (negative)
B48	GND	-	-	-	Ground
B49	X_OLDIO_A5N	I/O	Differential	AE5	OLDI Differential Data (negative)
B50	X_OLDIO_A5P	I/O	Differential	AD6	OLDI Differential Data (positive)
B51	X_OLDIO_A4N	I/O	Differential	AC6	OLDI Differential Data (negative)
B52	X_OLDIO_A4P	I/O	Differential	AC5	OLDI Differential Data (positive)
B53	GND	-	-	-	Ground
B54	X_OLDIO_CLK1P	I/O	Differential	AD5	OLDI Differential Clock (positive)
B55	X_OLDIO_CLK1N	I/O	Differential	AE4	OLDI Differential Clock (negative)
B56	GND	-	-	-	Ground
B57	X_WKUP_UART0_TXD	I/O	3.3V <sup>1</sup>	C5	UART Transmit Data
B58	X_WKUP_UART0_RXD	I/O	3.3V <sup>1</sup>	B4	UART Receive Data
B59	X_WKUP_UART0_RTSN	I/O	3.3V <sup>1</sup>	A4	UART Request to Send (active low)
B60	GND	-	-	-	Ground

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

<sup>2</sup>: More information about this signal can be found in section [5 Power](#).

Table 9 phyCORE-AM62xx Connector X1, Column C Pinout

X1, Column C					
Pin	Signal	Type	Level	Processor Ball	Description
C1	X_GPMCO_DIR	I/O	3.3V <sup>1</sup>	M22	GPMC Data Bus Signal Direction Control
C2	X_GPMCO_WAIT0	I/O	3.3V <sup>1</sup>	U23	GPMC External Indication of Wait
C3	X_GPMCO_CLK	I/O	3.3V <sup>1</sup>	P25	GPMC clock
C4	X_GPMCO_AD0/BOOTMODE_0 <sup>2</sup>	I/O	3.3V <sup>1</sup>	M25	GPMC Data 0 Input/Output (100K pullup on SOM)
C5	X_GPMCO_AD1/BOOTMODE_1 <sup>2</sup>	I/O	3.3V <sup>1</sup>	N23	GPMC Data 1 Input/Output (100K pullup on SOM)
C6	GND	-	-	-	Ground
C7	X_GPMCO_AD2/BOOTMODE_2 <sup>2</sup>	I/O	3.3V <sup>1</sup>	N24	GPMC Data 2 Input/Output (100K pulldown on SOM)
C8	X_GPMCO_AD3/BOOTMODE_3 <sup>2</sup>	I/O	3.3V <sup>1</sup>	N25	GPMC Data 3 Input/Output <sup>1</sup> (100K pullup on SOM)
C9	X_GPMCO_AD4/BOOTMODE_4 <sup>2</sup>	I/O	3.3V <sup>1</sup>	P24	GPMC Data 4 Input/Output <sup>1</sup> (100K pulldown on SOM)

X1, Column C					
Pin	Signal	Type	Level	Processor Ball	Description
C10	X_GPMCO_AD5/BOOTMODE_5 <sup>2</sup>	I/O	3.3V <sup>1</sup>	P22	GPMC Data 5 Input/Output (100K pulldown on SOM)
C11	X_GPMCO_AD6/BOOTMODE_6 <sup>2</sup>	I/O	3.3V <sup>1</sup>	P21	GPMC Data 6 Input/Output (100K pullup on SOM)
C12	GND	-	-	-	Ground
C13	X_GPMCO_WEn	I/O	3.3V <sup>1</sup>	L25	GPMC Write Enable (active low)
C14	X_GPMCO_CSn3	I/O	3.3V <sup>1</sup>	K24	GPMC Chip Select 3 (active low)
C15	X_GPMCO_ADVn_ALE	I/O	3.3V <sup>1</sup>	L23	GPMC Address Valid (active low) or Address Latch Enable
C16	X_GPMCO_BE0n_CLE	I/O	3.3V <sup>1</sup>	M24	GPMC Lower-Byte Enable (active low) or Command Latch Enable
C17	X_GPMCO_OEn_REn	I/O	3.3V <sup>1</sup>	L24	GPMC Output Enable (active low) or Read Enable (active low)
C18	X_GPMCO_BE1n	I/O	3.3V <sup>1</sup>	N20	GPMC Upper-Byte Enable (active low)
C19	GND	-	-	-	Ground
C20	X_MMC2_SD_CD	I/O	3.3V <sup>1</sup>	A23	SD Card Detect (10K pullup on SOM)
C21	X_MMC2_SD_WP	I/O	3.3V <sup>1</sup>	B23	SD Write Protect (10K pullup on SOM)
C22	X_MMC1_SD_WP	I/O	3.3V <sup>1</sup>	C17	SD Write Protect (10K pullup on SOM)
C23	X_MMC1_SD_CD	I/O	3.3V <sup>1</sup>	D17	SD card Detect (10K pullup on SOM)
C24	GND	-	-	-	Ground
C25	X_MMC1_DAT0	I/O	3.3V <sup>1</sup>	A22	MMC/SD/SDIO Data
C26	X_MMC1_DAT1	I/O	3.3V <sup>1</sup>	B21	MMC/SD/SDIO Data
C27	X_MCASP0_AXR2	I/O	3.3V <sup>1</sup>	A19	MCASP Serial Data
C28	X_MCASP0_AXR3	I/O	3.3V <sup>1</sup>	B19	MCASP Serial Data
C29	X_MCASP0_ACLK_X	I/O	3.3V <sup>1</sup>	B20	MCASP Transmit Bit Clock
C30	X_MCASP0_ACLK_R	I/O	3.3V <sup>1</sup>	A20	MCASP Receive Bit Clock
C31	GND	-	-	-	Ground
C32	X_I2C1_SCL	I/O	3.3V <sup>1</sup>	B17	I2C1 Clock
C33	X_I2C1_SDA	I/O	3.3V <sup>1</sup>	A17	I2C1 Data
C34	X_I2C0_SDA	I/O	3.3V <sup>1</sup>	A16	I2C0 Data (2.2K pullup on SOM)
C35	X_I2C0_SCL	I/O	3.3V <sup>1</sup>	B16	I2C0 Clock (2.2K pullup on SOM)
C36	X_MCAN0_TX	I/O	3.3V <sup>1</sup>	C15	MCAN Transmit Data
C37	X_MCAN0_RX	I/O	3.3V <sup>1</sup>	E15	MCAN Receive Data
C38	GND	-	-	-	Ground
C39	X_RTC_INT	I/O	3.3V <sup>1</sup>	D16	RTC Interrupt (10K pullup on SOM)
C40	X_SPI0_CS0	I/O	3.3V <sup>1</sup>	A13	SPI Chip Select 0
C41	X_SPI0_CS1	I/O	3.3V <sup>1</sup>	C13	SPI Chip Select 1
C42	X_TCK	I	3.3V <sup>1</sup>	A10	JTAG Test Clock Input (10K pullup on SOM)
C43	GND	-	-	-	Ground
C44	X_TDI	I	3.3V <sup>1</sup>	A11	JTAG Test Data Input (10K pullup on SOM)
C45	X_TMS	I	3.3V <sup>1</sup>	B11	JTAG Test Mode Select Input (10K pullup on SOM)
C46	X_TDO	O	3.3V <sup>1</sup>	D12	JTAG Test Data Output
C47	X_TRST_N	I	3.3V <sup>1</sup>	B10	JTAG Reset (10K pulldown)
C48	GND	-	-	-	Ground
C49	X_MCU_I2C0_SCL	I/O	3.3V <sup>1</sup>	A8	MCU I2C0 Clock
C50	X_MCU_I2C0_SDA	I/O	3.3V <sup>1</sup>	D10	MCU I2C0 Data
C51	X_PMIC_EN	I	5V	-	PMIC power enable (100k pullup on SOM)
C52	X_nRESET_IN	I	3.3V	-	Reset input (active low, 10K pullup, 100nF cap on SOM)
C53	GND	-	-	-	Ground
C54	X_PGOOD	OD-O	3.3V	-	Power good output (100K pullup on SOM)

X1, Column C					
Pin	Signal	Type	Level	Processor Ball	Description
C55	X MCU RESETSTATz	I/O	3.3V <sup>1</sup>	B12	MCU Domain warm reset status output (10K pulldown on SOM)
C56	X MCU RESETz	I	3.3V <sup>1</sup>	E11	MCU Domain warm reset (100K pullup on SOM)
C57	X PORz_OUT	O	3.3V <sup>1</sup>	E21	Main Domain POR status output (1.5K pulldown on SOM)
C58	X RESET REQz	I	3.3V <sup>1</sup>	F20	Main Domain external warm reset request input (100K pullup on SOM)
C59	GND	-	-	-	Ground
C60	X EXT REFCLK1	I/O	3.3V <sup>1</sup>	A18	External clock input to Main Domain

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

<sup>2</sup>: This signal should not be driven during reset. More information can be found in section [6.3 System Boot Configuration](#).

**Table 10 phyCORE-AM62xx Connector X1, Column D Pinout**

X2, Column D					
Pin	Signal	Type	Level	Processor Ball	Description
D1	X_GPMCO_AD7/BOOTMODE_7 <sup>2</sup>	I/O	3.3V <sup>1</sup>	R23	GPMC Data 7 Input/Output (100K pulldown on SOM)
D2	X_GPMCO_AD8/BOOTMODE_8 <sup>2</sup>	I/O	3.3V <sup>1</sup>	R24	GPMC Data 8 Input/Output (100K pullup on SOM)
D3	GND	-	-	-	Ground
D4	X_GPMCO_AD9/BOOTMODE_9 <sup>2</sup>	I/O	3.3V <sup>1</sup>	R25	GPMC Data 9 Input/Output (100K pullup on SOM)
D5	X_GPMCO_AD10/BOOTMODE_10 <sup>2</sup>	I/O	3.3V <sup>1</sup>	T25	GPMC Data 10 Input/Output (100K pullup on SOM)
D6	X_GPMCO_AD11/BOOTMODE_11 <sup>2</sup>	I/O	3.3V <sup>1</sup>	R21	GPMC Data 11 Input/Output (100K pulldown on SOM)
D7	X_GPMCO_AD12/BOOTMODE_12 <sup>2</sup>	I/O	3.3V <sup>1</sup>	T22	GPMC Data 12 Input/Output (100K pullup on SOM)
D8	X_GPMCO_AD13/BOOTMODE_13 <sup>2</sup>	I/O	3.3V <sup>1</sup>	T24	GPMC Data 13 Input/Output (100K pullup on SOM)
D9	GND	-	-	-	Ground
D10	X_GPMCO_AD14/BOOTMODE_14 <sup>2</sup>	I/O	3.3V <sup>1</sup>	U25	GPMC Data 14 Input/Output (100K pulldown on SOM)
D11	X_GPMCO_AD15/BOOTMODE_15 <sup>2</sup>	I/O	3.3V <sup>1</sup>	U24	GPMC Data 15 Input/Output (100K pulldown on SOM)
D12	X_GPMCO_CSn0	I/O	3.3V <sup>1</sup>	M21	GPMC Chip Select 0 (active low)
D13	X_GPMCO_CSn1	I/O	3.3V <sup>1</sup>	L21	GPMC Chip Select 1 (active low)
D14	X_GPMCO_CSn2	I/O	3.3V <sup>1</sup>	K22	GPMC Chip Select 2 (active low)
D15	X_GPMCO_WPn	I/O	3.3V <sup>1</sup>	K25	GPMC Flash Write Protect (active low)
D16	X_GPMCO_WAIT1	I/O	3.3V <sup>1</sup>	V25	GPMC External Indication of Wait
D17	GND	-	-	-	Ground
D18	X_MMC2_CLK	I/O	3.3V <sup>1</sup>	D25	MMC/SD/SDIO Clock (49.9K pulldown on SOM)
D19	X_MMC2_CMD	I/O	3.3V <sup>1</sup>	C24	MMC/SD/SDIO Command
D20	X_MMC2_DAT0	I/O	3.3V <sup>1</sup>	B24	MMC/SD/SDIO Data
D21	X_MMC2_DAT1	I/O	3.3V <sup>1</sup>	C25	MMC/SD/SDIO Data
D22	GND	-	-	-	Ground
D23	X_MMC2_DAT3	I/O	3.3V <sup>1</sup>	D24	MMC/SD/SDIO Data
D24	X_MMC2_DAT2	I/O	3.3V <sup>1</sup>	E23	MMC/SD/SDIO Data
D25	X_MMC1_CMD	I/O	3.3V <sup>1</sup>	A21	MMC/SD/SDIO Command
D26	X_MMC1_CLK	I/O	3.3V <sup>1</sup>	B22	MMC/SD/SDIO Clock (49.9K pulldown on SOM)

X2, Column D					
Pin	Signal	Type	Level	Processor Ball	Description
D27	GND	-	-	-	Ground
D28	X_MMC1_DAT2	I/O	3.3V <sup>1</sup>	C21	MMC/SD/SDIO Data
D29	X_MMC1_DAT3	I/O	3.3V <sup>1</sup>	D22	MMC/SD/SDIO Data
D30	X_MCASPO_AFSX	I/O	3.3V <sup>1</sup>	D20	MCASP Transmit Frame Sync
D31	X_MCASPO_AXR1	I/O	3.3V <sup>1</sup>	B18	MCASP Serial Data (Input/Output)
D32	X_MCASPO_AFSR	I/O	3.3V <sup>1</sup>	E19	MCASP Receive Frame Sync
D33	X_MCASPO_AXRO	I/O	3.3V <sup>1</sup>	E18	MCASP Serial Data (Input/Output)
D34	GND	-	-	-	Ground
D35	X_UART0_RTSN	I/O	3.3V <sup>1</sup>	B15	UART Request to Send (active low)
D36	X_UART0_CTSN	I/O	3.3V <sup>1</sup>	A15	UART Clear to Send (active low)
D37	X_UART0_RXD	I/O	3.3V <sup>1</sup>	D14	UART Receive Data
D38	X_UART0_TXD	I/O	3.3V <sup>1</sup>	E14	UART Transmit Data
D39	GND	-	-	-	Ground
D40	X_SPI0_CLK	I/O	3.3V <sup>1</sup>	A14	SPI Clock
D41	X_SPI0_D0	I/O	3.3V <sup>1</sup>	B13	SPI Data 0
D42	X_SPI0_D1	I/O	3.3V <sup>1</sup>	B14	SPI Data 1
D43	X_EMU0 <sup>3</sup>	I/O	3.3V <sup>1</sup>	E12	Emulation Control 0 (5.76K pullup)
D44	X_EMU1 <sup>3</sup>	I/O	3.3V <sup>1</sup>	C11	Emulation Control 1 (5.76K pullup)
D45	GND	-	-	-	Ground
D46	X MCU SPI0 CLK	I/O	3.3V <sup>1</sup>	A7	SPI Clock
D47	X MCU SPI0_D0	I/O	3.3V <sup>1</sup>	D9	SPI Data 0
D48	X MCU SPI0_D1	I/O	3.3V <sup>1</sup>	C9	SPI Data 1
D49	X MCU SPI0_CS1	I/O	3.3V <sup>1</sup>	B8	SPI Chip Select 1
D50	X_WKUP_I2C0_SCL	I/O	3.3V <sup>1</sup>	B9	WKUP I2C0 Clock
D51	X_WKUP_I2C0_SDA	I/O	3.3V <sup>1</sup>	A9	WKUP I2C0 Data
D52	GND	-	-	-	Ground
D53	X MCU UART0_CTSN	I/O	3.3V <sup>1</sup>	A6	UART Clear to Send (active low)
D54	X MCU UART0_RTSN	I/O	3.3V <sup>1</sup>	B6	UART Request to Send (active low)
D55	X MCU UART0_RXD	I/O	3.3V <sup>1</sup>	B5	UART Receive Data
D56	X MCU UART0_TXD	I/O	3.3V <sup>1</sup>	A5	UART Transmit Data
D57	GND	-	-	-	Ground
D58	X_RESETSTAT <sub>z</sub>	O	3.3V <sup>1</sup>	F22	Main Domain warm reset status output (10K pulldown on SOM)
D59	X MCU SAFETY_ERRORn	I/O	1.8V	D1	Error Signal Output
D60	X_WKUP_CLKOUT0	I/O	3.3V <sup>1</sup>	A12	WKUP Domain CLKOUT0 output

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

<sup>2</sup>: This signal should not be driven during reset. More information can be found in section [6.3 System Boot Configuration](#).

<sup>3</sup>: The signal brought out at this pin is controlled by a jumper. Refer to section [4.6 Solder Jumpers](#) for details.

## 4.9 Thermal Management

Thermal management is necessary to ensure proper operation of the phyCORE-AM62xx SOM, especially when integrated inside of an enclosure as the AM62xx processor generates considerable heat.

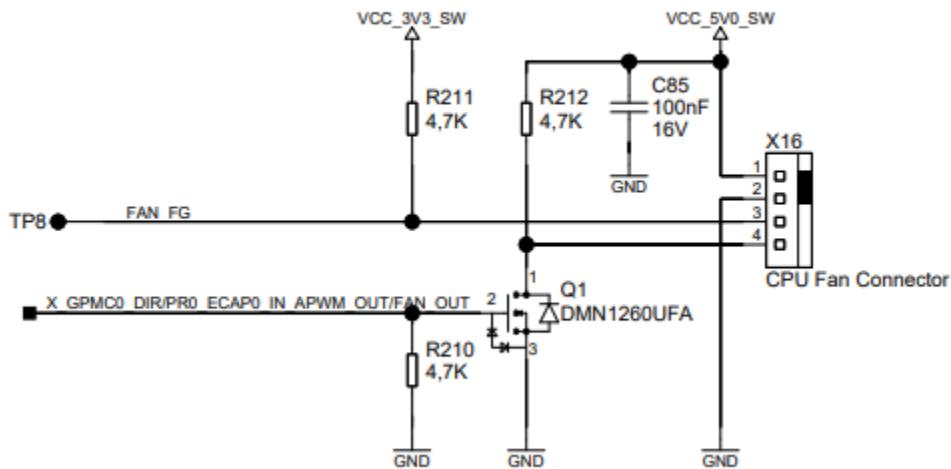
The phyCORE-AM62xx has a temperature rating of -40C to 85C. PHYTEC has found that a fan and a heatsink help prevent overheating at the higher end of the phyCORE-AM62xx's temperature operating range (during our temperature testing

the SOM would experience overheating shutdowns above 75C without an active cooling system). The following parts are used to attach the fan to the phyCORE-AM62xx SOM processor and to connect the fan power cable to the connector on the PHYTEC phyCORE-AM62xx Carrier Board:

**Table 11 Thermal Management Parts**

Recommended Thermal Component	Part Number
Heatsink	BDN10-3CB/A01
5VDC Fan	CFM-2510B-0100-218-22
Fan Connector	47054-1000
4x Fan Crimping Terminals	0850-0113
Carrier Board Connector	47053-1000
3x #4 5/8" Screws	90190A112

The heatsink is mounted on top of the processor with heatsink adhesive. Then the crimping terminals are crimped to the exposed fan wires, which allows the fan to be mounted to the 5-pin connector that mates with the PHYTEC Carrier board. Finally, the fan is secured to the heatsink with screws. The PHYTEC Carrier Board supplies 5V power to the fan via the 47053-1000 connector. The fan circuit on the AM62xx Carrier Board is shown below and allows for user control over the fan.



**Figure 15. Fan design reference circuit**

## 4.10 Layout Guidelines

### 4.10.1 High-Speed Differential Signal Routing Guidelines

#### Spacing

- Implement proper trace width and spacing to yield the recommended differential impedance value.

- Spacing between the differential pairs and other traces should be at least twice the distance between the inter-pair spacing.
- Avoid routing high-speed signals near other sensitive circuits (such as crystals, oscillators, switching regulators, clock signals, etc.).

### Routing

- Route the two traces of a differential pair on the same layer(s).
- Route signals over an adjacent, solid ground reference plane. Ensure there are no layers between the routing layer and reference layer.
- Avoid routing across a gap or cut-out in the reference plane or across different reference planes. Cuts in the reference plane should be avoided in general.
- Avoid sharp bends on differential lanes.
- Minimize total trace length.
- Keep the length of the two traces in a differential pair as close as possible. Recommended length matching is listed in the various Design In Guide sub-sections contain in this document as well as the length of the traces on the SOM. This information can be used to further correct or avoid worsening any SOM trace length mismatches in your own design.

### Vias and Stubs

- Avoid routing through vias when possible. The number of vias on the differential pairs should be minimized. If necessary, each signal of the differential pair should be routed through matching number of vias. In the case of multiple differential lanes in the same interface, all lines should have the same number of vias.
- Minimize discontinuities on the signal path (such as stubs) and avoid placing test points, external components like  $0\Omega$  resistors, or any other components that are not required when possible.
- Surface-mount receptacles are preferred over through-hole connectors, as signals can be routed on the top layer of the PCB without introducing vias to the signal path. If through-hole pins are necessary, it may be beneficial to route signals on the bottom layer.

## 4.10.2 General Signal Routing Guidelines

- Pay special attention to signal placement, trace impedances, maximum trace length, and trace length tolerances when routing SOM signals.
- Place and route high-speed signals, such as CSI, OLDI, Ethernet, etc. before placing and routing any other interfaces. This is recommended to ensure that the stricter trace lengths and length matching requirements of these interfaces are met.

- Place and route the remaining interfaces after the high-speed interfaces are completely routed.
- All communication signals/interfaces should have an accompanying solid reference plane.
- Separate clocks and other high-speed signals as much as possible from nearby traces to reduce crosstalk. A general rule is to use a clearance of at least 3 times the trace width.

## 5 Power

The following sub-sections discuss the power configuration of the phyCORE-AM62xx in detail. [Table 12](#) summarizes the relationships between the voltage rails and the devices on the phyCORE-AM62xx SOM.

**Table 12 External Supply Voltages**

Signal	Direction	Power Draw / Deliver	Pins	Description
VIN	I	Draw 5W (1A)	A1, A2, A3	5.0V Main Power Supply
VBAT	I	Draw 120 nW (40nA)	B2	Backup Power for RTC
SoC_VDDSHV5_SDIO	O	Deliver 1.32W (400mA)	B1	This rail can be used as a pullup voltage for the SD/MMC1 signals. The level of SoC_VDDSHV5_SDIO is driven by VSEL_SD to either 3.3V or 1.8V.
GND	O	None	A4, A9, A14, A19, A24, A29, A32, A37, A42, A45, A50, A55, B3, B8, B13, B18, B23, B28, B33, B38, B43, B48, B53, B56, B60, C6, C12, C19, C24, C31, C38, C43, C48, C53, C59, D3, D9, D17, D22, D27, D34, D39, D45, D52, D57	Ground

### 5.1 Primary System Power (VIN)

The phyCORE-AM62xx SOM operates from a primary voltage supply (VIN) with a nominal value of +5V. On-board PMIC and switching regulators generate the additional voltage supplies required by the phyCORE-AM62xx and on-board components from VIN supplied to the SOM.

For proper operation, the phyCORE-AM62xx SOM must be supplied with a voltage source of 5V ( $\pm 5\%$ ) with a minimum 1A capacity at the VIN pins on the phyCORE-Connector. These pins are A1, A2, and A3 on the X1 connector. In testing the current draw of the SOM did not exceed 1A, but it is important to perform a power analysis to determine how much current your complete system (both SOM and custom CB) requires. The phyCORE-AM62xx Carrier Board provides an easy access current shunt to measure SOM current under various operating conditions as part of your system power analysis. The reference designator of the shunt is R492 and has a value of 15 m $\Omega$  (and a size of 1206). Use the maximum measured SOM current combined with the current requirement for your carrier board peripheral devices to design your power system appropriately.

Connect all +5V VIN input pins to your power supply and all ground pins to ground.

#### 5.1.1 Primary Power Reference Circuit

An example reference circuit for powering the SOM is shown below.

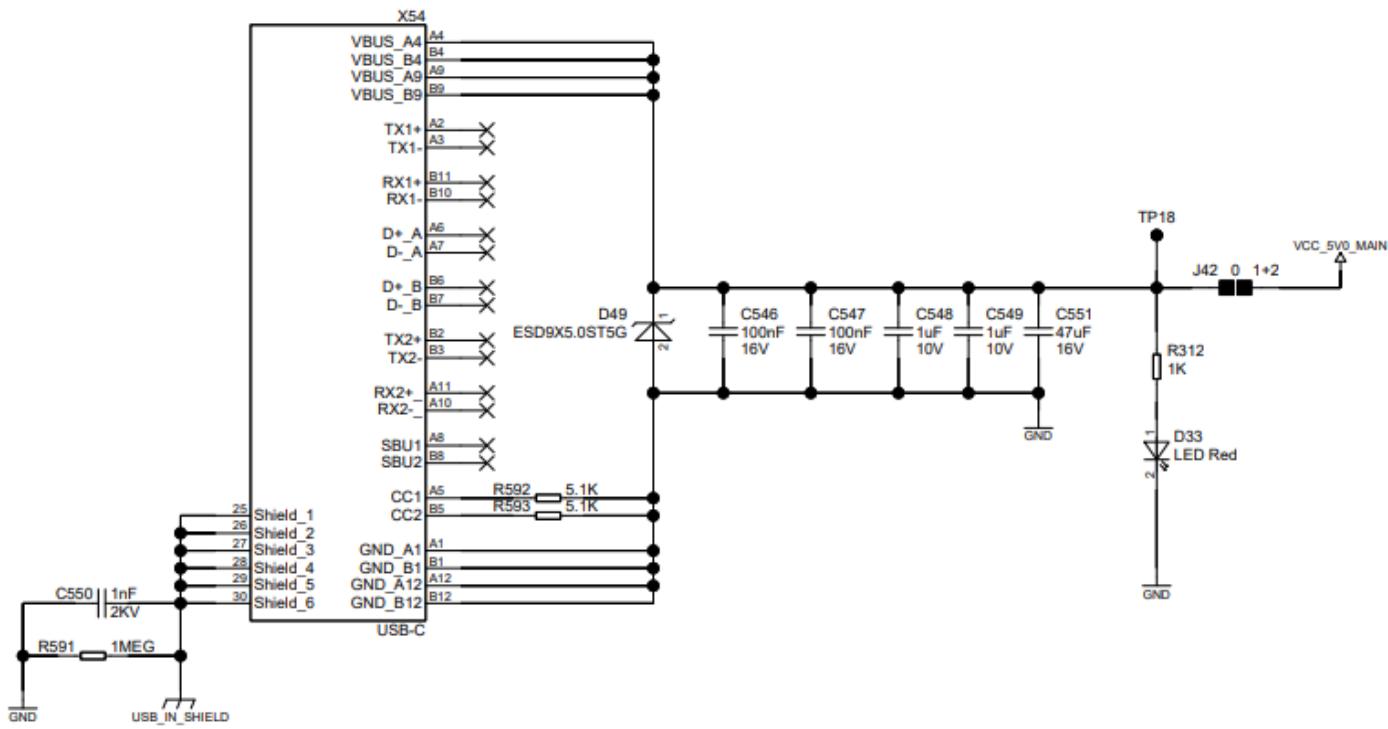


Figure 16. Primary Power VIN(VCC\_5V0\_MAIN) reference circuit

The circuit consists of:

- A USB-C connector for connecting an external USB-C power cable to the system
- A diode circuit (D49) that will trip in case of an overload preventing damage to the rest of the circuit

The reference circuits below showcase additional functionality that can be added to the primary power circuit. [Figure 17](#) is a circuit for measuring the input current to the SOM. It contains:

- A small resistor (R492) that the current is measured across
- A connector to connect to a current measurement board

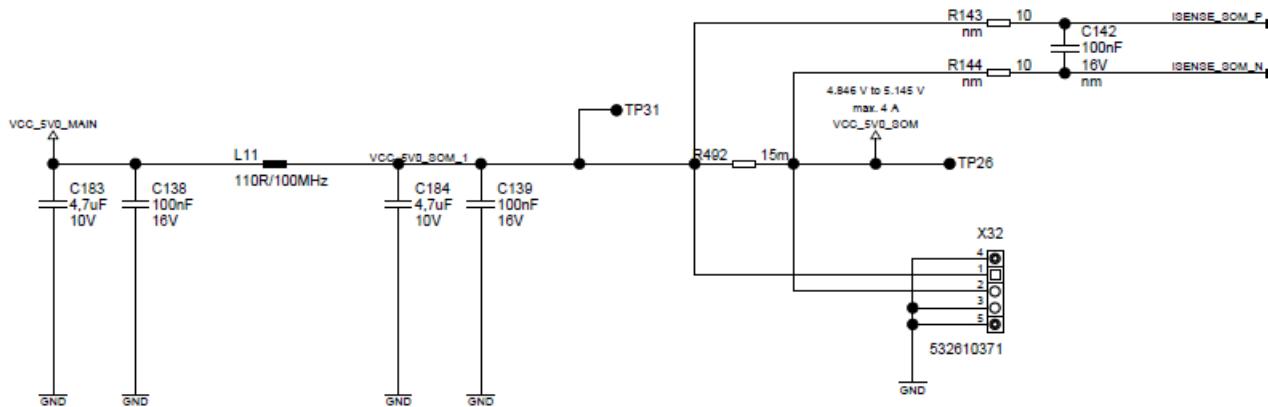


Figure 17. SOM current reader reference circuit

*Figure 18* is an alternative input power for industrial applications. It also contains a protection circuit that prevents overloads in current/voltage from damaging the SOM. It contains:

- A phoenix connector for connecting a 5V external power source to the system
- A fuse/diode circuit (F1/D5) that will trip in case of an overload preventing damage to the rest of the circuit
- A transistor network that provides reverse polarity protection

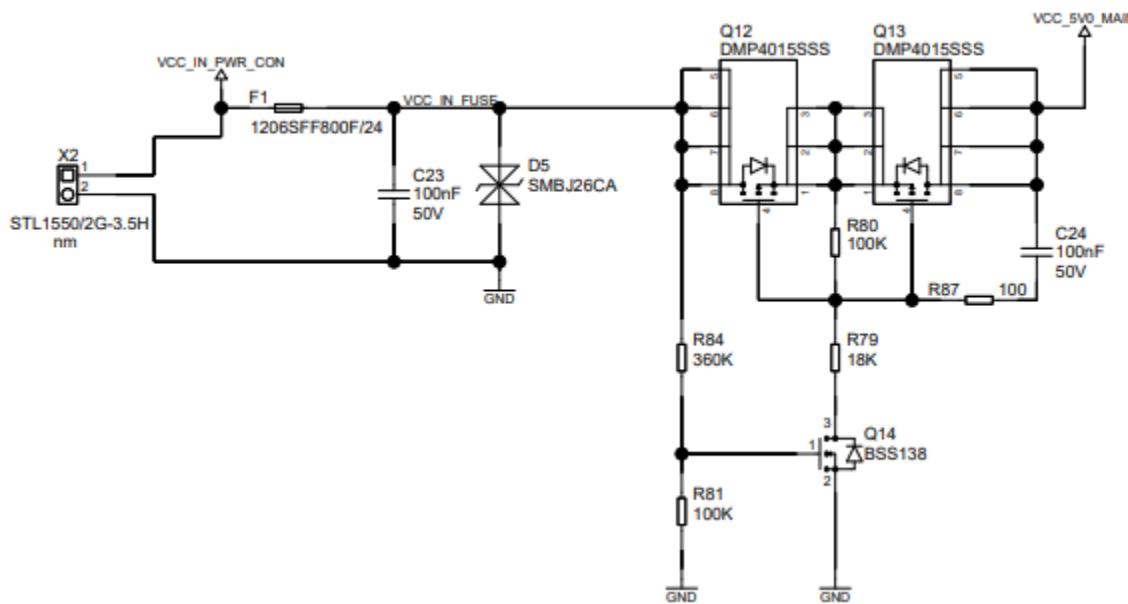


Figure 18. Phoenix connector power input with overload protection reference circuit

## 5.2 Backup Power (VBAT)

To keep the Real-Time Clock (RTC) module running, a secondary voltage source of 1.2-5.5V can be supplied to the phyCORE-AM62xx SOM at the VBAT pin (pin B2 of phyCORE-Connector X1). For the RTC to maintain time when main system power is removed, the VBAT input must be supplied with power. PHYTEC recommends using either a battery or a large gold cap capacitor (220mF or larger) for powering VBAT. The RTC draws 40 nA at 3V and is the only draw on VBAT. For more information regarding the recommended operating voltage of the Backup Power Source VBAT, refer to [Table 4](#).

## 5.3 Reset

Several reset inputs and outputs are accessible at the phyCORE-Connector as listed in [Table 13](#) below. The X\_nRESET\_IN, X MCU\_RESETz, and X\_RESET\_REQz signals can be driven low to trigger cold/warm resets of different domains without cycling power on the carrier board. We recommend designing reset buttons into your system that will tie the reset signals

to ground when pressed, allowing for manual control over system reset. These buttons can later be depopulated for production purposes but are generally useful during board bring up and verification.

The X\_PMIC\_EN signal is connected to the enable pin of the PMIC and will prevent the PMIC from starting when pulled low. The X\_MCU\_RESETSTAT<sub>z</sub>, X\_RESETSTAT<sub>z</sub>, X\_POR<sub>z</sub>\_OUT, and X\_PGOOD signals are status outputs. PGOOD indicates when the SOM power is stable and X\_MCU\_RESETSTAT<sub>z</sub> / X\_RESETSTAT<sub>z</sub> / X\_POR<sub>z</sub>\_OUT are status outputs for X\_MCU\_RESET<sub>z</sub> / X\_RESET\_REQ<sub>z</sub> / X\_nRESET\_IN respectively.

Most of the reset signals are connected to pullups/pulldowns (X\_nRESET\_IN also has an attached capacitor) so pullups/pulldowns are not needed on custom CBs for these signals. This information is in [Table 13](#) as well as shown in the figure below.

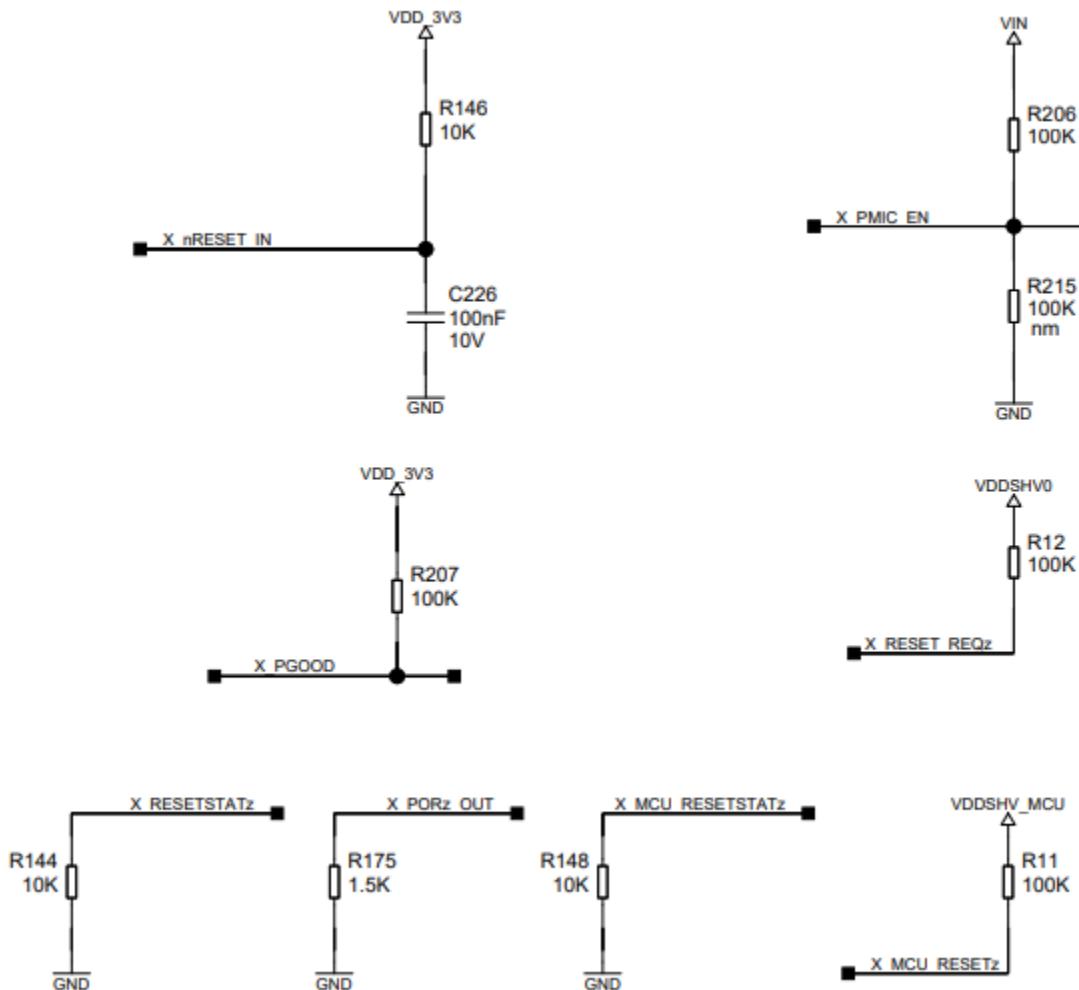


Figure 19. Reset signals pullups, pulldowns, and capacitors

**Table 13** Reset Pin Description

X1 Pin #	Signal	Type	Level	Description
C51	X_PMIC_EN (100K pullup on SOM)	I	5V	Enable pin for PMIC
C52	X_nRESET_IN (10K pullup, 100nF cap on SOM)	I	3.3V	Cold system Reset
C56	X MCU_RESETz (100K pullup on SOM)	I	3.3V <sup>1</sup>	Warm Reset of MCU Domain
C58	X_RESET_REQz (100K pullup on SOM)	I	3.3V <sup>1</sup>	Warm Reset of MAIN Domain
C55	X MCU_RESETSTATz (10K pulldown on SOM)	O	3.3V <sup>1</sup>	MCU Domain Reset Status Output
C57	X PORz_OUT (1.5K pulldown on SOM)	O	3.3V <sup>1</sup>	Cold Reset Status Output
D58	X RESETSTATz (10K pulldown on SOM)	O	3.3V <sup>1</sup>	MAIN Domain Reset Status Output
C54	X_PGOOD (100K pullup on SOM)	OD-O	3.3V	SOM/PMIC Power Good Status Output
D44	X_VPP_EN <sup>2</sup>	I	3.3V	Enable pin for VPP rail

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details

<sup>2</sup>: The signal brought out at this pin is controlled by a jumper. Refer to section [4.6 Solder Jumpers](#) for details

## 5.4 Power Sequencing

It is mandatory to avoid driving the I/O pins of the phyCORE-AM62xx SOM when the SOM is not fully powered up. Prematurely driving the pins may cause current to flow through the I/O pins before the processor is properly powered, potentially resulting in damage or unknown behavior after power-up or reset. Therefore, the peripheral carrier board power should be switched on/enabled by the X\_PGOOD signal to avoid powering external peripherals and circuits that directly interface with the phyCORE-AM62xx SOM I/Os until their respective voltage domains are powered. X\_PGOOD is a 3.3V level signal that is pulled high once the PMIC has finished its power sequencing and the SOM has been powered on. This should be used to sequence the baseboard power supplies (3.3V, 1.8V, etc.). This ensures that the I/O domains on the SOM are powered before any external circuits or peripherals drive power to the processor pins. To accomplish this, it is recommended to integrate load switches to turn on the peripheral voltage rails after the SOM has finished powering up. An example of this is shown in the reference circuit below.

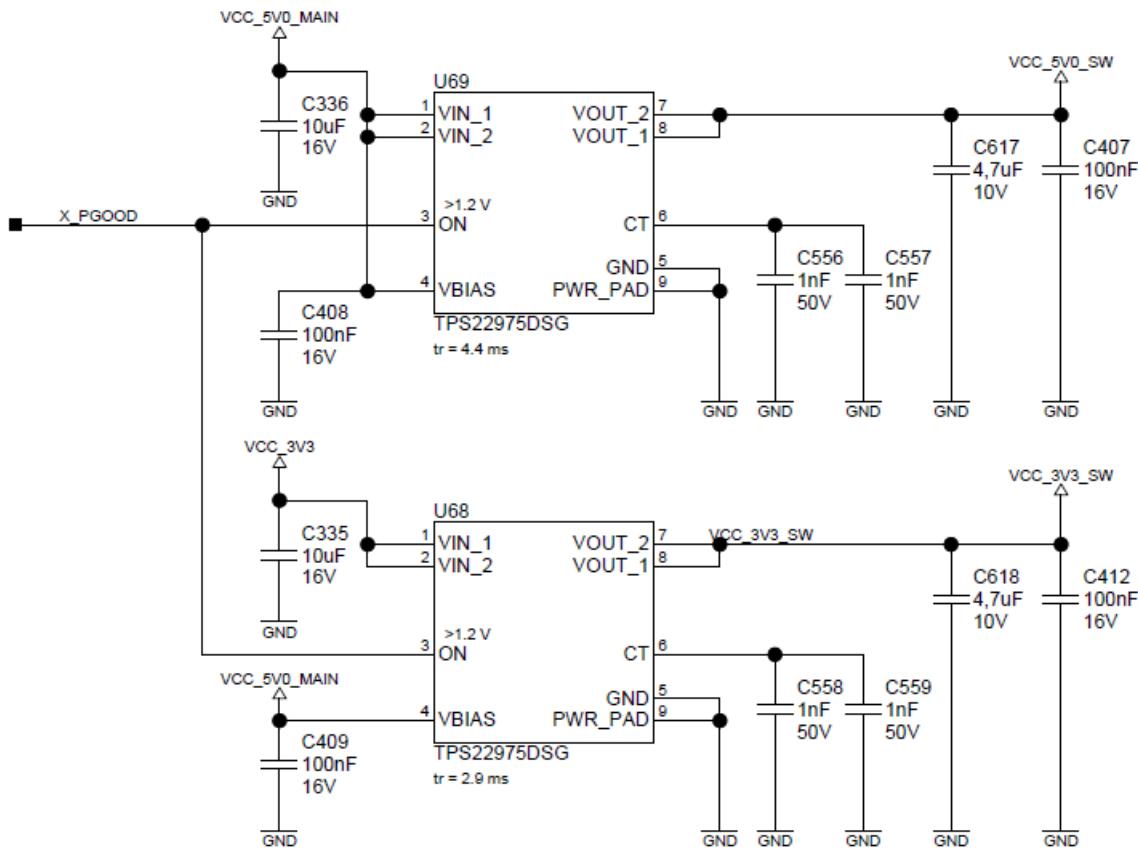


Figure 20. Carrier board power reference circuit

## 5.5 Safe Shutdown and Sudden Power Loss

Like a PC, a sudden power loss can result in a corrupted filesystem that renders your system unable to boot. When possible, initiating an OS controlled shutdown procedure is advised. Under Linux a poweroff or shutdown command will safely shutdown the system, allowing subsequent safe removal of power.

If sudden power loss is a concern in your system, then consider designing a battery backup or other similar failsafe solution. An appropriate battery backup provides enough temporary power for the system to complete a safe shutdown. The safe shutdown should be triggered via an interrupt to the processor when primary system power loss is detected. Another solution is to have a read-only file system as this would ensure nothing is modified in an unexpected manner in the event of an unexpected shutdown.

## 6 System Memory

The following sub-sections detail each memory type supported on the phyCORE-AM62xx as well as how to configure which memory system to boot from. This section is split into memories populated on the SOM and potential CB memory interfaces.

## 6.1 SOM Memory

### 6.1.1 DDR4 RAM

The RAM on the phyCORE-AM62xx is comprised of one DDR4 SDRAM chip for a 16-bit wide interface providing up to 4GB of SDRAM which can run at up to 1600MT/s. These chips are connected to the dedicated DDR subsystem of the AM62xx processor. Typically, the DDR4 SDRAM initialization is performed by a bootloader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or bootloader, SDRAM must be initialized through the appropriate SDRAM configuration registers on the AM62xx processor. Refer to the [AM62xx Technical Reference Manual](#) about accessing and configuring these registers. Contact our sales team for information on the available DDR4 population options: <https://PHYTEC.com/contact/>

### 6.1.2 EEPROM

The phyCORE-AM62xx is populated with one nonvolatile 4KB EEPROM with an I<sup>2</sup>C interface. This memory can be used to store configuration data or other general-purpose data. The device is accessed through the I<sup>2</sup>C0 on the AM62xx at address 0x50.

### 6.1.3 eMMC Flash

An eMMC flash device is populated on the SOM as a programmable nonvolatile storage. The eMMC flash is connected to the MMC0 8-bit interface of the phyCORE-AM62xx which supports the JEDEC eMMC electrical standard v5.1. Contact our sales team for information on the available eMMC population options: <https://PHYTEC.com/contact/>

### 6.1.4 OSPI

An Octal Serial Peripheral Interface (OSPI) Flash is populated on the SOM as a programmable nonvolatile storage. The OSPI interface supports single, dual, quad, or octal read/write access to the flash device. The OSPI Flash can be used for a fast boot. Contact our sales team for information on the available OSPI population options: <https://PHYTEC.com/contact/>

Some of the OSPI signals on the SOM are worth noting since their use on the SOM either does not match their processor ball name or are used for an entirely different circuit. OSPI0\_CS<sub>n</sub>3 is used for the OSPI reset, OSPI0\_CS<sub>n</sub>1 is used as the EEPROM WP pin, and OSPI2\_CS<sub>n</sub> is connected to the OSPI interrupt pin and the heartbeat LEDs discussed in section [12.5 Heartbeat LEDs](#). This information is also shown in the figure below.

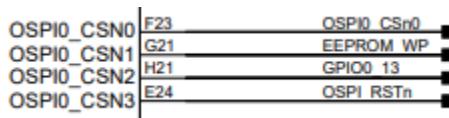


Figure 21. OSPI0 CS<sub>n</sub> signal use

## 6.2 External Memory Bus

### 6.2.1 GPMC

The General-Purpose Memory Control (GPMC) module can be used as a data path to an external memory device. The GPMC can support:

- An asynchronous or synchronous 8-bit memory or device (non-burst device)
- An asynchronous or synchronous 16-bit memory or device
- A 16-bit non-multiplexed NOR Flash device
- A 16-bit address and data multiplexed NOR Flash device
- An 8-bit and 16-bit NAND flash device
- A 16-bit pseudo-SRAM device

**Table 14 GPMC Signal Connections at the phyCORE-Connector**

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
GPMCO_ADVn_ALE	C15	X_GPMCO_ADVn_ALE	O	3.3V <sup>1</sup>	GPMC Address Valid (active low) or Address Latch Enable
GPMCO_CLK	C3	X_GPMCO_CLK	O	3.3V <sup>1</sup>	GPMC clock
GPMCO_DIR	C1	X_GPMCO_DIR	O	3.3V <sup>1</sup>	GPMC Data Bus Signal Direction Control
GPMCO_OEn_REn	C17	X_GPMCO_OEn_REn	O	3.3V <sup>1</sup>	GPMC Output Enable (active low) or Read Enable (active low)
GPMCO_WEn	C13	X_GPMCO_WEn	O	3.3V <sup>1</sup>	GPMC Write Enable (active low)
GPMCO_WPn	D15	X_GPMCO_WPn	O	3.3V <sup>1</sup>	GPMC Flash Write Protect (active low)
GPMCO_A0	B12	X_VOUT0_DATA0	O	3.3V <sup>1</sup>	GPMC Address 0 Output
GPMCO_A1	B6	X_VOUT0_DATA1	O	3.3V <sup>1</sup>	GPMC Address 1 Output
GPMCO_A2	B4	X_VOUT0_DATA2	O	3.3V <sup>1</sup>	GPMC Address 2 Output
GPMCO_A3	B5	X_VOUT0_DATA3	O	3.3V <sup>1</sup>	GPMC Address 3 Output
GPMCO_A4	B7	X_VOUT0_DATA4	O	3.3V <sup>1</sup>	GPMC Address 4 Output
GPMCO_A5	B10	X_VOUT0_DATA5	O	3.3V <sup>1</sup>	GPMC Address 5 Output
GPMCO_A6	B11	X_VOUT0_DATA6	O	3.3V <sup>1</sup>	GPMC Address 6 Output
GPMCO_A7	B9	X_VOUT0_DATA7	O	3.3V <sup>1</sup>	GPMC Address 7 Output
GPMCO_A8	B15	X_VOUT0_DATA8	O	3.3V <sup>1</sup>	GPMC Address 8 Output
GPMCO_A9	B14	X_VOUT0_DATA9	O	3.3V <sup>1</sup>	GPMC Address 9 Output
GPMCO_A10	A16	X_VOUT0_DATA10	O	3.3V <sup>1</sup>	GPMC Address 10 Output
GPMCO_A11	A11	X_VOUT0_DATA11	O	3.3V <sup>1</sup>	GPMC Address 11 Output
GPMCO_A12	A8	X_VOUT0_DATA12	O	3.3V <sup>1</sup>	GPMC Address 12 Output
GPMCO_A13	A10	X_VOUT0_DATA13	O	3.3V <sup>1</sup>	GPMC Address 13 Output
GPMCO_A14	A12	X_VOUT0_DATA14	O	3.3V <sup>1</sup>	GPMC Address 14 Output
GPMCO_A15	A13	X_VOUT0_DATA15	O	3.3V <sup>1</sup>	GPMC Address 15 Output
GPMCO_A16	A6	X_VOUT0_HSYNC	O	3.3V <sup>1</sup>	GPMC Address 16 Output
GPMCO_A17	A15	X_VOUT0_DE	O	3.3V <sup>1</sup>	GPMC Address 17 Output
GPMCO_A18	A5	X_VOUT0_VSYNC	O	3.3V <sup>1</sup>	GPMC Address 18 Output
GPMCO_A19	A7	X_VOUT0_PCLK	O	3.3V <sup>1</sup>	GPMC Address 19 Output

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
GPMCO_A20	C14	X_GPMCO_CSn3	O	3.3V <sup>1</sup>	GPMC Address 20 Output
GPMCO_A21	D16	X_GPMCO_WAIT1	O	3.3V <sup>1</sup>	GPMC Address 21 Output
GPMCO_A22	D15	X_GPMCO_WPn	O	3.3V <sup>1</sup>	GPMC Address 22 Output
GPMCO_AD0	C4	X_GPMCO_ADO/BOOTMODE_0 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 0 Input/Output
GPMCO_AD1	C5	X_GPMCO_AD1/BOOTMODE_1 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 1 Input/Output
GPMCO_AD2	C7	X_GPMCO_AD2/BOOTMODE_2 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 2 Input/Output
GPMCO_AD3	C8	X_GPMCO_AD3/BOOTMODE_3 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 3 Input/Output
GPMCO_AD4	C9	X_GPMCO_AD4/BOOTMODE_4 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 4 Input/Output
GPMCO_AD5	C10	X_GPMCO_AD5/BOOTMODE_5 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 5 Input/Output
GPMCO_AD6	C11	X_GPMCO_AD6/BOOTMODE_6 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 6 Input/Output
GPMCO_AD7	D1	X_GPMCO_AD7/BOOTMODE_7 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 7 Input/Output
GPMCO_AD8	D2	X_GPMCO_AD8/BOOTMODE_8 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 8 Input/Output
GPMCO_AD9	D4	X_GPMCO_AD9/BOOTMODE_9 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 9 Input/Output
GPMCO_AD10	D5	X_GPMCO_AD10/BOOTMODE_10 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 10 Input/Output
GPMCO_AD11	D6	X_GPMCO_AD11/BOOTMODE_11 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 11 Input/Output
GPMCO_AD12	D7	X_GPMCO_AD12/BOOTMODE_12 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 12 Input/Output
GPMCO_AD13	D8	X_GPMCO_AD13/BOOTMODE_13 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 13 Input/Output
GPMCO_AD14	D10	X_GPMCO_AD14/BOOTMODE_14 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 14 Input/Output
GPMCO_AD15	D11	X_GPMCO_AD15/BOOTMODE_15 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	GPMC Data 15 Input/Output
GPMCO_BE0n_CLE	C16	X_GPMCO_BE0n_CLE	O	3.3V <sup>1</sup>	GPMC Lower-Byte Enable (active low) or Command Latch Enable
GPMCO_BE1n	C18	X_GPMCO_BE1n	O	3.3V <sup>1</sup>	GPMC Upper-Byte Enable (active low)
GPMCO_CSn0	D12	X_GPMCO_CSn0	O	3.3V <sup>1</sup>	GPMC Chip Select 0 (active low)
GPMCO_CSn1	D13	X_GPMCO_CSn1	O	3.3V <sup>1</sup>	GPMC Chip Select 1 (active low)
GPMCO_CSn2	D14	X_GPMCO_CSn2	O	3.3V <sup>1</sup>	GPMC Chip Select 2 (active low)
GPMCO_CSn3	C14	X_GPMCO_CSn3	O	3.3V <sup>1</sup>	GPMC Chip Select 3 (active low)
GPMCO_WAIT0	C2	X_GPMCO_WAIT0	I	3.3V <sup>1</sup>	GPMC External Indication of Wait
GPMCO_WAIT1	D16	X_GPMCO_WAIT1	I	3.3V <sup>1</sup>	GPMC External Indication of Wait

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

<sup>2</sup>: This signal should not be driven during reset. More information can be found in section [6.3 System Boot Configuration](#).

## 6.2.2 SD/MMC/SDIO

The AM62xx processor provides three Secure Digital/MultiMedia Card interfaces as MMC0, MMC1, and MMC2. Only MMC1(SDIO) and MMC2 are accessible at the phyCORE-Connector as the MMC0 interface is connected to the on-board eMMC. The MMC1/MMC2 ports provides a 4-bit wide data bus that supports SD Host Controller Standard Specification 4.10, SD Physical Layer Specification v3.01, and SDIO Specification v3.00.

### 6.2.2.1 MMC Pinout

**Table 15 MMC Connections at the phyCORE-Connector**

SOM Signal(s)	X1 Pin #(s)	Type	Level	Description
X_MMC1_SDCD (10K pullup on SOM)	C23	I	3.3V <sup>1</sup>	MMC1 Card Detection
X_MMC1_SDWP (10K pullup on SOM)	C22	I	3.3V <sup>1</sup>	MMC1 Write Protect
X_MMC1_DAT3	D29	I/O	3.3V <sup>1</sup>	MMC1 Data 3
X_MMC1_DAT2	D28	I/O	3.3V <sup>1</sup>	MMC1 Data 2
X_MMC1_DAT1	C26	I/O	3.3V <sup>1</sup>	MMC1 Data 1
X_MMC1_DAT0	C25	I/O	3.3V <sup>1</sup>	MMC1 Data 0
X_MMC1_CLK (49.9K pulldown on SOM)	D26	I/O	3.3V <sup>1</sup>	MMC1 Clock
X_MMC1_CMD	D25	I/O	3.3V <sup>1</sup>	MMC1 Command
X_MMC2_SDCD (10K pullup on SOM)	D36	I	3.3V <sup>1</sup>	MMC2 Card Detection
	C20			
	C32			
X_MMC2_SDWP (10K pullup on SOM)	C33	I	3.3V <sup>1</sup>	MMC2 Write Protect
	D35			
	C21			
X_MMC2_DAT3	D23	I/O	3.3V <sup>1</sup>	MMC2 Data 3
X_MMC2_DAT2	D24	I/O	3.3V <sup>1</sup>	MMC2 Data 2
X_MMC2_DAT1	D21	I/O	3.3V <sup>1</sup>	MMC2 Data 1
X_MMC2_DAT0	D20	I/O	3.3V <sup>1</sup>	MMC2 Data 0
X_MMC2_CLK (49.9K pulldown on SOM)	D18	I/O	3.3V <sup>1</sup>	MMC2 Clock
X_MMC2_CMD	D19	I/O	3.3V <sup>1</sup>	MMC2 Command

<sup>1</sup>: The voltage level for these signals is configurable between 1.8V and 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details

### 6.2.2.2 MMC Design In Considerations

- MMC signals should be length matched within 12700 µm as described in [Table 16](#).
- Keep MMC trace lengths as short as possible.
- Route the MMC clock with enough clearance from other signals, when possible, to reduce crosstalk. A general rule is to use a clearance of at least 3 times the trace width.

- It is recommended to place series termination resistors ( $22\Omega$  or similar is recommended) near the SD card reader/WIFI module on the data and command signals.
- SD card power should be connected to a 3.3V power supply regardless of the MMC IO voltage level.
- SD card power needs to be toggled with on board power reset.

**Table 16** phyCORE-AM62xx MMC1 Layout Characteristics

Signal Name	SOM Trace Length ( $\mu\text{m}$ )	Length Matching ( $\mu\text{m}$ )	Single Ended Impedance ( $\Omega$ )
X_MMC1_DAT3	9066	12700	50
X_MMC1_DAT2	7923		
X_MMC1_DAT1	10031		
X_MMC1_DAT0	10574		
X_MMC1_CLK	9372		
X_MMC1_CMD	8260		
X_MMC2_DAT3	9427	12700	50
X_MMC2_DAT2	7428		
X_MMC2_DAT1	7787		
X_MMC2_DAT0	7112		
X_MMC2_CLK	9515		
X_MMC2_CMD	7418		

### 6.2.2.3 MMC Reference Circuit

Two reference circuits using MMC are shown in the figures below. The first connects the MMC1 signals to a micro-SD card reader for use as either a data transfer device or a boot device.

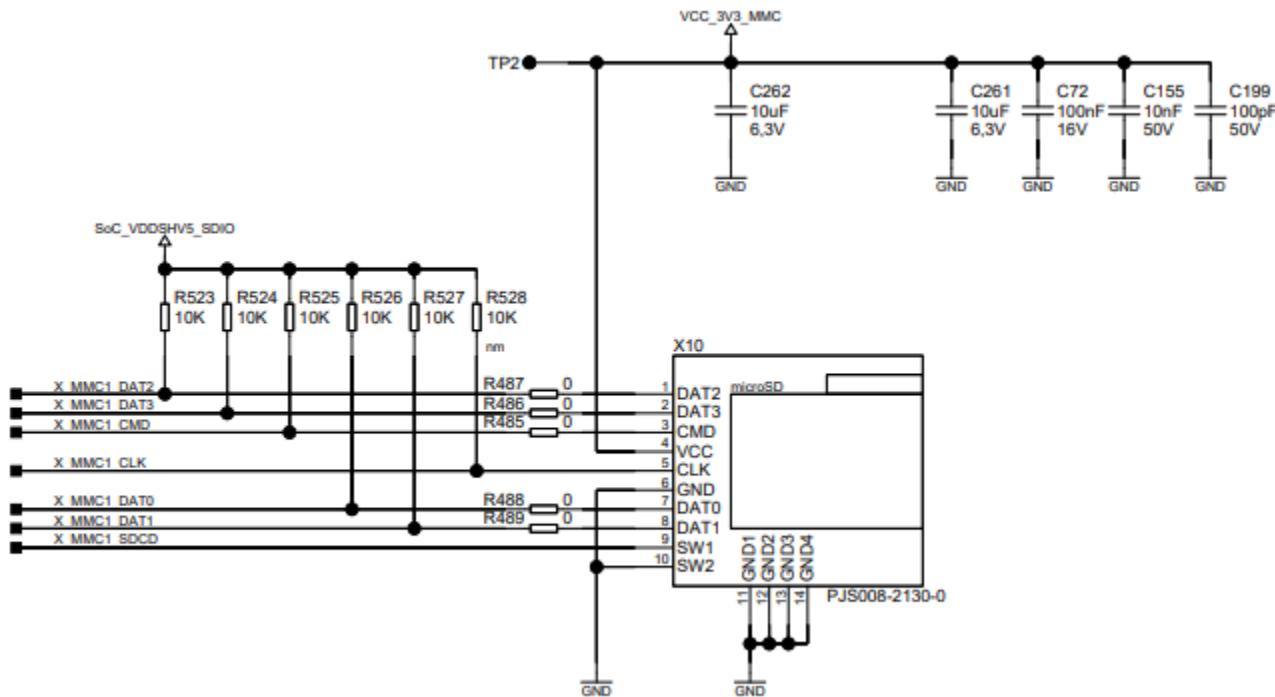


Figure 22. MMC1 SD-card Reader Reference Schematic

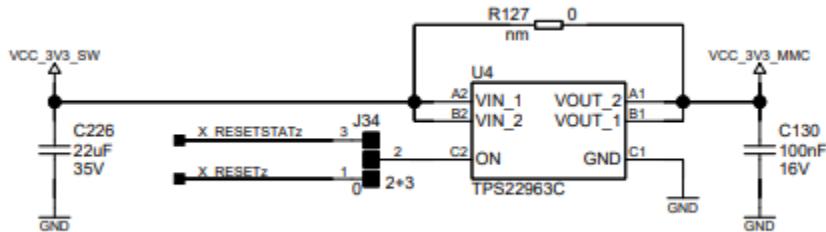


Figure 23. MMC1 Load Switch Reference Schematic

The circuit consists of:

- An SD-card reader with CMD/DATA line pullups
- A load switch

The second reference circuit connects MMC2 to a E key M.2 connector for use in WIFI/BT applications.

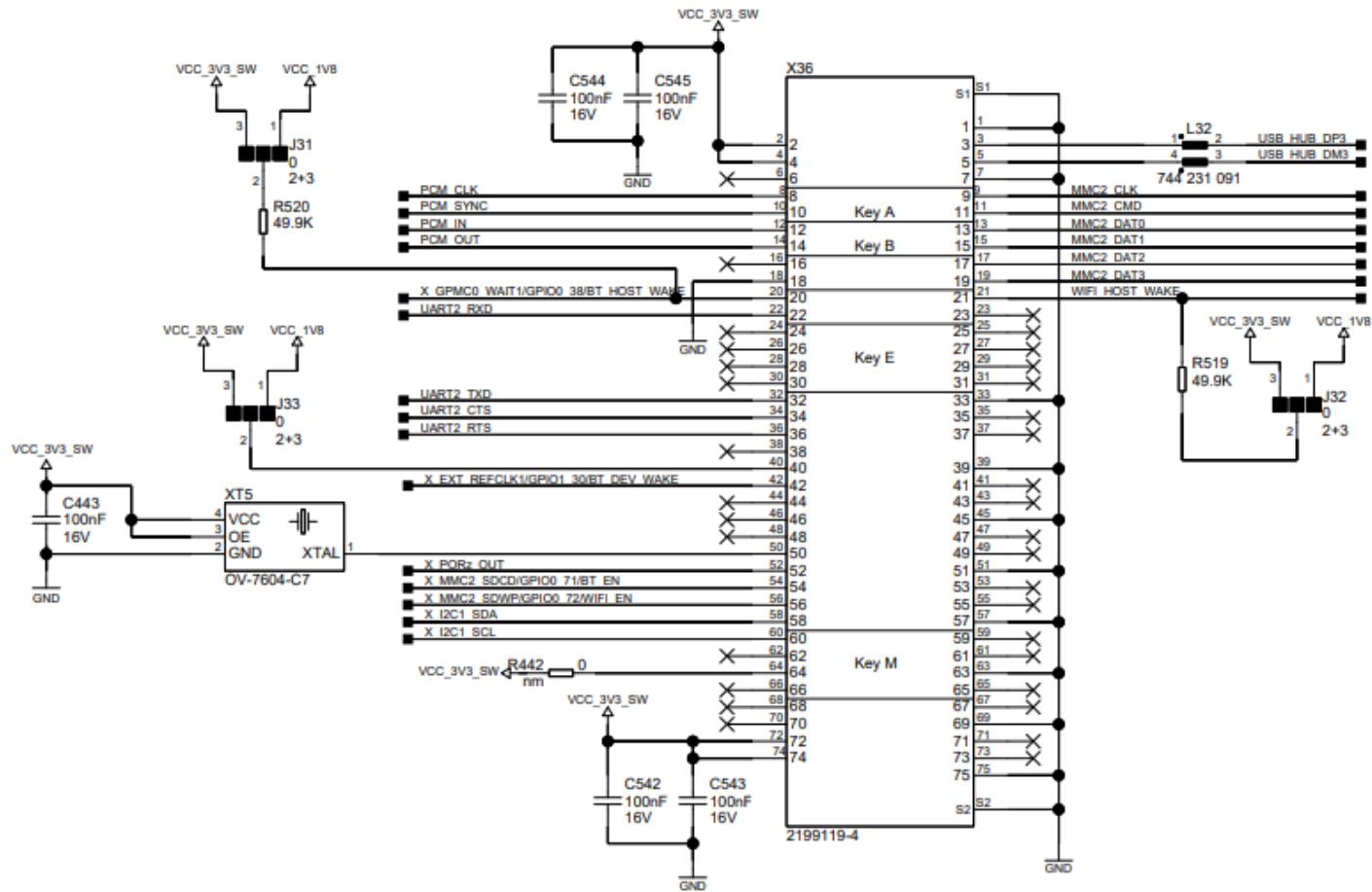


Figure 24. M.2 WIFI MMC2 Connector Reference Schematic

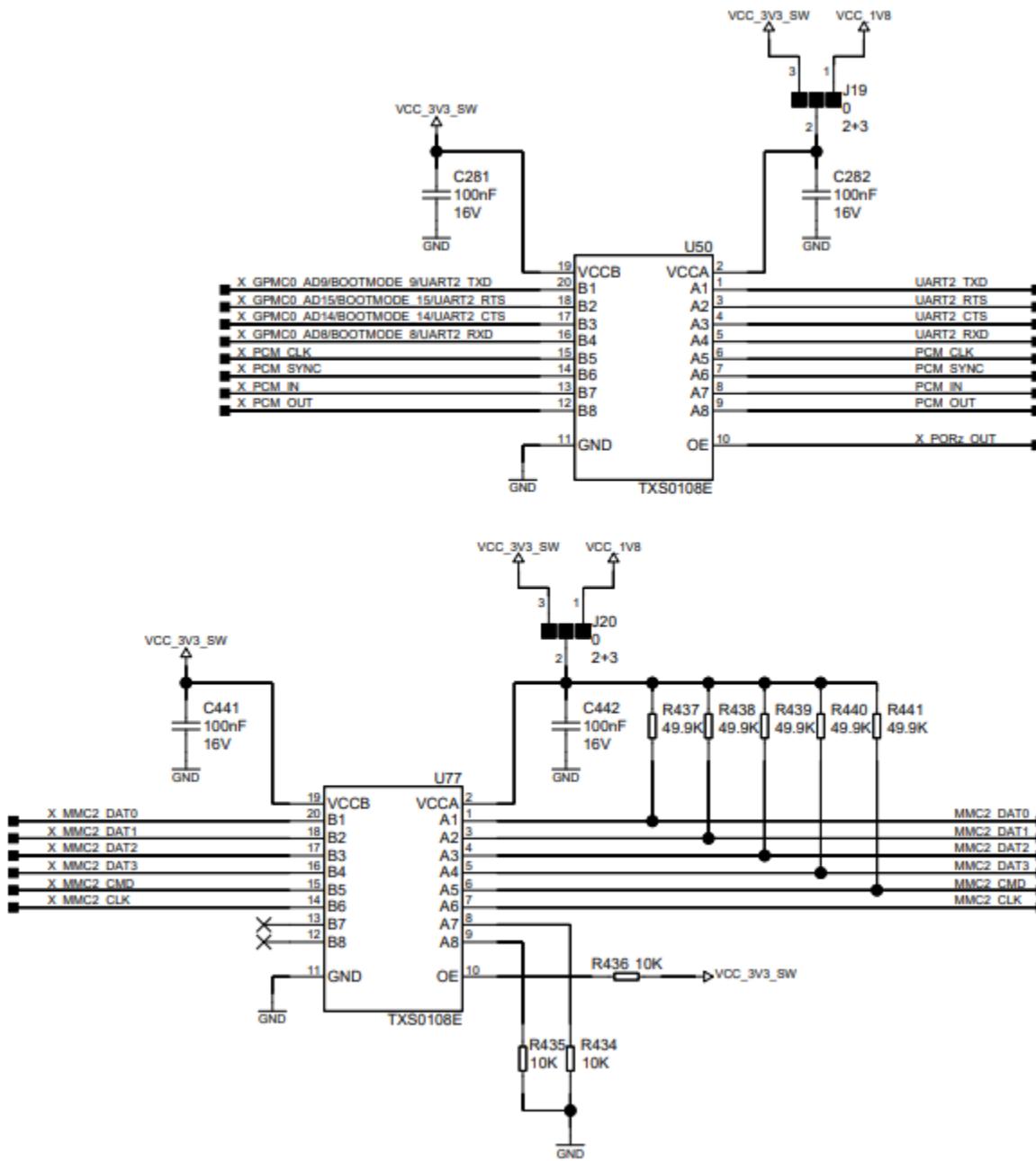


Figure 25. M.2 WIFI MMC2 Level Translators Reference Schematic

The circuit consists of:

- A E key M.2 connector to connect to a module
- Two voltage translators that serve as buffers for the bootmode signals as well allowing the module to operate at either 3.3V or 1.8V.
- A 32.768KHz oscillator

## 6.3 System Boot Configuration

Although most features of the phyCORE-AM62xx SOM are configured or programmed during the initialization routine, other features which impact program execution must be configured prior to initialization via pin termination. During the power-on reset cycle, the operational system boot mode of the phyCORE-AM62xx SOM is determined by the configuration of the BOOTMODE [15:0] signals. The BOOTMODE signals must be held at the desired configuration until X\_PORz\_OUT goes high to be properly latched into the system. For development and debugging purposes, the BOOTMODE pins are available at the phyCORE-Connector and are named X\_GPMC0\_AD#/BOOTMODE#. These signals are strapped to default values using on-board resistors, the populations of which are shown in [Figure 26. Table 17](#) below lists the various BOOTMODE configurations as well as the default configuration on the SOM, which is to boot from eMMC with SD card as a backup. Further BOOTMODE options are discussed in the [AM62xx Technical Reference Manual](#).

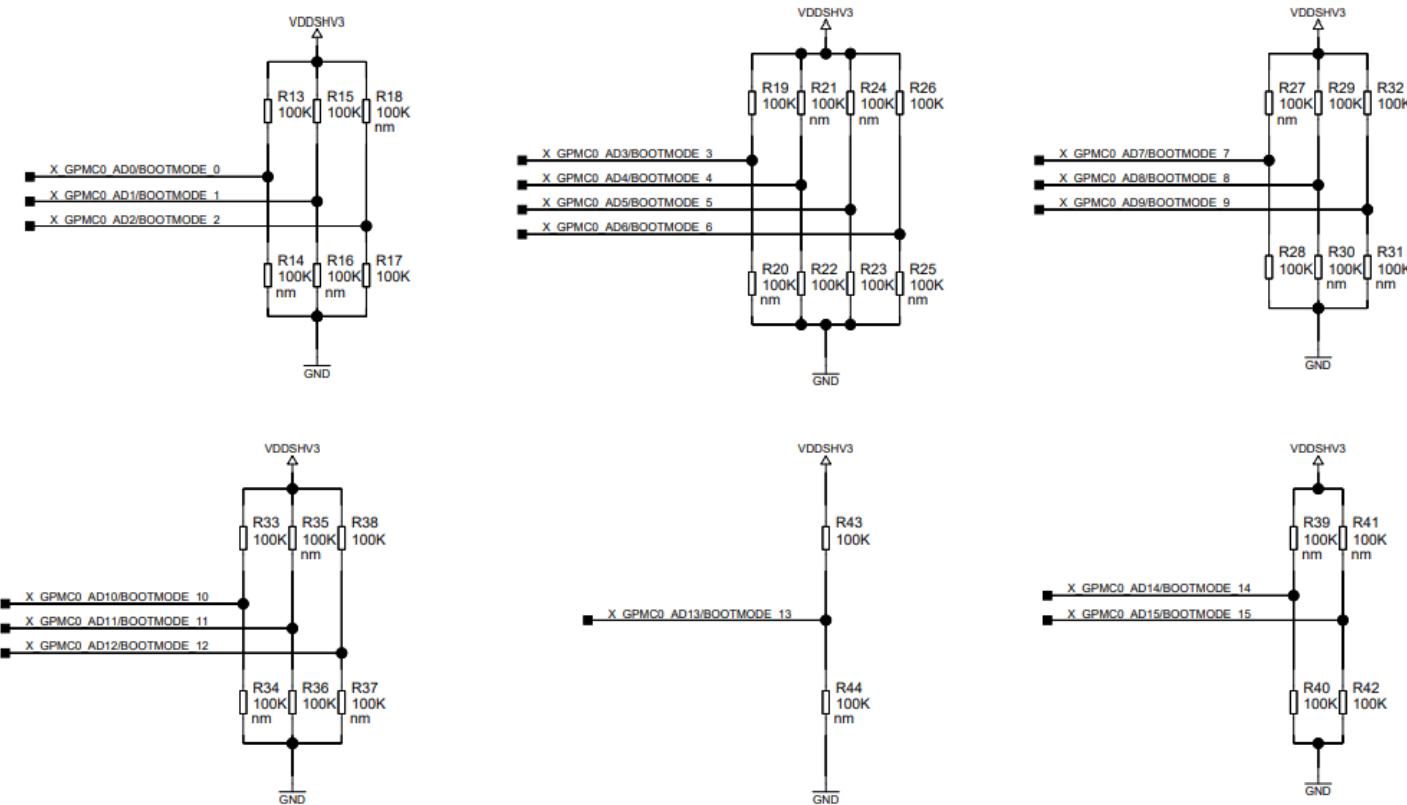


Figure 26. BOOTMODE pullups/pulldowns

**Table 17** BOOTMODE Description

<b>BOOTMODE pins</b>	<b>Description</b>	<b>Pin Settings</b>	<b>Pin Behavior</b>
BOOTMODE[15:14]	Reserved by the processor	XX	None
BOOTMODE[13:10]	Backup boot mode selection	X000	None
		0001	USB device mode
		1001	USB host mode
		X011	UART
		0100	Ethernet RGMII with internal TX delay
		1100	Ethernet RMII with external clock source
		0101	MMC0
		1101 (Default)	MMC1
		X110	SPI
		X111	I <sup>2</sup> C
BOOTMODE[9:3]	Primary boot mode selection and config	X00_0001	OSPI boot, Iclock is external, Boot flash is off
		X01_0001	OSPI boot, Iclock is internal, Boot flash is off
		X10_0001	OSPI boot, Iclock is external, Boot flash is on
		X11_0001	OSPI boot, Iclock is internal, Boot flash is on
		0XX_1001 (Default)	eMMC boot
		1X0_1000	SDIO boot in filesystem mode
		1X1_1000	SDIO boot in raw mode
		000	19.2 MHz
BOOTMODE[2:0]	PLL Reference Clock selection	001	20 MHz
		010	24 MHz
		011 (Default)	25 MHz
		100	26 MHz
		101	27 MHz

1: X means the pin is reserved by the processor and must be tied either high or low. The direction doesn't matter as long as the pin is not left floating.

To modify the default boot configuration on a custom carrier board, it is recommended to use 1kΩ pull-up resistors or 10kΩ pull-down resistors to override the SOM settings. For startup/verification testing, PHYTEC recommends designing the boot configuration circuit to include a DIP switch. This will make it easy to swap between various boot modes (an example circuit is shown below). This DIP switch can then be de-populated for production.

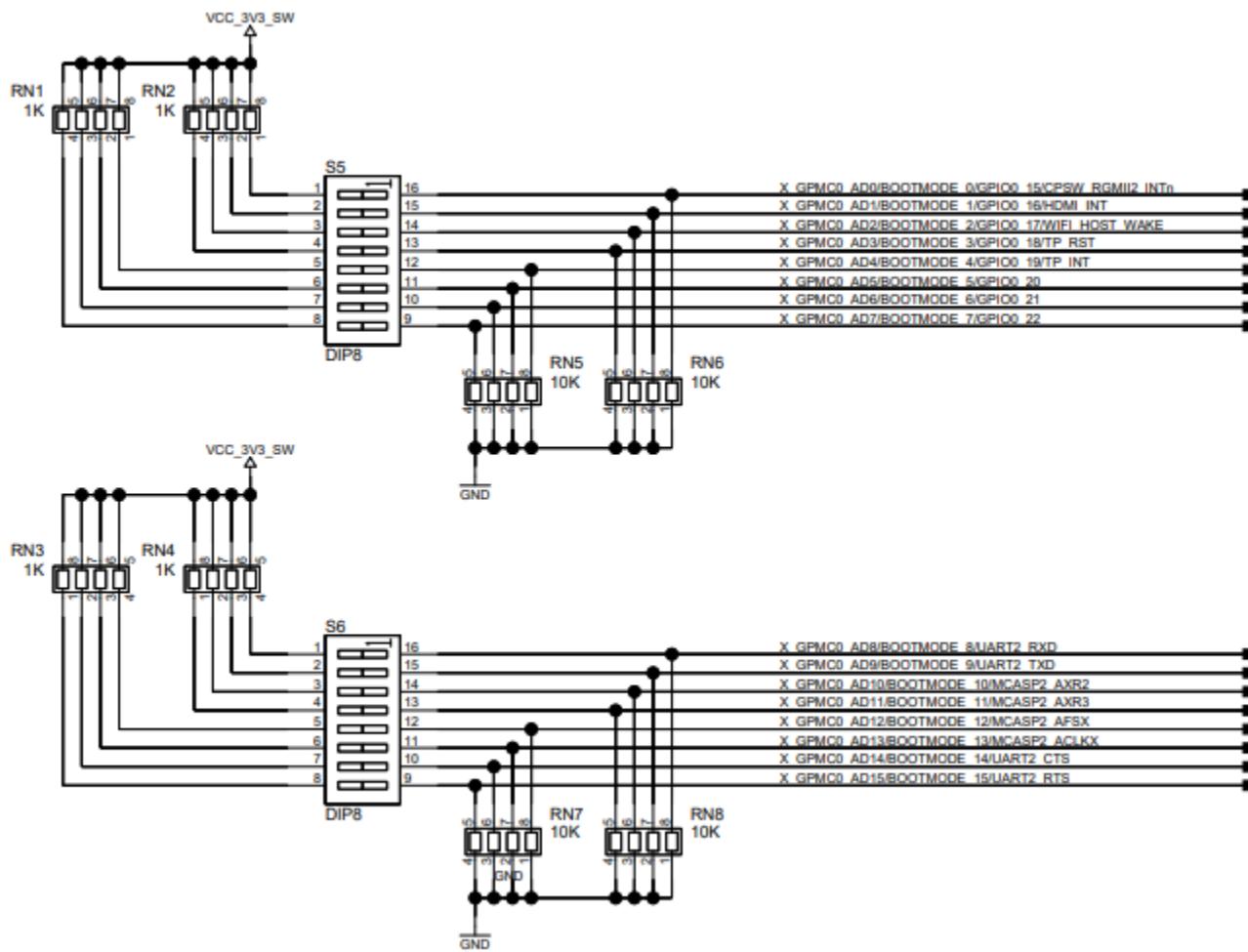


Figure 27. Reference Schematic for BOOTMODE configuration

# 7 Serial Interfaces

The following sub-sections detail each of the serial interfaces supported on the phyCORE-AM62xx.

## 7.1 CAN

The phyCORE-AM62xx SOM provides three Controller Area Network (MCAN) ports. The CAN interfaces support CAN and CAN FD (flexible data-rate) specifications, conforming with CAN protocol version 2.0 part A, B and ISO 11898-1:2015.

### 7.1.1 CAN Pinout

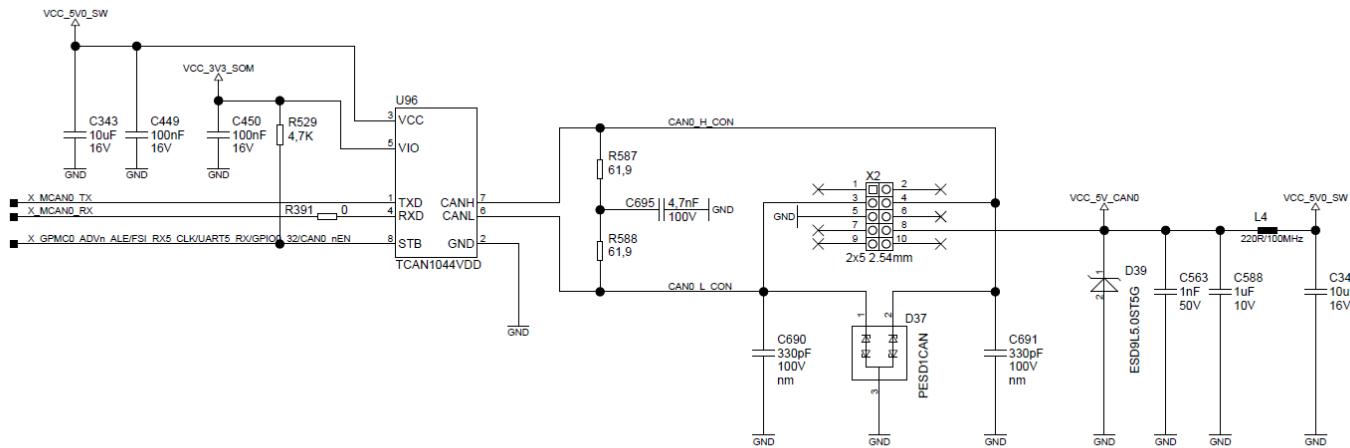
**Table 18 MCAN Connections at the phyCORE-Connector**

X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
C37	X_MCAN0_RX	I	3.3V <sup>1</sup>	MCANO Receive Data
C36	X_MCAN0_TX	O	3.3V <sup>1</sup>	MCANO Transmit Data
A58	X MCU_MCAN0_RX	I	3.3V <sup>1</sup>	MCU_MCAN0 Receive Data
A57	X MCU_MCAN0_TX	O	3.3V <sup>1</sup>	MCU_MCAN0 Transmit Data
A60	X MCU_MCAN1_RX	I	3.3V <sup>1</sup>	MCU_MCAN1 Receive Data
A59	X MCU_MCAN1_TX	O	3.3V <sup>1</sup>	MCU_MCAN1 Transmit Data

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

### 7.1.2 CAN Reference Circuit

An example reference circuit for connecting the MCANO signals to a 2x5 connector is shown below.



**Figure 28. MCANO Reference Schematic**

The circuit consists of:

- A 2x5 2.54mm pitch header
- A CAN FD Transceiver to convert the MCANO signals into differential CAN bus signal levels

## 7.2 Ethernet

The phyCORE-AM62xx SOM brings out two external 10/100/1000 Mbps Ethernet ports:

- One is translated on the SOM by a DP83867IRRGZ Ethernet PHY (a robust, low power transceiver) into the differential Ethernet data pairs that are accessible at the phyCORE-Connector. This Ethernet PHY:
  - Supports 10-BASE-T, 100BASE-TX, and 1000BASE-T protocols to interface directly to twisted pair media through an external transformer.
  - Provides two LED control outputs and one GPIO signal. The GPIO and LED I/O also serve as bootstrap pins for PHY configuration. Be careful to avoid pulling or driving these signals during power up and reset.
- The other, CPSW\_RGMII2, is brought out as RGMII/RMII

The on-board Ethernet PHY offers several default configuration options that include settings such as the PHY address and RGMII clock skew. Options such as these can be set via external strapping resistors which are described in the datasheet. The table below lists the default Ethernet PHY strapping configuration; however, these settings can be changed via the register settings of the PHY if necessary. Refer to the DP83867IRRGZ datasheet for further details on these configuration and strapping options ([DP83867IRRGZ Datasheet](#)).

**NOTE:**

Adjusting strapping options and PHY registers is not necessary when using PHYTEC provided BSPs.

**Table 19 Ethernet PHY Default Strapping Configuration**

Strapping Option	Default Setting	Strapping Signals
PHY Address	1	CPSW_RGMII1_RD0 CPSW_RGMII1_RD2
Mirror Mode	Disabled	CPSW_ETH0_LED0
Auto-negotiation	Enabled (advertise ability of 10/100/1000)	CPSW_RGMII1_RX_CTL
RGMII TX Clock Skew	2 ns	CPSW_ETH0_LED1 CPSW_ETH0_LED2
RGMII RX Clock Skew	2 ns	X_CPSW_ETH0_GPIO_0 X_CPSW_ETH0_GPIO_1

### 7.2.1 Ethernet Pinout

**Table 20 Ethernet Connections at the phyCORE-Connector**

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
-	B30	X_CPSW_ETH0_LED_ACTIVITY	OD	3.3V	LED Link Signal
-	B29	X_CPSW_ETH0_LED_LINK	OD	3.3V	LED Activity Signal
-	D43	X_CPSW_ETH0_GPIO_0 <sup>2</sup>	I/O	3.3V	SOM Ethernet PHY GPIO 0 <sup>2</sup>
-	D43	X_CPSW_ETH0_nINT <sup>2</sup> (2.2K pullup on SOM)	I/O	3.3V	SOM Ethernet PHY Interrupt (active low)
-	B27	X_CPSW_ETH0_A+	ETH_I/O	Differential	Ethernet Data A Positive

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
-	B26	X_CPSW_ETH0_A-	ETH_I/O	Differential	Ethernet Data A Negative
-	B25	X_CPSW_ETH0_B+	ETH_I/O	Differential	Ethernet Data B Positive
-	B24	X_CPSW_ETH0_B-	ETH_I/O	Differential	Ethernet Data B Negative
-	B22	X_CPSW_ETH0_C+	ETH_I/O	Differential	Ethernet Data C Positive
-	B21	X_CPSW_ETH0_C-	ETH_I/O	Differential	Ethernet Data C Negative
-	B20	X_CPSW_ETH0_D+	ETH_I/O	Differential	Ethernet Data D Positive
-	B19	X_CPSW_ETH0_D-	ETH_I/O	Differential	Ethernet Data D Negative
MDIO0_MDIO	B17	X_MDIO0_MDIO (1.5K pullup on SOM)	I/O	3.3V <sup>1</sup>	CPSW Management Data IO
MDIO0_MDC	B16	X_MDIO0_MDC (1.5K pullup on SOM)	O	3.3V <sup>1</sup>	CPSW Management Data Clock
RGMII2_RX_CTL	A17	X_CPSW_RGMII2_RX_CTL	I	3.3V <sup>1</sup>	CPSW RGMII2 Receive Control
RGMII2_RXC	A18	X_CPSW_RGMII2_RXC	I	3.3V <sup>1</sup>	CPSW RGMII2 Receive Clock
RGMII2_RD0	A23	X_CPSW_RGMII2_RD0	I	3.3V <sup>1</sup>	CPSW RGMII2 Receive Data 0
RGMII2_RD1	A22	X_CPSW_RGMII2_RD1	I	3.3V <sup>1</sup>	CPSW RGMII2 Receive Data 1
RGMII2_RD2	A21	X_CPSW_RGMII2_RD2	I	3.3V <sup>1</sup>	CPSW RGMII2 Receive Data 2
RGMII2_RD3	A20	X_CPSW_RGMII2_RD3	I	3.3V <sup>1</sup>	CPSW RGMII2 Receive Data 3
RGMII2_TX_CTL	A26	X_CPSW_RGMII2_TX_CTL	O	3.3V <sup>1</sup>	CPSW RGMII1 Transmit Control
RGMII2_TXC	A25	X_CPSW_RGMII2_TXC	I/O	3.3V <sup>1</sup>	CPSW RGMII1 Transmit Clock
RGMII2_TDO	A27	X_CPSW_RGMII2_TDO	O	3.3V <sup>1</sup>	CPSW RGMII1 Transmit Data 0
RGMII2_TD1	A28	X_CPSW_RGMII2_TD1	O	3.3V <sup>1</sup>	CPSW RGMII1 Transmit Data 1
RGMII2_TD2	A30	X_CPSW_RGMII2_TD2	O	3.3V <sup>1</sup>	CPSW RGMII1 Transmit Data 2
RGMII2_TD3	A31	X_CPSW_RGMII2_TD3	O	3.3V <sup>1</sup>	CPSW RGMII1 Transmit Data 3
RMII2_CRS_DV	A25	X_CPSW_RGMII2_TXC	I	3.3V <sup>1</sup>	RMII2 Carrier Sense / Data Valid
RMII2_REF_CLK	A18	X_CPSW_RGMII2_RXC	I	3.3V <sup>1</sup>	RMII Reference Clock
RMII2_RX_ER	A17	X_CPSW_RGMII2_RX_CTL	I	3.3V <sup>1</sup>	RMII2 Receive Data Error
RMII2_TX_EN	A26	X_CPSW_RGMII2_TX_CTL	O	3.3V <sup>1</sup>	RMII2 Transmit Enable
RMII2_RXD0	A23	X_CPSW_RGMII2_RD0	I	3.3V <sup>1</sup>	RMII2 Receive Data 0
RMII2_RXD1	A22	X_CPSW_RGMII2_RD1	I	3.3V <sup>1</sup>	RMII2 Receive Data 1
RMII2_TXD0	A27	X_CPSW_RGMII2_TD0	O	3.3V <sup>1</sup>	RMII2 Transmit Data 0
RMII2_TXD1	A28	X_CPSW_RGMII2_TD1	O	3.3V <sup>1</sup>	RMII2 Transmit Data 1

1: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

2: The signal brought out at this pin is controlled by a jumper. Refer to section [4.6 Solder Jumpers](#) for details.

The phyCORE-AM62xx SOM also brings out an Industrial Ethernet Peripheral (IEP) module that is not required for the PRG ethernet ports to function, but provide the following additional utility:

- An industrial ethernet timer with 18 compare events
- An industrial ethernet sync generator and latch capture
- An industrial ethernet watchdog timer

Table 21 IEP Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
PRGO_IEPO_EDIO_DATA_IN_OUT28	C28	X_MCASPO_AXR3	I/O	3.3V <sup>1</sup>	PRU Industrial Ethernet Distributed Clock Sync Output
PRGO_IEPO_EDIO_DATA_IN_OUT29	C27	X_MCASPO_AXR2	I/O	3.3V <sup>1</sup>	PRU Industrial Ethernet Distributed Clock Sync Output

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
PRGO_IEPO_EDIO_DATA_IN_OUT30	C35	X_I2C0_SCL (2.2K pullup on SOM)	I/O	3.3V <sup>1</sup>	PRU Industrial Ethernet Distributed Clock Sync Output
PRGO_IEPO_EDIO_DATA_IN_OUT31	C34	X_I2C0_SDA (2.2K pullup on SOM)	I/O	3.3V <sup>1</sup>	PRU Industrial Ethernet Distributed Clock Sync Output

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

## 7.2.2 Ethernet Design In Guide

### 7.2.2.1 CPSW\_ETH0 Ethernet Design In Considerations

- Connecting the phyCORE-AM62xx SOM to an existing 10/100/1000Base-T network involves adding an RJ45 and appropriate magnetic devices in the design. See the reference circuit in section [7.2.3 Ethernet Reference Circuits](#) for an example.
- Avoid any other signal lines crossing the Ethernet signals.
- More general differential pair routing guidelines are in section [4.10.1 High-Speed Differential Signal Routing Guidelines](#).

Table 22 phyCORE-AM62xx CPSW\_ETH0 Layout Characteristics

Signal Name	Length (μm)			Length Matching (μm)	Single Ended Impedance (Ω)	Differential Impedance (Ω)
	SOM Trace	Max Total	Max CB Trace			
X_CPSW_ETH0_A-	4625	101600	96975	254	50	100
X_CPSW_ETH0_A+	4588	101600	97012		50	
X_CPSW_ETH0_B-	5914	101600	95686	254	50	100
X_CPSW_ETH0_B+	5869	101600	95731		50	
X_CPSW_ETH0_C-	6376	101600	95224	254	50	100
X_CPSW_ETH0_C+	6254	101600	95346		50	
X_CPSW_ETH0_D-	6463	101600	95137	254	50	100
X_CPSW_ETH0_D+	6414	101600	95186		50	

### 7.2.2.2 RGMII Design In Considerations

- Place the Ethernet PHY as close as possible to the SOM connector and keep the trace lengths of the RGMII signals as short as possible.
- Add a 10kΩ pull-down resistor on any unused input or I/O signal on this interface if it is not connected to a PHY.
- Avoid any cuts in the ground plane or other references planes within the RGMII routing region.
- Place termination resistors (recommended to use 0Ω) near the PHY on all the RGMII RX\* signals.
- The MDIO clock and data signals do not need to be matched as strictly as RGMII. However, it is recommended to route these together and keep them length matched within 2540 μm.

- RGMII v2.0 Timing Requirements (shown in the table below) specify that the clock and data will be generated simultaneously by the transmitting source, which requires a skew be introduced between clock and data.

**Table 23 phyCORE-AM62xx RGMII Timing Requirements**

Parameter	Minimum	Typical	Maximum	Units
Data to clock output skew at transmitter	-500	0	500	ps
Data to clock output skew at receiver	1	1.8	2.6	ns

The skew can be introduced with additional PCB trace delay added to the clock signal on the carrier board or by adjusting the internal delay settings at the PHY or processor. However, please note that an internal delay may not be available on your selected ethernet PHY or it may not have sufficient adjustment to account for the required skew. The skew between the clock and each individual data and control signal should not fall below the 1ns minimum or exceed the 2.6ns maximum.

Ensure signals are properly length matched to meet these RGMII timing specifications. The following tables show the signal groups (TX vs. RX) that should be length matched and the trace length of each signal on the SOM. It is recommended to length match the control and data signals within 2540 µm, and then the trace length of the clock should be the average length of these control and data signals plus an additional 1.8ns delay. The recommended clock trace length on a carrier board is calculated using the following equation:

$$(\text{Average total length of control/data signals on SOM}) + (\text{Average total length of control/data signals on Carrier Board}) + (1.8\text{ns delay}) - (\text{Clock Trace Length on the SOM})$$

An example of using this equation to calculate the recommended clock lengths when implementing a physical delay for RGMII2 is shown in the equations below. The 1.8ns was translated to an estimated length using the general rule of 6.5ps/mm. However, the actual physical trace delay will vary depending on the PCB stackup, materials, etc.

- Transmit Clock Length Calculation with Physical Trace Delay:  $(18821 \mu\text{m}) + (\text{Average total length of control/data signals on Carrier Board}) + (276860 \mu\text{m}) - (19007 \mu\text{m})$
- Receive Clock Length Calculation with Physical Trace Delay:  $(14770 \mu\text{m}) + (\text{Average total length of control/data signals on Carrier Board}) + (276860 \mu\text{m}) - (14762 \mu\text{m})$

**Table 24 phyCORE-AM62xx RMGII2 Trace Length Characteristics**

Signal Name	SOM Trace Length (µm)	Match Group	Recommended Length Match
RGMII2_TXC	19007	RGMII2 Transmit	AVERAGE_LENGTH(TXCTL, TXD0, TXD1, TXD2, TXD3) + 1.8ns
RGMII2_TXCTL	18712		2540 µm
RGMII2_TXD0	18968		
RGMII2_TXD1	18545		
RGMII2_TXD2	18888		
RGMII2_TXD3	18994		

RGMII2_RXC	14762	RGMII2 Receive	AVERAGE_LENGTH(RXCTL, RXD0, RXD1, RXD2, RXD3) + 1.8ns
RGMII2_RXCTL	14963		2540 $\mu$ m
RGMII2_RXD0	14575		
RGMII2_RXD1	15030		
RGMII2_RXD2	14606		
RGMII2_RXD3	14674		

## 7.2.3 Ethernet Reference Circuits

Example reference circuits for connecting the CPSW\_RGMII1 differential signals from the on-board PHY to an RJ45 connector and CPSW\_RGMII2 signals to an Ethernet PHY are shown below.

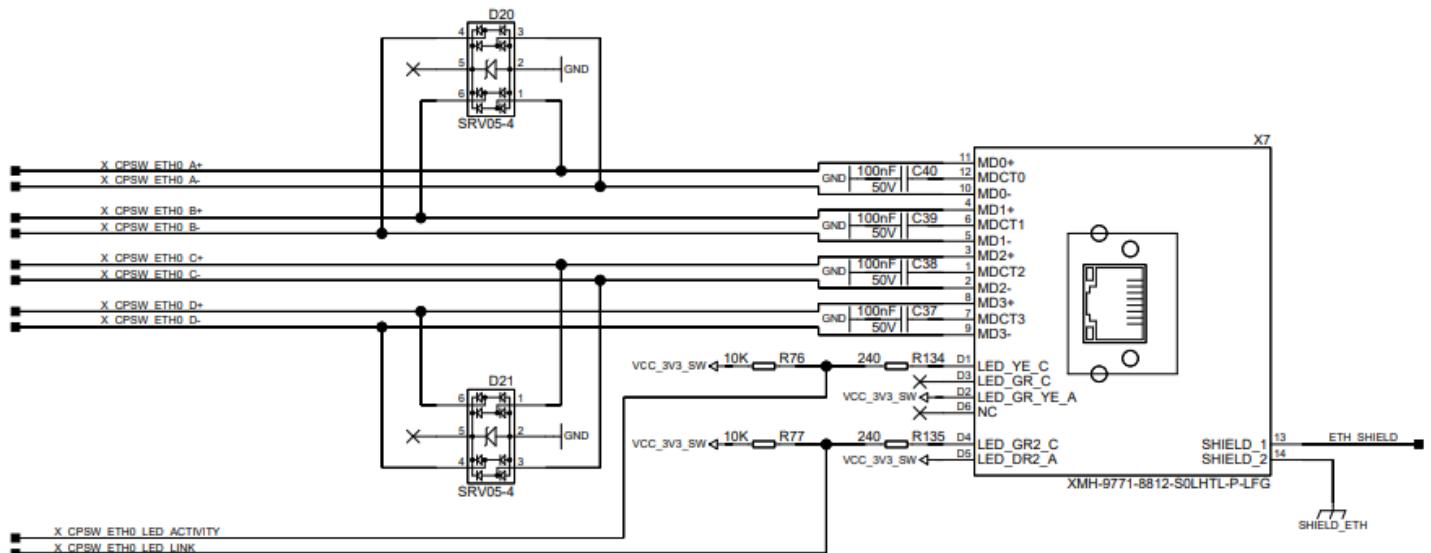


Figure 29. RJ45 Reference Schematic

The circuit consists of:

- An Ethernet Jack
- Two TVS diode arrays for ESD protection
- Two resistor networks to manage the Ethernet LEDs in the jack

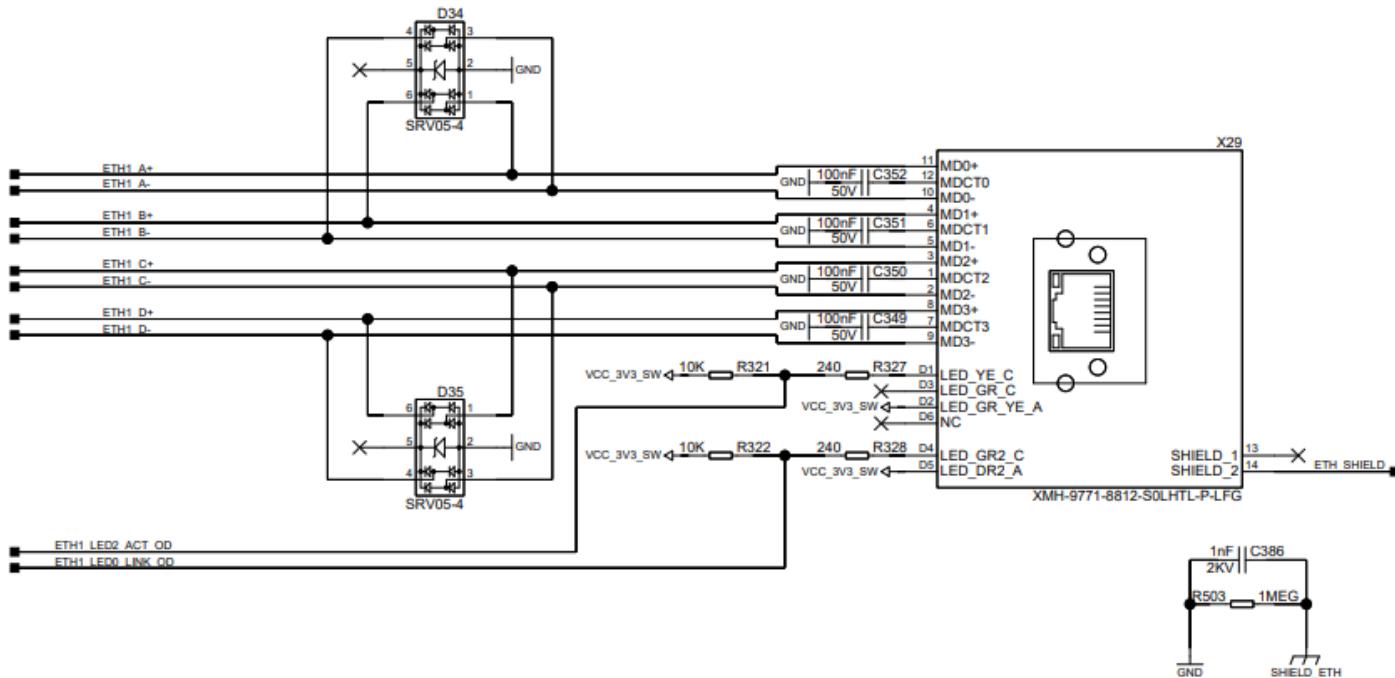


Figure 30. RGMII PHY RJ45 Reference Schematic

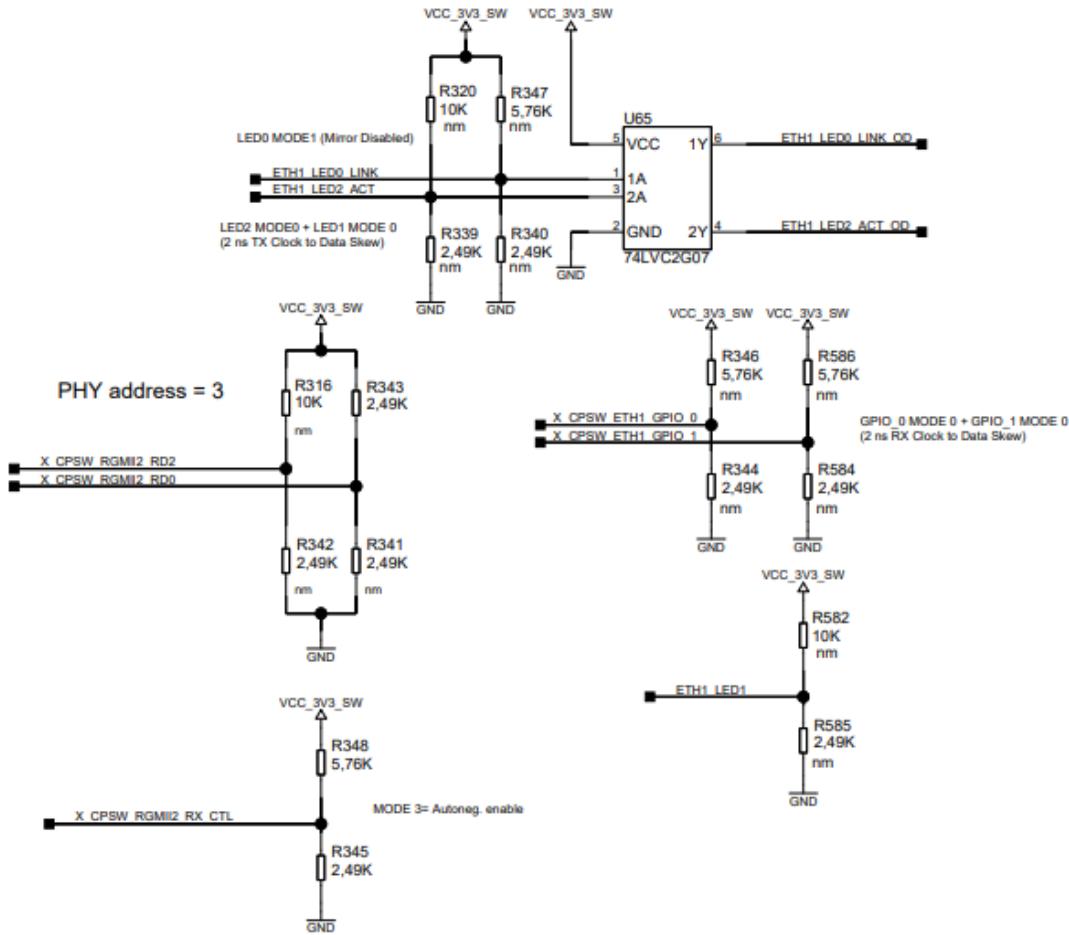


Figure 31. RGMII PHY Strapping Resistors Reference Schematic

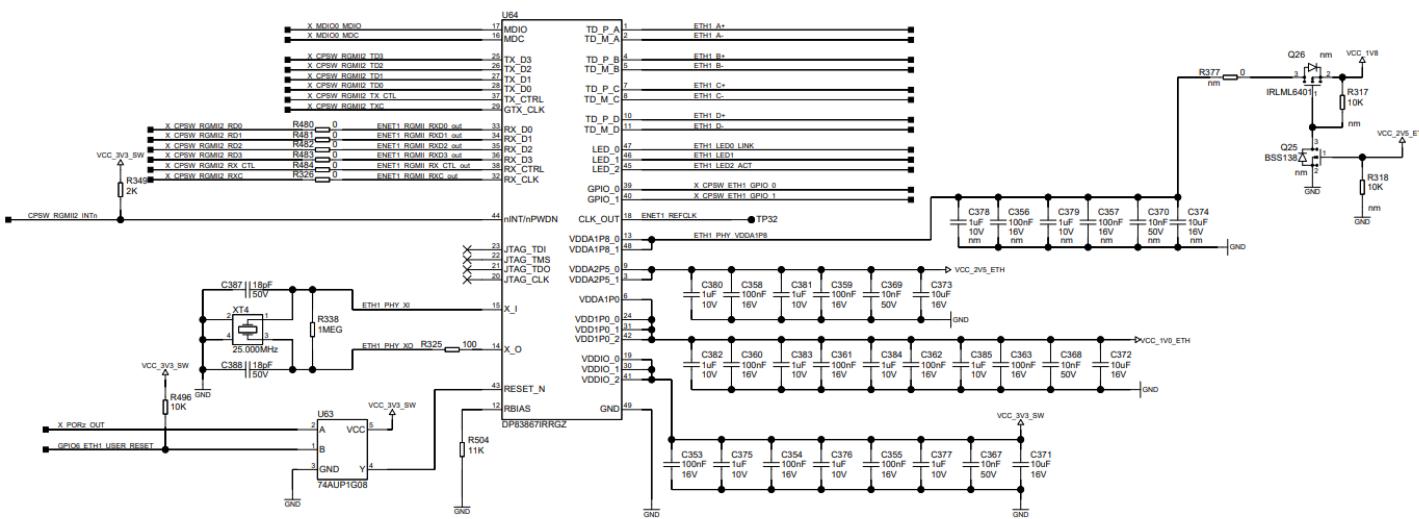


Figure 32. RGMII PHY Reference Schematic

The circuit consists of:

- An Ethernet PHY to convert the RGMII signals to differential Ethernet signals
- An AND gate to manage Ethernet reset and allow for the user to reset the PHY
- Strapping resistors to manage the PHY settings
- An RJ45 jack for connection to external networks

## 7.3 I<sup>2</sup>C

The Inter-Integrated Circuit (I<sup>2</sup>C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyCORE-AM62xx SOM provides six independent multimaster fast-mode I<sup>2</sup>C modules. The I<sup>2</sup>C interfaces provide the following functionality:

- Compliance with the Philips I<sup>2</sup>C specification version 2.1.
- Support standard mode (up to 100Kb/s), fast mode (up to 400Kb/s), and high-speed mode (up to 3.4Mb/s).

Aside from I<sup>2</sup>C0, which has pullups on the SOM, all the I<sup>2</sup>C signals require pullups in your custom CB design.

### CAUTION:

I<sup>2</sup>C0 is used by the on-board PMIC (I<sup>2</sup>C address 0x30), EEPROM (I<sup>2</sup>C address 0x50), and RTC (I<sup>2</sup>C address 0x52). Ensure any external use of the I<sup>2</sup>C0 line does not interfere with this communication.

## 7.3.1 I<sup>2</sup>C Pinout

Table 25 I<sup>2</sup>C Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal	Type	Level	Description
MCU_I2C0_SCL	C49	X_MCU_I2C0_SCL	OD-O	3.3V <sup>1</sup>	MCU I2C0 Clock
MCU_I2C0_SDA	C50	X_MCU_I2C0_SDA	OD-I/O	3.3V <sup>1</sup>	MCU I2C0 Data
WKUP_I2C0_SCL	D50	X_WKUP_I2C0_SCL	OD-O	3.3V <sup>1</sup>	WKUP I2C0 Clock
WKUP_I2C0_SDA	D51	X_WKUP_I2C0_SDA	OD-I/O	3.3V <sup>1</sup>	WKUP I2C0 Data
I2C0_SCL	C35	X_I2C0_SCL (2.2K pullup on SOM)	OD-O	3.3V <sup>1</sup>	Main I2C0 Clock
I2C0_SDA	C34	X_I2C0_SDA (2.2K pullup on SOM)	OD-I/O	3.3V <sup>1</sup>	Main I2C0 Data
I2C1_SCL	C32	X_I2C1_SCL	OD-O	3.3V <sup>1</sup>	Main I2C1 Clock
I2C1_SDA	C33	X_I2C1_SDA	OD-I/O	3.3V <sup>1</sup>	Main I2C1 Data
I2C2_SCL	D14	X_GPMCO_CSn2	OD-O	3.3V <sup>1</sup>	Main I2C2 Clock
I2C2_SDA	C14	X_GPMCO_CSn3	OD-I/O	3.3V <sup>1</sup>	Main I2C2 Data
I2C3_SCL	D36	X_UART0_CTSN	OD-O	3.3V <sup>1</sup>	Main I2C3 Clock
I2C3_SDA	D35	X_UART0_RTSN	OD-I/O	3.3V <sup>1</sup>	Main I2C3 Data

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

## 7.4 SPI

The Serial Peripheral Interface (SPI) is a transmit/receive, master/slave synchronous serial bus. The phyCORE-AM62xx SOM provides access to four SPI ports at the phyCORE-Connector.

### 7.4.1 SPI Pinout

Table 26 SPI Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
SPI0_CLK	D40	X_SPI0_CLK	I/O	3.3V <sup>1</sup>	SPI0 Clock
SPI0_CS0	C40	X_SPI0_CS0	I/O	3.3V <sup>1</sup>	SPI0 Chip Select 0
SPI0_CS1	C41	X_SPI0_CS1	I/O	3.3V <sup>1</sup>	SPI0 Chip Select 1
SPI0_CS2	D36	X_UART0_CTSN	I/O	3.3V <sup>1</sup>	SPI0 Chip Select 2
SPI0_CS3	D35	X_UART0_RTSN	I/O	3.3V <sup>1</sup>	SPI0 Chip Select 3
SPI0_D0	D41	X_SPI0_D0	O	3.3V <sup>1</sup>	SPI0 Data Out
SPI0_D1	D42	X_SPI0_D1	I	3.3V <sup>1</sup>	SPI0 Data In
SPI2_CLK	C33 C30	X_I2C1_SDA X_MCASPO_ACLKR	I/O	3.3V <sup>1</sup>	SPI2 Clock
SPI2_CS0	C35 D32	X_I2C0_SCL (2.2K pullup on SOM) X_MCASPO_AFSR	I/O	3.3V <sup>1</sup>	SPI2 Chip Select 0
SPI2_CS1	C32 C29	X_I2C1_SCL X_MCASPO_ACLKX	I/O	3.3V <sup>1</sup>	SPI2 Chip Select 1
SPI2_CS2	C34 D31	X_I2C0_SDA (2.2K pullup on SOM) X_MCASPO_AXR1	I/O	3.3V <sup>1</sup>	SPI2 Chip Select 2
SPI2_CS3	C60 D30	X_EXT_REFCLK1 X_MCASPO_AFSX	I/O	3.3V <sup>1</sup>	SPI2 Chip Select 3
SPI2_D0	C28	X_MCASPO_AXR3	O	3.3V <sup>1</sup>	SPI2 Data Out

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
	D37	X_UART0_RXD	I	3.3V <sup>1</sup>	SPI2 Data In
SPI2_D1	C27	X_MCASPO_AXR2			
	D38	X_UART0_TXD			
MCU_SPI0_CLK	D46	X MCU_SPIO_CLK	I/O	3.3V <sup>1</sup>	MCU SPI0 Clock
MCU_SPI0_CS1	D49	X MCU_SPIO_CS1	I/O	3.3V <sup>1</sup>	MCU SPI0 Chip Select 1
MCU_SPI0_CS2	B58	X_WKUP_UART0_RXD	I/O	3.3V <sup>1</sup>	MCU SPI0 Chip Select 2
	A60	X MCU_MCAN1_RX			
MCU_SPI0_CS3	A57	X MCU_MCAN0_TX	I/O	3.3V <sup>1</sup>	MCU SPI0 Chip Select 3
MCU_SPI0_D0	D47	X MCU_SPIO_D0	O	3.3V <sup>1</sup>	MCU SPI0 Data Out
MCU_SPI0_D1	D48	X MCU_SPIO_D1	I	3.3V <sup>1</sup>	MCU SPI0 Data In
MCU_SPI1_CLK	B59	X_WKUP_UART0_RTSN	I/O	3.3V <sup>1</sup>	MCU SPI1 Clock
	A60	X MCU_MCAN1_RX			
MCU_SPI1_CS0	A56	X_WKUP_UART0_CTSN	I/O	3.3V <sup>1</sup>	MCU SPI1 Chip Select 0
MCU_SPI1_CS1	A59	X MCU_MCAN1_TX	I/O	3.3V <sup>1</sup>	MCU SPI1 Chip Select 1
MCU_SPI1_CS2	B57	X_WKUP_UART0_RXD	I/O	3.3V <sup>1</sup>	MCU SPI1 Chip Select 2
	A60	X MCU_MCAN1_RX			
MCU_SPI1_CS3	A58	X MCU_MCAN0_RX	I/O	3.3V <sup>1</sup>	MCU SPI1 Chip Select 3
MCU_SPI1_D0	D53	X MCU_UART0_CTSN	O	3.3V <sup>1</sup>	MCU SPI1 Data Out
MCU_SPI1_D1	D54	X MCU_UART0_RTSN	I	3.3V <sup>1</sup>	MCU SPI1 Data In

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

## 7.5 UART

The Universal Asynchronous Receiver/Transmitter module is a slave peripheral that utilizes direct memory access (DMA) for data transfer or interrupt polling via a host CPU. There are ten UART modules provided, and each can be used for configuration and data exchange with external peripheral devices. UART0 is the default console and as such PHYTEC recommends bringing out UART0 for console access. More information on using it as a debug console is provided in section [11.3 UART0](#).

### 7.5.1 UART Pinout

Table 27 UART Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
UART0_CTSN	D36	X_UART0_CTSN	I	3.3V <sup>1</sup>	UART0 Clear to Send
UART0_RTSN	D35	X_UART0_RTSN	O	3.3V <sup>1</sup>	UART0 Request to Send
UART0_RXD	D37	X_UART0_RXD	I	3.3V <sup>1</sup>	UART0 Receive Data
UART0_TXD	D38	X_UART0_TXD	O	3.3V <sup>1</sup>	UART0 Transmit Data
UART1_CTSN	C28	X_MCASPO_AXR3	I	3.3V <sup>1</sup>	UART1 Clear to Send
UART1_DCDN	C35	X_I2C0_SCL (2.2K pullup on SOM)	I	3.3V <sup>1</sup>	UART1 Data Carrier Detect (active low)
UART1_DSRN	C34	X_I2C0_SDA (2.2K pullup on SOM)	I	3.3V <sup>1</sup>	UART1 Data Set Ready (active low)
UART1_DTRN	C36	X_MCAN0_TX	O	3.3V <sup>1</sup>	UART1 Data Terminal Ready (active low)
UART1_RIN	C37	X_MCAN0_RX	I	3.3V <sup>1</sup>	UART1 Ring Indicator

<b>Processor Signal</b>	<b>X1 Pin #(s)</b>	<b>SOM Signal(s)</b>	<b>Type</b>	<b>Level</b>	<b>Description</b>
UART1_RTSN	C27	X_MCASPO_AXR2	O	3.3V <sup>1</sup>	UART1 Request to Send
UART1_RXD	C32	X_I2C1_SCL	I	3.3V <sup>1</sup>	UART1 Receive Data
	D32	X_MCASPO_AFSR			
UART1_TXD	C33	X_I2C1_SDA	O	3.3V <sup>1</sup>	UART1 Transmit Data
	C30	X_MCASPO_ACLKR			
UART2_CTSN	C25	X_MMC1_DAT0	I	3.3V <sup>1</sup>	UART2 Clear to Send
	A7	X_VOUT0_PCLK			
	D10	X_GPMCO_AD14/BOOTMODE_14 <sup>2</sup> (100K pulldown on SOM)			
UART2_RTSN	A5	X_VOUT0_VSYNC	O	3.3V <sup>1</sup>	UART2 Request to Send
	C26	X_MMC1_DAT1			
	D11	X_GPMCO_AD15/BOOTMODE_15 <sup>2</sup> (100K pulldown on SOM)			
UART2_RXD	D36	X_UART0_CTSN	I	3.3V <sup>1</sup>	UART2 Receive Data
	D29	X_MMC1_DAT3			
	D2	X_GPMCO_AD8/BOOTMODE_8 <sup>2</sup> (100K pullup on SOM)			
	B12	X_VOUT0_DATA0			
UART2_TXD	D35	X_UART0_RTSN	O	3.3V <sup>1</sup>	UART2 Transmit Data
	D28	X_MMC1_DAT2			
	D4	X_GPMCO_AD9/BOOTMODE_9 <sup>2</sup> (100K pullup on SOM)			
	B6	X_VOUT0_DATA1			
UART3_CTSN	C22	X_MMC1_SDWP (10K pullup on SOM)	I	3.3V <sup>1</sup>	UART3 Clear to Send
	A15	X_VOUT0_DE			
UART3_RTSN	A6	X_VOUT0_HSYNC	O	3.3V <sup>1</sup>	UART3 Request to Send
	C23	X_MMC1_SD_CD (10K pullup on SOM)			
UART3_RXD	D26	X_MMC1_CLK (49.9K pulldown on SOM)	I	3.3V <sup>1</sup>	UART3 Receive Data
	D5	X_GPMCO_AD10/BOOTMODE_10 <sup>2</sup> (100K pullup on SOM)			
	B4	X_VOUT0_DATA9			
UART3_TXD	D25	X_MMC1_CMD	O	3.3V <sup>1</sup>	UART3 Transmit Data
	D6	X_GPMCO_AD11/BOOTMODE_11 <sup>2</sup> (100K pulldown on SOM)			
	B5	X_VOUT0_DATA3			
UART4_CTSN	A13	X_VOUT0_DATA15	I	3.3V <sup>1</sup>	UART4 Clear to Send
UART4_RTSN	A12	X_VOUT0_DATA14	O	3.3V <sup>1</sup>	UART4 Request to Send
UART4_RXD	C20	X_MMC2_SD_CD (10K pullup on SOM)	I	3.3V <sup>1</sup>	UART4 Receive Data
	D14	X_GPMCO_CSn2			
	D7	X_GPMCO_AD12/BOOTMODE_12 <sup>2</sup> (100K pullup on SOM)			
	B7	X_VOUT0_DATA4			
UART4_TXD	C21	X_MMC2_SDWP (10K pullup on SOM)	O	3.3V <sup>1</sup>	UART4 Transmit Data
	C14	X_GPMCO_CSn3			
	D8	X_GPMCO_AD13/BOOTMODE_13 <sup>2</sup> (100K pullup on SOM)			
	B10	X_VOUT0_DATA5			
UART5_CTSN	A10	X_VOUT0_DATA13	I	3.3V <sup>1</sup>	UART5 Clear to Send

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
UART5_RTSN	A8	X_VOUT0_DATA12	I	3.3V <sup>1</sup>	UART5 Request to Send
UART5_RXD	C36	X_MCAN0_TX			
	D23	X_MMIC2_DAT3			
	D10	X_GPMCO_AD14/BOOTMODE_14 <sup>2</sup> (100K pulldown on SOM)			UART5 Receive Data
	B11	X_VOUT0_DATA6			
UART5_TXD	B9	X_VOUT0_DATA7	O	3.3V <sup>1</sup>	
	C37	X_MCAN0_RX			UART5 Transmit Data
	D24	X_MMIC2_DAT2			
UART6_CTSN	A11	X_VOUT0_DATA11	I	3.3V <sup>1</sup>	UART6 Clear to Send
UART6_RTSN	A16	X_VOUT0_DATA10	O	3.3V <sup>1</sup>	UART6 Request to Send
UART6_RXD	C28	X_MCASPO_AXR3	I	3.3V <sup>1</sup>	
	C23	X_MMIC1_SDCD (10K pullup on SOM)			
	D18	X_MMIC2_CLK (49.9K pulldown on SOM)			UART6 Receive Data
	B15	X_VOUT0_DATA8			
	D16	X_GPMCO_WAIT1			
UART6_TXD	C27	X_MCASPO_AXR2	O	3.3V <sup>1</sup>	
	C22	X_MMIC1_SDWP (10K pullup on SOM)			UART6 Transmit Data
	D19	X_MMIC2_CMD			
	D15	X_GPMCO_WPn			
	B14	X_VOUT0_DATA9			
MCU_UART0_CTSN	D53	X MCU_UART0_CTSN	I	3.3V <sup>1</sup>	MCU_UART0 Clear to Send
MCU_UART0_RTSN	D54	X MCU_UART0_RTSN	O	3.3V <sup>1</sup>	MCU_UART0 Request to Send
MCU_UART0_RXD	D55	X MCU_UART0_RXD	I	3.3V <sup>1</sup>	MCU_UART0 Receive Data
MCU_UART0_TXD	D56	X MCU_UART0_TXD	O	3.3V <sup>1</sup>	MCU_UART0 Transmit Data
WKUP_UART1_CTSN	A56	X WKUP_UART1_CTSN	I	3.3V <sup>1</sup>	WKUP_UART1 Clear to Send
WKUP_UART1_RTSN	B59	X WKUP_UART1_RTSN	O	3.3V <sup>1</sup>	WKUP_UART1 Request to Send
WKUP_UART1_RXD	B58	X WKUP_UART1_RXD	I	3.3V <sup>1</sup>	WKUP_UART1 Receive Data
WKUP_UART1_TXD	B57	X WKUP_UART1_TXD	O	3.3V <sup>1</sup>	WKUP_UART1 Transmit Data
PRO_UART0_CTSN	A31	X CPSW_RGMII2_TD3	I	3.3V <sup>1</sup>	PRO_UART0 Clear to Send
PRO_UART0_RTSN	A23	X CPSW_RGMII2_RD0	O	3.3V <sup>1</sup>	PRO_UART0 Request to Send
PRO_UART0_RXD	A21	X CPSW_RGMII2_RD2	I	3.3V <sup>1</sup>	
	D31	X MCASPO_AXR1			PRO_UART0 Receive Data
	C28	X MCASPO_AXR3			
	C36	X_MCAN0_TX			
PRO_UART0_TXD	C27	X MCASPO_AXR2	O	3.3V <sup>1</sup>	
	A20	X CPSW_RGMII2_RD3			PRO_UART0 Transmit Data
	C37	X_MCAN0_RX			
	D33	X MCASPO_AXR0			

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

<sup>2</sup>: This signal should not be driven during reset. More information can be found in section [6.3 System Boot Configuration](#).

## 7.6 USB

The phyCORE-AM62xx SOM provides two USB2.0 Dual-Role Device (DRD) Subsystems with integrated USB VBUS detection.

### 7.6.1 USB Pinout

**Table 28 USB Connections at the phyCORE-Connector**

X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
A40	X_USB0_VBUS	A/I	5V	USB Level-shifted VBUS Input (resistor/diode network on SOM)
A41	X_USB0_DRVVBUS	O	3.3V <sup>1</sup>	USB VBUS control output (active high)
A38	X_USB0_DM	I/O	Differential	USB OTG1 2.0 Differential Data Negative
A39	X_USB0_DP	I/O	Differential	USB OTG1 2.0 Differential Data Positive
B41	X_USB1_VBUS	A/I	5V	USB Level-shifted VBUS Input (resistor/diode network on SOM)
B42	X_USB1_DRVVBUS	O	3.3V <sup>1</sup>	USB VBUS control output (active high)
B39	X_USB1_DM	I/O	Differential	USB OTG1 2.0 Differential Data Negative
B40	X_USB1_DP	I/O	Differential	USB OTG1 2.0 Differential Data Positive

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

### 7.6.2 USB Design In Considerations

- X\_USB#\_DP/X\_USB#\_DM trace lengths should be matched and should be no more than 12 inches in total length (SOM + Carrier Board), though 4 inches is considered typical. The table below shows the length of the USB2.0 traces on the SOM and required constraints.

**Table 29 phyCORE-AM62xx USBO Layout Characteristics**

Signal Name	Length (μm)			Length Matching (μm)	Single Ended Impedance (Ω)	Differential Impedance (Ω)
	SOM Trace	Max Total	Max CB Trace			
X_USB0_DP	20309	304800	284491	1270	50	90
X_USB0_DM	20350	304800	284450		50	
X_USB1_DP	14038	304800	290762	1270	50	90
X_USB1_DM	14212	304800	290588		50	

### 7.6.3 USB Reference Circuits

Example reference circuits for connecting the USB1 signals to a HUB and then connecting the HUB to a USB 2.0 connector as well as connecting USB0 to a USB-C connector are shown below.

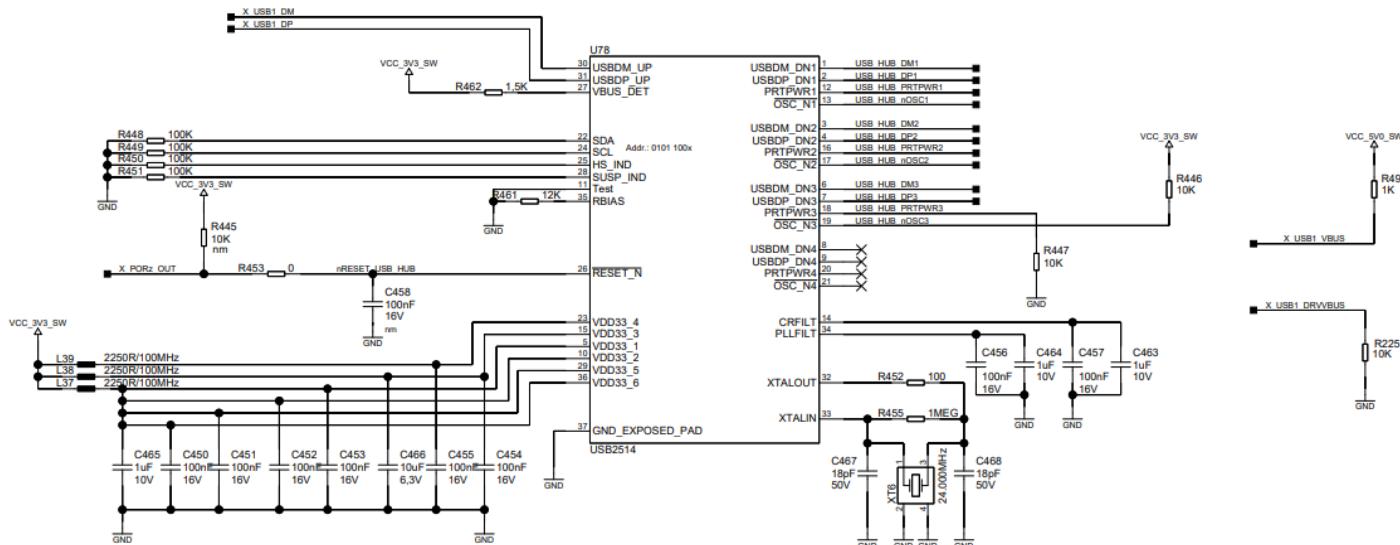


Figure 33. USB-HUB Reference Schematic

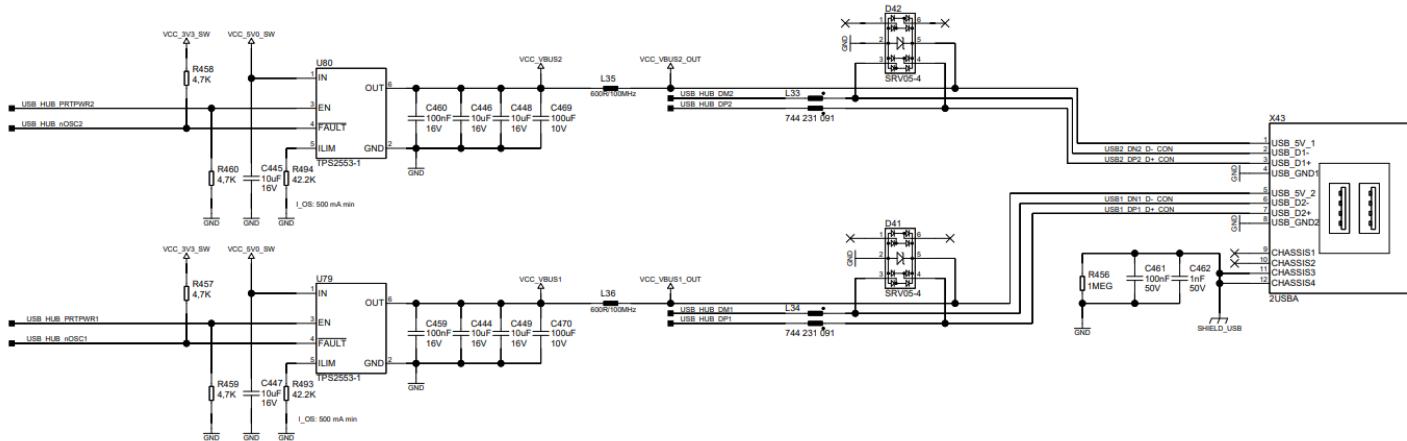


Figure 34. USB 2.0 Connector Reference Schematic

The above circuits consist of the following parts:

- A USB-HUB to convert the USB2.0 and SERDES signals into four USB outputs
- Two USB power switches to shut down the USB power rails if the current exceeds 0.6A
- Two TVS diode arrays and two common mode filters (CMF) for ESD and EMI considerations
- A two port USB 2.0 connector

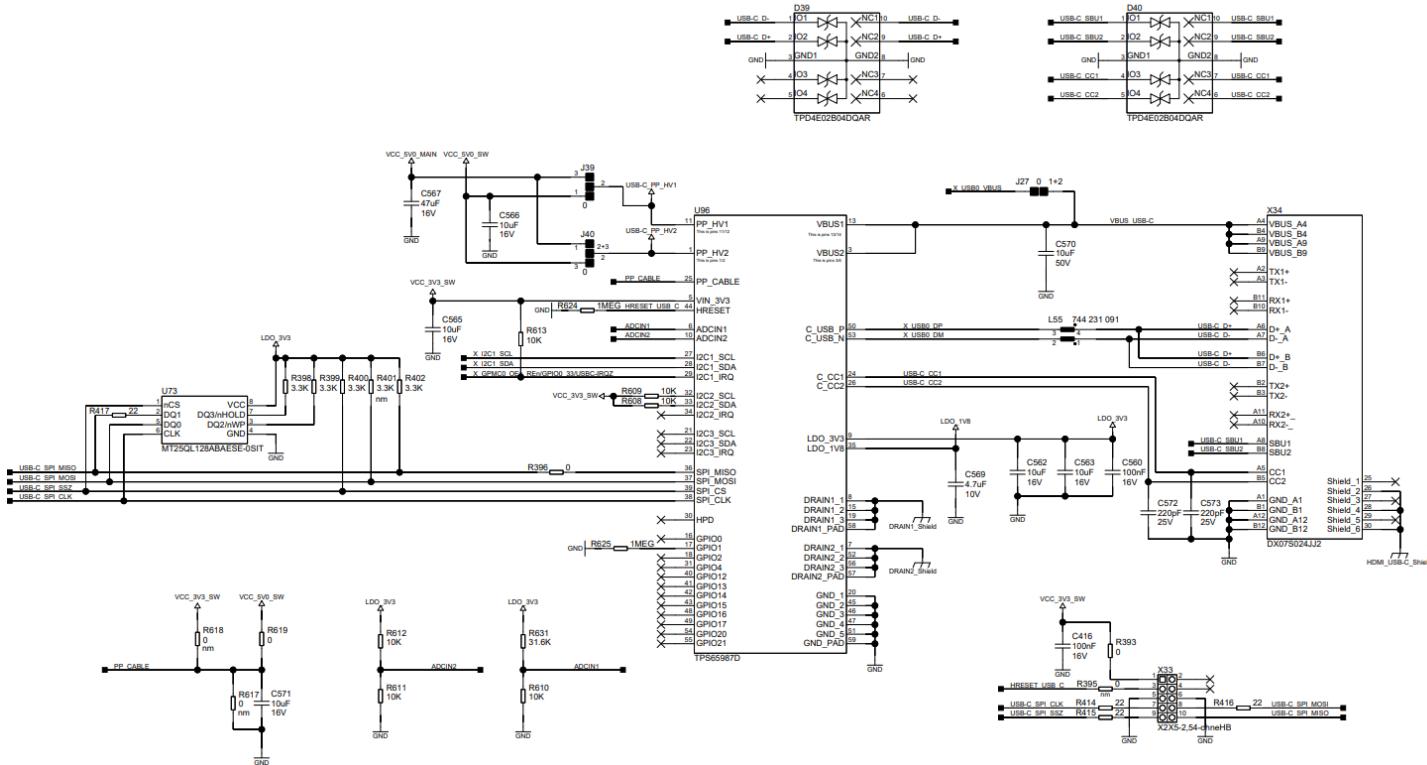


Figure 35. USB-C Connector Reference Schematic

The above circuits consist of the following parts:

- A USB-C controller to manage the USB-C control signals
- A serial NOR memory and 2x5 header to program the USB-C controller
- Two TVS diode arrays for ESD and EMI considerations
- A USB-C connector

## 7.7 MCASP

The phyCORE-AM62xx SOM provides three Multichannel Audio Serial Ports (MCASP). The MCASP interfaces provide the following functionality:

- Supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and similar formats
- Supports digital audio interface transmission formats (SPDIF, IEC60958-1, and AES-3)

### 7.7.1 MCASP Pinout

Table 30 MCASP Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
MCASPO_ACLKR	C30	X_MCASPO_ACLKR	I/O	3.3V <sup>l</sup>	MCASP Receive Bit Clock
MCASPO_ACLKX	C29	X_MCASPO_ACLKX	I/O	3.3V <sup>l</sup>	MCASP Transmit Bit Clock
MCASPO_AFSR	D32	X_MCASPO_AFSR	I/O	3.3V <sup>l</sup>	MCASP Receive Frame Sync
MCASPO_AF SX	D30	X_MCASPO_AF SX	I/O	3.3V <sup>l</sup>	MCASP Transmit Frame Sync
MCASPO_AXRO	D33	X_MCASPO_AXRO	I/O	3.3V <sup>l</sup>	MCASP Serial Data (Input/Output)

MCASP0_AXR1	D31	X_MCASP0_AXR1	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
MCASP0_AXR2	C27	X_MCASP0_AXR2	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
MCASP0_AXR3	C28	X_MCASP0_AXR3	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
MCASP1_ACLKR	D18	X_MMC2_CLK (49.9K pulldown on SOM)	I/O	3.3V <sup>1</sup>	MCASP Receive Bit Clock
	C14	X_GPMCO_CSn3			
MCASP1_ACLKX	C20	X_MMC2_SDCD (10K pullup on SOM)	I/O	3.3V <sup>1</sup>	MCASP Transmit Bit Clock
	C16	X_GPMCO_BE0n_CLE			
MCASP1_AFSR	D19	X_MMC2_CMD	I/O	3.3V <sup>1</sup>	MCASP Receive Frame Sync
	D14	X_GPMCO_CSn2			
MCASP1_AFSX	C21	X_MMC2_SDWP (10K pullup on SOM)	I/O	3.3V <sup>1</sup>	MCASP Transmit Frame Sync
	C2	X_GPMCO_WAIT0			
MCASP1_AXR0	D20	X_MMC2_DAT0	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	C13	X_GPMCO_WEn			
MCASP1_AXR1	D21	X_MMC2_DAT1	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	C17	X_GPMCO_OEn_REn			
MCASP1_AXR2	D24	X_MMC2_DAT2	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	C15	X_GPMCO_ADVn_ALE			
MCASP1_AXR3	D23	X_MMC2_DAT3	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	C3	X_GPMCO_CLK			
MCASP1_AXR4	D14	X_GPMCO_CSn2	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	D19	X_MMC2_CMD			
MCASP1_AXR5	D18	X_MMC2_CLK (49.9K pulldown on SOM)	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	C14	X_GPMCO_CSn3			
MCASP2_ACLKR	A28	X_CPSW_RGMII2_TD1	I/O	3.3V <sup>1</sup>	MCASP Receive Bit Clock
	D11	X_GPMCO_AD15/BOOTMODE_15 <sup>2</sup> (100K pulldown on SOM)			
MCASP2_ACLKX	A31	X_CPSW_RGMII2_TD3	I/O	3.3V <sup>1</sup>	MCASP Transmit Bit Clock
	D35	X_UART0_RTSN			
	D8	X_GPMCO_AD13/BOOTMODE_13 <sup>2</sup> (100K pullup on SOM)			
MCASP2_AFSR	A22	X_CPSW_RGMII2_RD1	I/O	3.3V <sup>1</sup>	MCASP Receive Frame Sync
	D10	X_GPMCO_AD14/BOOTMODE_14 <sup>2</sup> (100K pulldown on SOM)			
MCASP2_AFSX	D36	X_UART0_CTSN	I/O	3.3V <sup>1</sup>	MCASP Transmit Frame Sync
	A30	X_CPSW_RGMII2_TD2			
	D7	X_GPMCO_AD12/BOOTMODE_12 <sup>2</sup> (100K pullup on SOM)			
MCASP2_AXR0	A21	X_CPSW_RGMII2_RD2	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	C36	X_MCAN0_TX			
	D2	X_GPMCO_AD8/BOOTMODE_8 <sup>2</sup> (100K pullup on SOM)			
MCASP2_AXR1	A18	X_CPSW_RGMII2_RXC	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	C37	X_MCAN0_RX			
	D4	X_GPMCO_AD9/BOOTMODE_9 <sup>2</sup> (100K pullup on SOM)			
MCASP2_AXR2	A23	X_CPSW_RGMII2_RDO	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)

	D5	X_GPMCO_AD10/BOOTMODE_10 <sup>2</sup> (100K pullup on SOM)			
MCASP2_AXR3	A17	X_CPSW_RGMII2_RX_CTL	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	D6	X_GPMCO_AD11/BOOTMODE_11 <sup>2</sup> (100K pulldown on SOM)			
MCASP2_AXR4	A26	X_CPSW_RGMII2_TX_CTL	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	C4	X_GPMCO_ADO/BOOTMODE_0 <sup>2</sup> (100K pullup on SOM)			
MCASP2_AXR5	A25	X_CPSW_RGMII2_TXC	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	C5	X_GPMCO_AD1/BOOTMODE_1 <sup>2</sup> (100K pullup on SOM)			
MCASP2_AXR6	C7	X_GPMCO_AD2/BOOTMODE_2 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	A27	X_CPSW_RGMII2_TD0			
MCASP2_AXR7	A22	X_CPSW_RGMII2_RD1	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	C8	X_GPMCO_AD3/BOOTMODE_3 <sup>2</sup> (100K pullup on SOM)			
MCASP2_AXR8	C9	X_GPMCO_AD4/BOOTMODE_4 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
	A28	X_CPSW_RGMII2_TD1			
MCASP2_AXR9	C10	X_GPMCO_AD5/BOOTMODE_5 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
MCASP2_AXR10	C11	X_GPMCO_AD6/BOOTMODE_6 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
MCASP2_AXR11	D1	X_GPMCO_AD7/BOOTMODE_7 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
MCASP2_AXR12	C18	X_GPMCO_BE1n	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
MCASP2_AXR13	C1	X_GPMCO_DIR	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
MCASP2_AXR14	D12	X_GPMCO_CSn0	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)
MCASP2_AXR15	D13	X_GPMCO_CSn1	I/O	3.3V <sup>1</sup>	MCASP Serial Data (Input/Output)

1: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

2: This signal should not be driven during reset. More information can be found in section [6.3 System Boot Configuration](#).

## 8 Display and Camera Interfaces

The following sub-sections detail each of the display/camera interfaces supported on the phyCORE-AM62xx.

### 8.1 VOUT

The phyCORE-AM62xx SOM brings out one 24-bit RGB parallel video output (VOUT). VOUT supports the following display interface modes:

- Parallel MIPI DPI 2.0 (Digital Pixel Interface): RGB 16/18/24-bit outputs with separate sync signals
- BT.656/BT.1120 interface: YUV422 outputs (8/10-bit modes) with embedded syncs

## 8.1.1 VOUT Pinout

Table 31 VOUT Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
VOUT0_DE	A15	X_VOUT0_DE	O	3.3V <sup>1</sup>	Video Output Data Enable
VOUT0_EXTPCLKIN	D16	X_GPMCO_WAIT1	I	3.3V <sup>1</sup>	Video Output External Pixel Clock Input
VOUT0_HSYNC	A6	X_VOUT0_HSYNC	O	3.3V <sup>1</sup>	Video Output Horizontal Sync
VOUT0_PCLK	A7	X_VOUT0_PCLK	O	3.3V <sup>1</sup>	Video Output Pixel Clock Output
VOUT0_VSYNC	A5	X_VOUT0_SYNC	O	3.3V <sup>1</sup>	Video Output Vertical Sync
VOUT0_DATA0	B12	X_VOUT0_DATA0	O	3.3V <sup>1</sup>	Video Output Data 0
VOUT0_DATA1	B6	X_VOUT0_DATA1	O	3.3V <sup>1</sup>	Video Output Data 1
VOUT0_DATA2	B4	X_VOUT0_DATA2	O	3.3V <sup>1</sup>	Video Output Data 2
VOUT0_DATA3	B5	X_VOUT0_DATA3	O	3.3V <sup>1</sup>	Video Output Data 3
VOUT0_DATA4	B7	X_VOUT0_DATA4	O	3.3V <sup>1</sup>	Video Output Data 4
VOUT0_DATA5	B10	X_VOUT0_DATA5	O	3.3V <sup>1</sup>	Video Output Data 5
VOUT0_DATA6	B11	X_VOUT0_DATA6	O	3.3V <sup>1</sup>	Video Output Data 6
VOUT0_DATA7	B9	X_VOUT0_DATA7	O	3.3V <sup>1</sup>	Video Output Data 7
VOUT0_DATA8	B15	X_VOUT0_DATA8	O	3.3V <sup>1</sup>	Video Output Data 8
VOUT0_DATA9	B14	X_VOUT0_DATA9	O	3.3V <sup>1</sup>	Video Output Data 9
VOUT0_DATA10	A16	X_VOUT0_DATA10	O	3.3V <sup>1</sup>	Video Output Data 10
VOUT0_DATA11	A11	X_VOUT0_DATA11	O	3.3V <sup>1</sup>	Video Output Data 11
VOUT0_DATA12	A8	X_VOUT0_DATA12	O	3.3V <sup>1</sup>	Video Output Data 12
VOUT0_DATA13	A10	X_VOUT0_DATA13	O	3.3V <sup>1</sup>	Video Output Data 13
VOUT0_DATA14	A12	X_VOUT0_DATA14	O	3.3V <sup>1</sup>	Video Output Data 14
VOUT0_DATA15	A13	X_VOUT0_DATA15	O	3.3V <sup>1</sup>	Video Output Data 15
VOUT0_DATA16	D2	X_GPMCO_AD8/BOOTMODE_8 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Video Output Data 16
VOUT0_DATA17	D4	X_GPMCO_AD9/BOOTMODE_9 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Video Output Data 17
VOUT0_DATA18	D5	X_GPMCO_AD10/BOOTMODE_10 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Video Output Data 18
VOUT0_DATA19	D6	X_GPMCO_AD11/BOOTMODE_11 <sup>2</sup> (100K pulldown on SOM)	O	3.3V <sup>1</sup>	Video Output Data 19
VOUT0_DATA20	D7	X_GPMCO_AD12/BOOTMODE_12 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Video Output Data 20
VOUT0_DATA21	D8	X_GPMCO_AD13/BOOTMODE_13 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Video Output Data 21
VOUT0_DATA22	D10	X_GPMCO_AD14/BOOTMODE_14 <sup>2</sup> (100K pulldown on SOM)	O	3.3V <sup>1</sup>	Video Output Data 22
VOUT0_DATA23	D11	X_GPMCO_AD15/BOOTMODE_15 <sup>2</sup> (100K pulldown on SOM)	O	3.3V <sup>1</sup>	Video Output Data 23

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

<sup>2</sup>: This signal should not be driven during reset. More information can be found in section [6.3 System Boot Configuration](#).

## 8.2 OLDI/LVDS

The phyCORE-AM62xx SOM brings out two OLDI display ports each with up to four data lanes and one clock lane to support 21/28 bit serialized RGB pixel data and synchronization transmissions. The first port, OLDI0, consists of OLDI0\_A0-3/CLK0 and corresponds to odd pixels and the second port, OLDI1, consists of OLDI1\_A4-7/CLK1 and correspond to even pixels. More information about the supported video formats are discussed in the [AM62xx Technical Reference Manual](#).

### 8.2.1 OLDI/LVDS Pinout

**Table 32** OLDI/LVDS Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
OLDI0_A0N	A53	X_ODI0_A0N	I/O	Differential	OLDI Differential Data (negative)
OLDI0_A0P	A54	X_ODI0_A0P	I/O	Differential	OLDI Differential Data (positive)
OLDI0_A1N	A51	X_ODI0_A1N	I/O	Differential	OLDI Differential Data (negative)
OLDI0_A1P	A52	X_ODI0_A1P	I/O	Differential	OLDI Differential Data (positive)
OLDI0_A2N	A47	X_ODI0_A2N	I/O	Differential	OLDI Differential Data (negative)
OLDI0_A2P	A46	X_ODI0_A2P	I/O	Differential	OLDI Differential Data (positive)
OLDI0_A3N	A49	X_ODI0_A3N	I/O	Differential	OLDI Differential Data (negative)
OLDI0_A3P	A48	X_ODI0_A3P	I/O	Differential	OLDI Differential Data (positive)
OLDI0_A4N	B51	X_ODI0_A4N	I/O	Differential	OLDI Differential Data (negative)
OLDI0_A4P	B52	X_ODI0_A4P	I/O	Differential	OLDI Differential Data (positive)
OLDI0_A5N	B49	X_ODI0_A5N	I/O	Differential	OLDI Differential Data (negative)
OLDI0_A5P	B50	X_ODI0_A5P	I/O	Differential	OLDI Differential Data (positive)
OLDI0_A6N	B47	X_ODI0_A6N	I/O	Differential	OLDI Differential Data (negative)
OLDI0_A6P	B46	X_ODI0_A6P	I/O	Differential	OLDI Differential Data (positive)
OLDI0_A7N	B44	X_ODI0_A7N	I/O	Differential	OLDI Differential Data (negative)
OLDI0_A7P	B45	X_ODI0_A7P	I/O	Differential	OLDI Differential Data (positive)
OLDI0_CLK0N	A44	X_ODI0_CLK0N	I/O	Differential	OLDI Differential Clock (negative)
OLDI0_CLK0P	A43	X_ODI0_CLK0P	I/O	Differential	OLDI Differential Clock (positive)
OLDI0_CLK1N	B55	X_ODI0_CLK1N	I/O	Differential	OLDI Differential Clock (negative)
OLDI0_CLK1P	B54	X_ODI0_CLK1P	I/O	Differential	OLDI Differential Clock (positive)

### 8.2.2 OLDI/LVDS Design In Considerations

- Each OLDI supports up to 4x data lanes and 1x clock lane.
- More general differential pair routing guidelines are in section [4.10.1 High-Speed Differential Signal Routing Guidelines](#).

Table 33 phyCORE-AM62xx USBO Layout Characteristics

Signal Name	SOM Trace Length ( $\mu\text{m}$ )	Match Group	Recommended Length Match
OLDIO_A0N	20933	OLDIO	254 $\mu\text{m}$
OLDIO_A0P	21172		
OLDIO_A1N	20928		
OLDIO_A1P	21157		
OLDIO_A2N	21260		
OLDIO_A2P	21095		
OLDIO_A3N	21412		
OLDIO_A3P	21310		
OLDIO_CLK0N	21181		
OLDIO_CLK0P	21087		
OLDIO_A4N	19900	OLDI1	254 $\mu\text{m}$
OLDIO_A4P	19888		
OLDIO_A5N	20093		
OLDIO_A5P	20279		
OLDIO_A6N	20117		
OLDIO_A6P	20350		
OLDIO_A7N	19880		
OLDIO_A7P	19871		
OLDIO_CLK1N	20122		
OLDIO_CLK1P	20310		

### 8.2.3 OLDI/LVDS Reference Circuits

Example reference circuits for connecting the OLDI signals to a 40-pin connector are shown below.

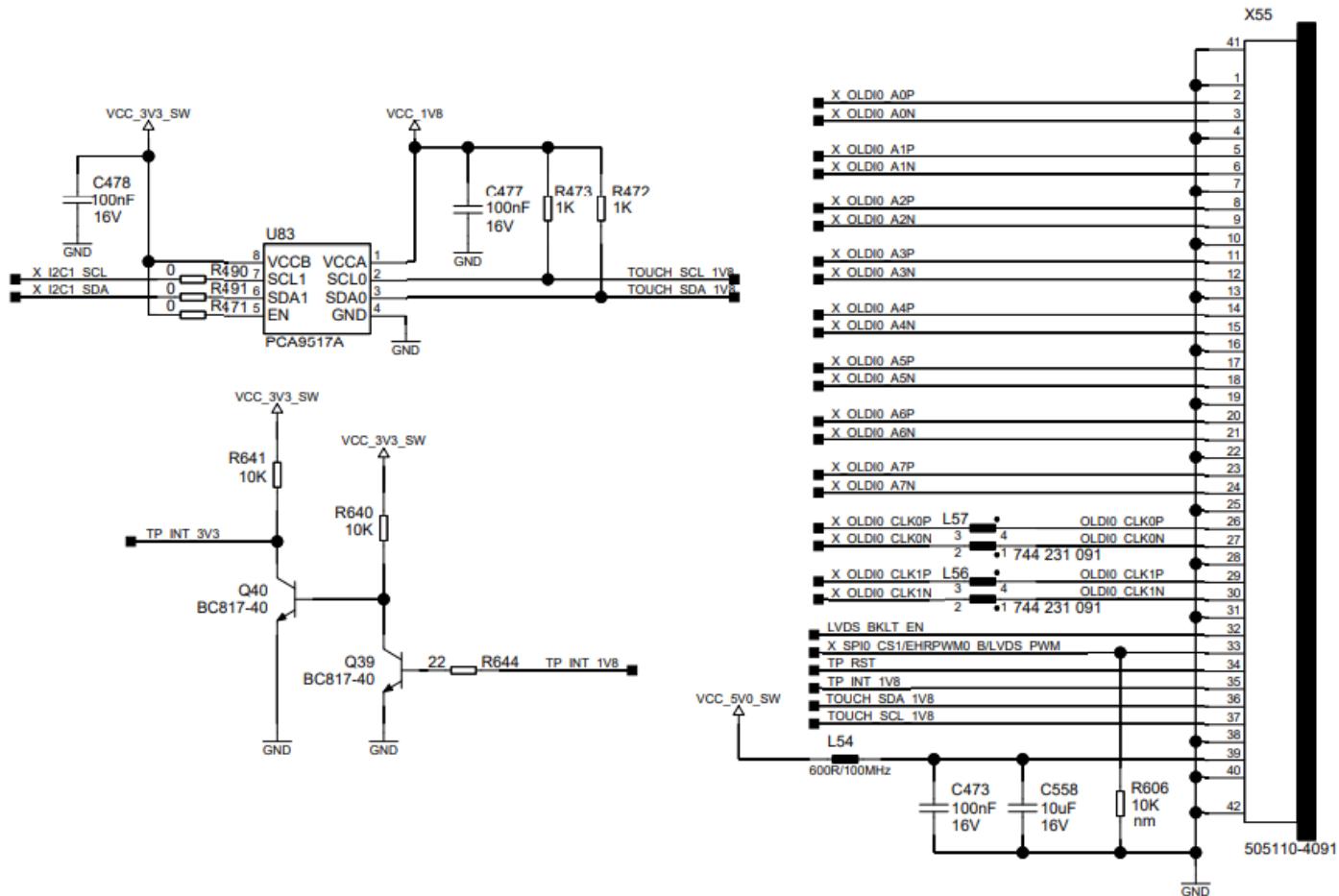


Figure 36. OLDI Connector Reference Schematic

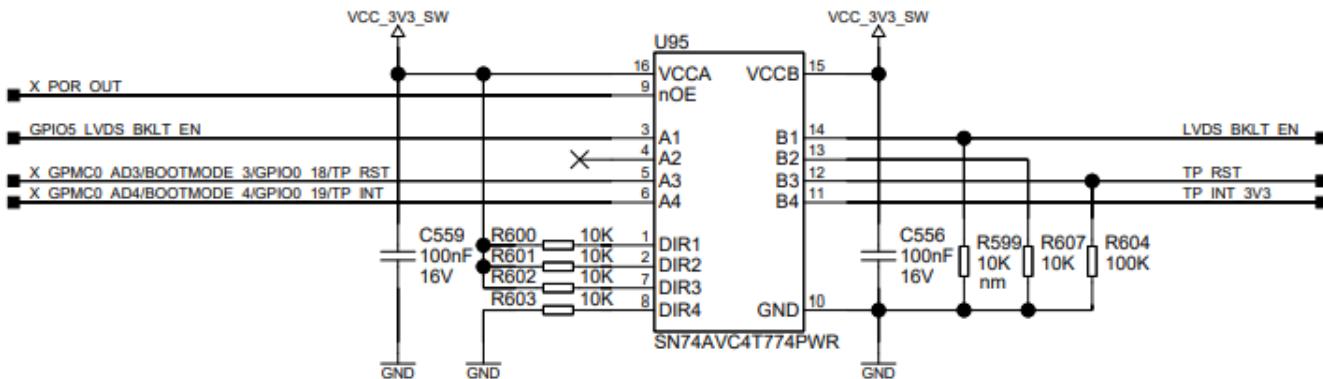


Figure 37. OLDI Level Translator Reference Schematic

The above circuits consist of the following parts:

- Two level translators for adjusting the voltage level/buffering the signals
- A transistor network for translating the interrupt signal
- A 40-pin FFC/FPC connector

## 8.3 CSI

The phyCORE-AM62xx SOM brings out one 4 lane CSI (camera serial interface). The CSI interfaces provide the following functionality:

- Compliant with MIPI CSI 1.3 and MIPI-DPHY 1.2
- Support for 1,2,3 or 4 data lane mode up to 2.5Gbps
- Supports up to 16 virtual channels per input

### 8.3.1 CSI Pinout

**Table 34 CSI Connections at the phyCORE-Connector**

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
CSI0_RXCLKN	B32	X_CSI0_RXCLKN	I	Differential	CSI Differential Receive Clock Input (negative)
CSI0_RXCLKP	B31	X_CSI0_RXCLKP	I	Differential	CSI Differential Receive Clock Input (positive)
CSI0_RXN0	A36	X_CSI0_RXN0	I	Differential	CSI Differential Receive Input (negative)
CSI0_RXP0	A35	X_CSI0_RXP0	I	Differential	CSI Differential Receive Input (positive)
CSI0_RXN1	A34	X_CSI0_RXN1	I	Differential	CSI Differential Receive Input (negative)
CSI0_RXP1	A33	X_CSI0_RXP1	I	Differential	CSI Differential Receive Input (positive)
CSI0_RXN2	B35	X_CSI0_RXN2	I	Differential	CSI Differential Receive Input (negative)
CSI0_RXP2	B34	X_CSI0_RXP2	I	Differential	CSI Differential Receive Input (positive)
CSI0_RXN3	B37	X_CSI0_RXN3	I	Differential	CSI Differential Receive Input (negative)
CSI0_RXP3	B36	X_CSI0_RXP3	I	Differential	CSI Differential Receive Input (positive)

### 8.3.2 CSI Design In Considerations

- CSI supports up to 4x data lanes and 1x clock lane.
- More general differential pair routing guidelines are in section [4.10.1 High-Speed Differential Signal Routing Guidelines](#).

**Table 35 phyCORE-AM62xx USB0 Layout Characteristics**

Signal Name	SOM Trace Length ( $\mu\text{m}$ )	Match Group	Recommended Length Match
CSI0_RXCLKN	16161	CSI	254 $\mu\text{m}$
CSI0_RXCLKP	16074		
CSI0_RXN0	16069		
CSI0_RXP0	15832		

CSI0_RXN1	16009		
CSI0_RXP1	15785		
CSI0_RXN2	16210		
CSI0_RXP2	15991		
CSI0_RXN3	15846		
CSI0_RXP3	15900		

### 8.3.3 CSI Reference Circuits

Example reference circuits for connecting the CSI signals to a 30-pin connector are shown below. The 30-pin connector pinout is designed to connect to a PHYTEC camera and supports both 3.3V and 5V cameras.

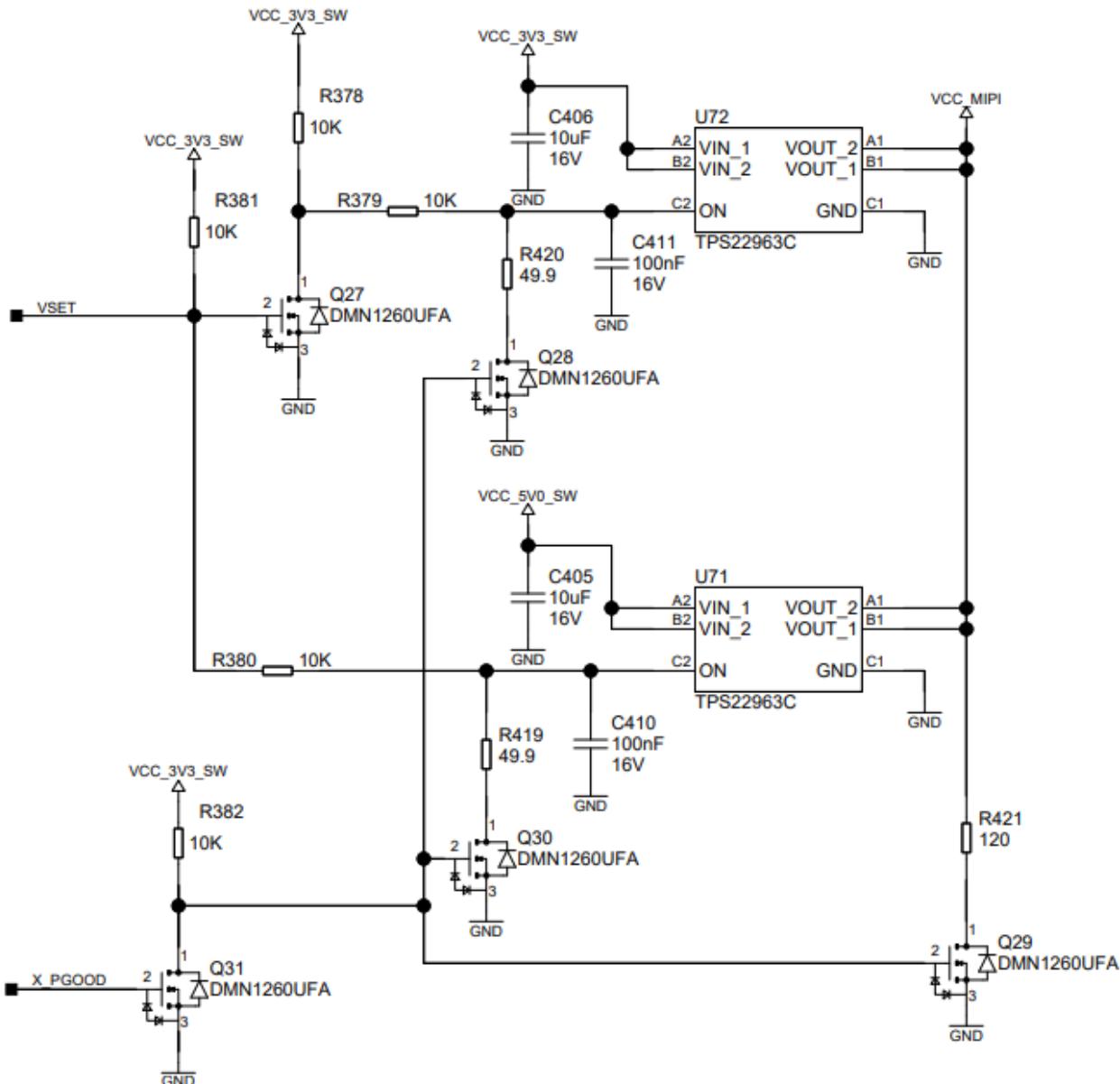


Figure 38. CSI Power Toggle Reference Schematic

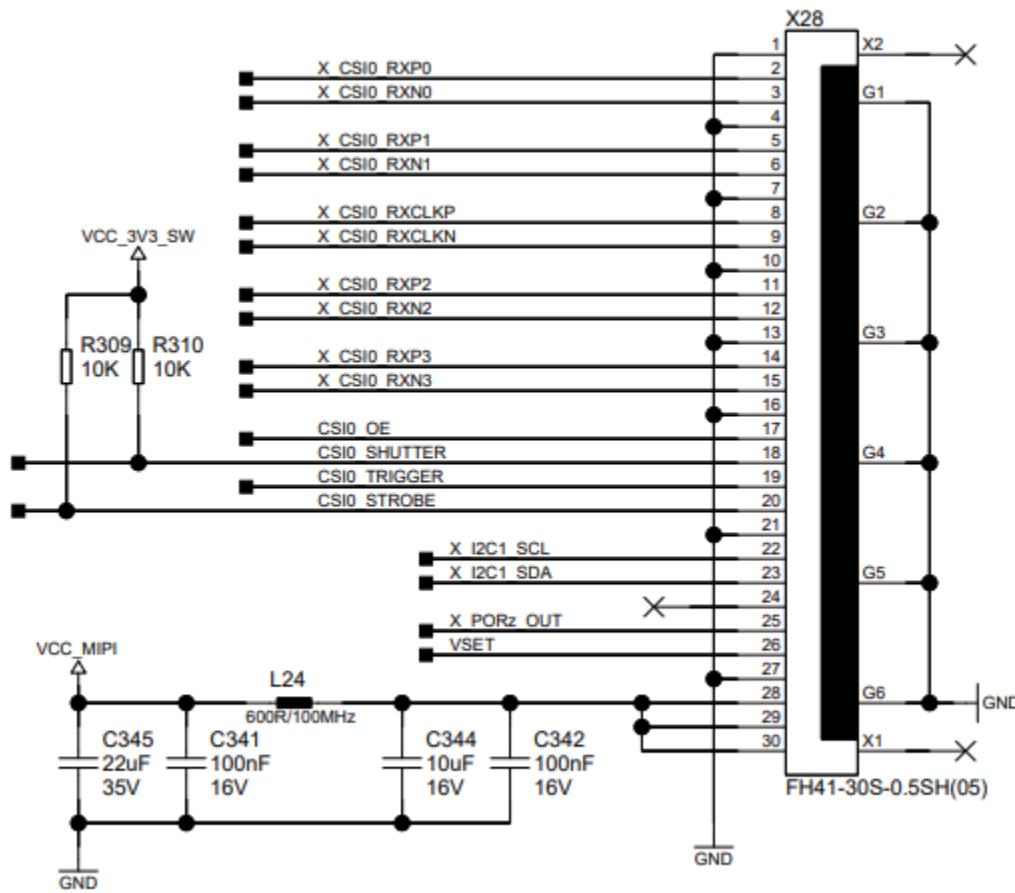


Figure 39. CSI Connector Reference Schematic

The above circuits consist of the following parts:

- A power circuit to swap between 5V and 3.3V voltage power
- A 30-pin FFC connector

## 9 Control Interfaces

The following sub-sections detail each of the control interfaces supported on the phyCORE-AM62xx.

### 9.1 Enhanced Capture

The phyCORE-AM62xx SOM brings out 4x Enhanced Capture (ECAP) modules.

## 9.1.1 ECAP Pinout

Table 36 ECAP Connections at the phyCORE-Connector

<b>Processor Signal</b>	<b>X1 Pin #(s)</b>	<b>SOM Signal(s)</b>	<b>Type</b>	<b>Level</b>	<b>Description</b>
ECAP0_IN_APWM_OUT	C60	X_EXT_REFCLK1	I/O	3.3V <sup>1</sup>	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output
	C41	X_SPI0_CS1			
ECAP1_IN_APWM_OUT	C35	X_I2C0_SCL (2.2K pullup on SOM)	I/O	3.3V <sup>1</sup>	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output
	D31	X_MCASPO_AXR1			
	C28	X_MCASPO_AXR3			
	C26	X_MMIC1_DAT1			
	D37	X_UART0_RXD			
ECAP2_IN_APWM_OUT	C34	X_I2C0_SDA (2.2K pullup on SOM)	I/O	3.3V <sup>1</sup>	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output
	C27	X_MCASPO_AXR2			
	C25	X_MMIC1_DAT0			
	C29	X_MCASPO_ACLKX			
	D38	X_UART0_TXD			
PRG0_ECAP0_IN_APWM_OUT	A7	X_VOUT0_PCLK	I/O	3.3V <sup>1</sup>	PRU-ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output
	A30	X_CPSW_RGMII2_TD2			
	D35	X_UART0_RTSN			
	D33	X_MCASPO_AXR0			
	C1	X_GPMCO_DIR			
PRG0_ECAP0_SYNC_IN	C40	X_SPI0_CS0	I	3.3V <sup>1</sup>	PRU-ICSSG ECAP Sync Input
	A18	X_CPSW_RGMII2_RXC			
PRG0_ECAP0_SYNC_OUT	D36	X_UART0_CTSN	O	3.3V <sup>1</sup>	PRU-ICSSG ECAP Sync Output
	A31	X_CPSW_RGMII2_TD3			

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

## 9.2 Enhanced Pulse-Width Modulation

The phyCORE-AM62xx SOM supports up to four Enhanced Pulse-Width Modulation (PWM) modules. Each PWM provides the following functionality:

- A dedicated 16-bit time-base counter with period and frequency control.
- Two PWM outputs that can be used as either:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation

## 9.2.1 EPWM Pinout

Table 37 EPWM Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
EHRPWM_SOCA	C35	X_I2C0_SCL (2.2K pullup on SOM)	O	3.3V <sup>1</sup>	EHRPWM Start of Conversion A
EHRPWM_SOCB	C34	X_I2C0_SDA (2.2K pullup on SOM)	O	3.3V <sup>1</sup>	EHRPWM Start of Conversion B
EHRPWM_TZn_IN0	D42	X_SPI0_D1	I	3.3V <sup>1</sup>	EHRPWM Trip Zone Input 2 (active low)
EHRPWM_TZn_IN3	C36	X_MCAN0_TX	I	3.3V <sup>1</sup>	EHRPWM Trip Zone Input 2 (active low)
EHRPWM_TZn_IN4	C37	X_MCAN0_RX	I	3.3V <sup>1</sup>	EHRPWM Trip Zone Input 2 (active low)
EHRPWM_TZn_IN5	C41	X_SPI0_CS1	I	3.3V <sup>1</sup>	EHRPWM Trip Zone Input 2 (active low)
EHRPWM0_A	C40	X_SPI0_CS0	I/O	3.3V <sup>1</sup>	EHRPWM Output A
	D32	X_MCASPO_AFSR			
EHRPWM0_B	C30	X_MCASPO_ACLKR	I/O	3.3V <sup>1</sup>	EHRPWM Output B
	C41	X_SPI0_CS1			
EHRPWM0_SYNCI	C32	X_I2C1_SCL	I	3.3V <sup>1</sup>	Sync Input to EHRPWM module from an external pin
EHRPWM0_SYNCO	C33	X_I2C1_SDA	O	3.3V <sup>1</sup>	Sync Output to EHRPWM module to an external pin
EHRPWM1_A	D40	X_SPI0_CLK	I/O	3.3V <sup>1</sup>	EHRPWM Output A
	D31	X_MCASPO_AXR1			
EHRPWM1_B	D41	X_SPI0_D0	I/O	3.3V <sup>1</sup>	EHRPWM Output B
	D33	X_MCASPO_AXR0			
EHRPWM2_A	C32	X_I2C1_SCL	I/O	3.3V <sup>1</sup>	EHRPWM Output A
	D37	X_UART0_RXD			
EHRPWM2_B	C33	X_I2C1_SDA	I/O	3.3V <sup>1</sup>	EHRPWM Output B
	D38	X_UART0_TXD			

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

## 9.3 Enhanced Quadrature Encoder Pulse

The phyCORE-AM62xx SOM brings out 3x Enhanced Quadrature Encoder Pulse (EQEP) modules.

### 9.3.1 EQEP Pinout

Table 38 EQEP Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
EQEPO_A	C28	X_MCASPO_AXR3	I	3.3V <sup>1</sup>	EQEP Quadrature Input A
EQEPO_B	C27	X_MCASPO_AXR2	I	3.3V <sup>1</sup>	EQEP Quadrature Input B
EQEPO_I	D33	X_MCASPO_AXR0	I/O	3.3V <sup>1</sup>	EQEP Index
EQEPO_S	D31	X_MCASPO_AXR1	I/O	3.3V <sup>1</sup>	EQEP Strobe
EQEP1_A	C29	X_MCASPO_ACLKX	I	3.3V <sup>1</sup>	EQEP Quadrature Input A
EQEP1_B	D30	X_MCASPO_AFSX	I	3.3V <sup>1</sup>	EQEP Quadrature Input B
EQEP1_I	C30	X_MCASPO_ACLKR	I/O	3.3V <sup>1</sup>	EQEP Index
EQEP1_S	D32	X_MCASPO_AFSR	I/O	3.3V <sup>1</sup>	EQEP Strobe
EQEP2_A	A21	X_CPSW_RGMII2_RD2	I	3.3V <sup>1</sup>	EQEP Quadrature Input A
	C35	X_I2C0_SCL (2.2K pullup on SOM)			

EQEP2_B	C34	X_I2C0_SDA (2.2K pullup on SOM)	I	3.3V <sup>1</sup>	EQEP Quadrature Input B
	A20	X_CPSW_RGMII2_RD3			
EQEP2_I	A30	X_CPSW_RGMII2_TD2	I/O	3.3V <sup>1</sup>	EQEP Index
	C36	X_MCAN0_TX			
EQEP2_S	D16	X_GPMCO_WAIT1	I/O	3.3V <sup>1</sup>	EQEP Strobe
	A31	X_CPSW_RGMII2_TD3			
EQEP2_S	C37	X_MCAN0_RX			
	C1	X_GPMCO_DIR			

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

## 10 Peripheral Interfaces

The following sub-sections detail each of the peripheral interfaces supported on the phyCORE-AM62xx.

### 10.1 CPTS

The phyCORE-AM62xx SOM brings out the Common Platform Time Sync (CPTS) module that is used to facilitate host control of time sync operations.

#### 10.1.1 CPTS Pinout

**Table 39 CPTS Connections at the phyCORE-Connector**

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
CP_GEMAC_CPTSO_RFT_CLK	C60	X_EXT_REFCLK1	I	3.3V <sup>1</sup>	CPTS Reference Clock
CP_GEMAC_CPTSO_TS_COMP	C41	X_SPI0_CS1	O	3.3V <sup>1</sup>	CPTS Time Stamp Counter Compare
	D29	X_MMC1_DAT3			
CP_GEMAC_CPTSO_TS_SYNC	D40	X_SPI0_CLK	O	3.3V <sup>1</sup>	CPTS Time Stamp Counter Bit
	D28	X_MMC1_DAT2			
CP_GEMAC_CPTSO_HW1TSPUSH	D41	X_SPI0_D0	I	3.3V <sup>1</sup>	CPTS Hardware Time Stamp Push 1
	C26	X_MMC1_DAT1			
CP_GEMAC_CPTSO_HW2TSPUSH	C25	X_MMC1_DATA0	I	3.3V <sup>1</sup>	CPTS Hardware Time Stamp Push 2
	D42	X_SPI0_D1			
SYNC0_OUT	C35	X_I2C0_SCL (2.2K pullup on SOM)	O	3.3V <sup>1</sup>	CPTS Time Stamp Generator Bit 0
SYNC1_OUT	C60	X_EXT_REFCLK1	O	3.3V <sup>1</sup>	CPTS Time Stamp Generator Bit 1
SYNC2_OUT	C36	X_MCAN0_TX	O	3.3V <sup>1</sup>	CPTS Time Stamp Generator Bit 2
SYNC3_OUT	C37	X_MCAN0_RX	O	3.3V <sup>1</sup>	CPTS Time Stamp Generator Bit 3

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

### 10.2 GPIO

The General-Purpose Input/Output interfaces provides pins that can be configured as either inputs or outputs. Many of the signals available at the phyCORE-Connector can be multiplexed as GPIOs. The AM62xx processor supports five independent GPIO modules:

- GPIO0

- GPIO1
- MCU\_GPIO0
- PRG0\_PRU0\_GPIO
- PRG0\_PRU1\_GPIO

The following table lists the number of GPIOs available from each of these GPIO modules at the phyCORE-Connector, with a total of 169 GPIOs available depending on the multiplexing configuration. Note that not all GPIOs can be used simultaneously as there is overlap of connector pins between the GPIO modules.

**Table 40 Total Available GPIO**

GPIO Module	Number of GPIO Available
GPIO0	65
GPIO1	42
MCU_GPIO0	22
PRG0_PRU0_GPIO	20
PRG0_PRU1_GPIO	20
Total	169

Many of the GPIOs are multiplexed with other interfaces, some of which connect to on-board circuits. Review the tables below when using these GPIOs to check for pull-up and pull-down resistors, connected devices, etc.

**CAUTION:**

The majority of the GPIO pins can be either 1.8V or 3.3V depending on the jumper settings. Take care when using these signals and consider the voltage levels.

## 10.2.1 GPIO Pinout

**Table 41 GPIO0 Accessibility at phyCORE-Connector**

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Internal SOM Usage
GPIO0_15	C4	X_GPMCO_AD0/BOOTMODE_0	I/O	3.3V <sup>1</sup>	100K pullup Do not drive during reset
GPIO0_16	C5	X_GPMCO_AD1/BOOTMODE_1	I/O	3.3V <sup>1</sup>	100K pullup Do not drive during reset
GPIO0_17	C7	X_GPMCO_AD2/BOOTMODE_2	I/O	3.3V <sup>1</sup>	100K pulldown Do not drive during reset
GPIO0_18	C8	X_GPMCO_AD3/BOOTMODE_3	I/O	3.3V <sup>1</sup>	100K pullup Do not drive during reset
GPIO0_19	C9	X_GPMCO_AD4/BOOTMODE_4	I/O	3.3V <sup>1</sup>	100K pulldown Do not drive during reset
GPIO0_20	C10	X_GPMCO_AD5/BOOTMODE_5	I/O	3.3V <sup>1</sup>	100K pulldown Do not drive during reset
GPIO0_21	C11	X_GPMCO_AD6/BOOTMODE_6	I/O	3.3V <sup>1</sup>	100K pullup Do not drive during reset
GPIO0_22	D1	X_GPMCO_AD7/BOOTMODE_7	I/O	3.3V <sup>1</sup>	100K pulldown Do not drive during reset
GPIO0_23	D2	X_GPMCO_AD8/BOOTMODE_8	I/O	3.3V <sup>1</sup>	100K pullup

<b>Processor Signal</b>	<b>X1 Pin #(s)</b>	<b>SOM Signal(s)</b>	<b>Type</b>	<b>Level</b>	<b>Internal SOM Usage</b>
					Do not drive during reset
GPIO0_24	D4	X_GPMCO_AD9/BOOTMODE_9	I/O	3.3V <sup>1</sup>	100K pullup Do not drive during reset
GPIO0_25	D5	X_GPMCO_AD10/BOOTMODE_10	I/O	3.3V <sup>1</sup>	100K pullup Do not drive during reset
GPIO0_26	D6	X_GPMCO_AD11/BOOTMODE_11	I/O	3.3V <sup>1</sup>	100K pulldown Do not drive during reset
GPIO0_27	D7	X_GPMCO_AD12/BOOTMODE_12	I/O	3.3V <sup>1</sup>	100K pullup Do not drive during reset
GPIO0_28	D8	X_GPMCO_AD13/BOOTMODE_13	I/O	3.3V <sup>1</sup>	100K pullup Do not drive during reset
GPIO0_29	D10	X_GPMCO_AD14/BOOTMODE_14	I/O	3.3V <sup>1</sup>	100K pulldown Do not drive during reset
GPIO0_30	D11	X_GPMCO_AD15/BOOTMODE_15	I/O	3.3V <sup>1</sup>	100K pulldown Do not drive during reset
GPIO0_31	C3	X_GPMCO_CLK	I/O	3.3V <sup>1</sup>	None
GPIO0_32	C15	X_GPMCO_ADVn_ALE	I/O	3.3V <sup>1</sup>	None
GPIO0_33	C17	X_GPMCO_OEn_REn	I/O	3.3V <sup>1</sup>	None
GPIO0_34	C13	X_GPMCO_WEn	I/O	3.3V <sup>1</sup>	None
GPIO0_35	C16	X_GPMCO_BE0n_CLE	I/O	3.3V <sup>1</sup>	None
GPIO0_36	C18	X_GPMCO_BE1n	I/O	3.3V <sup>1</sup>	None
GPIO0_37	C2	X_GPMCO_WAIT0	I/O	3.3V <sup>1</sup>	None
GPIO0_38	D16	X_GPMCO_WAIT1	I/O	3.3V <sup>1</sup>	None
GPIO0_39	D15	X_GPMCO_WPn	I/O	3.3V <sup>1</sup>	None
GPIO0_40	C1	X_GPMCO_DIR	I/O	3.3V <sup>1</sup>	None
GPIO0_41	D12	X_GPMCO_CSn0	I/O	3.3V <sup>1</sup>	None
GPIO0_42	D13	X_GPMCO_CSn1	I/O	3.3V <sup>1</sup>	None
GPIO0_43	D14	X_GPMCO_CSn2	I/O	3.3V <sup>1</sup>	None
GPIO0_44	C14	X_GPMCO_CSn3	I/O	3.3V <sup>1</sup>	None
GPIO0_45	B12	X_VOUT0_DATA0	I/O	3.3V <sup>1</sup>	None
GPIO0_46	B6	X_VOUT0_DATA1	I/O	3.3V <sup>1</sup>	None
GPIO0_47	B4	X_VOUT0_DATA2	I/O	3.3V <sup>1</sup>	None
GPIO0_48	B5	X_VOUT0_DATA3	I/O	3.3V <sup>1</sup>	None
GPIO0_49	B7	X_VOUT0_DATA4	I/O	3.3V <sup>1</sup>	None
GPIO0_50	B10	X_VOUT0_DATA5	I/O	3.3V <sup>1</sup>	None
GPIO0_51	B11	X_VOUT0_DATA6	I/O	3.3V <sup>1</sup>	None
GPIO0_52	B9	X_VOUT0_DATA7	I/O	3.3V <sup>1</sup>	None
GPIO0_53	B15	X_VOUT0_DATA8	I/O	3.3V <sup>1</sup>	None
GPIO0_54	B14	X_VOUT0_DATA9	I/O	3.3V <sup>1</sup>	None
GPIO0_55	A16	X_VOUT0_DATA10	I/O	3.3V <sup>1</sup>	None
GPIO0_56	A11	X_VOUT0_DATA11	I/O	3.3V <sup>1</sup>	None
GPIO0_57	A8	X_VOUT0_DATA12	I/O	3.3V <sup>1</sup>	None
GPIO0_58	A10	X_VOUT0_DATA13	I/O	3.3V <sup>1</sup>	None
GPIO0_59	A12	X_VOUT0_DATA14	I/O	3.3V <sup>1</sup>	None
GPIO0_60	A13	X_VOUT0_DATA15	I/O	3.3V <sup>1</sup>	None
GPIO0_61	A6	X_VOUT0_HSYNC	I/O	3.3V <sup>1</sup>	None
GPIO0_62	A15	X_VOUT0_DE	I/O	3.3V <sup>1</sup>	None

<b>Processor Signal</b>	<b>X1 Pin #(s)</b>	<b>SOM Signal(s)</b>	<b>Type</b>	<b>Level</b>	<b>Internal SOM Usage</b>
GPIO0_63	A5	X_VOUT0_VSYNC	I/O	3.3V <sup>1</sup>	None
GPIO0_64	A7	X_VOUT0_PCLK	I/O	3.3V <sup>1</sup>	None
GPIO0_65	D23	X_MMC2_DAT3	I/O	3.3V <sup>1</sup>	None
GPIO0_66	D24	X_MMC2_DAT2	I/O	3.3V <sup>1</sup>	None
GPIO0_67	D21	X_MMC2_DAT1	I/O	3.3V <sup>1</sup>	None
GPIO0_68	D20	X_MMC2_DAT0	I/O	3.3V <sup>1</sup>	None
GPIO0_69	D18	X_MMC2_CLK	I/O	3.3V <sup>1</sup>	49.9K pulldown
GPIO0_70	D19	X_MMC2_CMD	I/O	3.3V <sup>1</sup>	None
GPIO0_71	C20	X_MMC2_SDCD	I/O	3.3V <sup>1</sup>	10K pullup
GPIO0_72	C21	X_MMC2_SDWP	I/O	3.3V <sup>1</sup>	10K pullup
GPIO0_85	B17	X_MDIO0_MDIO (1.5K pullup)	I/O	3.3V <sup>1</sup>	None
GPIO0_86	B16	X_MDIO0_MDC (1.5K pullup)	I/O	3.3V <sup>1</sup>	None
GPIO0_87	A26	X_CPSW_RGMII2_TX_CTL	I/O	3.3V <sup>1</sup>	None
GPIO0_88	A25	X_CPSW_RGMII2_TXC	I/O	3.3V <sup>1</sup>	None
GPIO0_89	A27	X_CPSW_RGMII2_TDO	I/O	3.3V <sup>1</sup>	None
GPIO0_90	A28	X_CPSW_RGMII2_TD1	I/O	3.3V <sup>1</sup>	None
GPIO0_91	A30	X_CPSW_RGMII2_TD2	I/O	3.3V <sup>1</sup>	None

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

**Table 42 GPIO1 Accessibility at phyCORE-Connector**

<b>Processor Signal</b>	<b>X1 Pin #(s)</b>	<b>SOM Signal(s)</b>	<b>Type</b>	<b>Level</b>	<b>Internal SOM Usage</b>
GPIO1_0	A31	X_CPSW_RGMII2_TD3	I/O	3.3V <sup>1</sup>	None
GPIO1_1	A17	X_CPSW_RGMII2_RX_CTL	I/O	3.3V <sup>1</sup>	None
GPIO1_2	A18	X_CPSW_RGMII2_RXC	I/O	3.3V <sup>1</sup>	None
GPIO1_3	A23	X_CPSW_RGMII2_RD0	I/O	3.3V <sup>1</sup>	None
GPIO1_4	A22	X_CPSW_RGMII2_RD1	I/O	3.3V <sup>1</sup>	None
GPIO1_5	A21	X_CPSW_RGMII2_RD2	I/O	3.3V <sup>1</sup>	None
GPIO1_6	A20	X_CPSW_RGMII2_RD3	I/O	3.3V <sup>1</sup>	None
GPIO1_7	C28	X_MCASPO_AXR3	I/O	3.3V <sup>1</sup>	None
GPIO1_8	C27	X_MCASPO_AXR2	I/O	3.3V <sup>1</sup>	None
GPIO1_9	D31	X_MCASPO_AXR1	I/O	3.3V <sup>1</sup>	None
GPIO1_10	D33	X_MCASPO_AXR0	I/O	3.3V <sup>1</sup>	None
GPIO1_11	C29	X_MCASPO_ACLKX	I/O	3.3V <sup>1</sup>	None
GPIO1_12	D30	X_MCASPO_AFSX	I/O	3.3V <sup>1</sup>	None
GPIO1_13	D32	X_MCASPO_AFSR	I/O	3.3V <sup>1</sup>	None
GPIO1_14	C30	X_MCASPO_ACLKR	I/O	3.3V <sup>1</sup>	None
GPIO1_15	C40	X_SPI0_CS0	I/O	3.3V <sup>1</sup>	None
GPIO1_16	C41	X_SPI0_CS1	I/O	3.3V <sup>1</sup>	None
GPIO1_17	D40	X_SPI0_CLK	I/O	3.3V <sup>1</sup>	None
GPIO1_18	D41	X_SPI0_D0	I/O	3.3V <sup>1</sup>	None
GPIO1_19	D42	X_SPI0_D1	I/O	3.3V <sup>1</sup>	None
GPIO1_20	D37	X_UART0_RXD	I/O	3.3V <sup>1</sup>	None
GPIO1_21	D38	X_UART0_TXD	I/O	3.3V <sup>1</sup>	None
GPIO1_22	D36	X_UART0_CTSN	I/O	3.3V <sup>1</sup>	None

<b>Processor Signal</b>	<b>X1 Pin #(s)</b>	<b>SOM Signal(s)</b>	<b>Type</b>	<b>Level</b>	<b>Internal SOM Usage</b>
GPIO1_23	D35	X_UART0_RTSN	I/O	3.3V <sup>1</sup>	None
GPIO1_24	C36	X_MCAN0_TX	I/O	3.3V <sup>1</sup>	None
GPIO1_25	C37	X_MCAN0_RX	I/O	3.3V <sup>1</sup>	None
GPIO1_26	C35	X_I2C0_SCL	I/O	3.3V <sup>1</sup>	2.2K pullup
GPIO1_27	C34	X_I2C0_SDA	I/O	3.3V <sup>1</sup>	2.2K pullup
GPIO1_28	C32	X_I2C1_SCL	I/O	3.3V <sup>1</sup>	None
GPIO1_29	C33	X_I2C1_SDA	I/O	3.3V <sup>1</sup>	None
GPIO1_30	C60	X_EXT_REFCLK1	I/O	3.3V <sup>1</sup>	None
GPIO1_31	C39	X_RTC_INT	I/O	3.3V <sup>1</sup>	10K pullup
GPIO1_42	D29	X_MMC1_DAT3	I/O	3.3V <sup>1</sup>	None
GPIO1_43	D28	X_MMC1_DAT2	I/O	3.3V <sup>1</sup>	None
GPIO1_44	C26	X_MMC1_DAT1	I/O	3.3V <sup>1</sup>	None
GPIO1_45	C25	X_MMC1_DAT0	I/O	3.3V <sup>1</sup>	None
GPIO1_46	D26	X_MMC1_CLK	I/O	3.3V <sup>1</sup>	49.9K pulldown
GPIO1_47	D25	X_MMC1_CMD	I/O	3.3V <sup>1</sup>	None
GPIO1_48	C23	X_MMC1_SDCD	I/O	3.3V <sup>1</sup>	10K pullup
GPIO1_49	C22	X_MMC1_SDWP	I/O	3.3V <sup>1</sup>	10K pullup
GPIO1_50	A41	X_USB0_DRVVBUS	I/O	3.3V <sup>1</sup>	None
GPIO1_51	B42	X_USB1_DRVVBUS	I/O	3.3V <sup>1</sup>	None

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

**Table 43 MCU\_GPIO0 Accessibility at phyCORE-Connector**

<b>Processor Signal</b>	<b>X1 Pin #(s)</b>	<b>SOM Signal(s)</b>	<b>Type</b>	<b>Level</b>	<b>Internal SOM Usage</b>
MCU_GPIO0_1	D49	X_MCU_SPI0_CS1	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_2	D46	X_MCU_SPI0_CLK	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_3	D47	X_MCU_SPI0_D0	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_4	D48	X_MCU_SPI0_D1	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_5	D55	X_MCU_UART0_RXD	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_6	D56	X_MCU_UART0_TXD	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_7	D53	X_MCU_UART0_CTSN	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_8	D54	X_MCU_UART0_RTSN	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_9	B58	X_WKUP_UART0_RXD	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_10	B57	X_WKUP_UART0_TXD	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_11	A56	X_WKUP_UART0_CTSN	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_12	B59	X_WKUP_UART0_RTSN	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_13	A57	X_MCU_MCAN0_TX	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_14	A58	X_MCU_MCAN0_RX	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_15	A59	X_MCU_MCAN1_TX	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_16	A60	X_MCU_MCAN1_RX	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_17	C49	X_MCU_I2C0_SCL	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_18	C50	X_MCU_I2C0_SDA	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_19	D50	X_WKUP_I2C0_SCL	I/O	3.3V <sup>1</sup>	None
MCU_GPIO0_20	D51	X_WKUP_I2C0_SDA	I/O	3.3V <sup>1</sup>	None

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Internal SOM Usage
MCU_GPIO0_21	C55	X MCU_RESETSTATz	I/O	3.3V <sup>1</sup>	10K pulldown
MCU_GPIO0_23	D60	X_WKUP_CLKOUT0	I/O	3.3V <sup>1</sup>	10K pulldown

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

**Table 44 PRO\_PRU0\_GPIO Accessibility at phyCORE-Connector**

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Internal SOM Usage
PRO_PRU0_GPIO/GPO0	A17	X_CPSW_RGMII2_RX_CTL	I/O	3.3V <sup>1</sup>	None
	C4	X_GPMCO_ADO/BOOTMODE_0 <sup>2</sup> (100K pullup on SOM)			
	D7	X_GPMCO_AD12/BOOTMODE_12 <sup>2</sup> (100K pullup on SOM)			
	A16	X_VOUT0_DATA10			
PRO_PRU0_GPI1/GPO1	A11	X_VOUT0_DATA11	I/O	3.3V <sup>1</sup>	None
	A18	X_CPSW_RGMII2_RXC			
	C5	X_GPMCO_AD1/BOOTMODE_1 <sup>2</sup> (100K pullup on SOM)			
	D8	X_GPMCO_AD13/BOOTMODE_13 <sup>2</sup> (100K pullup on SOM)			
PRO_PRU0_GPI2/GPO2	A8	X_VOUT0_DATA12	I/O	3.3V <sup>1</sup>	None
	A23	X_CPSW_RGMII2_RD0			
	C7	X_GPMCO_AD2/BOOTMODE_2 <sup>2</sup> (100K pulldown on SOM)			
	D10	X_GPMCO_AD14/BOOTMODE_14 <sup>2</sup> (100K pulldown on SOM)			
PRO_PRU0_GPI3/GPO3	A10	X_VOUT0_DATA13	I/O	3.3V <sup>1</sup>	None
	A22	X_CPSW_RGMII2_RD1			
	C8	X_GPMCO_AD3/BOOTMODE_3 <sup>2</sup> (100K pullup on SOM)			
	D11	X_GPMCO_AD15/BOOTMODE_15 <sup>2</sup> (100K pulldown on SOM)			
PRO_PRU0_GPI4/GPO4	A21	X_CPSW_RGMII2_RD2	I/O	3.3V <sup>1</sup>	None
	C9	X_GPMCO_AD4/BOOTMODE_4 <sup>2</sup> (100K pulldown on SOM)			
	A12	X_VOUT0_DATA14			
PRO_PRU0_GPI5/GPO5	A13	X_VOUT0_DATA15	I/O	3.3V <sup>1</sup>	None
	C10	X_GPMCO_AD5/BOOTMODE_5 <sup>2</sup> (100K pulldown on SOM)			
PRO_PRU0_GPI6/GPO6	A6	X_VOUT0_HSYNC	I/O	3.3V <sup>1</sup>	None
	C11	X_GPMCO_AD6/BOOTMODE_6 <sup>2</sup> (100K pullup on SOM)			
PRO_PRU0_GPI7/GPO7	D1	X_GPMCO_AD7/BOOTMODE_7 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	None
	A15	X_VOUT0_DE			
PRO_PRU0_GPI8/GPO8	C3	X_GPMCO_CLK	I/O	3.3V <sup>1</sup>	None
	B12	X_VOUT0_DATA0			
PRO_PRU0_GPI9/GPO9	C15	X_GPMCO_ADVn_ALE	I/O	3.3V <sup>1</sup>	None

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Internal SOM Usage
PRO_PRU0_GPI10/GPO10	B6	X_VOUT0_DATA1	I/O	3.3V <sup>1</sup>	None
	C17	X_GPMCO_OEn_REn			
	B4	X_VOUT0_DATA2			
PRO_PRU0_GPI11/GPO11	C13	X_GPMCO_WEn	I/O	3.3V <sup>1</sup>	None
	B5	X_VOUT0_DATA3			
PRO_PRU0_GPI12/GPO12	C16	X_GPMCO_BEOn_CLE	I/O	3.3V <sup>1</sup>	None
	B7	X_VOUT0_DATA4			
PRO_PRU0_GPI13/GPO13	C18	X_GPMCO_BE1n	I/O	3.3V <sup>1</sup>	None
	B10	X_VOUT0_DATA5			
PRO_PRU0_GPI14/GPO14	C2	X_GPMCO_WAIT0	I/O	3.3V <sup>1</sup>	None
	B11	X_VOUT0_DATA6			
PRO_PRU0_GPI15/GPO15	B9	X_VOUT0_DATA7	I/O	3.3V <sup>1</sup>	None
	D15	X_GPMCO_WPn			
PRO_PRU0_GPI16/GPO16	A20	X_CPSW_RGMII2_RD3	I/O	3.3V <sup>1</sup>	None
	C1	X_GPMCO_DIR			
	B14	X_VOUT0_DATA9			
PRO_PRU0_GPI17/GPO17	D12	X_GPMCO_CSn0	I/O	3.3V <sup>1</sup>	None
	B15	X_VOUT0_DATA8			
PRO_PRU0_GPI18/GPO18	A5	X_VOUT0_VSYNC	I/O	3.3V <sup>1</sup>	None
	D13	X_GPMCO_CSn1			
PRO_PRU0_GPI19/GPO19	A7	X_VOUT0_PCLK	I/O	3.3V <sup>1</sup>	None
	D14	X_GPMCO_CSn2			

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

<sup>2</sup>: This signal should not be driven during reset. More information can be found in section [6.3 System Boot Configuration](#).

**Table 45 PRO\_PRU1\_GPIO Accessibility at phyCORE-Connector**

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Internal SOM Usage
PRO_PRU1_GPI0/GPO0	A26	X_CPSW_RGMII2_TX_CTL	I/O	3.3V <sup>1</sup>	None
	D2	X_GPMCO_AD8/BOOTMODE_8 <sup>2</sup> (100K pullup on SOM)			
	B12	X_VOUT0_DATA0			
PRO_PRU1_GPI1/GPO1	A25	X_CPSW_RGMII2_TXC	I/O	3.3V <sup>1</sup>	None
	D4	X_GPMCO_AD9/BOOTMODE_9 <sup>2</sup> (100K pullup on SOM)			
	B6	X_VOUT0_DATA1			
PRO_PRU1_GPI2/GPO2	D5	X_GPMCO_AD10/BOOTMODE_10 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	None
	B4	X_VOUT0_DATA2			
	A27	X_CPSW_RGMII2_TD0			
PRO_PRU1_GPI3/GPO3	A28	X_CPSW_RGMII2_TD1	I/O	3.3V <sup>1</sup>	None
	D6	X_GPMCO_AD11/BOOTMODE_11 <sup>2</sup> (100K pulldown on SOM)			
	B5	X_VOUT0_DATA3			
PRO_PRU1_GPI4/GPO4	A30	X_CPSW_RGMII2_TD2	I/O	3.3V <sup>1</sup>	None
	B7	X_VOUT0_DATA4			

PRO_PRU1_GPI5/GPO5	B10	X_VOUT0_DATA5	I/O	3.3V <sup>1</sup>	None
PRO_PRU1_GPI6/GPO6	B11	X_VOUT0_DATA6	I/O	3.3V <sup>1</sup>	None
PRO_PRU1_GPI7/GPO7	B9	X_VOUT0_DATA7	I/O	3.3V <sup>1</sup>	None
PRO_PRU1_GPI8/GPO8	C4	X_GPMCO_AD0/BOOTMODE_0 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	None
	B14	X_VOUT0_DATA9			
PRO_PRU1_GPI9/GPO9	C5	X_GPMCO_AD1/BOOTMODE_1 <sup>2</sup> (100K pullup on SOM)	I/O	3.3V <sup>1</sup>	None
	A16	X_VOUT0_DATA10			
PRO_PRU1_GPI10/GPO10	A11	X_VOUT0_DATA11	I/O	3.3V <sup>1</sup>	None
	C7	X_GPMCO_AD2/BOOTMODE_2 <sup>2</sup> (100K pulldown on SOM)			
PRO_PRU1_GPI11/GPO11	A8	X_VOUT0_DATA12	I/O	3.3V <sup>1</sup>	None
	C8	X_GPMCO_AD3/BOOTMODE_3 <sup>2</sup> (100K pullup on SOM)			
PRO_PRU1_GPI12/GPO12	A10	X_VOUT0_DATA13	I/O	3.3V <sup>1</sup>	None
	C9	X_GPMCO_AD4/BOOTMODE_4 <sup>2</sup> (100K pulldown on SOM)			
PRO_PRU1_GPI13/GPO13	C10	X_GPMCO_AD5/BOOTMODE_5 <sup>2</sup> (100K pulldown on SOM)	I/O	3.3V <sup>1</sup>	None
	A12	X_VOUT0_DATA14			
PRO_PRU1_GPI14/GPO14	A13	X_VOUT0_DATA15	I/O	3.3V <sup>1</sup>	None
	C11	X_GPMCO_AD6/BOOTMODE_6 <sup>2</sup> (100K pullup on SOM)			
PRO_PRU1_GPI15/GPO15	A6	X_VOUT0_HSYNC	I/O	3.3V <sup>1</sup>	None
	D1	X_GPMCO_AD7/BOOTMODE_7 <sup>2</sup> (100K pulldown on SOM)			
PRO_PRU1_GPI16/GPO16	A31	X_CPSW_RGMII2_TD3	I/O	3.3V <sup>1</sup>	None
	D13	X_GPMCO_CSn1			
	B15	X_VOUT0_DATA8			
PRO_PRU1_GPI17/GPO17	A15	X_VOUT0_DE	I/O	3.3V <sup>1</sup>	None
PRO_PRU1_GPI18/GPO18	A5	X_VOUT0_VSYNC	I/O	3.3V <sup>1</sup>	1.5K pullup
PRO_PRU1_GPI19/GPO19	A7	X_VOUT0_PCLK	I/O	3.3V <sup>1</sup>	1.5K pullup

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

<sup>2</sup>: This signal should not be driven during reset. More information can be found in section [6.3 System Boot Configuration](#).

## 10.3 TIMER

The phyCORE-AM62xx SOM brings out 12x Timer modules. The modules have a 32-bit data bus width and provide interrupts generated on overflow, compare, and capture.

### 10.3.1 Timer Pinout

**Table 46 Timer Signals**

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
TIMER_IO0	C32	X_I2C1_SCL	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
	D29	X_MMC1_DAT3			
TIMER_IO1	C33	X_I2C1_SDA	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
	D28	X_MMC1_DAT2			
TIMER_IO2	C26	X_MMC1_DAT1	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
	C36	X_MCAN0_TX			
TIMER_IO3	C25	X_MMC1_DAT0	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
	C37	X_MCAN0_RX			
TIMER_IO4	C60	X_EXT_REFCLK1	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
	D26	X_MMC1_CLK (49.9K pulldown on SOM)			
TIMER_IO5	C34	X_I2C0_SDA (2.2K pullup on SOM)	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
	D25	X_MMC1_CMD			
TIMER_IO6	D36	X_UART0_CTSN	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
	C23	X_MMC1_SDCD (10K pullup on SOM)			
TIMER_IO7	D35	X_UART0_RTSN	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
	C22	X_MMC1_SDWP (10K pullup on SOM)			
MCU_TIMER_IO0	D53	X MCU_UART0_CTSN	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
	A58	X MCU_MCAN0_RX			
MCU_TIMER_IO1	D54	X MCU_UART0_RTSN	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
	D49	X MCU_SPI0_CS1			
MCU_TIMER_IO2	A59	X MCU_MCAN1_TX	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs
MCU_TIMER_IO3	A60	X MCU_MCAN1_RX	I/O	3.3V <sup>1</sup>	Timer Inputs and Outputs

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

## 11 Debug Interfaces

The following sub-sections detail each of the debug interfaces supported on the phyCORE-AM62xx.

### 11.1 JTAG

The phyCORE-AM62xx SOM is equipped with a JTAG interface for downloading program code into the internal RAM or for debugging programs currently executing. The JTAG interface is accessible via the phyCORE-Connector and provides seven standard IEEE1149.6 JTAG signals.

## 11.1.1 JTAG Pinout

Table 47 JTAG Connections at the phyCORE-Connector

X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
D43	X_EMU0 <sup>2</sup> (5.76K pullup on SOM)	I/O	3.3V <sup>1</sup>	Emulation Control 0
D44	X_EMU1 <sup>2</sup> (5.76K pullup on SOM)	I/O	3.3V <sup>1</sup>	Emulation Control 1
C42	X_JTCK (10K pullup on SOM)	I	3.3V <sup>1</sup>	JTAG Test Clock
C44	X_TDI (10K pullup on SOM)	I	3.3V <sup>1</sup>	JTAG Test Data Input
C46	X_TDO	O	3.3V <sup>1</sup>	JTAG Test Data Output
C45	X_TMS (10K pullup on SOM)	I	3.3V <sup>1</sup>	JTAG Test Mode Select
C47	X_TRSTN (10K pulldown on SOM)	I	3.3V <sup>1</sup>	JTAG Reset

1: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

2: The signal brought out at this pin is controlled by a jumper. Refer to section [4.6 Solder Jumpers](#) for details.

## 11.1.2 JTAG Reference Circuit

An example reference circuit for connecting the JTAG signals to a 2x20 connector is shown below. Note that the pinout is based on TI's compact 20-pin JTAG connector setup. More details on the specifics of that pinout can be found here [JTAG Connectors and Pinout](#).

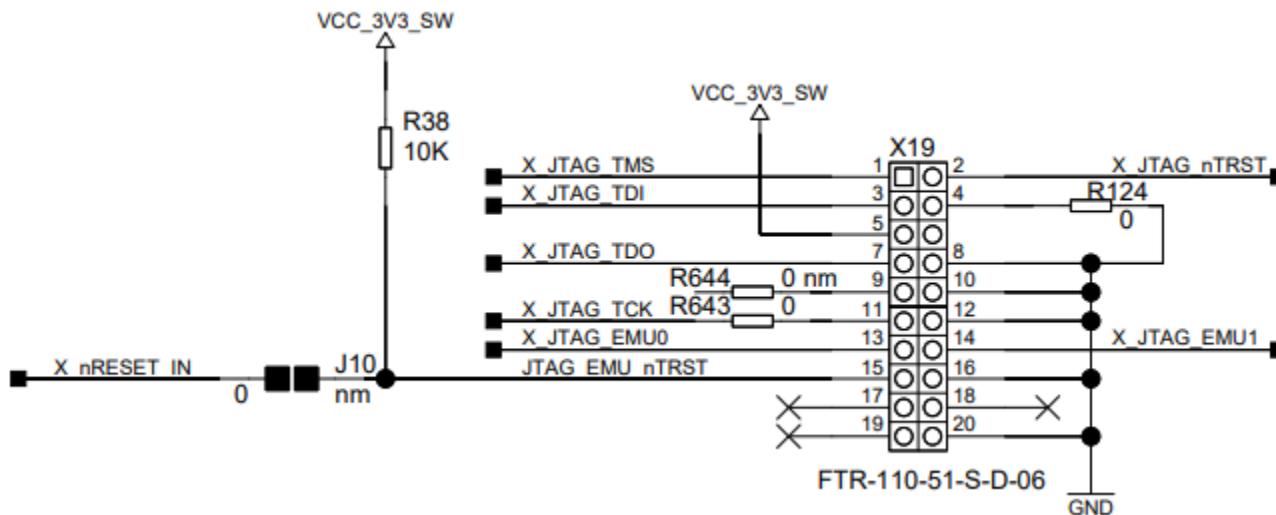


Figure 40. JTAG Reference Schematic

## 11.2 TRACE (TRC)

The phyCORE-AM62xx SOM is equipped with a TRACE (TRC) module that can be used to record operation of the ROM code and debug unexpected occurrences.

### 11.2.1 TRC Pinout

Table 48 TRC Connections at the phyCORE-Connector

<b>Processor Signal</b>	<b>X1 Pin #(s)</b>	<b>SOM Signal(s)</b>	<b>Type</b>	<b>Level</b>	<b>Description</b>
TRC_CLK	C4	X_GPMCO_AD0/BOOTMODE_0 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Trace Clock
TRC_CTL	C5	X_GPMCO_AD1/BOOTMODE_1 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Trace Control
TRC_DATA0	C7	X_GPMCO_AD2/BOOTMODE_2 <sup>2</sup> (100K pulldown on SOM)	O	3.3V <sup>1</sup>	Trace Data 0
TRC_DATA1	C8	X_GPMCO_AD3/BOOTMODE_3 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Trace Data 1
TRC_DATA2	C9	X_GPMCO_AD4/BOOTMODE_4 <sup>2</sup> (100K pulldown on SOM)	O	3.3V <sup>1</sup>	Trace Data 2
TRC_DATA3	C10	X_GPMCO_AD5/BOOTMODE_5 <sup>2</sup> (100K pulldown on SOM)	O	3.3V <sup>1</sup>	Trace Data 3
TRC_DATA4	C11	X_GPMCO_AD6/BOOTMODE_6 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Trace Data 4
TRC_DATA5	D1	X_GPMCO_AD7/BOOTMODE_7 <sup>2</sup> (100K pulldown on SOM)	O	3.3V <sup>1</sup>	Trace Data 5
TRC_DATA6	C3	X_GPMCO_CLK	O	3.3V <sup>1</sup>	Trace Data 6
TRC_DATA7	C15	X_GPMCO_ADVn_ALE	O	3.3V <sup>1</sup>	Trace Data 7
TRC_DATA8	C17	X_GPMCO_OEn_REn	O	3.3V <sup>1</sup>	Trace Data 8
TRC_DATA9	C13	X_GPMCO_WEn	O	3.3V <sup>1</sup>	Trace Data 9
TRC_DATA10	C16	X_GPMCO_BEOn_CLE	O	3.3V <sup>1</sup>	Trace Data 10
TRC_DATA11	C18	X_GPMCO_BE1n	O	3.3V <sup>1</sup>	Trace Data 11
TRC_DATA12	C2	X_GPMCO_WAIT0	O	3.3V <sup>1</sup>	Trace Data 12
TRC_DATA13	D15	X_GPMCO_WPn	O	3.3V <sup>1</sup>	Trace Data 13
TRC_DATA14	C1	X_GPMCO_DIR	O	3.3V <sup>1</sup>	Trace Data 14
TRC_DATA15	D12	X_GPMCO_CSn0	O	3.3V <sup>1</sup>	Trace Data 15
TRC_DATA16	D13	X_GPMCO_CSn1	O	3.3V <sup>1</sup>	Trace Data 16
TRC_DATA17	D14	X_GPMCO_CSn2	O	3.3V <sup>1</sup>	Trace Data 17
TRC_DATA18	C14	X_GPMCO_CSn3	O	3.3V <sup>1</sup>	Trace Data 18
TRC_DATA19	D11	X_GPMCO_AD15/BOOTMODE_15 <sup>2</sup> (100K pulldown on SOM)	O	3.3V <sup>1</sup>	Trace Data 19
TRC_DATA20	D10	X_GPMCO_AD14/BOOTMODE_14 <sup>2</sup> (100K pulldown on SOM)	O	3.3V <sup>1</sup>	Trace Data 20
TRC_DATA21	D8	X_GPMCO_AD13/BOOTMODE_13 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Trace Data 21
TRC_DATA22	D7	X_GPMCO_AD12/BOOTMODE_12 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Trace Data 22
TRC_DATA23	D6	X_GPMCO_AD11/BOOTMODE_11 <sup>2</sup> (100K pulldown on SOM)	O	3.3V <sup>1</sup>	Trace Data 23

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

<sup>2</sup>: This signal should not be driven during reset. More information can be found in section [6.3 System Boot Configuration](#).

## 11.3 UART0

The phyCORE-AM62xx SOM can also be communicated with using UART0 for downloading program code into the internal RAM or for debugging programs currently executing. UART0 is the default console and as such PHYTEC recommends bringing out UART0 for console access. The UART0 interface is accessible via the phyCORE-Connector.

### 11.3.1 UART0 Pinout

**Table 49** **UART0 Connections at the phyCORE-Connector**

X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
D37	X_UART0_RX	I	3.3V <sup>1</sup>	UART0 Receive Data
D38	X_UART0_TX	O	3.3V <sup>1</sup>	UART0 Transmit Data
D36	X_UART0_CTS	I	3.3V <sup>1</sup>	UART0 Clear to Send
D35	X_UART0_RTS	O	3.3V <sup>1</sup>	UART0 Request to Send

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

### 11.3.2 UART0 Reference Circuits

An example reference circuit for connecting the UART0 signals to a Micro USB connector is shown below.

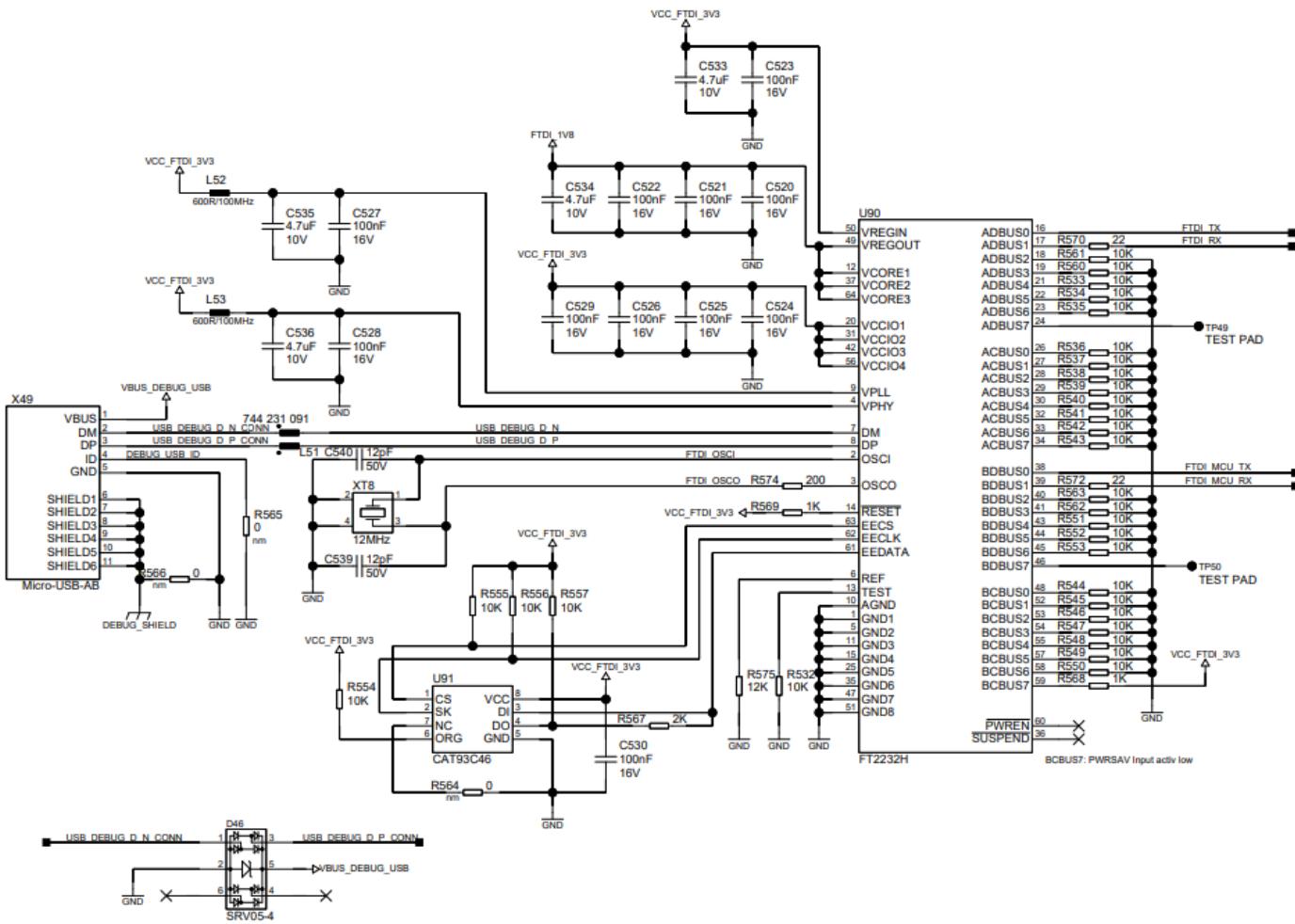


Figure 41. UART0 to USB Bridge Reference Schematic

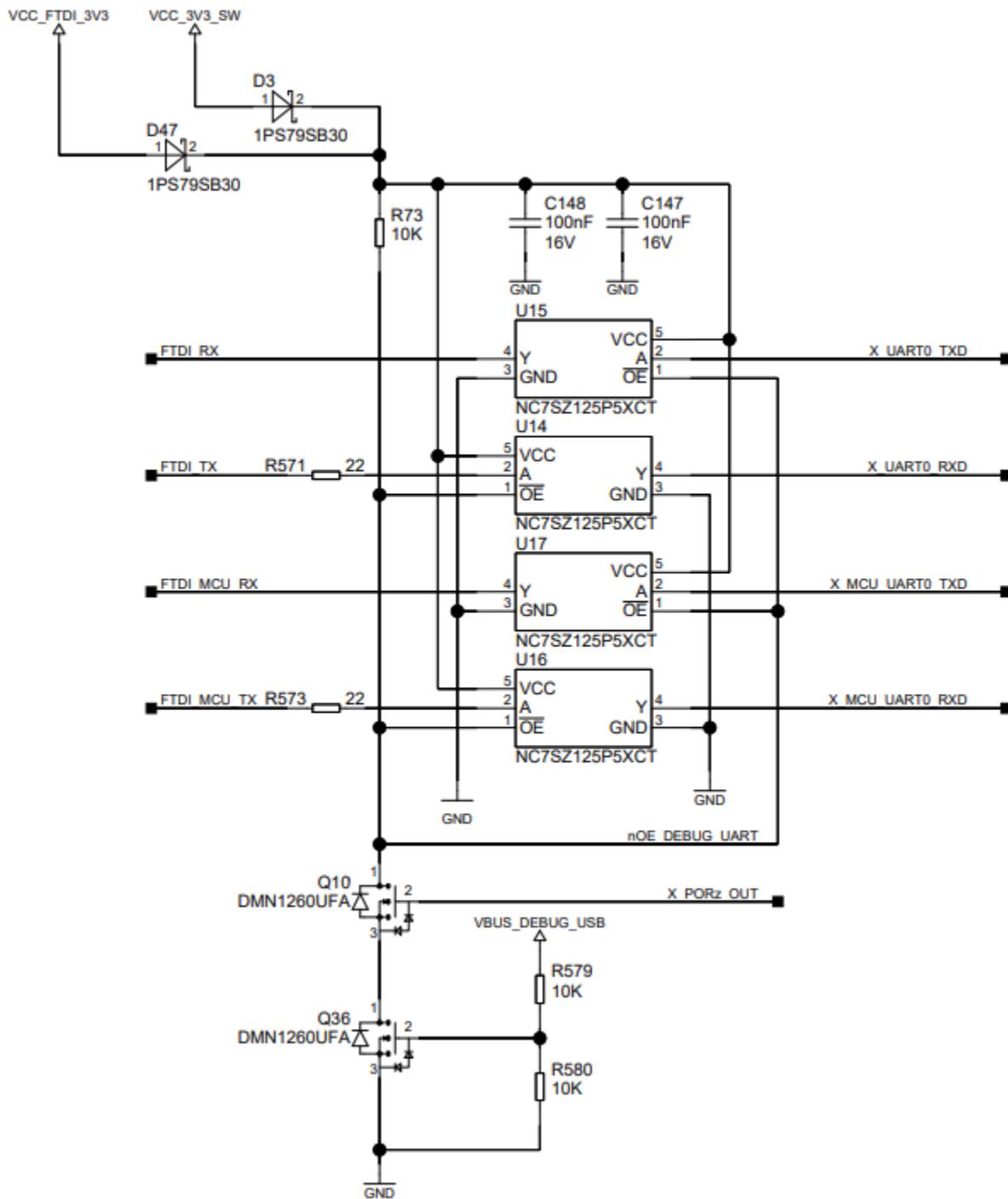


Figure 42. UART0 to USB Buffers and Regulator Reference Schematic

The circuit consists of:

- Four buffers to isolate the UART signals from the bridge/header until SOM power is brought up and PGOOD has gone high (this is important as driving these signals high too early will prevent the SOM from powering on)
- A dual UART to USB bridge to convert the UART signals into USB signals

- A TVS diode array for ESD protection
- A micro-USB connector
- A DC regulator to convert the 5V USB power to 3.3V

A simpler design that just brings out the bare minimum UART signals for use with FTDI USB adapter cables is shown below. Note that the buffers are still required to prevent power back feeding into the SOM, preventing it from properly turning on.

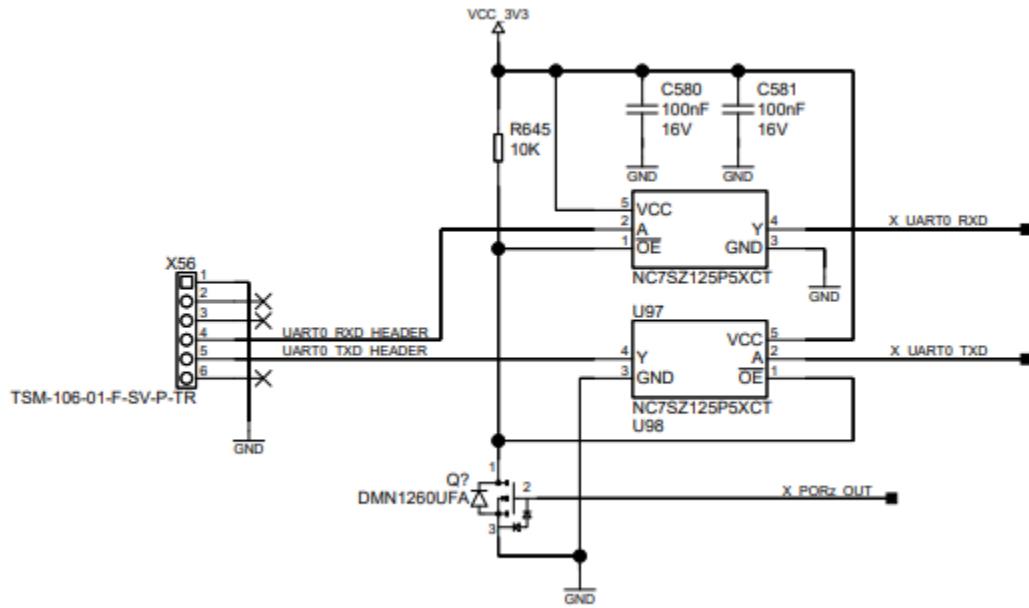


Figure 43. Simple UART0 Reference Schematic

# 12 System Interfaces

The following sub-sections detail the system signals brought out to the phyCORE connectors from the MAIN, MCU, and WKUP domains of the AM62xx processor that are not discussed elsewhere in the manual. It also covers the on-board RTC and the two heartbeat LEDs.

## 12.1 MAIN Pinout

**Table 50** MAIN Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
CLKOUT0	C60	X_EXT_REFCLK1	O	3.3V <sup>1</sup>	Clock Output
EXTINTn	C39	X_RTC_INT (10K pullup on SOM)	I	3.3V <sup>1</sup>	External Interrupt
EXT_REFCLK1	C60	X_EXT_REFCLK1	I	3.3V <sup>1</sup>	External clock input to Main Domain
GPMCO_FCLK_MUX	C3	X_GPMCO_CLK	O	3.3V <sup>1</sup>	GPMC functional clock output
	C35	X_I2C0_SCL (2.2K pullup on SOM)			
OBSCLK0	D5	X_GPMCO_AD10/BOOTMODE_10 <sup>2</sup> (100K pullup on SOM)	O	3.3V <sup>1</sup>	Observation clock output for test and debug
PORz_OUT	C57	X_PORz_OUT (1.5K pulldown on SOM)	O	3.3V <sup>1</sup>	Main Domain POR status output
RESETSTATz	D58	X_RESETSTATz (10K pulldown on SOM)	O	3.3V <sup>1</sup>	Main Domain warm reset status output
RESET_REQz	C58	X_RESET_REQz (100K pullup on SOM)	I	3.3V <sup>1</sup>	Main Domain external warm reset request input
SYSCLKOUT0	C60	X_EXT_REFCLK1	O	3.3V <sup>1</sup>	SYSCLK0 output from Main PLL controller for test and debug
AUDIO_EXT_REFCLK0	D36	X_UART0_CTSN			
	A20	X_CPSW_RGMII2_RD3	I/O	3.3V <sup>1</sup>	External clock input/output for MCASP
	D33	X_MCASPO_AXR0			
AUDIO_EXT_REFCLK1	D35	X_UART0_RTSN			
	D30	X_MCASPO_AFSX	I/O	3.3V <sup>1</sup>	External clock input/output for MCASP
	D15	X_GPMCO_WPn			

1: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

2: This signal should not be driven during reset. More information can be found in section [6.3 System Boot Configuration](#).

## 12.2 MCU Pinout

**Table 51** MCU Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
MCU_OBSCLK0	D49	X_MCU_SPI0_CS1	O	3.3V <sup>1</sup>	Observation clock output for test and debug
MCU_RESETSTATz	C55	X_MCU_RESETSTATz (10K pulldown on SOM)	O	3.3V <sup>1</sup>	MCU Domain warm reset status output
MCU_RESETz	C56	X_MCU_RESETz (100K pullup on SOM)	I	3.3V <sup>1</sup>	MCU Domain warm reset
MCU_ERRORn	D59	X_MCU_SAFETY_ERRORn	I/O	1.8V	Error signal output from MCU Domain ESM
MCU_EXT_REFCLK0	D49	X_MCU_SPI0_CS1	I	3.3V <sup>1</sup>	External input to MCU Domain
	A59	X_MCU_MCAN1_TX			
MCU_SYSCLKOUT0	D49	X_MCU_SPI0_CS1	O	3.3V <sup>1</sup>	MCU Domain system clock output for test and debug

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

## 12.3 WKUP Pinout

Table 52 WKUP Connections at the phyCORE-Connector

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
WKUP_CLKOUT0	D60	X_WKUP_CLKOUT0	O	3.3V <sup>1</sup>	WKUP Domain CLKOUT0 output

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

## 12.4 RTC Pinout

The on-board RTC provides accurate time keeping ( $\pm 1$  ppm @ 25°C) at extremely low power consumption (40 nA @ 3 V). The RTC can keep track of the year, month, date, weekday, hour, minute, and seconds and has timer, alarm, and external event input functionality.

Table 53 RTC Connections at the phyCORE-Connector

X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
D44	X_RTC_EVI <sup>2</sup> (10K pullup on SOM)	I	3.3V <sup>1</sup>	RTC Event Input
C39	X_RTC_INT (10K pullup on SOM)	I	3.3V <sup>1</sup>	RTC Interrupt

<sup>1</sup>: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section [4.6 Solder Jumpers](#) for details.

<sup>2</sup>: The signal brought out at this pin is controlled by a jumper. Refer to section [4.6 Solder Jumpers](#) for details.

## 12.5 Heartbeat LEDs

The phyCORE-AM62xx has two LEDs, one green (connected to the Linux domain) and one red (connected to the MCU domain), named the heartbeat LEDs. In PHYTEC's software, the green LED is configured to flash in a heartbeat pattern once the SOM starts booting into Linux. This provides a visual indicator that the board is booting during debug. However, the user can configure the LEDs to behave in a manner most suitable to their design needs. The red LED is connected to X\_MCU\_GPIO0\_0 (processor ball E8) and the green LED is connected to GPIO0\_13 (processor ball H21).

# 13 Integrating and Updating the phyCORE-AM62xx

## 13.1 Integration

The various reference circuits contained in sections 5-12 as well as the information in section [4.5 Minimum Requirements for Operation](#) can be used as a starting point for integrating the phyCORE-AM62xx SOM into target circuitry. Additional information/tools are available to facilitate the integration of the phyCORE-AM62xx SOM into customer applications, such as:

phyCORE-AM62xx SOM and Carrier Board Schematic References:

- Schematics are made available upon request [here](#).

phyCORE-AM62xx Pin Resources:

- PHYTEC recommends the use of [TI's System Configuration Tool](#)
- Access to PHYTEC's pinmuxing tool is made available upon request [here](#).
- A configuration file for importing into TI's System Configuration Tool is available [here](#).

phyCORE-AM62xx Symbol/Cell Resources:

- Symbols/cells of the SOM connector are available [here](#).

Phone, e-mail, FAQ, wiki, and other online support by visiting <http://PHYTEC.com/contact/>

## 13.2 Modification

Removal of various components, such as the SoC and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the SOM inoperable.

**CAUTION:**

If any modifications to the module are performed, regardless of their nature, the manufacturer warranty is voided.

## 13.3 In-Field Updates

It is important that your system is designed so that firmware can be updated remotely in case there are issues "in the field." PHYTEC recommends choosing at least one or more of the following design features:

- Include an Ethernet jack in your design that can be used to access the system. See section [7.2.2 Ethernet Design In Guide](#) for more details on integrating Ethernet into your design.

- Add a Wi-Fi module to your design connected to MMC2. See section [6.2.2.2 MMC Design In Considerations](#) for more details.
- Add an SD card slot from which new software can be flashed to the device. This is especially useful when internet is inaccessible, intermittent, or if Ethernet connection is not possible.

## 13.4 Product Change Management

Use of PHYTEC products ensures interchangeable SoC core circuitry in the event of obsolescence of parts used on our SOMs and SBCs. End users no longer need to redesign entire CPU circuitry and engage in version control to accommodate new or obsolete parts. Instead, PHYTEC manages this at the SOM-level. PHYTEC ensures continued availability of pin- and function-compatible SOMs and SBCs, further minimizing maintenance costs and risks. This pro-active product lifecycle management (PLM) policy has enabled deployment of the same PHYTEC SOM in designs for over twenty years. See <https://www.phytec.com/support/product-lifecycle-management/> for more details on our Product Longevity, Product Obsolescence and Product Maintenance policies.

# 14 Additional Information

Members of PHYTEC's phyCORE® product family can be populated with different processors and offer various functions and configurations. PHYTEC supports a variety of ARM-based and other SoCs in two ways.

1. As the basis for PHYTEC development kits and Single Board Computers, which serves as a reference and evaluation platform.
2. As insert-ready, fully functional phyCORE® OEM System on Modules (SOMs) and phyBOARD Single Board Computers (SBCs), which can be incorporated directly into the user's hardware design.

For more information go to: <https://PHYTEC.com/design-services/>

Declaration of Electromagnetic Conformity of the  
PHYTEC phyCORE-AM62xx System On Module



PHYTEC System on Modules (SOM) and Single Board Computers (SBC) are designed as subcomponents for integration in electrical devices.

Combined with PHYTEC Carrier Boards, PHYTEC SOMs can be used as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

## CAUTION:

PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians, electronic manufacturing personnel and engineers) handle and/or operate these products.

PHYTEC products fulfill the rules and regulations of the European Union's Directive for Electromagnetic Conformity and the Federal Communications Commission Title 47 CFR Part 15 Subpart B only in accordance with the descriptions and rules of usage indicated in this hardware manual, particularly in respect to the external SOM connector, power interfaces and interfaces to host systems for programming.

## NOTE:

Integration of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electromagnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

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# 15 Revision History

**Table 54 Document Revision History**

Date	Version Number	Changes in this Manual
2022/09/22	L-1038.A0	Preliminary Release
2023/03/22	L-1038.A1	Updated current draw information to match latest testing, fixed various typos, changed references of X_PGOOD from output to open drain output, updated EEPROM to 4KB (as it is 32 Kbits, not 32KBs), added some information to the RTC section, and added some reference circuits of the SOM.