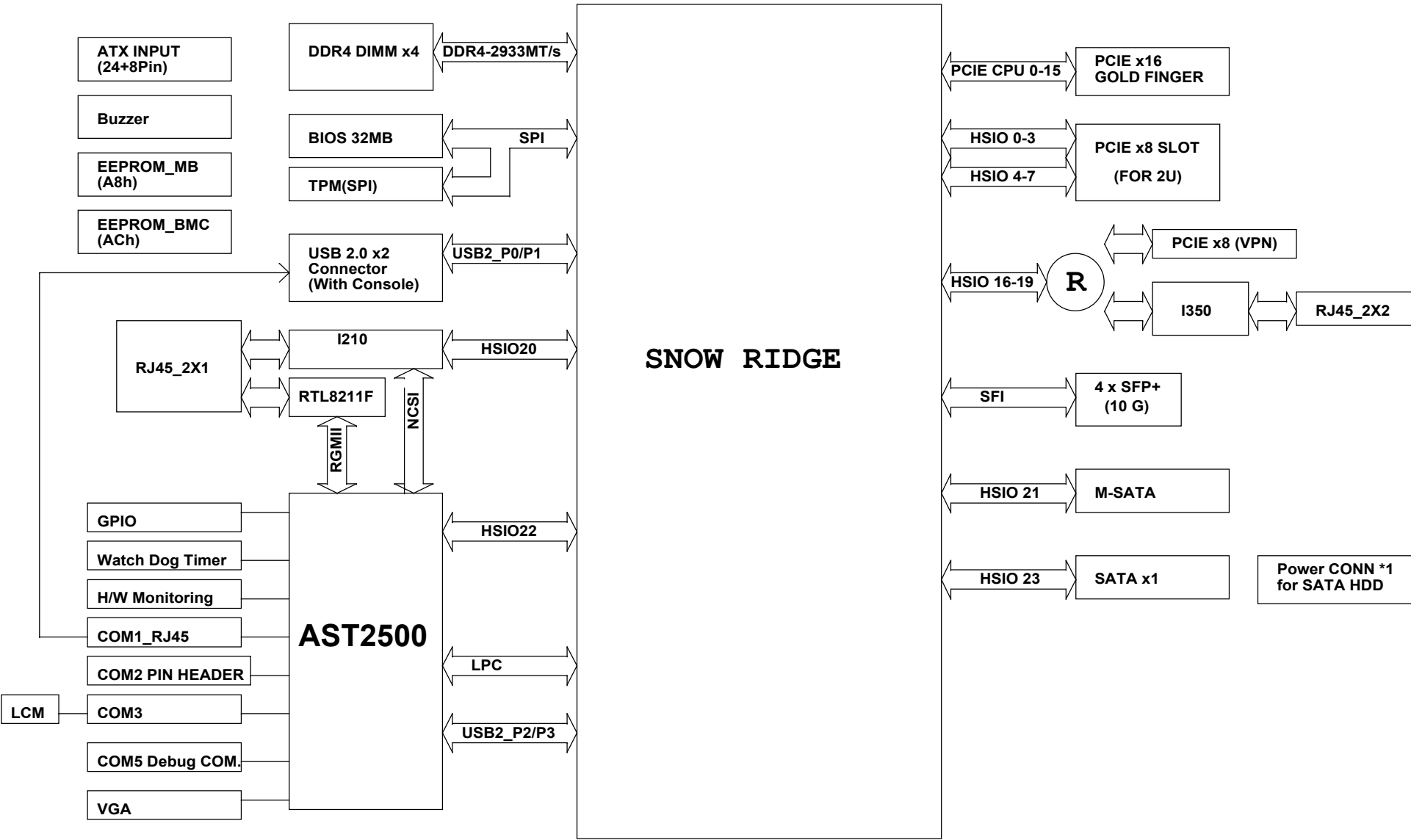


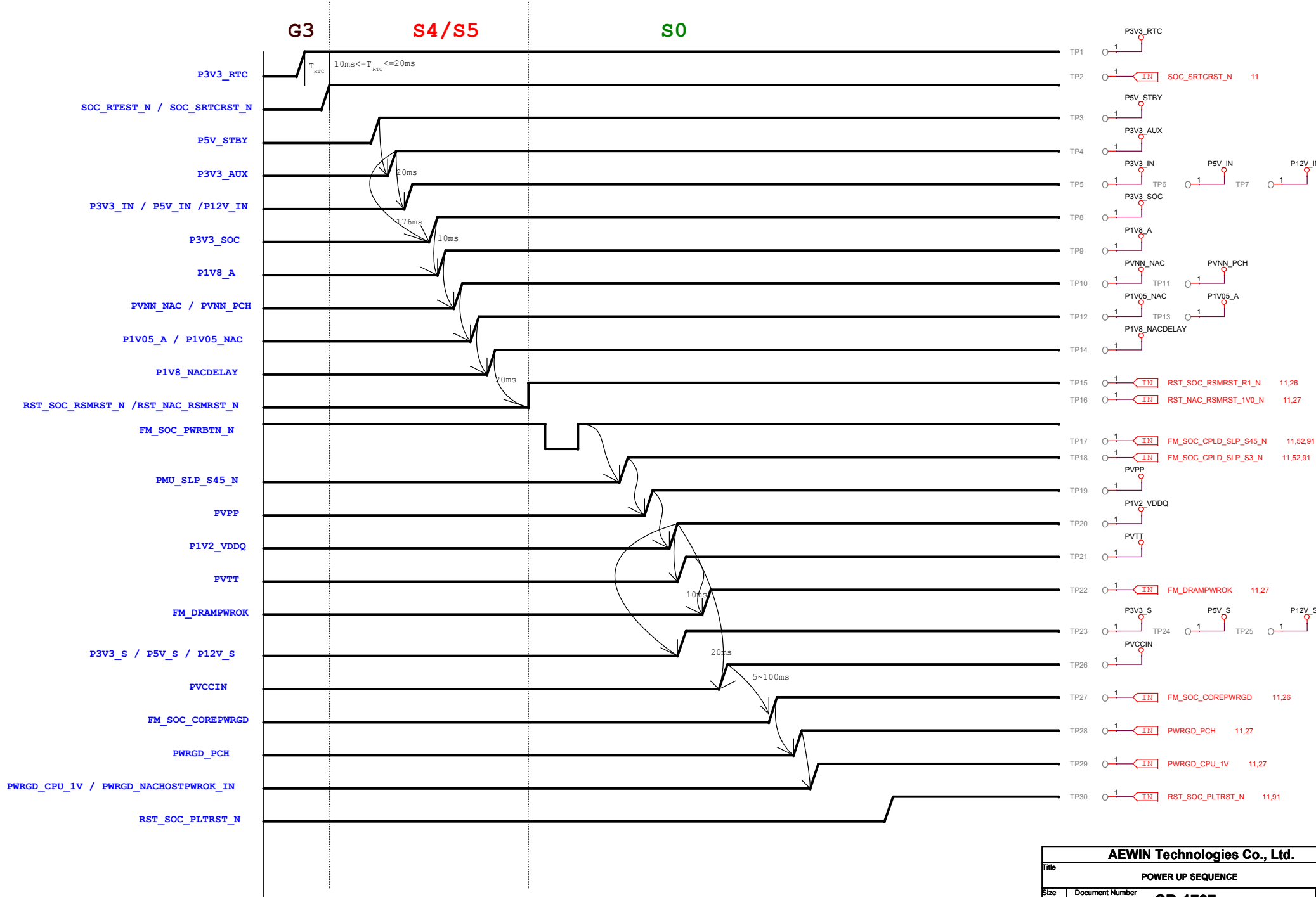
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BLOCK DIAGRAM



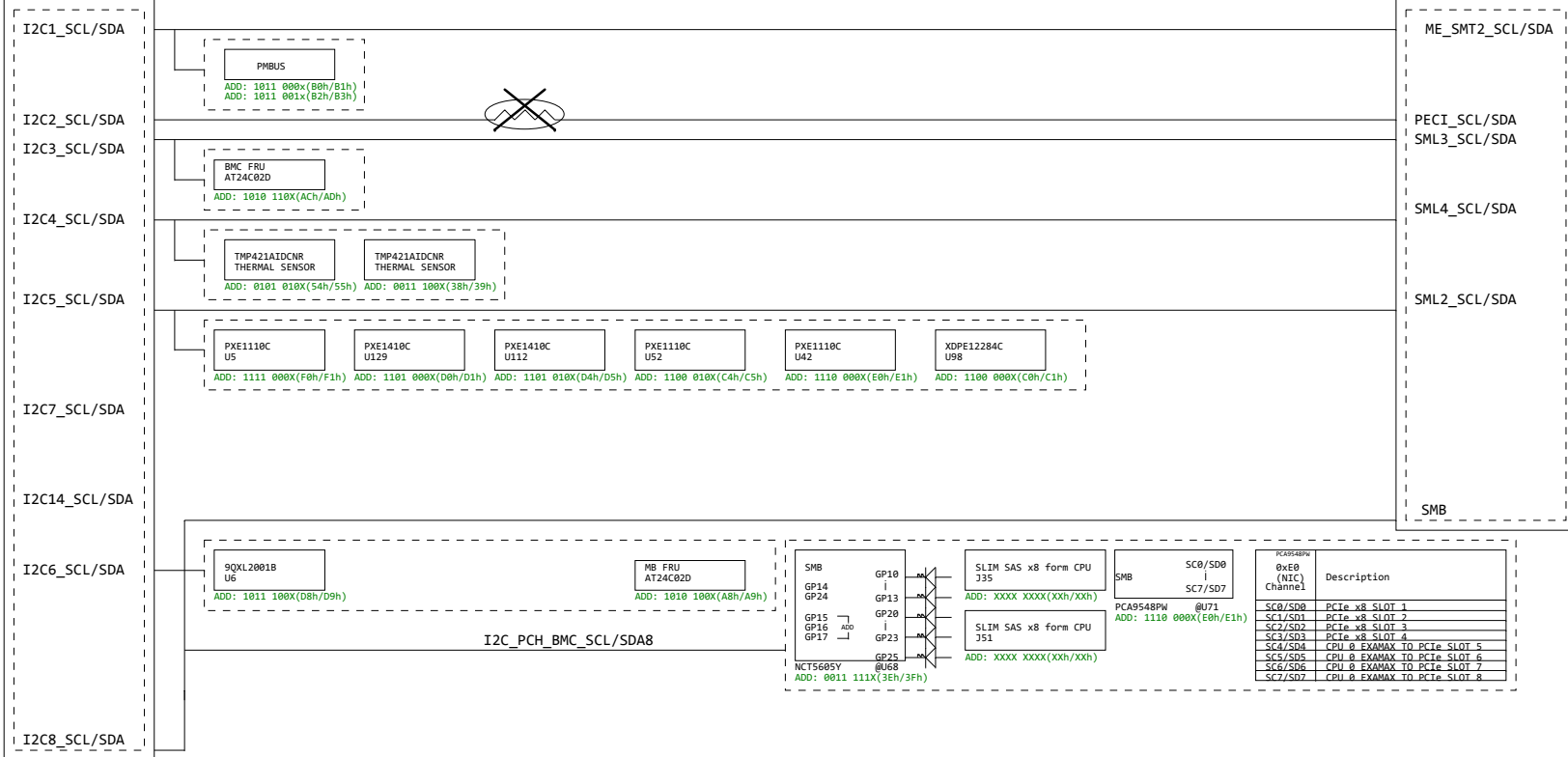
POWER UP TIMING (Non-Deep Sx Platform]



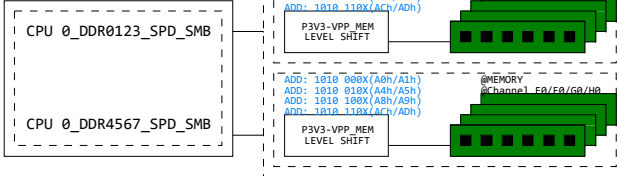
POWER NET	VOLTAGE (V)	POWER WELL	SOURCE	TYPE	Imax (A)	ACTIVE STATE	CONTROL	USAGE
P3V3_RTC	2.8-3.3	RTC	BATT/P3V3_AUX	BATT/DIODE		G3-S0		SOC, BMC
P5V_STBY	4.75-5.25	STANDBY	ATX PSU	ATX PSU	2	S5-S0	ATX PSU	P3V3_AUX
P3V3_AUX	3.1-3.46	STANDBY	P5V_STBY/P5V_IN	TPS568215	8	S5-S0	P5V_STBY	CPLD,P3V3_SOC,P2V5_BMC,P3V3_BMC_SPI RTL8211F, I210, BMC, EMMC, PCIE SLOT
P12V_IN	11.4-12.6	STANDBY	ATX PSU	ATX PSU		S5-S0	CPLD (PWRGD_P3V3_STBY)	PVNN_NAC,P1V05_NAC,VFP,P1V2_VDDQ,PVCCIN P12V_S
P5V_IN	4.75-5.25	STANDBY	ATX PSU	ATX PSU		S5-S0	CPLD (PWRGD_P3V3_STBY)	P3V3_AUX,P1V8_A,P5V_S,GPIO PORT
P3V3_IN	3.1-3.46	STANDBY	ATX PSU	ATX PSU		S5-S0	CPLD (PWRGD_P3V3_STBY)	P1V5_A, P3V3_S, SFP
P3V3_SOC	3.1-3.46	STANDBY	P3V3_AUX	PDC3960X	1	S5-S0	CPLD (PWRGD_P3V3_STBY +5ms Delay)	P3V3_SPI,EMMC, SOC
P1V8_A	1.7-1.9	STANDBY	P5V_IN	TLV62095	3.5	S5-S0	CPLD (PWRGD_P3V3_SOC)	P1V8_NACDELAY,P1V2_BMC,P1V15_BMC,EMMC,SOC
PVNN_NAC	SVID	STANDBY	P12V_IN	PXM1310CPM	51	S5-S0	CPLD ((PWRGD_P1V8_A)	SOC
PVNN_PCH	SVID	STANDBY	P12V_IN	PXM1310CPM	7	S5-S0	CPLD ((PWRGD_P1V8_A)	SOC
P1V05_NAC	SVID	STANDBY	P12V_IN	PXM1310CPM		S5-S0		

AST2500

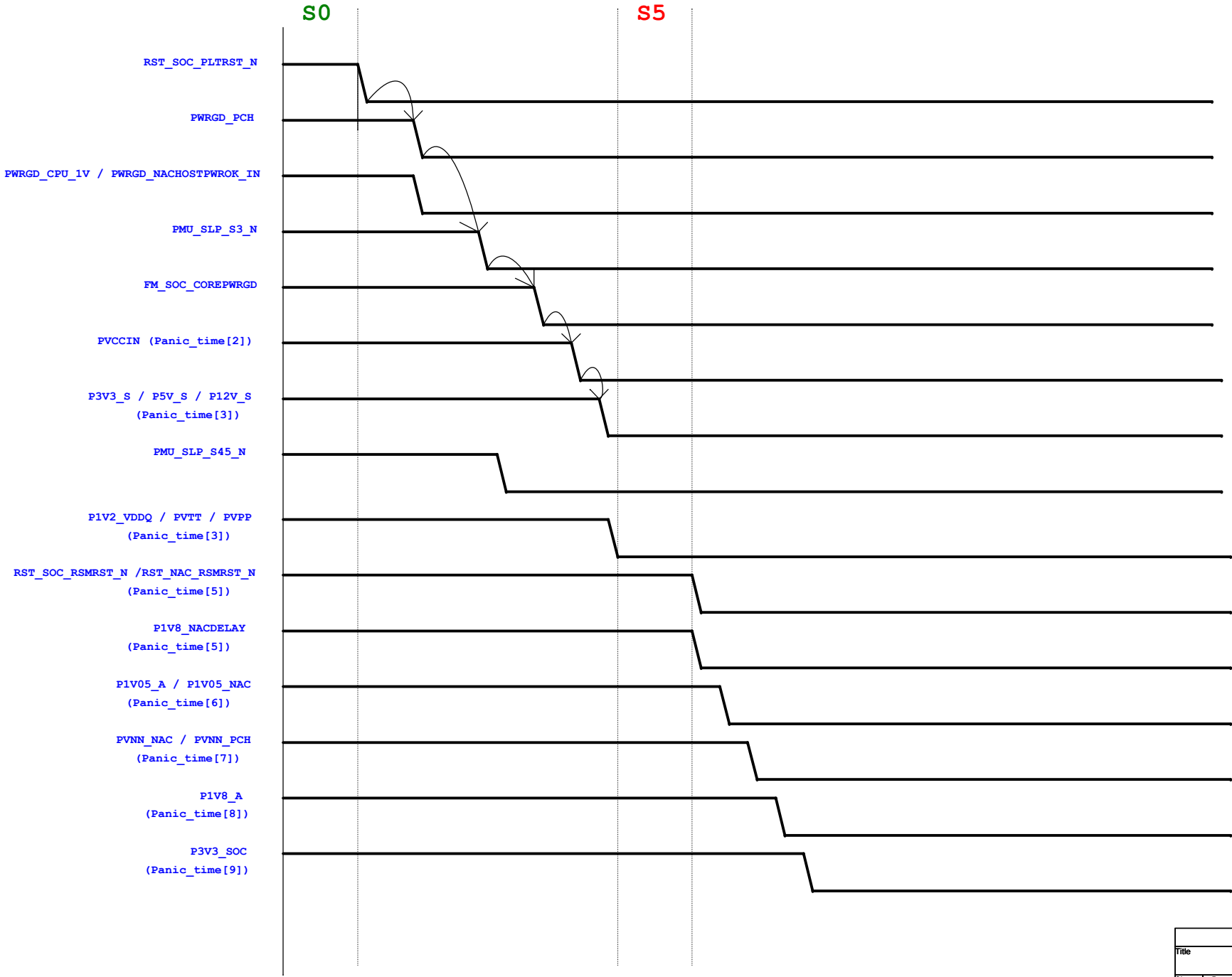
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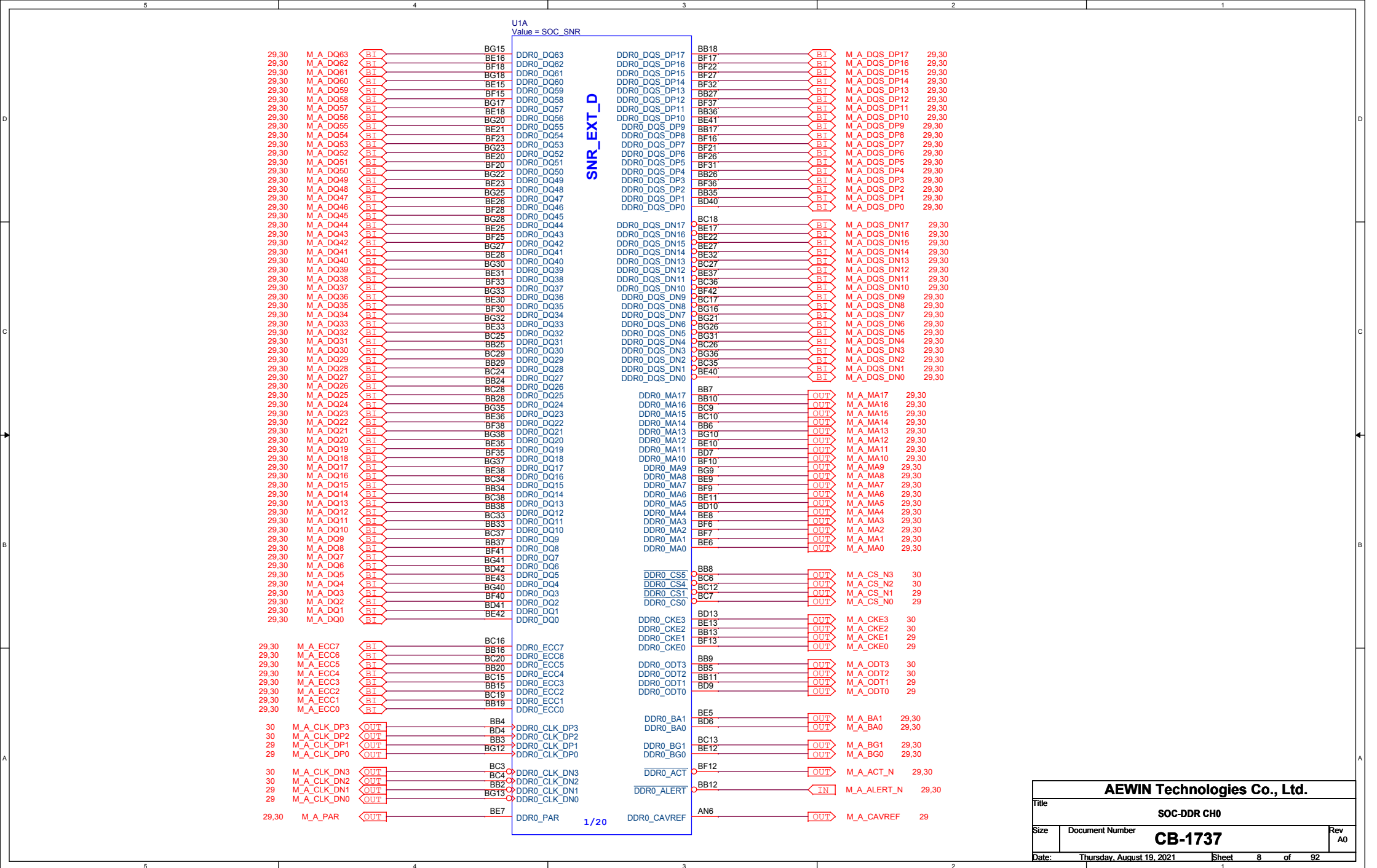
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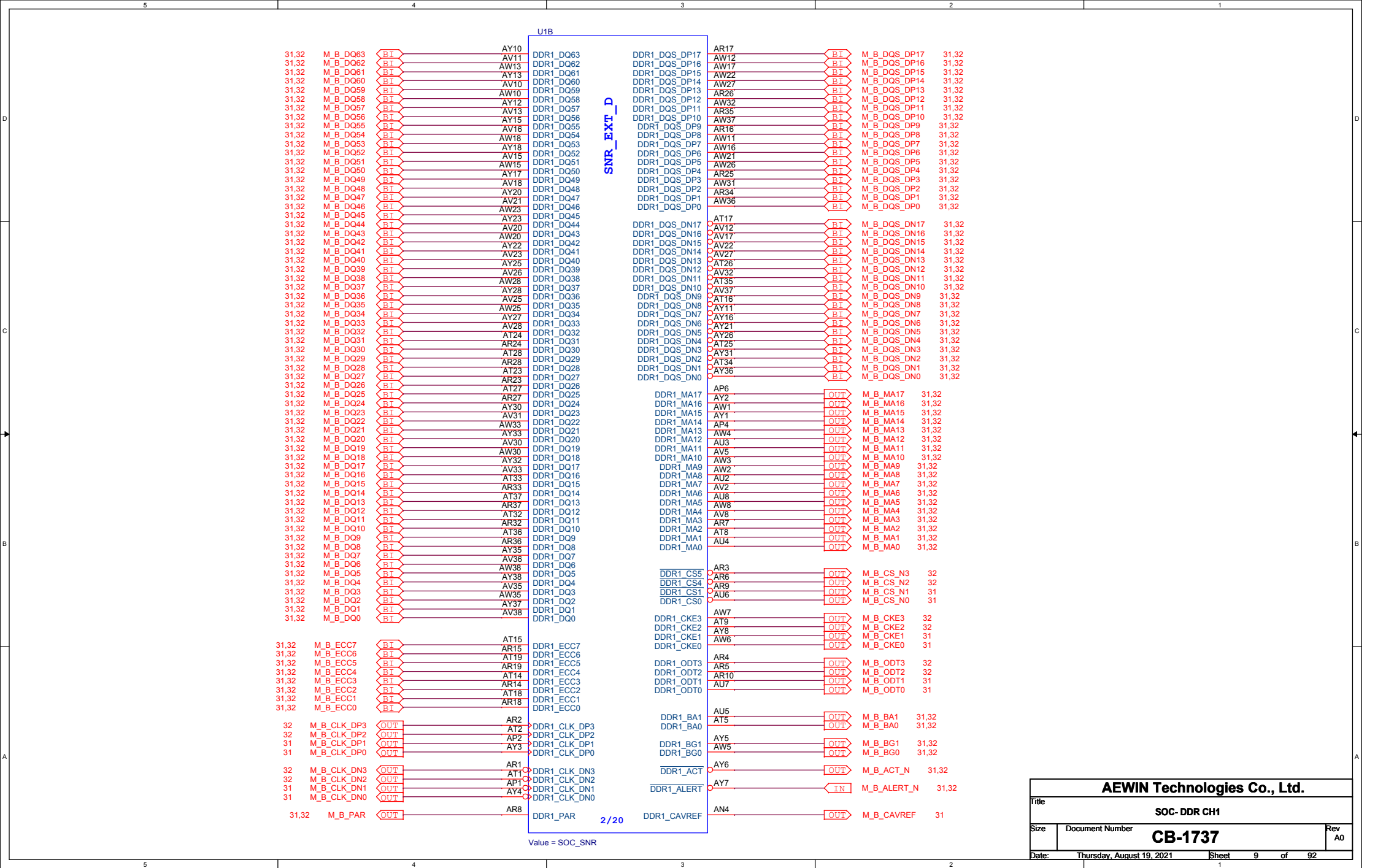


POWER DOWN SEQUENCE

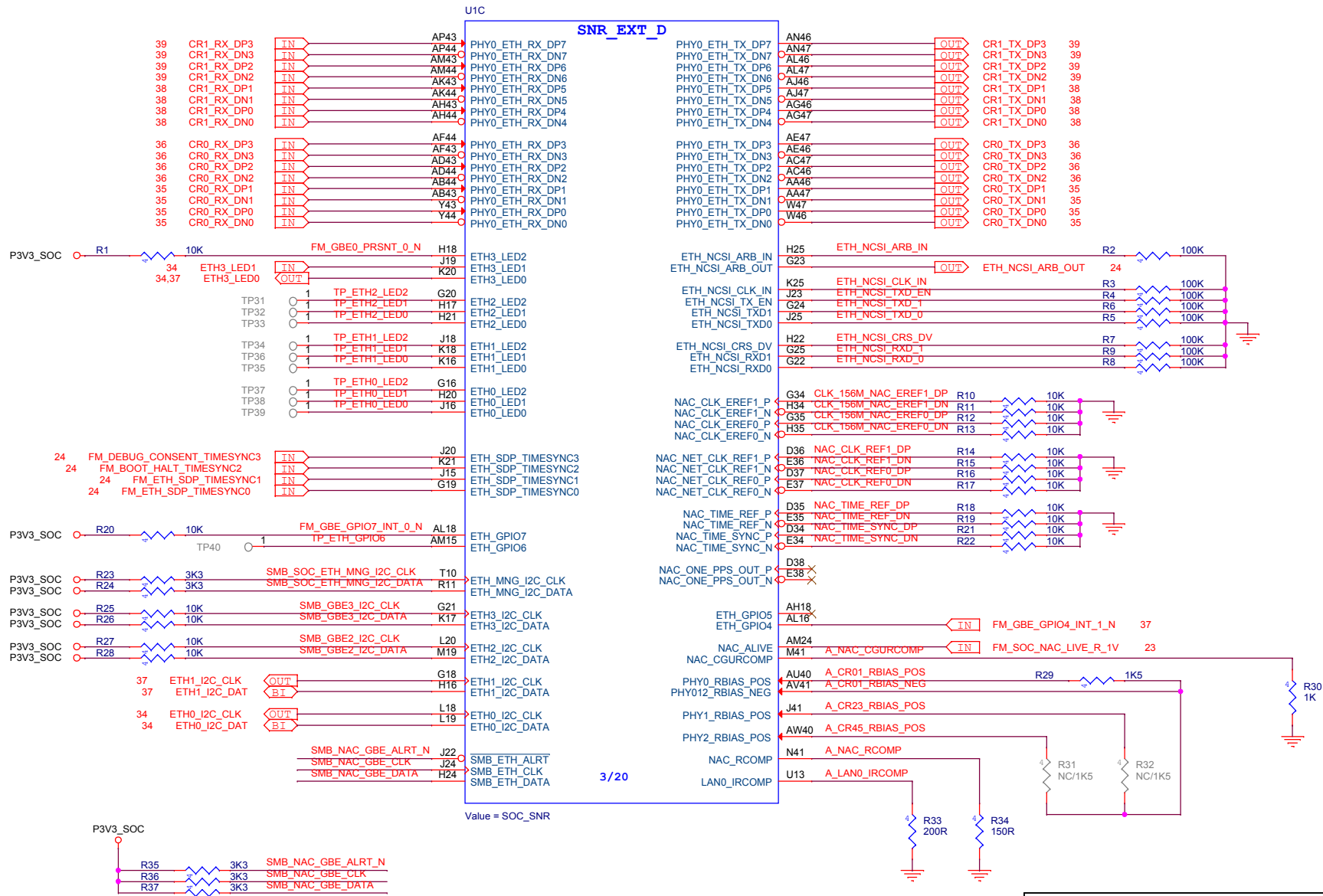


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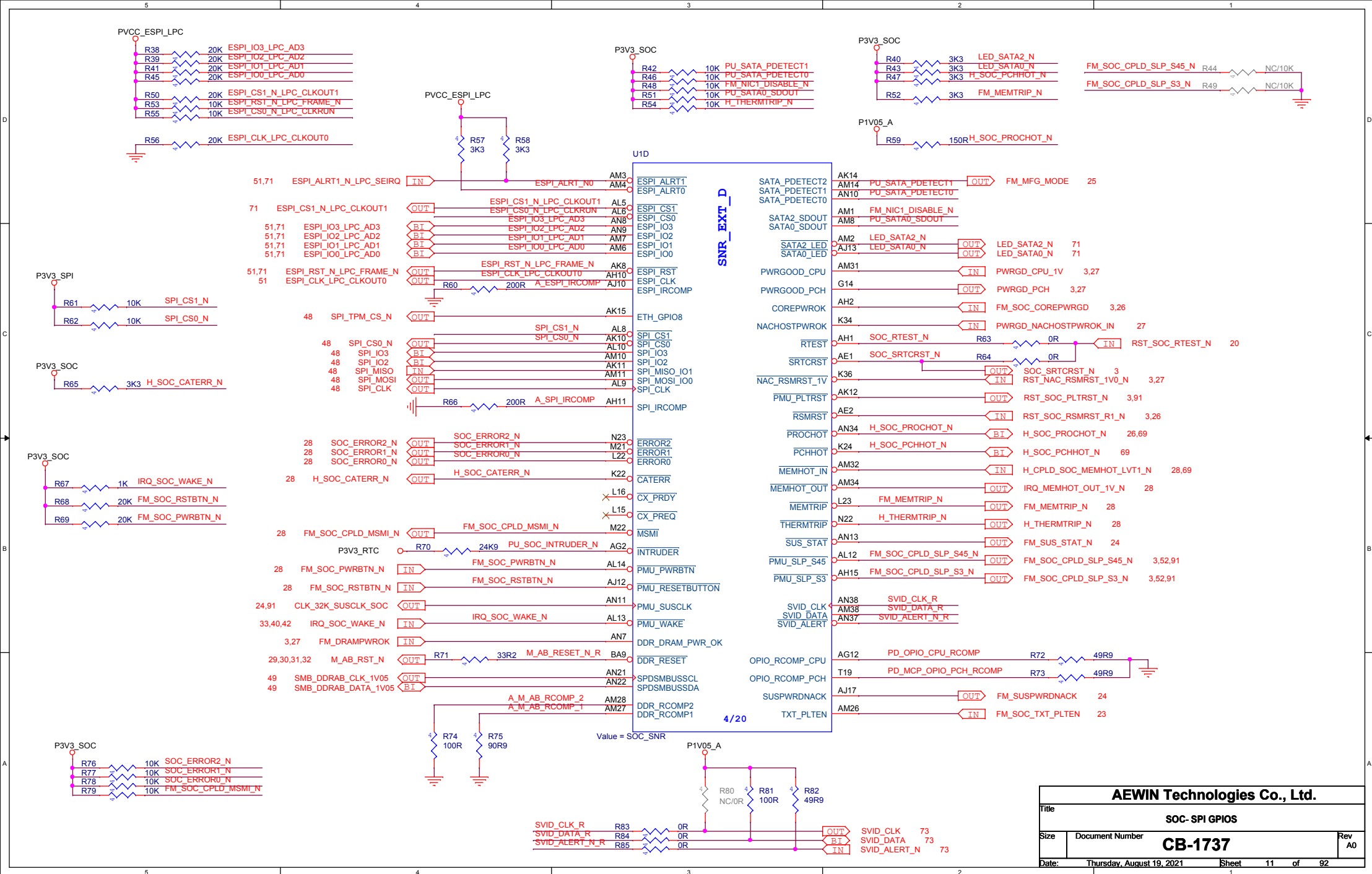


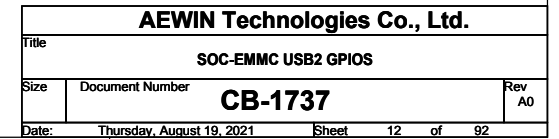
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Size	Document Number	Rev	
	CB-1737	A0	
Date:	Thursday, August 19, 2021	Sheet	9 of 92

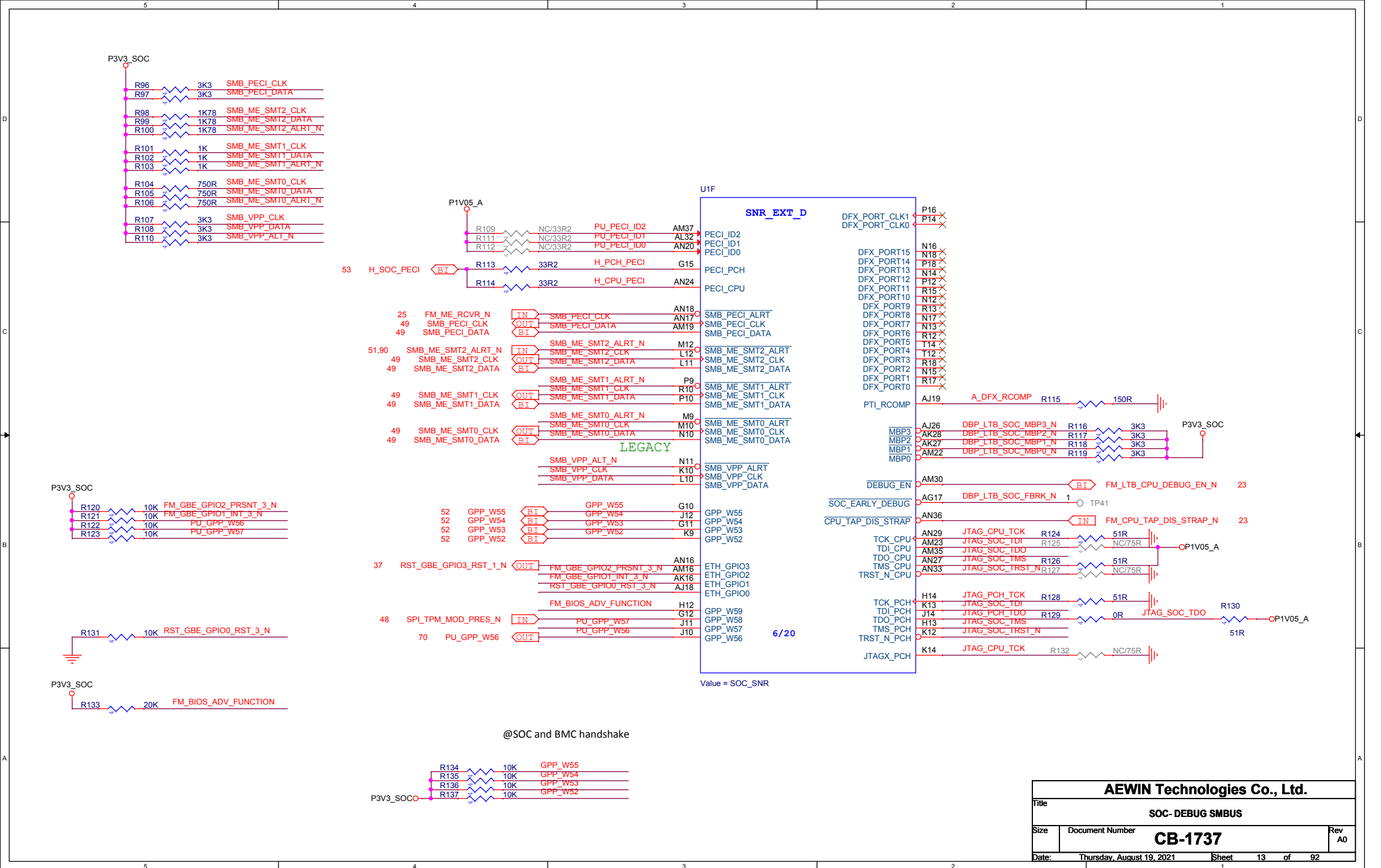


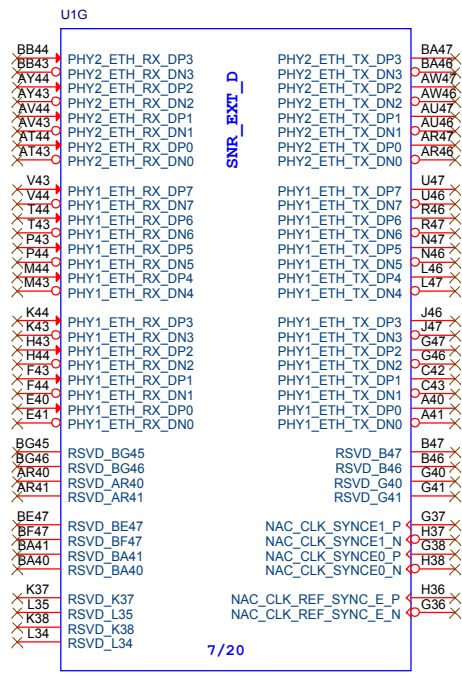
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Title			SOC- NAC GBE	
Size	Document Number	CB-1737		Rev A0
Date:	Thursday, August 19, 2021	Sheet	10	of 92

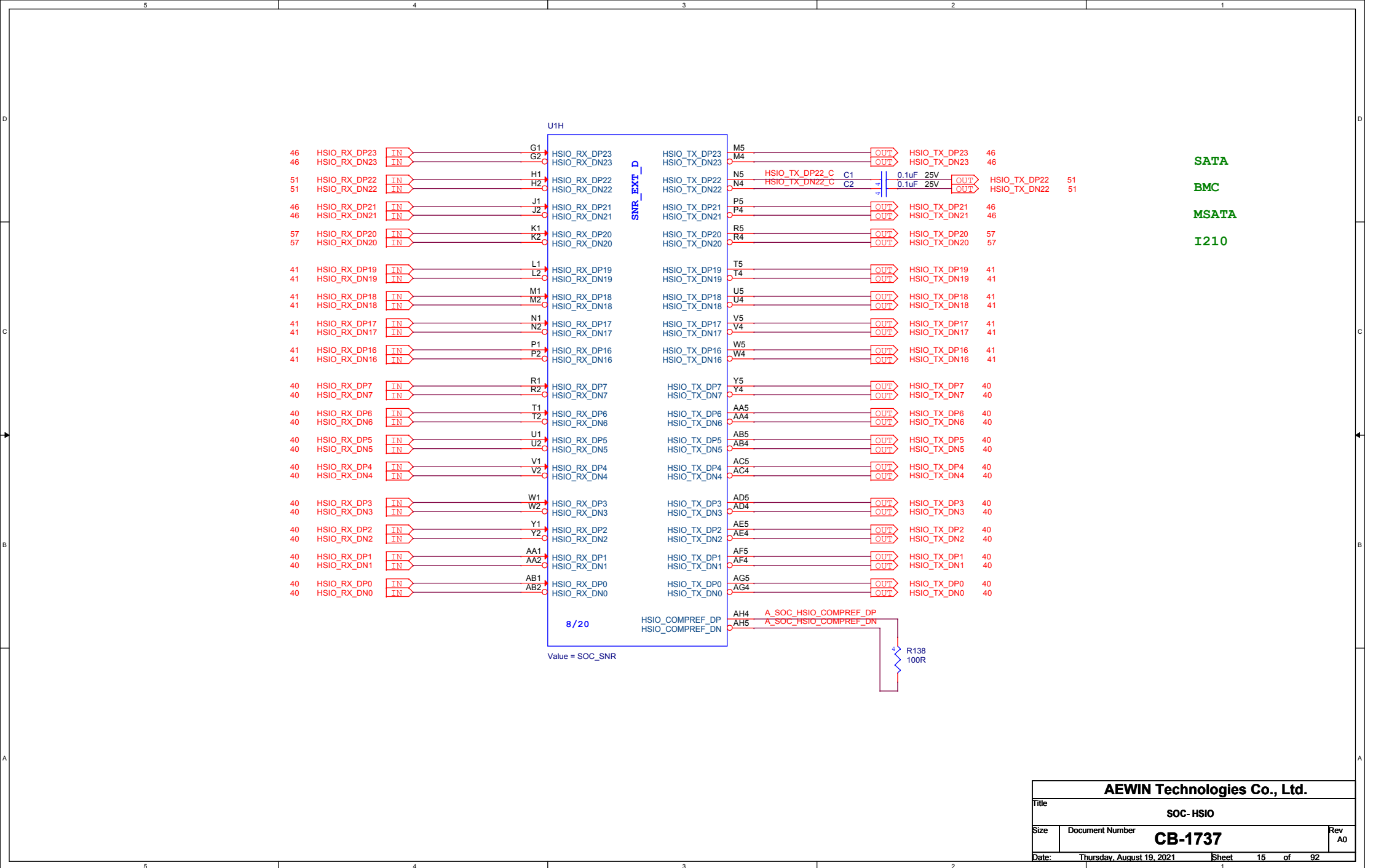


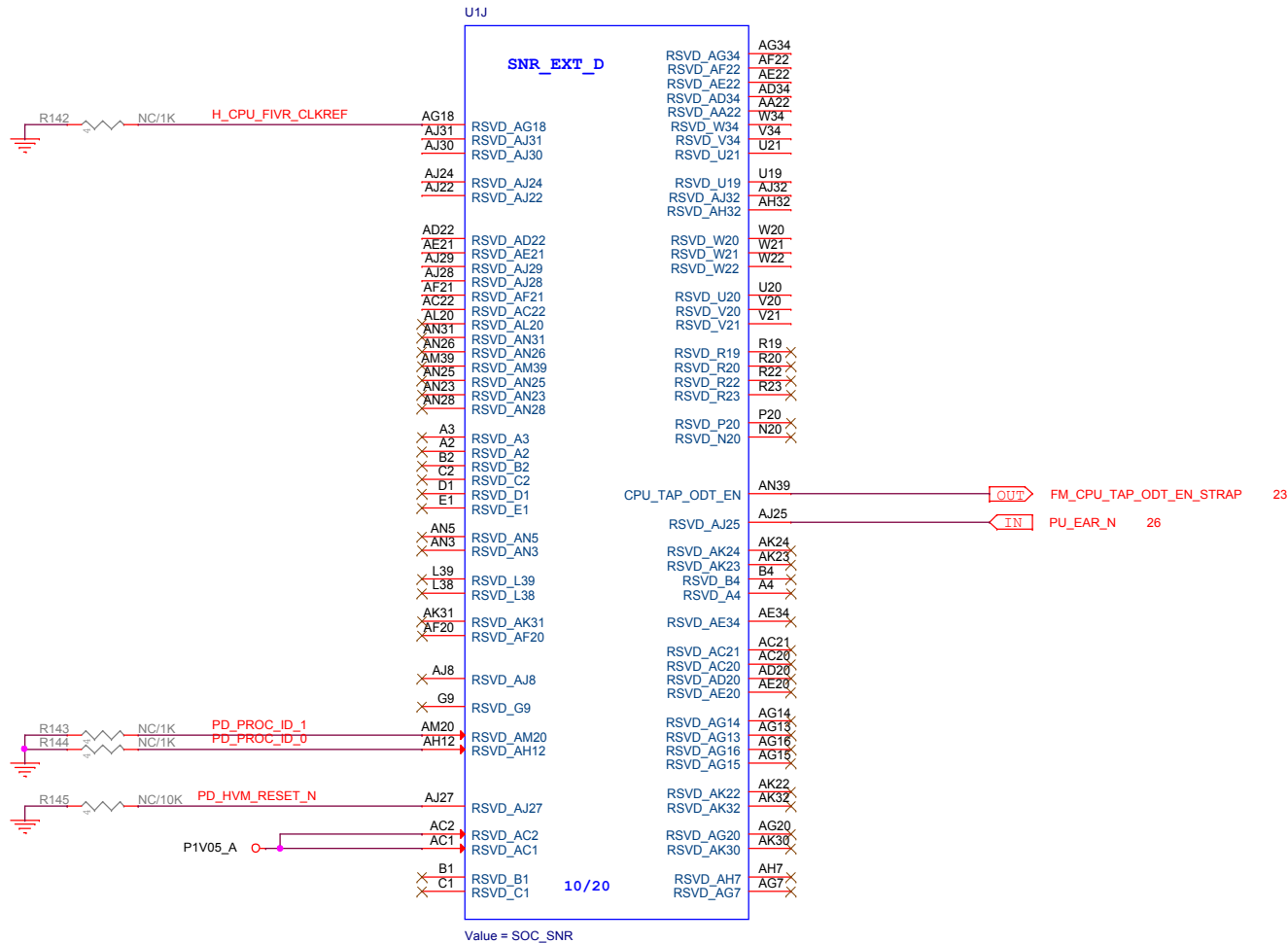




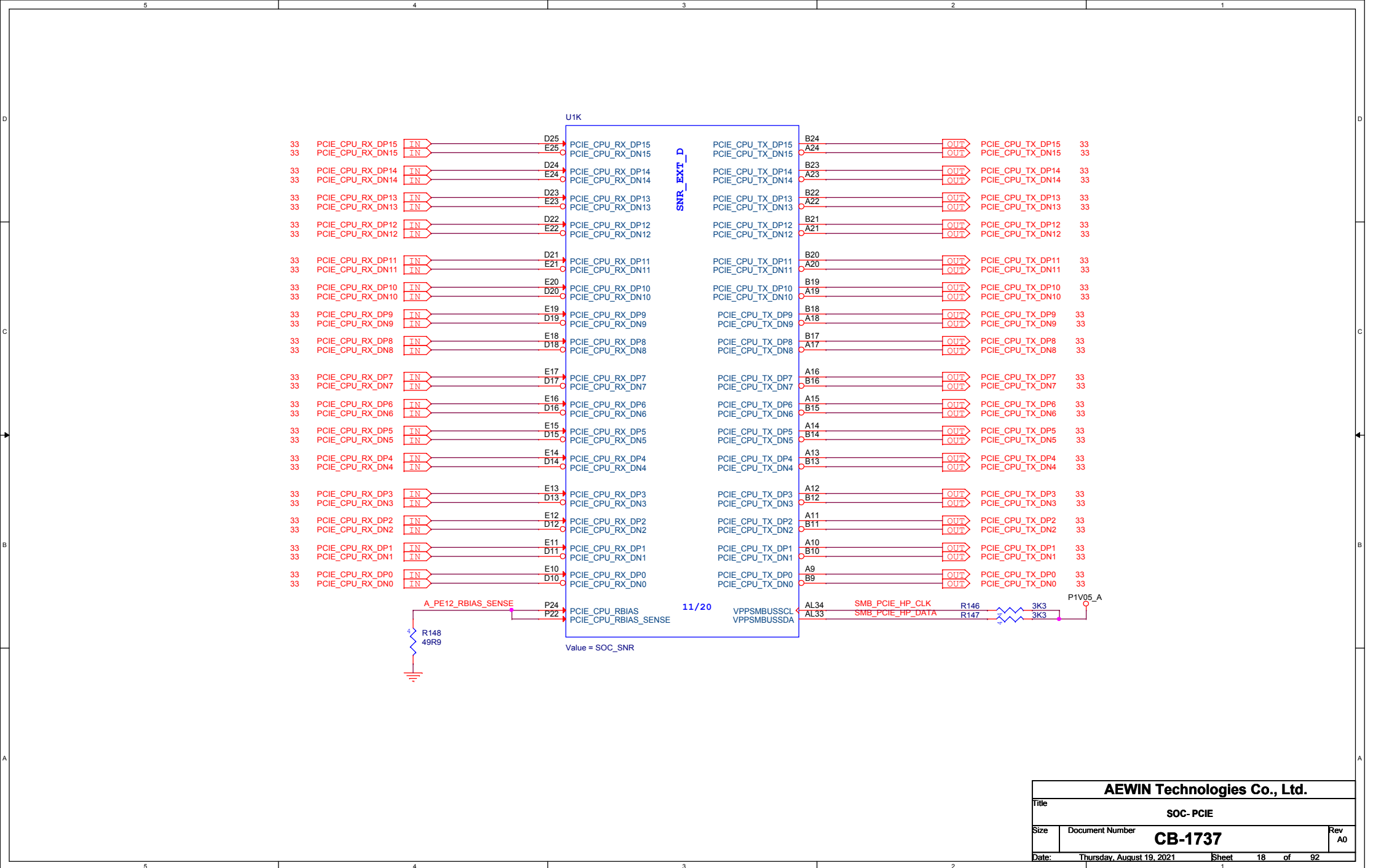


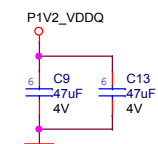
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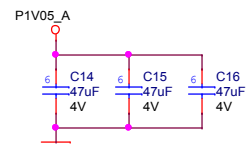


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Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021		Sheet 17 of 92

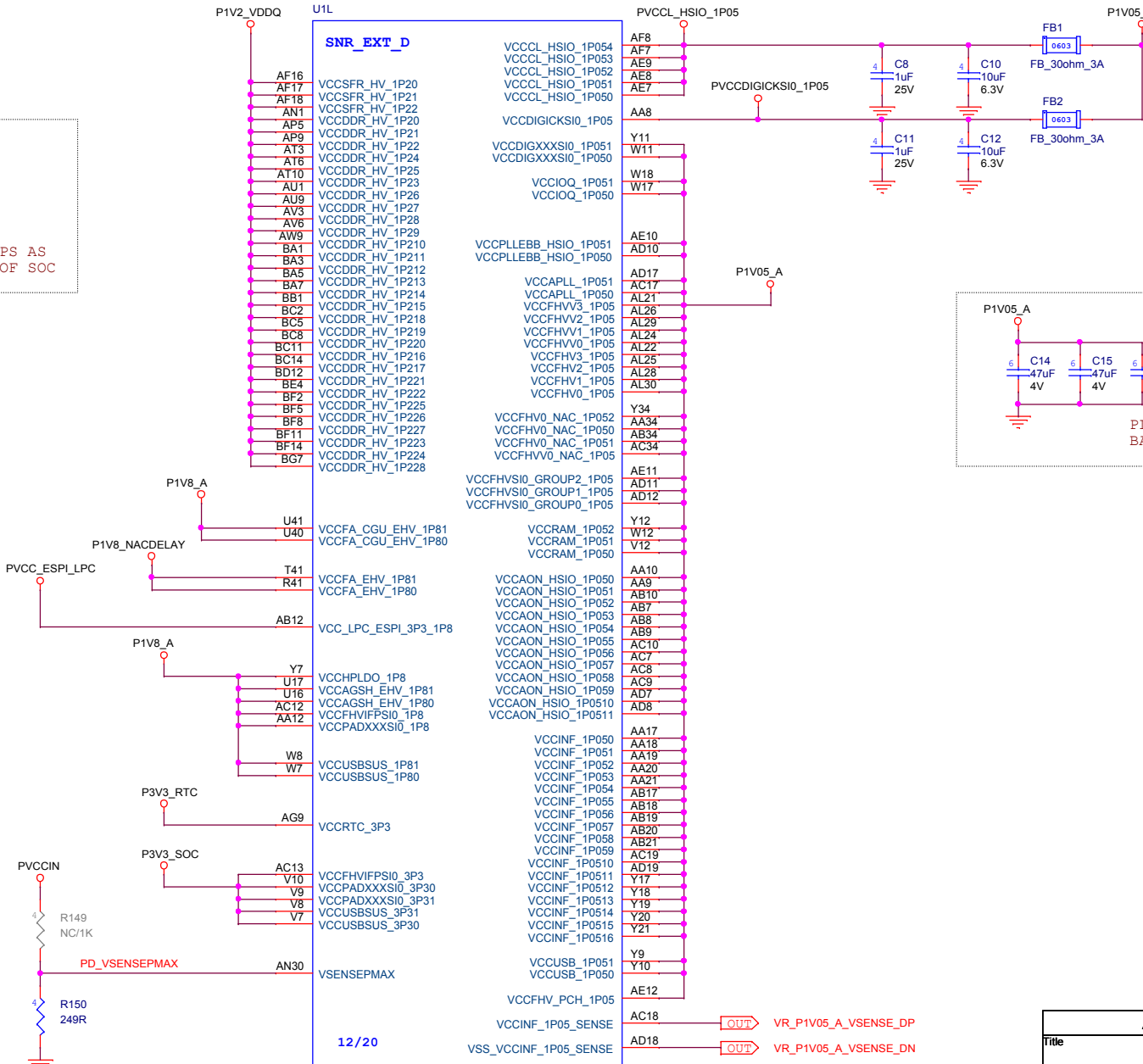




PLACE THESE CAPS AS
BACKSIDE CAPS OF SOC



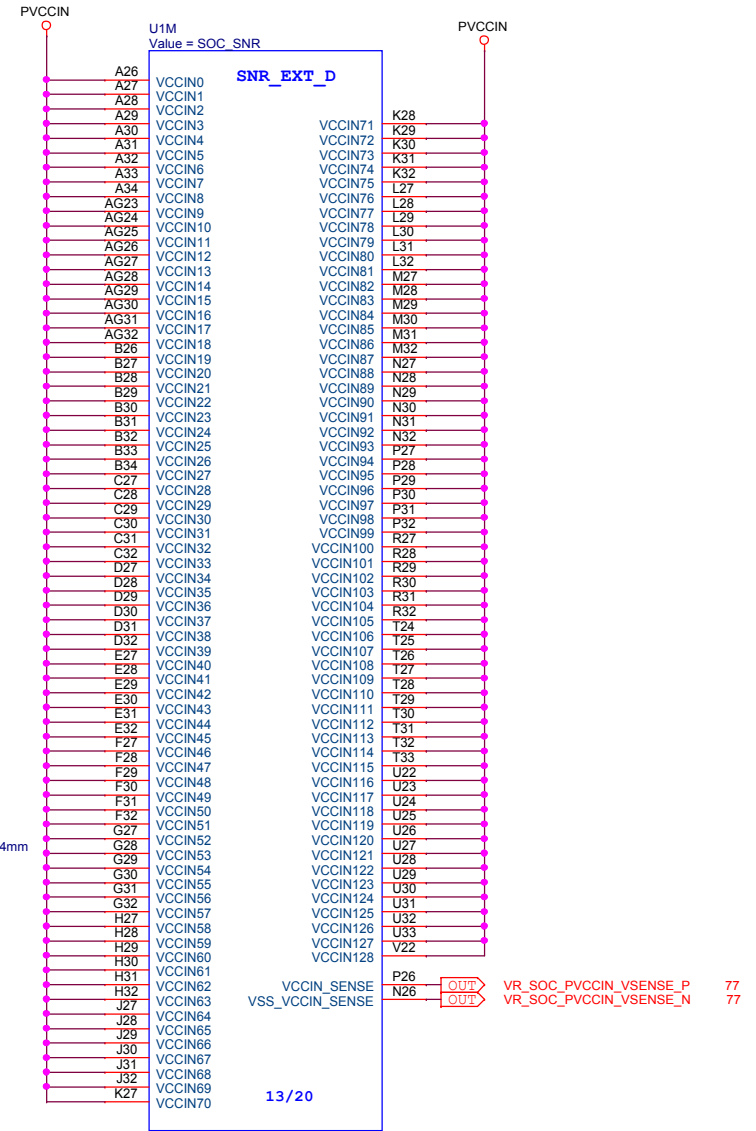
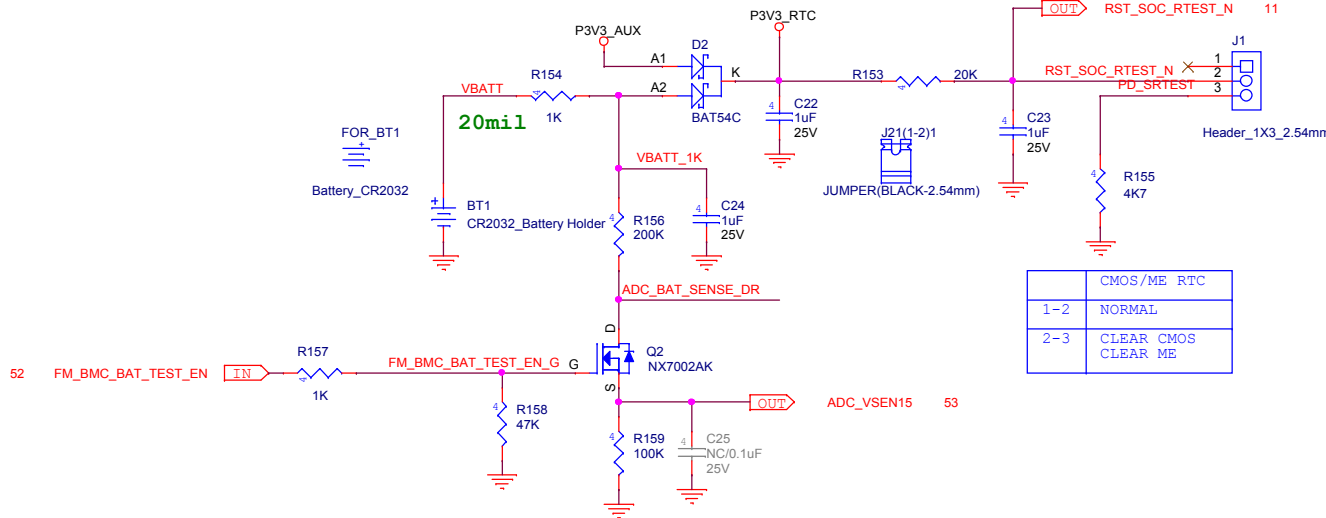
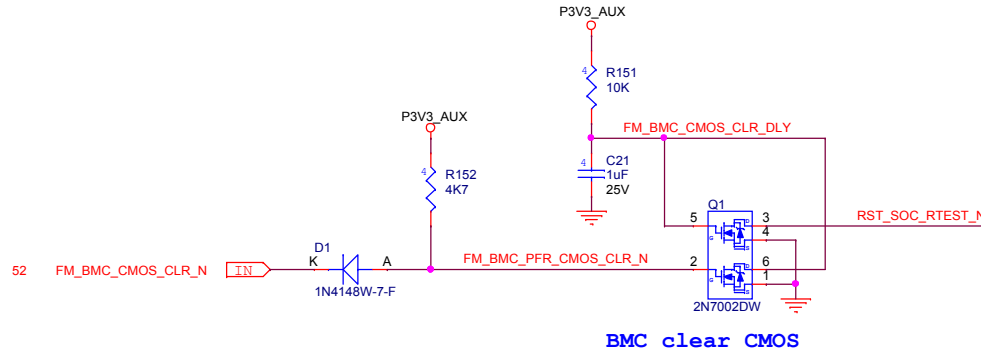
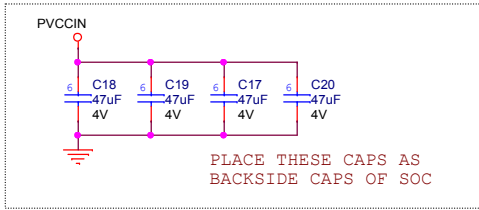
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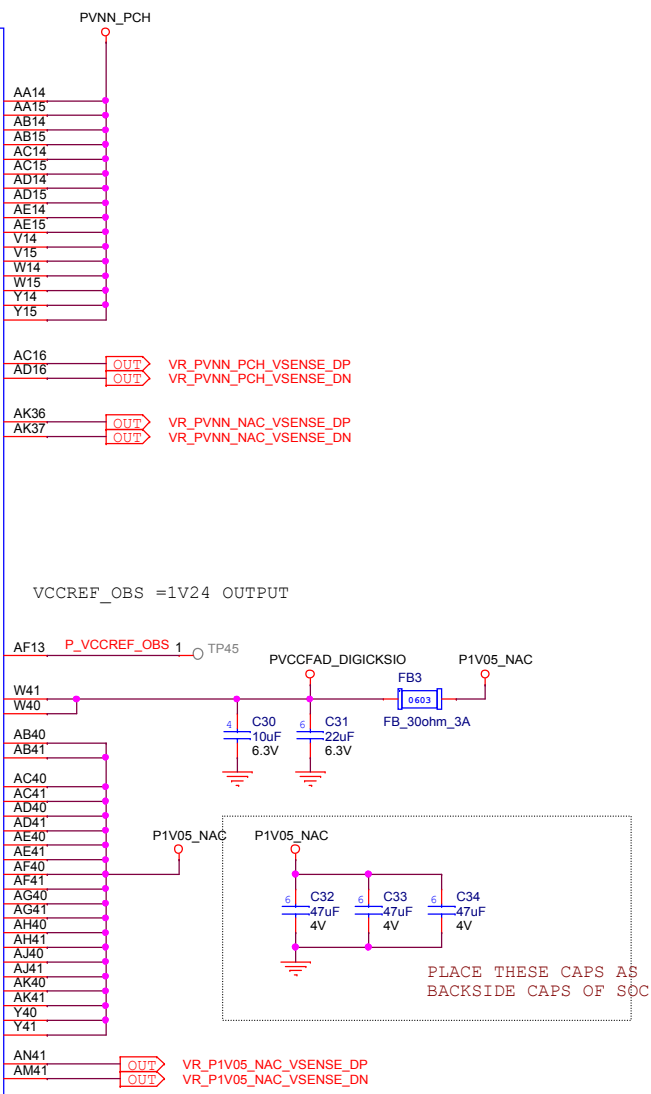


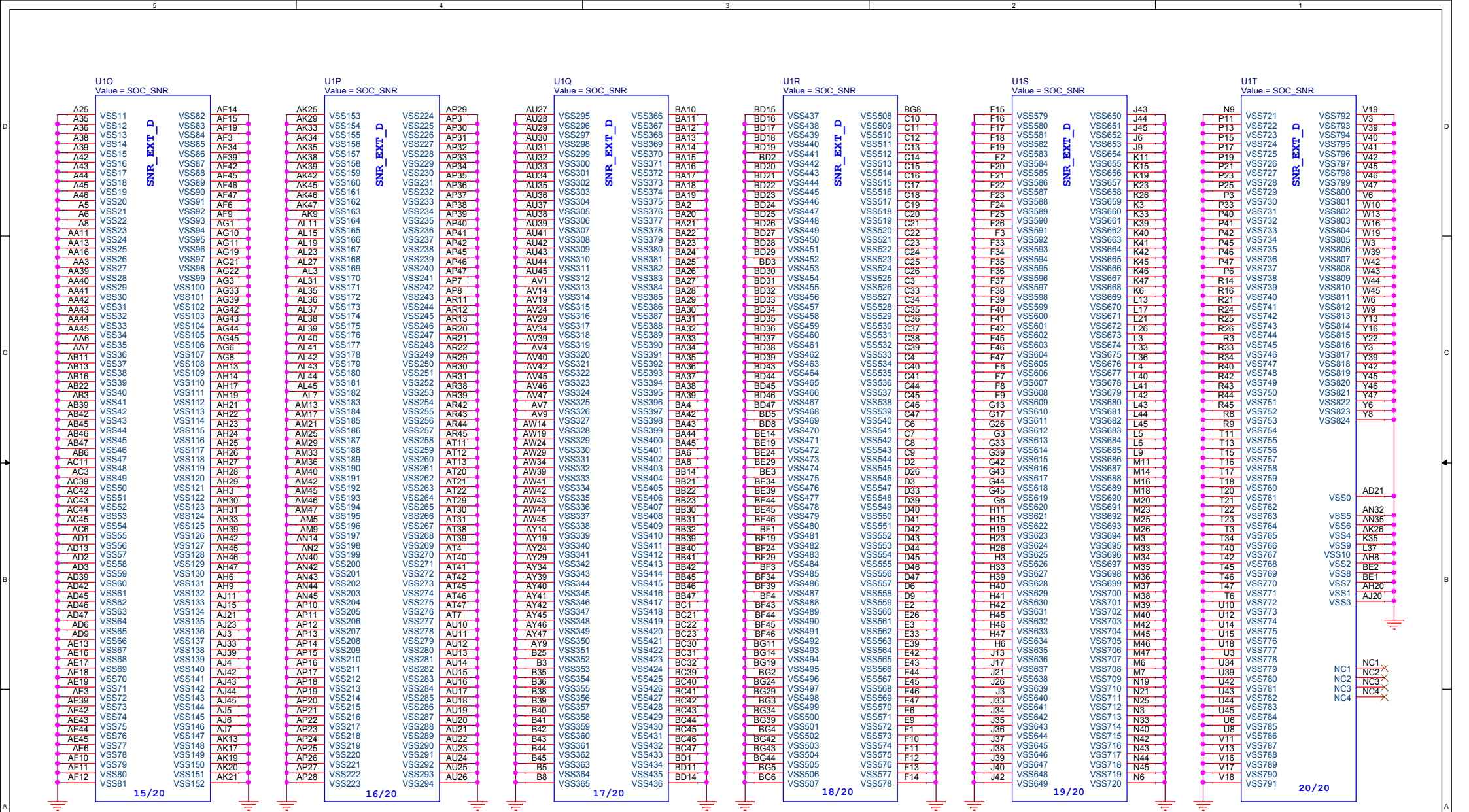
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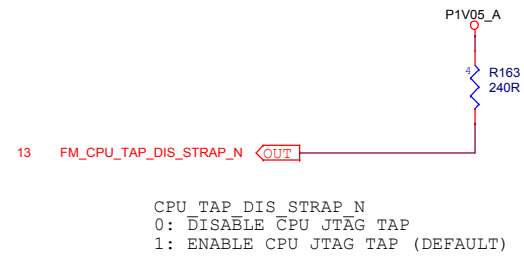
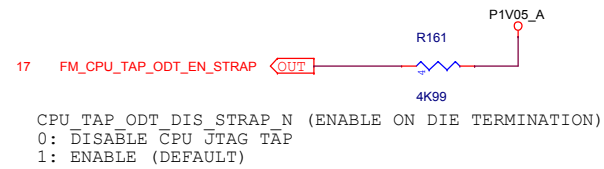
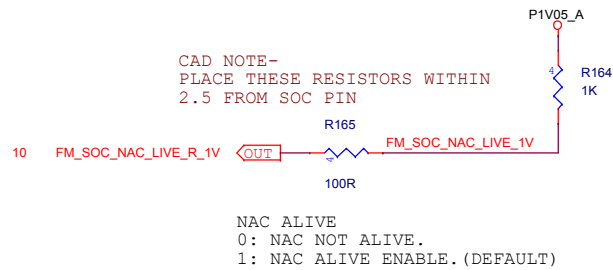
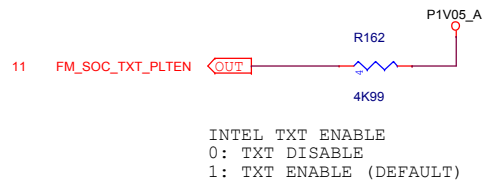
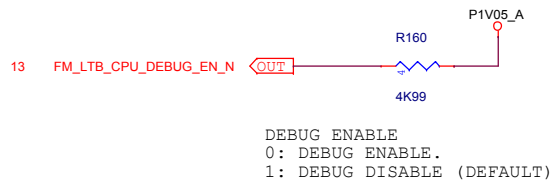
AEWIN Technologies Co., Ltd.

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Size	Document Number	Rev	
	CB-1737	A0	
Date:	Thursday, August 19, 2021	Sheet	19 of 92

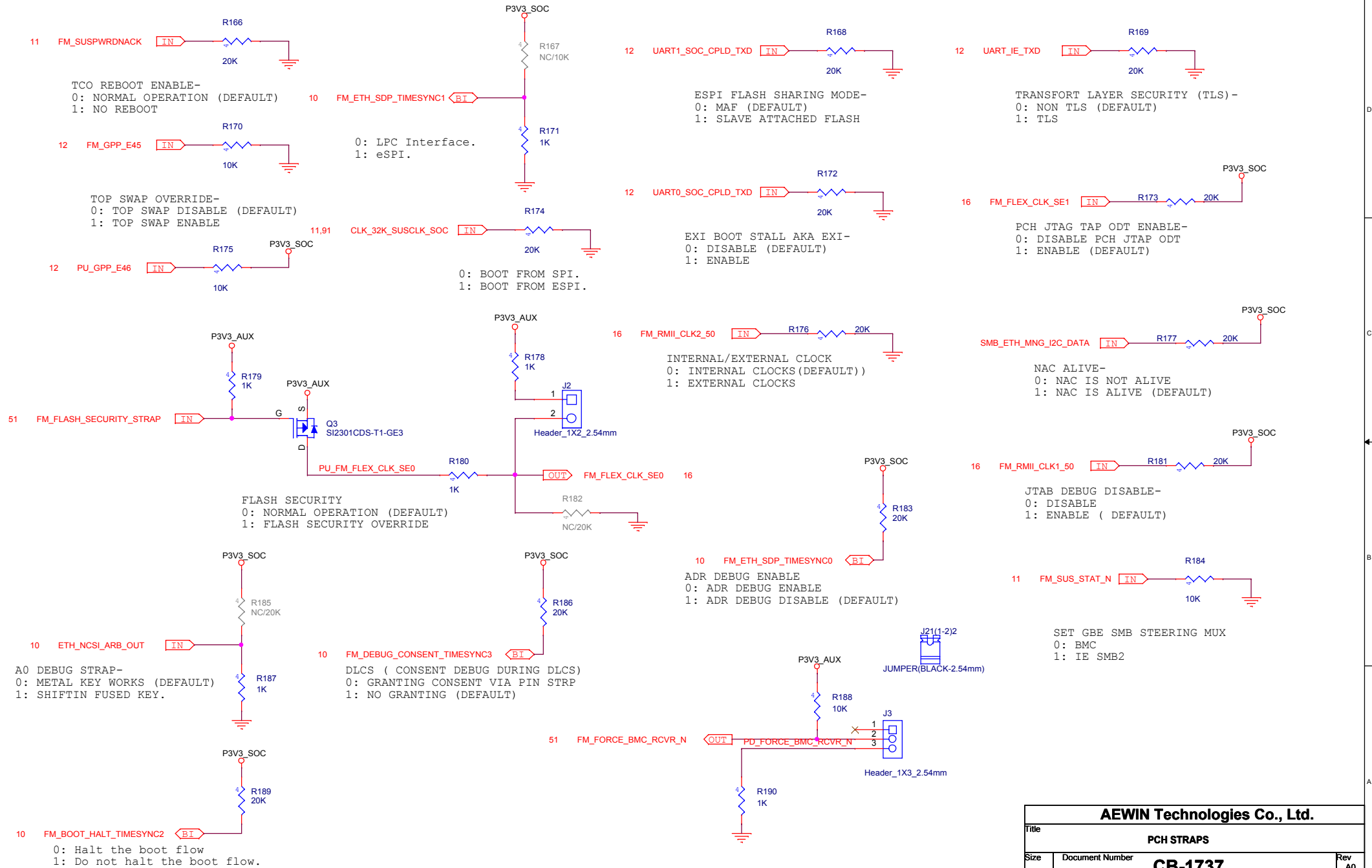






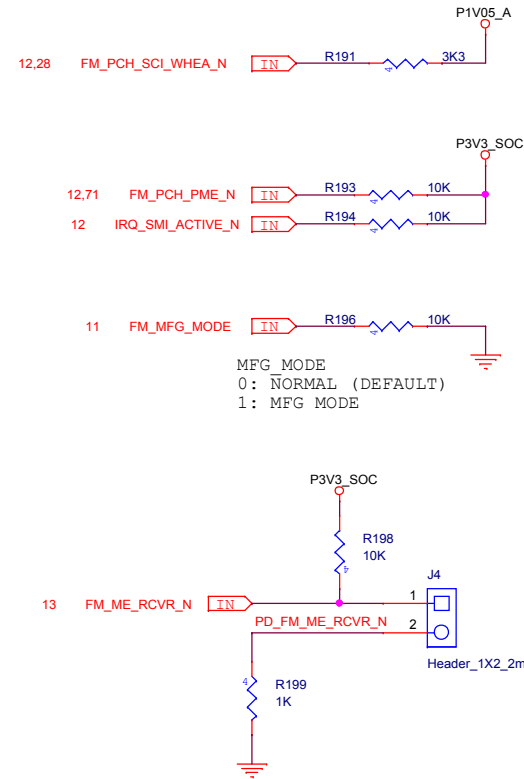
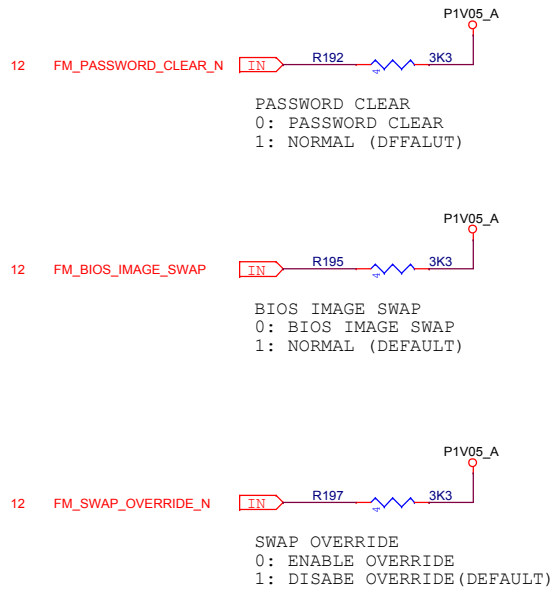


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Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 23	of 92

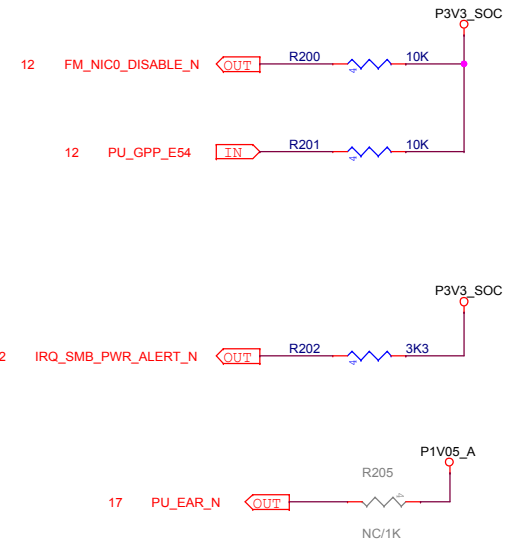
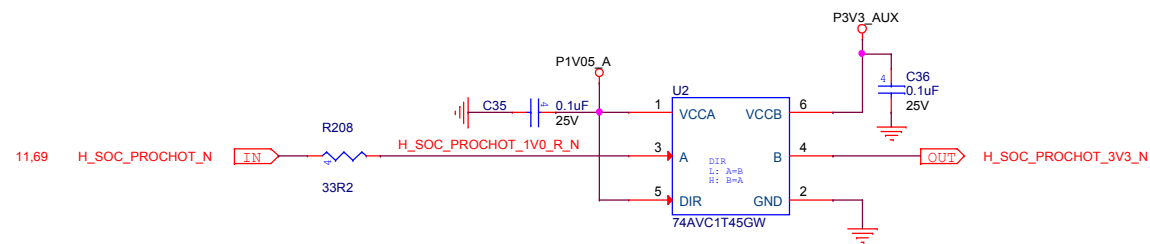
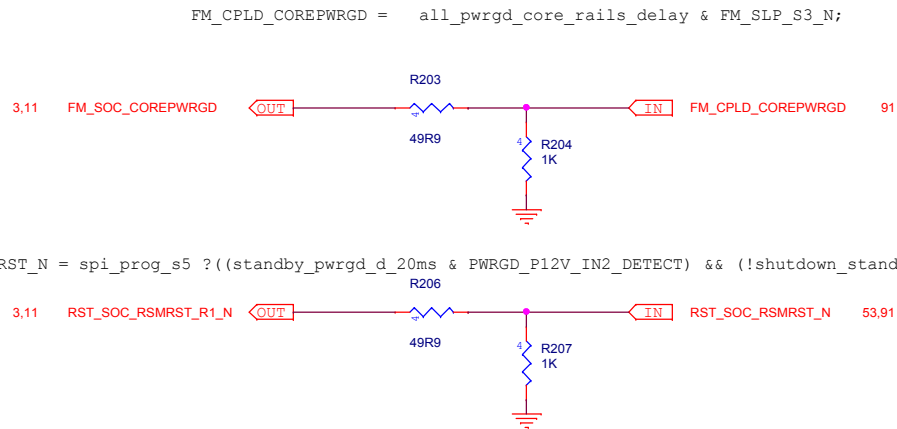


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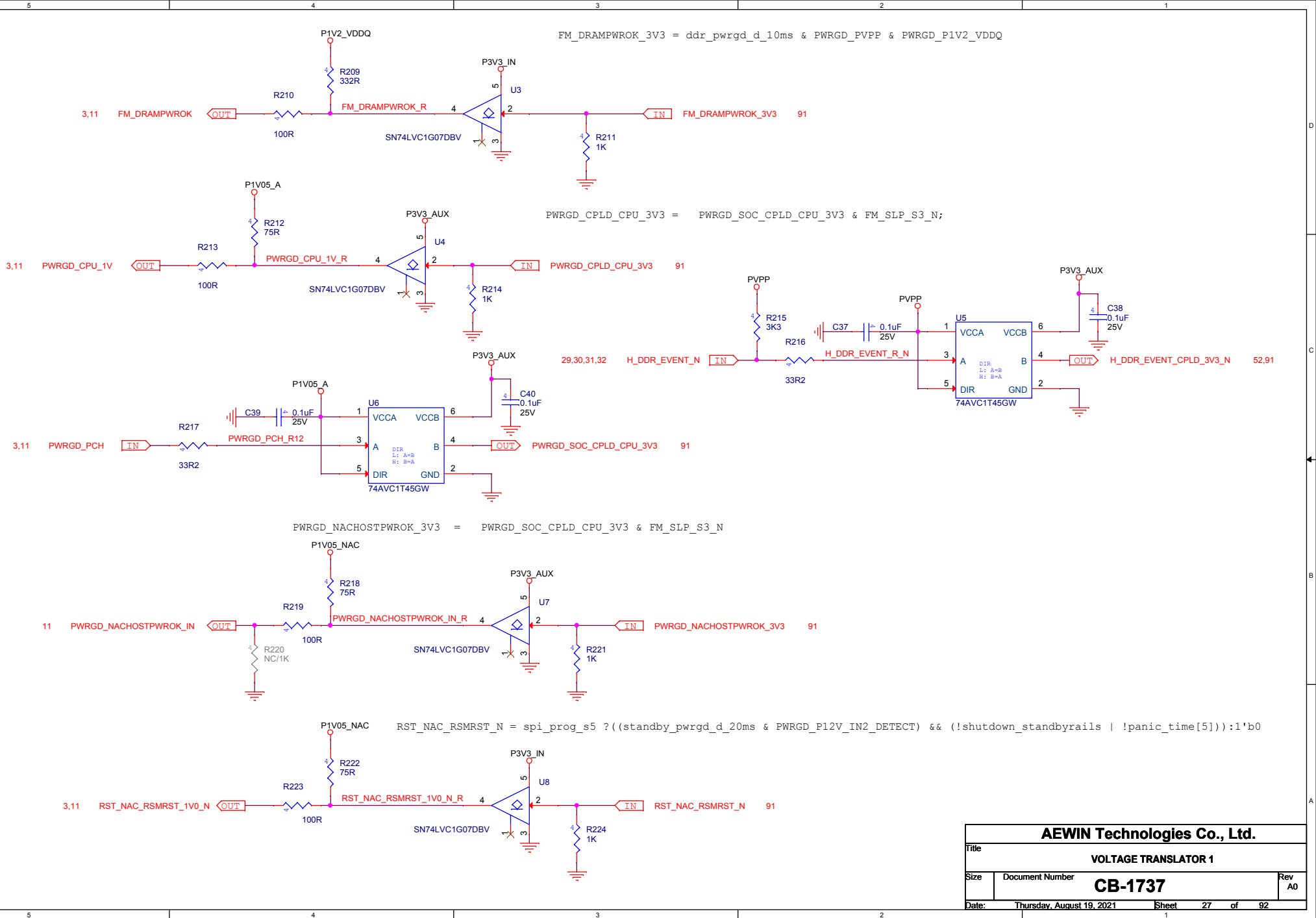
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Size	Document Number			Rev
	CB-1737			A0
Date:	Thursday, August 19, 2021		Sheet	24 of 92

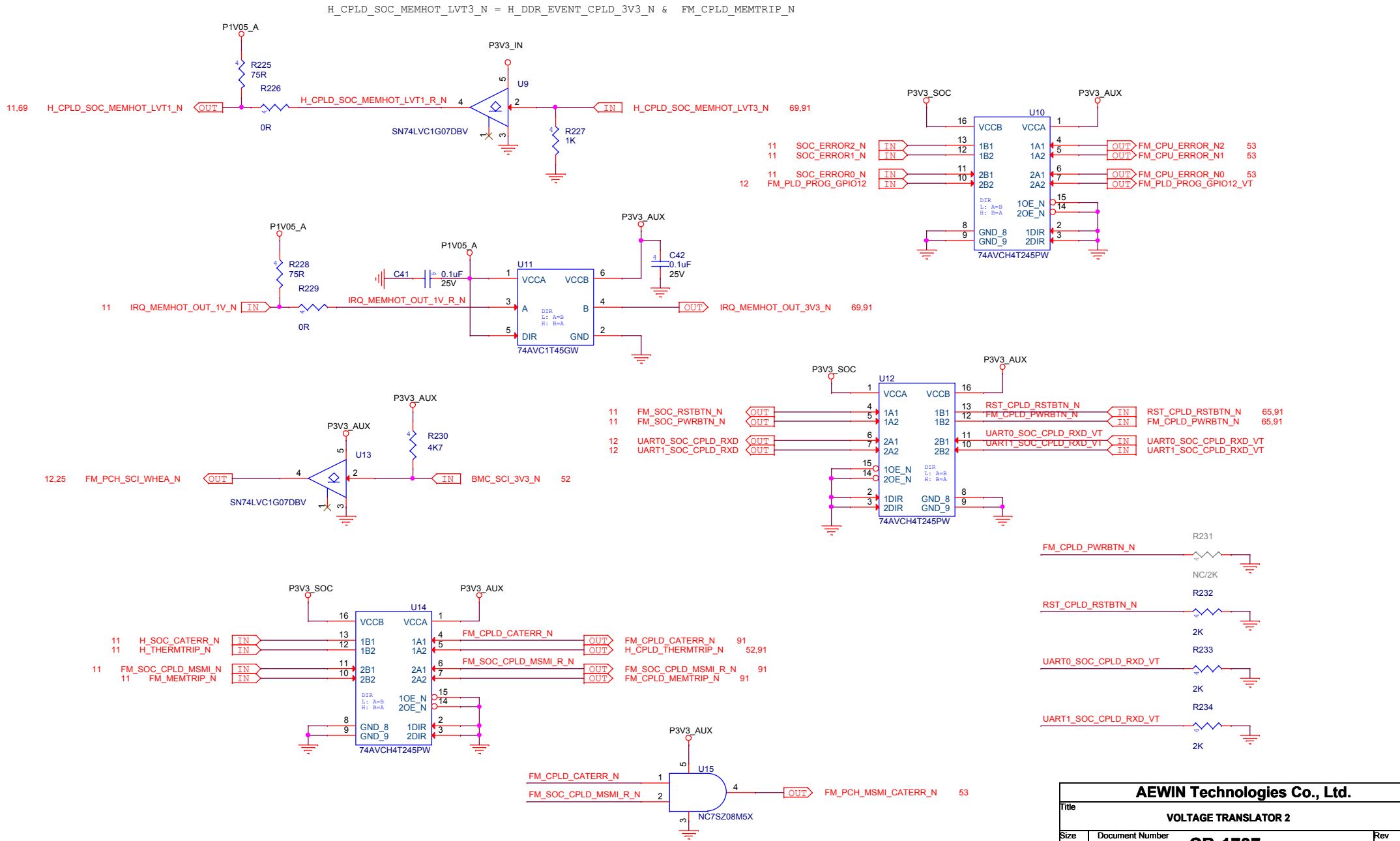


AEWIN Technologies Co., Ltd.			
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Size	Document Number		Rev
	CB-1737		A0
Date:	Thursday, August 19, 2021	Sheet	25 of 92



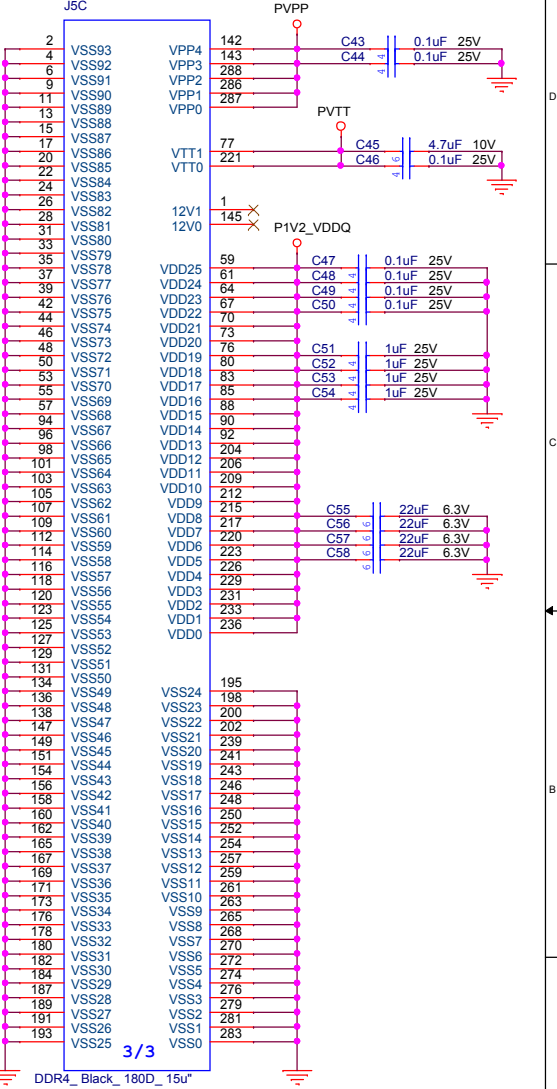
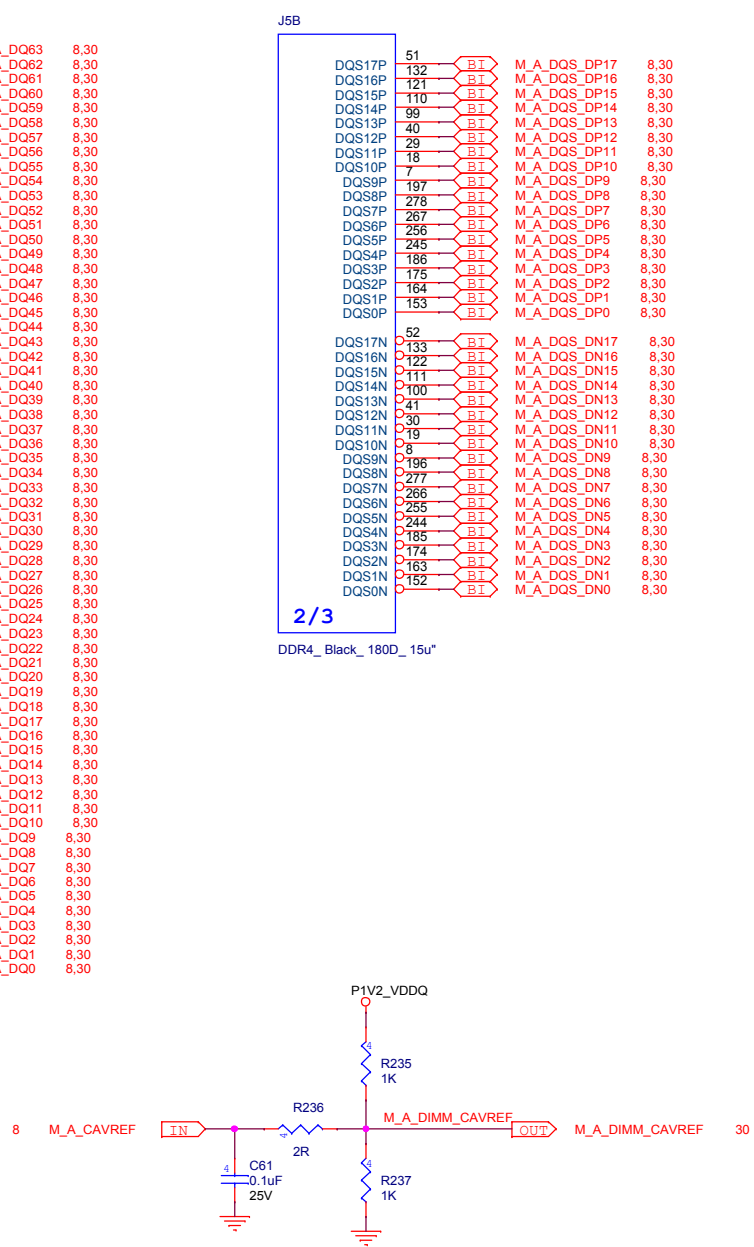
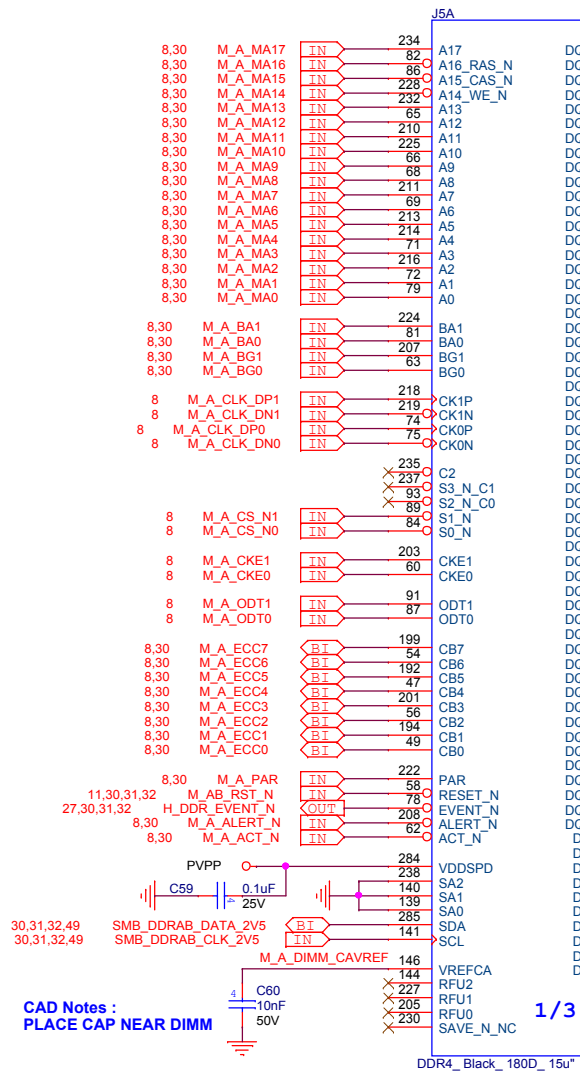
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Size	Document Number	Rev	A0
Date:		Thursday, August 19, 2021	
Sheet		26 of 92	

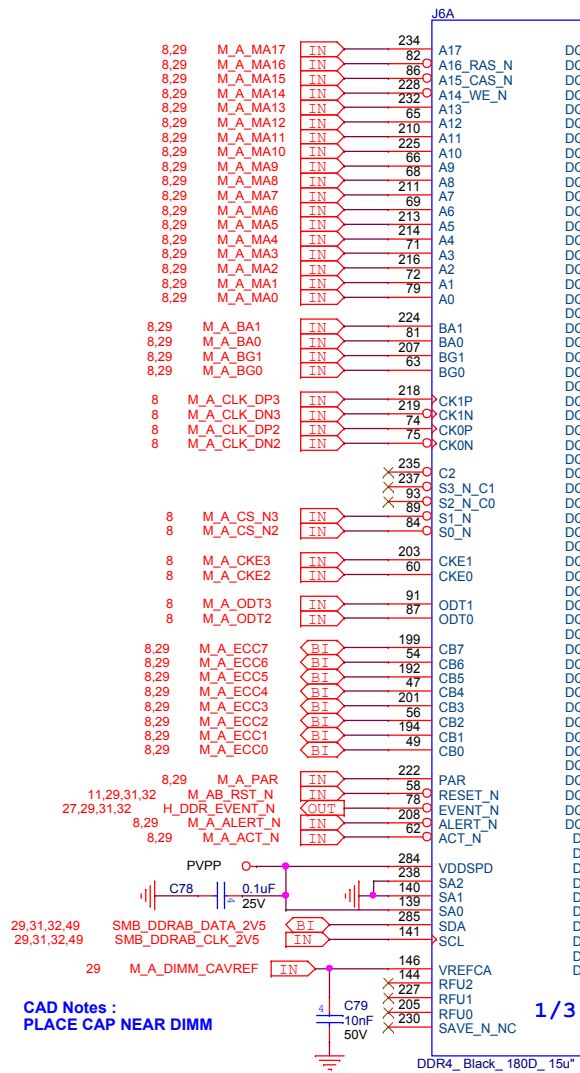




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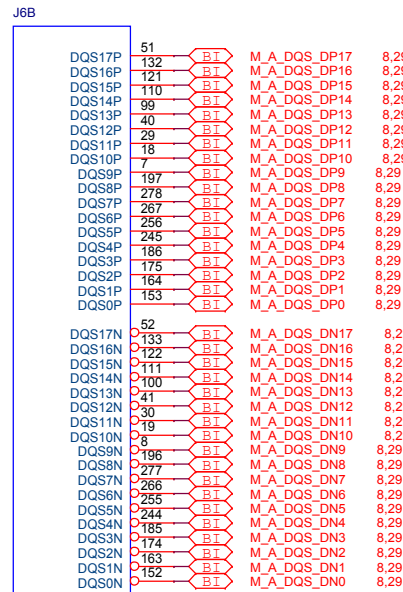
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Size	Document Number			Rev
	CB-1737			A0
Date:	Thursday, August 19, 2021		Sheet	28 of 92





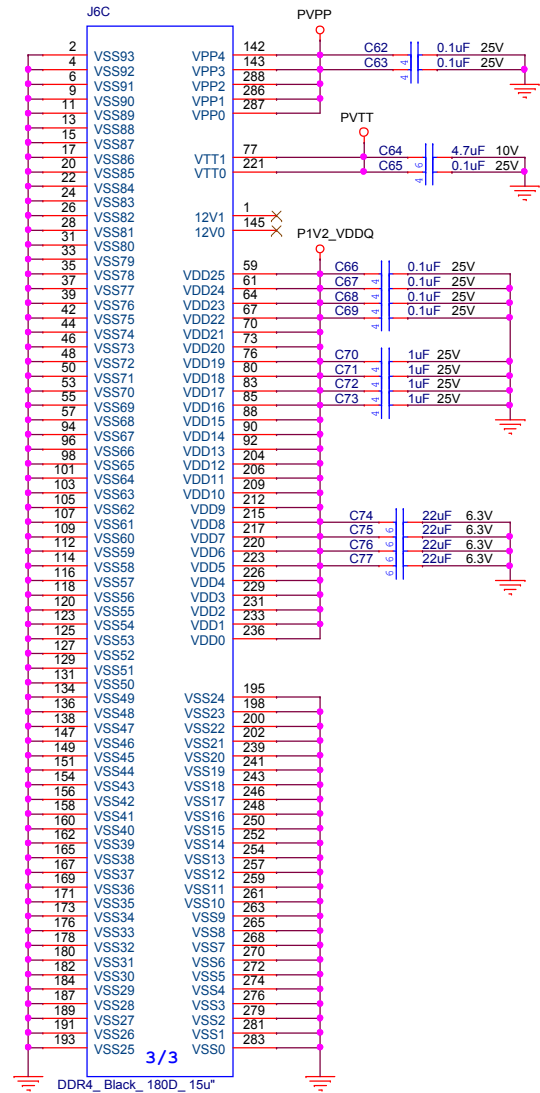
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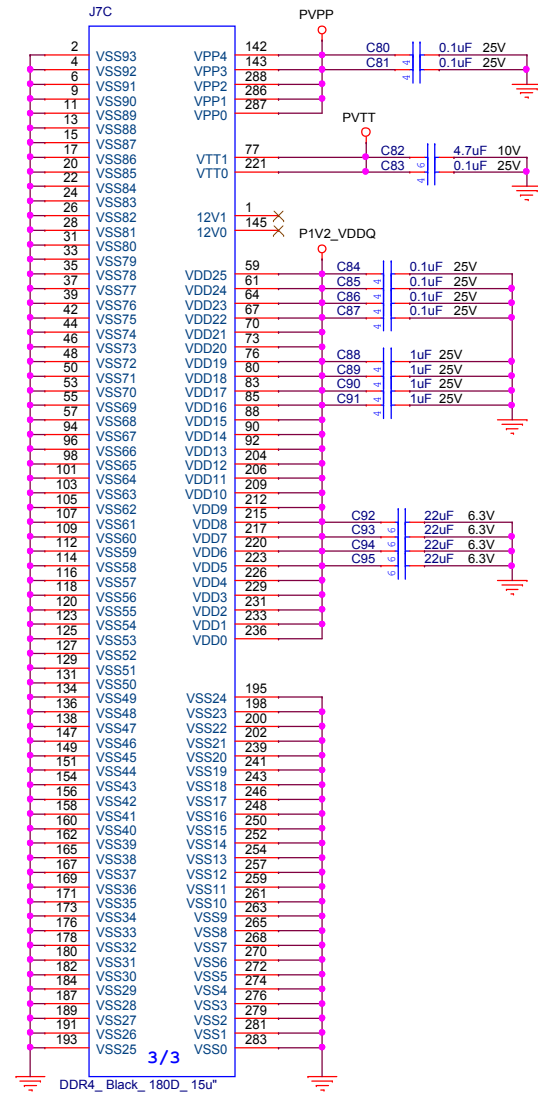
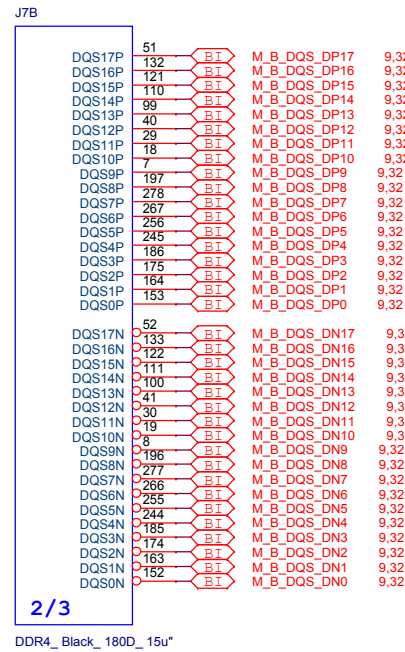
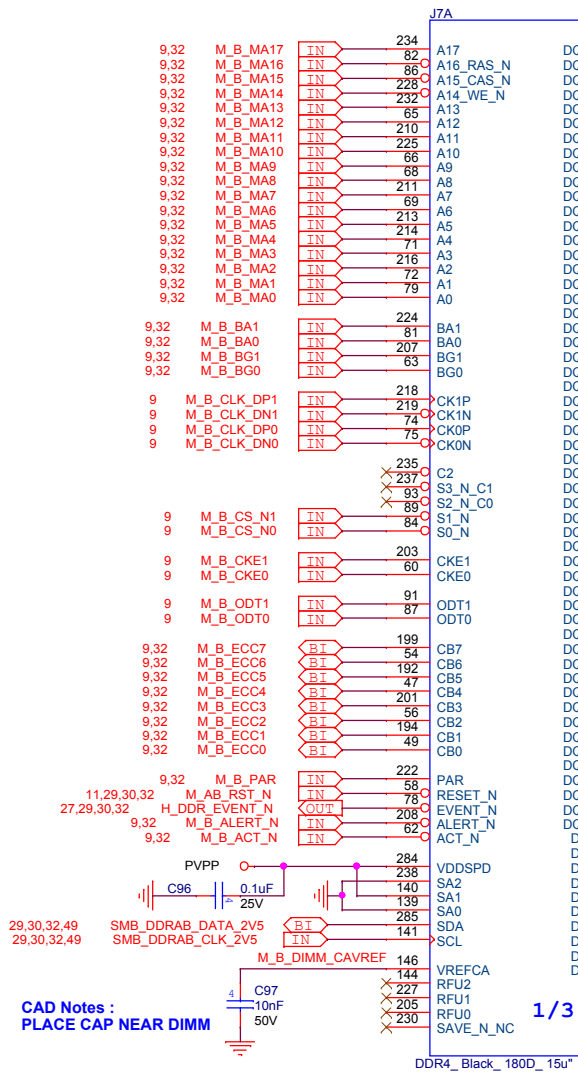
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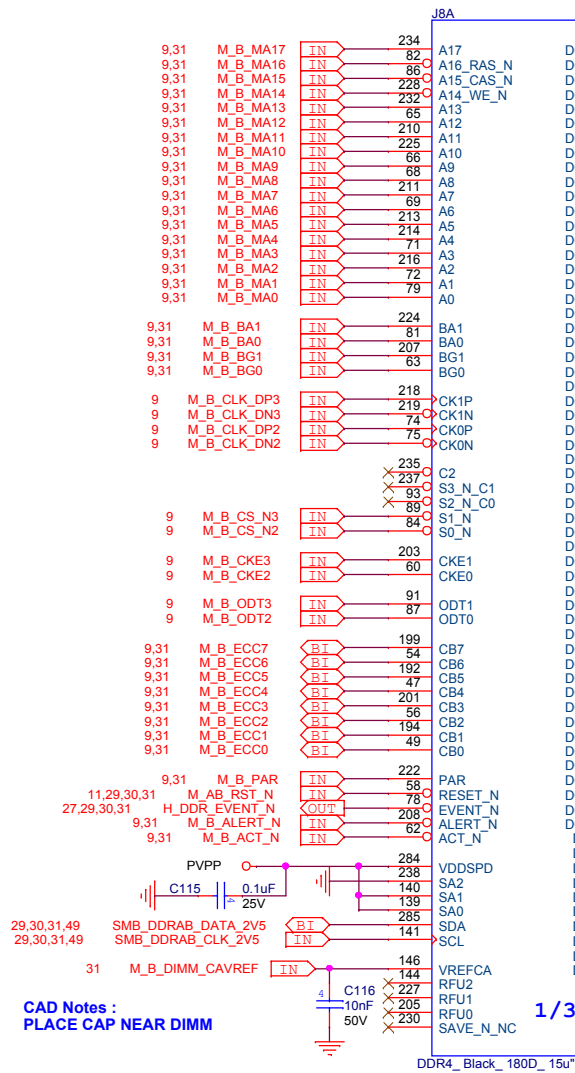


AEWIN Technologies Co., Ltd.

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Size	Document Number	Rev
	CB-1737	A0
Date:	Thursday, August 19, 2021	Sheet 30 of 92



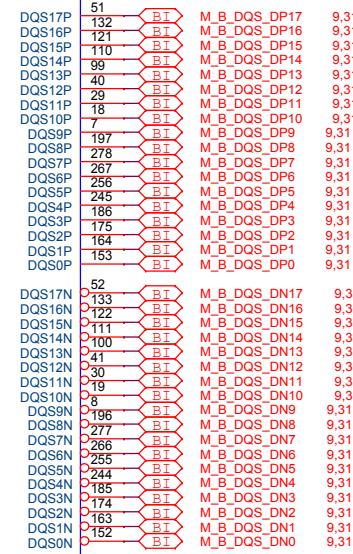
AEWIN Technologies Co., Ltd.			
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Size	Document Number	Rev	
	CB-1737	A0	
Date:	Thursday, August 19, 2021	Sheet	31 of 92



1/3

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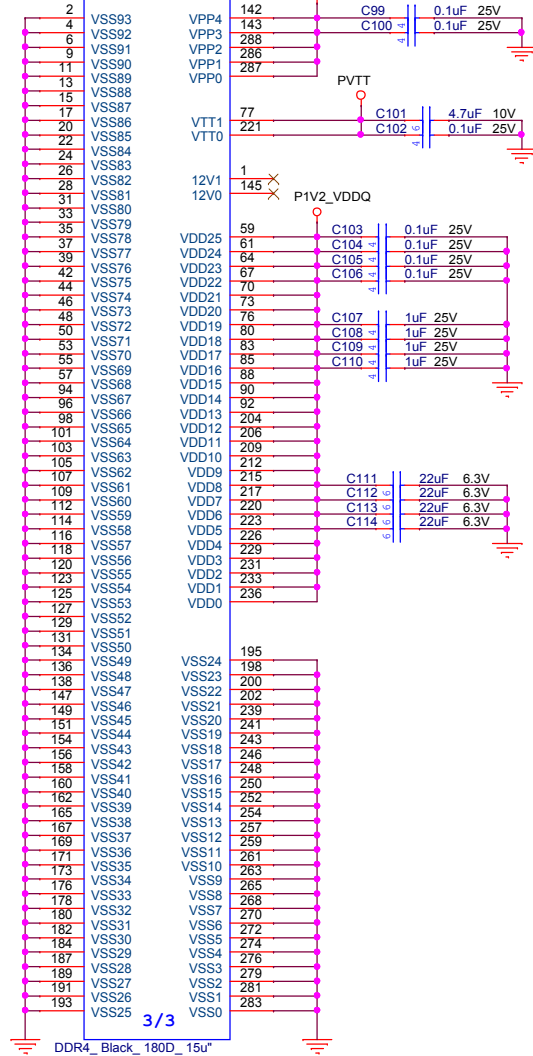
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2/3

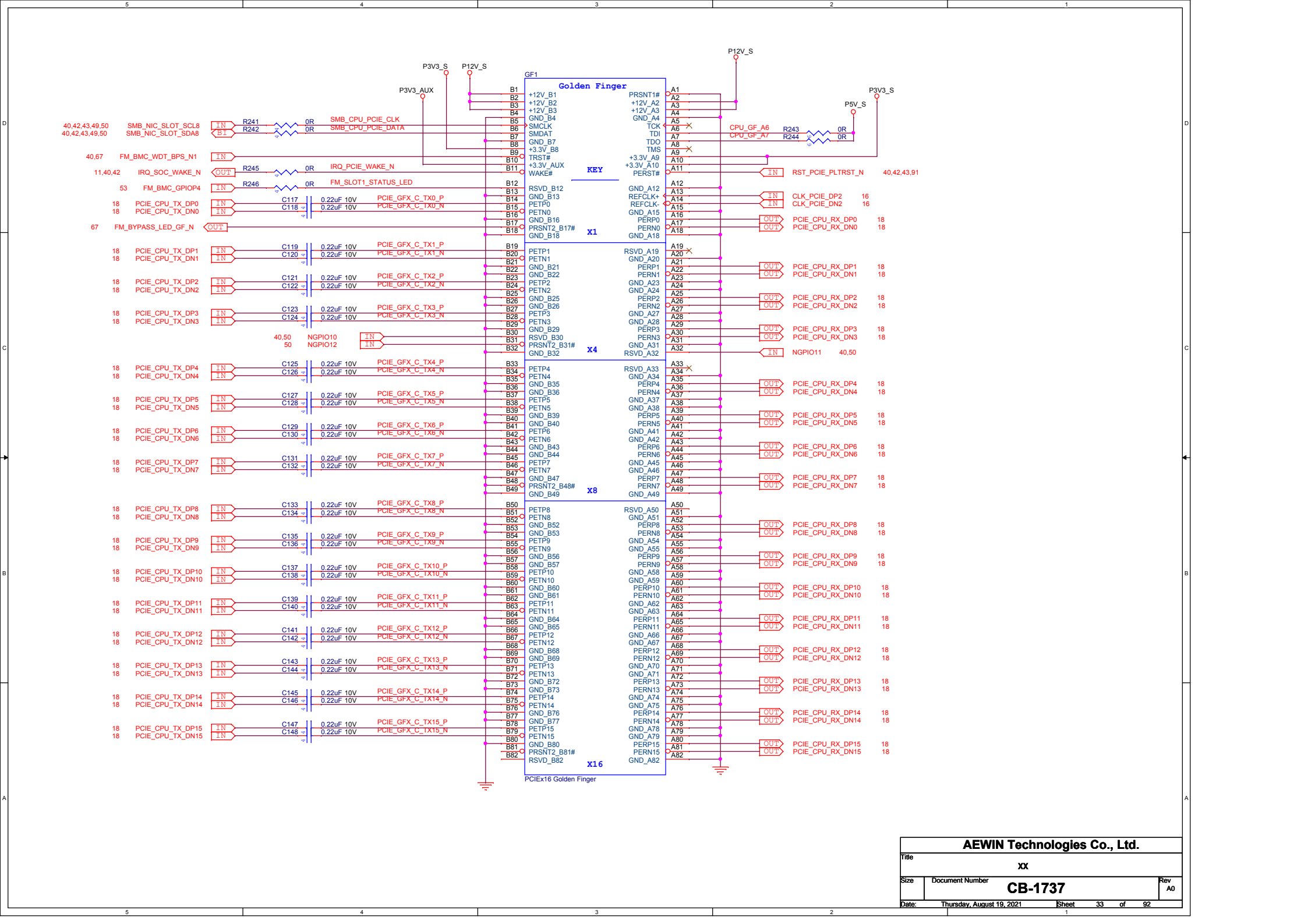
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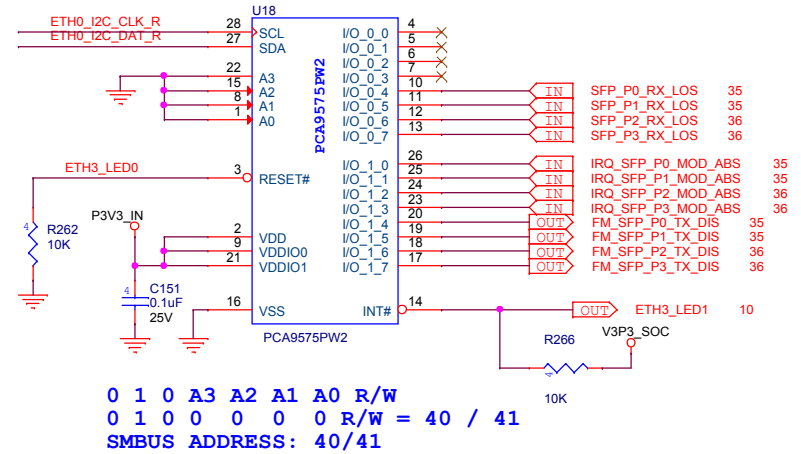
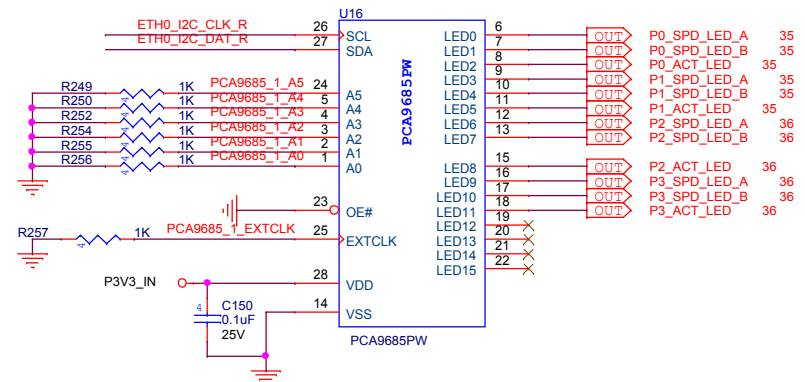
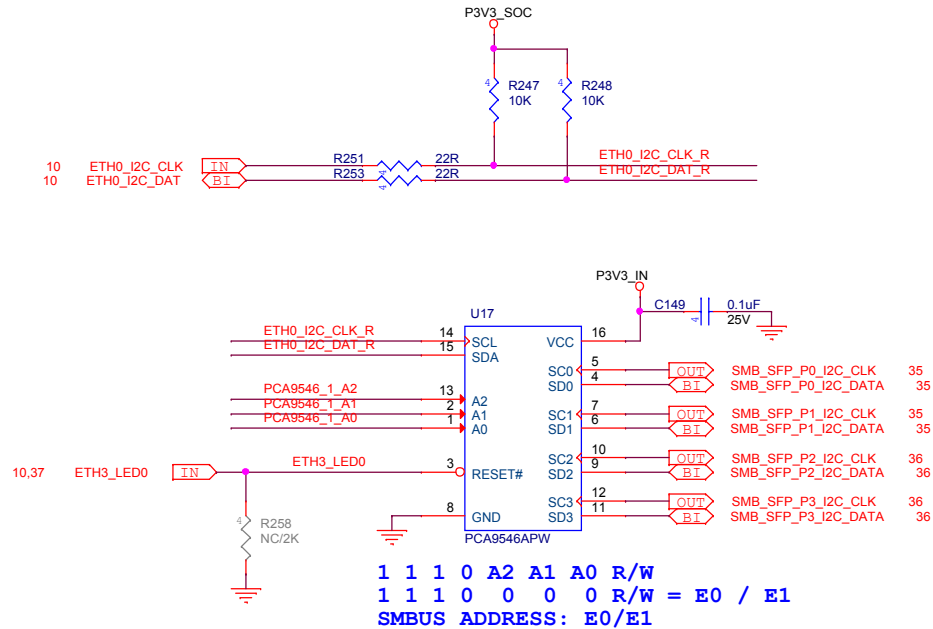
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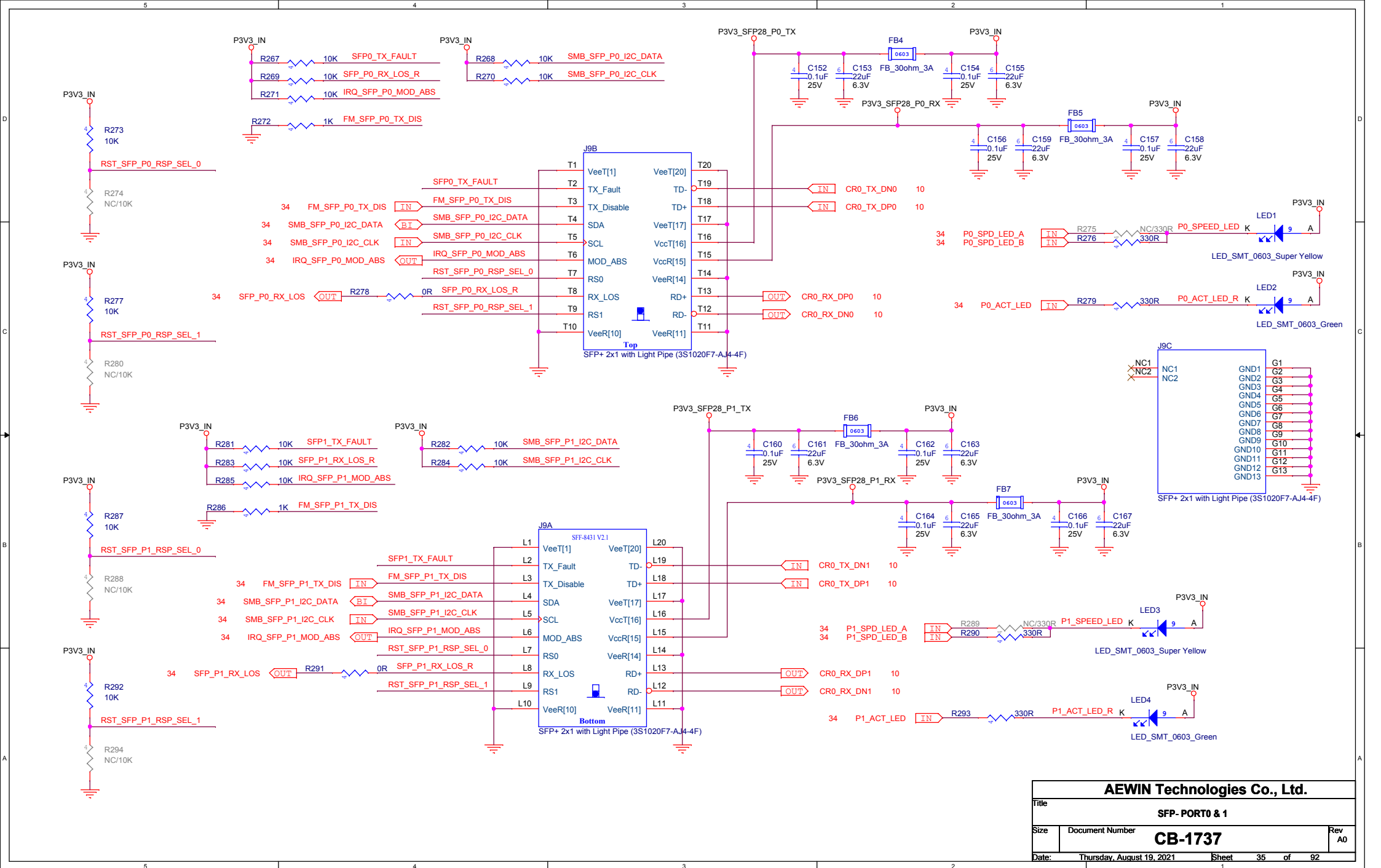
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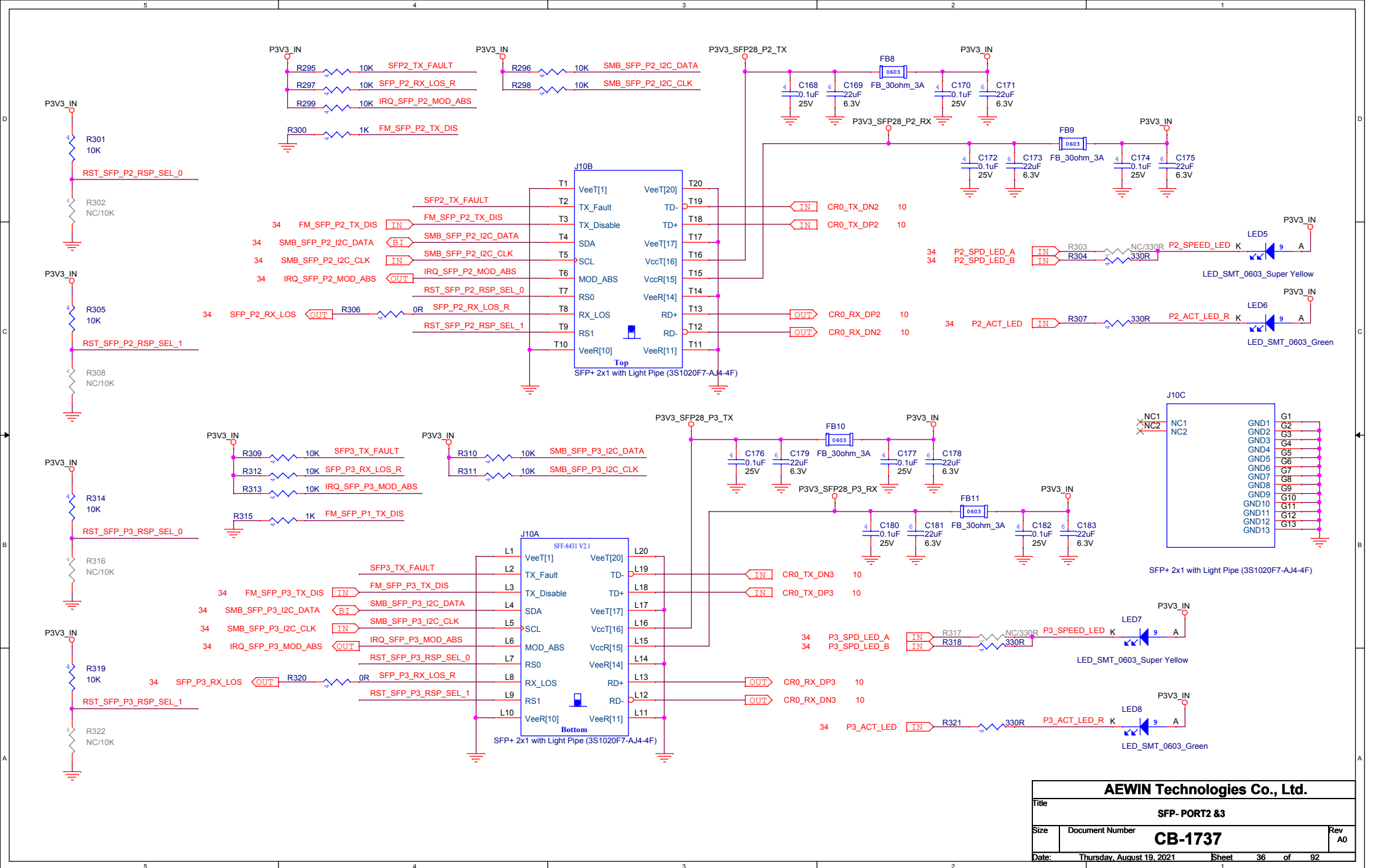
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Size	Document Number	Rev	
	CB-1737	A0	
Date:	Thursday, August 19, 2021	Sheet	32 of 92





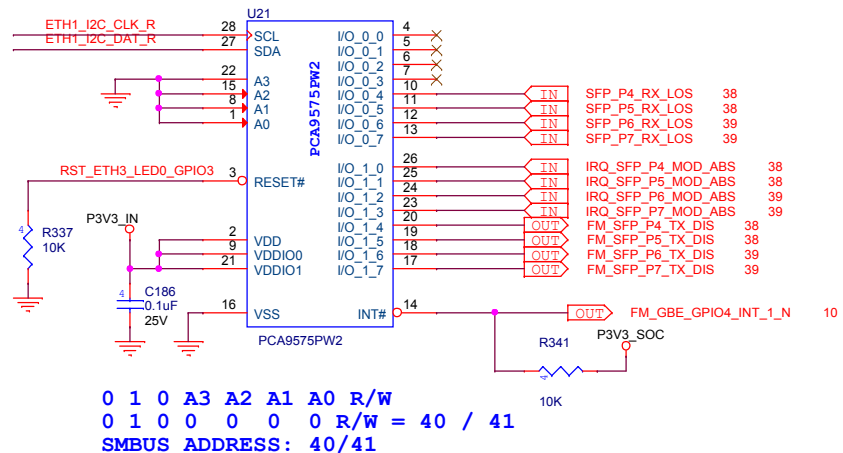
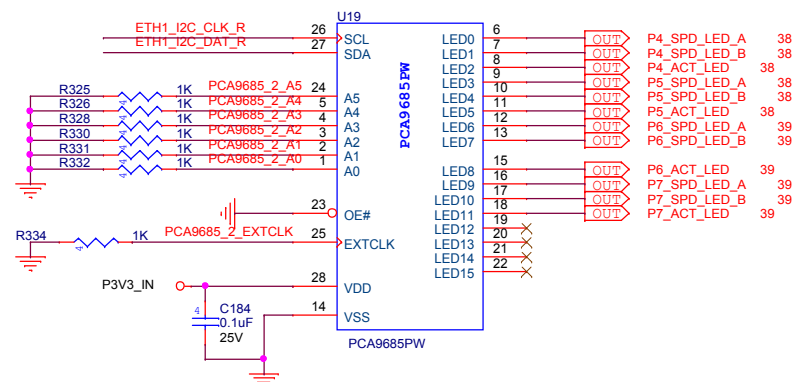
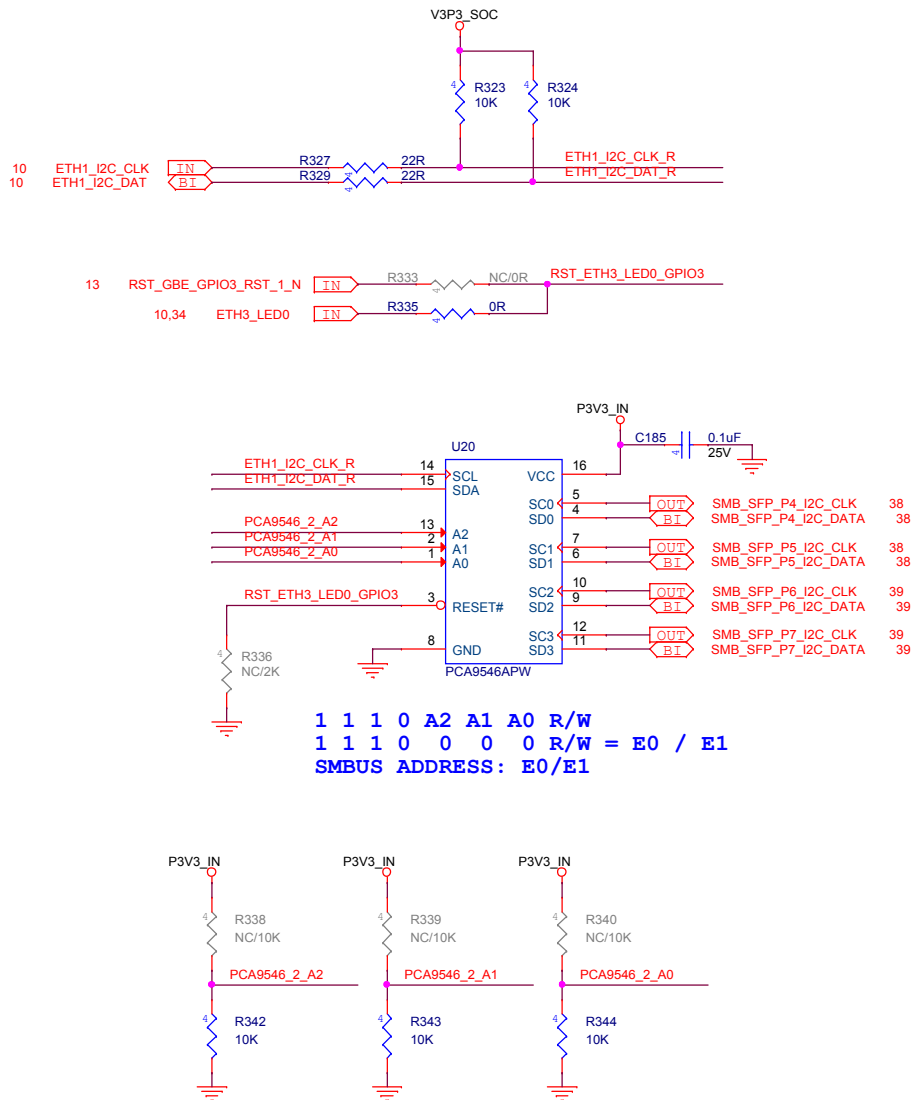
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Size	Document Number		Rev
	CB-1737		A0
Date:	Thursday, August 19, 2021		Sheet 34 of 92



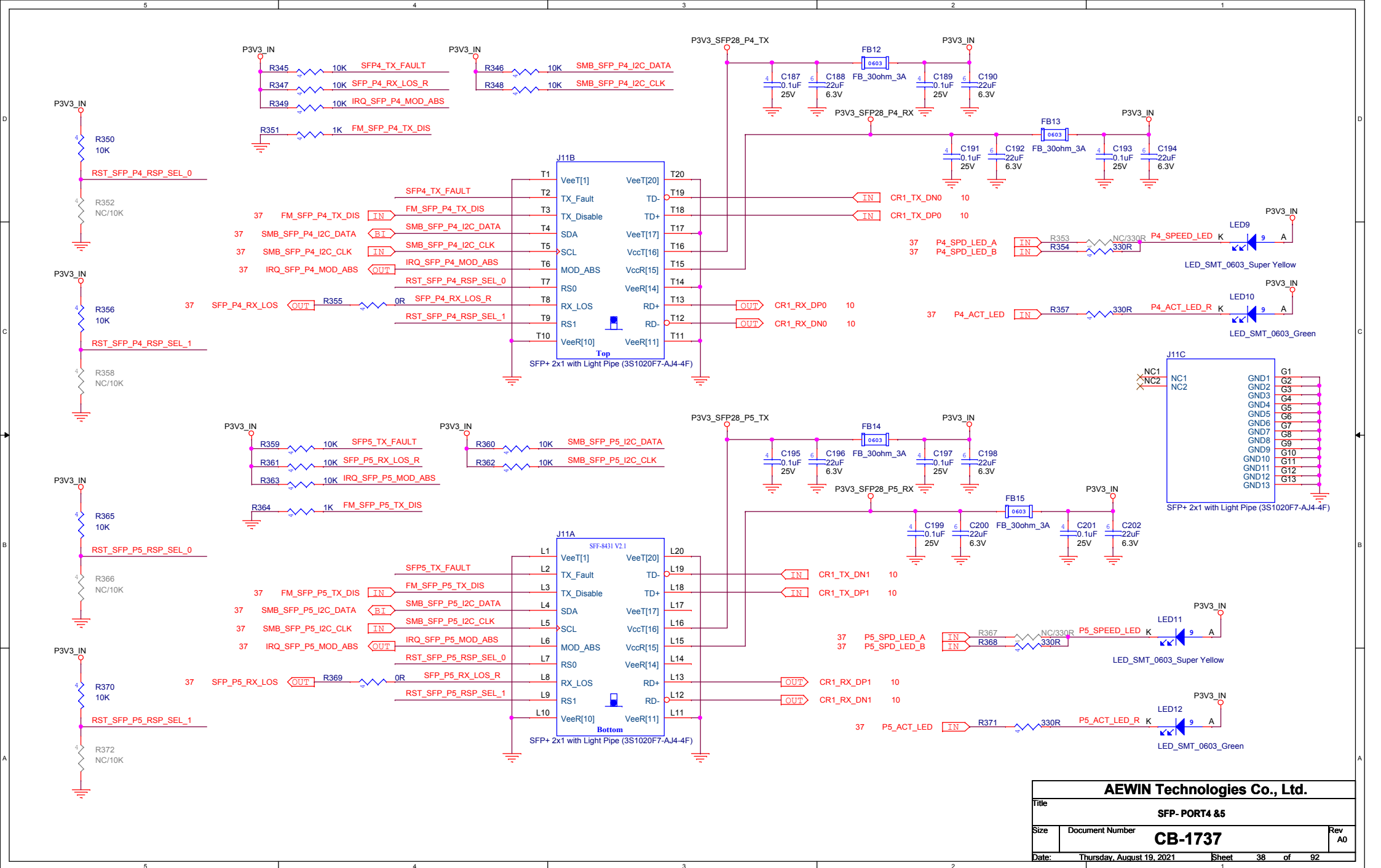


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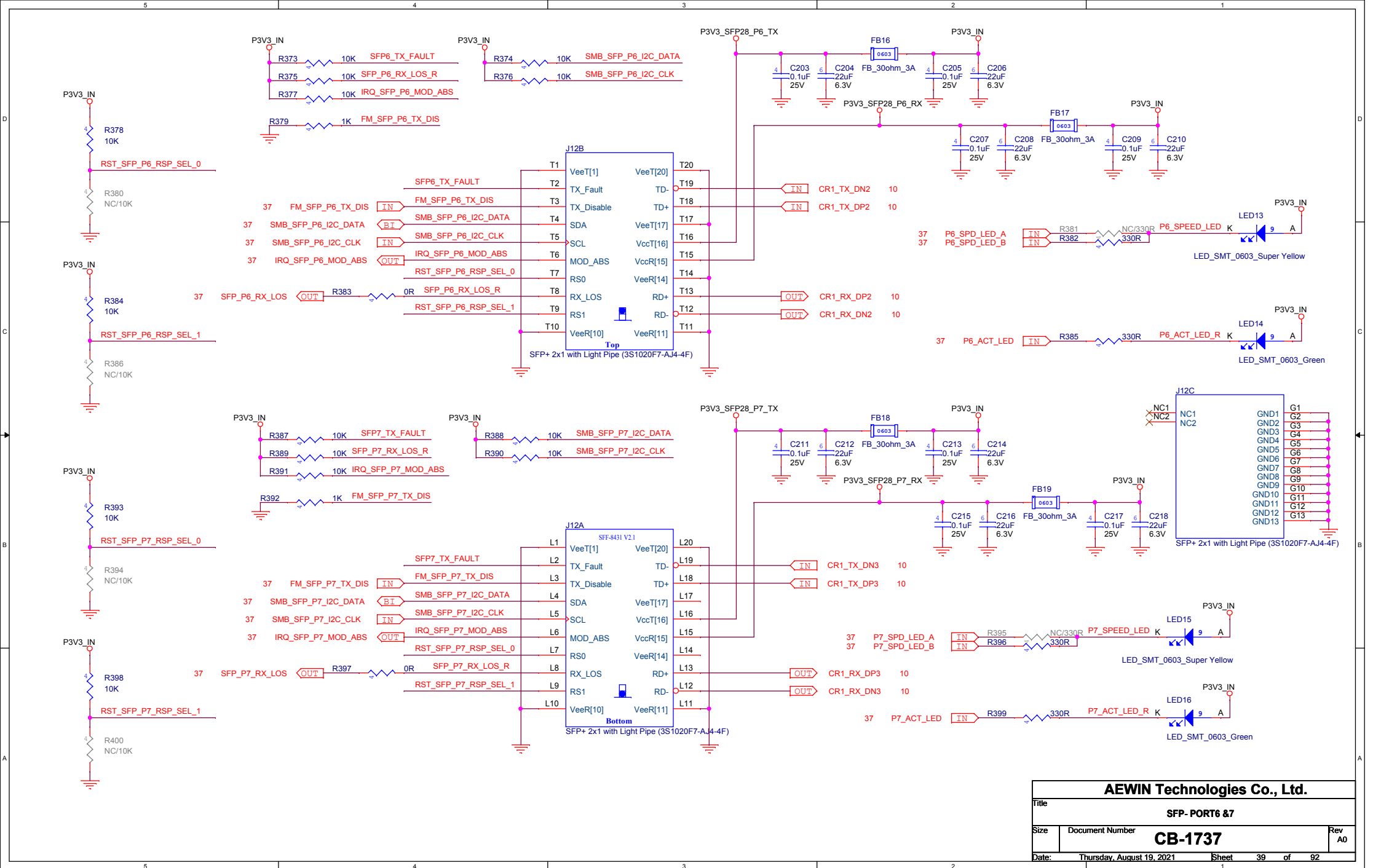
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Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 36	of 92

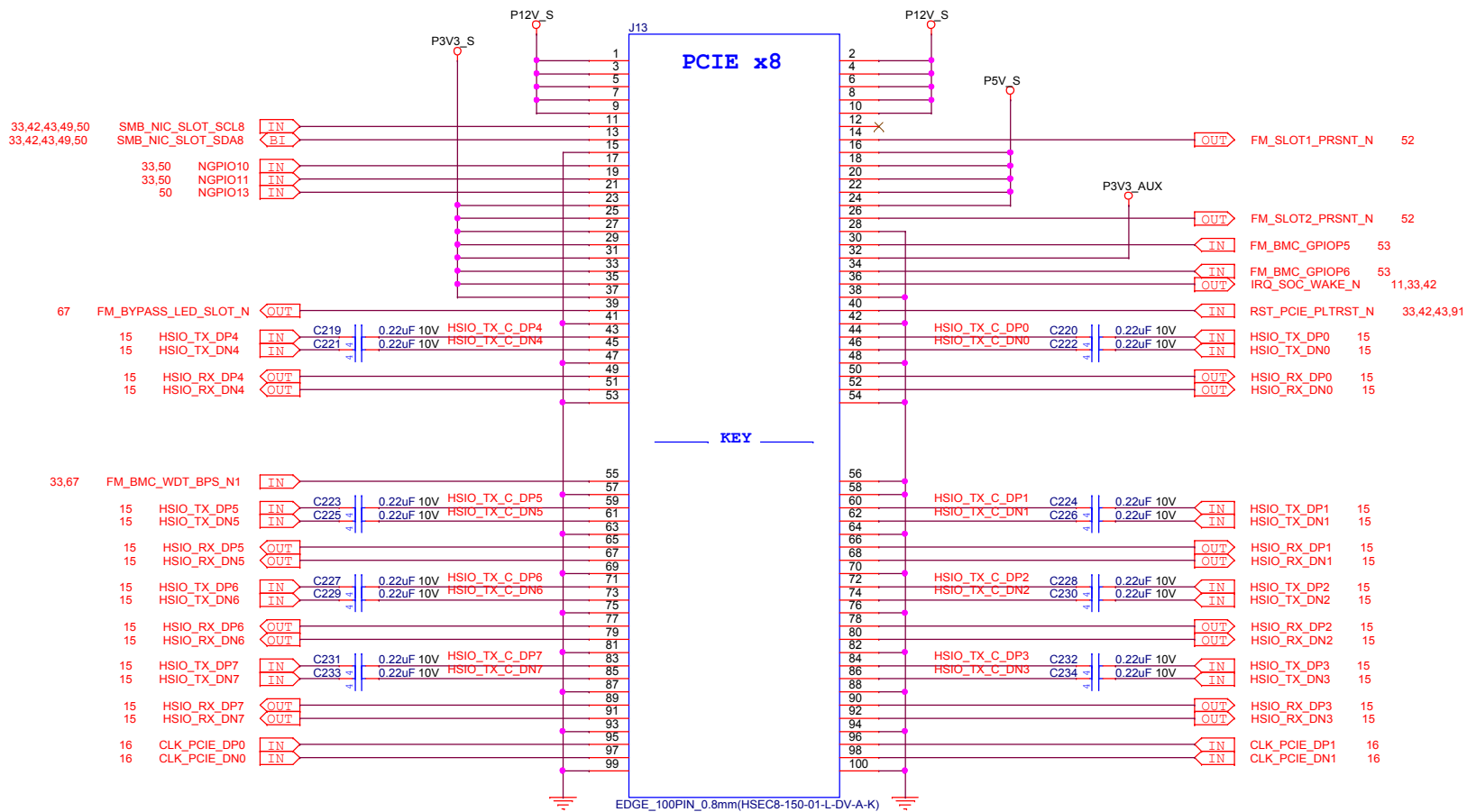


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Size	Document Number		Rev
	CB-1737		A0
Date:	Thursday, August 19, 2021		Sheet 37 of 92



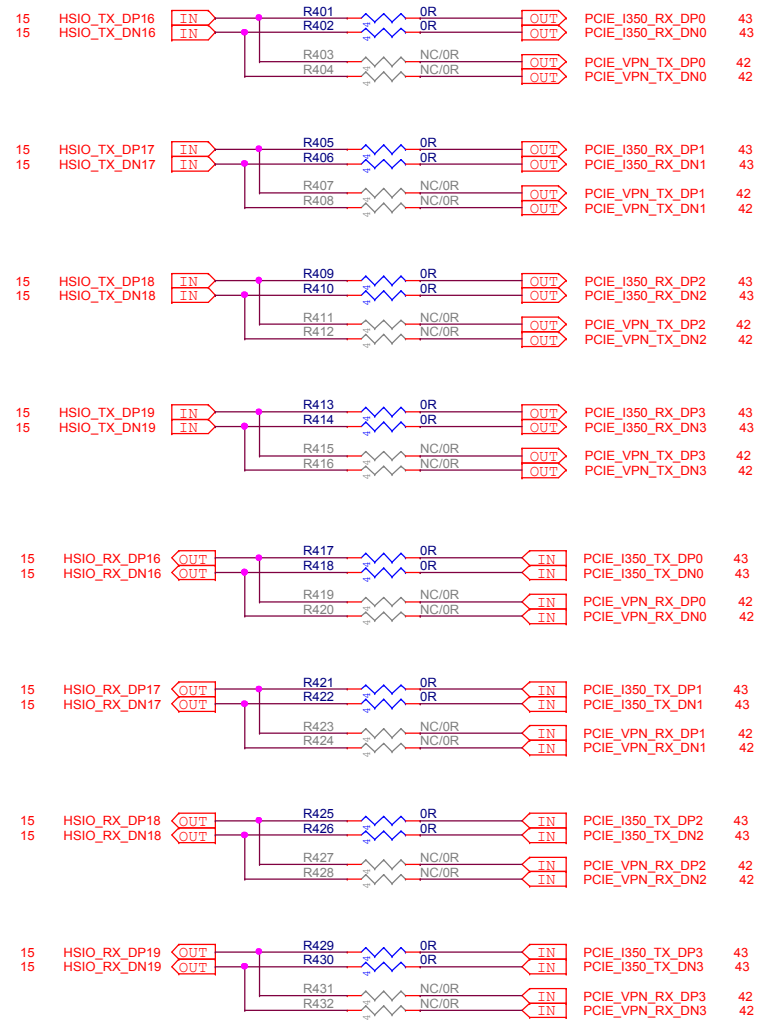
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Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 38	of 92



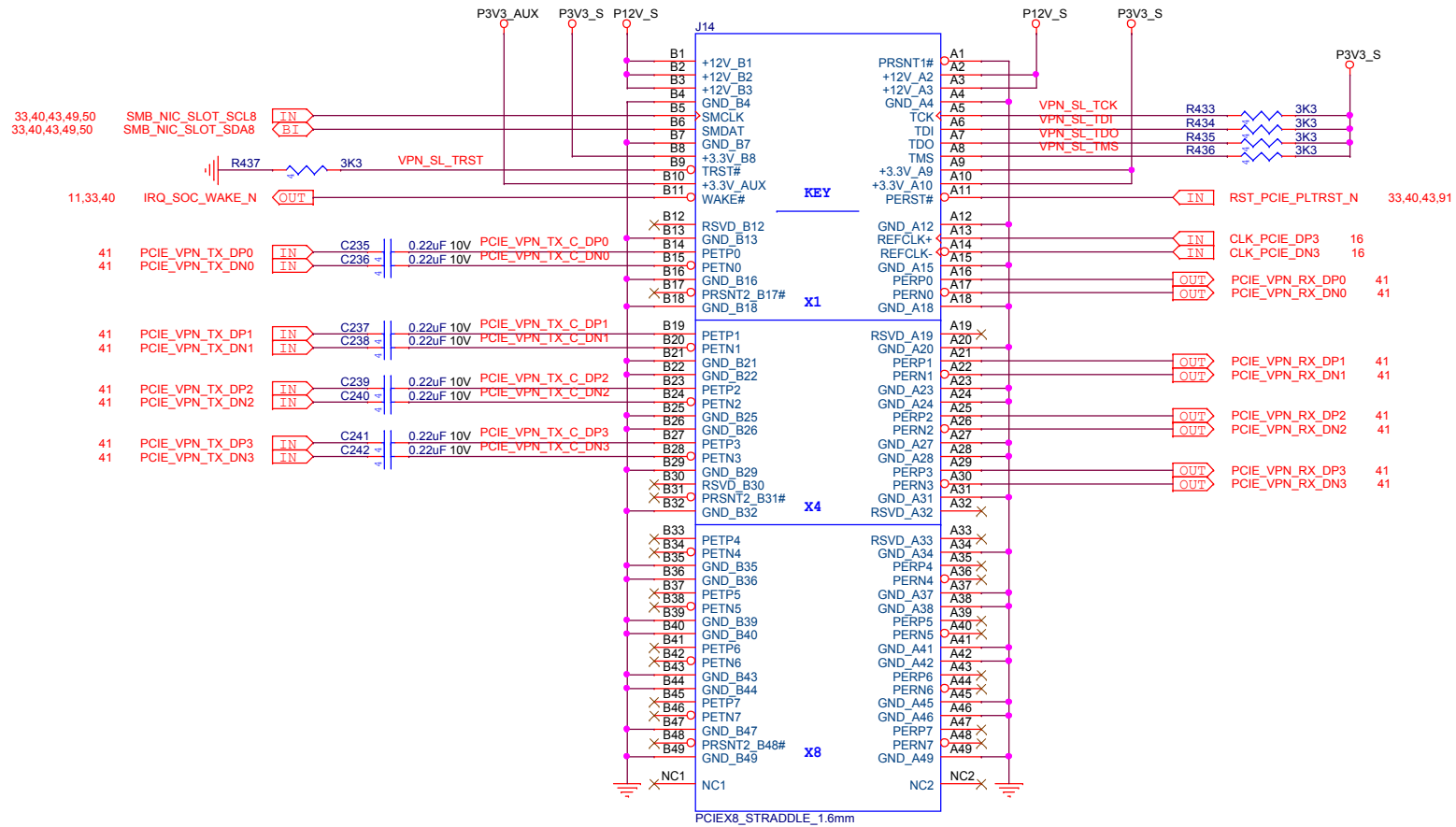


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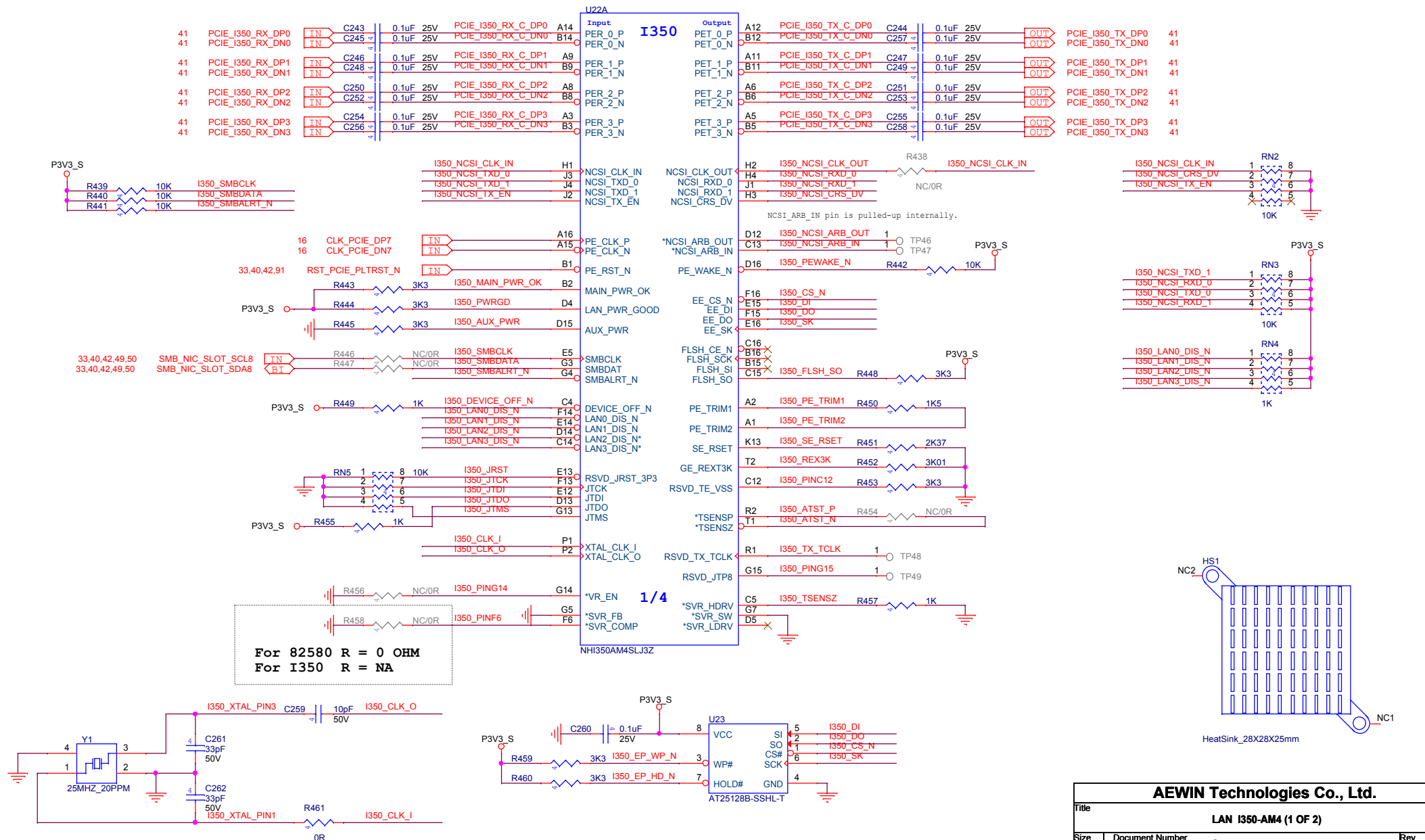
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Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 40 of 92	

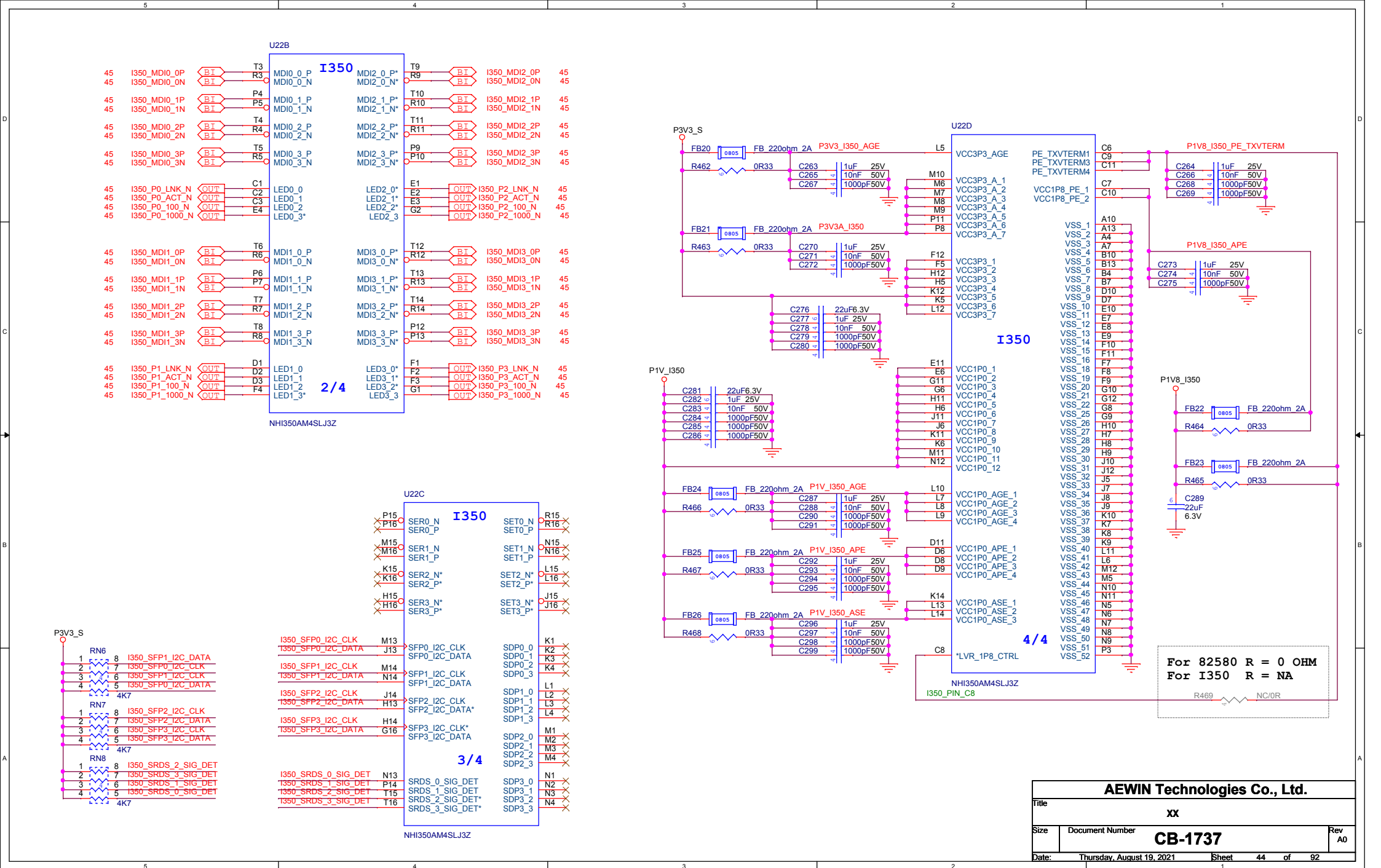


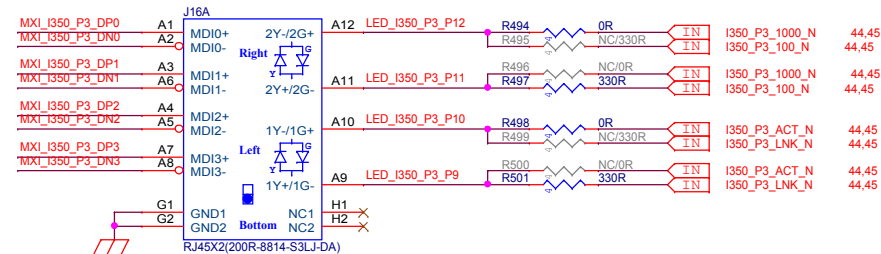
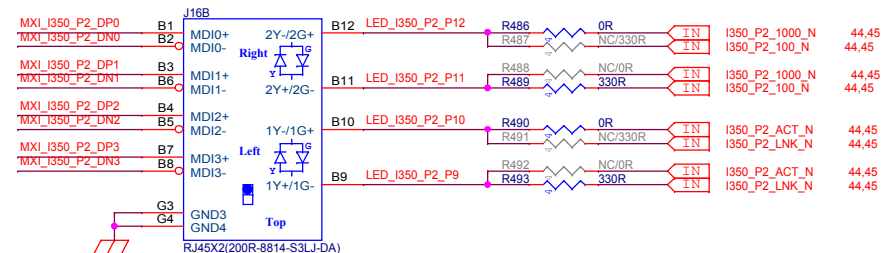
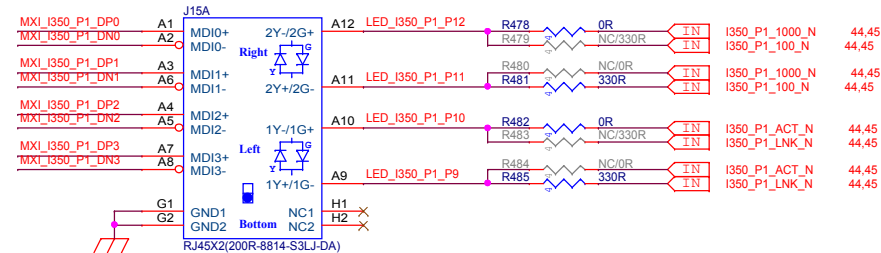
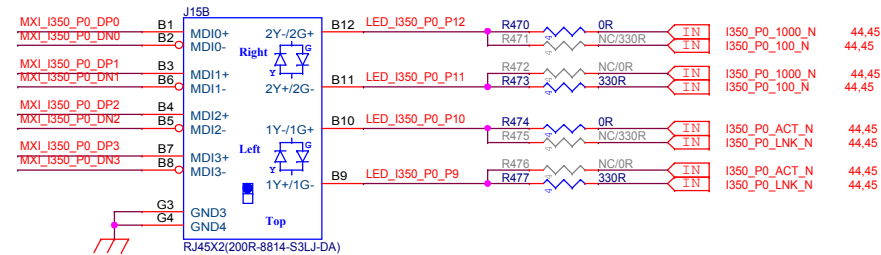
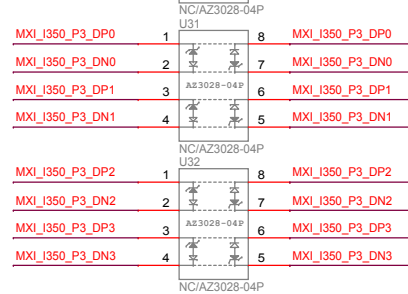
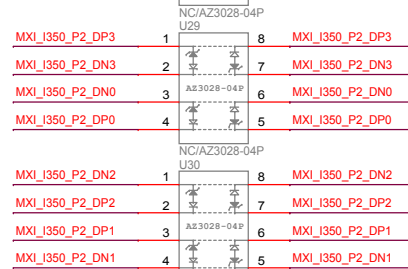
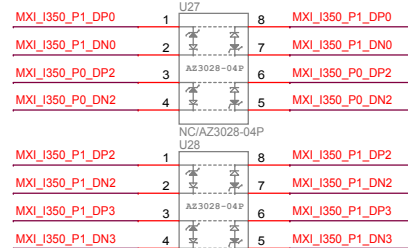
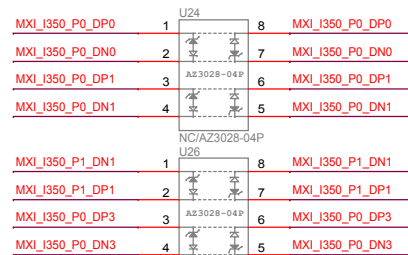
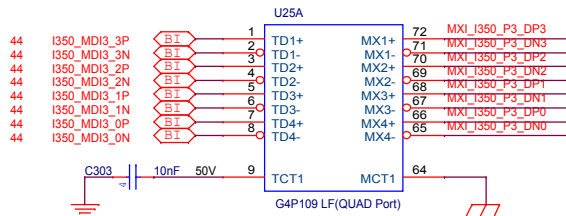
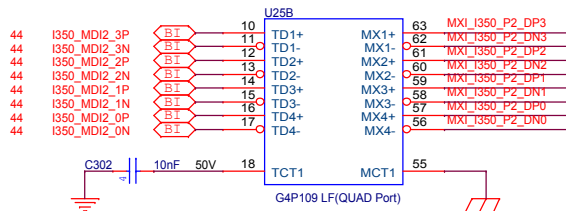
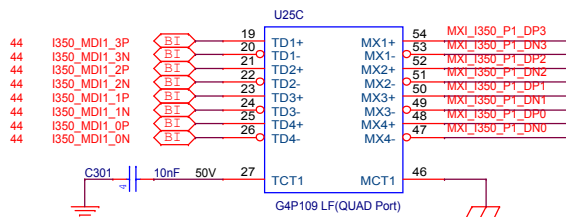
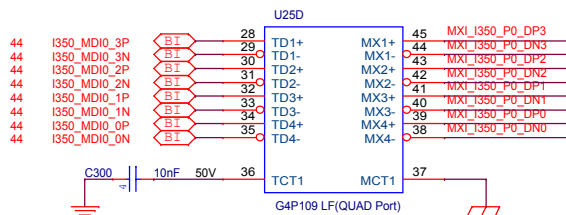
AEWIN Technologies Co., Ltd.			
Title		XX	
Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 41 of 92	

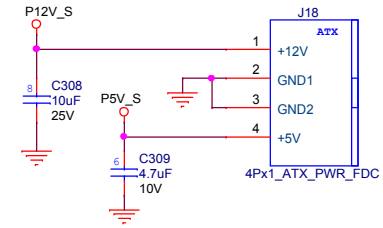
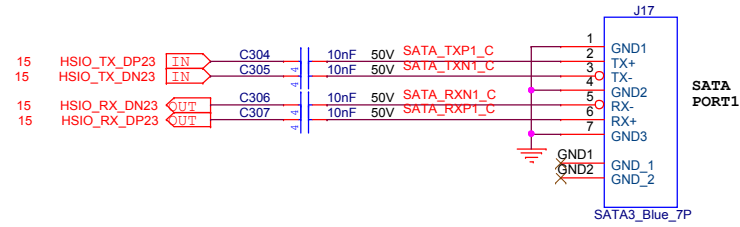


AEWIN Technologies Co., Ltd.			
Title		PCIE- SLOT (VPN)	
Size	Document Number	CB-1737	
Date:		Thursday, August 19, 2021	Sheet 42 of 92
			Rev A0

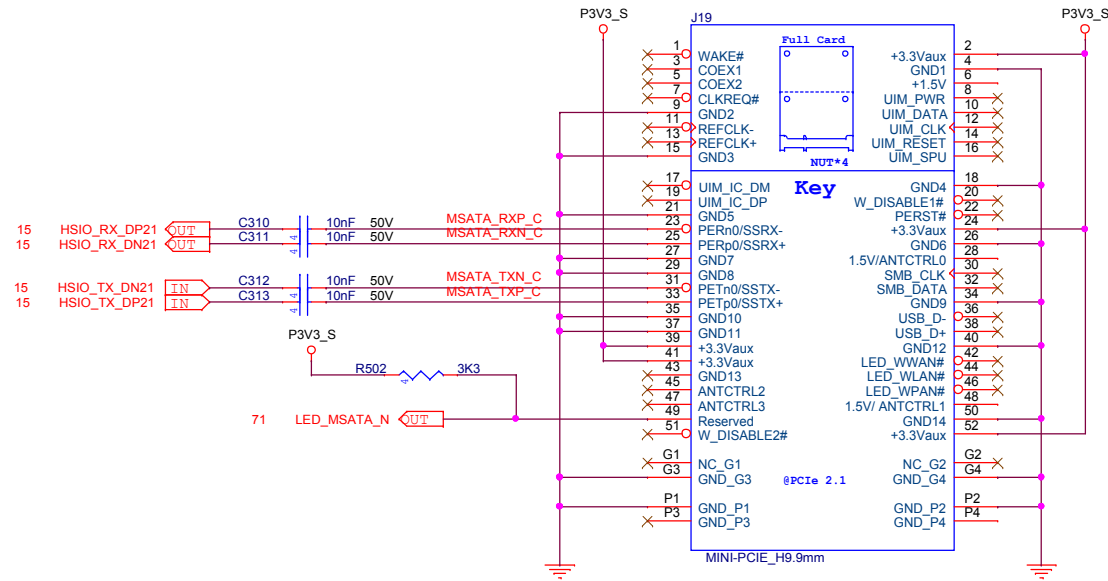






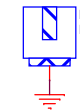
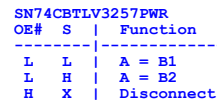


+12V
Spin up: 2A
Operation: 0.46A

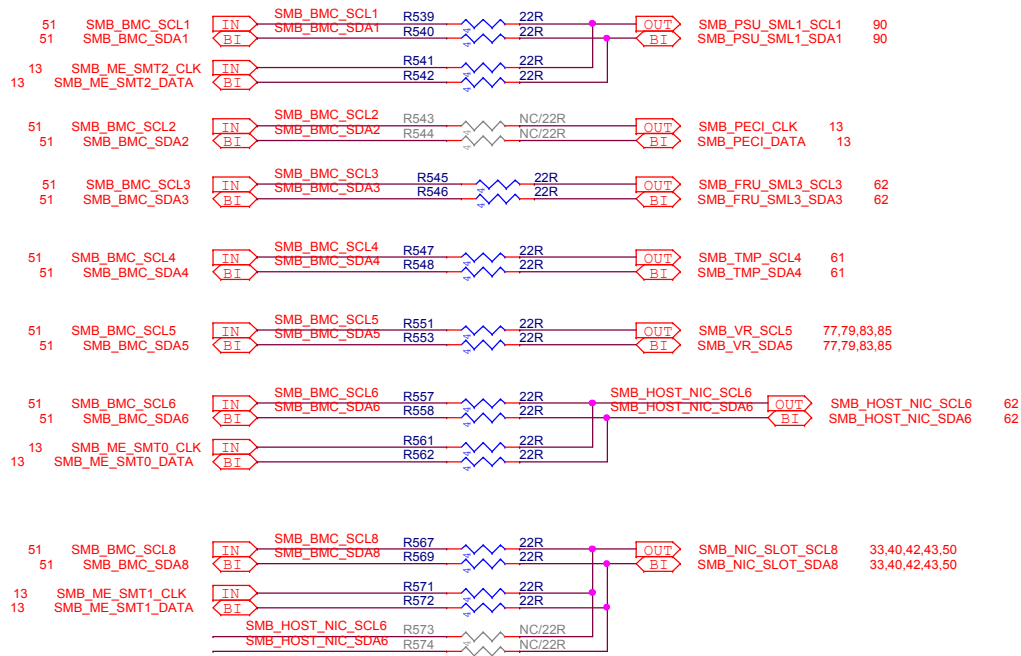
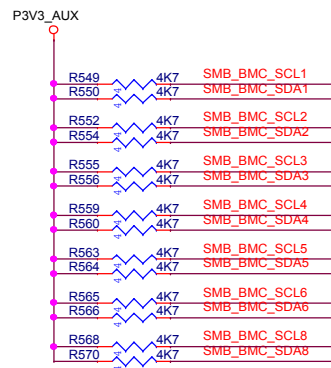
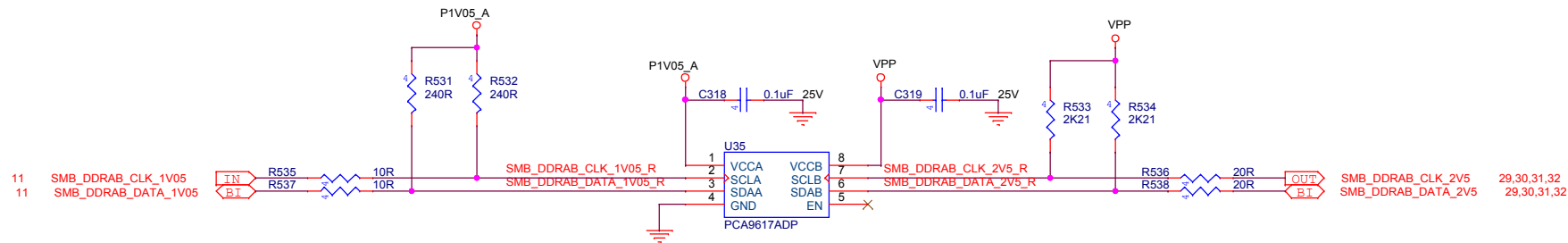


AEWIN Technologies Co., Ltd.			
Title		SATA & MSATA	
Size	Document Number	CB-1737	
Date:	Thursday, August 19, 2021	Sheet	46 of 92

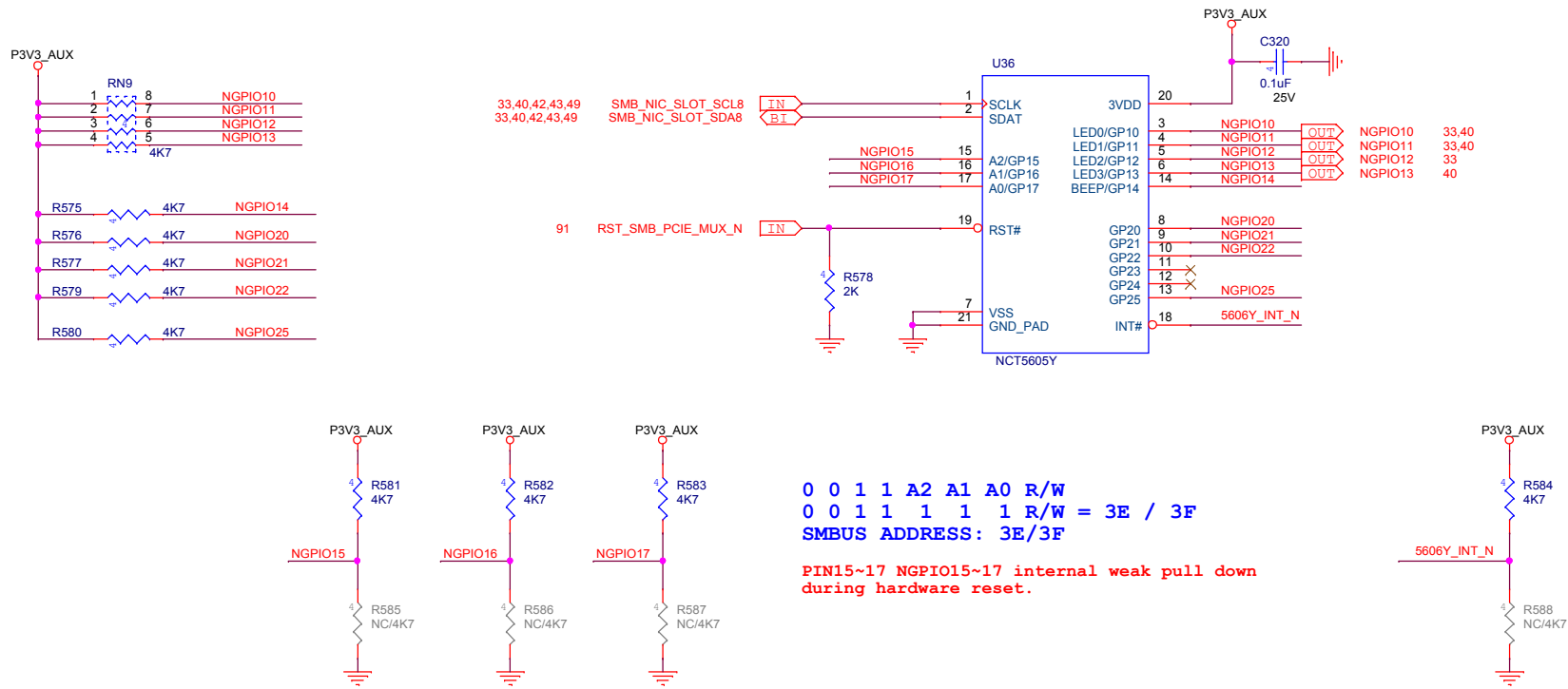
AEWIN Technologies Co., Ltd.			
Title			
EMMC (SOC)			
Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 47 of 92	

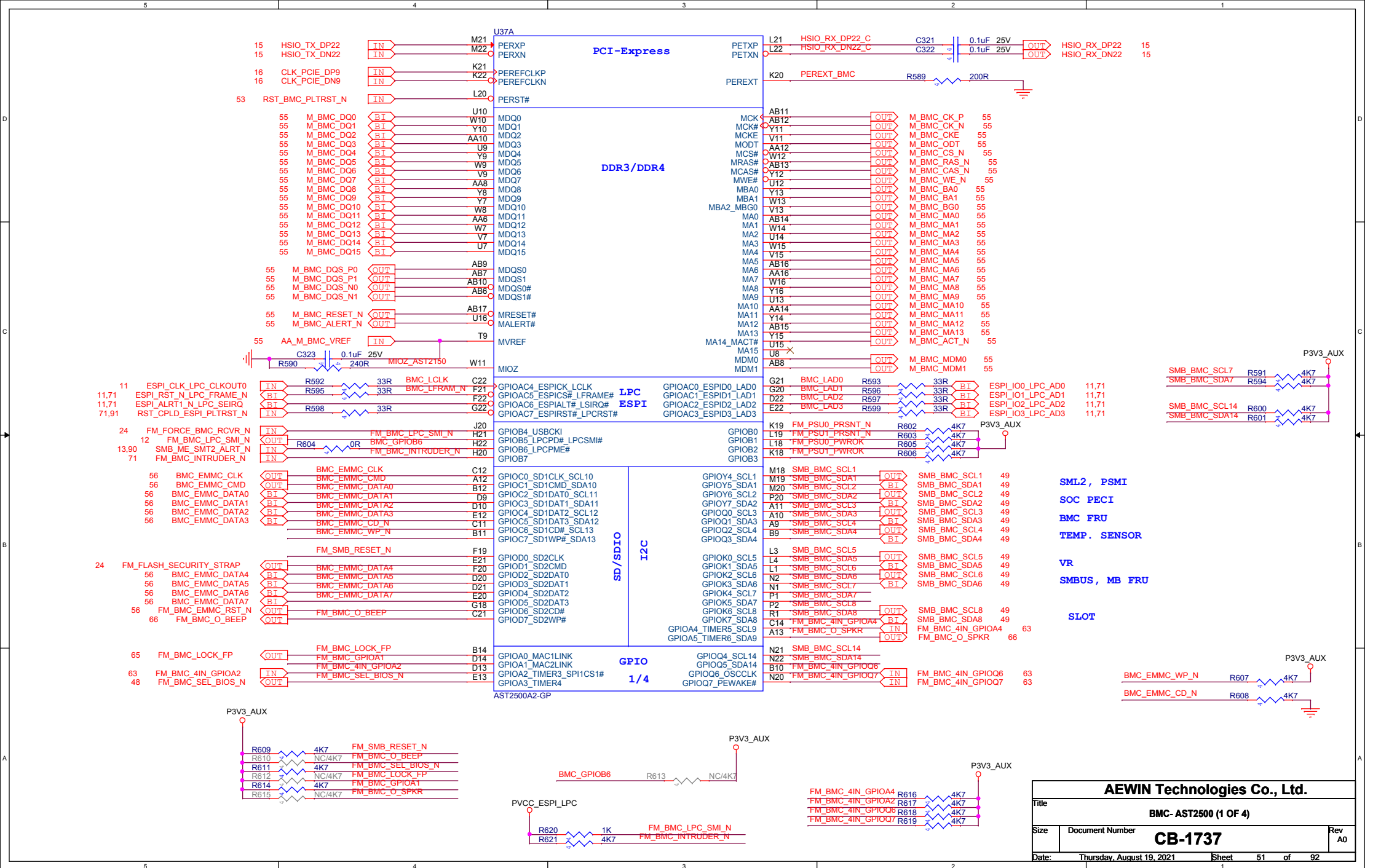


FOR SPI TPM

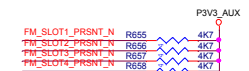
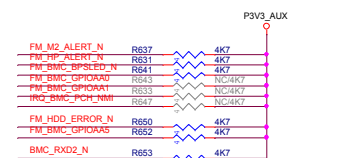
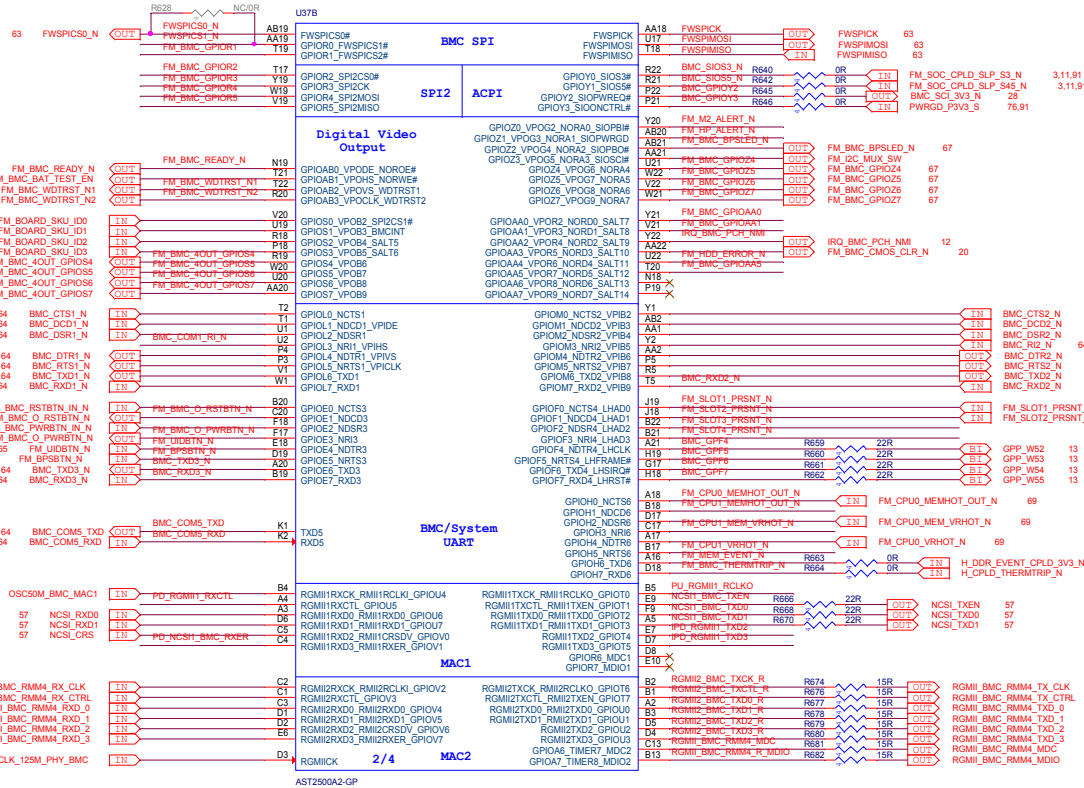
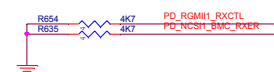


AEWIN Technologies Co., Ltd.			
Title		SMBUS	
Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 49 of 92	

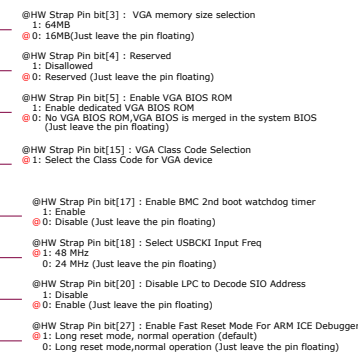
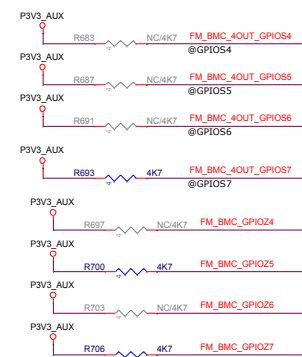
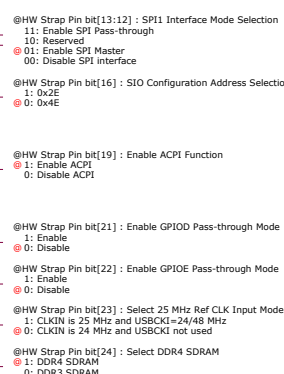
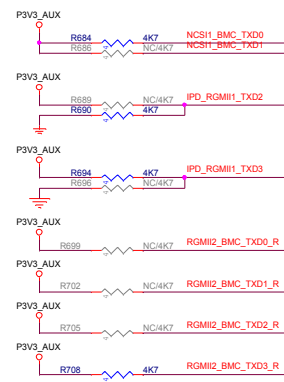
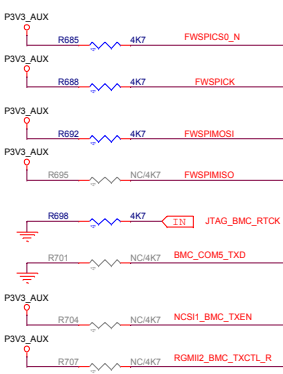
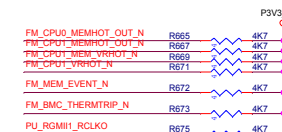


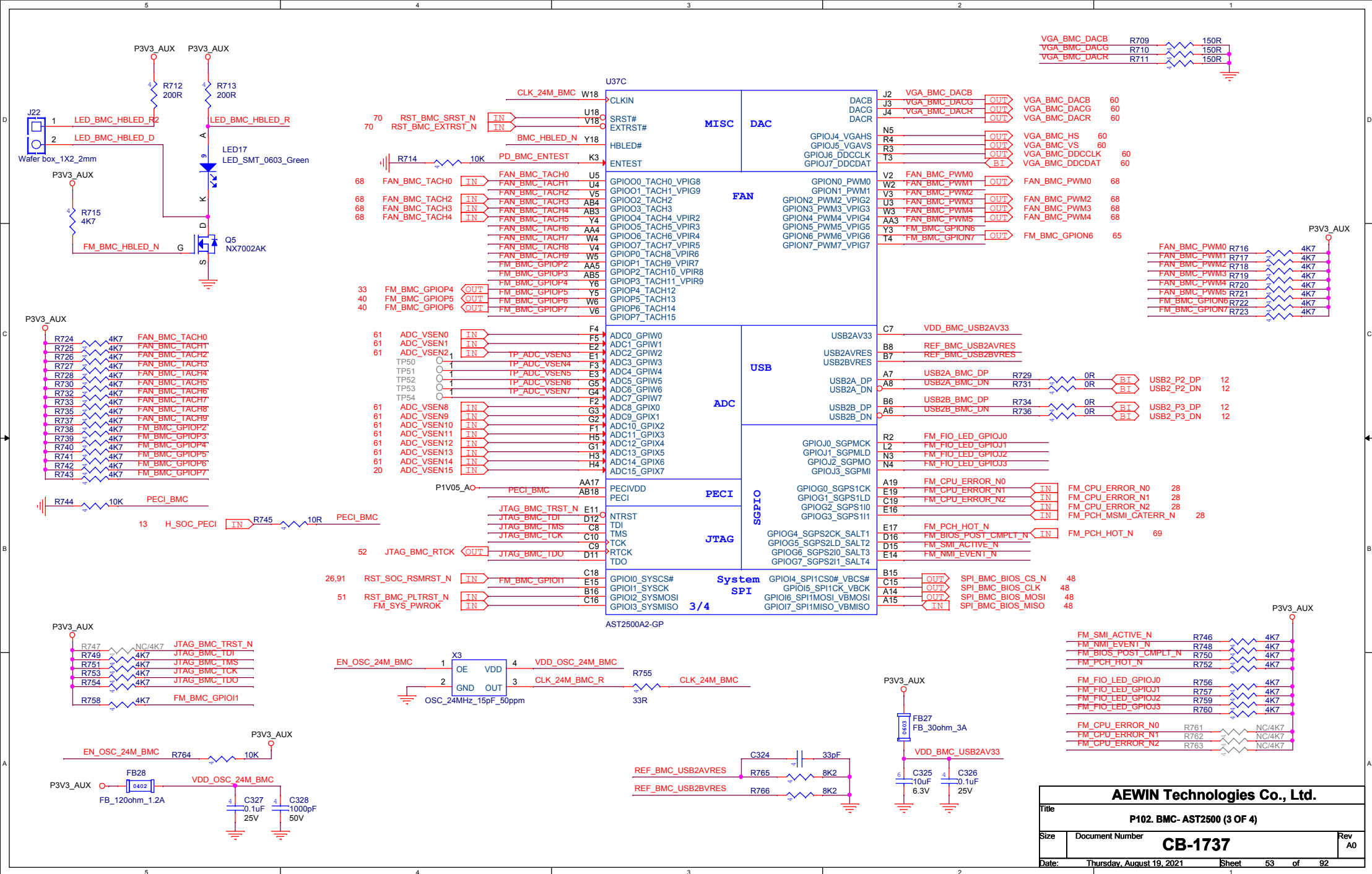


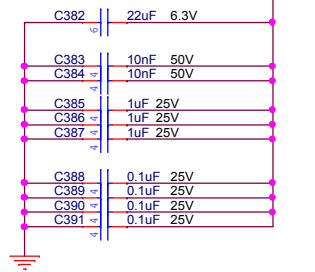
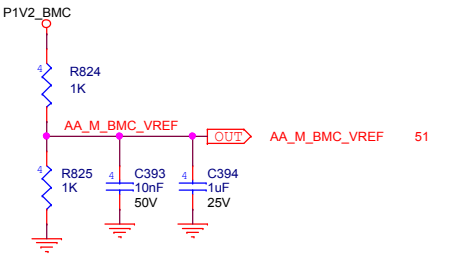
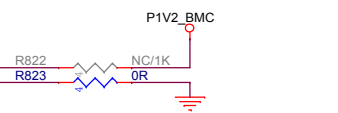
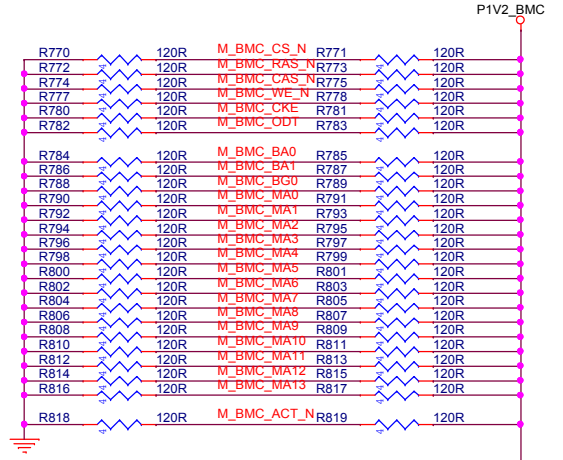
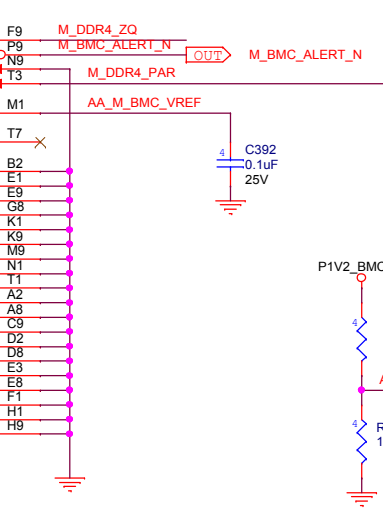
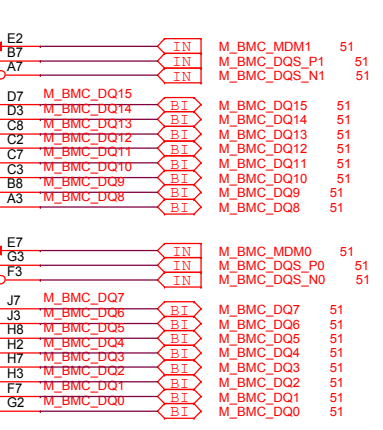
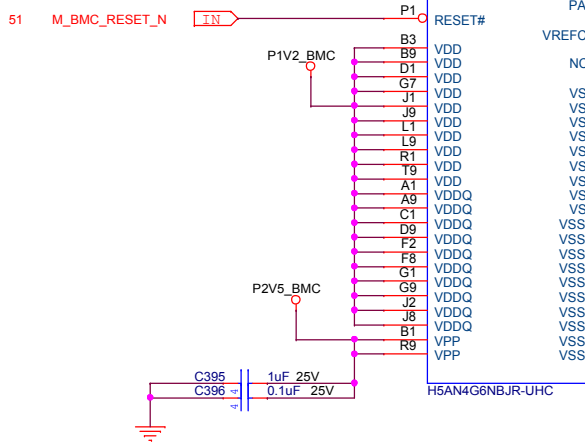
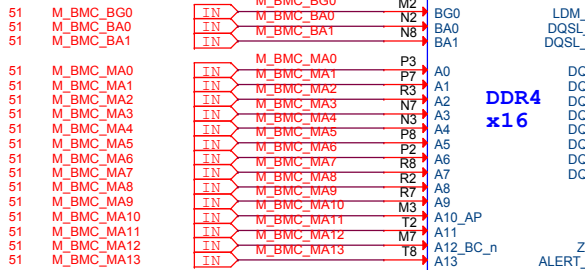
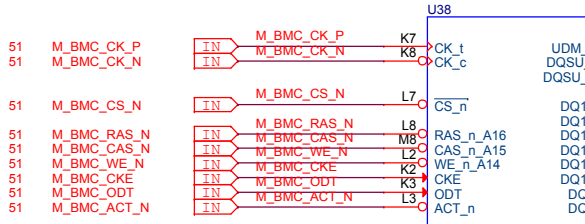
AEWIN Technologies Co., Ltd.			
Title			
BMC- AST2500 (1 OF 4)			
Size	Document Number		Rev
	CB-1737		A0
Date:	Thursday, August 19, 2021	Sheet	51 of 92



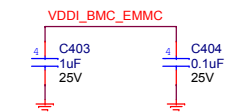
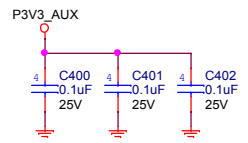
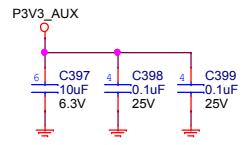
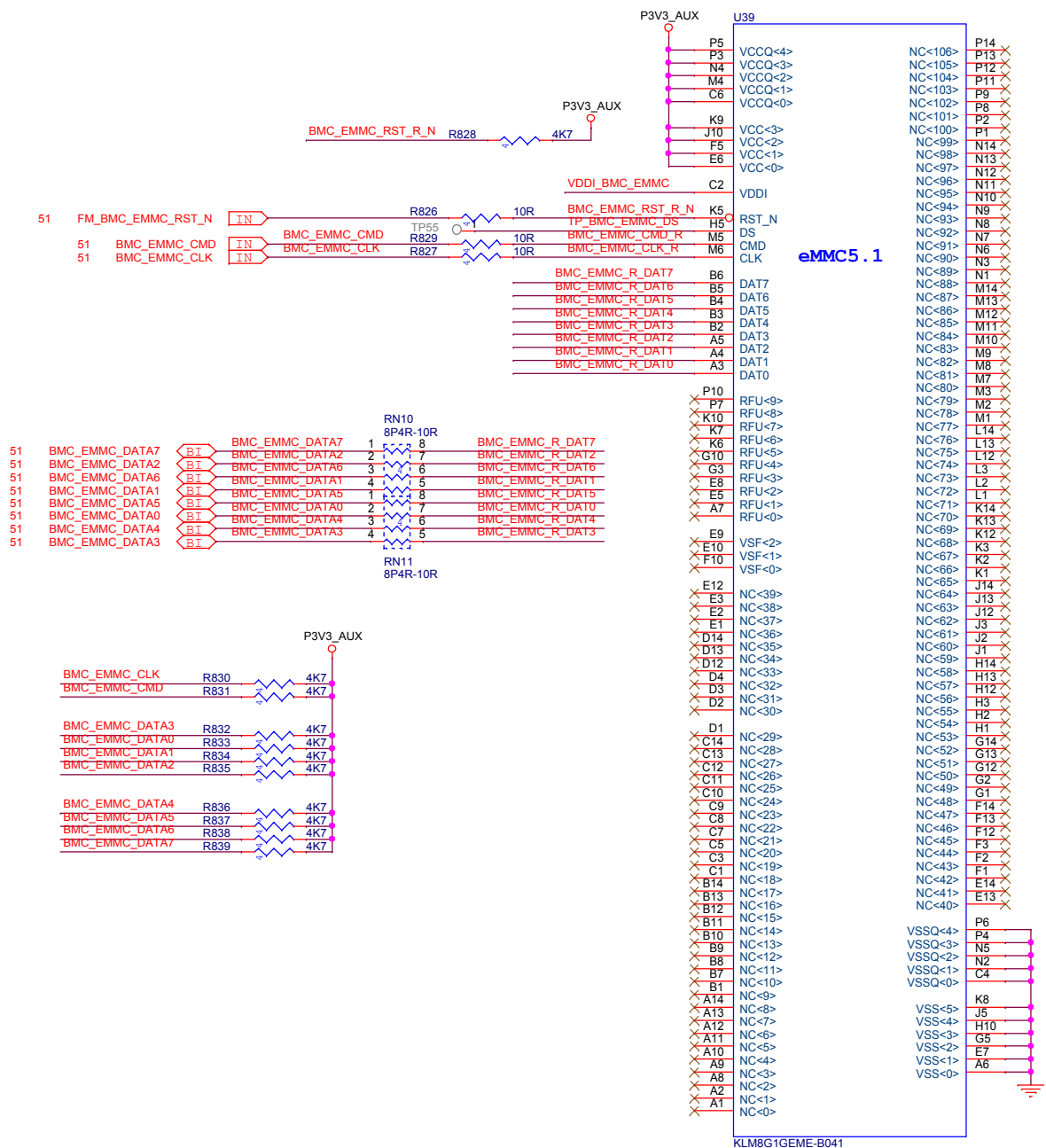
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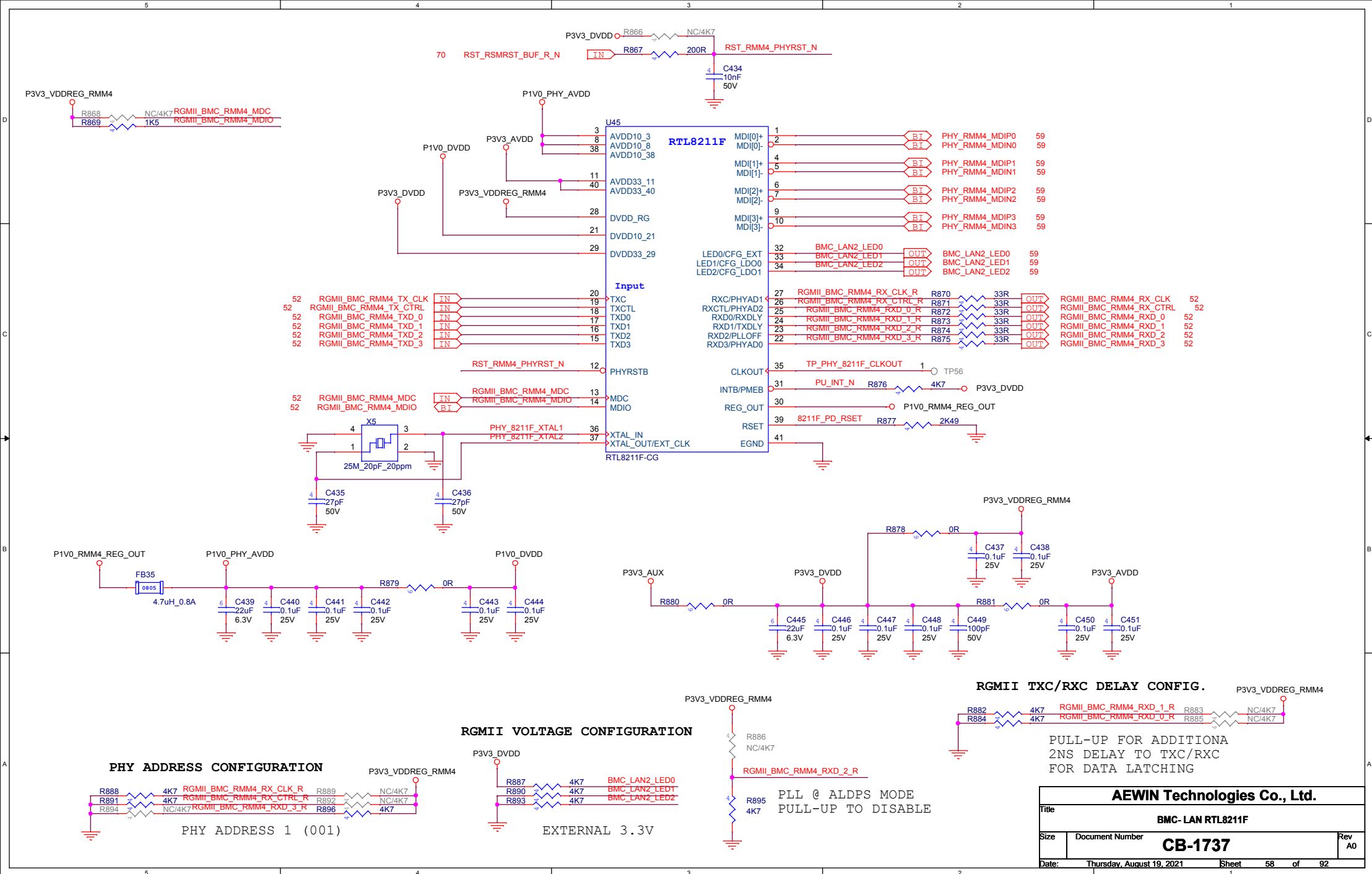


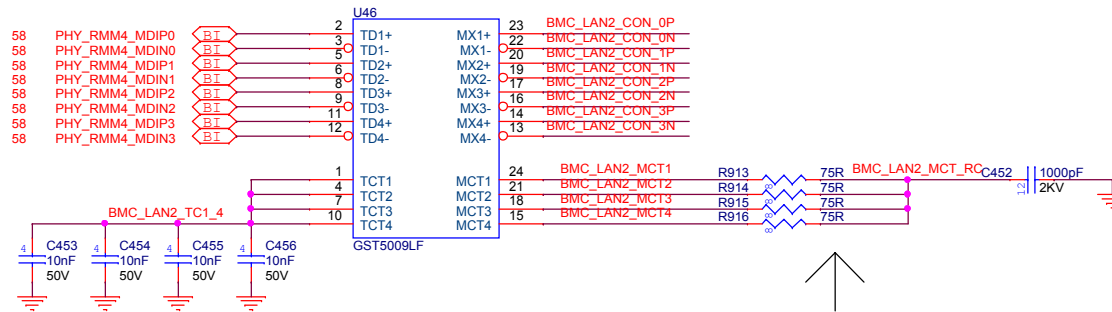
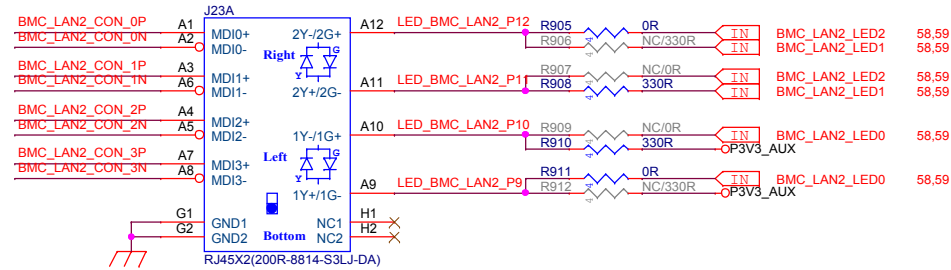
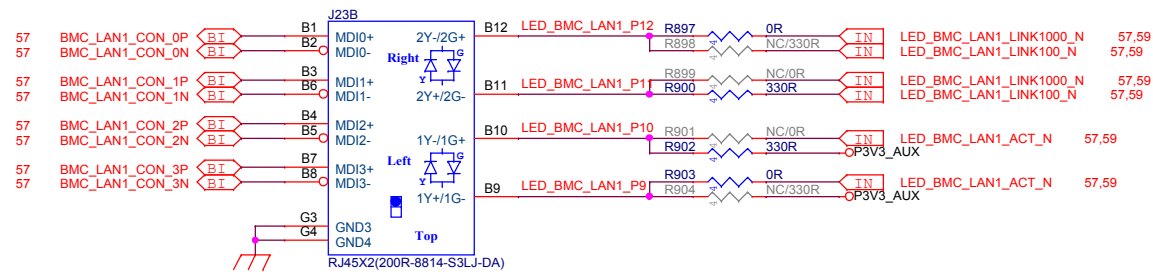


AEWIN Technologies Co., Ltd.				
Title				
BMC-DDR4				
Size	Document Number			Rev
	CB-1737			A0
Date:	Thursday, August 19, 2021		Sheet	55 of 92

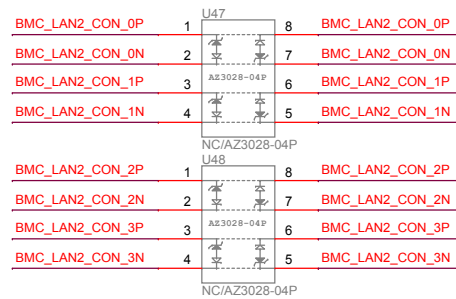


AEWIN Technologies Co., Ltd.			
Title			
BMC-EMMC			
Size	Document Number	Rev	
	CB-1737	A0	
Date:	Thursday, August 19, 2021	Sheet	56 of 92

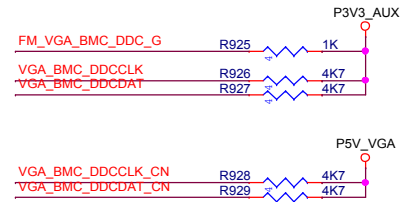
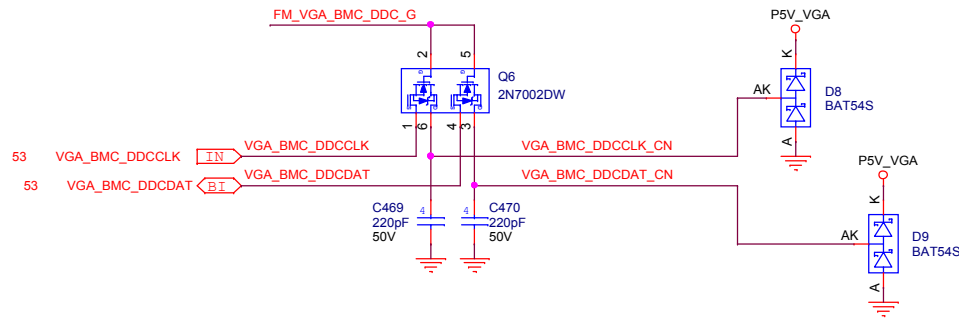
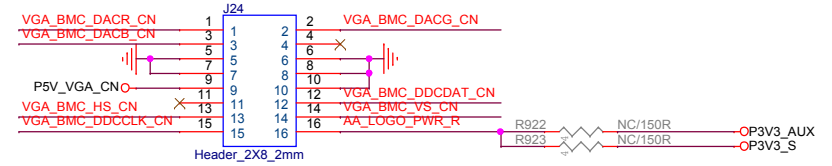
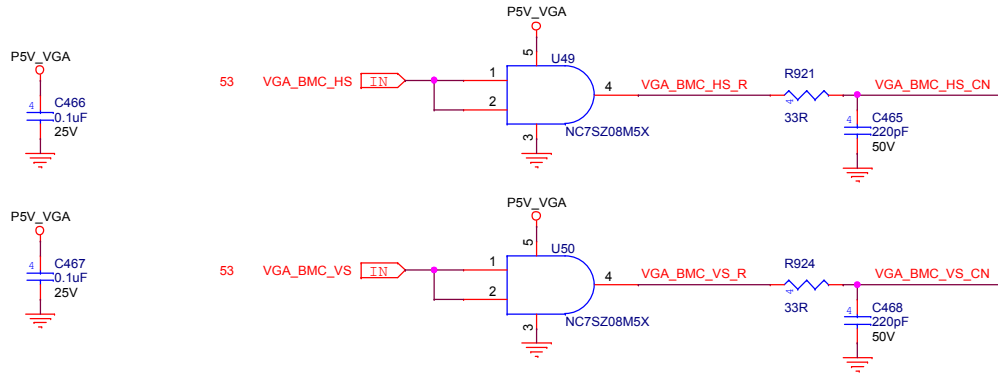
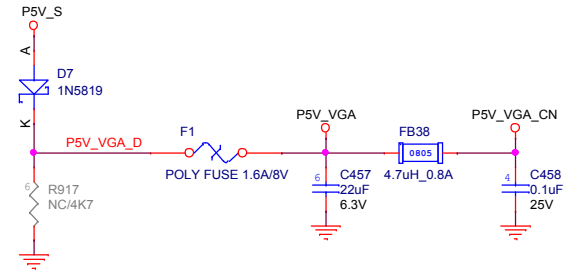
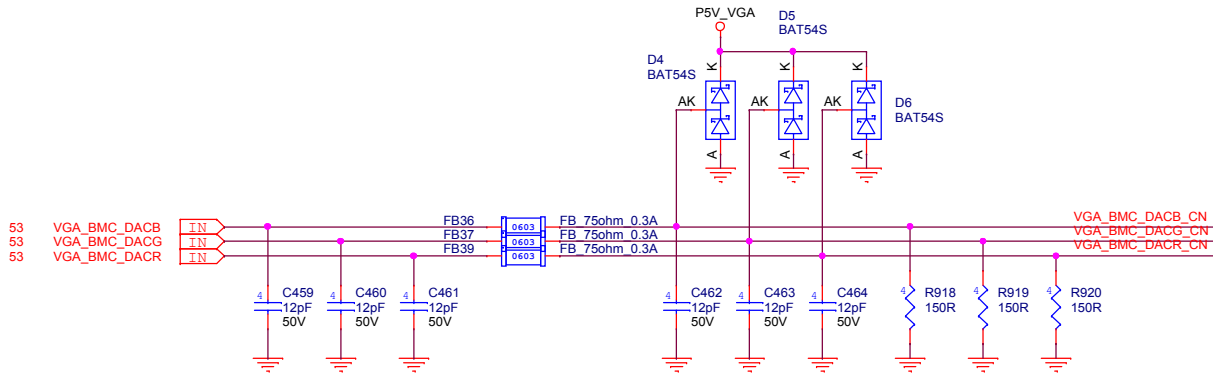




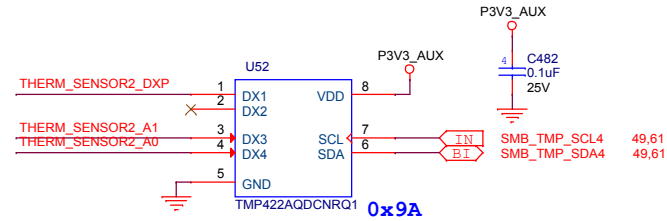
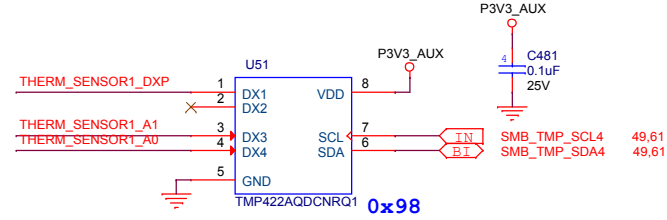
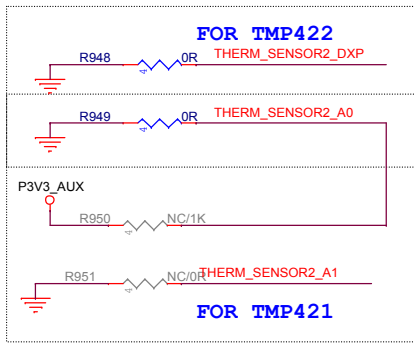
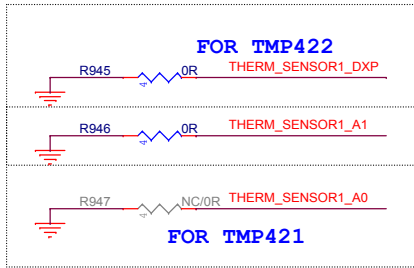
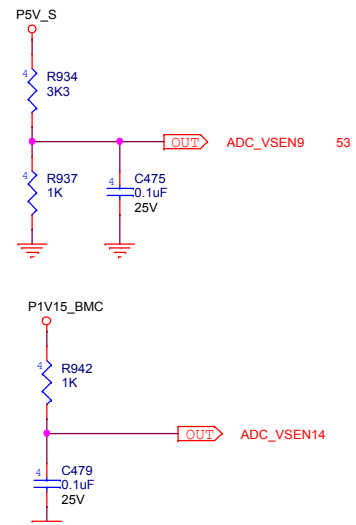
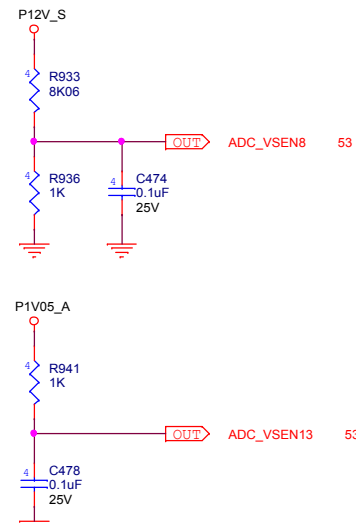
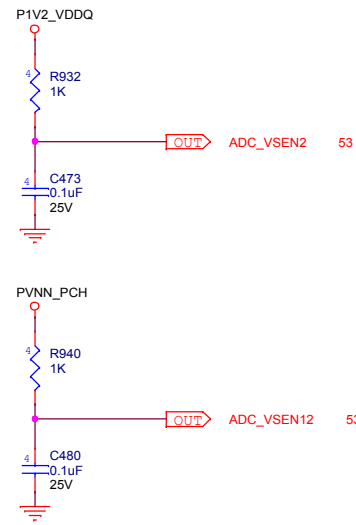
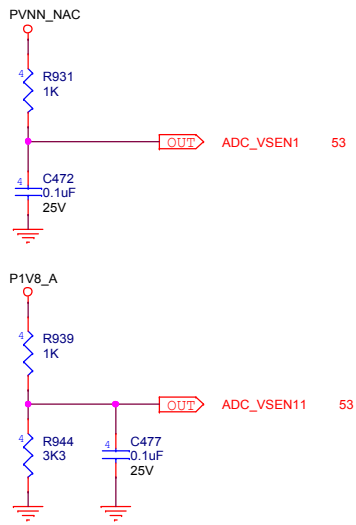
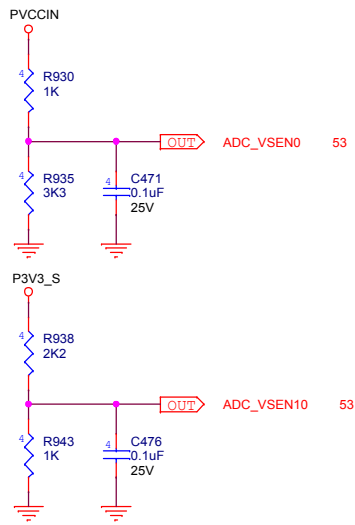
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AEWIN Technologies Co., Ltd.			
Title	XX		
Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 59 of 92	

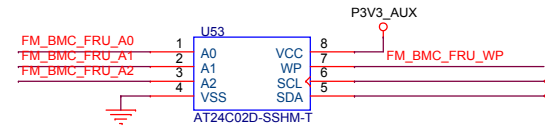
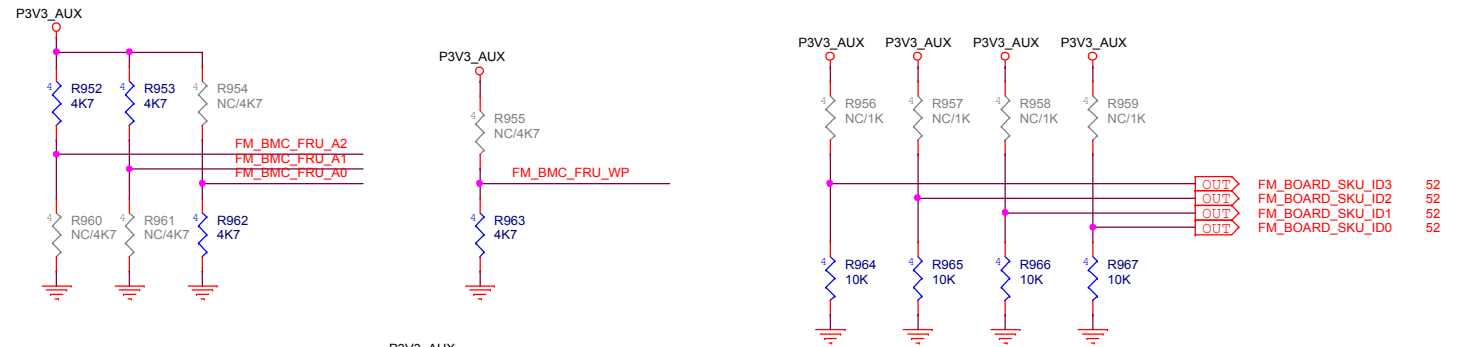


AEWIN Technologies Co., Ltd.			
Title			
BMC- VGA			
Size	Document Number		Rev
	CB-1737		A0
Date:	Thursday, August 19, 2021	Sheet	60 of 92



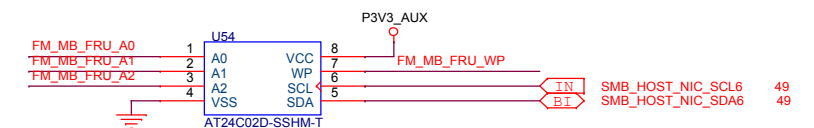
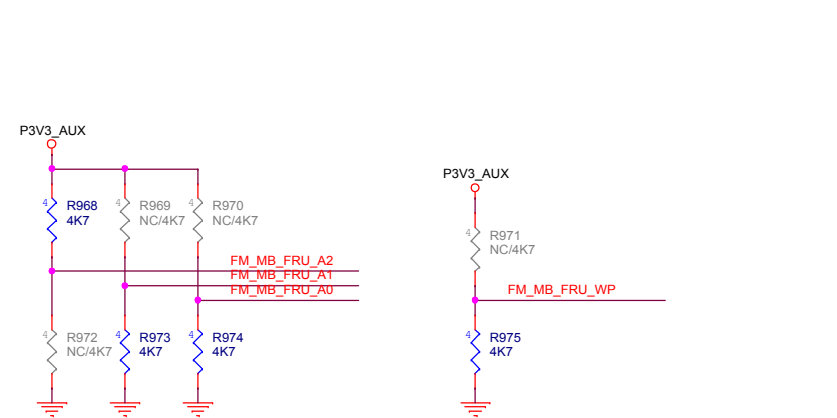
AEWIN Technologies Co., Ltd.			
Title		BMC- HW MONITOR	
Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 61	of 92

BMC FRU.

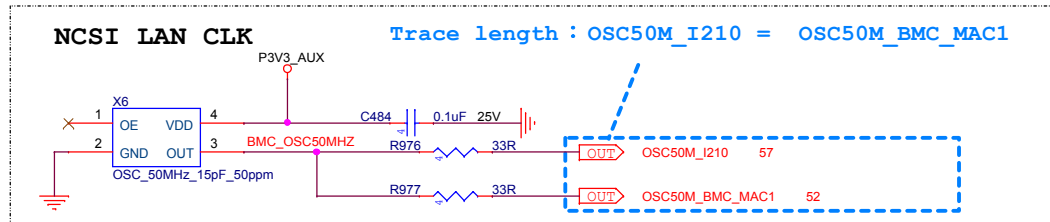
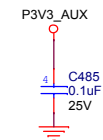


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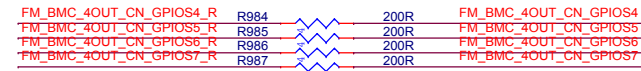
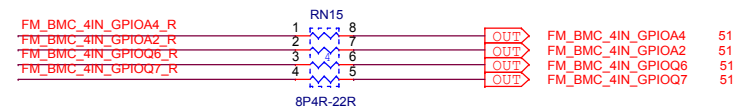
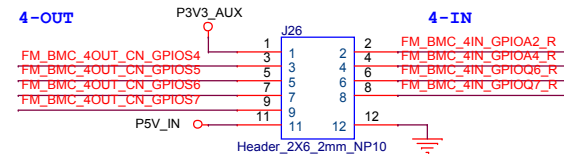
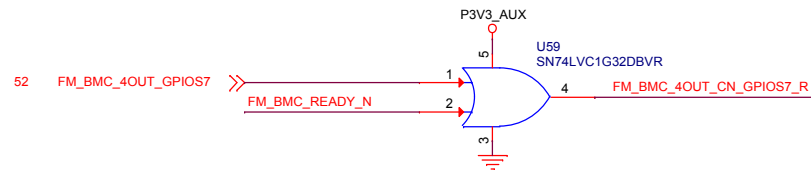
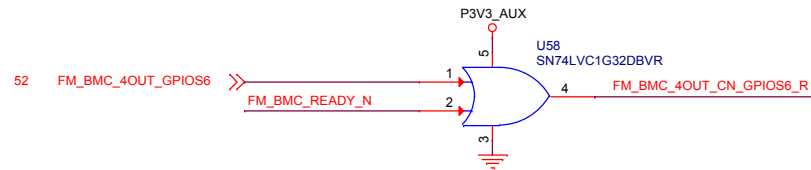
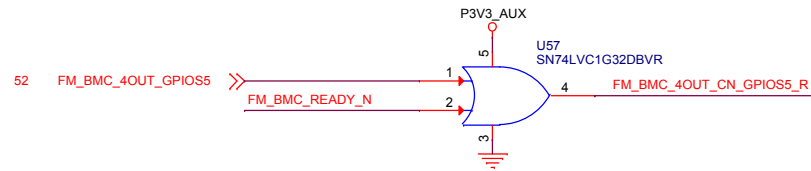
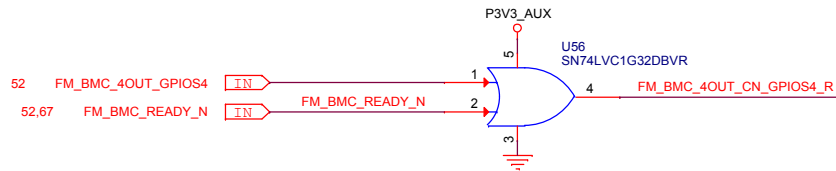
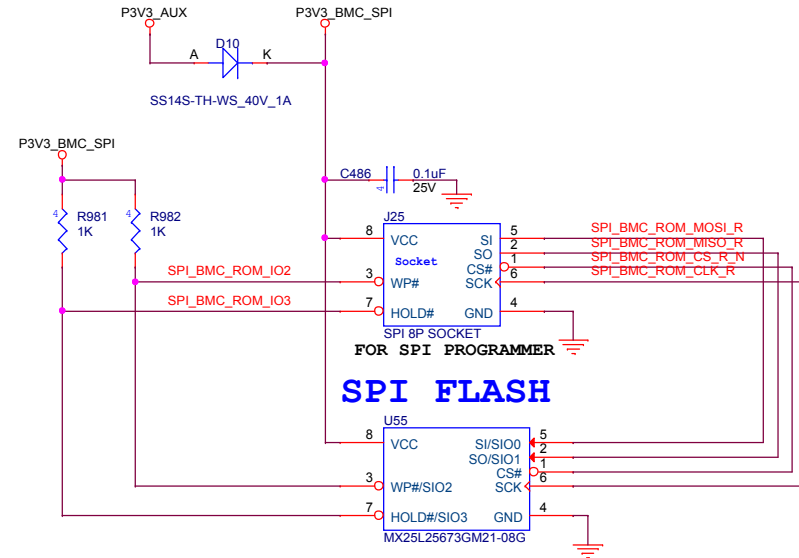
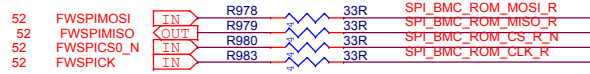
MB FRU.



SMBUS Address: 0XA8

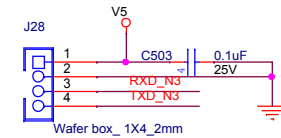
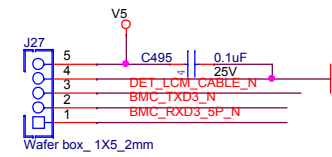
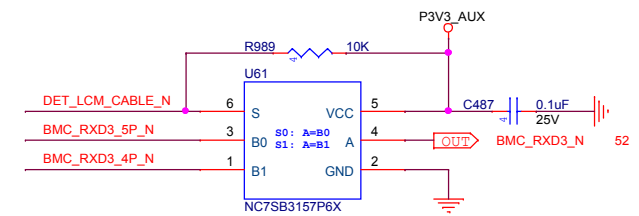
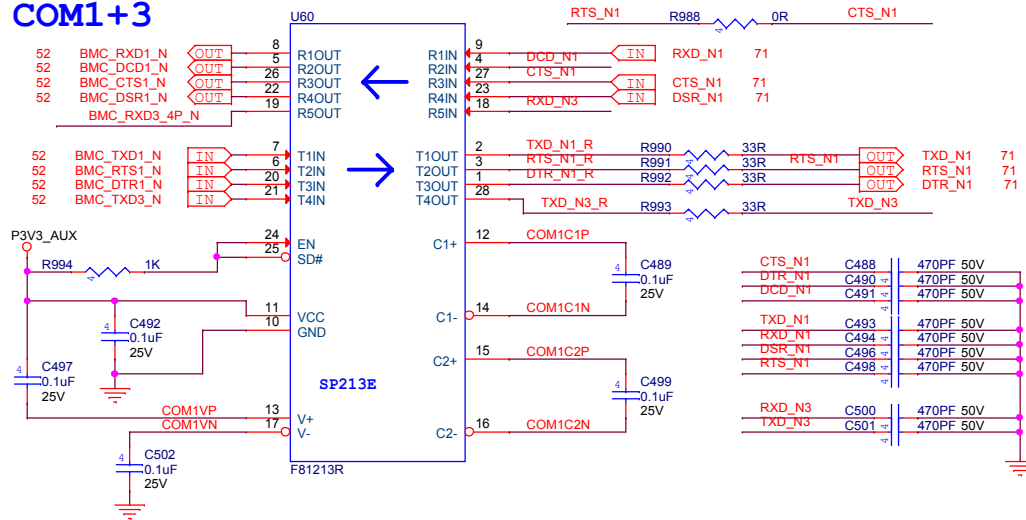


AEWIN Technologies Co., Ltd.			
Title		MB & BMC FRU	
Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 62 of 92	

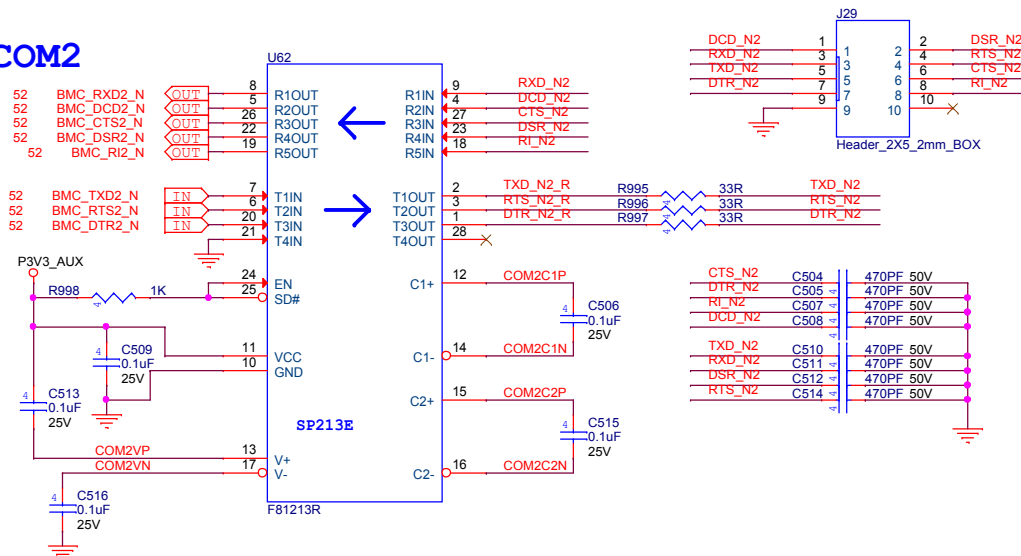


AEWIN Technologies Co., Ltd.			
Title		BMC- SPI & GPIO	
Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 63	of 92

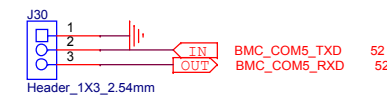
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COM2

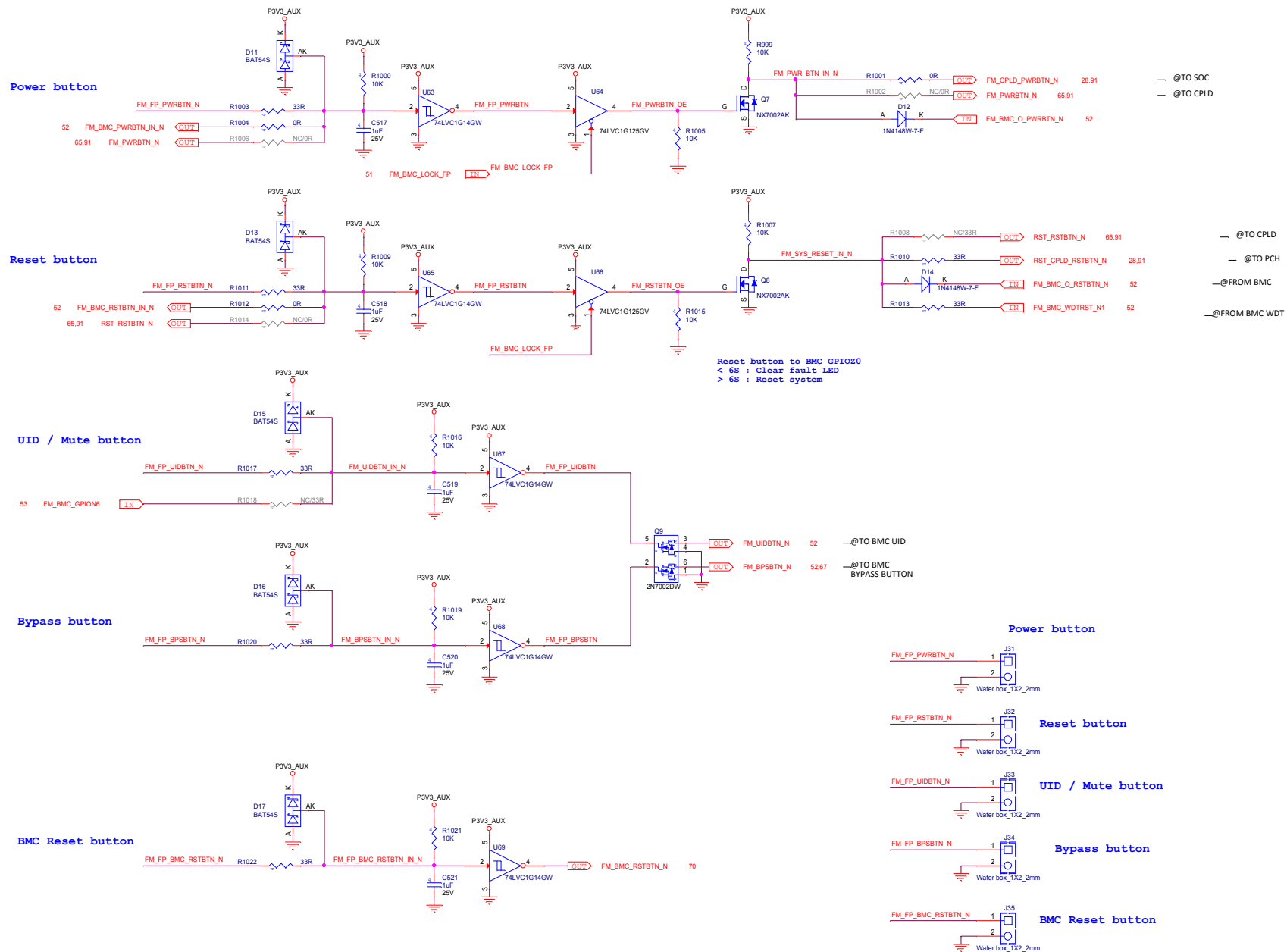


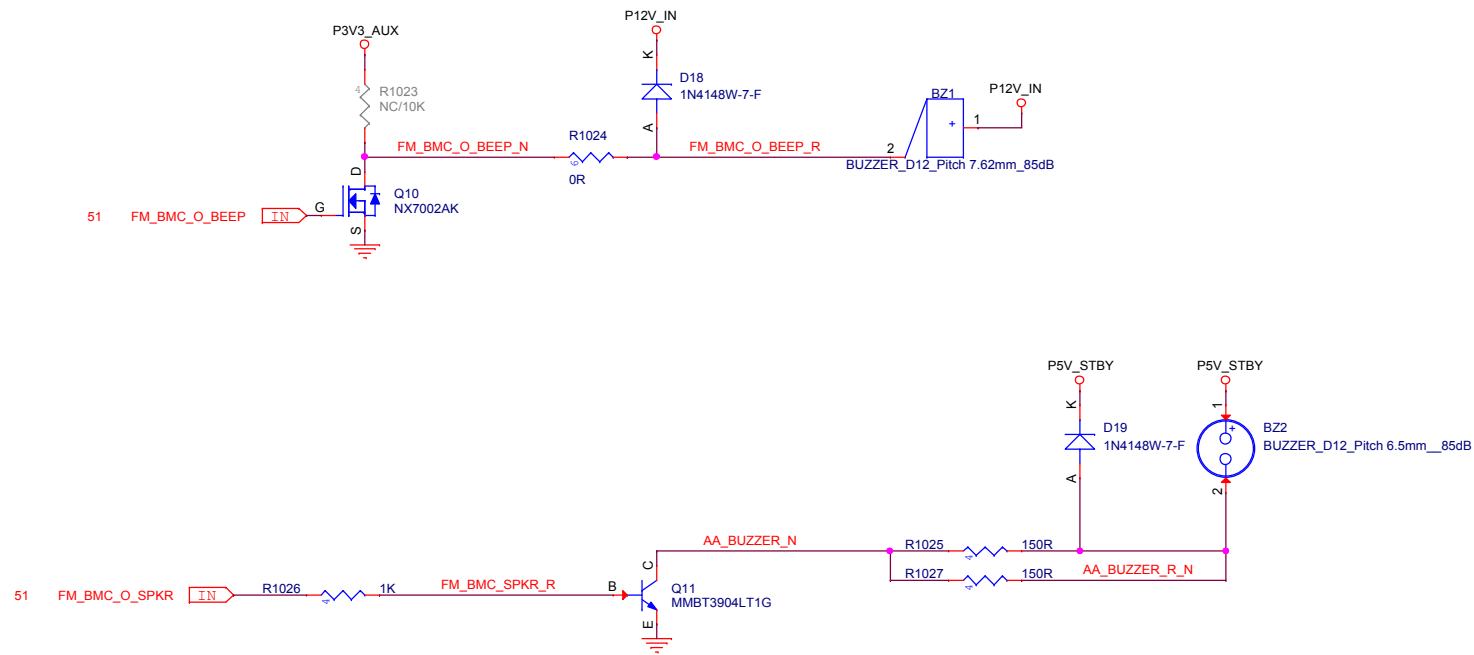
BMC debug port



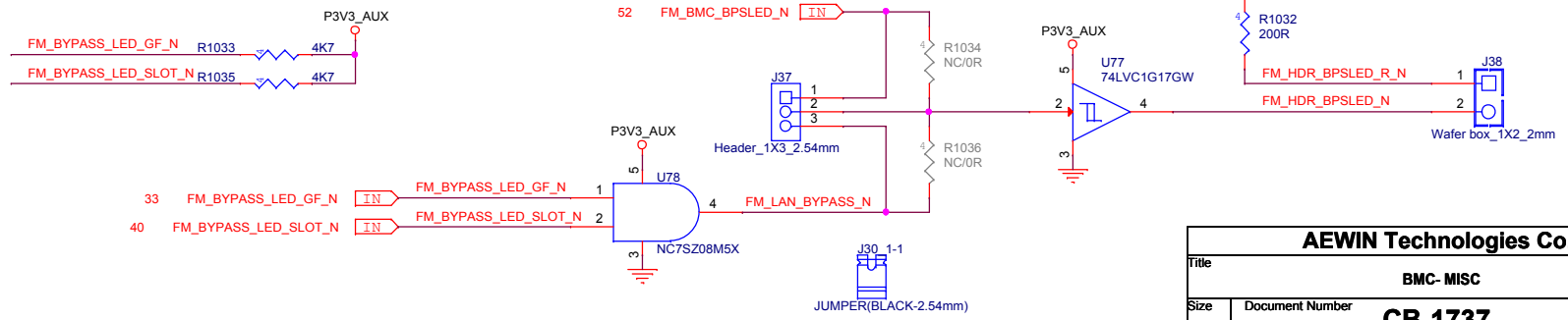
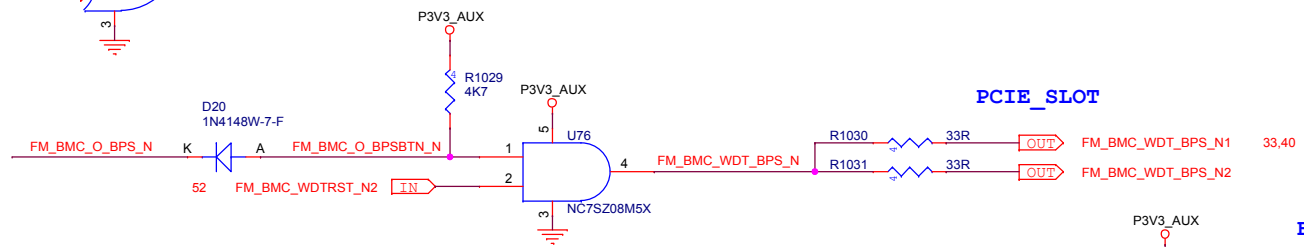
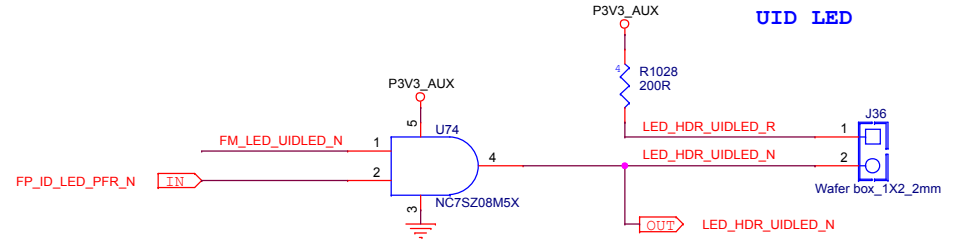
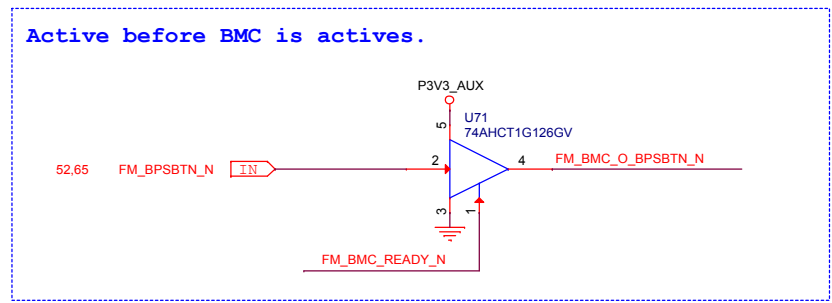
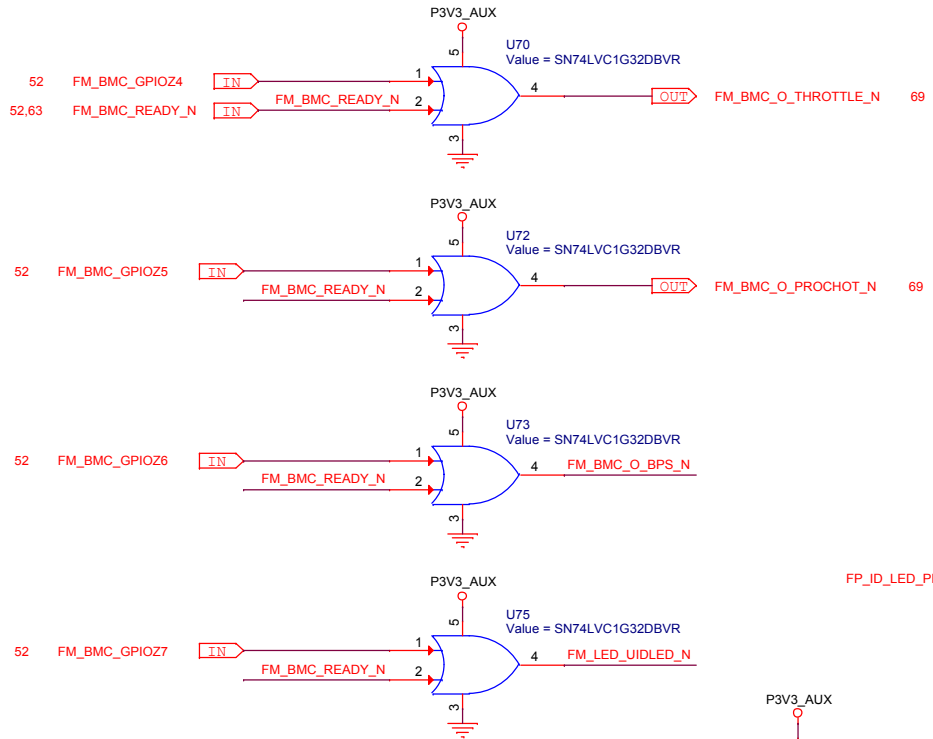
AEWIN Technologies Co., Ltd.

Title			BMC-COM	
Size	Document Number		CB-1737	
Date:	Thursday, August 19, 2021		Sheet	64 of 92
		Rev		A0



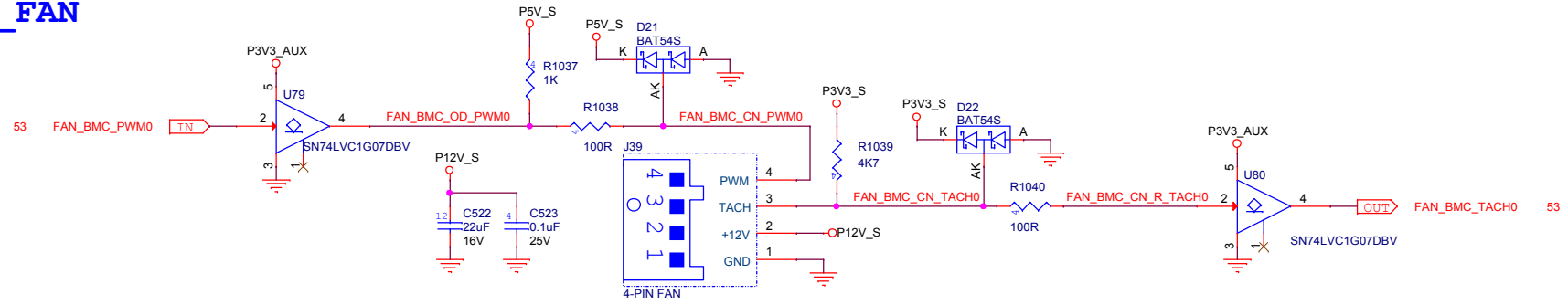


AEWIN Technologies Co., Ltd.			
Title		XX	
Size	Document Number		Rev
	CB-1737		A0
Date:	Thursday, August 19, 2021		Sheet 66 of 92

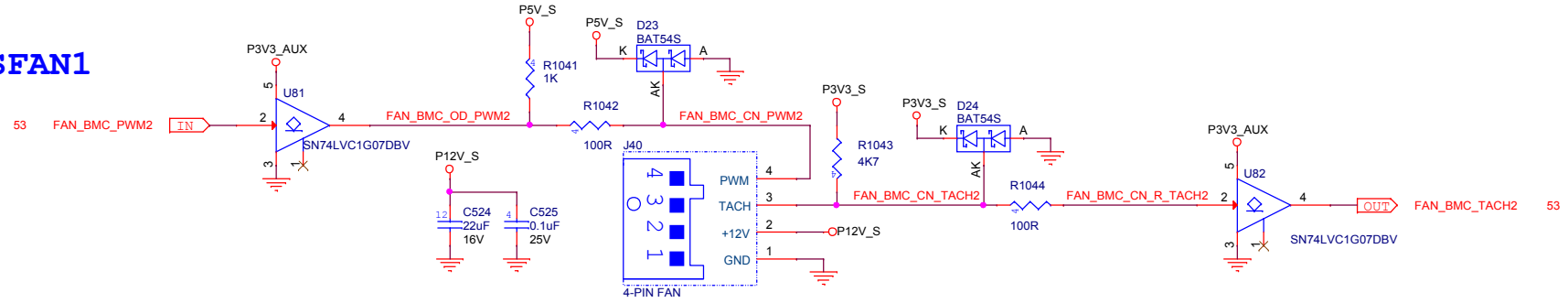


AEWIN Technologies Co., Ltd.			
Title		BMC- MISC	
Size	Document Number	CB-1737	
Date:	Thursday, August 19, 2021	Sheet	67 of 92

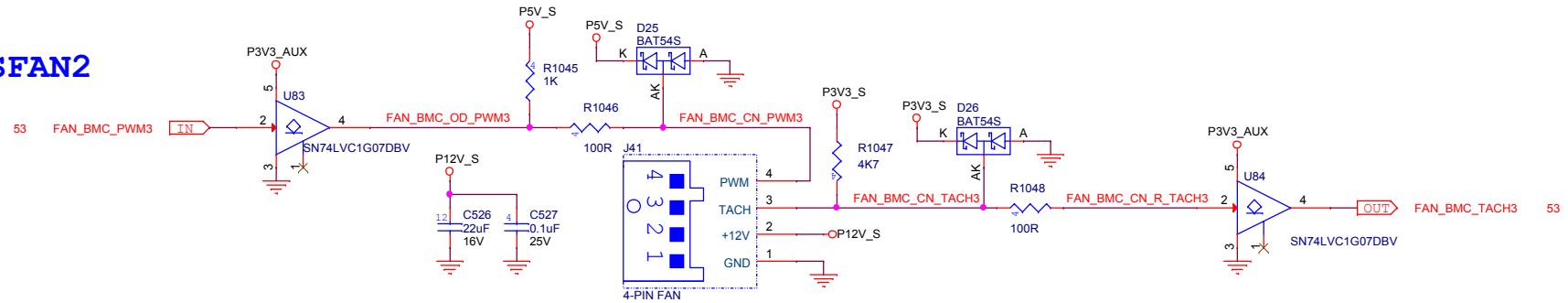
CPU_FAN



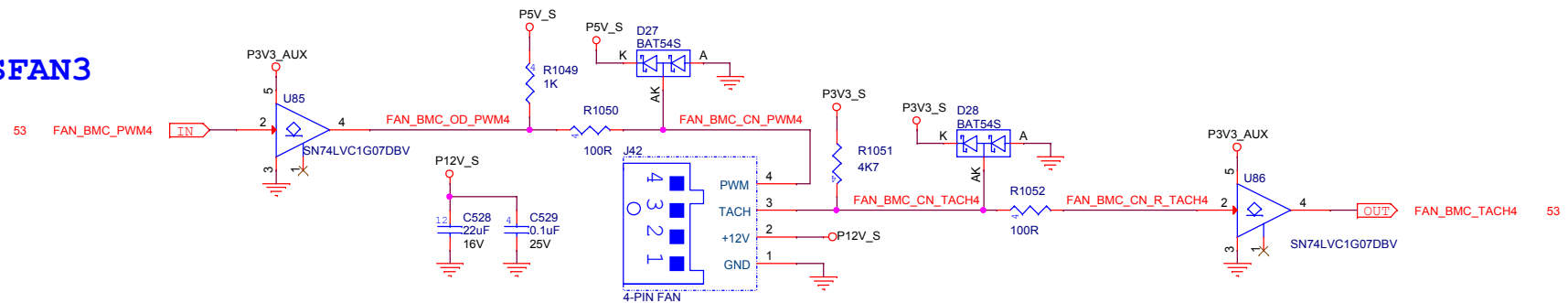
SYSFAN1



SYSFAN2

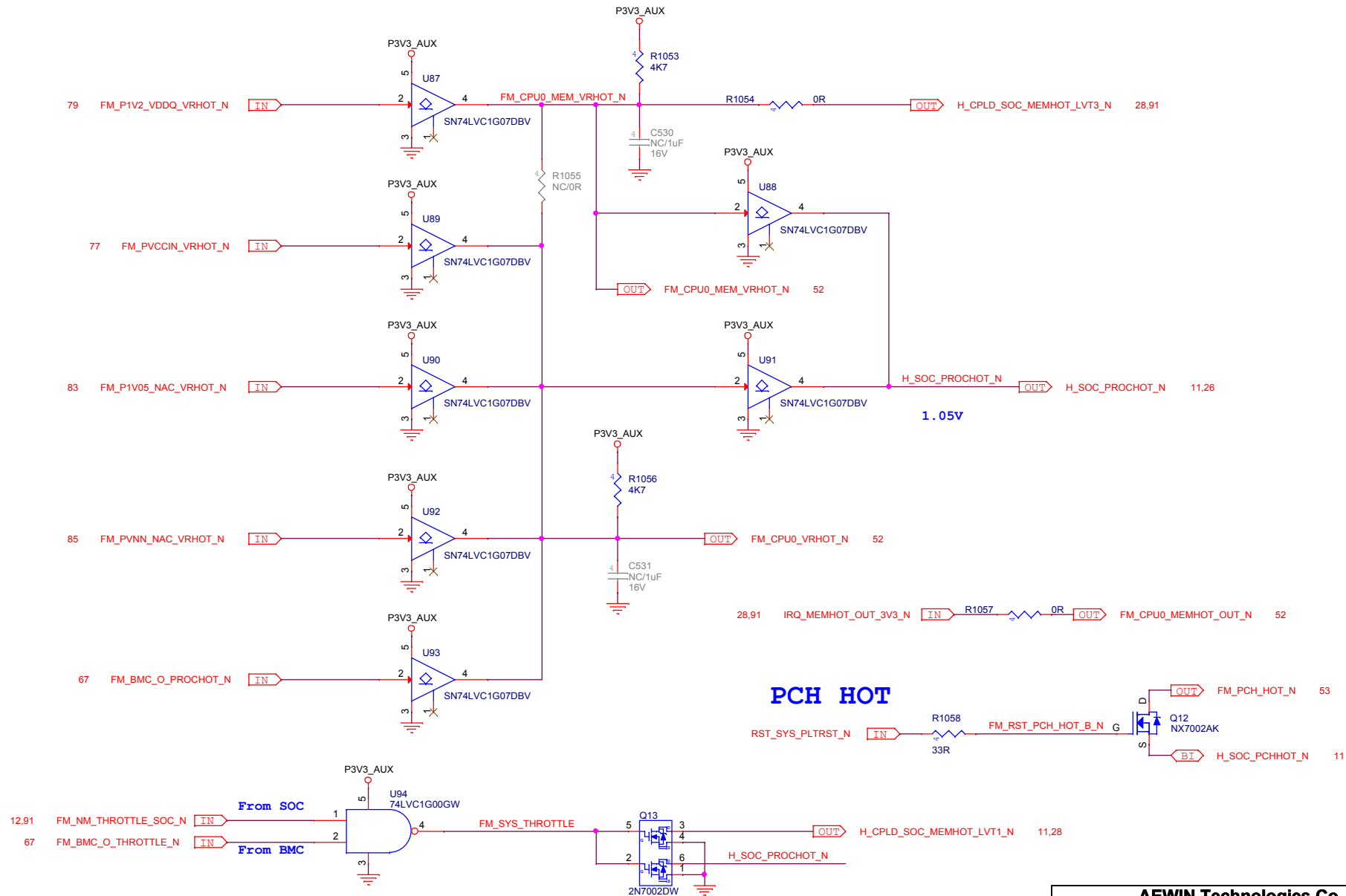


SYSFAN3



AEWIN Technologies Co., Ltd.

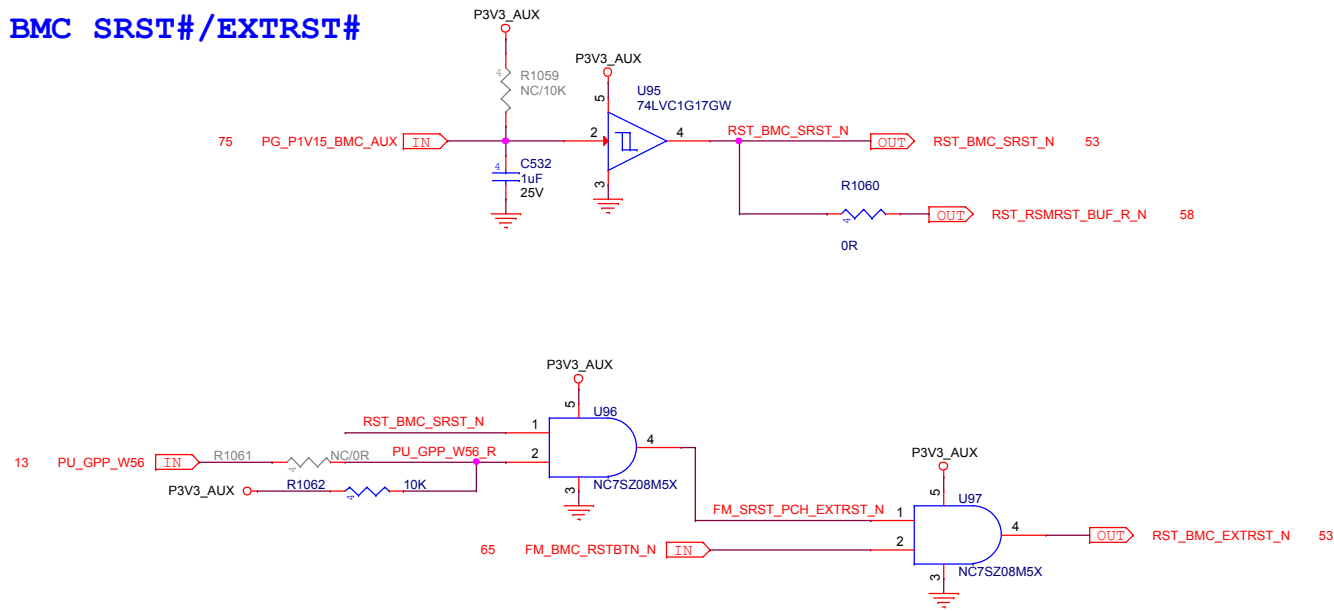
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Size	Document Number	Rev
	CB-1737	A0
Date:	Thursday, August 19, 2021	Sheet 68 of 92



AEWIN Technologies Co., Ltd.

Title			BMC_VRHOT	
Size	Document Number		CB-1737	
Date:		Thursday, August 19, 2021	Sheet	69 of 92
				Rev A0

BMC SRST#/EXTRST#



AEWIN Technologies Co., Ltd.

Title

BMC-RESET

Size

Document Number

CB-1737

Rev

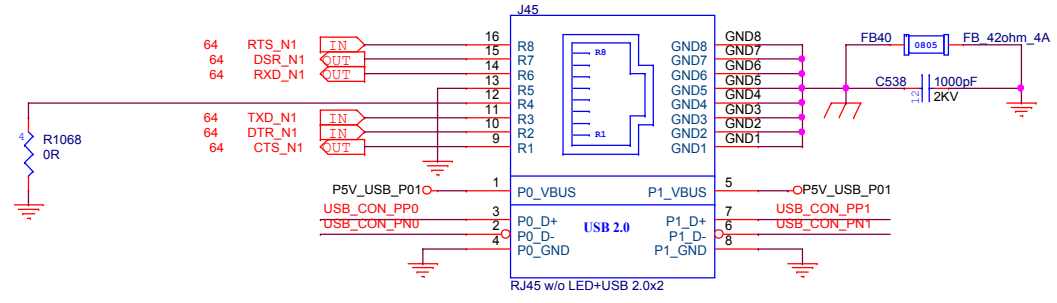
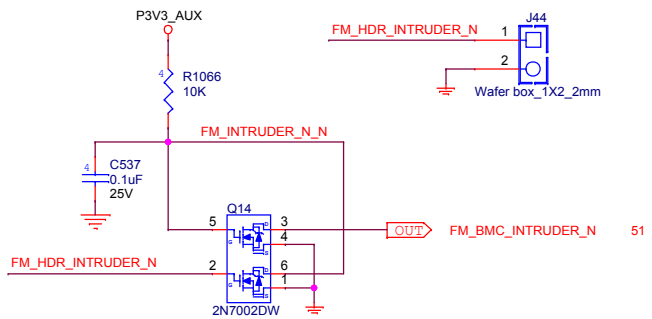
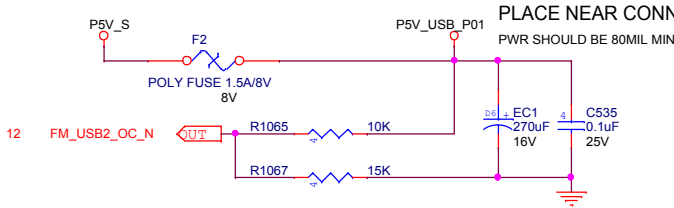
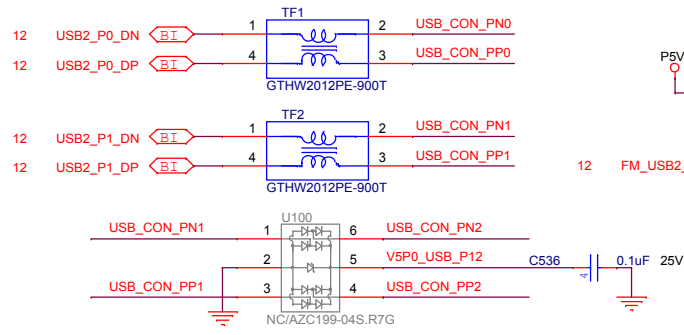
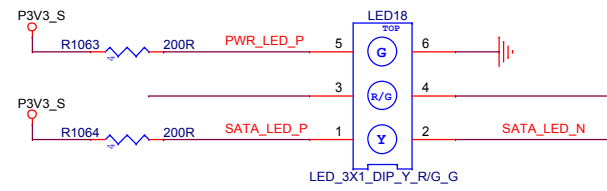
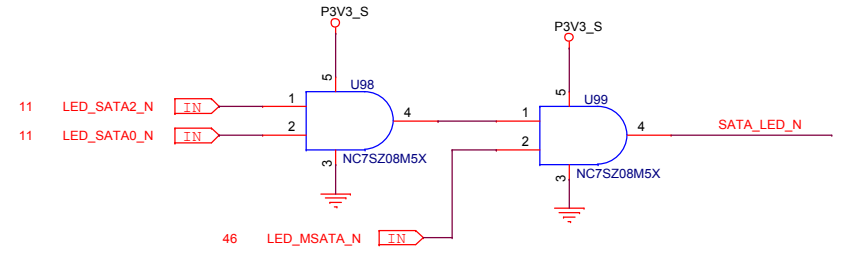
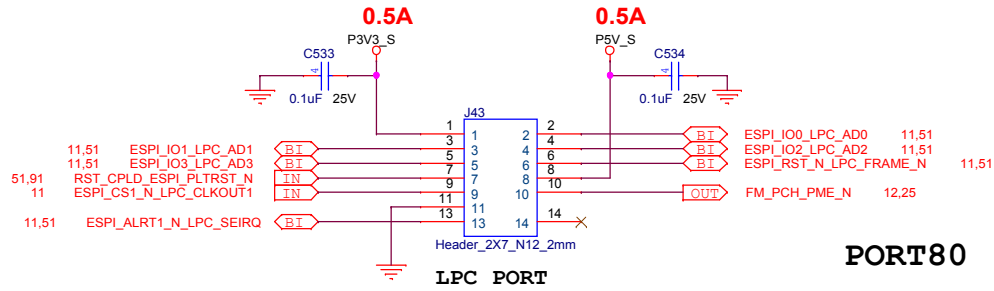
A0

Date:

Thursday, August 19, 2021

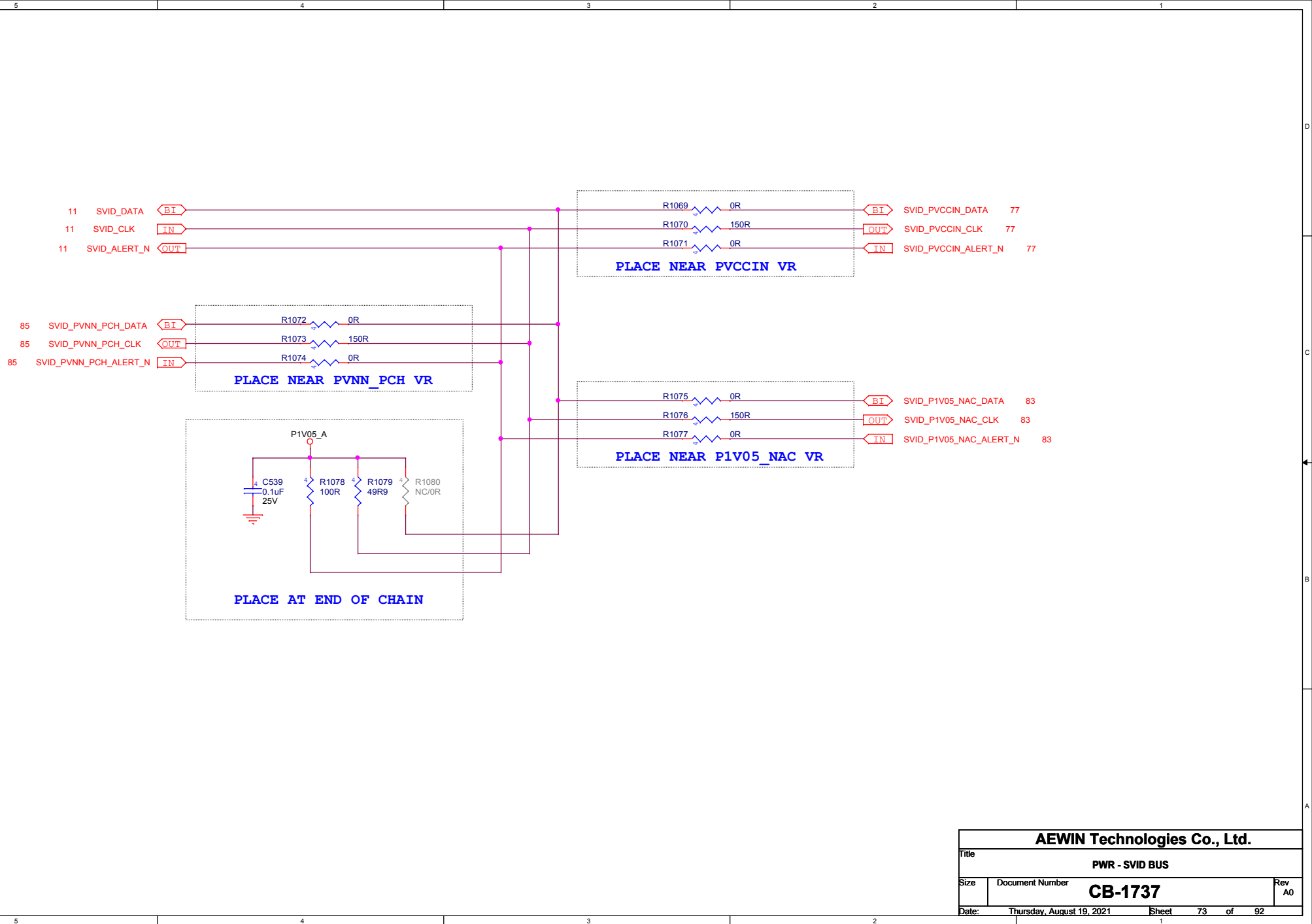
Sheet

70 of 92



AEWIN Technologies Co., Ltd.			
Title	XX		
Size	Document Number	Rev A0	
Date:	Thursday, August 19, 2021	Sheet	71 of 92

AEWIN Technologies Co., Ltd.			
Title			
XX			
Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 72 of 92	



AEWIN Technologies Co., Ltd.			
Title		PWR - SVID BUS	
Size	Document Number	Rev	A0
Date: Thursday, August 19, 2021		Sheet	73 of 92

APL5934:

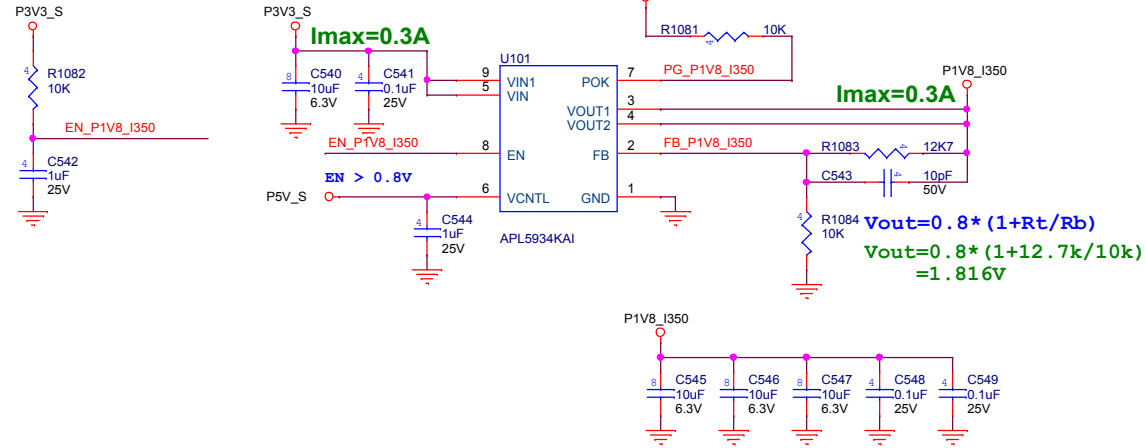
Vin:1.2V ~ 3.65V; Iout:3A

EN High Threshold:1.1V

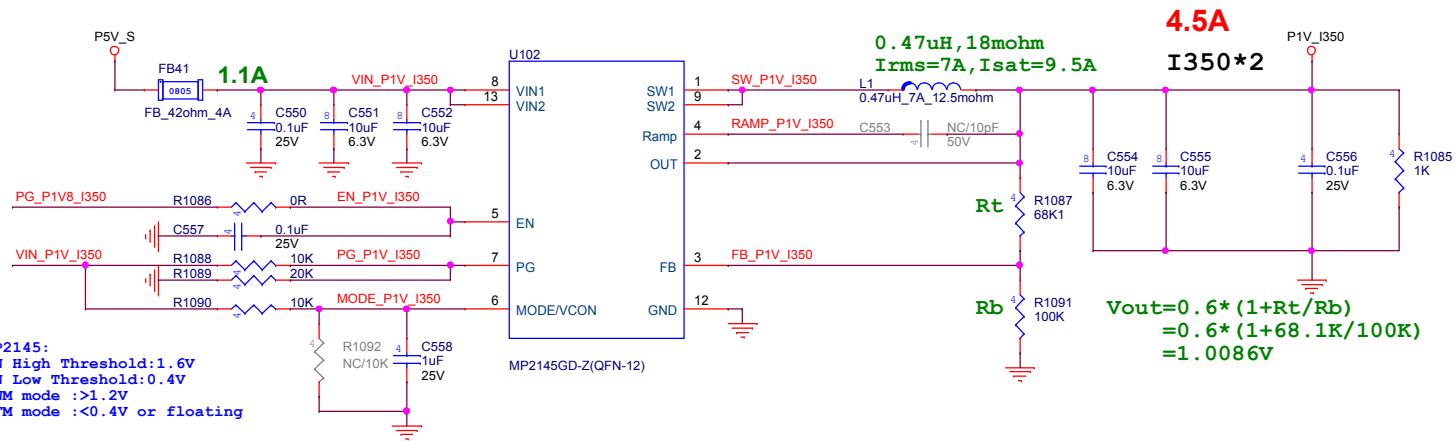
EN Low Threshold:0.5V

EN internal pull-up VCNTL
current (5uA typical)

VCNTL-V_OUT>1.9V



MP2145:
EN High Threshold:1.6V
EN Low Threshold:0.4V
PWM mode :>1.2V
PFM mode :<0.4V or floating



AEWIN Technologies Co., Ltd.

Title	XX		
Size	Document Number	CB-1737	
Date:	Thursday, August 19, 2021	Sheet	74 of 92

Rev A0

GS7133 3A LDO POWER

Power Rail : V2P5_BMC_AUX

VIN : 3.3V

Vout : 2.5V

IOU TDC : 0.3A

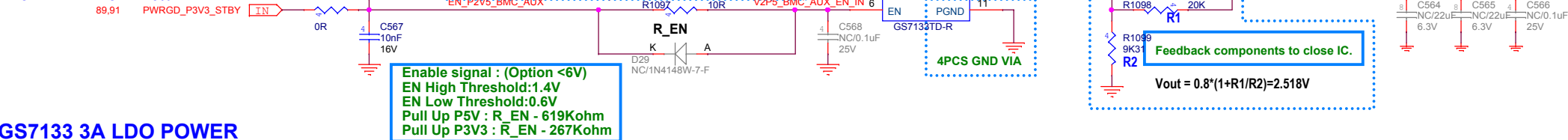
IOU PEAK : 0.5A

IOU OCP : 5.5A

DC TOL : $\pm 1.5\%$

RIPPLE : $\pm 1.0\%$

DC+RIPPLE+AC : $\pm 4.5\%$



GS7133 3A LDO POWER

Power Rail : V1P2_BMC_AUX

VIN : 1.8V

Vout : 1.2V

IOU TDC : 0.6A

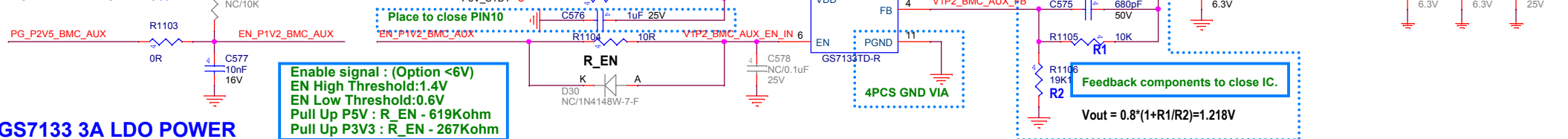
IOU PEAK : 0.75A

IOU OCP : 5.5A

DC TOL : $\pm 3.0\%$

RIPPLE : $\pm 0.5\%$

DC+RIPPLE+AC : $\pm 4.5\%$



GS7133 3A LDO POWER

Power Rail : V1P15_BMC_AUX

VIN : 1.8V

Vout : 1.15V

IOU TDC : 0.9A

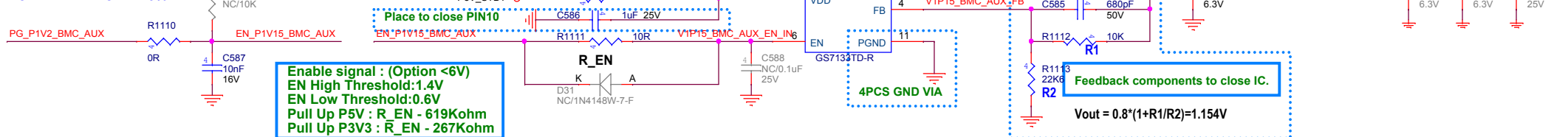
IOU PEAK : 1.2A

IOU OCP : 5.5A

DC TOL : $\pm 3.0\%$

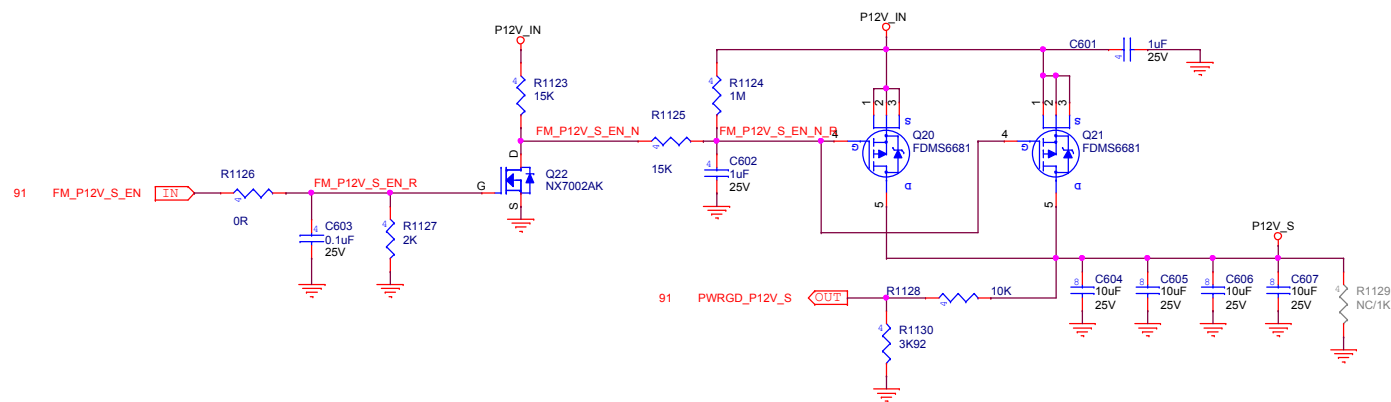
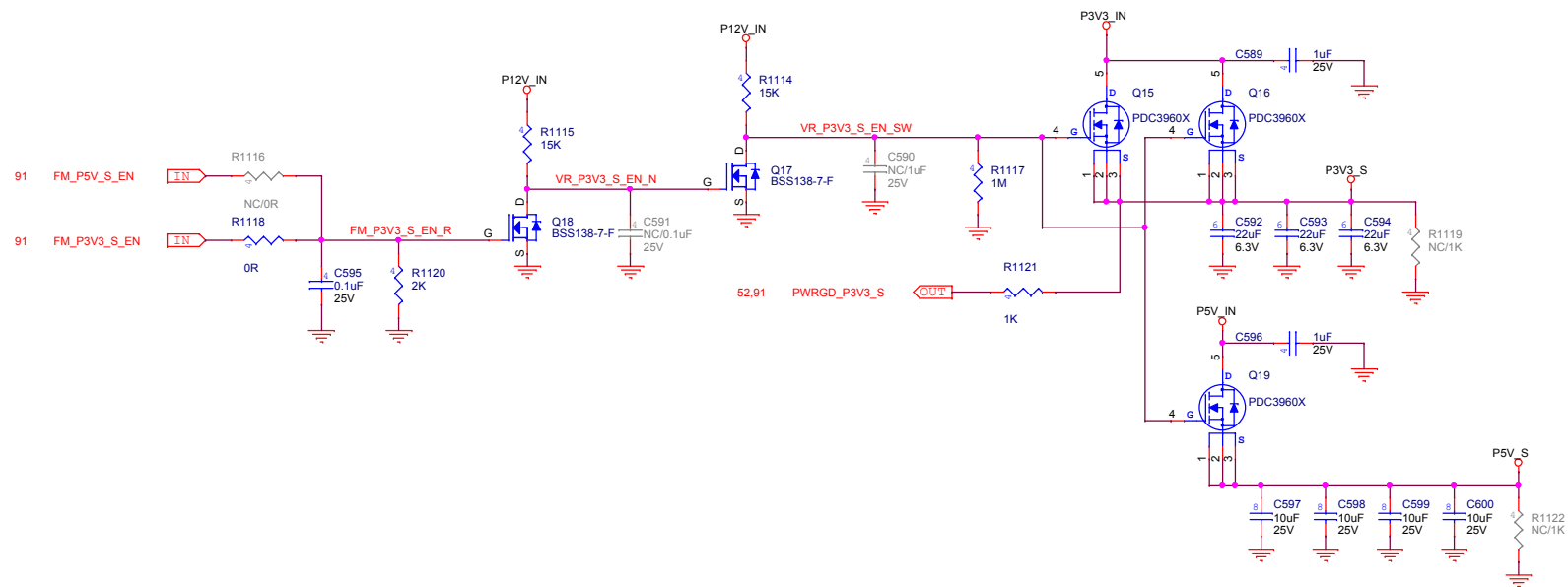
RIPPLE : $\pm 0.5\%$

DC+RIPPLE+AC : $\pm 4.5\%$

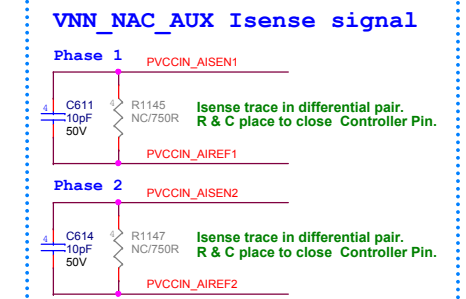
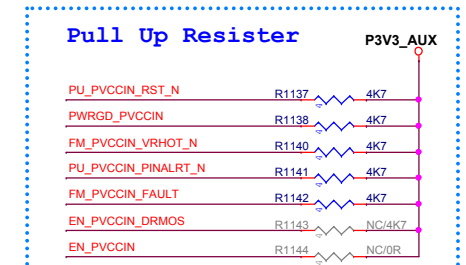
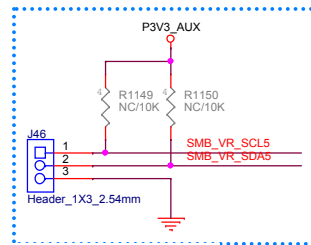
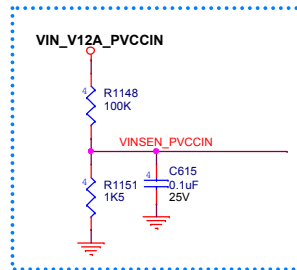
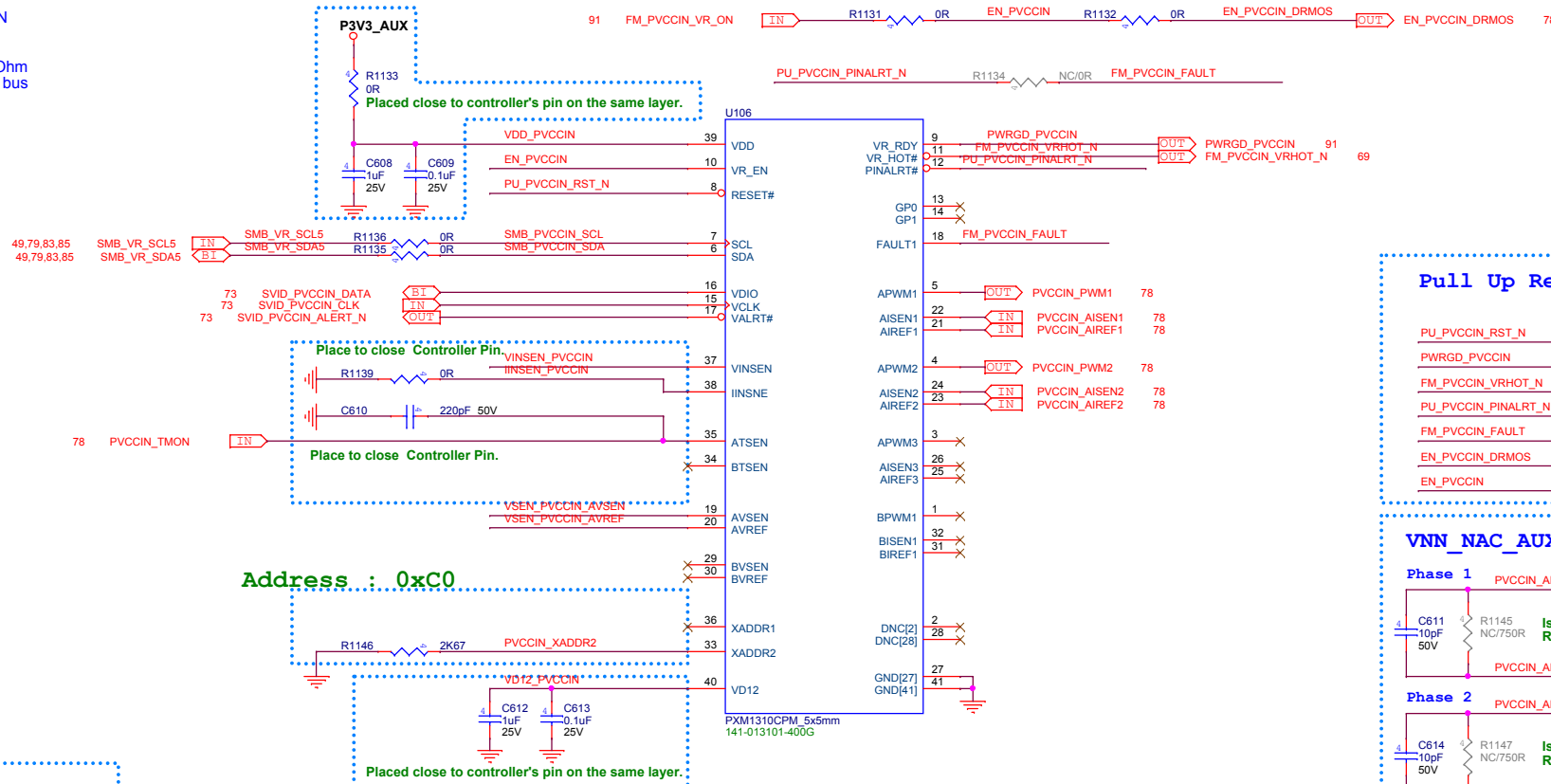


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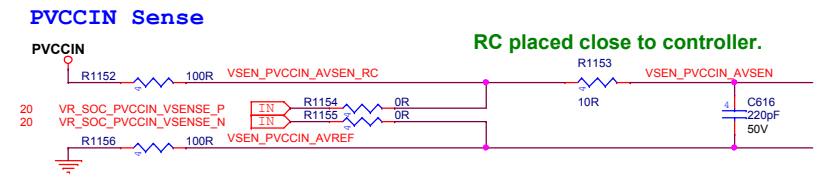
Title	PWR- BMC		
Size	Document Number	CB-1737	Rev A0
Date:	Thursday, August 19, 2021	Sheet 75 of 92	



```
Power Rail : PVCCIN
Vout       : SVID
Imax       : 73 A
LoadLine   : 2.00 mOhm
SVID       : 0x00 @ bus
0
SMBus      : 0xC0
```

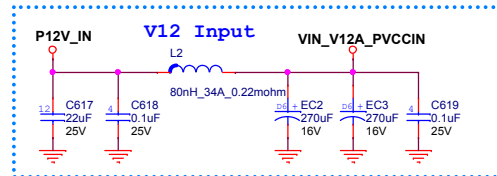


Vsense signal in differential pair with decent width(=10mils) and keep routing 5mils Air GAP, 15~20mils space to other signals.

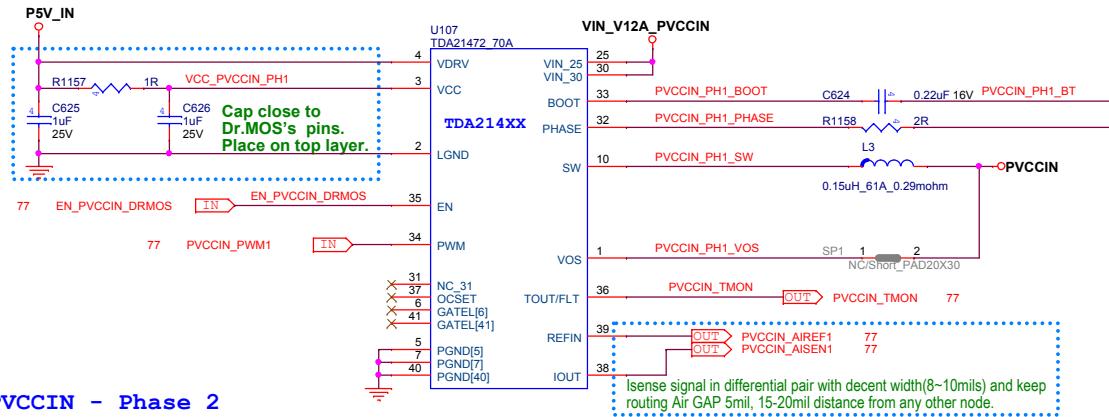


Device I2C Slave Address									
Resistor-to-GND (1%)		XADDR2							
		2.26 kΩ	2.67 kΩ	3.16 kΩ	4.02 kΩ	5.36 kΩ	8.06 kΩ	16.0 kΩ	Open
XADDR1	2.26 kΩ	FC	DC	BC	9C	7C	5C	3C	1C
	2.67 kΩ	F8	D8	B8	98	78	58	38	reserved
	3.16 kΩ	F4	D4	B4	94	74	54	34	14
	4.02 kΩ	F0	D0	B0	90	70	50	30	10
	5.36 kΩ	EC	CC	AC	8C	6C	4C	2C	0C
	8.06 kΩ	E8	C8	A8	88	68	48	28	08
	16.0 kΩ	E4	C4	A4	84	64	44	24	04
	Open	E0	C0	A0	80	60	40	20	reserved

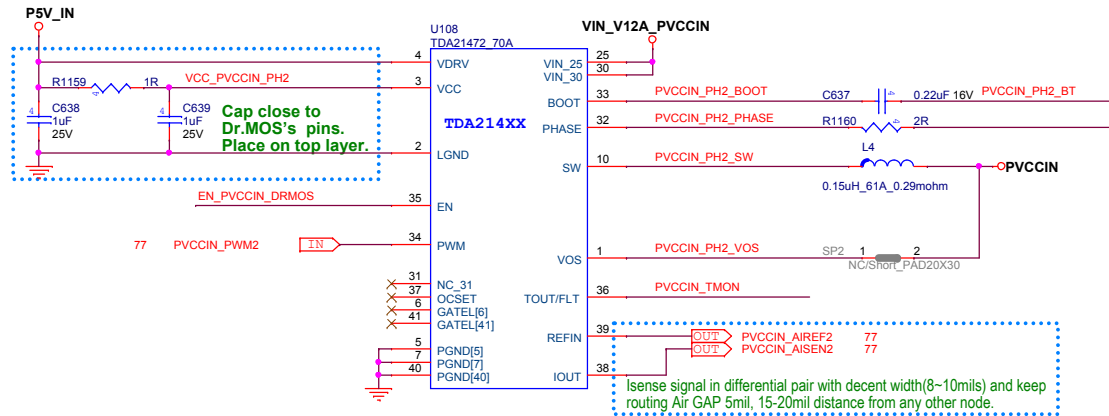
```
Power Rail : PVCCIN
Vout      : SVID
Imax      : 73A
SVID      : 0x00@bus 0
SMBus     : 0xC0
```



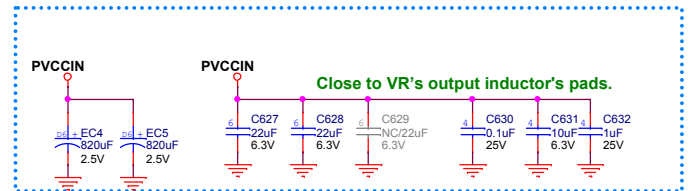
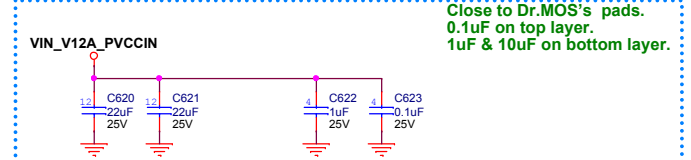
PVCCIN - Phase 1



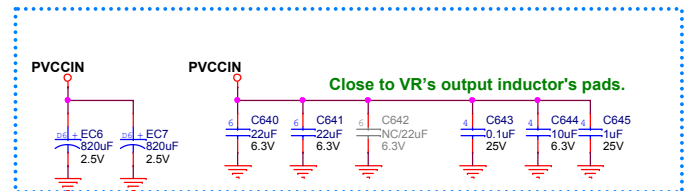
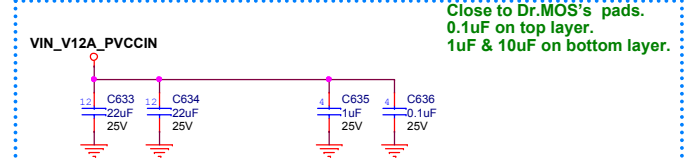
PVCCIN - Phase 2



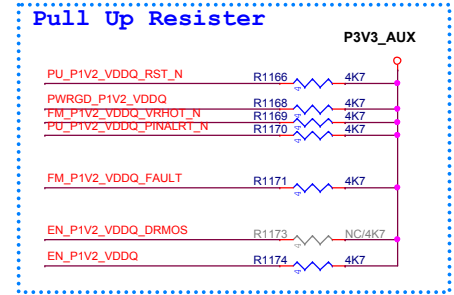
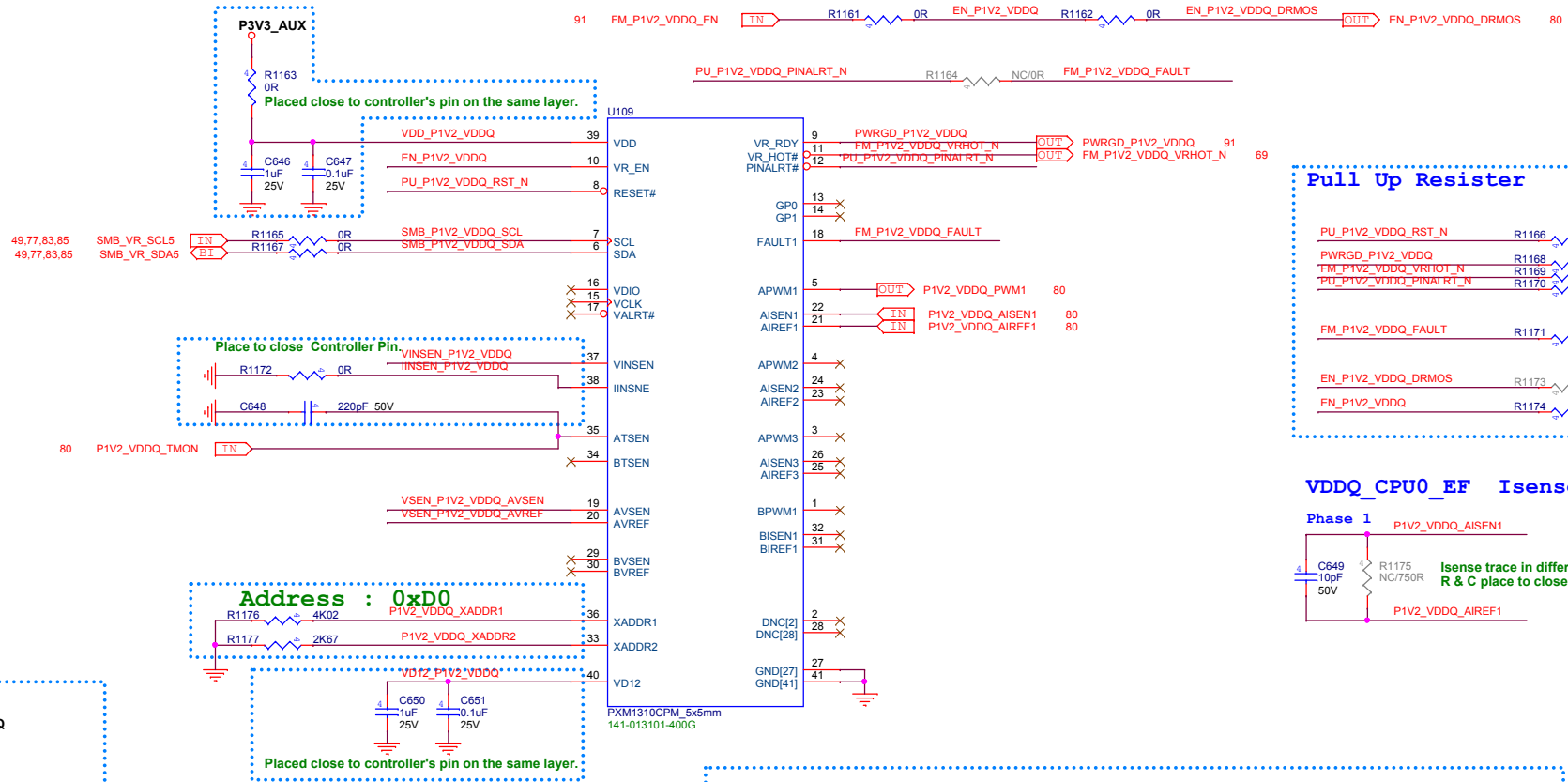
PVCCIN - Phase 1



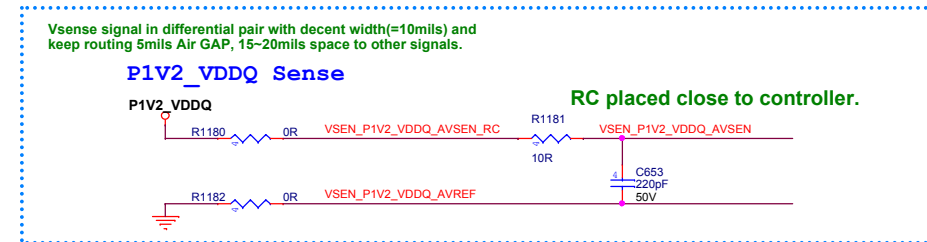
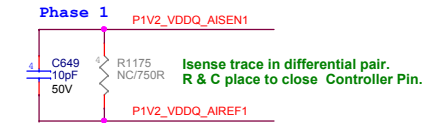
PVCCIN - Phase 2



Power Rail : P1V2_VDDQ
Vout : 1.215V
Imax : 27A
SVID :
SMBus : 0xD0



VDDQ_CPU0_EF Isense signal

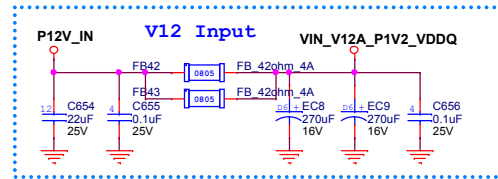
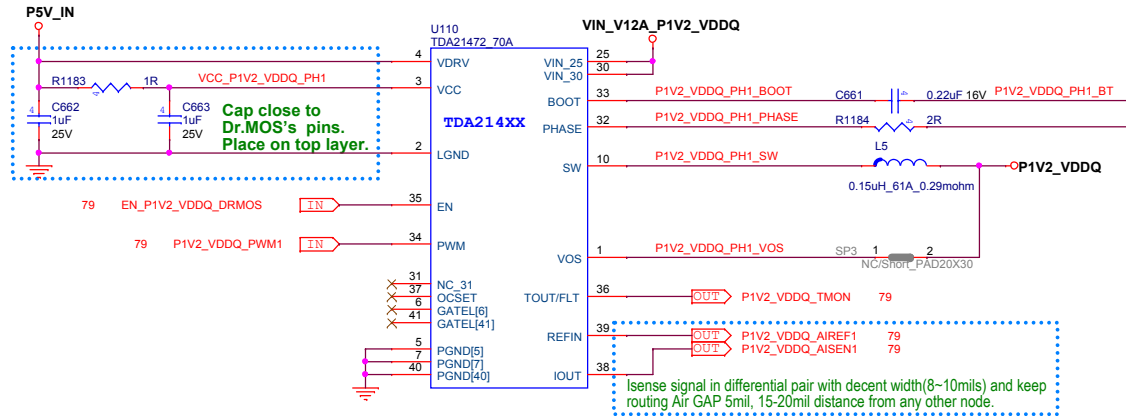


Device I2C Slave Address

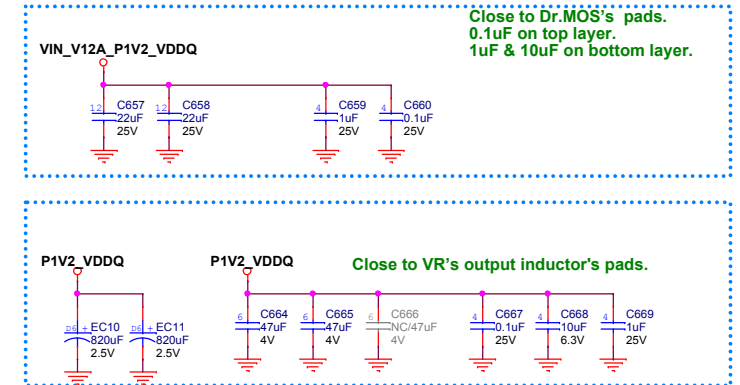
Resistor-to-GND (1%)	XADDR2							
	2.26 kΩ	2.67 kΩ	3.16 kΩ	4.02 kΩ	5.36 kΩ	8.06 kΩ	16.0 kΩ	Open
XADDR1	2.26 kΩ	FC	DC	BC	9C	7C	5C	1C
	2.67 kΩ	F8	D8	B8	98	78	58	reserved
	3.16 kΩ	F4	D4	B4	94	74	54	14
	4.02 kΩ	F0	D0	B0	90	70	50	10
	5.36 kΩ	EC	CC	AC	8C	6C	4C	0C
	8.06 kΩ	E8	C8	A8	88	68	48	08
	16.0 kΩ	E4	C4	A4	84	64	44	04
	Open	E0	C0	A0	80	60	40	reserved

Power Rail : P1V2_VDDQ
Vout : 1.215V
Imax : 27A
SVID :
SMBus : 0xD0

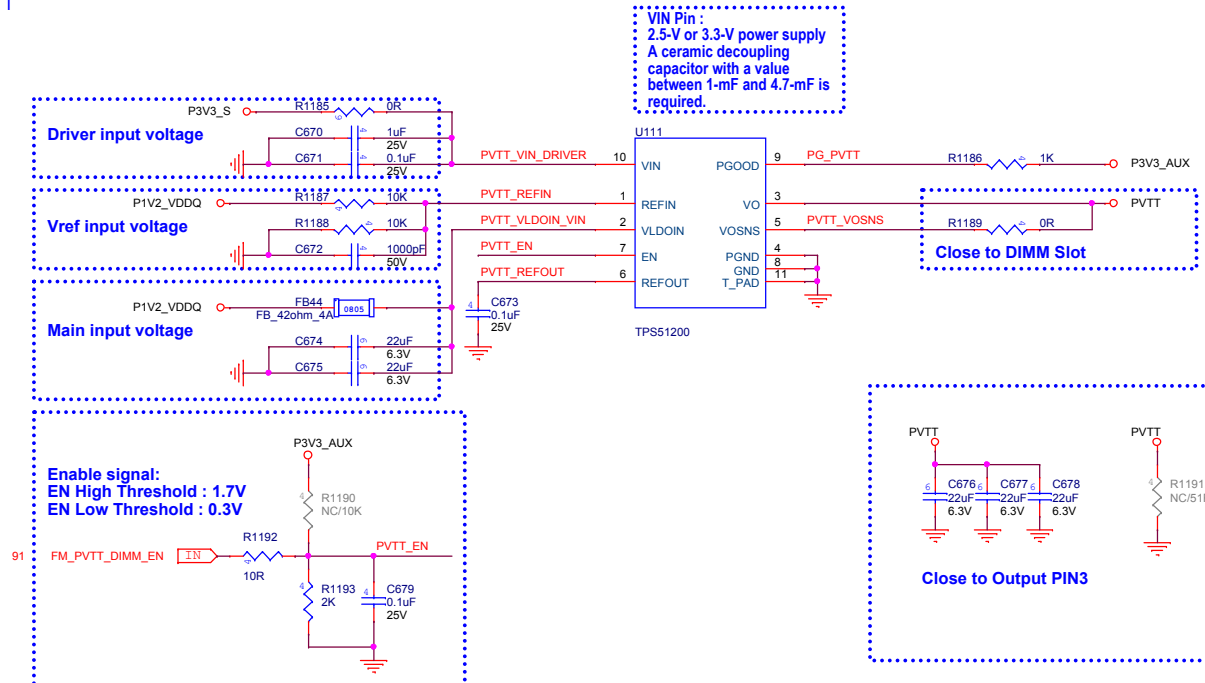
P1V2_VDDQ Phase 1



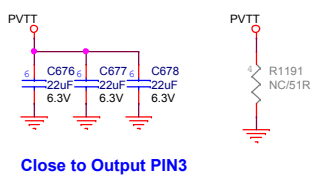
P1V2_VDDQ Phase 1

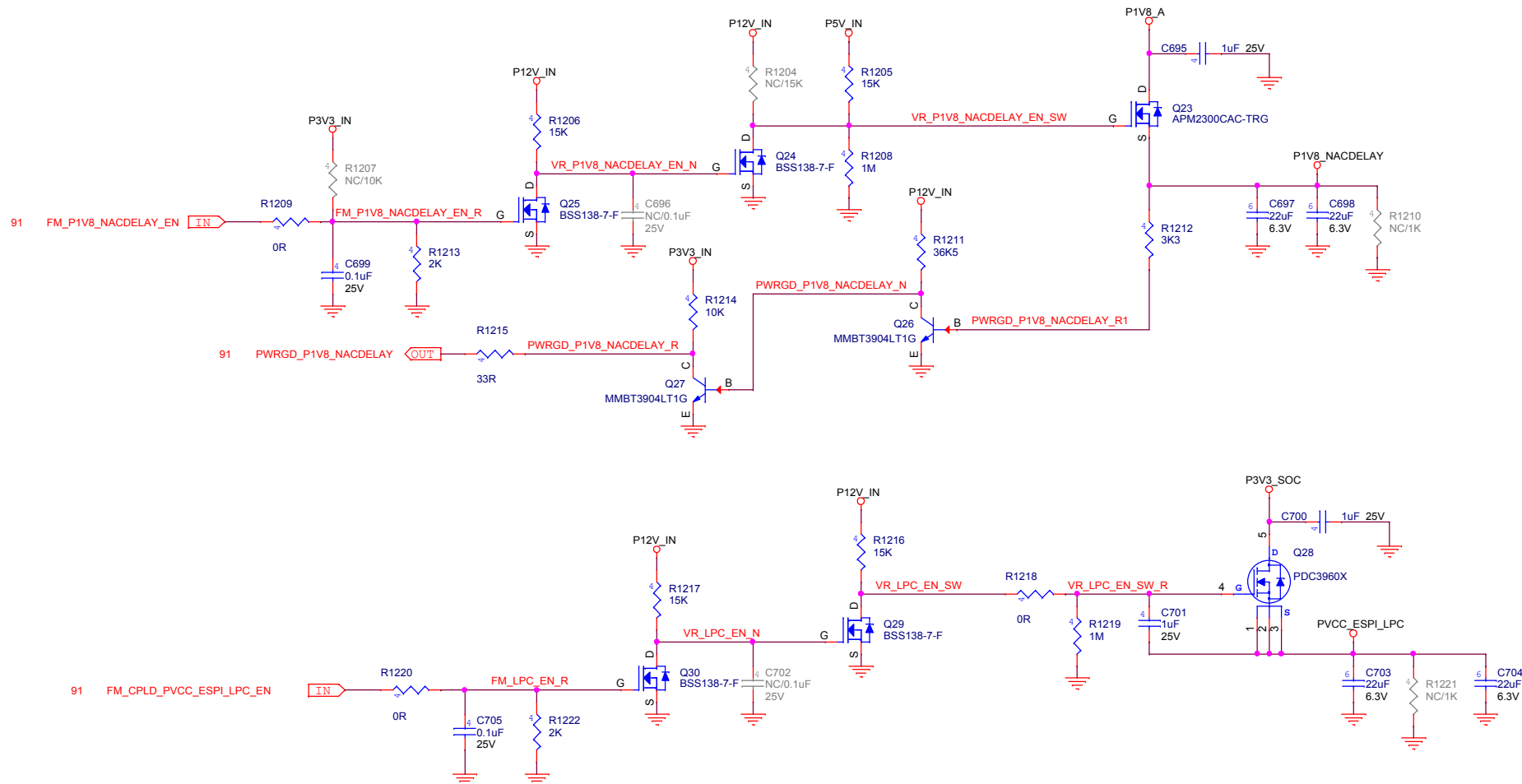


Power Rail : PVT
Vout : 0.6V
Imax : 0.84A



VIN Pin :
2.5-V or 3.3-V power supply
A ceramic decoupling capacitor with a value between 1-mF and 4.7-mF is required.

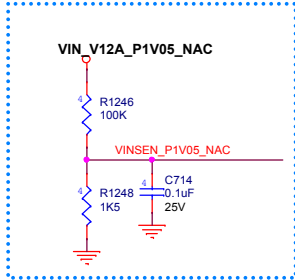
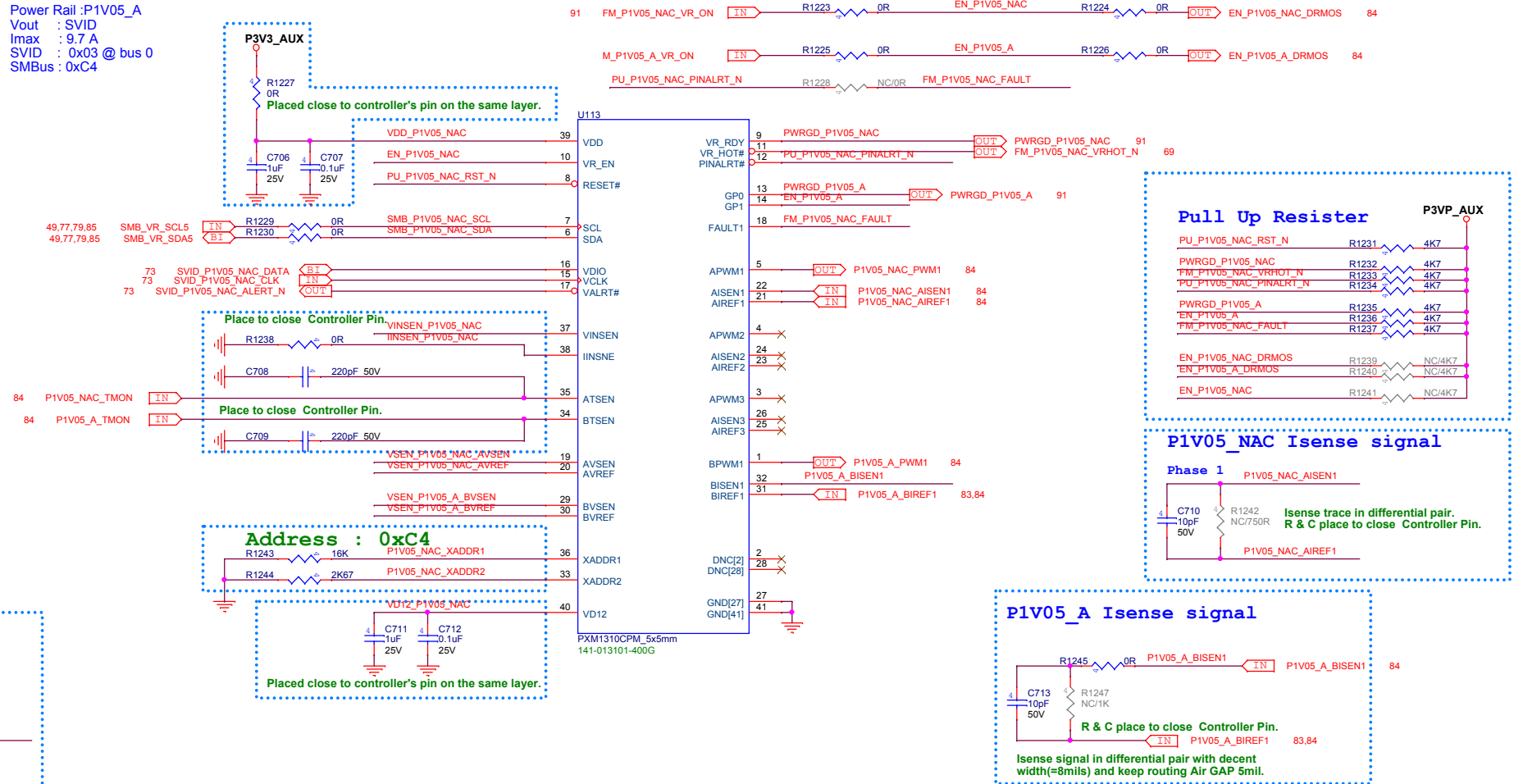




AEWIN Technologies Co., Ltd.			
Title		PWR- P1V8_NACDELAY	
Size	Document Number	CB-1737	
Date:	Thursday, August 19, 2021	Sheet	82 of 92

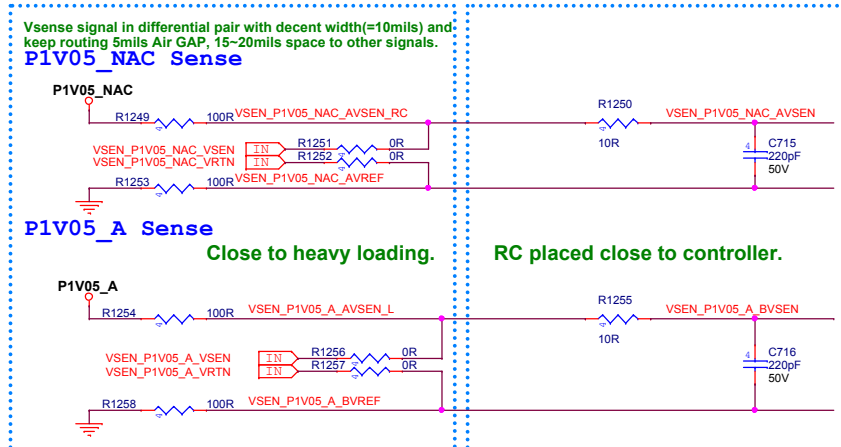
Power Rail :P1V05_NAC
Vout : SVID
Imax : 5.5 A
SVID : 0x02 @ bus 0
SMBus : 0xC4

Power Rail :P1V05_A
Vout : SVID
Imax : 9.7 A
SVID : 0x03 @ bus 0
SMBus : 0xC4



Device I2C Slave Address

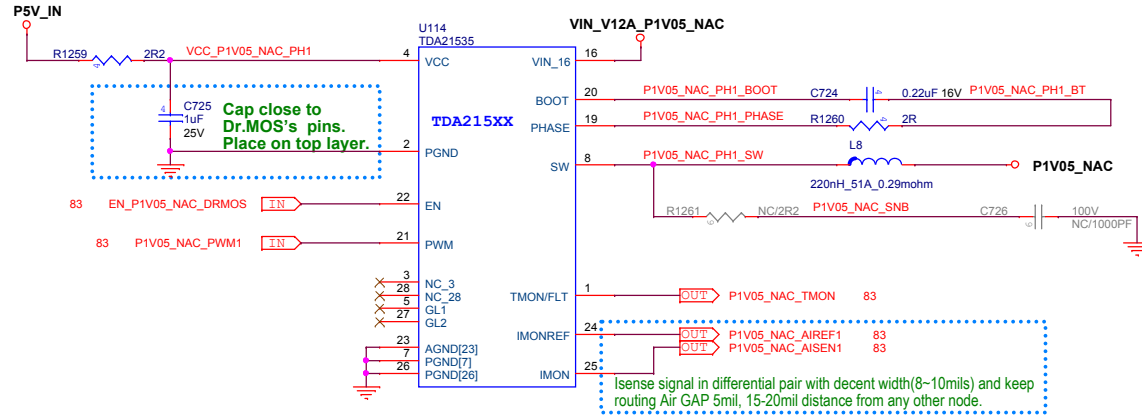
Resistor-to- GND (1%)	XADDR2							
	2.26 kΩ	2.67 kΩ	3.16 kΩ	4.02 kΩ	5.36 kΩ	8.06 kΩ	16.0 kΩ	Open
2.26 kΩ	FC	DC	BC	9C	7C	5C	3C	1C
2.67 kΩ	F8	D8	B8	98	78	58	38	reserved
3.16 kΩ	F4	D4	B4	94	74	54	34	14
4.02 kΩ	F0	D0	B0	90	70	50	30	10
5.36 kΩ	EC	CC	AC	8C	6C	4C	2C	0C
8.06 kΩ	E8	C8	A8	88	68	48	28	08
16.0 kΩ	E4	C4	A4	84	64	44	24	04
Open	E0	C0	A0	80	60	40	20	reserved



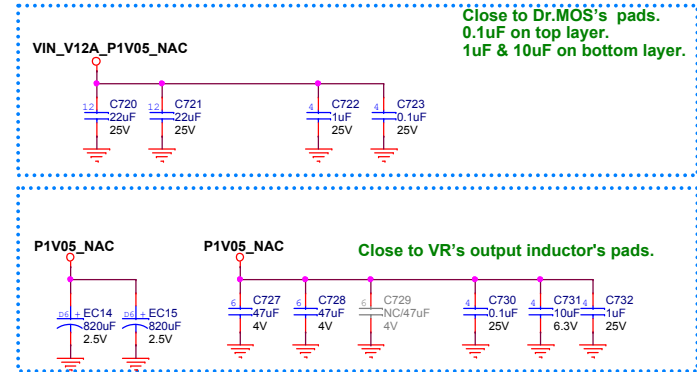
Power Rail :P1V05_NAC
Vout : SVID
Imax : 5.5 A
SVID : 0x02 @ bus 0
SMBus : 0xC4

Power Rail :P1V05_A
Vout : SVID
Imax : 9.7 A
SVID : 0x03 @ bus 0
SMBus : 0xC4

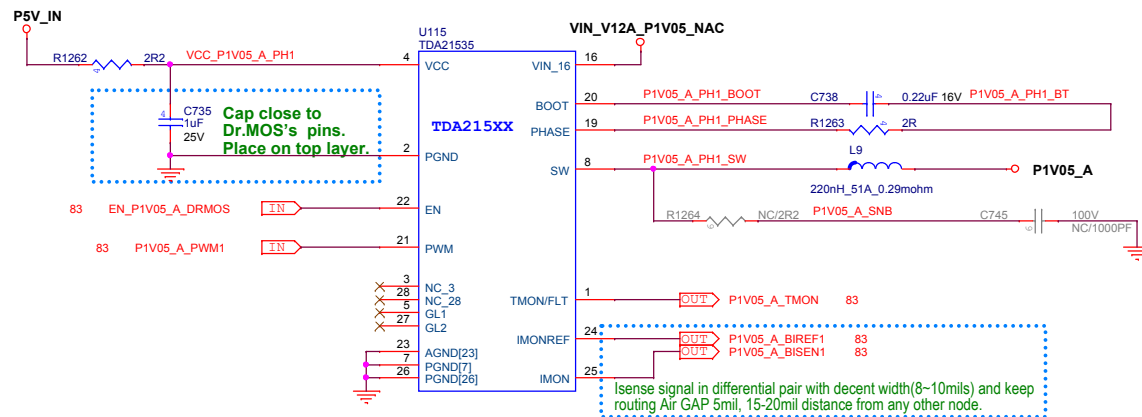
P1V05_NAC Phase 1



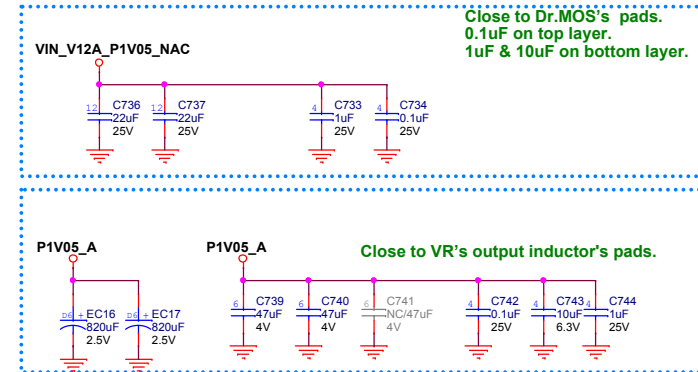
P1V05_NAC Phase 1



P1V05_A Phase 1

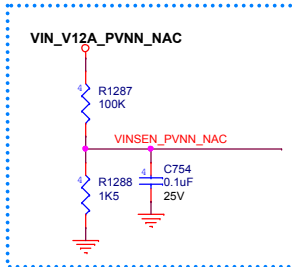
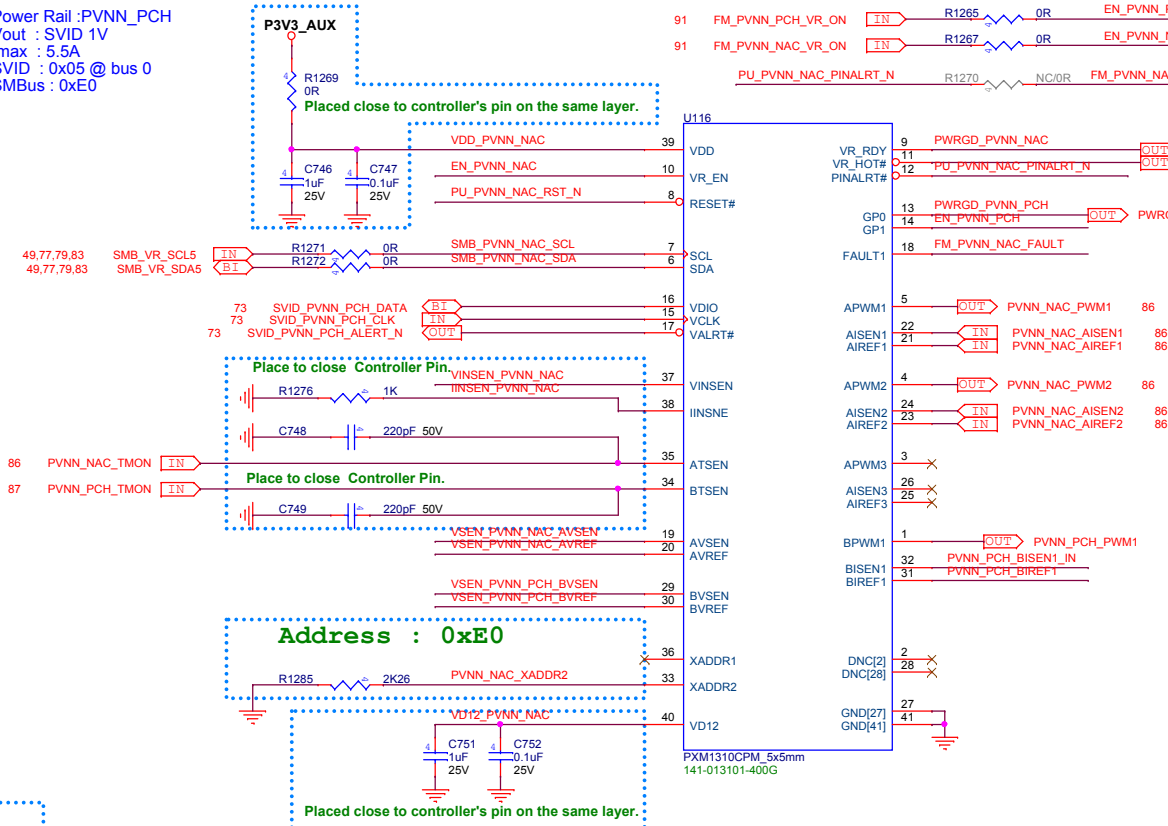


P1V05_A Phase 1



Power Rail : PVNN_NAC
Vout : SVID 1V
Imax : 51A
SVID : 0x04@bus 0
SMBus : 0xE0

Power Rail :PVNN_PCH
Vout : SVID 1V
Imax : 5.5A
SVID : 0x05 @ bus 0
SMBus : 0xE0

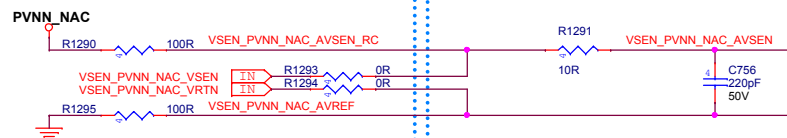


Device I2C Slave Address

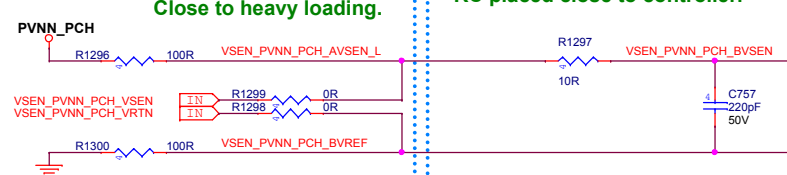
Resistor-to-GND (1%)	XADDR2							
	2.26 kΩ	2.67 kΩ	3.16 kΩ	4.02 kΩ	5.36 kΩ	8.06 kΩ	16.0 kΩ	Open
XADDR1	2.26 kΩ	FC	DC	BC	9C	7C	5C	3C
	2.67 kΩ	F8	D8	B8	98	78	58	38
	3.16 kΩ	F4	D4	B4	94	74	54	34
	4.02 kΩ	F0	D0	B0	90	70	50	30
	5.36 kΩ	EC	CC	AC	8C	6C	4C	2C
	8.06 kΩ	E8	C8	A8	88	68	48	28
	16.0 kΩ	E4	C4	A4	84	64	44	24
	Open	E0	C0	A0	80	60	40	20
								reserved

Vsense signal in differential pair with decent width(=10mils) and keep routing 5mils Air GAP, 15~20mils space to other signals.

PVNN_NAC Sense



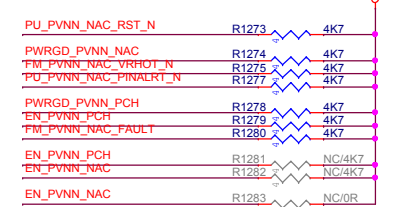
PVNN_PCH Sense



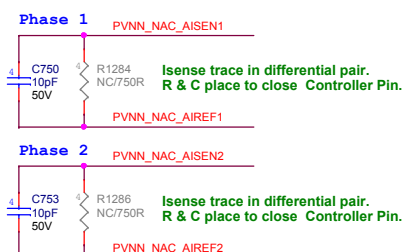
Close to heavy loading.

RC placed close to controller.

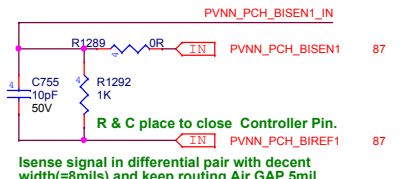
Pull Up Resister



PVNN_NAC Isense signal

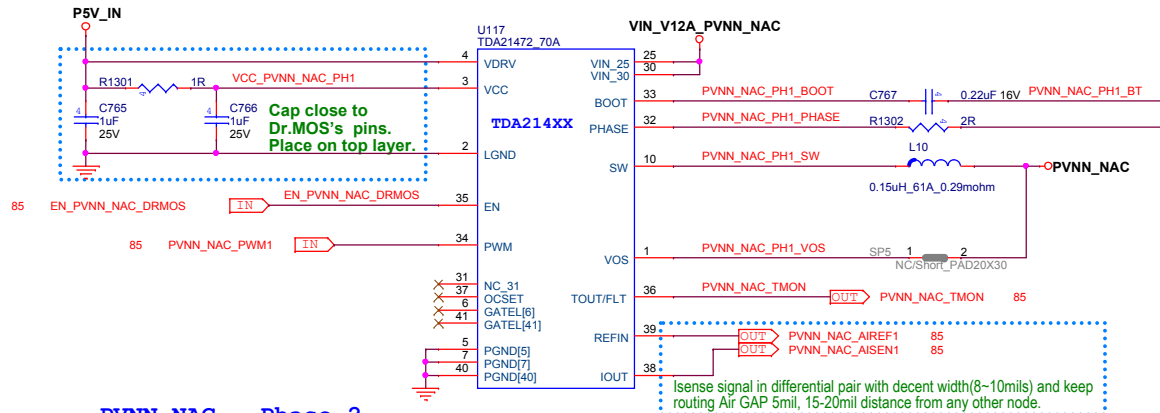


PVNN_PCH Isense signal

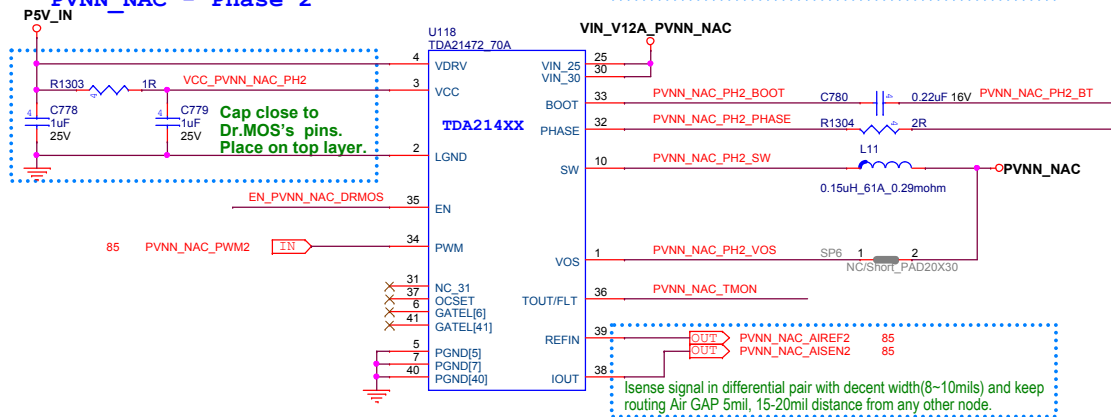


Power Rail : PVNN_NAC
Vout : SVID 1V
Imax : 51A
SVID : 0x04@bus 0
SMBus : 0xE0

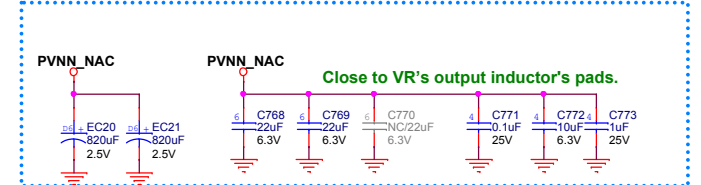
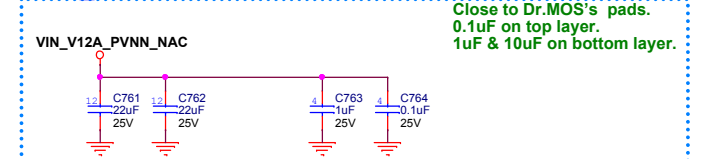
PVNN_NAC - Phase 1



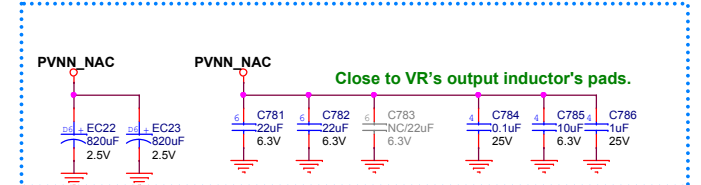
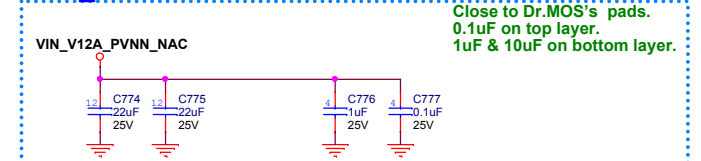
PVNN_NAC - Phase 2



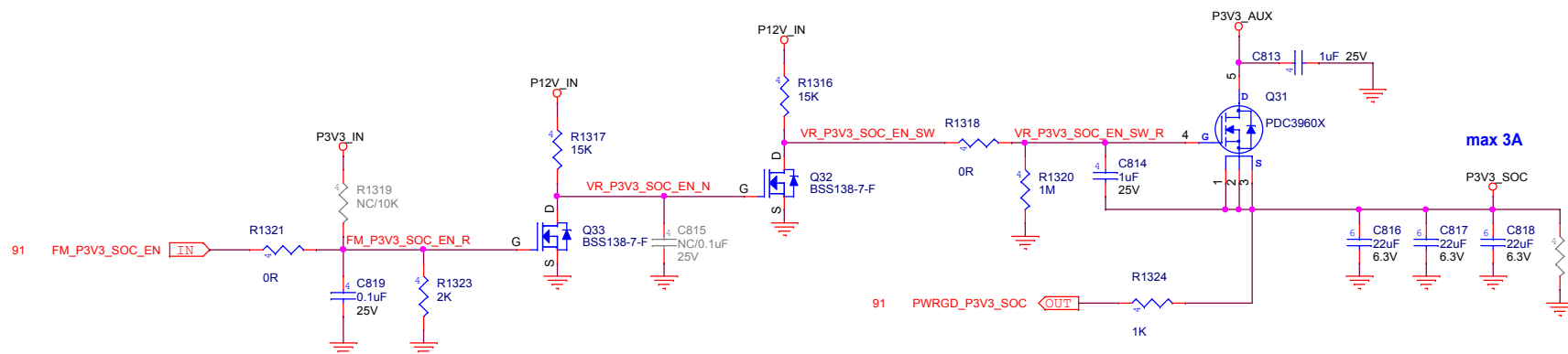
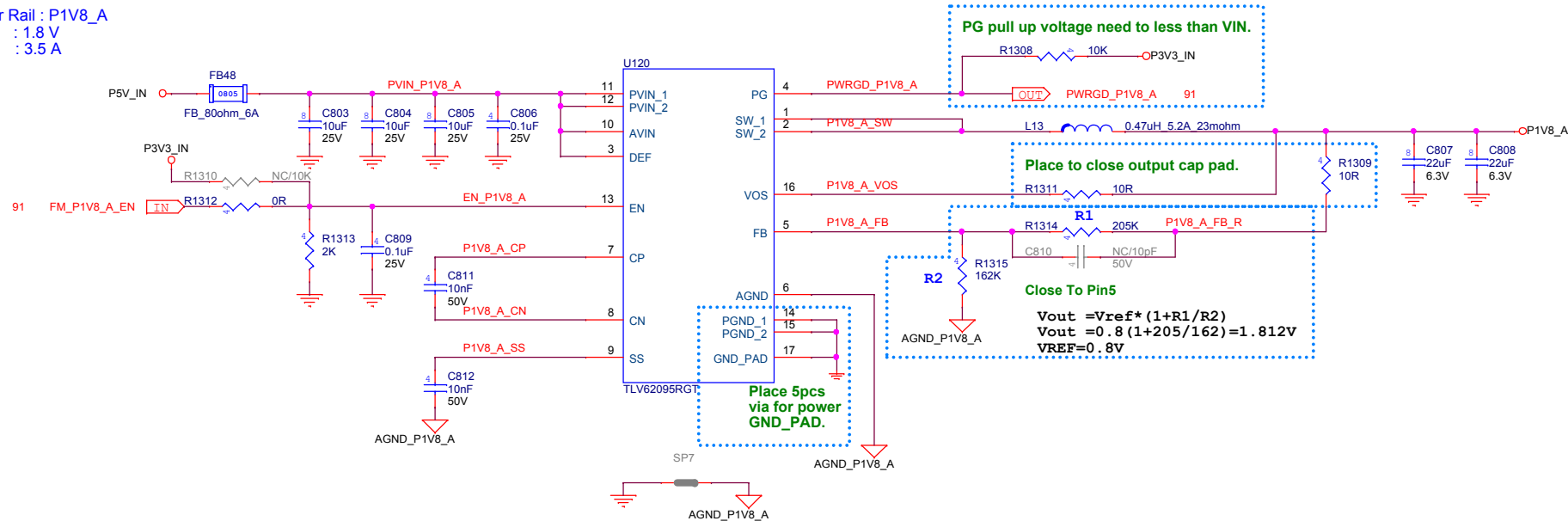
PVNN_NAC - Phase 1



PVNN_NAC - Phase 2



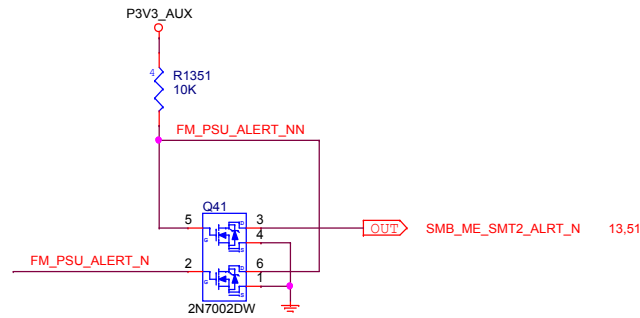
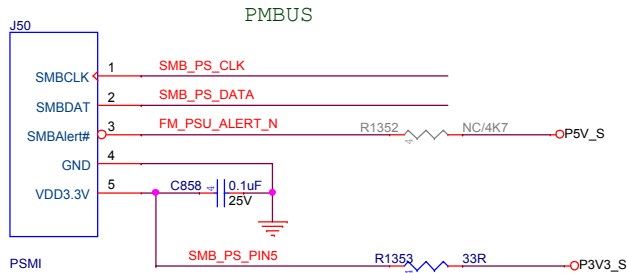
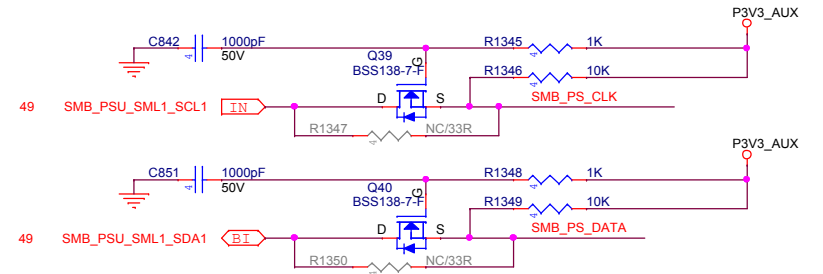
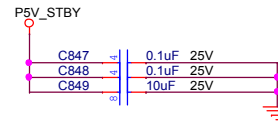
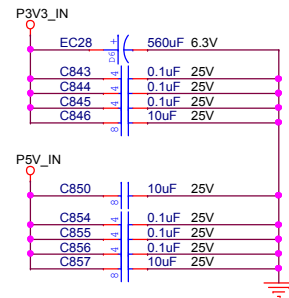
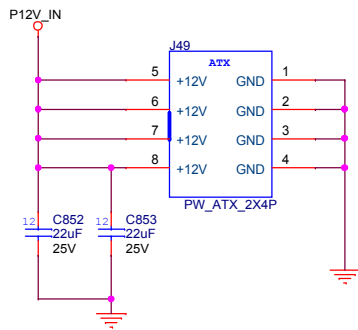
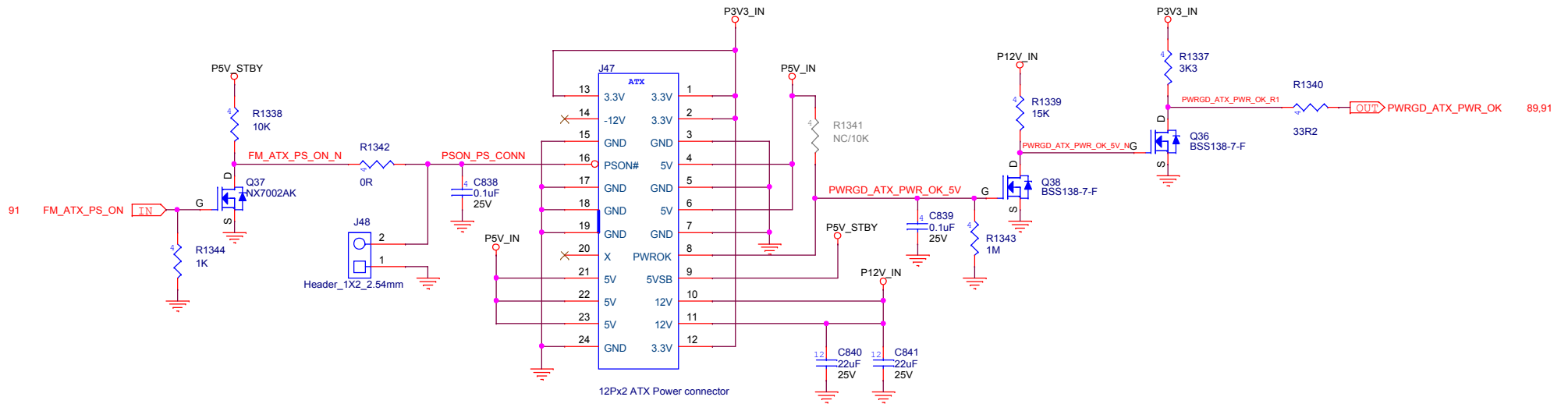
Power Rail : P1V8_A
Vout : 1.8 V
Imax : 3.5 A



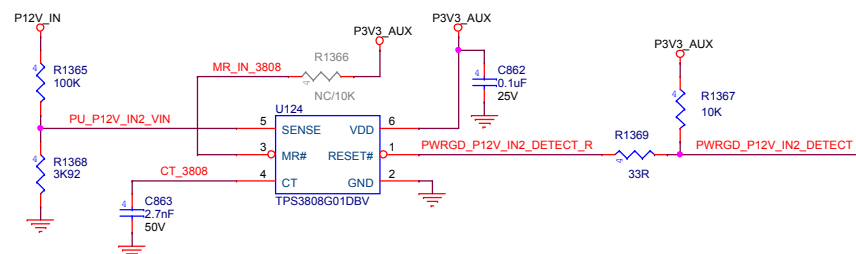
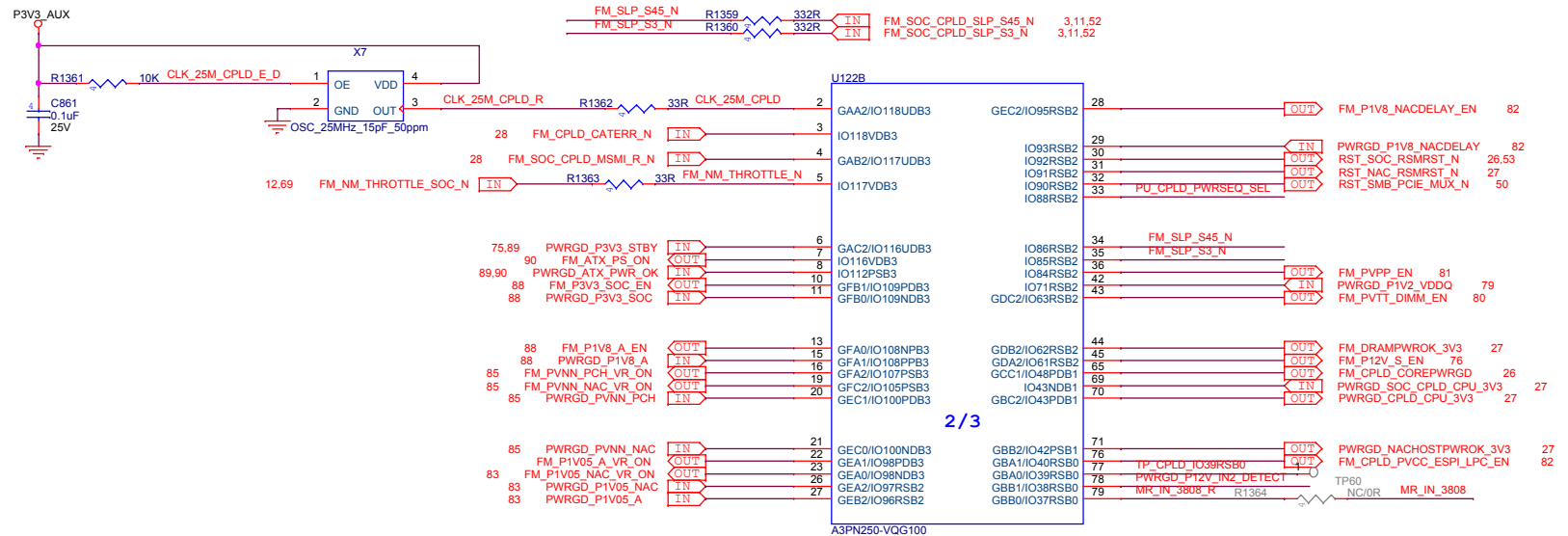
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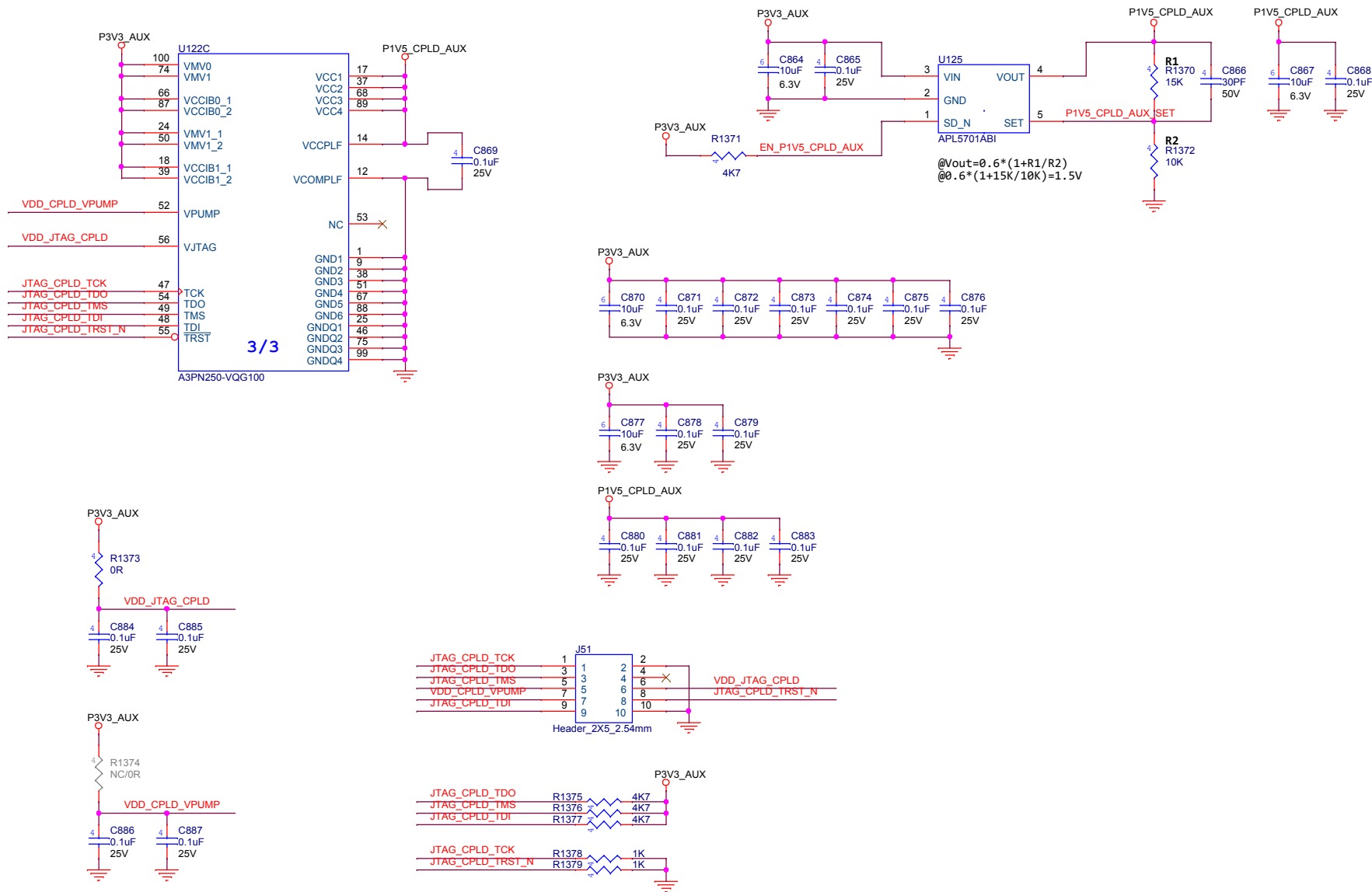
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Size	Document Number		CB-1737	
Date:	Thursday, August 19, 2021		Sheet	88 of 92

Rev A0



AEWIN Technologies Co., Ltd.			
Title		PWR - ATX IN	
Size	Document Number	CB-1737	
Date:	Thursday, August 19, 2021	Sheet	90 of 92
		Rev	A0





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Title		CPLD (2/2)	
Size	Document Number	CB-1737	
Date:	Thursday, August 19, 2021	Sheet	92 of 92

Rev
A0