Sports: HMC CS Prof. qualifies for Olympics in new Spam-eating event.

#### In the News Today

#### **News Briefs**

County fair serves up average food, but the price may be too high. What's fair fare for fair fair fare? (p.42)

## Spam-Based Computer Hailed as Technological Marvel

(Pasadena, AP): A team of computer science professors at the Pasadena Institute of Technology (P.I.T.) has unveiled a new computer that operates on pureed Spam rather than on electricity. "It's a work of genius that will undoubtedly revolutionize the way we think about Spam," said an enthusiastic spokesman of the canned meat products industry. However, a vegetarian alternative, operating on minced tofu, is also expected to be announced soon and this technology is less likely to smell considerably better. Industry analysts believe, however, that a chocolate pudding based computer being developed at Harvey Mudd College shows the greatest promise.

### True Story: Alan Turing



Alan Turing 1912-1954





1938 Princeton Ph.D. thesis on uncomputability

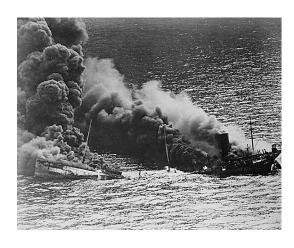
#### Alan Turing



**Bletchley Park** 



German WWII U-Boat



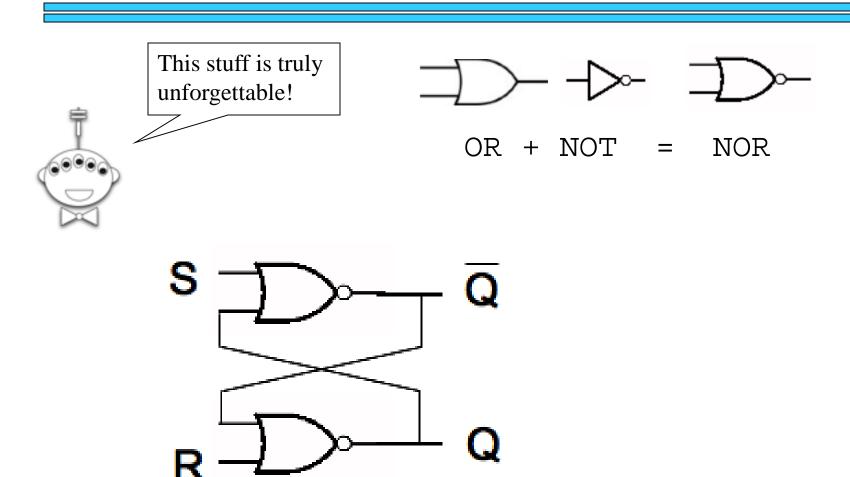
Allied Tanker hit by U-Boat Torpedo



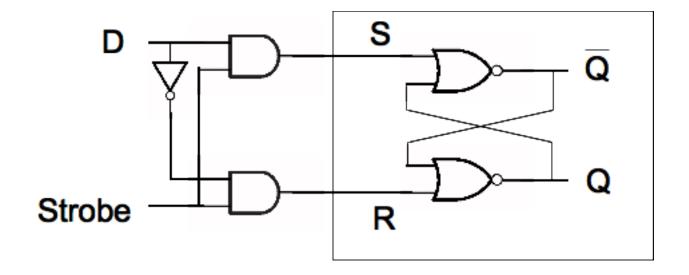
Enigma

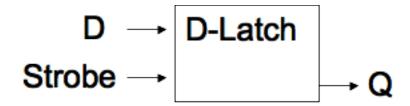


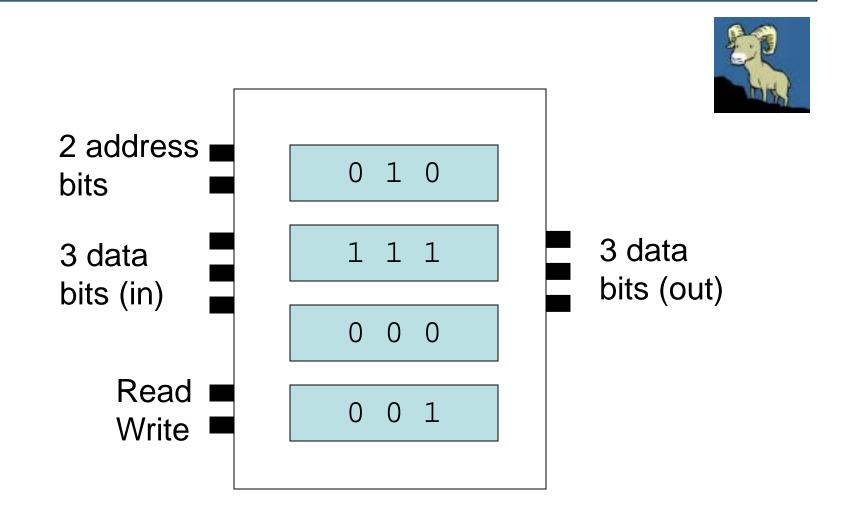
#### A 1-bit Memory

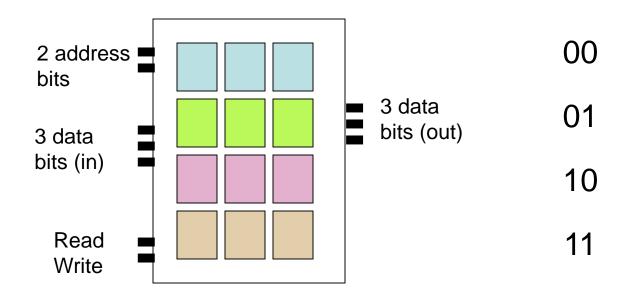


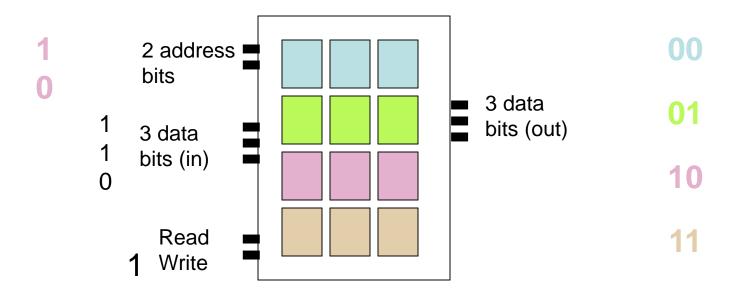
#### From S-R Latches to D-Latches

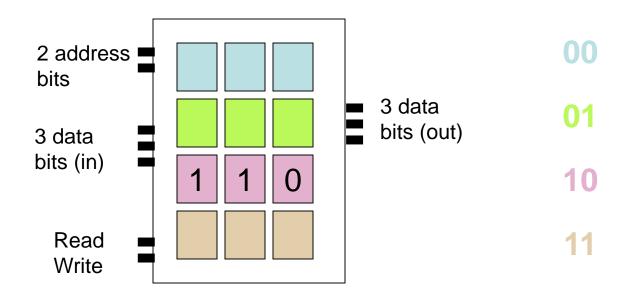


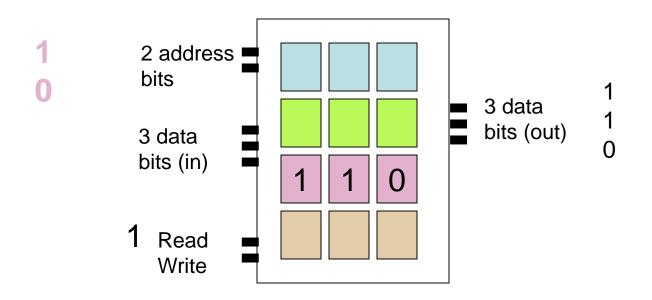


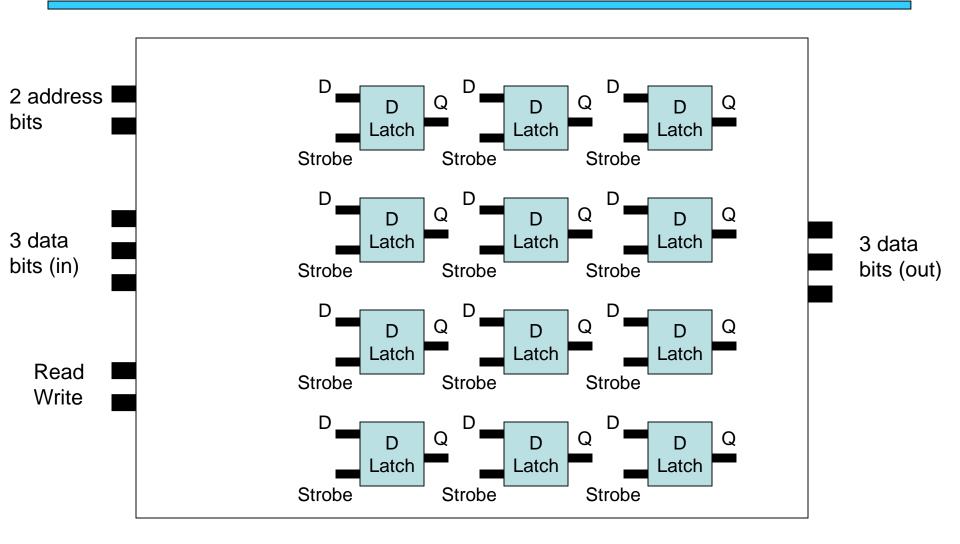


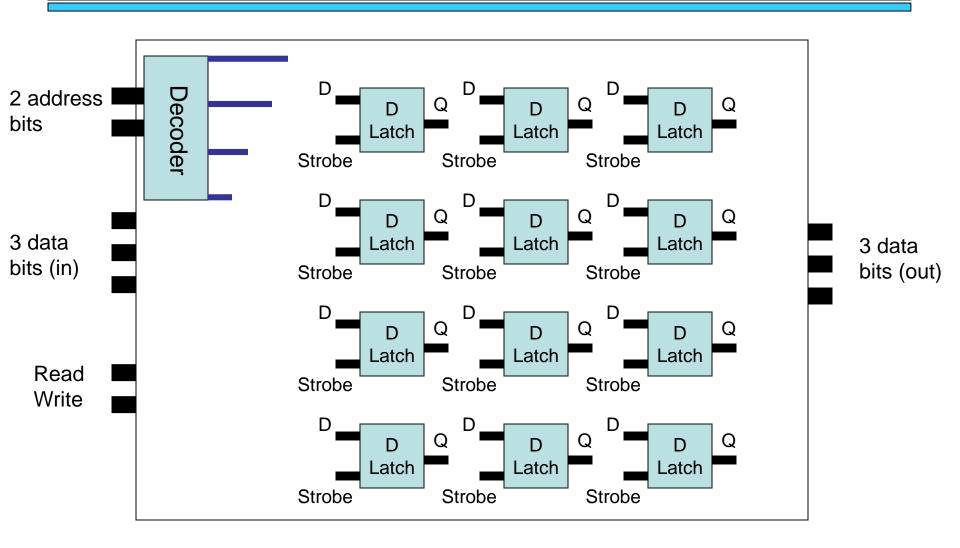


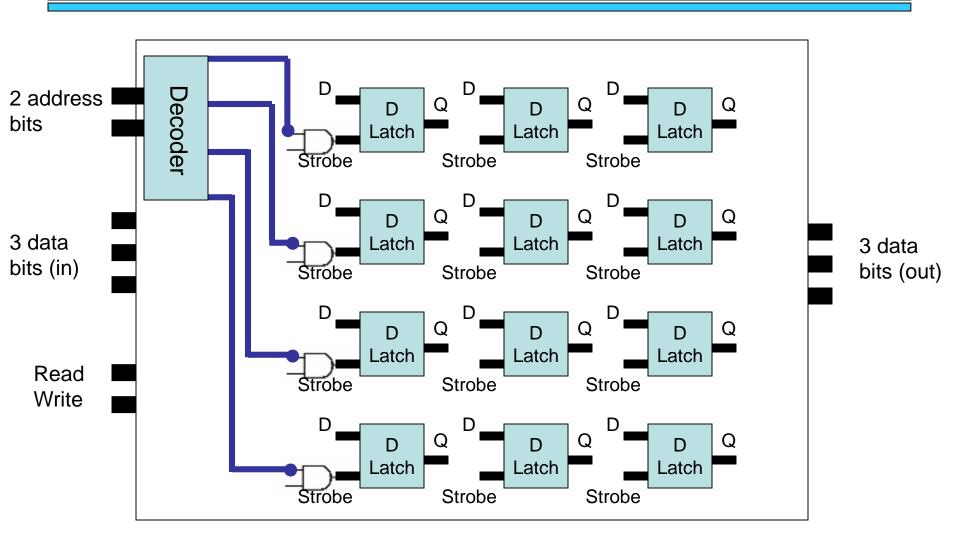


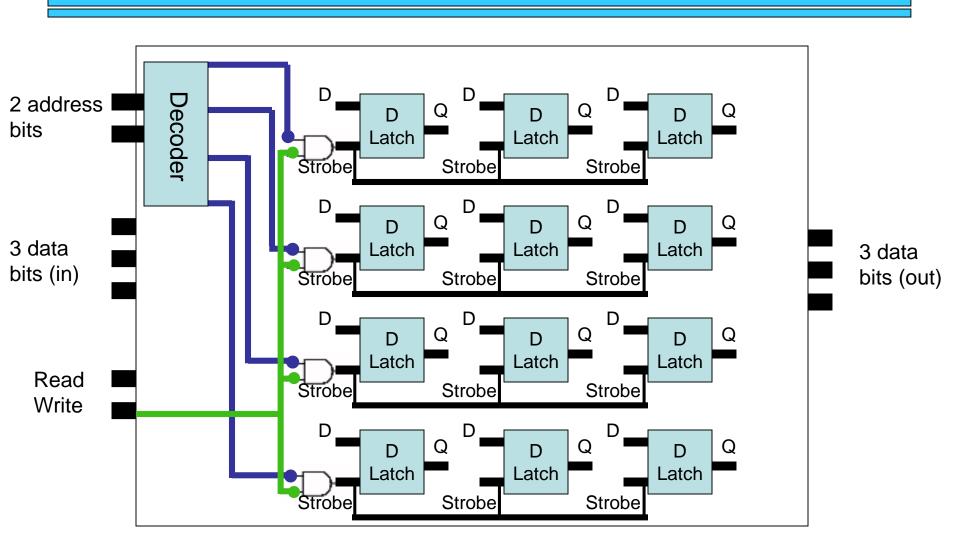


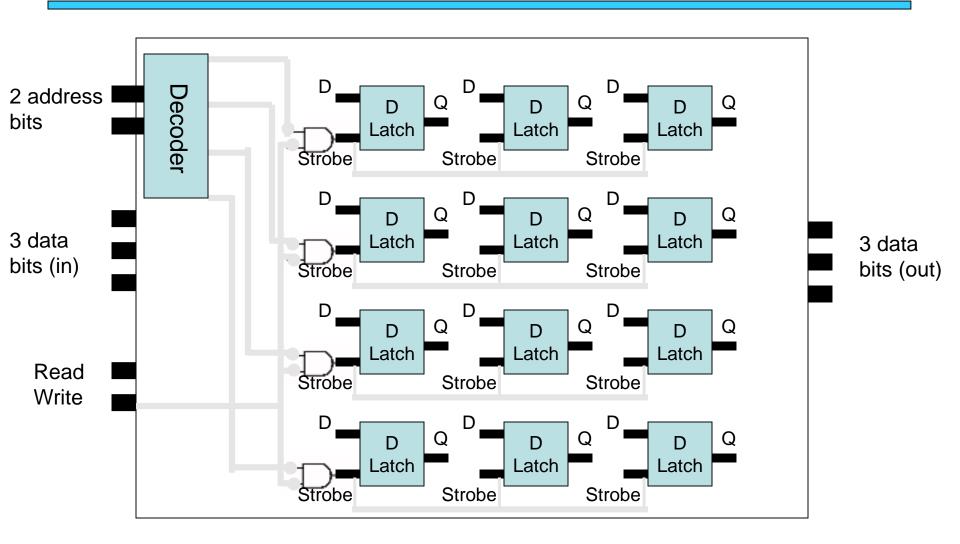


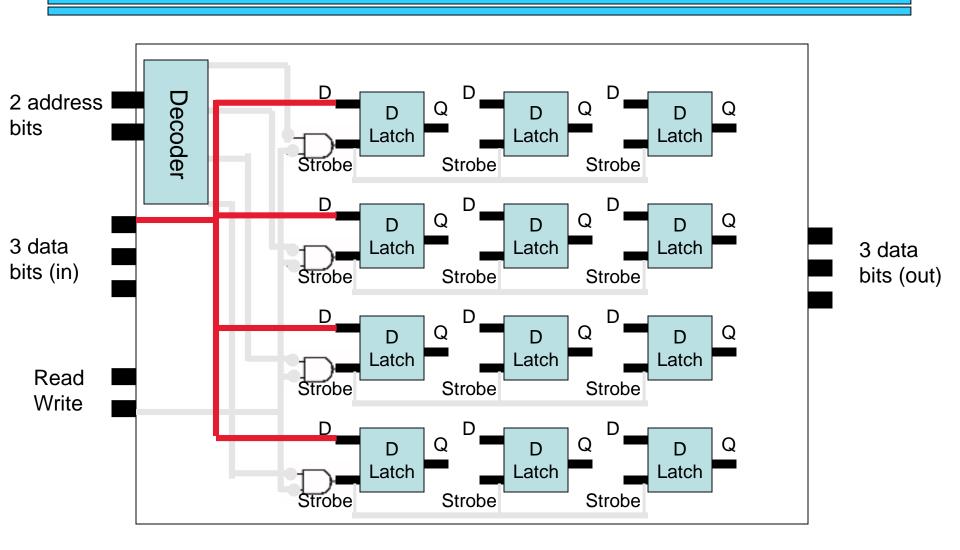


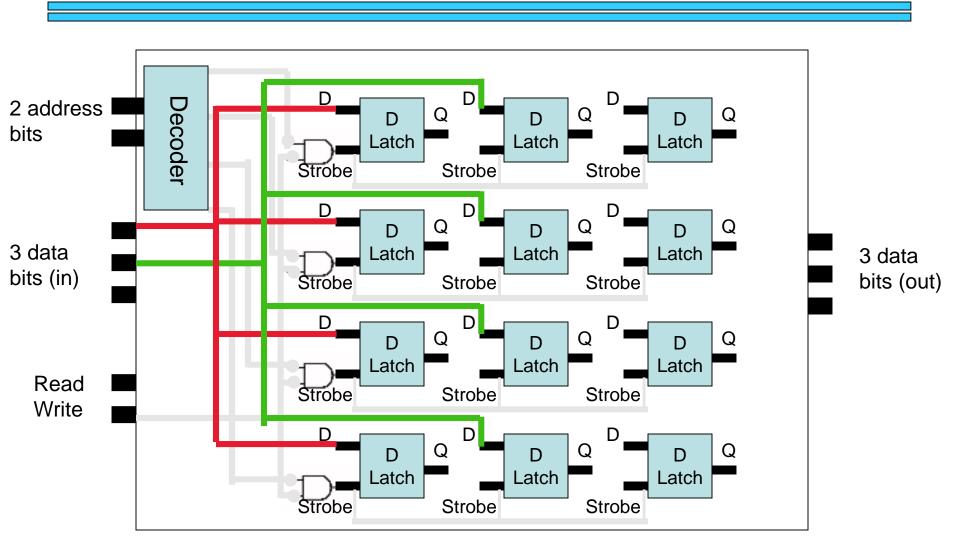


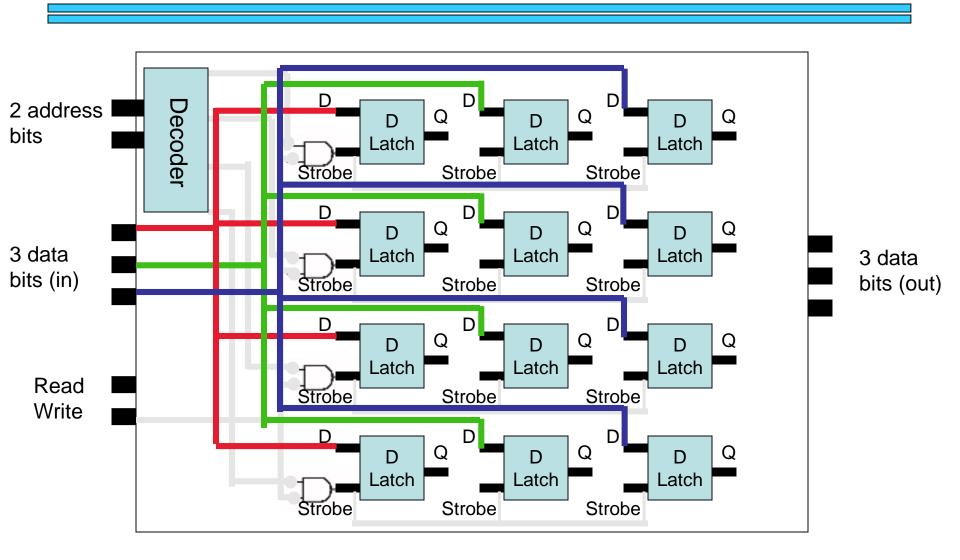










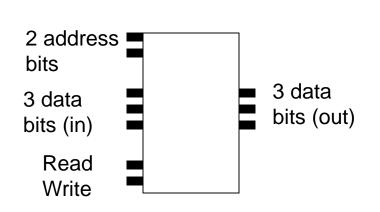


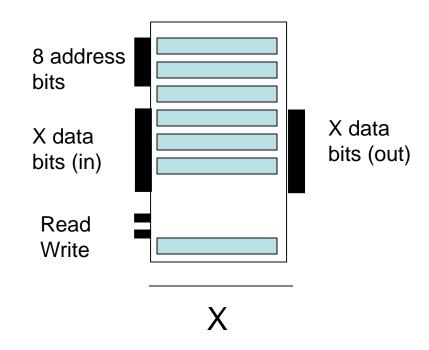




A 512K RAM (About 4.2 million bits)

# Small memory, "big" memory...





Instruction Register	Load 5 into Register 0	
Register 0	0	
Register 1	0	
Register 2	0	
Register 3	0	

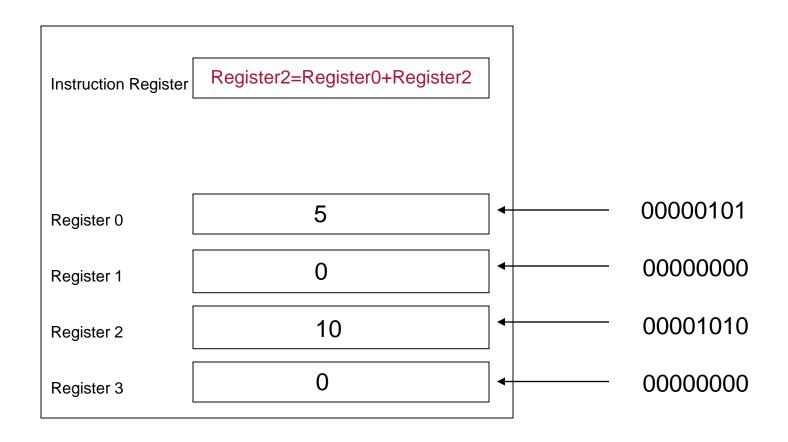
Instruction Register	Load 5 into Register 0	
Register 0	5	
Register 1	0	
Register 2	0	
Register 3	0	

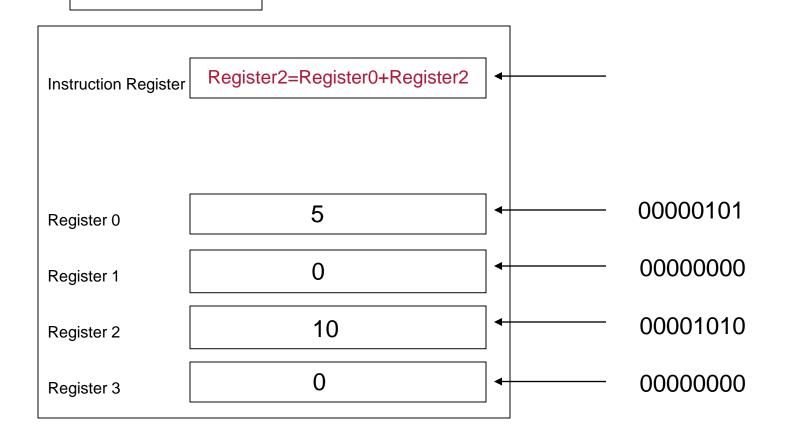
Instruction Register	nstruction Register Register2=Register0+Register1		
Register 0	5		
Register 1	0		
Register 2	0		
Register 3	0		

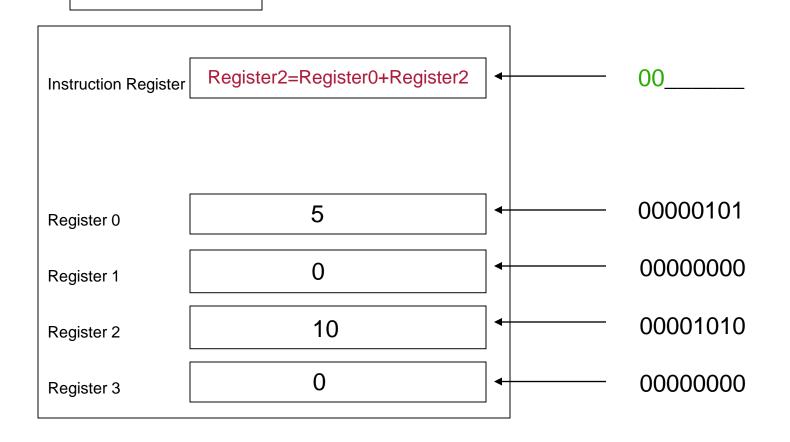
Instruction Register	Register2=Register0+Register1	
Register 0	5	
Register 1	0	
Register 2	5	
Register 3	0	

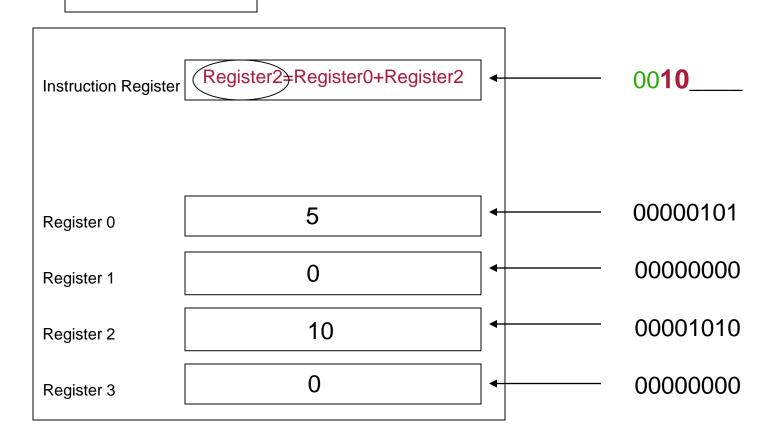
Instruction Register	n Register Register0+Register2	
Register 0	5	
Register 1	0	
Register 2	5	
Register 3	0	

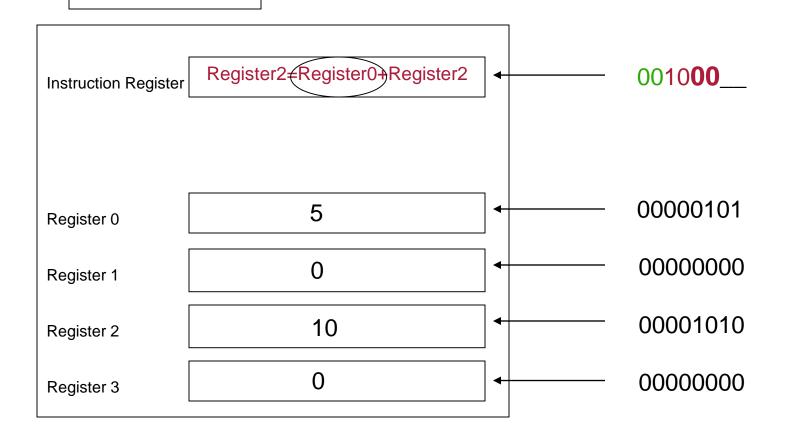
Instruction Register Register2=Register0+Register2		
Register 0	5	
Register 1	0	
Register 2	10	
Register 3	0	

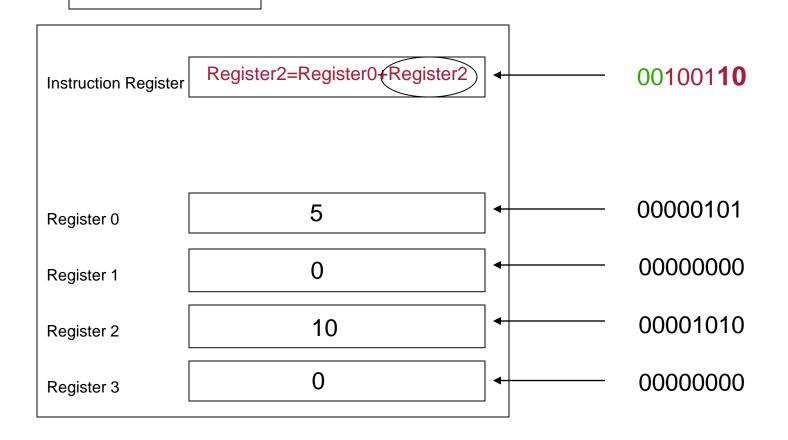


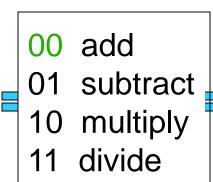












#### A Computer!

Program Counter	00000000
Instruction Register	00000000
Register 0	0000010
Register 1	00000000
Register 2	0000001
Register 3	00000000

	Binary	Base 10
00110010	00000000	0
00011010	00000001	1
10001100	00000010	2
	00000011	3
	00000100	4
	I	
	11111111	255

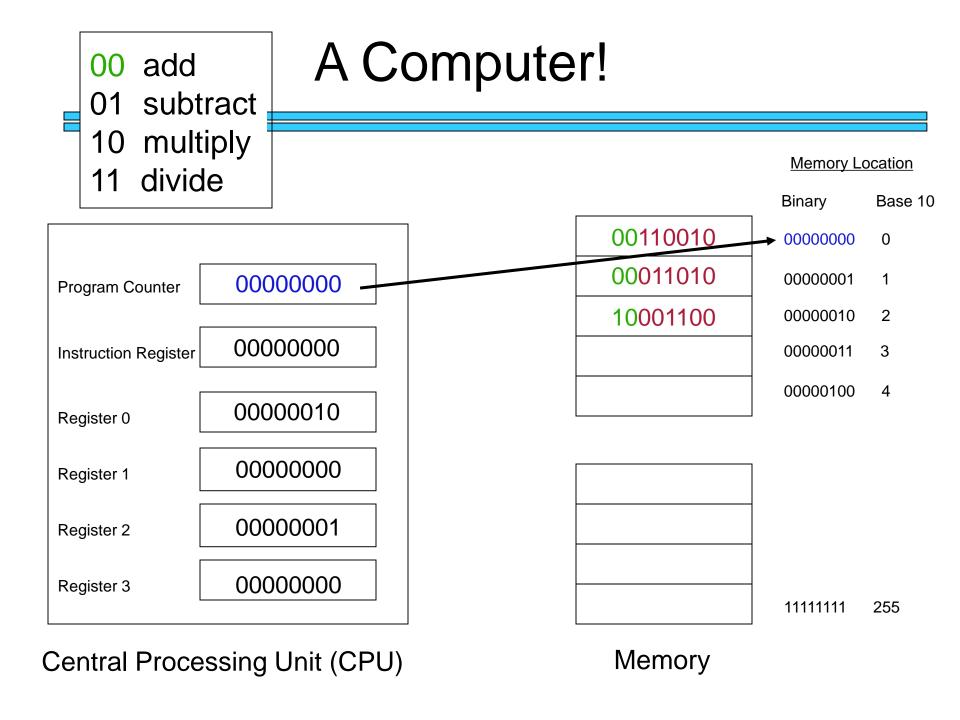
**Memory Location** 

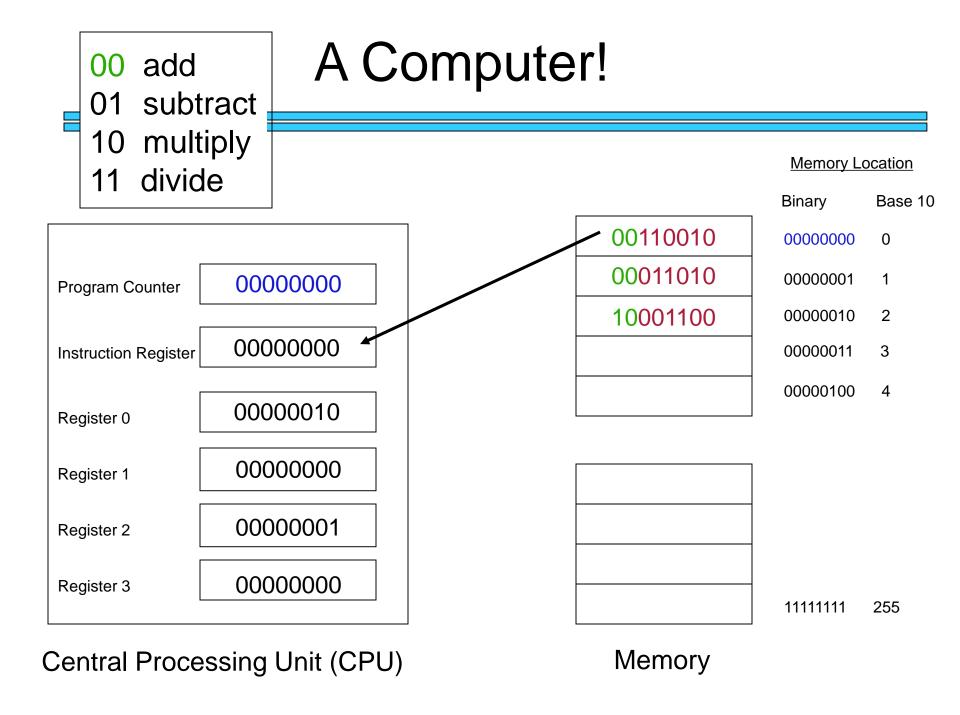
Raca 10

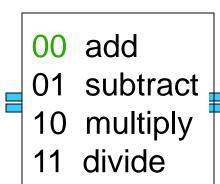
Rinary

Central Processing Unit (CPU)

Memory







#### A Computer!

Program Counter	00000000
Instruction Register	00110010
Register 0	00000010
Register 1	00000000
Register 2	0000001
Register 3	00000000

	Dillary	base 10
00110010	00000000	0
00011010	00000001	1
10001100	00000010	2
	00000011	3
	00000100	4
	l	
	11111111	255

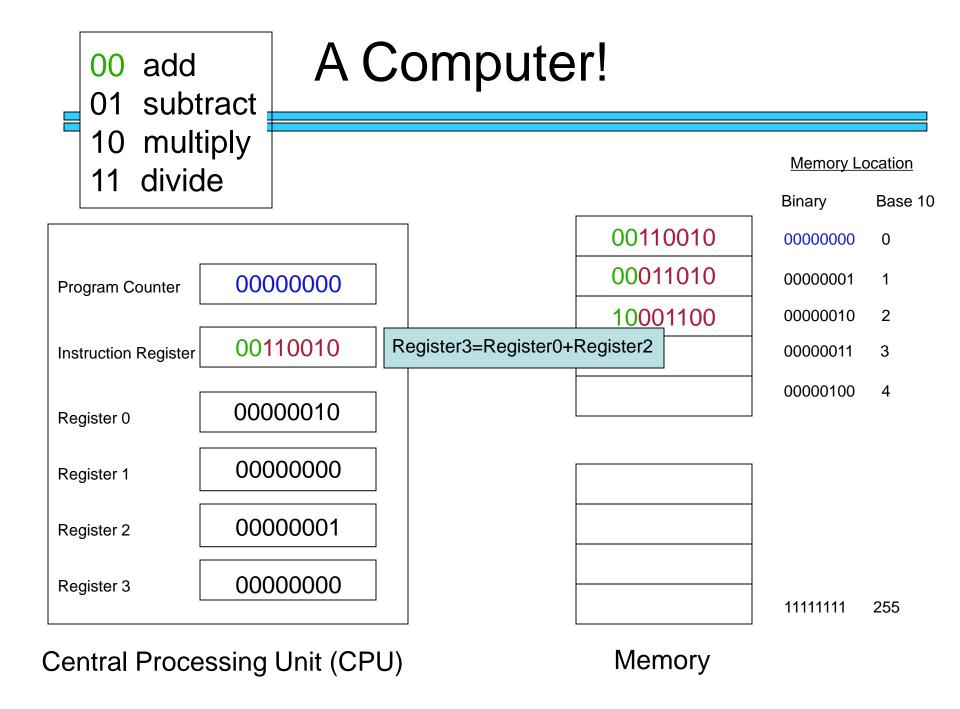
**Memory Location** 

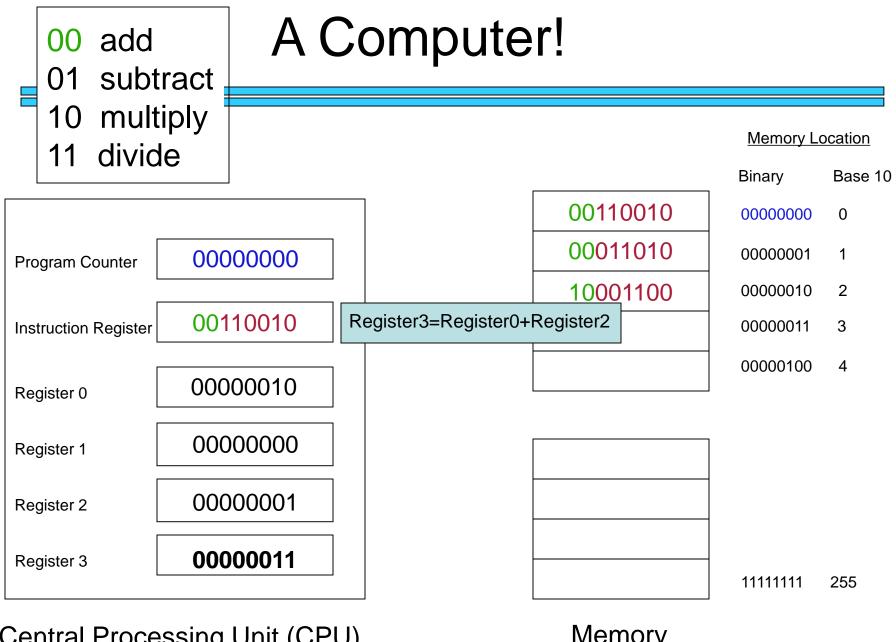
Base 10

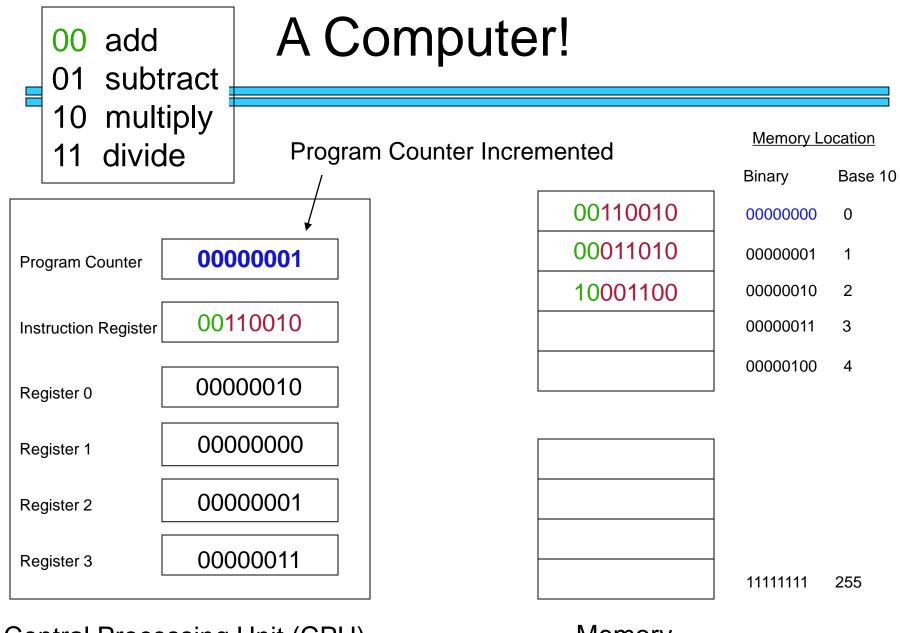
**Binary** 

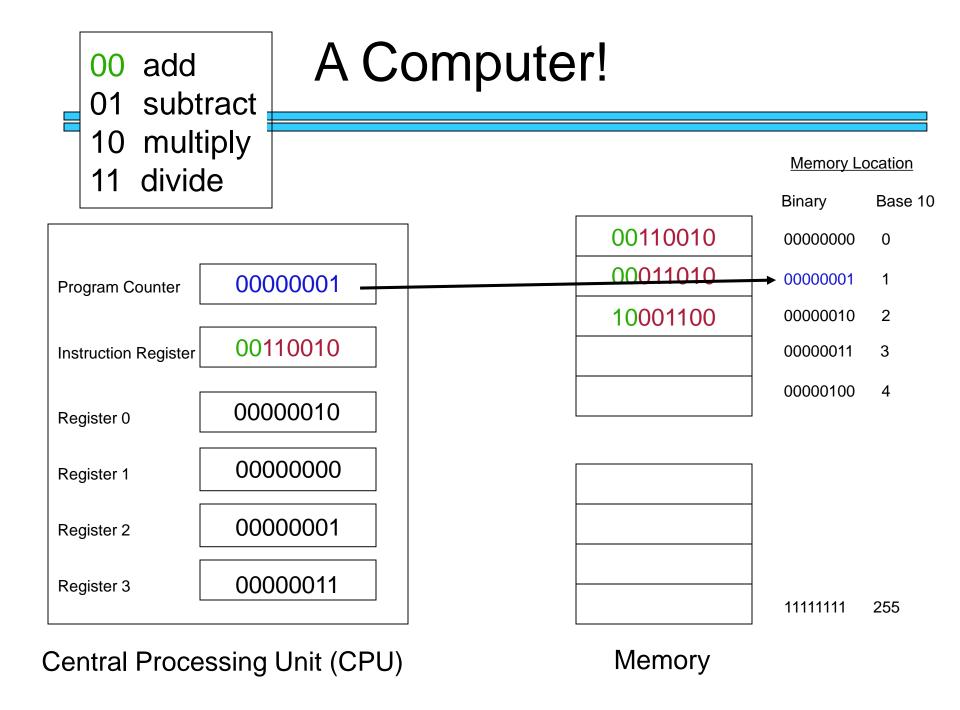
Central Processing Unit (CPU)

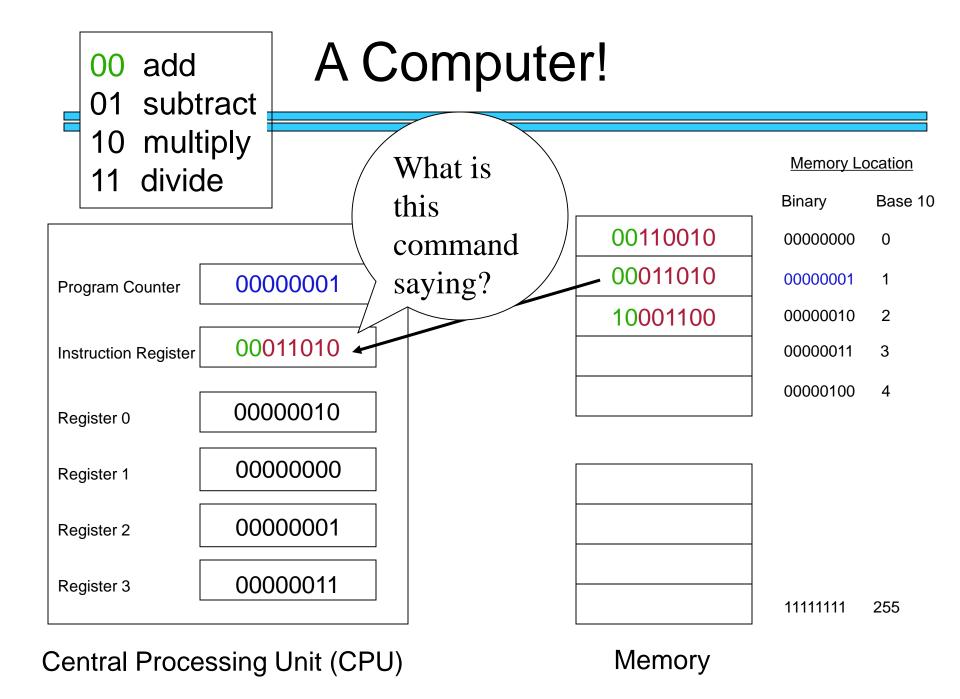
Memory

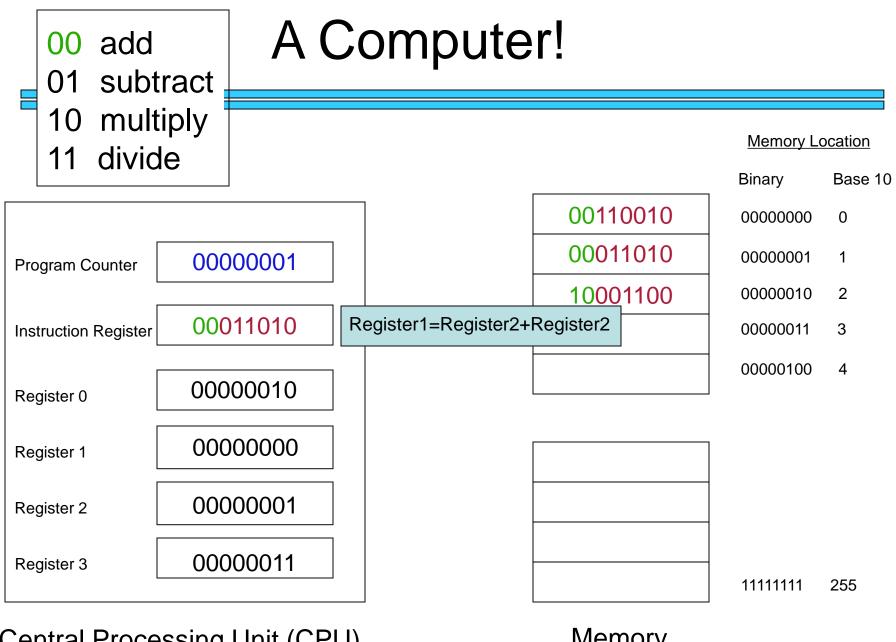


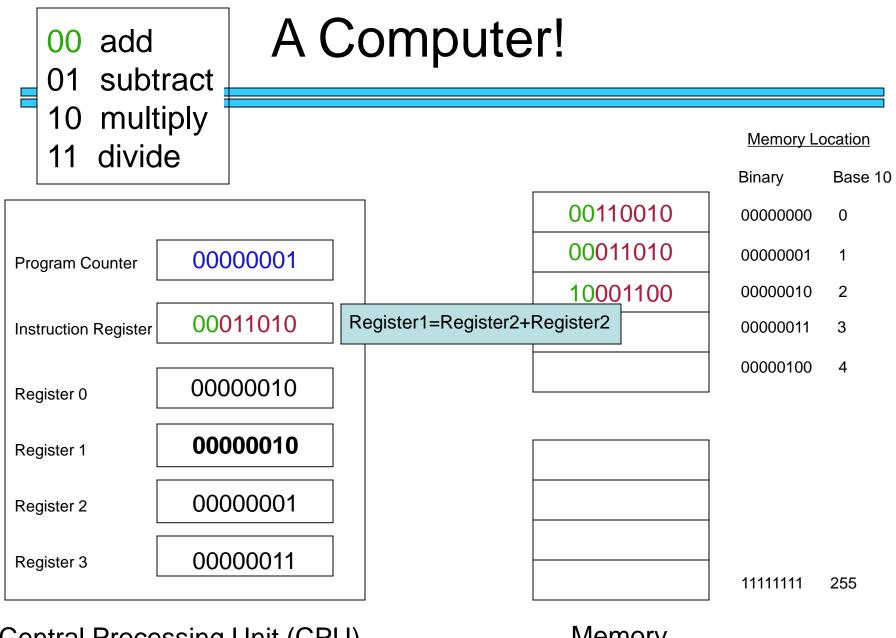


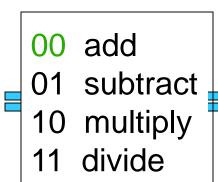












## A Computer!

Program Counter	0000001
Instruction Register	00011010
Register 0	0000010
Register 1	0000010
Register 2	0000001
Register 3	00000011

	Diriary	Dasc 10
00110010	00000000	0
00011010	00000001	1
10001100	00000010	2
	00000011	3
	00000100	4

**Memory Location** 

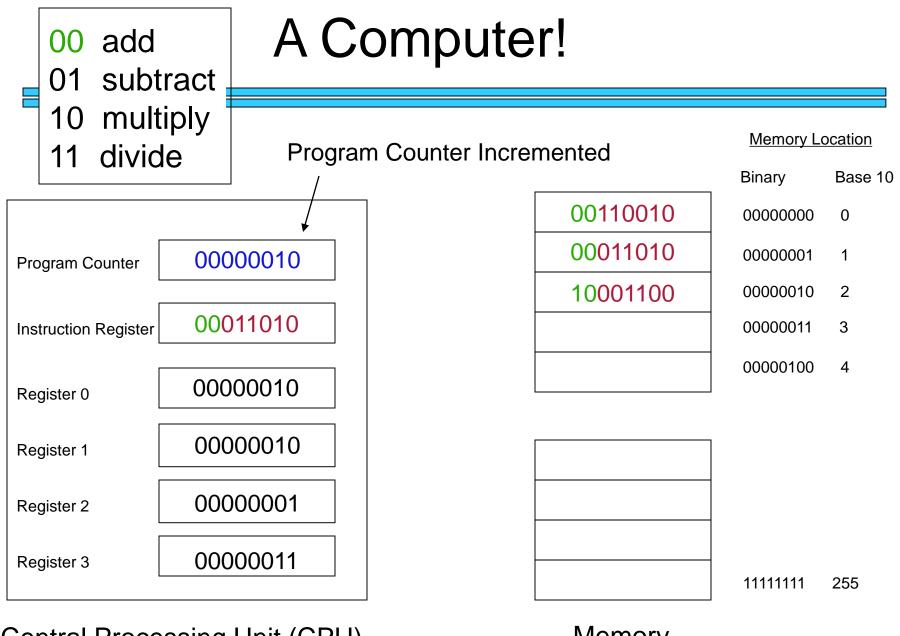
Base 10

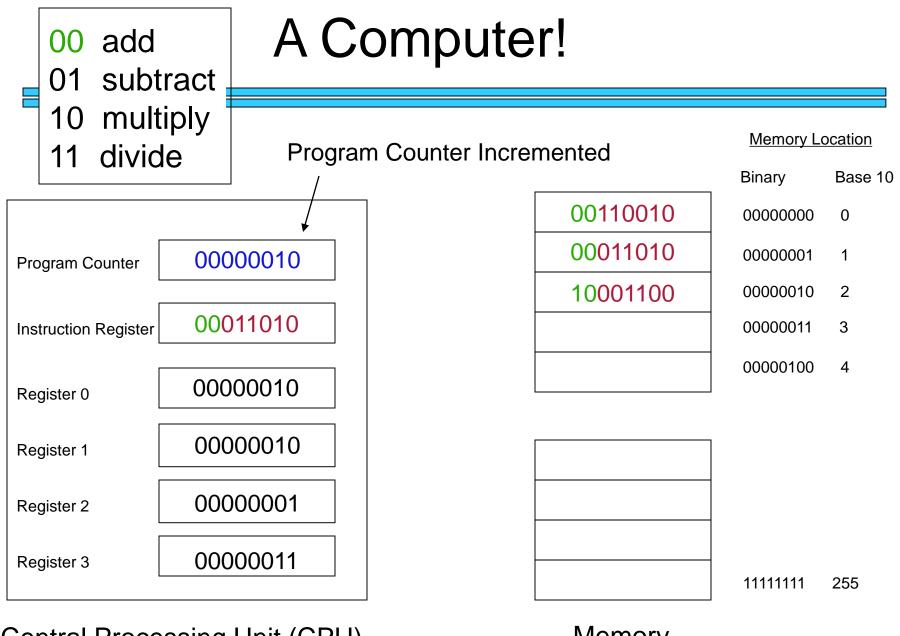
**Binary** 

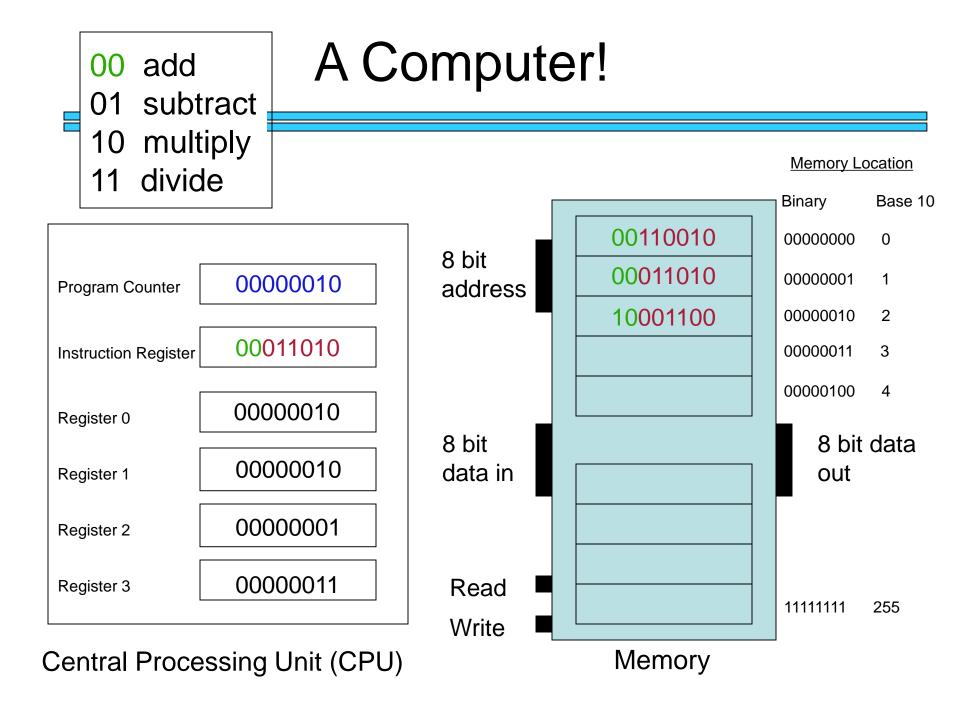
11111111

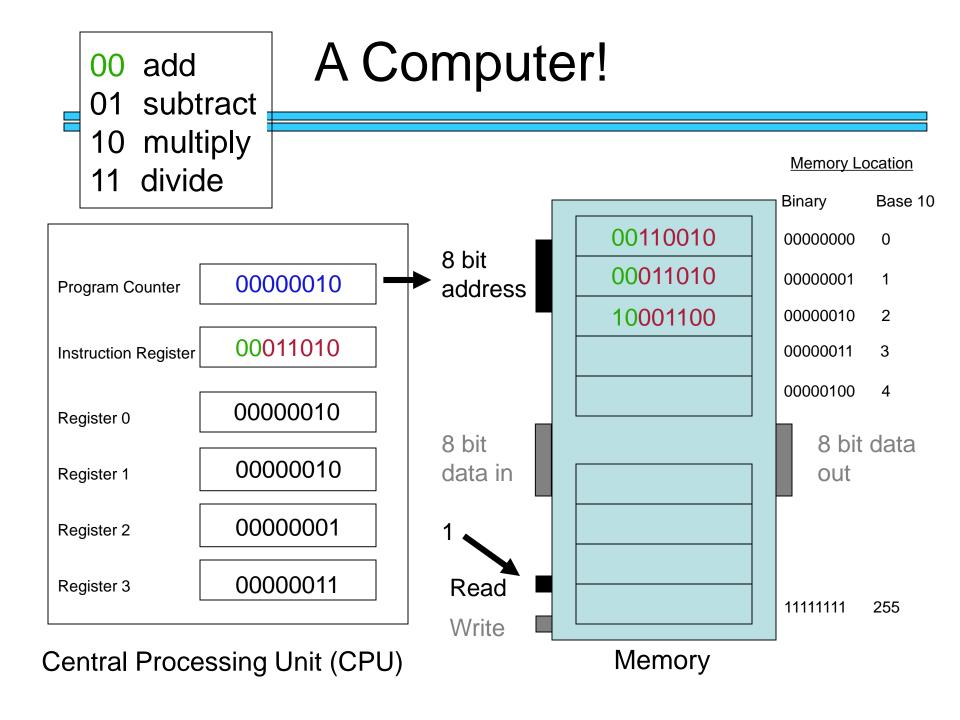
255

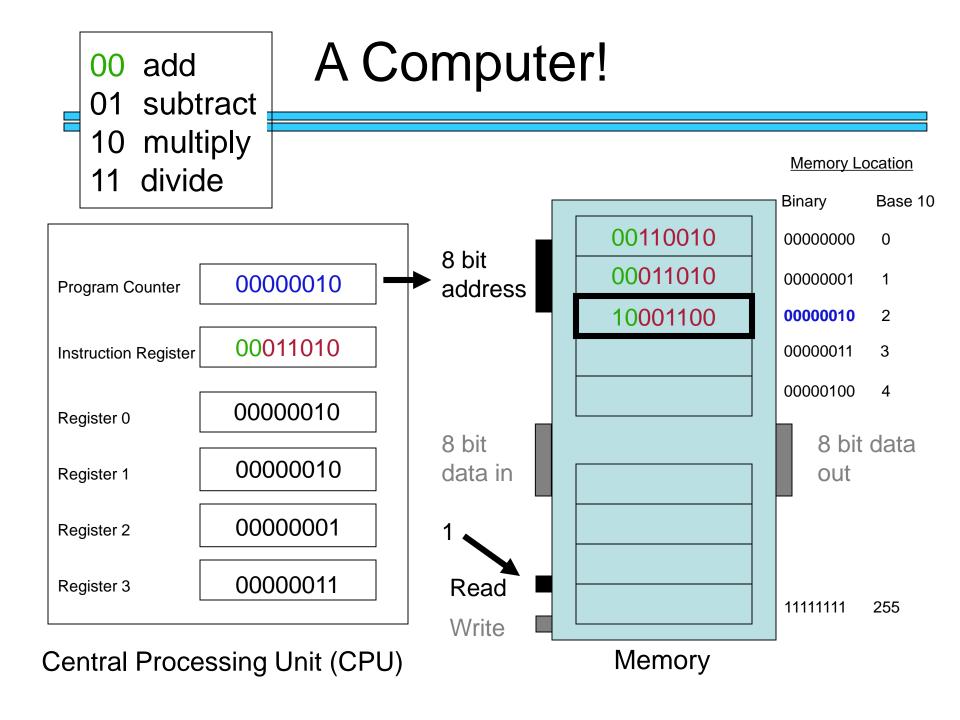
Central Processing Unit (CPU)

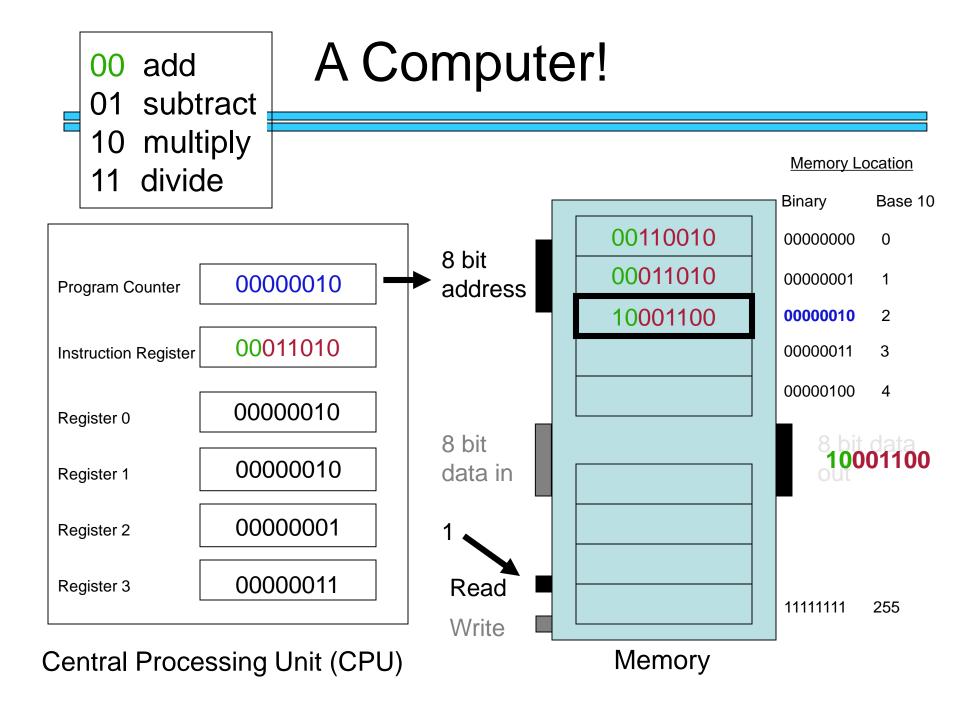


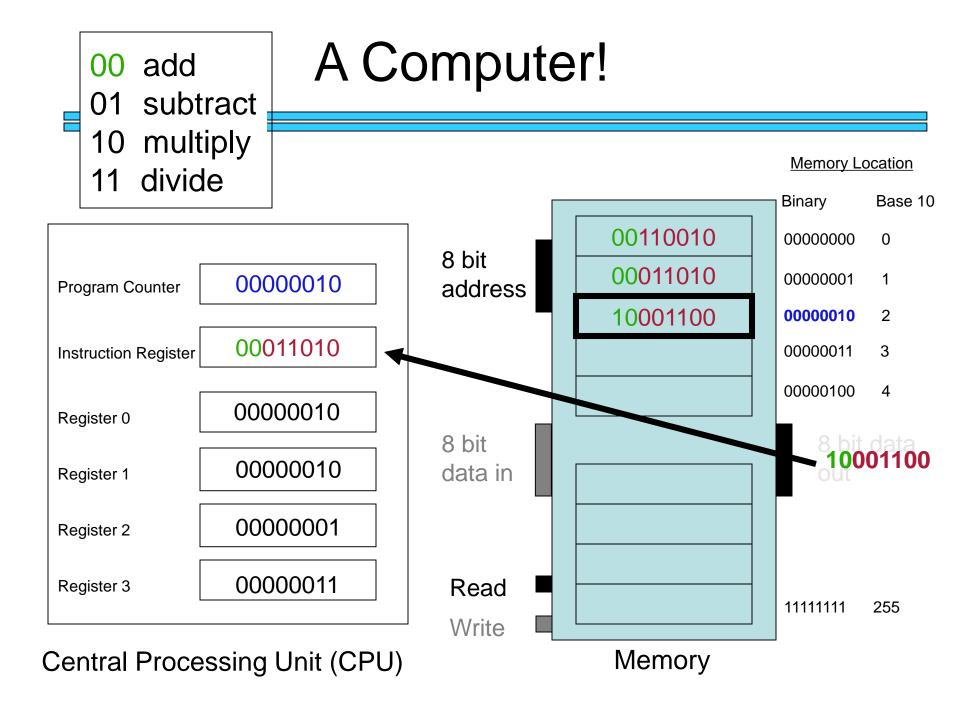


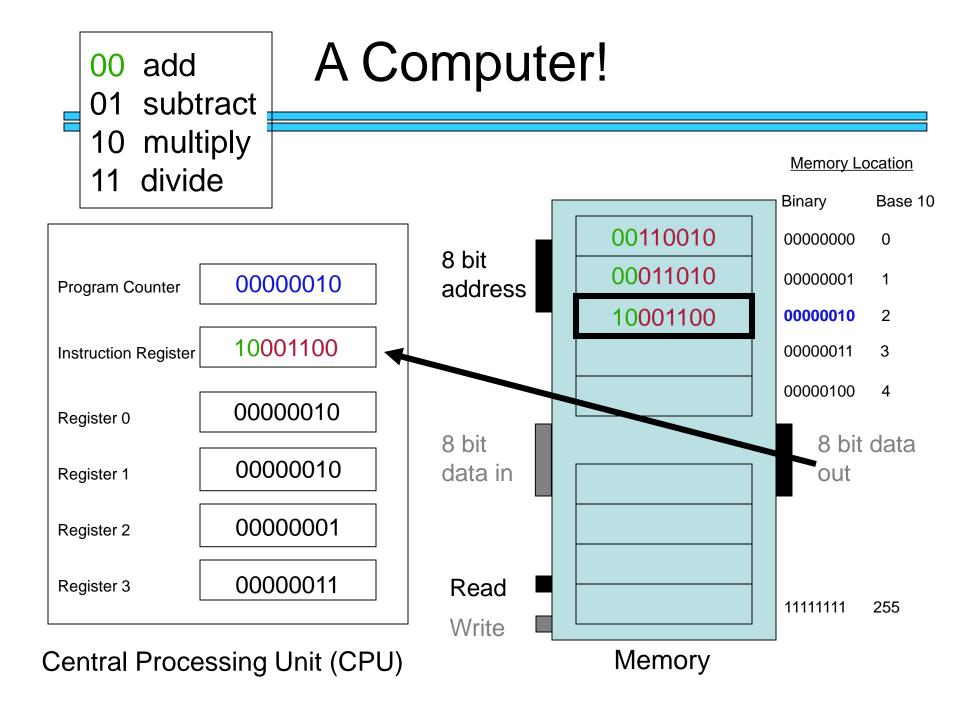


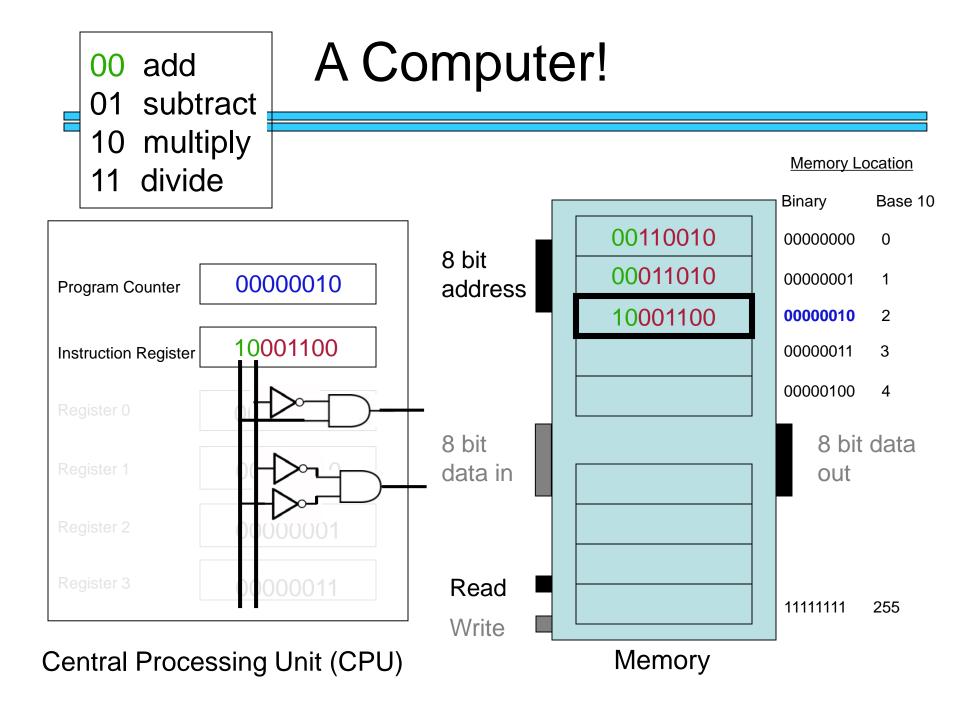


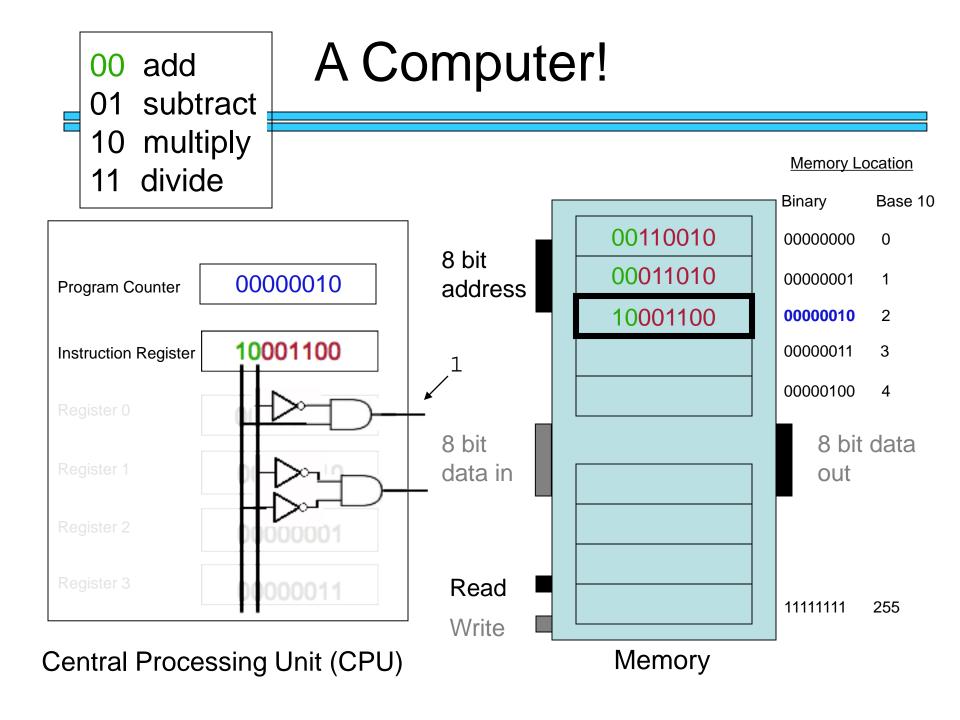












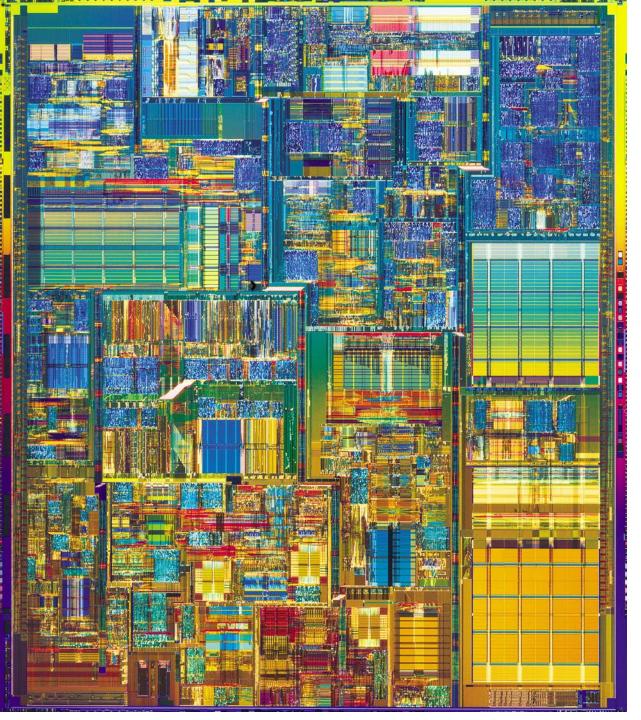
## The von Neumann "architecture"



John von Neumani

						JOHN V	JII NEU
	C	Ripple-carry Multiplier, Registers, et CPU entral processing unit	P		Lots of I	RAM m access memory	
of fast registers	r0 [ r1 [ r2 [		Program Counter  Instruction Register	arge but slow memory		00110010 00011010 10001100	

Small number



2006
Intel Core 2 Duo
3 GHz clock
64-bit processor
291 million transistors
65 nm wires





It doesn't look all that fast to me!

