MOST®

Media **O**riented **S**ystems **T**ransport

Multimedia and Control Networking Technology

MOST150 oPHY Automotive Physical Layer Sub-Specification

Rev. 1.1

05/2010

MOSTCO CONFIDENTIAL

See page 3 for the terms of disclosure

Legal Notice

COPYRIGHT

LICENSE DISCLAIMER

Nothing on any MOST Cooperation Web Site, or in any MOST Cooperation document, shall be construed as conferring any license under any of the MOST Cooperation or its members or any third party's intellectual property rights, whether by estoppel, implication, or otherwise.

CONTENT AND LIABILITY DISCLAIMER

MOST Cooperation or its members shall not be responsible for any errors or omissions contained at any MOST Cooperation Web Site, or in any MOST Cooperation document, and reserves the right to make changes without notice. Accordingly, all MOST Cooperation and third party information is provided "AS IS". In addition, MOST Cooperation or its members are not responsible for the content of any other Web Site linked to any MOST Cooperation Web Site. Links are provided as Internet navigation tools only.

MOST COOPERATION AND ITS MEMBERS DISCLAIM ALL WARRANTIES WITH REGARD TO THE INFORMATION (INCLUDING ANY SOFTWARE) PROVIDED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT. Some jurisdictions do not allow the exclusion of implied warranties, so the above exclusion may not apply to you.

In no event shall MOST Cooperation or its members be liable for any damages whatsoever, and in particular MOST Cooperation or its members shall not be liable for special, indirect, consequential, or incidental damages, or damages for lost profits, loss of revenue, or loss of use, arising out of or related to any MOST Cooperation Web Site, any MOST Cooperation document, or the information contained in it, whether such damages arise in contract, negligence, tort, under statute, in equity, at law or otherwise.

FEEDBACK INFORMATION

Any information provided to MOST Cooperation in connection with any MOST Cooperation Web Site, or any MOST Cooperation document, shall be provided by the submitter and received by MOST Cooperation on a non-confidential basis. MOST Cooperation shall be free to use such information on an unrestricted basis.

TRADEMARKS

MOST Cooperation and its members prohibit the unauthorized use of any of their trademarks. MOST Cooperation specifically prohibits the use of the MOST Cooperation LOGO unless the use is approved by the Steering Committee of MOST Cooperation.

SUPPORT AND FURTHER INFORMATION

For more information on the MOST technology, please contact:

MOST Cooperation
Administration
Bannwaldallee 48
D-76185 Karlsruhe
Germany

Phone: (+49) (0) 721 966 50 00
E-mail: contact@mostcooperation.com
Web: www.mostcooperation.com

This Specification is Confidential Information of the MOST Cooperation. It may only be disclosed to member companies. Member companies wishing to discuss these Specifications with suppliers or other third parties must ensure that a commercially standard form of non-disclosure agreement has been previously executed by the party receiving such Specifications. Use of these Specifications may only be for purposes for which they are intended by the MOST Cooperation. Unauthorized use or disclosure is a violation of law.

Contents

1 Bibliography

Number	Document
[1]	MOST Specification Rev 3.0
[2]	MOST Physical Layer Basic Specification Rev. 1.0
[3]	Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits (TIA/EIA-644-A-2001)
[4]	Interface Standard for Nominal 3 V / 3.3 V Supply Digital Integrated Circuits (JEDEC No. JESD8C.01)
[5]	Safety of Optical Fiber Communication Systems (IEC 60825-2)

Table 1-1 Bibliography

2 Document History

Changes Rev. 1.0 to Rev. 1.1

Change Ref.	Section	Changes
1V1_001	4.3	Table 4-1: Consider termination at SP1 & SP4
1V1_002	6.1	Optical Output Power at SP2 changed: -8,5dBm
1V1_003	6.1, 6.2	Footnote adapted: Pigtail loss removed for integrated pigtail.
1V1_004	6.2.1.1	Undershoot mask adapted.
1V1_005	7.3.1	Correlation of on state parameters detailed (at 7.3.1.g)): "When being supplied with … *and activate SP2 output*."
1V1_006	7.3.1	Figure 7-1adapted: split in 4 sections: OnReset, OnSignal and OffReset, OffSignal
1V1_007	7.3.2	Table 7-3 changed "Parameter PON3 to STATUS falling" to "Delay to STATUS falling" and "Signal off to STATUS rising" to "Delay to STATUS rising"
1V1_008	7.3.2	OEC power-off delay t_{OFF4} expanded to 1ms (formerly: 10 µs)
1V1_009	10.1, 10.2, 11.1	Referencing to drawings without any versioning (version, date)! Sentence added: up-to-date drawings have to be used
1V1_010	11.2	Sections added: Optical Attenuation of ECU Harness and inline connector

Revision 1.0

Revision	Changes
1.0	First issue (October 03, 2008)
0.9	First published draft (January 24, 2008)

3 Terminology and Abbreviations

b_0: the optical signal level when a logic zero is being transmitted

b_1: the optical signal level when a logic one is being transmitted

DC Adaptive Coding (DCA): coding method used for MOST150 oPHY Automotive network

Digital Sum Value (DSV): accumulated DC offset contained in the data

ECU: electronic control unit

EOC: electrical to optical converter

FOR: fiber optic receiver

FOT: fiber optic transceiver, consisting of a paired FOR and FOX

FOX: fiber optic transmitter

Frequency Reference: A device, usually crystal controlled, that provides an accurate and low drift frequency standard for the NIC and network timing

NA: numerical aperture

Network Frame Rate (Fs): The frequency at which frames are started on the MOST150 oPHY Automotive network

NIC: network interface controller

OEC: optical to electrical converter

PLL: phase locked loop

POF: polymer (plastic) optical fiber

RMS: root mean square

RX Data: MOST150 oPHY Automotive encoded digital bitstream being received

TX Data: MOST150 oPHY Automotive encoded digital bitstream being transmitted

UI: unit interval (see section 4.2.2)

This sub-specification references additional terms in [2]. Abbreviations that are defined in that specification are also valid here.

3.1 Usage of Expressions

The following table covers usage of expressions:

Expression	Meaning
Shall	Mandatory provision to maintain compliance.
Must	
Shall Not	Prohibition whose violation results in non-compliance
Must Not	
Should	Recommended but not mandatory.
May	Feature might or might not be present, at the option of the implementer, and has no effect on compliance.
Can	

Table 3-1: Meanings of Expressions

3.2 Resolution of Conflicts

If there are any conflicts between the textual information presented in this document and the corresponding figures, the text shall have priority in resolving the conflict.

3.3 Logic Terminology

The following tables serve to clarify the electrical logic descriptions used in this specification.

3.3.1 Single-Ended Low Voltage Digital Signals

The following table relates the words used in this document to the parameters defined in the JEDEC specification [4]. These words are used to describe the logic states of signals **/RST** and **STATUS**.

Expression	Corresponding JEDEC Parameter
Low	V_{OL}
Logic 0	
0	
Zero	
High	V_{OH}
Logic 1	
1	
One	

Table 3-2: Meaning of Logic Expressions for Single-Ended Signals

3.3.2 Differential LVDS Signals

This document does not precisely follow the conventions shown in the TIA/EIA specification [3] because that document labels device output terminals A and B while this specification uses a P and an N to denote the two terminals of the LVDS signal. The following table explains the expressions used to describe the logic states of the LVDS signals and follows the intent of the wording in the TIA/EIA specification.

Expression	Corresponding TIA/EIA Description
Low	The P terminal shall be negative with respect to the N terminal for a binary 0 state.
Logic 0	
0	
Zero	
High	The P terminal shall be positive with respect to the N terminal for a binary 1 state.
Logic 1	
1	
One	

Table 3-3: Meaning of Logic Expressions for LVDS Signals

The paired P and N LVDS signals are called a bus. The TIA/EIA specification only defines logic levels for a two-state bus. Since some of the devices specified in this document use a tri-state LVDS interface, the following table defines some additional expressions:

Expression	Corresponding Description
Disabled	The P and N terminals are in a high impedance state. Small leakage currents may exist which can cause an indeterminate voltage on the line/load.
Off	
Enabled	Both the P and the N terminals are driving the line/load. The outputs shall be at valid LVDS logic levels provided the input data is valid.
On	
Valid LVDS Signal	Toggling data or a Zero with LVDS voltage levels.

Table 3-4: Meaning of Expressions for LVDS Bus States

4 General Network Parameters

4.1 Overview

This document describes the physical parameters and limits required to guarantee operation of the MOST150 oPHY Automotive network. This sub-specification references terms and measurement methods defined in [2].

4.2 Network Coding

The following sections describe a technique of encoding digital data called DCA coding. This information is presented in order to assure a better understanding of the network but DCA coding is not a part of the physical layer specification [2].

4.2.1 Pulse Characteristics

MOST150 traffic is scrambled and encoded using DCA coding, resulting in a data-stream that contains timing information and is DC free. Data pulses range from 2 UI to 6 UI yielding 5 different pulse widths, as shown in Figure 4-1.

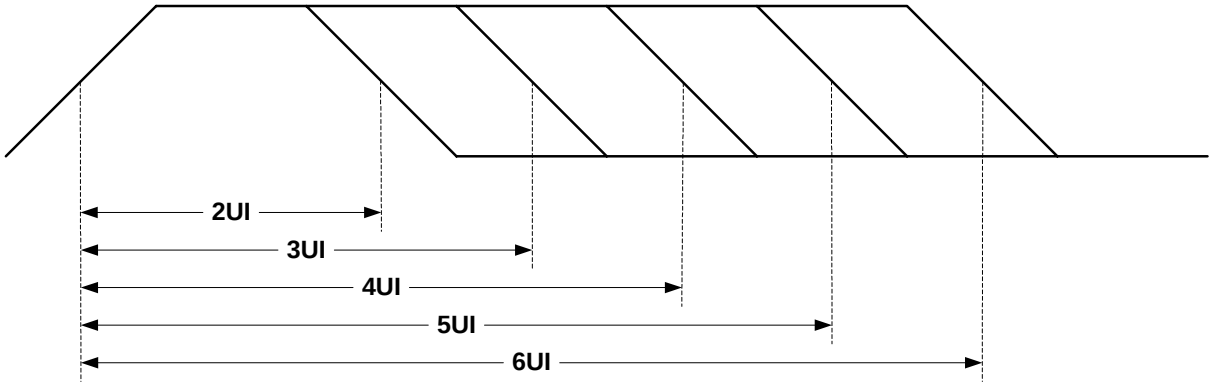


Figure 4-1: Allowable Pulse Widths When Using DCA Coding

4.2.2 Unit Interval Definition

The UI width calculation is shown in the following, Equation 4-1.

$$UI = \frac{1}{Fs * 2 * BPF}$$

Equation 4-1: Unit Interval Calculation

For MOST150, there are 3072 Bits Per Frame (BPF). Using the above formula for a frame rate of 48.000 kHz will result in a Unit Interval of 3.391 ns. A frame rate of 44.100 kHz will have a Unit Interval of 3.691 ns.

4.2.3 DC Balance

DCA coding is inherently DC-free. However, short term imbalances in offset are required for data transmission. These imbalances are tracked with a running total called the Digital Sum Value (DSV).

The DSV is calculated by incrementing the sum for every UI where the data is high, and decrementing the sum for every UI where the data is low. The calculation for DSV is illustrated in Figure 4-2.

Dynamic properties of DCA coding:

- The DSV is periodically driven to zero at least once per frame.
- The range of DSV values in a valid DCA stream are {-5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5}.
- The shortest DCA period is 4 UI.
- The longest DCA period is 10 UI.
- The data stream is guaranteed to have a period of 10 UI at least once per frame.
    - These 10 UI periods can either be made of pulses that are 6 UI high/low with 4 UI low/high, or 5 UI high/low with 5 UI low/high.

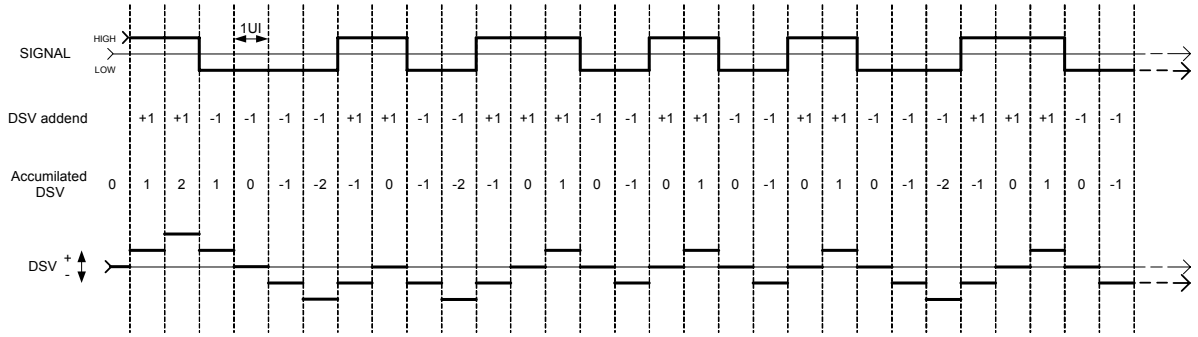


Figure 4-2: DSV Calculation

4.3 Specification Point Details

Specification point locations and details are shown in the following table and figure. Typically an Optical Pigtail, a short piece of fiber or a light pipe, connects the FOR or FOX to the device optical connector. The Optical Pigtail can cause some power loss between the converter and the device optical connector. For more information about the device optical connector, see section 11.

Specification Point	Location	Interface
SP1	EOC electrical input pins including termination	LVDS
SP2	End face of optical contact of device optical connector	Radiated optical
SP3	End face of optical contact of device optical connector	Coupled optical
SP4	OEC electrical output pins including termination	LVDS

Table 4-1: Specification Point Locations and Interfaces

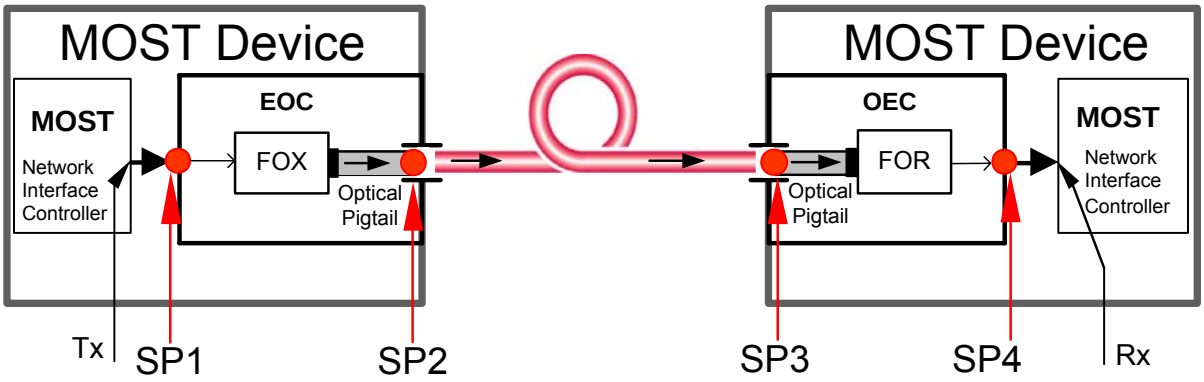


Figure 4-3: Location of Specification Points

5 Models and Measurement Methods

The following models and methods are used as the basis for measurements in this sub-specification.

5.1 Golden PLL

The golden PLL describes the required worst-case jitter performance of a NIC, and is used to form receiver eye-diagrams. The golden PLL must reference to the positive edge of the signal. The transfer function is a low pass filter with unity gain at DC, but for practicality of measurements is specified for 10 Hz and above.

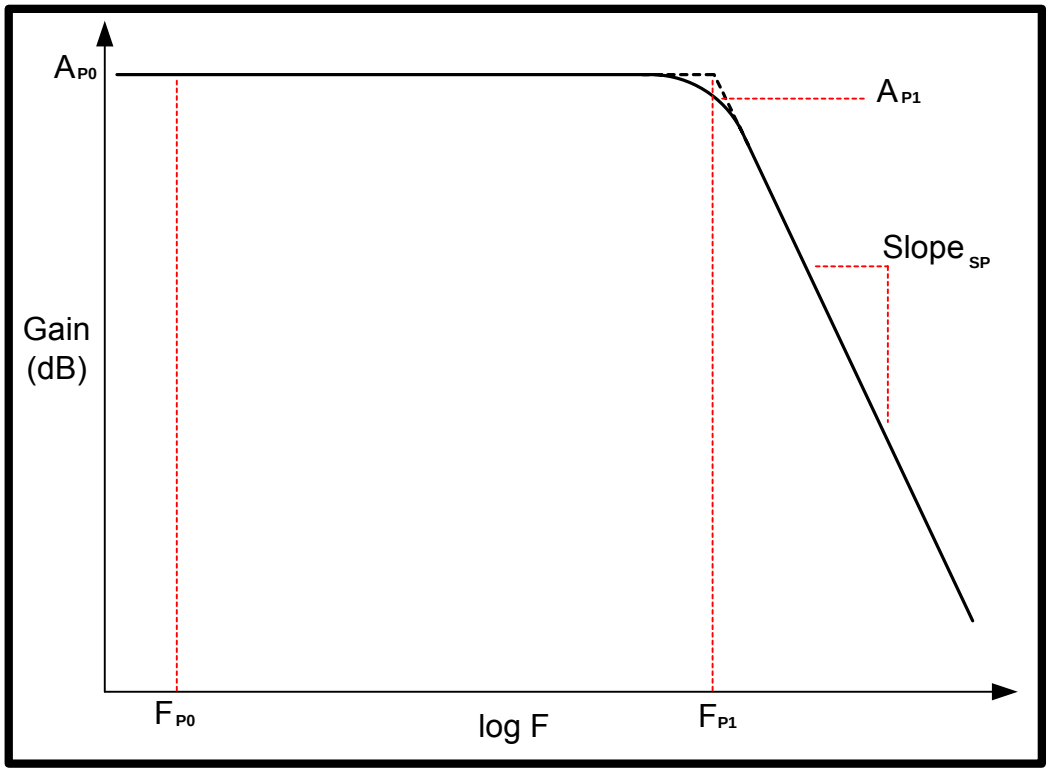


Figure 5-1: Golden PLL Transfer Function

Parameter	Value	Unit
A_{P0}	0	dB
F_{P0}	10	Hz
A_{P1}	-3	dB
F_{P1}	125	kHz
$Slope_{SP}$	-20	dB/dec

Table 5-1: Golden PLL Specifications

5.2 Jitter Filter

The jitter filter describes the worst-case jitter transfer function of a NIC, and is used to calculate transferred jitter along the link. The transfer function is a low pass filter with unity gain at DC, but for practicality of measurements is specified for 10 Hz and above.

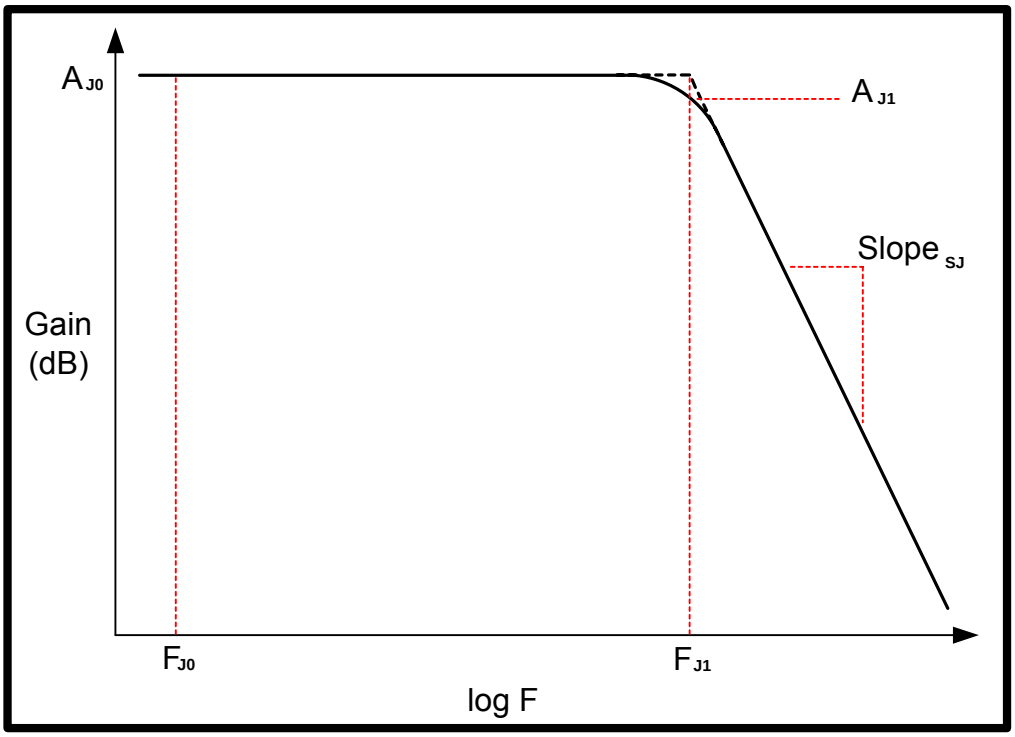


Figure 5-2: Jitter Filter Response

Parameter	Value	Unit
A_{J0}	0	dB
F_{J0}	10	Hz
A_{J1}	-3	dB
F_{J1}	200	kHz
$Slope_{SJ}$	-20	dB/dec

Table 5-2: Jitter Filter Specifications

5.3 Test Pattern

The MOST150 Test Pattern shall be used for the following measurements:

- Optical signal level detection measurements
- Optical overshoot and undershoot measurements
- All eye-diagrams

Description Code	File Name
MOST150 Test Pattern	*MOST150_Stress_Pattern-1v0.pat*
	Files are available on www.mostcooperation.com

Table 5-3: Description of MOST150 Test Pattern

5.4 Optical Signal Level Detection

Measurement of the optical logic levels (b_0 and b_1) is required to calculate the extinction ratio and to determine the placement of the SP2 and SP3 eye masks. The vertical amplitude of the SP2 and SP3 eye masks is scaled relative to the b_0 and b_1 levels.

5.4.1 Measurement Region

The b_1 level is measured during a high 5 or 6 UI pulse while the b_0 level is measured during a low 5 or 6 UI pulse. The transient regions are the areas of the pulse where the signal is not settled enough to yield a repeatable measurement for b_1 or b_0. The b_1 and b_0 values are the statistical mean of the high and low signal amplitude respectively during the interval defined in Figure 5-3 and Table 5-4.

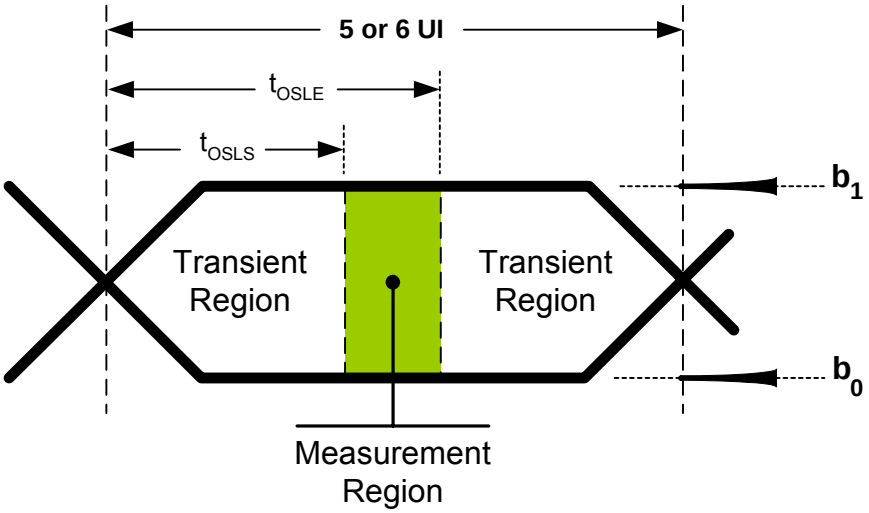


Figure 5-3: Optical Signal Level Test Eye

Measurement Region	Value	Unit
t_{OSLS}	2.500	UI
t_{OSLE}	4.000	UI

Table 5-4: Optical Signal Level Measurement Interval

6 Link Specifications

This specification utilizes eye pattern diagrams and mask templates to validate the serial data link. A high-quality signal with low jitter and distortion will show a large eye opening, which can be compared to a standardized mask, placed in the center of the eye for comparison (a diamond shape in the center of the eye). The mask is designed such that a good signal will not touch the mask at any location. A pattern that touches the mask must be recorded as a failure and logged by the test equipment automatically. Signals with slow rise times, low amplitudes, jitter, or pulse width variations will show up as closure in the eye diagram. Signals with excessively high amplitudes will touch the horizontal bars above and below the eye diagram and also cause a failure to be recorded.

All the components along the link must operate with a Bit Error Rate (BER) lower than 10^{-9}. Consequently, all of the mask violation parameters have been specified with that goal in mind.

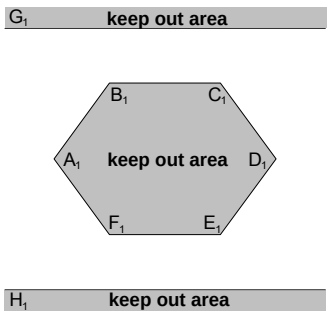
6.1 Specification Point SP1

The signal at SP1 must meet the requirements in Table 6-1 and must not touch the "Keep-Out" areas of the mask. Refer to sections 7.1, 8.4, and 9 for operating conditions and interface standards.

Link Quality SP1	Symbol	Condition	Min.	Typ.	Max.	Unit
Transferred Jitter	Jtr_1	1)	-	-	50	ps RMS
Eye-Mask	A_1… H_1	2)	-	-	-	-

Parameter	Amplitude (mV)	Timing (UI)
A_1	0	0.075
B_1	100	0.325
C_1	100	0.675
D_1	0	0.925
E_1	-100	0.675
F_1	-100	0.325
G_1	636	-
H_1	-636	-

Eye-mask



Notes:

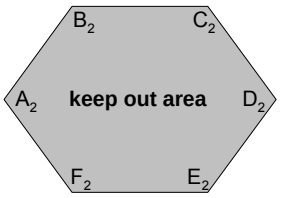
1) Using the Jitter-Filter specified in section 5.2.
2) Using the Golden PLL specified in section 5.1.

Table 6-1: Link Quality Parameters of SP1

6.2 Specification Point SP2

The signal at SP2 must meet the requirements in Table 6-2 and must not touch the "Keep-Out" area of the mask. Refer to sections 7.1, 8.4, and 9 for operating conditions and interface standards.

Link Quality SP2	Symbol	Condition	Min.	Typ.	Max.	Unit
Center wavelength	λc_2	1)	635	650	675	nm
Spectral Width (RMS)	$\sigma\lambda_2$	2)	-	-	17	nm
Average optical output power	P_{opt2}	3), 4), 5)	-8.500	-	-1.500	dBm
Extinction ratio	r_{e2}	6), 7)	10	-	-	dB
Transition times (rise or fall)	t_{tr2}	8)	-	-	0.500	UI
Transferred Jitter	Jtr_2	9)	-	-	112	ps RMS
Eye-Mask	A_2… F_2	6), 10)	-	-	-	-

Parameter	Amplitude	Timing (UI)	Eye-mask
A_2	0.5 * (b_1 + b_0)	0.150	
B_2	0.8 * (b_1-b_0) + b_0	0.400	
C_2	0.8 * (b_1-b_0) + b_0	0.600	
D_2	0.5 * (b_1 + b_0)	0.850	
E_2	0.2 * (b_1-b_0) + b_0	0.600	
F_2	0.2 * (b_1-b_0) + b_0	0.400	

Notes:

1) Center wavelength λ_{c2} is given with: $\lambda_{c2} = \frac{\sum_{i=\lambda start}^{i=\lambda end} P_i \lambda_i}{\sum_{i=\lambda start}^{i=\lambda end} P_i}$; $\lambda start = 500nm$, $\lambda end = 800nm$; where P_i is the optical power measured at the wavelength λ_i.

2) Spectral width $\sigma\lambda_2$ is given with: $\sigma\lambda_2 = \sqrt{\frac{\sum_{i=\lambda start}^{i=\lambda end} P_i (\lambda_i - \lambda_{c2})^2}{\sum_{i=\lambda start}^{i=\lambda end} P_i}}$; $\lambda start = 500nm$, $\lambda end = 800nm$;

3) The recommendations of IEC 60825-2 - Part 2: "Safety of Optical Fiber Communication Systems" [5] must be taken into account. Laser Class 1 limits must be met in any circumstance. In failure cases, such as when no data transitions are present at the input of the transmitter, the output must be disabled within a time t_{off2} (defined in Table 7-2).
4) Power within a far field angle of 30° (NA = 0.5) and a diameter of 1.0 mm.
5) Losses through the optical pigtail must be kept below 1.5 dB, except integrated pigtail.
6) Measurement of b_0 and b_1 is specified in section 5.3.
7) $r_{e2} = 10 * \log(b_1 / b_0)$
8) Transition times are measured between the 20% - 80% points.
9) Using the Jitter-Filter specified in section 5.2.
10) Using the Golden PLL specified in section 5.1.

Table 6-2: Link Quality Parameters of SP2

6.2.1 Optical Overshoot and Undershoot

Measurement of the optical overshoot and undershoot is required to ensure proper operation of the optical receiver. The optical pulse shape is tested with a parameterized mask. The mask parameters are based on the measured optical logic levels b_0 and b_1. Optical transmitting devices must produce an optical signal complying with the defined mask, when driven with a compliant electrical signal. Optical receiving devices must produce a compliant electrical output signal, when driven with an optical signal compliant with the relevant mask..

6.2.1.1 Method

Mask amplitude parameters are normalized and are calculated based on the measured b_1 and b_0 levels. Time parameters are specified in units of UI and the origin is defined from the mid point of the rising or falling edge of the signal, as illustrated in Figure 6-1 and Figure 6-2. The signal must not touch the “Keep Out” areas of the masks.

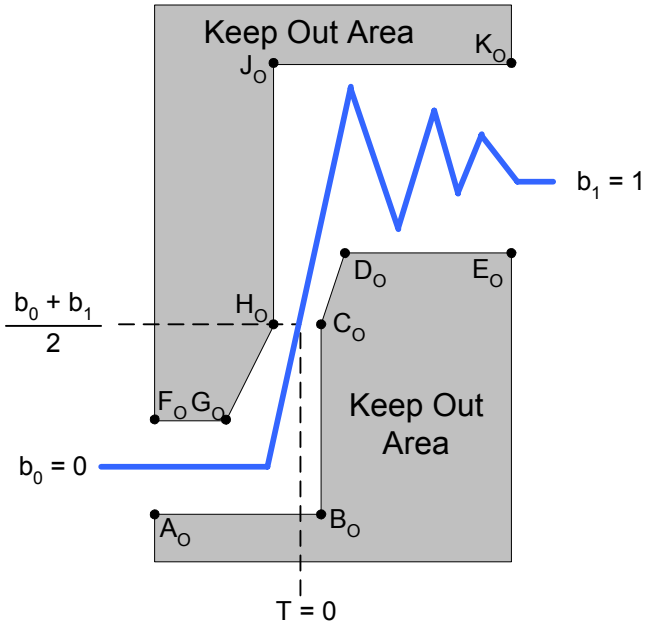


Figure 6-1: SP2 Overshoot Mask

Mask Parameter	Normalized Amplitude	Time (UI)
A_O	-0.200	-0.630
B_O	-0.200	0.100
C_O	0.500	0.100
D_O	0.800	0.350
E_O	0.800	1.370
F_O	0.200	-0.630
G_O	0.200	-0.350
H_O	0.500	-0.100
J_O	1.400	-0.100
K_O	1.400	1.370
Note: All amplitude values are normalized to $b_0 = 0$ and $b_1 = 1$.		

Table 6-3: SP2 Overshoot Mask Parameter Values

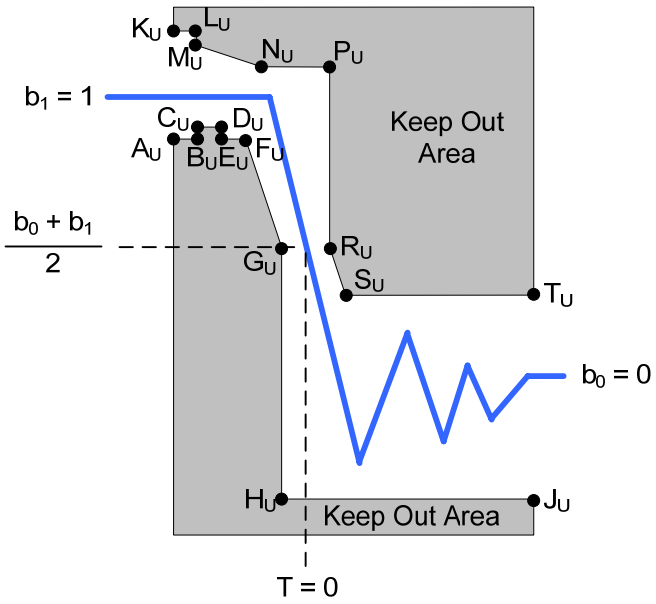


Figure 6-2: SP2 Undershoot Mask

Mask Parameter	Normalized Amplitude (1)	Time (UI) (2)
A_U	0.800	-0.630 - x
B_U	0.800	-0.530 - x
C_U	0.850	-0.530 - x
D_U	0.850	-0.430
E_U	0.800	-0.430
F_U	0.800	-0.350
G_U	0.500	-0.100
H_U	-0.200	-0.100
J_U	-0.200	1.370
K_U	1.400	-0.630 - x
L_U	1.400	-0.530 - x
M_U	1.340	-0.530 - x
N_U	1.150	-0.220 - x
P_U	1.150	0.100
R_U	0.500	0.100
S_U	0.200	0.350
T_U	0.200	1.370

Notes:
1) All amplitude values are normalized to $b_0 = 0$ and $b_1 = 1$.
2) The locations of A_U, B_U, C_U, K_U, L_U, and M_U on the time-axis depend on the nominal pulse width to be measured. In the table this dependency is expressed by the parameter x, which is calculated by: x = nominal pulse width in UI - 2. (For 2UI, x = 0; for 6UI, x = 4)

Table 6-4: SP2 Undershoot Mask Parameter Values

6.3 Specification Point SP3

The stimuli for the receiver must be calculated by SP2 worst case conditions and the transfer function of the POF in Table 6-5. Refer to sections 7.1, 8.4, and 9 for operating conditions and interface standards. The signal at SP3 must meet the requirements in Table 6-6.

	Condition	Mathematical representation of the POF Link
3 dB Bandwidth depending on L_{POF}	1), 2), 3)	$B_{3dB} = 1009 \cdot 10^6 \cdot L_{POF}^{-0.8747}$
Standard deviation of Gaussian transfer function	3)	$\sigma = 0.132 / B_{3dB}$
POF transfer function	4)	$\lvert H \rvert_{POF}(f) = \exp(-2(\pi\sigma f)^2)$
1) For calculation of SP3 stimulus minimum and maximum L_{POF} shall be considered. 2) For maximum length of POF refer to chapter 8.3.1. 3) L_{POF} is the length of the fiber in meter. The dimension of B_{3dB} is Hz 4) Valid for 1mm polymer optical step index fiber with launch condition NA 0.5.		

Table 6-5: Transfer function of optical fiber

Link Quality SP3	Symbol	Condition	Min.	Typ.	Max.	Unit
Center wavelength	λc_3	1)	635	650	675	nm
Spectral Width (RMS)	$\sigma\lambda_3$	2)	-	-	17	nm
Receivable average optical power range for data recovery	P_{opt3}	3), 4), 5), 6), 7)	-22	-	-2	dBm

Notes:

1) Center wavelength λ_{c3} is given with: $\lambda_{c3} = \frac{\sum_{i=\lambda start}^{i=\lambda end} P_i \lambda_i}{\sum_{i=\lambda start}^{i=\lambda end} P_i}$; $\lambda start = 500nm$, $\lambda end = 800nm$; where P_i is the optical power measured at the wavelength λ_i.

2) Spectral width $\sigma\lambda_3$ is given with: $\sigma\lambda_3 = \sqrt{\frac{\sum_{i=\lambda start}^{i=\lambda end} P_i (\lambda_i - \lambda_{c3})^2}{\sum_{i=\lambda start}^{i=\lambda end} P_i}}$; $\lambda start = 500nm$, $\lambda end = 800nm$;

3) The recommendations of IEC 60825-2: 2007 – Part 2: "Safety of Optical Fiber Communication Systems" [5] must be taken into account when measuring SP3.
4) Power within a far field angle of 30° (NA = 0.5) and a diameter of 1.0 mm.
5) Assuming an attenuation of >0.5 dB between SP2 and SP3.
6) Losses through the optical pigtail must be kept below 1.5 dB, except integrated pigtail.
7) Value when the incoming signal has passed the receiving contact end face.

Table 6-6: Link Quality Parameters of SP3

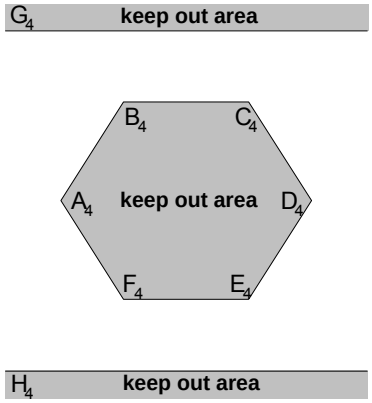
6.4 Specification Point SP4

The signal at SP4 must meet the requirements in Table 6-7 and must not touch the “Keep-Out” areas of the mask. Refer to sections 7.1, 8.4, and 9 for operating conditions and interface standards.

Link Quality SP4	Symbol	Condition	Min.	Typ.	Max.	Unit
Transferred Jitter	Jtr_4	1)	-	-	230	ps RMS
Eye-Mask	A_4…H_4	2), 3), 4)	-	-	-	-

Parameter	Amplitude (mV)	Timing (UI)
A_4	0	0.275
B_4	148	0.425
C_4	148	0.575
D_4	0	0.725
E_4	-148	0.575
F_4	-148	0.425
G_4	636	-
H_4	-636	-

Eye-mask



Notes:

1) Using the Jitter-Filter specified in section 5.2.
2) Using the Golden PLL specified in section 5.1.
3) The mask parameters include tolerances for overshoot and ringing.
4) The steady-state differential voltage must not be less than that specified in [3].

Table 6-7: Link Quality Parameters of SP4

7 Power Up / Power Down

7.1 ECU Requirements

The ECU must provide a stable frequency reference for the NIC, supply power to NIC, EOC and OEC, and provide power supply monitoring circuitry.

- Frequency reference:
  The frequency reference is typically a crystal controlled oscillator or derivative. The requested accuracy is specified in section 9.2.

- Power supply:
  - V_{CCTX}: NIC and EOC supply with a nominal operating range of 3.3V ± 5%, which must be able to be shut down
  - V_{CCRX}: OEC power supply with a nominal operating range of 3.3V ± 5%, which should always be supplied. Due to the recommendation that V_{CCRX} remain powered, it is typically provided by a supply independent from V_{CCTX}.

- Power supply monitoring circuitry:
  The ECU shall provide power supply monitoring circuitry for supervising V_{CCTX} which is specified in section 7.2. The ECU shall connect the active-low reset signal /RST provided by the power supply monitoring circuitry to the /RST inputs of the EOC and the NIC.

7.2 Power Supply Monitoring Circuitry

The power supply monitoring circuitry shall.

- Provide an active-low reset signal, **/RST** that is a valid LVTTL (JESD8C) signal over the power supply range V_{VALID} specified in Table 7-1.
- Set the **/RST** signal to high when the power supply voltage ramps above the threshold, V_T. Switching from low to high shall be delayed by a minimum time of t_{D+} to allow the circuitry in the EOC to stabilize, the LVDS pins of the NIC to be driven, and the local frequency reference to stabilize. Although a maximum time for tD+ is not specified, an implicit maximum value exists due to the required start-up time (light in to light out). Refer to the MOST Specification [1] for more details.
- Set the **/RST** signal to low when the voltage drops below the threshold, V_T. Switching from high to low shall occur within a time of t_{D-}.

/RST Signal	Symbol	Condition	Min	Max	Unit
Supply range for valid logic levels	V_{VALID}		1	3.465	V
Logic switching threshold	V_T		2.970	-	V
Logic 0 to 1 Time Delay	t_{D+}		1	-	ms
Logic 1 to 0 Time Delay	t_{D-}		0	100	µs

Table 7-1: Specifications for /RST Signal Generation

7.3 Optical and Electrical Signal Power State

System optical wakeup and shutdown methods require certain functionality to be built into the EOC and OEC components.

7.3.1 EOC Requirements

The EOC functional requirements are listed below.

a) The EOC must have an LVTTL (JESD8C) reset bar (**/RST**) input pin.
b) The EOC must be capable of performing transition detection at its input. Transition detection is the ability to monitor the input frequency of the signal at SP1 and make a logical decision as to whether the frequency meets the specifications of F_{OFF1} or F_{ON1}.
c) The *Off-State* for the EOC is defined as follows:
   - The EOC must not output optical power above P_{OFF2}.
   - The EOC must perform transition detection at SP1 in order to check for a valid wakeup condition, defined as the input signal frequency being within F_{ON1}.
d) The *On-State* for the EOC is defined as follows:
   - The EOC shall produce an optical output that is compliant with all the SP2 parameters defined in Table 6-2 when being driven by valid SP1 data.
   - The EOC must perform transition detection at SP1 in order to check for a valid shutdown condition, defined as the input signal frequency being within F_{OFF1}.
e) The EOC must not generate any optical signals exceeding P_{OFF2} when being supplied with an operating voltage within $V_{CCTXOFF}$ regardless of the state of the SP1 and **/RST** inputs.
f) The EOC must not generate any optical signals exceeding P_{OFF2} when the **/RST** input is low.
g) When being supplied with an operating voltage within V_{CCTXGR}, the internal circuitry of the EOC shall settle into stable operation with the ability to perform transition detection within a time defined by the minimum value of the parameter t_{D+} and activate SP2 output.
h) When being supplied with an operating voltage within V_{CCTXOR}, the EOC shall settle into operation defined as the *On-State*, within a time t_{ON2} when:
   - The **/RST** input pin is driven high AND
   - The frequency of the SP1 signal is within F_{ON1} (transition detection).
i) When being supplied with an Operating Voltage within V_{CCTXGR}, the EOC shall be capable of performing transition detection and shall enter the *Off-State*, within a time t_{OFF2} when:
   - The **/RST** input pin is driven low OR
   - The frequency of the SP1 signal is within F_{OFF1} (transition detection).
j) While F_{ON1} defines the frequency range where the EOC **must** be on and F_{OFF1} defines the frequency range where the EOC **must** be off, the actual transition points will most likely be in the region between F_{OFF1} max. and F_{ON1} min.

The EOC requirements are summarized in Table 7-2. Refer to Figure 7-1 for more details.

EOC Power State Requirements	Symbol	Condition	Min.	Typ.	Max.	Unit
EOC Operating Voltage Range	V_{CCTXOR}		3.135	3.300	3.465	V
EOC Glitch-Safe Voltage Range	V_{CCTXGR}		2.970	-	3.465	V
EOC Off Voltage Range	$V_{CCTXOFF}$		0	-	1	V
EOC On frequency range at SP1	F_{ON1}	1)	12	-	73.743	MHz
EOC Off frequency range at SP1	F_{OFF1}		0	-	10	kHz
EOC power on delay	t_{ON2}	3)	-	-	100	µs
EOC power off delay	t_{OFF2}		-	-	2	µs
Average optical output power for the *Off-State*	P_{OFF2}	2)	-	-	-50	dBm

Notes:

1) The EOC can still be in the On-State above this frequency.
2) Power within a far field angle of 30° (NA = 0.5) and a diameter of 1.0 mm.
3) See section 7.3.1.h)

Table 7-2: EOC Power State Requirements

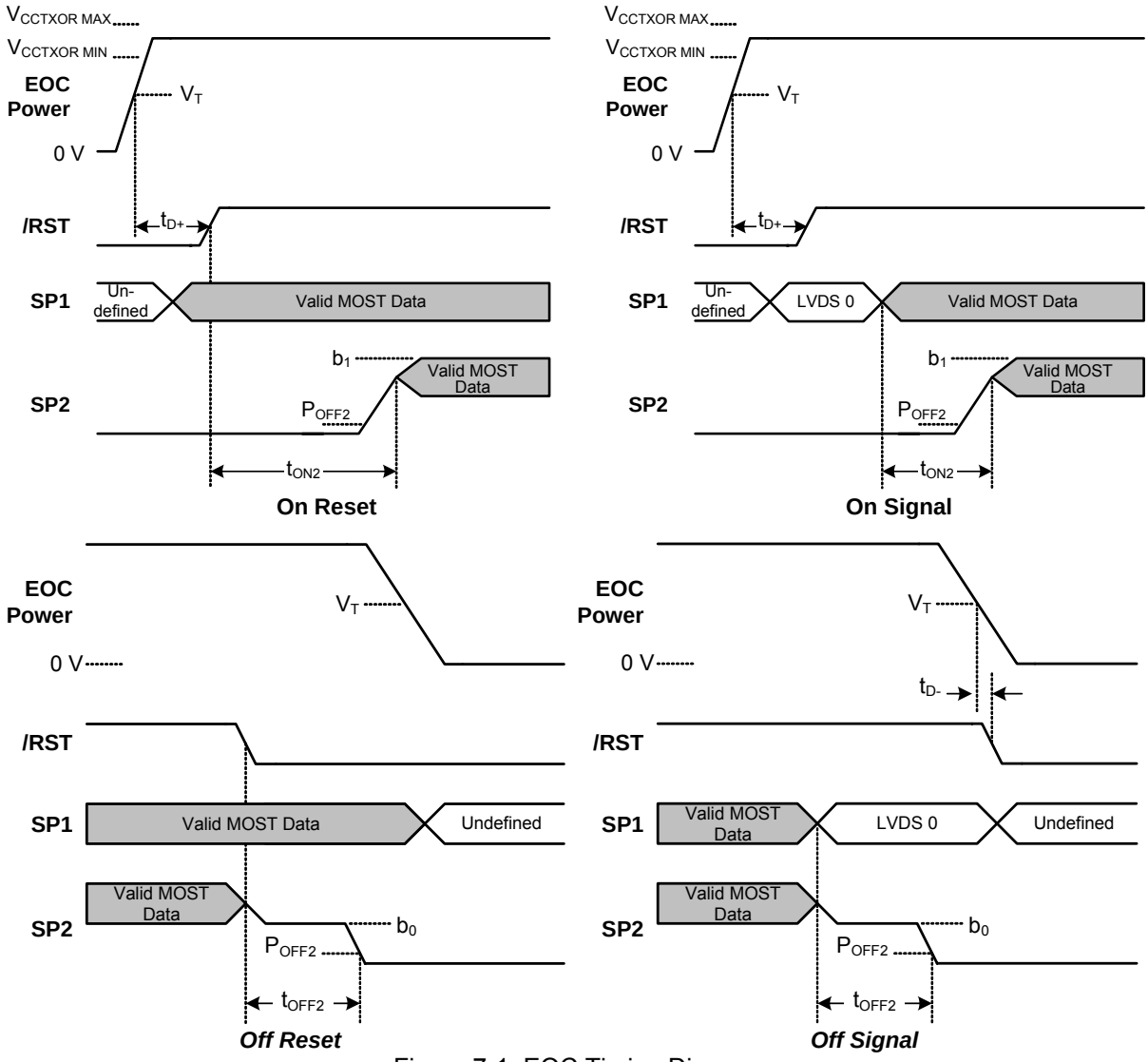


Figure 7-1: EOC Timing Diagram

7.3.1.1 Example Scenarios

A typical powering up sequence and a typical powering down sequence for the EOC are described below and are referenced to Figure 7-1. In the above figure, Valid MOST Data is defined as follows:

- For SP1, Valid MOST Data is DCA encoded data that meets the link quality parameters defined in Table 6-1 and the bit rate requirements defined in Table 9-2.
- For SP2, Valid MOST Data is DCA encoded data that meets the link quality parameters defined in Table 6-2, Table 6-3, Table 6-4, and the bit rate requirements defined in Table 9-2.

7.3.1.1.1 Power On Sequence

The power-on sequence starts with the system power supply voltage to the NIC and EOC ramping up. During the time at which the power supply voltage is not within the EOC's normal operating range, the **/RST** pin is pulled low by the power supply monitoring circuitry to prevent optical glitches from being generated at SP2. Immediately after the supply voltage has reached its normal operating level, the circuitry inside the NIC and EOC may not have fully stabilized. The power supply monitoring circuitry provides a time delay from when the supply voltage has reached its normal operating value until **/RST** goes high so that the local frequency reference, NIC circuitry, and EOC circuitry will have time to stabilize. Some time after the power supply has reached its typical value, the local frequency reference that provides the NIC with timing will have stabilized, and valid LVDS logic levels will be generated by the NIC at SP1. Once the proper frequency is detected at SP1, and **/RST** is high, the EOC can then drive valid data on SP2.

7.3.1.1.2 Power Off Sequence

The normal power-off sequence is initiated by SP1 traffic being driven to logic 0 by the NIC. The EOC detects this event using its internal transition detection circuit and disables the output by driving SP2 to a power level below P_{OFF2} within the required time. The power supply to the EOC will be shut down some time later. During the ramp down of the power supply, the **/RST** pin transitions low before the EOC's power supply drops below the Glitch Safe Voltage Range, preventing any glitches on the output at SP2. The **/RST** signal is valid down to V_{VALID} min. Below V_{VALID} min, the EOC is responsible for preventing any light output at SP2 regardless of the state of **/RST**.

7.3.2 OEC Requirements

The OEC functional requirements are listed below. These requirements are applicable for the OEC when being powered by an operating voltage in the range defined by V_{CCRXOR} in Table 7-3.

a) The OEC must provide an output pin (**STATUS**) in accordance with LVTTL (JESD8C) [4].
b) An OEC in the *Off-State* must meet the following requirements:
   - The OEC must keep its **STATUS** signal high, the SP4 bus disabled, and consume no more than the sleep current, $I_{CCSLEEP}$.
   - The OEC must monitor the optical input power and frequency at SP3.
   - Current consumption may exceed $I_{CCSLEEP}$ if the OEC is being exposed to light above the range P_{OFF3} with a frequency below the range F_{ON3}
c) An OEC in the *On-State* must meet the following requirements:
   - The OEC must keep its **STATUS** signal low and must provide valid output data that meets all the SP4 specifications in Table 6-7 when receiving valid data at SP3.
   - The OEC must monitor the optical input power and frequency at SP3.
d) An OEC must transition from the *Off-State* to the *On-State* upon detecting valid wakeup conditions, defined as an SP3 signal with optical power greater than P_{ON3} and a frequency within F_{ON3} as specified in Table 7-3. The wakeup procedure has the following requirements:

- The OEC must transition the **STATUS** signal low within time t_{STATF} after valid wakeup conditions have been detected at SP3.
- The OEC must enable the SP4 LVDS bus and produce a valid LVDS signal within time t_{LVDSV4} from when **STATUS** was set low.
- The OEC must enter the *On-State* within time t_{ON4} from when the valid wakeup condition was detected.

e) An OEC in the *On-State* must constantly monitor the input power level and signal frequency and must transition to the *Off-State* upon detecting valid shutdown conditions. When the signal at SP3 has optical power less than P_{OFF3} or a frequency within F_{OFF3} as specified the OEC must be in Off-State. The transition procedure to the *Off-State* has the following requirements:
   - The OEC must force the signal at SP4 to LVDS 0 and set **STATUS** high within a time t_{STATR} upon detecting valid shutdown conditions on SP3. The OEC must maintain a valid LVDS signal during the detection phase.
   - The OEC must maintain its LVDS output at a logical 0 for a hold time of t_{LVDSH4} after **STATUS** transitions high.
   - The OEC must enter the *Off-State* within time t_{OFF4} from when the valid shutdown conditions occurred.

f) While F_{ON3} defines the frequency range where the OEC **must** be on and F_{OFF3} defines the frequency range where the OEC **must** be off, the actual transition points will be in the region between F_{OFF3} max. and F_{ON3} min. A similar transition zone exists for the optical power specifications. While P_{ON3} defines the power range where the OEC **must** be on and P_{OFF3} defines the power range where the OEC **must** be off, the actual transition points will be in the region between P_{OFF3} max. and P_{ON3} min.

The OEC must meet the requirements listed in Table 7-3. Refer to Figure 7-2 for more details.

OEC Power State Requirements	Symbol	Condition	Min.	Typ.	Max.	Unit
Powering On						
Average optical input power range for *On-State* operation	P_{ON3}	1)	-22	-	-2	dBm
Frequency range of input at SP3 for *On-State* operation	F_{ON3}	2)	12	-	73.743	MHz
OEC power-on delay	t_{ON4}	3)	-	-	10	ms
Delay to **STATUS** falling	t_{STATF}	5)	200	-	1000	µs
STATUS falling to LVDS valid	t_{LVDSV4}		-	-	100	µs
OEC Operating Voltage Range	V_{CCRXOR}		3.135	3.300	3.465	V
Powering Off						
Average optical input power range for *Off-State* operation	P_{OFF3}	1)	-∞	-	-35	dBm
Frequency range of input at SP3 for *Off-State* operation	F_{OFF3}		0	-	10	kHz
OEC power-off delay	t_{OFF4}	4)	-	-	1	ms
OEC LVDS hold time	t_{LVDSH4}		1	-	-	µs
Delay to **STATUS** rising	t_{STATR}	6)	-	-	2	µs
Current consumption in the *Off-State*	$I_{CCSLEEP}$		-	-	30	µA

Notes:

1) Power within a far field angle of 30º (NA = 0.5) and a diameter of 1.0 mm.
2) The OEC can still be in the On-State above this frequency.
3) t_{ON4} is the sum of t_{STATF}, t_{LVDSV4} and an additional time required for SP4 to be valid MOST traffic.
4) t_{OFF4} is the sum of t_{STATR} and t_{LVDSH4}.
5) Time from valid wakeup condition to status low, see section 7.3.2.d).
6) Time from signal off to status high, see section 7.3.2.e).

Table 7-3: OEC Power State Requirements

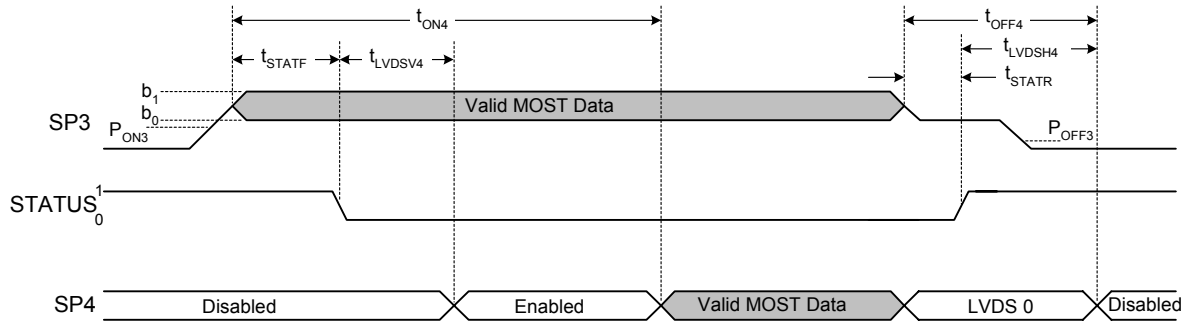


Figure 7-2: OEC Timing Diagram

7.3.2.1 Example Scenarios

The typical sequences explained below provide a description of the timing shown in Figure 7-2. Initially it is assumed that the OEC is powered but in its *Off-State* with **STATUS** high and the SP4 bus disabled. In the above figure, Valid MOST Data is defined as follows:

- For SP3, Valid MOST Data is DCA encoded data that meets the link quality parameters defined in Table 6-6 and the bit rate requirements listed in Table 9-2.
- For SP4, Valid MOST Data is DCA encoded data that meets the link quality parameters defined in Table 6-7 and the bit rate requirements listed in Table 9-2.

7.3.2.1.1 Power On Sequence

The OEC is that is in the *Off-State* monitors the input the SP3 signal. The OEC verifies that the optical power and signal frequency meet specifications before exiting the *Off-State*. If valid wakeup conditions are present, the OEC sets **STATUS** low, enables the SP4 LVDS bus. After a settling time, valid LVDS logic levels are present although valid MOST data may not be on the bus yet. After a short period, the OEC is fully on and valid MOST data is on the SP4 bus.

7.3.2.1.2 Power Off Sequence

An OEC that is in the *On-State* is always monitoring the input power level and signal frequency at SP3. If either the power level or frequency does not meet specifications, the OEC begins transitioning to the *Off-State* by setting the SP4 output to LVDS 0 and driving the **STATUS** pin high. The SP4 bus is then be maintained at LVDS 0 for a hold time while **STATUS** is high. After this hold time, the OEC disables the SP4 bus and enters the *Off-State*.

8 System Specifications

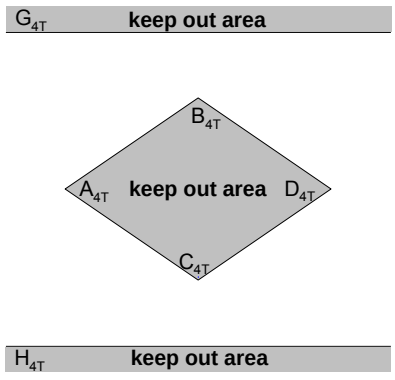
8.1 SP4 Receiver Tolerance

The mask is designed such that a good signal will not touch the mask at any location. A pattern that touches the mask must be recorded as a failure and logged by the test equipment automatically. Signals with slow rise times, low amplitudes, jitter, or pulse width variations will show up as closure in the eye diagram. Signals with excessively high amplitudes will touch the horizontal bars above and below the eye diagram and also cause a failure to be recorded.

All the components along the link must operate with a Bit Error Rate (BER) lower than 10^{-9}. Consequently, all of the mask violation parameters have been specified with that goal in mind. Refer to sections 7.1, 8.4, and 9 for operating conditions and interface standards.

Receiver tolerance SP4	Symbol	Condition	Min.	Typ.	Max.	Unit
Eye-Mask	A_{4T}…H_{4T}	1), 2), 3)	-	-	-	-

Parameter	Amplitude (mV)	Timing (UI)
A_{4T}	0	0.300
B_{4T}	80	0.500
C_{4T}	-80	0.500
D_{4T}	0	0.700
G_{4T}	636	-
H_{4T}	-636	-



Notes:

1) Using the Golden PLL specified in section 5.1.
2) The difference between the SP4 Eye-mask and the SP4 Receiver Tolerance Eye-mask in the horizontal timing direction is due to accumulated jitter along the link.
3) Additional vertical closure on the mask is caused by the large amount of jitter present on the signal. The signal must still comply with the LVDS specification regarding the minimum signal amplitude.

Table 8-1: Receiver Tolerance Parameters of SP4

8.2 Master Delay Tolerance

The master delay is the sum of all static phase (delay) and phase variation measured between the Rx input relative to the Tx output of the master device. The master delay and the total node count must not exceed the maximums shown in Table 8-2.

System Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Node Count	N		-	-	20	nodes
Master Delay Tolerance	T_{MDT}		-	-	$\frac{0.5}{Fs}$	µs

Table 8-2: Master Delay Tolerance Requirements

8.3 Optical Fiber Requirements

8.3.1 Link Length

The maximum node-to-node link length shall be 15 meters.

8.4 Environmental Considerations and Requirements

From the automotive OEM perspective, there are additional specifications which are considered to be minimum requirements. Nevertheless, certain OEMs may have additional requirements:

- The given parameters for all specification points have to be guaranteed by the ECU and its consisting subcomponents, like FOT and Pigtail, under “automotive worst case conditions”, which have to be considered as OEM specific requirements. Ambient conditions like temperature range, humidity, vibration and shock, resistance against chemical agents, EMC/EMI and lifetime are defined for the ECU in these OEM specifications. To fulfill these conditions:
    - FOT and Pigtail shall be characterized and qualified to comply with the appropriate Automotive Application Recommendation.
    - Network Interface Controllers shall be characterized and qualified according to the AEC-Q100 requirements.
    - MOST interfaces should utilize an EMC optimized design
    - The MOST150 oPHY Automotive connector overall dimensions should not exceed those of MOST25 connectors

Other functional requirements that must be considered:

- For the EOC and OEC, an operating temperature range of T_A = -40°C to +95°C is required.
- The temperature at SP2 and SP3 of the ECU shall not exceed T_A = +85°C, based on the maximum allowed temperature of the POF harness.

9 Electrical Interfaces

9.1 LVDS

All component-level RX data and TX data electrical interfaces must be LVDS [3] compliant. One exception is listed in Table 9-1. All PCB-level RX data and TX data electrical interfaces must be designed such that components compliant with [3] shall operate correctly. This requirement applies to PCB-level components only and is not intended for the wiring harness. All electrical signals must maintain the correct polarity from OEC to NIC and from NIC to EOC.

Exception regarding LVDS [3]	Symbol	Min.	Typ.	Max.	Unit
Common-mode Input Voltage range	V_{CM}	0.05	-	Vcctx – 1.2V	V

Table 9-1: Exception regarding LVDS [3]

9.2 Bit Rate and Frequency Tolerance

Specifications for the operating bit rates are shown in Table 9-2. Each MOST150 oPHY Automotive node requires a local frequency reference. Manufacturable frequency references operate at some frequency offset tolerance around the nominal Fs (either 44.1 kHz or 48 kHz). System interoperation relies on these offsets being minimized. The Time Base Deviation, Δ_{FS}, is this offset and is measured in parts per million (ppm).

Bit Rate and Frequency Tolerance	Symbol	Min.	Typ.	Max.	Unit
Time Base Deviation	Δ_{FS}	-200	0	+200	ppm
Bit Rate for 44.1 kHz frame rate	BR_{44}	135.448105	-	135.502295	Mbits/s
Bit Rate for 48.0 kHz frame rate	BR_{48}	147.426509	-	147.485491	Mbits/s

Table 9-2: Bit Rate and Frequency Tolerance

The nominal Bit Rate is obtained by multiplying the frame rate by 3072. The minimum values are obtained by taking the nominal frame rates and subtracting the time base deviation. The maximum values are obtained by taking the nominal frame rates and adding the time base deviation.

10 FOT Packaging

10.1 SMD Package

References for drawings related to the SMD FOT package are listed in Table 10-1.

Drawing Code	File Name
MOST150 FO-Transceiver	MOST150 FO-Transceiver_SMD_AVx.PDF
	PDF Files are available on www.mostcooperation.com x indicates version number of drawing file

Table 10-1: Drawing Codes and File Names for the SMD FOT

The corresponding up-to-date drawings have to be applied.

10.1.1 SMD FOT Pinout

An EOC and OEC shall be combined into one 24-pin surface mount package having a body of 7.5 mm x 15.6 mm. The pinout is shown below. The printed circuit board footprint shall be compatible with the JEDEC standard package type R-PDSO-G.

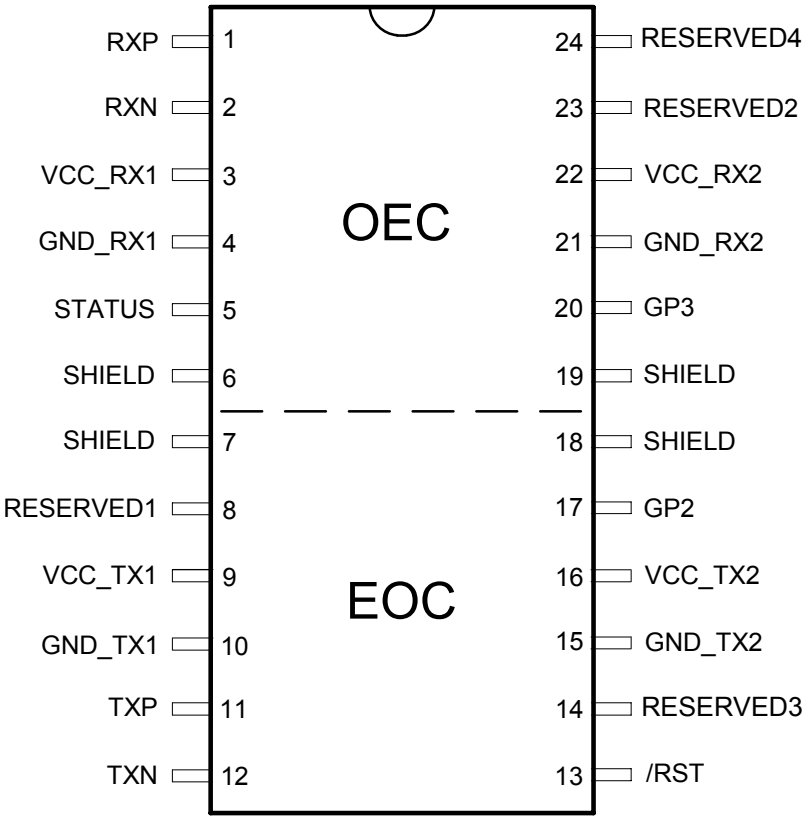


Figure 10-1: SMD Transceiver Pinout

10.1.2 OEC Signal Descriptions

The SMD OEC section illustrated in Figure 10-1 must conform to the pinout and signal functionality as described in Table 10-2.

Pin Name	Pin No.	Functional Description
RXP	1	OEC data output +. P terminal of the differential signal.
RXN	2	OEC data output -. N terminal of the differential signal.
VCC_RX1	3	Power supply pin for the digital circuitry.
GND_RX1	4	Ground return for the digital circuitry.
STATUS	5	STATUS output. Logic low when the OEC is in the On-State. Logic High when the OEC is in the Off-State. Refer to section 7.3.2 for more details.
SHIELD	6, 19	Internal EMI shield. Connect to the OEC side ground on the PCB.
GP3	20	General purpose pin, not used for basic MOST functionality. The OEC must be MOST compliant independent of whether this pin is left unconnected or connected to external circuitry described in the OEC datasheet.
GND_RX2	21	Ground return for the analog circuitry.
VCC_RX2	22	Power supply for the analog circuitry.
RESERVED2	23	Reserved for future use in MOST. On the PCB, connect to VCC_RX2 through a 0-Ohm resistor.
RESERVED4	24	Connect according OEC datasheet.

Table 10-2: Signal Descriptions for the OEC

10.1.3 EOC Signal Descriptions

The SMD EOC section illustrated in Figure 10-1 must conform to the pinout and signal functionality as described in Table 10-3.

Pin Name	Pin No.	Functional Description
SHIELD	7, 18	Internal EMI shield. Connect to the EOC side ground on the PCB.
RESERVED1	8	Reserved for future use. On the PCB, connect to ground through a 0-Ohm resistor.
VCC_TX1	9	Power supply for the EOC.
GND_TX1	10	Ground return for the EOC power supply.
TXP	11	EOC data input +. P terminal of the differential signal.
TXN	12	EOC data input -. N terminal of the differential signal.
/RST	13	Active-low logic input signal that disables optical output. Refer to section 7.3.1 for more detail.
RESERVED3	14	Connect according EOC datasheet.
GND_TX2	15	Ground return for the EOC power supply.
VCC_TX2	16	Power supply for the EOC.
GP2	17	General purpose pin, not used for basic MOST functionality. The EOC must be MOST compliant independent of whether this pin is left unconnected or connected to external circuitry described in the EOC datasheet.

Table 10-3: Signal Descriptions for the EOC

10.2 Through-hole mount (THM) Package

References for drawings related to the THM FOT Package are listed in Table 10-4.

Drawing Code	File Name
MOST FO-Transceiver THM	MOST150_FO-Transceiver_THM_AVx.pdf
	PDF Files are available on www.mostcooperation.com x indicates version number of drawing file

Table 10-4: Drawing Codes and File Names for the THM FOT

The corresponding up-to-date drawings have to be applied.

10.2.1 THM FOT Pinout

The EOC and OEC are separated in two 7-pin THM packages. The pinout is shown below.

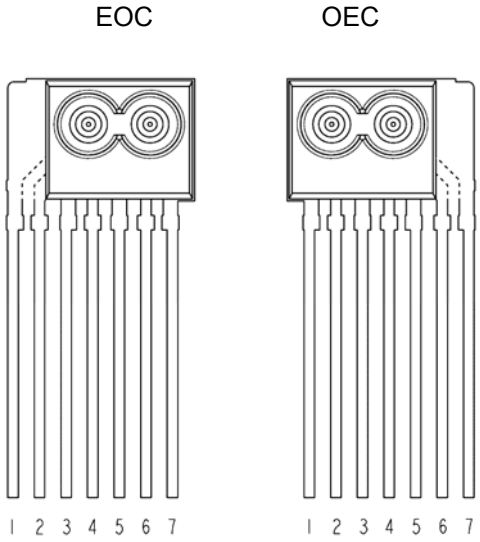


Figure 10-2 : THM Pinout

10.2.2 OEC Signal Descriptions

The OEC illustrated in Figure 10-2 must be conform to the pinout and signal functionality as described in Table 10-5.

Pin Name	Pin No.	Functional Description
STATUS	1	STATUS output. Logic low when the OEC is in the On-State. Logic High when the OEC is in the Off-State. Refer to section 7.3.2 for more details.
VCC_RX1	2	Power supply for the OEC.
GND_RX	3	Ground return for the OEC power supply.
RXN	4	OEC data output -. N terminal of the differential signal.
RXP	5	OEC data output +. P terminal of the differential signal.
RESERVED4	6	Connected according OEC datasheet.
VCC_RX2	7	Power supply for the OEC.

Table 10-5 : Signal Descriptions for the OEC

10.2.3 EOC Signal Descriptions

The EOC illustrated in Figure 10-2 must be conform to the pinout and signal functionality as described in Table 10-6.

Pin Name	Pin.No.	Functional Description
/RST	1	Active-low logic input signal that disables optical output. Refer to section 7.3.1 for more detail.
RESERVED3	2	Connect according EOC datasheet.
TXN	3	EOC data input -. N terminal of the differential signal.
TXP	4	EOC data input +. P terminal of the differential signal.
GND_TX	5	Ground return for the EOC power supply.
VCC_TX	6	Power supply for the EOC.
RESERVED1	7	Reserved for future use in MOST. On the PCB, connect to ground through 0-Ohm resistor.

Table 10-6: Signal Description for the EOC

.

11 Device Connectors

11.1 Connector Interfaces

Table 11-1 summarizes the five specified connector interfaces.

"Nick Name"	Number of Optical Contacts	Number of Electrical Contacts		
		PIN = 0.63 mm	PIN = 1.5 mm	PIN = 2.8 mm
2+0	**2**	**-**	**-**	**-**
2+4	**2**	**4**	**-**	**-**
2+12	**2**	**12**	**-**	**-**
2+20	**2**	**18**	**2**	**-**
4+40	**2 x 2**	**2 x 12**	**-**	**2 x 8**

Table 11-1: Connector Family

Table 11-2 is a listing of all standardized connectors and indicates the drawing codes, the file names of all specified connector interfaces and the drawing date.

"Nick Name"	Drawing Code	TIFF File
2+0	MOST-CON-2-0	MOST-CON-2-0.TIF
2+4	MOST-CON-2-4-AD-C	MOST-CON-2-4-AD-C.TIF
2+12	MOST-CON-2-12-AD-C	MOST-CON-2-12-AD-C.TIF
2+20	MOST-CON-2-20-AD-C	MOST-CON-2-20-AD-C.TIF
4+40	MOST-CON-4-40	MOST-CON-4-40.TIF
Fiber Module Interface	MOST-FM-I	MOST-FM-I.TIF
Test Connector	MOST-CON-T	MOST-CON-T.TIF
LWL Collar	MOST-FM-C	MOST-FM-C.TIF
		TIFF Files available on www.mostcooperation.com

Table 11-2: Drawing Codes and File Names of Connector Interfaces

The corresponding up-to-date drawings have to be applied.

11.2 Connector Interface Loss

Figure 11-1 shows details of the connector insertion loss D_{con} between devices and cabling:

- The attenuation of optical power may not exceed $D_{con2max}$ = 2.5 dB, when optical signal transits from SP2 into the cabling fiber.
- The attenuation of optical power may not exceed $D_{con3max}$ = 2.5 dB, when optical signal transits from the cabling fiber into SP3.

Note: The maximum connector attenuation is a part of this specification.

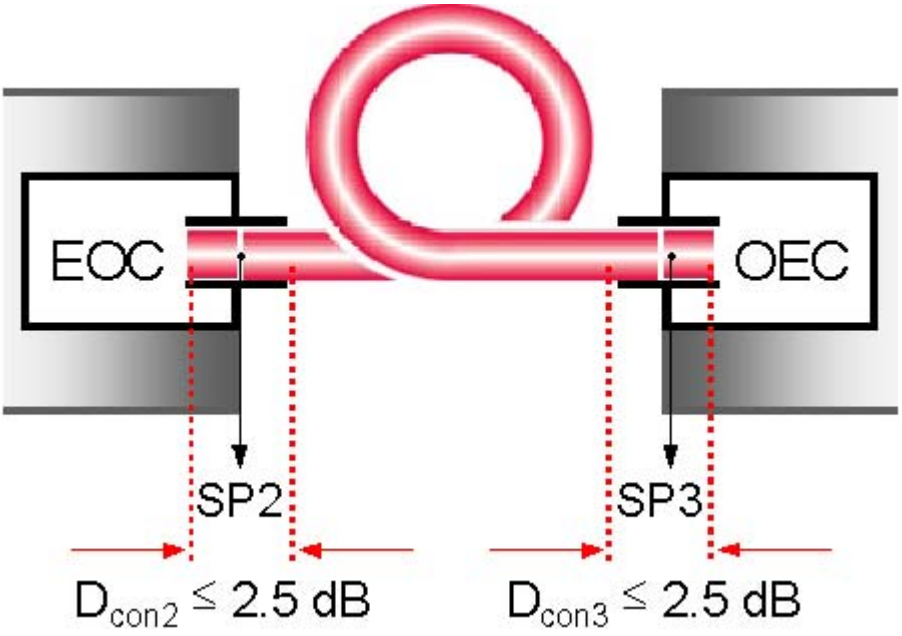


Figure 11-1: Connector insertion loss.

Appendix A: Index of Figures

12 Appendix B: Index of Tables

Notes: