MOST

Media **O**riented **S**ystems **T**ransport

Multimedia and Control Networking Technology

MOST150 oPhy Compliance Verification Procedure – Physical Layer
Rev 1.1
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Contents

Bibliography

All documents, which are referenced by this MOST document, are listed here along with their versions. For the current release status, please refer to the MOST Cooperation Document List.

Document		Revision
[1]	**MOST Specification**	3.0E2
[2]	**MOST Basic Physical Specification**	1.0
[3]	**MOST150 oPhy Automotive Physical Layer Sub-Specification**	1.1
[4]	**MOST Compliance Requirements**	2.1
[5]	**MOST150 oPhy Compliance Measurement Guideline**	1.1
[6]	**FBlock Enhanced Testability**	3.0.1

MOST Document references

Document History

Changes

Change Ref.	Section	Changes
1.1		New Issue

1 Introduction

1.1 Relevance of Compliance

Compliance in terms of Physical layer means products have to fulfill all specified parameters. This includes electrical and optical parameters, signal-timing as well as mechanical properties. For verification of these parameters, suppliers of devices, modules and components have to implement suitable processes like product-characterization, qualification and end-of-line-testing (considering environmental conditions, stability over lifetime etc.) There are various Industry and automotive standards defining procedures and quality requirements. (e.g. ISO 9000, ISO/TS 16949, AEC Q100, AAR).

The process of compliance certification is defined to check a subset of parameters. Therefore the compliance certification performs only a crosscheck with focus on basic network interoperability.

1.2 Related Documents

The MOST Basic Physical Specification [2] in combination with the MOST150 oPhy Automotive Physical Layer Sub-Specification [3] defines all relevant parameters. There are also mechanical drawings, referenced in [3] which are relevant for compliance. The MOST150 oPhy Compliance Measurement Guideline [5] describes how to determine and measure parameters. These documents are applicable for MOST devices as well as for modules and components. The process of Compliance Verification is defined in the Most document MOST Compliance requirements [4]. It describes how to achieve a compliance certification for MOST subsystems.

Terminology of naming within these documents:

MOST End Product in document [4] = Device in document [3,5]:

Any product within the bounds of scope that is offered for sale or is distributed in an unmodified form to any end user who acquires the product for such end user's personal or commercial use, alone or in combination with any other product.
Electronic Control Unit (ECU) that contains MOST modules

MOST Component in document [4] covers Module in document [3,5]:

Assembly of components that are bounded between two specification points
(e. g. EOC, OEC).

MOST Component in document [4] covers Components in document [3,5]:

Parts that are used to build up modules (e. g. Fiber Optical Transceivers (FOT), Connector, housing). The components like FOTs can contain components itself (LED, driver – IC, etc.).

→ A component product within the bounds of Scope designed and marketed for the enabling of a complete MOST End Product, yet not being able to function as a complete MOST End Product. A MOST Component is only licensed for integration into a MOST End Product that is subsequently verified for compliance.

1.3 MOST Link

1.3.1 Location of Interfaces

SP1 describes input parameters for the EOC. It also describes the output parameters of a NIC, including data path between NIC and EOC.
SP2 defines the optical output signal.

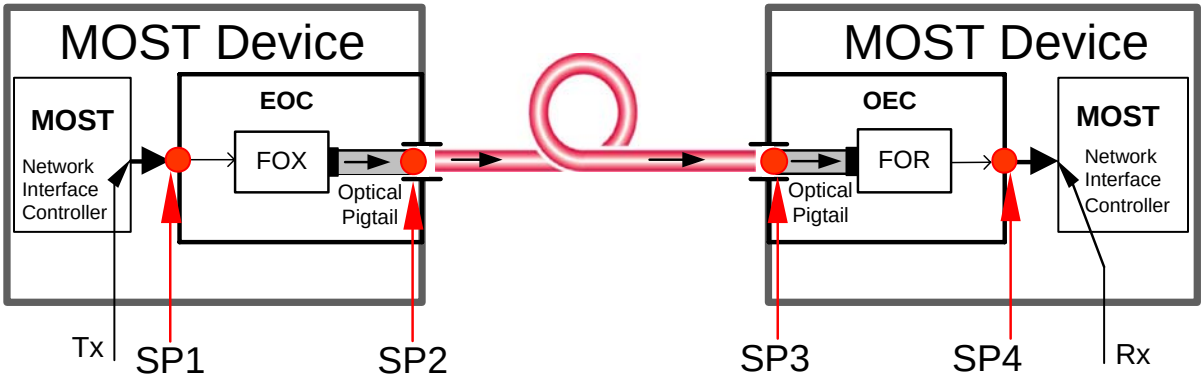

Figure 1-1: Location of Specification Points

SP3 describes the optical input interface for the OEC. Signal characteristics at SP3 need to consider worst case optical signal according SP2-definition plus deterioration due to the transport media.
SP4 link quality describes the output parameters for OECs including termination.
SP4 receiver tolerance specifies the input tolerance for NICs and is relevant for system evaluation.

Signals that fulfill the SP4-parameters can be recovered by the NIC, signals outside the ranges may cause bit-errors. On TX of the NIC (node n+1) a recovered signal is available according to SP1 requirements, timing distortion (except transferred jitter) is eliminated.

1.3.2 Control Signals

In addition to Power supply terminals and Data-pins, an EOC need to provide a /RST input. The EOC provides activity detection in order to enable/disable light emission. Activity depends on VCC-state, Data content of SP1and Reset state.

The OEC also provides activity detection. Depending on the characteristics of the input signal (power level, signal content) ON/OFF state is signaled by the Status line.

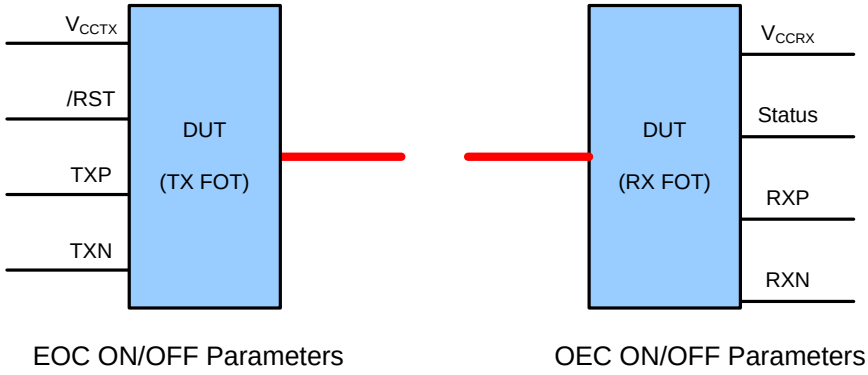

Figure 1-2: Control Signals for ON/Off Behavior

1.4 Limited access to specification points

Verification of parameters at particular SPs requires access to that particular interface. In addition for most of the parameters a stimulation signal at the previous SP is required. Full access to all SPs is only guaranteed on "component" level and "module" level (refer chapter 4, Full Physical Layer Compliance).

On "device" level MCTHs do not have access to SP1 and SP4. Therefore compliance verification on "component" and "module" level is required. This is a pre-condition for simplification of the compliance verification of devices, using the limited (access) compliance procedure.
For an MCTH on "device" level only SP2 and SP3 are visible. Therefore variation on input parameters can only be applied at SP3 (optical signal input of the device). Parameters can only be measured at SP2. The power supply of NIC, EOC and OEC is fixed by the design of the device and can not be varied. Considering these circumstances the "limited physical layer compliance" describes a simplified test procedure that uses only the accessible interfaces of a MOST device, SP2 and SP3 (refer chapter 5, Limited Physical Compliance).

The MOST specification of ***MOST Compliance Requirements*** [4] offers the opportunity of testing components and modules according their "covered functionality". Depending on the partitioning of components within modules or Devices the respective parameters can be verified at single components. These parameters need to be verified on higher product integration levels.

1.4.1 Example for "covered functionality"

An EOC is defined by the interfaces SP1 and SP2, including the electrical to optical conversion and the geometry of the connecting system. An EOC is compliant when all SP2-requirements are fulfilled, considering input parameter and the respective ranges at SP1.

- A light emitting source (e.g. LED) that is part of the EOC affects directly the parameters with respect to emitting wavelength. (➔ center wavelength, spectral width)
  Component
  ↓
  - An optical transmitter (e.g. FOT-TX (driver-chip & LED-Chip)) covers nearly the complete EOC-performance, (➔timing; transition times; Overshoot; optical power).
    Component/Module
    ↓
    - The EOC contains the above mentioned transmitter. The optical output power is influenced by the optical transmitter and the interface geometry at SP2. (➔ optical power; interface geometry)

Module
↓

- The device contains the EOC (module). The optical output power is only influenced by the application of the EOC in the device.
  Device

2 Parameter-Overview

The following table shows all parameters of the MOST150 oPhy Automotive Physical Layer Sub-Specification [3] Indications about the meaning of the parameters for the interfacing components, modules and device (input, output, property) and appropriate measuring methods are given in MOST150 oPhy Compliance Measurement Guideline [5]. For each parameter it indicates how compliance can be achieved dependent from type (component (MOST NIC), module (EOC/OEC) and device).

Parameters, defined in the MOST150 oPhy Automotive Physical Layer Sub-Specification [3] are mandatory parameters for component/module datasheets. The verification of these parameters is done using the procedure of the product characterization.

This section describes every parameter at every specification point from the standpoint of the MOST compliance that has to be fulfilled by MOST components and MOST devices.
Table 2-1 shows all the specified parameters of the MOST150 oPhy Compliance Measurement Guideline [5]. In addition, this table indicates whether the parameters have to be interpreted for inputs, outputs or properties related to hardware components.

Note: *Developers of components or modules have to ensure that their products fulfill the specification under min/max conditions of their input parameters, considering environmental conditions and over lifetime.*

	Parameter to be compliant	Component		Module	Device
		EOC	OEC		
SP1					
	Bit Rate	-		-	Output via SP2 M, V
	LVDS conformity	-		-	
	Alignment Jitter acc. to Eye Mask	-		-	
	Transferred Jitter via RMS	-		-	
SP2					
	Eye safety	V			
	Center wavelength	V		V	-
	Spectral width (RMS)	V		V	-
	Optical output power	M(TU), V		M(TU), V	M(TU)
	Extinction ratio	M(TU), V		V	-
	Transition time (rise and fall)	M(TU), V		V	M(TU)
	Alignment Jitter acc. to Eye Mask	M(TU), V		V	M(TU)
	Transferred Jitter via RMS	M(TU), V		V	M(TU)

	Parameter to be compliant	Component		Module	Device
		EOC	OEC		
	Optical Overshoot/Undershoot	M(TU), V		V	M(TU)
	EOC Test Sequence #1 - OFF-to-ON by SP1 Signal	M(U), V		V	-
	EOC Test Sequence #2 - OFF-to-ON by SP1 Signal	M(U), V		V	-
	EOC Test Sequence #3 – ON-to-OFF by SP1 Signal	M(U), V		V	-
	EOC Test Sequence #4 - OFF-to-ON by SP1 Signal	M(U), V		V	-
	EOC Test Sequence #5 – ON-to-OFF by SP1 Signal	M(U), V		V	-
	EOC Test Sequence #6 - OFF-to-ON by /RST Signal	M(U), V		V	-
	EOC Test Sequence #7 - ON-to-OFF by /RST Signal	M(U), V		V	-
SP3					
	Center wavelength	-	V	V	-
	Spectral width (RMS)	-	V	V	-
	Receivable optical power range for data recovery	-	V	V	-
	Limited Physical Layer Test of Data consistency	-	-	-	M(TU)
SP4	***Link Quality***				
	LVDS conformity		V	V	-
	Alignment Jitter acc. to Eye Mask		M(TUP),V	M(TUP),V	
	Transferred Jitter via RMS		M(TUP),V	M(TUP),V	
	Current consumption in the OFF state		M(TU), V	V	
	OEC Test Sequence #1 - OFF-to-ON		M(U),V	V	
	OEC Test Sequence #2 - OFF-to-ON		M(U),V	V	
	OEC Test Sequence #3 - OFF-to-ON		M(U),V	V	
	OEC Test Sequence #4 - OFF-to-ON		M(U),V	V	
	OEC Test Sequence #5 - ON-to-OFF		M(U),V	V	
	OEC Test Sequence #6 - OFF-to-ON		M(U),V	V	
	OEC Test Sequence #7 - ON-to-OFF		M(U),V	V	
SP4	***System Performance***				
	Receiver Tolerance	-	-	-	-
	Master Delay Tolerance	-	-	-	-
Mechanical interface requirements				M	

Table 2-1: Compliance procedures for all parameters of specification points.

Legend:

Full Physical Layer: Component (OEC/EOC), module
Limited Physical Layer: Device

Procedures:

- = No compliance test necessary

M = Measure (T=Temperature Range, U=Voltage Range, P=Optical Input Power Range)

V = Verification by datasheet of the used MOST compliant components (no influence possible due to application)
The parameter needs to be measured on the particular level (component → module → device).
If characterization data are available of components which are used in modules and if it is proved that the module (application) has no influence to that parameter the module needs not to be measured again for this parameter. This is the same when using characterized components or modules in devices. The supplier may provide evidence for characterization/qualification process on lower level.
E.g. spectral width is characterized and guaranteed by the LED manufacturer and can not be influenced by other parameters like power supply. Therefore FOT-manufacturers or EOC-manufacturers do not need to characterize this parameter if they get characterization results of the LED from their suppliers. Device manufacturers just refer to the FOT datasheet for that parameter.

3 Physical Layer Testing for Modules, Components and Devices

Definition of Terms:

MOST Module	Product between two interfaces, which are defined in the **MOST150 oPhy Automotive Physical Layer Sub-Specification** [3] and **MOST Basic Physical Specification** [2]
Product information	for compliance needed information: construction, data sheet, application spec, list of used compliant parts, characterization information of product (covered functionality can be part of the characterization information)
Correction factor	deviation between MOST specification point and measurable point of part (optical path (example: Transmitter sending light with min. –7 dBm to achieve limit of SP2 of –8.5 dBm))

FOT: Full Physical Layer Compliance Verification has to be performed with one of five pieces. that have to be submitted by the manufacturer.

Pigtail: a) with FOT (THM): Full Physical Layer Compliance Test with subset Pigtail has to be performed with one of five pieces that have to be submitted by the manufacturer.
The pre-condition is that the FOT has already passed Full Physical Layer Compliance Verification successfully.

b) with FOT (SMD): Pigtail Fibre and Connector are subject of Full Physical Layer Compliance Verification.
Characterization report has to be submitted by the manufacturer for verification by the MCTH.

Device: a) THM : Limited Physical Layer Compliance Verification has to be performed with one device that has to be submitted by the manufacturer.
The pre-condition is that both the FOT and the Pigtail have already passed Full Physical Layer Compliance Verification successfully.
b) SMD: Limited Physical Layer Compliance Verification
The pre-condition is that the FOT has already passed Full Physical Layer Compliance Verification successfully and that the Pigtail has been characterized accordingly.

Development Tool: Compliance Verification of applicable parts according to MCTH.

4 Full Physical Layer Compliance

4.1 Overview

Full Physical Layer Compliance refers to MOST modules or MOST components.

4.2 Consideration of FOT

The parameters to be tested and verified are given Table 2-1.

For compliance testing according to Fig. 5-3 (EOC Signal Chart No. 2) of MOST150 oPhy Compliance Measurement Guideline [5], V_{CCTX} must have reached V_{CCTXOR} at the time of reset signal going high.

4.3 Consideration of Pigtail

a) Pigtail with FOT (THM): Full Phy Compliance Test according to Table 2-1, column “module”.

b) Pigtail with FOT (SMD): Pigtail Fibre and Connector are subject of Compliance Verification. Listing of Pigtail Fibre and Connector in the MCPL will be done together as an entity.

4.3.1 Consideration of Connector Interfaces (Check of dimensions)

The compliance verification of the connector interface contains two steps. First, a characterization report, to be provided by the supplier, is checked by the MCTH. Secondly the MCTH verifies 3 dimensions, arbitrarily chosen from the MOST connector drawings. The supplier provides 3 samples of each connector-type to be verified.

4.4 Generating test signals for the DUT

With respect to Full Physical Layer compliance the generation of dynamic jitter for SP2 within the jitter extremes has to consider both deterministic and random jitter. The actual consistency of the jitter signal must be reproducible. It is determined by the MCTH.

4.4.1 Test Setup for Jitter Measurement

The test setup for jitter measurement according to MOST150 oPhy Compliance Measurement Guideline [5] shall be used but with the following restrictions:

Basic Setup – to be used for the complete input power range:
Setup: < 2 m POF
Light Levels: -2 dBm to -22 dBm (min. 6 Steps)
Light Source: Transition Time: < 1.00 ns

Low BW Setup – to be used additionally for the minimum optical input power:

Setup: Mode Mixer + 15m POF
Light Levels: -22dBm
Light Source: Transition Time: between 1.00ns and 0.5UI
Extinction Ratio: 10dB to 12dB

5 Limited Physical Compliance

5.1 Overview

Limited Physical Layer Compliance refers to MOST devices (refer section 1.4, Limited access to specification points).

Generally compliance testing requires access to all specification points. In addition various test signals have to be applied to particular interface in order to check worst case performance of components and modules that are connected to that interface. The whole testing has to consider all environment conditions (e.g. specified operating temperature, power supply variations).

An overview of the parameters to be tested and verified is given Table 2-1.

The following diagram shows the required test setup for limited physical layer testing comprising the following equipment:

- Physical Layer Stress Test Tool (PhLSTT)
- Optical attenuator
- Mode mixer
- Optical splitter
- Optical Power Meter
- Measurement OEC
- Oscilloscope

Test-SetUp 1:

- Check of lock capability depending on variation of the optical input power
- Measurement of optical output power of SP2
- Check of data consistency by comparison of the DUT's input- and output data stream

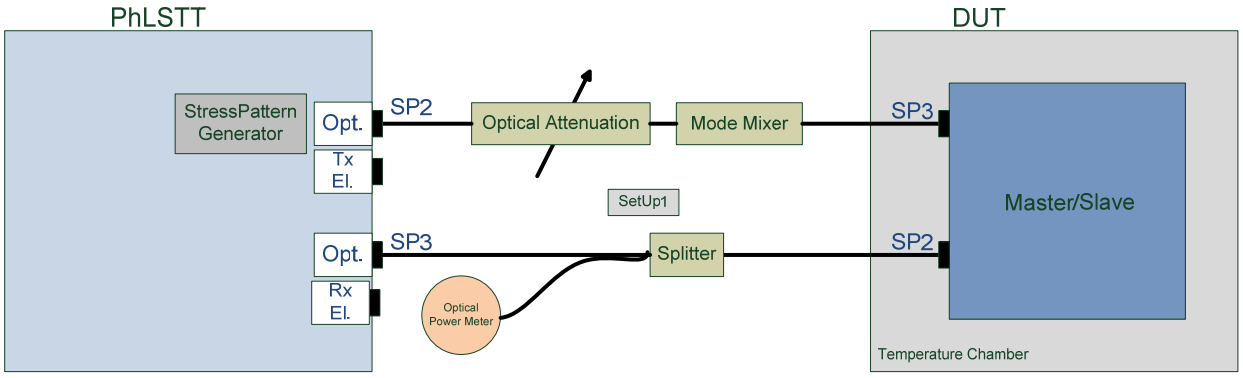

Figure 5-1: Test setup 1 for Limited Physical Layer Compliance test

Test-SetUp 2:

- Verification of signal integrity of optical signal at SP2 - DUT.

Verification of signal integrity includes measurement of pulse shape and timing characteristics at the DUT's optical SP2 interface. The test flow shown in section 5.4 requires a closed loop between PhLSTT and DUT, providing functional communication over MOST. In addition, the measurement at SP2 of the DUT requires an OEC in the optical path with its electrical output coupled to the oscilloscope. The OEC's electrical output signal gives an analogue representation of the optical signal. Therefore some kind of splitter-functionality is required. Basically there are two options. An optical splitter can be used transferring a part of the optical signal to the measurement OEC and another part of the signal to the optical input of the PhLSTT. Challenge of this approach is to provide sufficient power to both optical sinks for achieving sufficient S/N for the measurements and proper data recovery at the PhLSTT. The second option splits the electrical signal behind the OEC, while the DUT's optical signal is directly coupled to the OEC. Challenge of this approach is to realize the electrical splitter without degrading the electrical signal (e. g. by reflections). It is up to the MCTH to choose an appropriate setup.

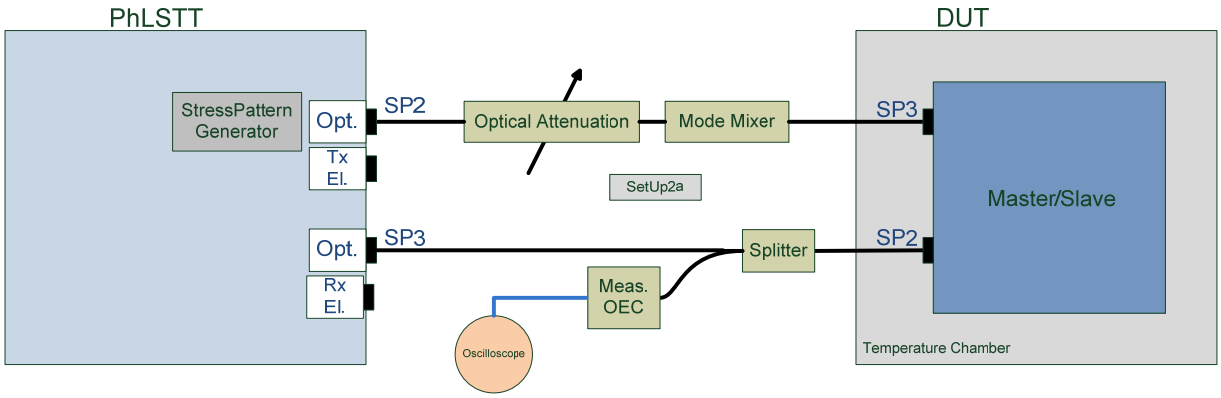

Figure 5-2: Basic Test setup 2a for Limited Physical Layer Compliance test

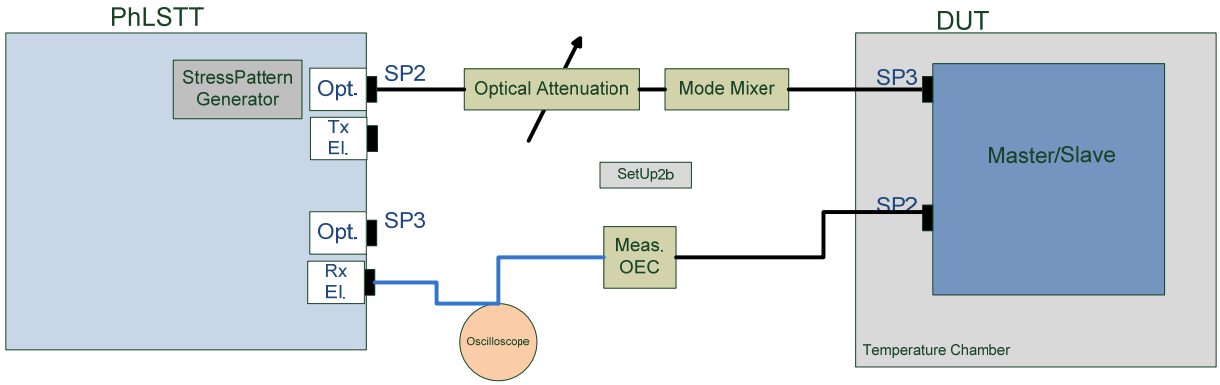

Figure 5-3: Basic Test setup 2b for Limited Physical Layer Compliance test

Test-SetUp 3:

- Verification of t_{Wakeup} and $t_{Shutdown}$.

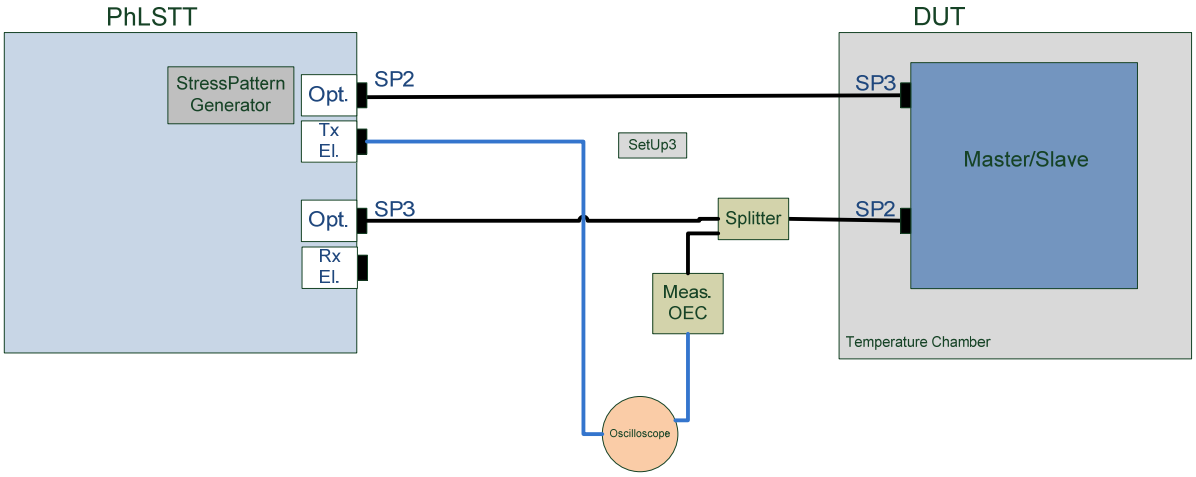

Figure 5-4: Basic Test setup 3 for Limited Physical Layer Compliance test

5.2 Generating test signals for the DUT Input section SP3

A test signal for testing the DUT´s input section may be varied in several instances and combinations of these instances (e. g. timing properties, data content, optical power and pulse shape characteristics). A subset of such variations is realized with the PhLSTT which is a mandatory tool for Limited Physical Layer Test.

The PhLSTT initiates and controls the whole test sequences. The PhLSTT controls the DUT using communication via MOST control channel. It addresses the DUT's FBlock Enhanced Testability (ET) which covers all necessary DUT functions for the tests (e.g. "retimed bypass", handling of various error counters). The PhLSTT is capable to act as Timing Master or Slave. Besides standard MOST communication, the PhLSTT has the capability to send a worst case stress pattern.

For the test, the worst case stress pattern is combined with attenuation on the optical link and bandwidth limitation due to the transport medium before being applied to the DUT's SP3 Interface.

5.3 Analysis of Test results

Error Counters are implemented in the DUT (FBlock Enhanced Testability). These counters give a measure for communication errors on the input of a device. These counters are activated during the test sequence. The result can be read after the test.

During the test sequence, the DUT is set in the "retimed bypass". This means that the recovered data on the input side are sampled with the internal clock and transferred to the output. Therefore as long as there are no bit errors, the worst case stress pattern created by the PhLSTT will appear with identical content on the output of the DUT. This enables a comparison of the data content inside the PhLSTT (Limited Physical Layer Test of Data consistency).

In addition to generation of the signal, it is important to check whether the pattern sent is also correctly recognized by the DUT during the test execution. In order to be able to carry out this check, the DUT is set in a special bypass mode; the "Retimed Bypass Mode". This mode forwards the received pattern in unmodified form. In this way, the pattern at the output of the DUT can be compared with the pattern applied from the PhLSTT. For this case a pattern comparator is implemented in the PhLSTT. Analysis of

the pattern comparator relates to two characteristics: The bit errors occurred and sudden phase shifts in the received signal. Both incidents are counted by the PhLSTT and reported after completion of the test.

5.4 Test Flow Overview

Figure 5-5 depicts an overview of the test flow.

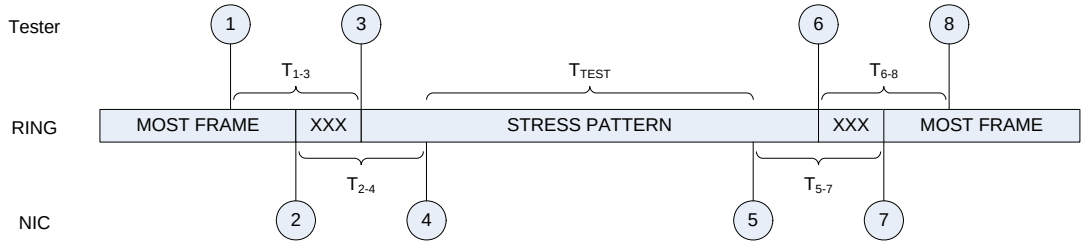

Figure 5-5: Test Flow Overview

1 – PhLSTT sends command to DUT over MOST150 (FBlock Enhanced Testabilty) to enter Test Mode.
2 – DUT enters Retimed Bypass Mode.
3 – PhLSTT starts transmitting the Stress Pattern.
4 – DUT clears the Error Counter and Lock Log.

… PHYSICAL LAYER STRESS TESTING …

5 – DUT reads back Error Counter and Lock Log.
6 – PhLSTT switches to MOST150 Communication Mode.
7 – DUT switches back to its original MOST150 Mode.
8 – PhLSTT reads back the result.

Switching times (T_{X-Y}) are in the range 10 – 500 ms with accuracy better or equal than 10 ms;

Lead-in / Lead-out: typ. 1000ms (min. 500ms ; max. 2000ms).

T_{TEST} time is in the range 1 sec – 1000 sec with accuracy better or equal than 10 ms.

Duration: max.1000 seconds.

5.5 Measurement of SP3 input signal of the DUT

The following parameters on SP3 have most significant influence to the behavior of a device:

Optical input power at SP3	P_{opt3} (max) without mode mixer and short POF
	P_{opt3} (min) with mode mixer with 15 m POF
Timing	minimum duty cycle
	maximum duty cycle

As a consequence the optical transmitter that is implemented into the PHLSTT has to correspond to the following requirements:

- The test setup has to fulfill all parameters of the MOST Physical Layer specification for SP3

- The Duty Cycle according to eye mask of the transmitted signal has to be adjustable according to limits of the specified eye mask.
- The defined stress pattern has to be applied.

Test case	Popt @SP3	Duty Cycle@SP3	Temperature/Power Range
1	P_{opt3} (max)	Duty Cycle min	$T_{23°C}$ / U_{typ}
2	P_{opt3} (max)	Duty Cycle max	$T_{23°C}$ / U_{typ}
3	P_{opt3} (min)	Duty Cycle min	$T_{23°C}$ / U_{typ}
4	P_{opt3} (min)	Duty Cycle max	$T_{23°C}$ / U_{typ}
5	P_{opt3} (max)	Duty Cycle min	T_{max} / U_{min}
6	P_{opt3} (max)	Duty Cycle max	T_{max} / U_{max}
7	P_{opt3} (min)	Duty Cycle min	T_{max} / U_{min}
8	P_{opt3} (min)	Duty Cycle max	T_{max} / U_{max}
9	P_{opt3} (max)	Duty Cycle min	T_{min} / U_{min}
10	P_{opt3} (max)	Duty Cycle max	T_{min} / U_{max}
11	P_{opt3} (min)	Duty Cycle min	T_{min} / U_{min}
12	P_{opt3} (min)	Duty Cycle max	T_{min} / U_{max}

Note:

- Rise-/Fall-times, positive overshoot, negative overshoot, extinction ratio are typical but have to fulfill the specification.
- Again, be aware that these settings do not cover all possible failure modes of a DUT.

Table 5-1: Summary of Test cases.

5.6 Measurement of SP2 output signal of the DUT

According to Table 2-1 the parameters in Table 5-2 below have to be measured for each test case. The tests have to be performed at

1. $T_{23°C}$ / U_{typ} ; ,
2. T_{min} / U_{min} ;
3. T_{min} / U_{max} ;
4. T_{max} / U_{min} ;
5. T_{max} / U_{max} ;

while going from U_{typ} → U_{min} → U_{max}.

Measurement of the DUT-SP2 signal	Setup
▪ Average optical output power Popt2	Test Setup 1
Timing: ▪ Transferred Jitter via RMS ▪ Alignment Jitter acc. to Eye Mask ▪ Transition times (rise-/fall-times ($t_{r2,}$ t_{f2}))	Test Setup 2
Pulse shape: ▪ Optical Overshoot/Undershoot	Test Setup 2

Table 5-2: Summary of measurements at SP2 (DUT)

Note: All measurements have to be done with the stress pattern.

A detailed description of the measurement is given by the MOST150 oPhy Compliance Measurement Guideline [5].

5.7 Measurement of t_{Wakeup} and $t_{Shutdown}$

For verification of correct design of all physical layer components within devices, t_{WakeUp} and $t_{ShutDown}$ have to be measured using Test Setup 3. The tester is in master mode resp. in slave mode depending on the DUT.

1. Measurement of t_{WakeUp}:
   Starting from DUT in SleepMode (detectable by monitoring of power consumption), a wake-up event is applied to the DUT. The DUT has to generate the MOST signal within t_{WakeUp_max}.

2. Measurement of $t_{ShutDown}$:
   Starting from DUT in NormalOperation, the tester switches off the MOST signal. The DUT has to stop generating the MOST signal within $t_{ShutDown\_max}$.

6 Direct physical measuring accuracy

Requirement for measurement equipment distinguishes the following notions:

1. Requested accuracy
2. Validated measurement uncertainty: (95% confidence interval)
3. Systematic measurement deviation are either negligible or needs to be compensated.

Direct physical measuring accuracy:	
Operating voltage	± 0,05 V-range for full physical compliance ± 0,25 V-range for Limited Compliance / U_{Batt}
Current measurement	Accuracy: better than 2 µA
Optical power	± 0,5dB-range for setup ± 0,25dB-range for measuring equipment (means optical power meter with SP2 adapter)
Timing, optical signals	Measurement Accuracy for optical values: ***Transition time***: Mean value, Accuracy: ±50 ps In case of discrepancies the measurement has to be performed with different UI classes. ***Overshoot/ Undershoot mask***: Accuracy: a) timing: mask already considers margin b) amplitude: depending on SNR Overshoot/ Undershoot mask measurement is a pass / fail test. SNR min for measurement setup: see Note 1 below. In case of mask violations, the impact of noise in the measurement setup needs to be considered (see Note 2 below). If the violation is in the range of the measurement accuracy (according to SNR), the result will be judged as passed. If the violation is out of the range of the measurement accuracy (according to SNR), a compensation of the mismatch due to the insufficient SNR must be applied. ***Alignment Jitter according to eye mask:*** Alignment Jitter according to eye mask measurement is a pass / fail test. Jitter measurement depending on SNR. SNR min for measurement setup: see Note 1 below In case of mask violations, the impact of noise in the measurement setup needs to be considered (see Note 2 below). If the violation is in the range of the measurement accuracy (according to SNR), the result will be judged as passed. If the violation is out of the range of the measurement accuracy (according to SNR), a compensation of the mismatch due to the insufficient SNR must be applied.

	Transfer Jitter: Accuracy: ±10 ps. SNR min for measurement setup: see Note 1 below.
Timing, electrical	***Signal timing:*** 20 ps for measurement equipment ***Transfer Jitter:*** Accuracy: ±10 ps. ***On-/Off Behavior:*** ± 100 ns full physical compliance ***Timing for*** t_{Wakeup}, $t_{Shutdown}$: 0,5 ms
Temperature	± 2°C
Mechanical dimensions	0,1mm.

Note 1 – SNR min:

For SP2 measurements, it is required that the Test System has to achieve at least the following SNR values according to the specified validation method for SNR.

Category FOT: SNR > 8

Category Device: SNR > 6

Note 2 - concerning the optical signal timing:
In contrast to measurements in the electrical domain, the determination of optical timing and pulse shape parameters requires usage of optical electrical converters (OECs), transferring optical signals into the electrical domain. (Example for measurement setup, see [5], section 4.4.3) However, these converters introduce additional signal degradation, mainly by adding amplitude noise to the measured signal.

The signal amplitude on the OEC's output depends on the optical input power of the signal being applied to the OEC. Assuming a constant noise figure as a characteristic of such an OEC, the signal-noise-ratio SNR varies with the optical input power. Furthermore, the sampling unit of the oscilloscope may add uncertainties, for instance by adding sampling noise in the A/D-conversion. Considering the need to adapt the vertical resolution to the particular signal amplitude, this impact will vary with the amplitude swing and will overlay with the OEC's SNR characteristic.

Amplitude noise, created by the measurement system, impacts the verification of amplitude limits (e.g. pass/fail test using Over- / Undershoot mask) as well as determination of pure timing parameters. Timing parameters are always related to signal transitions, which are overlaid by the amplitude noise. The degradation in accuracy depends on the slew rate of these transitions.

The achievable measurement accuracy strongly depends on the signal's optical power. As a matter of fact, compliance verification requests measurements in a wide dynamic range of optical power. In addition to the specified SP2 power range, also losses due to the measurement setup need to be considered. However, a systematic measurement deviation (as shown with the OEC's amplitude noise) shall be excluded from the measurement result.

As a consequence some specific regulations for measurements at SP2 were defined:

- Minimum SNR for the measurement setup in dependency of optical input power
- Procedure, how to handle PASS/FAIL-Tests
- Usage of parameter-averaging for parameter transition times

Table 6-1: Summary of accuracy of measurement setup

7 General Remarks

7.1 Definition of family

Definition of "family" to minimize test effort for a couple of products with many similarities. A family member is a variation of parameter invariant to MOST Compliance Verification
e.g.

- pigtail with different fibre length in range of already tested fibre lengths
- pigtail with different shielding
- pigtail with different pin orientation (90° / 180°)
- and supersets

In case a change supersedes the already tested range it has to be considered as "level 3" change.

Note: Change of FOT implies a new family.

7.2 Product changes

Guideline for supplier in case of product changes:

Changes, that may impact

- the optical path or
- mechanical/optical interface

and which have to be considered as "level 3" changes:

- Coupling concept
- Fixation of the ferrule
- Fibre type
- Extension of temperature range
- Change of component manufacturer (e.g. FOT)
- Material in the optical path
- Receiver and transmitter chips / changes of FOT
- Measurement Verification not performed in case of connector interface changes
- (Refer also recommended Guideline AEC-Q100, p. 19, col. E5, Electrical Distribution, http://www.aecouncil.com)

Note: Of course, this guideline is valid for changes during product development process, too.

Note:
Treatment of Pigtail with different (electrical) connector interface:

In case the construction does not change the principal optical path, only the mechanical/optical interface has to be tested.
Consequently this will be seen as level 3 change.

Example:
Pigtail-Family1 (with FOT1) and Pigtail- Family2 (with FOT2) have been both tested for Full Physical Compliance.
A device using Pigtail-Family1 (with FOT1) has been tested for Limited Physical Compliance.
Layout or circuitry or application or power supply changed?

- Yes: level 3 change
- No: level 2 change

7.3 Consideration of sample frequency

The procedure for Compliance testing with different sample frequencies FS will be as follows:

- Limited Physical Compliance:
  Each supported FS has to be tested, i.e. a device supporting FS 44,1 kHz and FS 48 kHz has to be tested for both frequencies. The supported frequencies will be marked in the MCPL.

- Full Physical Compliance:
  - For FOTs each supported FS has to be tested, i.e. a FOTsupporting FS 44,1 kHz and FS 48 kHz has to be tested for both frequencies. The supported frequencies will be marked in the MCPL.
  - As Pigtails will not be affected by the sample frequency FS the test with one FS will be sufficient.

Clarification Compliance testing with different sample frequencies FS:
“For electronic control units (ECU) the limited physical compliance will be done at the specified frame sampling rate.
If the FOT is not tested for Full Physical Layer Compliance at this frame sampling rate, at least the data sheet of the FOT must cover this sampling rate. If the sampling rate of the ECU is not covered by the data sheet of the FOT, the ECU is not compliant because the components are operated outside of the FOT specification.

The compliance testing of pigtails is not affected by the sampling rate, because for the Full Physical Layer test of pigtail subset, one frame sampling rate is sufficient.”

8 Appendix A:Index of Figures

9 Appendix B: Index of Tables

Notes: