# MOST

**M**edia **O**riented **S**ystems **T**ransport

**Multimedia and Control
Networking Technology**

**MOST Electrical Physical Layer
Compliance Specification
Rev 1.0
06/2006**

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## Contents

## Document Structure

**All documents this MOST document is referring to are listed here with the actual revision.**

| Document | Revision |
|---|---|
| MOST Specification of Electrical Physical Layer | 1V1_00 |
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# Document History

Initial Release: 04/2006

First version 1.0-00

| Change Ref. | Section | Changes |
|-------------|---------|---------|
| 1V0_00 | - | First issue |

# 1 Introduction

The Electrical Physical Layer Compliance Specification is part of the MOST® (Multimedia Oriented System Transport) system. This document, the "MOST Electrical Physical Layer Compliance Specification", defines the requirements of test equipment, measurement setups and procedures for verifying the Specification Points (SP's) at the Device Level.

A Device is considered a MOST Compliant Device if and only if the device is tested according to the exact procedures described in this document and fulfills the criteria of each measurement listed in the MOST Electrical Physical Layer Specification.

## 1.1 Measurement Level

This specification measures the performance of a MOST50 Device (sometimes called a node or module) such as a CD changer, display module, head-unit, etc.

## 1.2 Responsibility

A MOST50 ePHY System is a complex combination of many devices from several suppliers. These devices are integrated into a complete system by the System Integrator or car-maker. Due to the numerous parties involved in the design and implementation of these systems, it is necessary to define responsibilities for certain segments of the system. The measurements defined in this specification are the responsibility of the OEM (Original Equipment Manufacturer), or supplier.

# 2 Test Equipment Requirements

The device and test equipment must be prepared in order to perform the Compliance Test. This chapter lists and explains the equipment required by the Compliance Test. The party responsible for preparing each piece of equipment is also listed.

To be able to perform all the tests described by the current document (get a certification), the laboratory and device supplier will need a minimal set of equipment with the following requirements:

## 2.1 Test Equipment for the Signal Compliance

### 2.1.1 Device Under Test

**Description:**
The device under test (DUT) is the MOST50 ePHY device submitted to the test house by the supplier for compliance testing. The DUT should be configured for the intended mode of operation in the vehicle (i.e. timing-master or timing-slave, sampling rate, etc.).
**Responsibility:**
Supplier

### 2.1.2 Digital Oscilloscope

**Description:**
The digital storage oscilloscope used should be able to work with active differential probes, have a minimum bandwidth of 500 MHz and at least a 5 GS/s sampling rate. It should also be able to accumulate at least 100,000 Unit Intervals of the measured signal, and have either built-in features for performing eye-diagram measurements with user-defined masks, or have an interface to an external software package to perform this task. The eye-diagram feature or external software should be able to generate its clock from the recovered data; the (software) PLL settings should be user programmable.

The mask feature or external software should offer user defined masks and be capable of detecting/counting mask violations.

The oscilloscope should also be capable of filtering and calculating the skew of a captured waveform versus an internally generated, ideal clock. Math functions within the oscilloscope shall be able to calculate the RMS (Root Mean Square) value or standard deviation of the skew.

The oscilloscope should be set to sample at 5 G samples/s and the internal PLL should be configured with a single pole frequency of 125 kHz. The oscilloscope should be run until at least 100,000 UI have been acquired.

One example of the digital oscilloscope satisfies the above requirement is "LeCroy WaveRunner 6100A (1GHz Digital Oscilloscope)"

**Responsibility:**
Test House

## 2.1.3 Differential Probe

**Description:**
The differential probe should be an active probe with input parameters (differential): C < 2 pF, R > 100 kOhm and bandwidth of at least 500 MHz. It should have an input dynamic range of min. 2 Vp-p diff. and a common mode range of ± 5 V.

One example of the differential probe satisfies the above requirement is "AP034 (1GHz Differential Probe)" which is the optional part of "LeCroy WaveRunner 6100A (1GHz Digital Oscilloscope)"

**Responsibility:**
Test House

## 2.1.4 Signal Generator

**Description:**
The Signal Generator should be a Tektronix AWG600 or AWG700 series Arbitrary Waveform Generator.

Appropriate data streams are provided with the electronic version of this specification.

The Signal Generator is used in two different methods depending on the test:
- Ideal Signal Transmitter: The Signal Generator is used as ideal transmitter when the Transmission Quality (refer to 3.1.1 Transmission Quality (SP2E)) of a slave device is tested.
- Worst-case Signal Transmitter: The Signal Generator is used as worst-case transmitter when the Receiver Tolerance of SP3E (refer to 3.1.3 Receiver Tolerance (SP3E)) of a device is tested.

**Responsibility:**
Test House

## 2.1.5 Cable

**Description:**
The cable should be the cable that is selected by a car-maker.
**Responsibility:**
Supplier/OEM

## 2.1.6 Connector

**Description:**
The connector should be the connector that is selected by a car-maker
**Responsibility:**
Supplier/OEM

## 2.1.7 Termination Resistors

**Description:**
For some tests, termination resistors are inserted after the output of the DUT in order to provide a stable measurement. The value of the termination resistors should be 64.9 ohm 1%.
**Responsibility:**
Test House

## 2.1.8 Accessories

**Description:**
In some cases, external accessories (such as filters, impedance converters, transformers, etc.) that are not part of the above-described equipment will be necessary to build a test setup. Their parameters and working conditions must be chosen in such a way they don't compromise the parameters of the measurement equipment.
**Responsibility:**
Supplier/OEM

# 3 Compliance Verification

A device shall meet the requirements of signal quality and electromagnetic compatibility in order to be a MOST Compliant Device. This chapter shows the exact setup diagrams and explains the test procedures used to verify compliance.
Please note that a device only needs to fulfill the requirements of SP2E and SP3E for signal compliance. This is because SP2E and SP3E are points at the device level whereas SP1E and SP4E are points at the NIC level.

## 3.1 Signal Compliance (SP2E and SP3E)

A device consists of a transmitter, receiver and associated circuitry. Each device must transmit a signal within certain quality limits and receive signals of certain quality limits in order to achieve proper communication.
This section shows the test setups and procedures used to measure and verify the transmitter quality and receiver tolerance.

### 3.1.1 Transmission Quality (SP2E)

The following sections explain the test setup and test procedure for Transmission Quality at SP2E.

#### 3.1.1.1 Test Setup

Diagrams indicating the test setup used to capture an eye diagram for Device Transmission Quality are shown in Figure 3-1 and Figure 3-2. This specification point should be tested with the Device under test in one of the following configurations:
- Timing-master mode: when the DUT is a timing-master device
- Timing-slave mode: when the DUT is a timing-slave device

##### 3.1.1.1.1 Timing-master Mode

- Use the setup shown in Figure 3-1 when testing a DUT in Timing-master. The TX+ and TX- outputs of the device are terminated into a resistive load as shown in the figure.
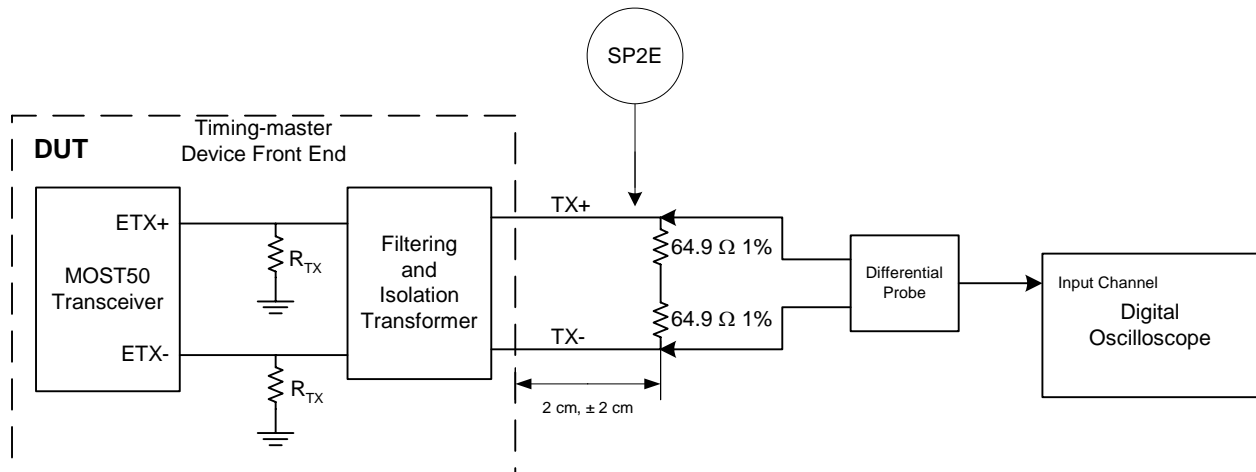
*Figure 3-1: Device Transmission Quality Test Setup (Timing-master mode)*

### 3.1.1.1.2  Timing-slave Mode

- Use the setup shown in Figure 3-2 when testing a DUT in Timing-slave mode.

The DUT is placed in node position 1 and locked to a reference signal from the Signal Generator.  The TX+ and TX- outputs of the device are terminated into a resistive load as shown in the figure.
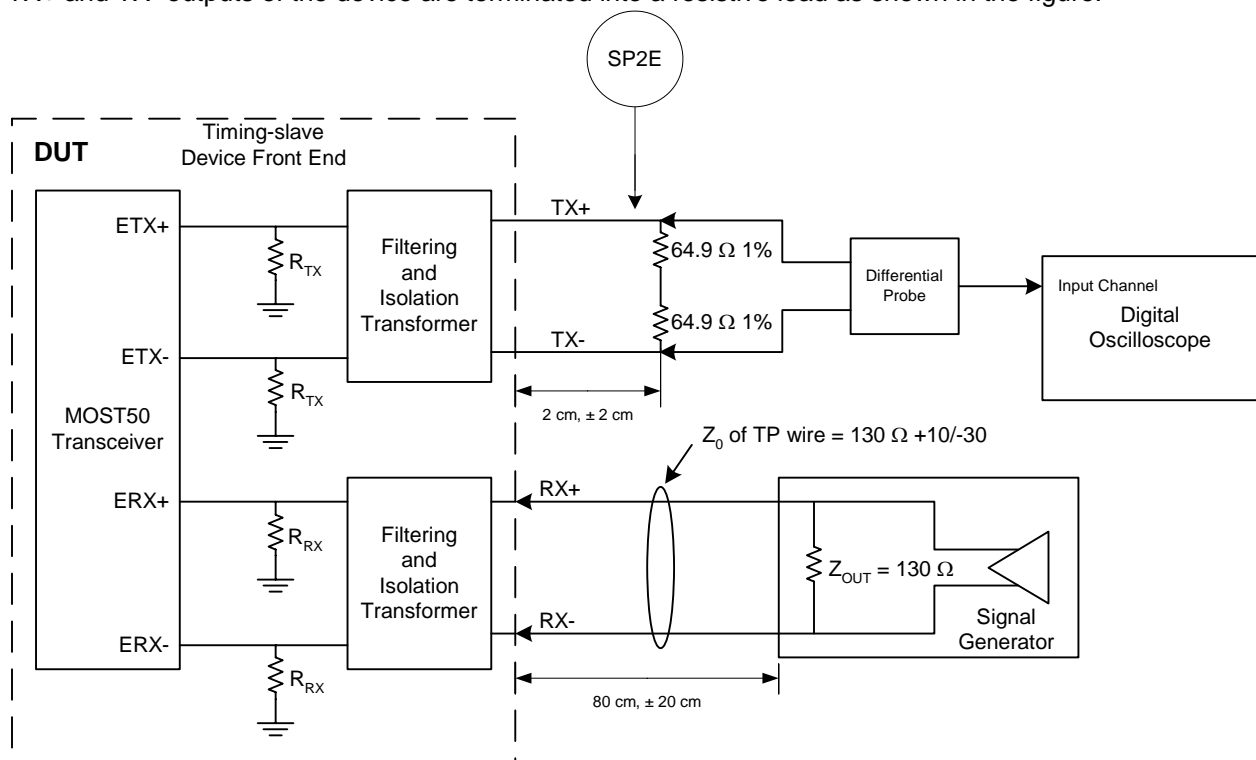


*Figure 3-2: Device Transmission Quality Test Setup (Timing-slave mode)*

## 3.1.1.2  Test Procedure

- Configure the oscilloscope to capture an eye diagram as detailed in the ePHY Specification using the SP2E eye mask specified in the ePHY Specification.
- If testing a timing-slave DUT, load the *SP2E Transmission Quality* test data stream, which is provided with the electronic version of this specification, into the signal generator.

- Configure the system as shown in either Figure 3-1 or Figure 3-2, depending upon the type of DUT submitted for testing.
- Apply power to the DUT and enable the output of the signal generator (if used).
- Ensure that the DUT is locked to the local crystal or signal generator.
- Attach the differential probe as shown in the test setups above.
- Capture enough UI in the eye diagram on the oscilloscope to satisfy the bit-error-rate requirements of the system.
- Evaluate the eye diagram against the SP2E eye mask.

The signal transmitted from SP2E should satisfy the criteria of SP2E specified in the ePHY Specification

## 3.1.2  Transferred Jitter (SP2E)

The following sections explain the test setup and test procedure for Transferred Jitter at SP2E.

### 3.1.2.1  Test Setup

This specification point should be tested with the device under test in one of the following configurations:
- Timing-master mode: when the DUT is a timing-master device
- Timing-slave mode: when the DUT is a timing-slave device

Transferred Jitter of the DUT for either mode (timing-master mode or timing-slave mode) is measured by capturing a long record of the signal at SP2E, using a software routine to generate a perfect clock from the captured data and then calculating the skew between the captured data and the perfect clock.

The test setups for each mode are described in following sections.

#### 3.1.2.1.1  Timing-master Mode

- Use the setup shown in Figure 3-3 when testing a DUT in Timing-master.  The TX+ and TX- outputs of the device are terminated into a resistive load as shown in the figure.
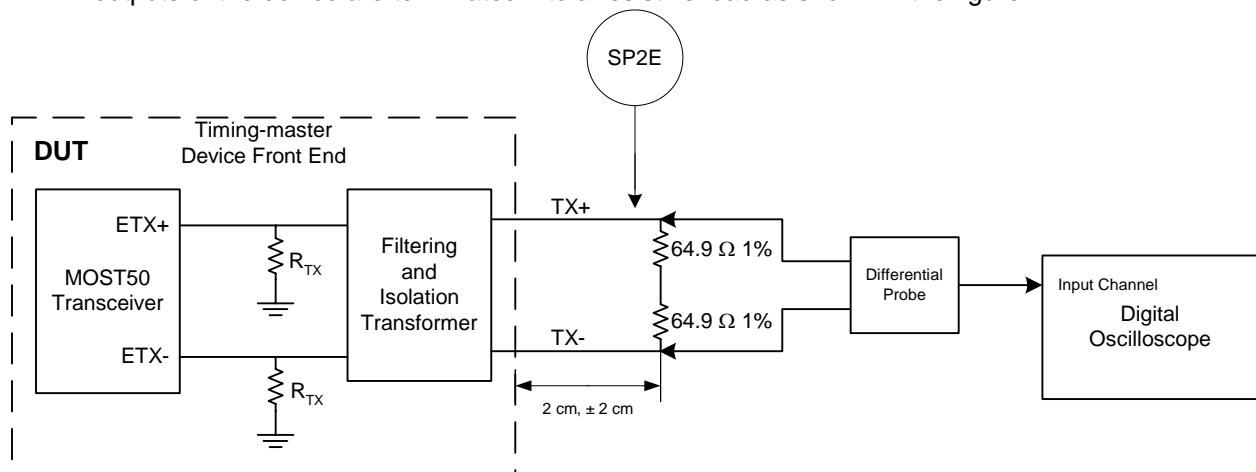


*Figure 3-3: Device Transferred Jitter Test Setup (Timing-master)*

#### 3.1.2.1.2  Timing-slave Mode

- Use the setup shown in Figure 3-4 when testing a DUT in Timing-slave mode.

The DUT is placed in node position 1 and locked to a reference signal from the Signal Generator.  The TX+ and TX- outputs of the device are terminated into a resistive load as shown in the figure.
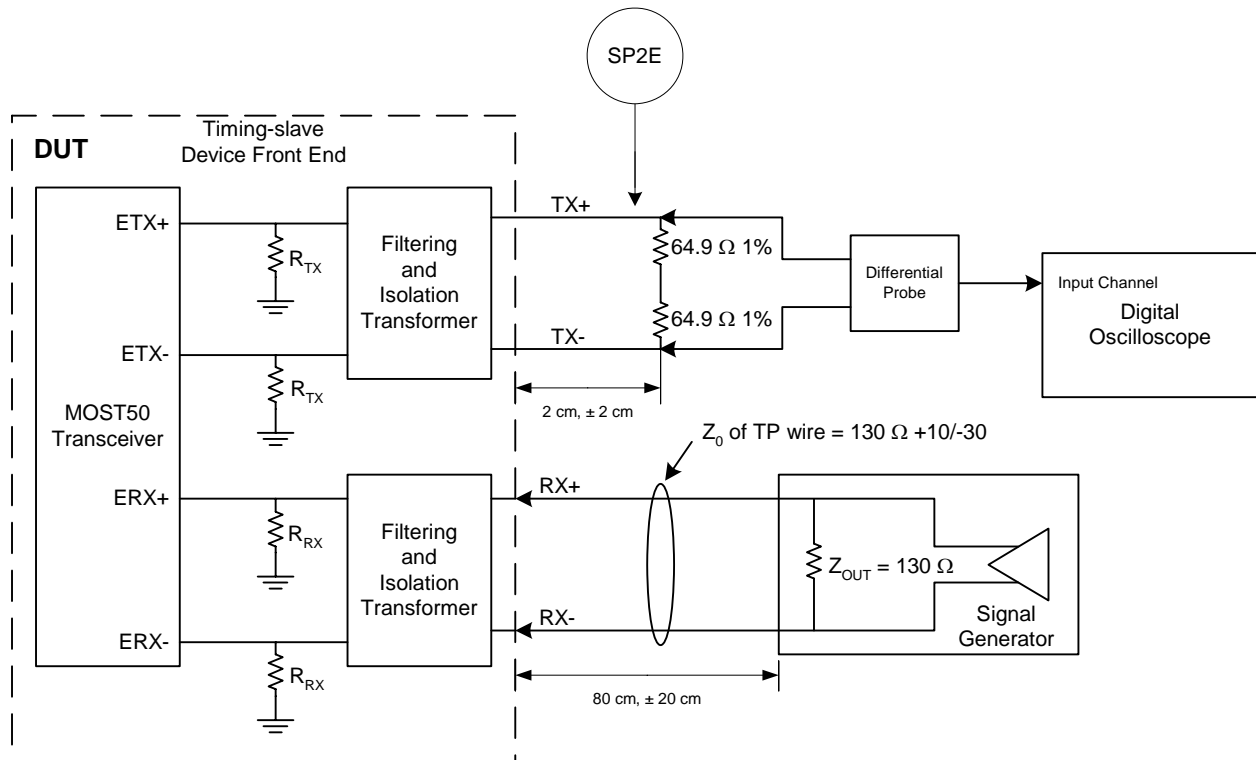
*Figure 3-4: Device Transferred Jitter Test Setup (Timing-slave mode)*

## 3.1.2.2  Test Procedure

- If testing a timing-slave DUT, load the *SP2E Transferred Jitter* test data stream, which is provided with the electronic version of this specification, into the signal generator.
- Configure the system as shown in either Figure 3-3 or Figure 3-4, depending upon the type of DUT submitted for testing.
- Apply power to the DUT and enable the output of the signal generator (if used).
- Ensure that the DUT is locked to the local crystal or signal generator.
- Attach the differential probe as shown in the test setups above.
- Capture enough UI in the eye diagram on the oscilloscope to satisfy the bit-error-rate requirements of the system.
- Generate an ideal clock based upon the captured data.
- Evaluate each captured data edge against the ideal clock and measure the time deviation from the expected position.  This is the "skew".
- Let the Digital Oscilloscope filter the skew values using the filter characteristics specified in the ePHY specification.
- Let the Digital Oscilloscope calculate the RMS (Root Mean Square) value (standard deviation) of the filtered skew values.  This is the Transferred Jitter in $ps_{RMS}$.

The signal transmitted from SP2E should satisfy the criteria for Transferred Jitter specified in the ePHY Specification

## 3.1.3 Receiver Tolerance (SP3E)

The following sections explain the test setup and test procedure for SP3E.

### 3.1.3.1 Test Setup

A diagram showing the test setup used to measure the receiver tolerance is shown in Figure 3-5. The Signal Generator, which simulates the worst-case transmitter, transmits the SP3E signal specified in the ePHY Specification.
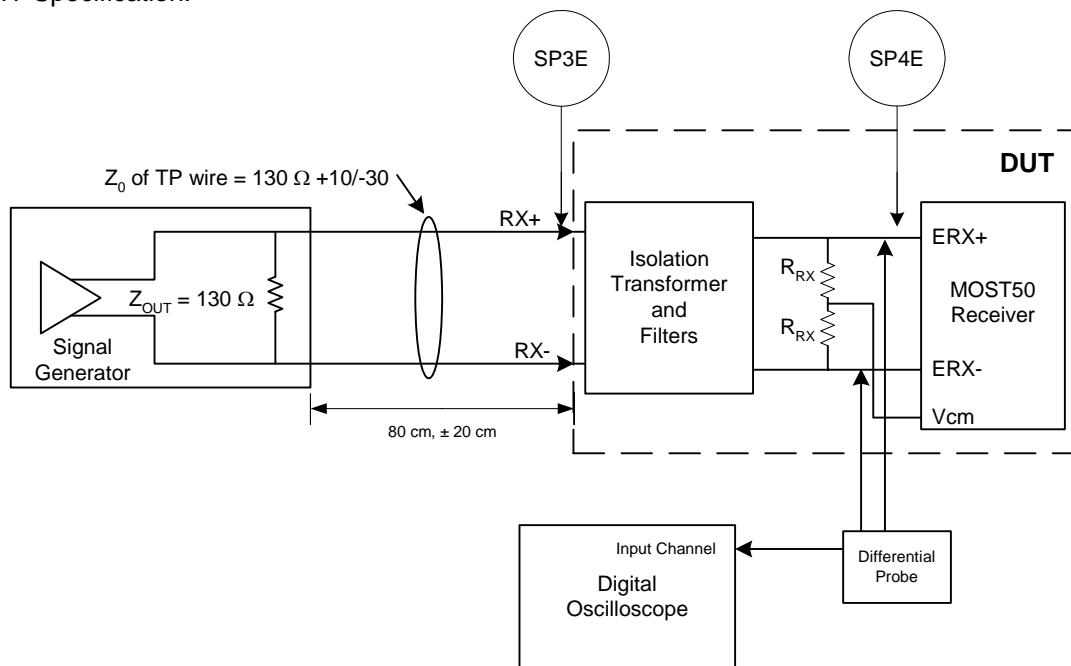


*Figure 3-5: Device Receiver Tolerance Test Setup*

### 3.1.3.2 Test Procedure

- Configure the oscilloscope to capture an eye diagram as detailed in the ePHY Specification using the SP4E eye mask specified in the ePHY Specification.
- Load the *SP3E Receiver Tolerance* test data stream, which is provided with the electronic version of this specification, into the signal generator.
- Configure the system as shown in Figure 3-5 depending upon the type of DUT submitted for testing.
- Apply power to the DUT and enable the output of the signal generator.
- Ensure that the DUT is locked to the signal generator.
- Attach the differential probe as shown in the test setup above.
- Capture enough UI in the eye diagram on the oscilloscope to satisfy the bit-error-rate requirements of the system.
- Evaluate the eye diagram against the SP4E eye mask.

The signal received at SP4E should satisfy the criteria of SP4E specified in the ePHY Specification.

# Appendix A. NIC Level Measurement (SP1E and SP4E)

This Appendix gives the information about mesuring procedure of SP1E and SP4E.
These procedures are not required for MOST Compliance.
The tests in this appendix are intended to measure the performance of the MOST50 Network Interface Controller (NIC).

## A.1 Transmission Quality (SP1E)

The following sections explain the test setup and test procedure for Transmission Quality at SP1E.

## A.1.1 Test Setup

Diagrams showing the test setup used to capture an eye diagram for NIC Transmission Quality are shown in Figure A-1 and Figure A-2. This specification point should be tested with the device under test in both of the following configurations:

- Timing-master mode: when the DUT is a timing-master device
- Timing-slave mode: when the DUT is a timing-slave device

A low-pass filter is used to band-limit the signal at the input to the oscilloscope. The filter details are defined in the next section.

### A.1.1.1 Timing-master Mode

Use the setup shown in Figure A-1 when testing a DUT in Timing-master mode. The ETX+ and ETX- outputs of the device are terminated into a resistive load as shown in the figure.
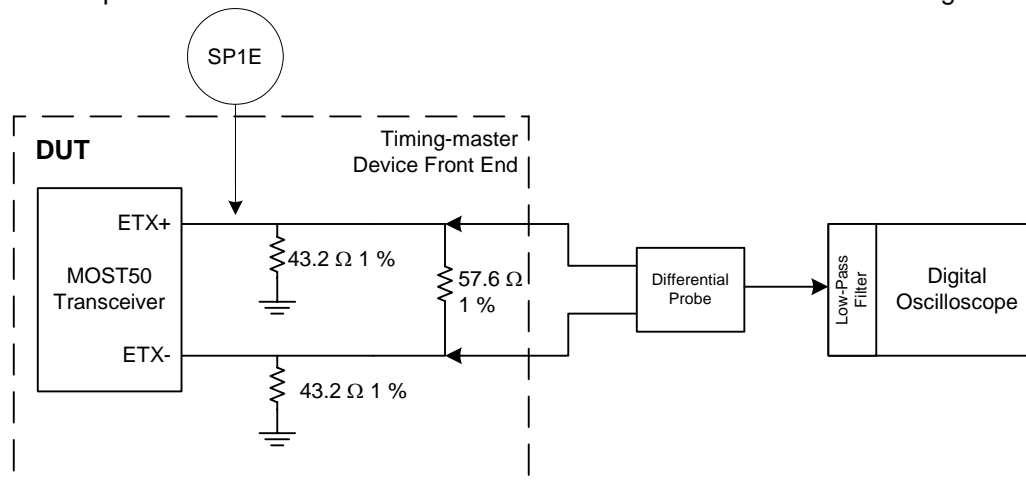


*Figure A-1: NIC Transmission Quality Test Setup (Timing-master mode)*

Note: The load termination resistor of 57.6 ohms is derived from the impedance transformation through the 1:1.5 turns ratio transformer used in the typical front-end circuit. The typical load termination of 130 ohms is divided by 2.25 which results in 57.78 ohms. 57.6 ohms is the nearest standard value to 57.8 ohms.

### A.1.1.2 Timing-slave Mode

- Use the setup shown in Figure A-2 when testing a DUT in Timing-slave mode. The DUT is placed in node position 1 and locked to a reference signal from the Signal Generator. The ETX+ and ETX- outputs of the device are terminated into a resistive load as shown in the figure.
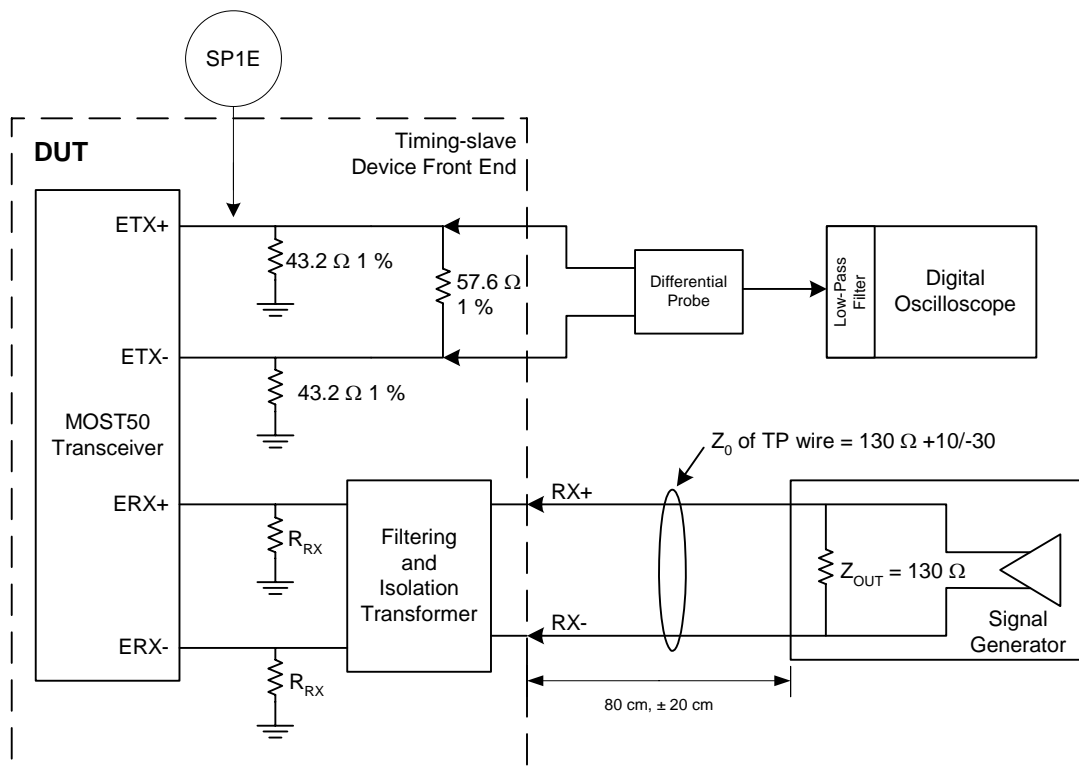
*Figure A-2: NIC Transmission Quality Test Setup (Timing-slave mode)*

Note: The load termination resistor of 57.6 ohms is derived from the impedance transformation through the 1:1.5 turns ratio transformer used in the typical front-end circuit. The typical load termination of 130 ohms is divided by 2.25 which results in 57.78 ohms. 57.6 ohms is the nearest standard value to 57.8 ohms.

## A.1.2 Test Procedure

- Configure the oscilloscope to capture an eye diagram as detailed in the ePHY Specification using the SP1E eye mask specified in the ePHY Specification.
- If testing a timing-slave DUT, load the *SP1E Transmission Quality* test data stream, which is provided with the electronic version of this specification, into the signal generator.
- Configure the system as shown in either Figure A-1 or Figure A-2, depending upon the type of DUT submitted for testing.
- Apply power to the DUT and enable the output of the signal generator (if used).
- Ensure that the DUT is locked to the local crystal or signal generator.
- Attach the differential probe as shown in the test setups above.
- Capture enough Unit Intervals in the eye diagram on the oscilloscope to satisfy the required bit-error-rate.
- Let the Digital Oscilloscope filter the captured data using the filter characteristics shown in Table A-1 and Figure A-3.
- Let the Digital Oscilloscope form an eye diagram based upon the filtered data.
- Evaluate the eye diagram against the SP1E eye mask.

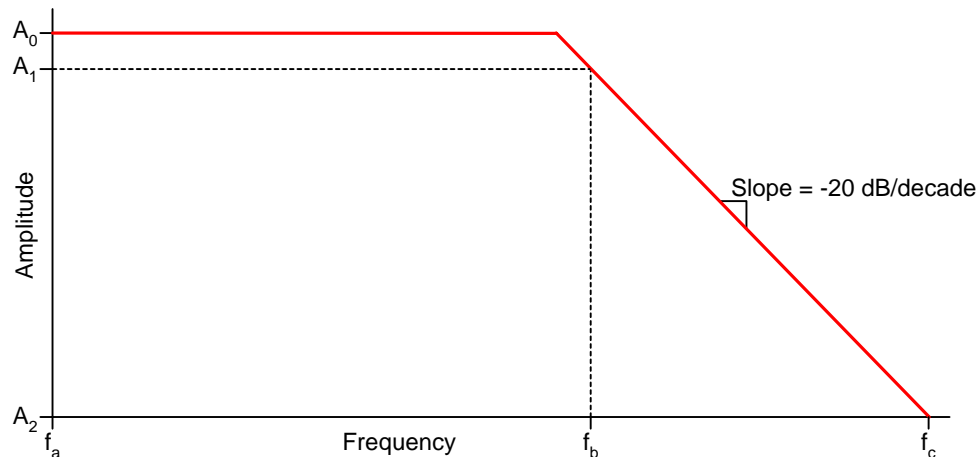| Parameter | Value | Unit |
|:---:|:---:|:---:|
| $A_0$ | 0 | dB |
| $A_1$ | -3 | dB |
| $A_2$ | -20 | dB |
| $f_a$ | 10 | kHz |
| $f_b$ | 40 | MHz |
| $f_c$ | 400 | MHz |

*Table A-1: SP1E Filter Characteristics*



*Figure A-3: SP1E Input Filter Template*

The signal transmitted from SP1E should satisfy the criteria of SP1E specified in the ePHY Specification

# A.2 Transferred Jitter (SP1E)

The following sections explain the test setup and test procedure for Transferred Jitter at SP1E.

## A.2.1 Test Setup

Diagrams showing the test setup used to capture an eye diagram for NIC Transferred Jitter are shown in Figure A-4 and Figure A-5. This specification point should be tested with the device under test in both of the following configurations:
- Timing-master mode: when the DUT is a timing-master device
- Timing-slave mode: when the DUT is a timing-slave device

A low-pass filter is used to band-limit the signal at the input to the oscilloscope. The filter details are defined in the next section.

### A.2.1.1 Timing-master Mode

Use the setup shown in Figure A-4 when testing a DUT in Timing-master mode. The ETX+ and ETX- outputs of the device are terminated into a resistive load as shown in the figure.
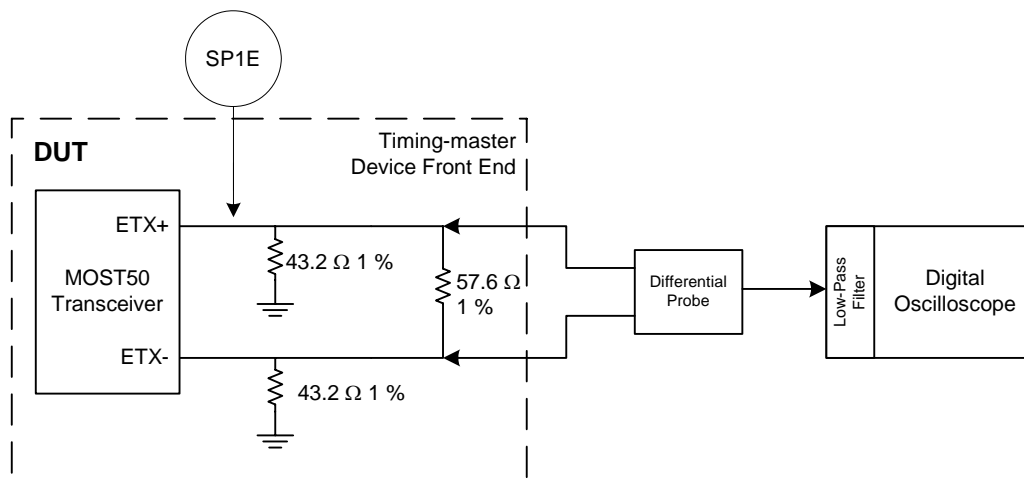
*Figure A-4: NIC Transferred Jitter Test Setup (Timing-master mode)*

## A.2.1.2 Timing-slave Mode

- Use the setup shown in Figure A-5 when testing a DUT in Timing-slave mode. The DUT is placed in node position 1 and locked to a reference signal from the Signal Generator. The ETX+ and ETX- outputs of the device are terminated into a resistive load as shown in the figure.
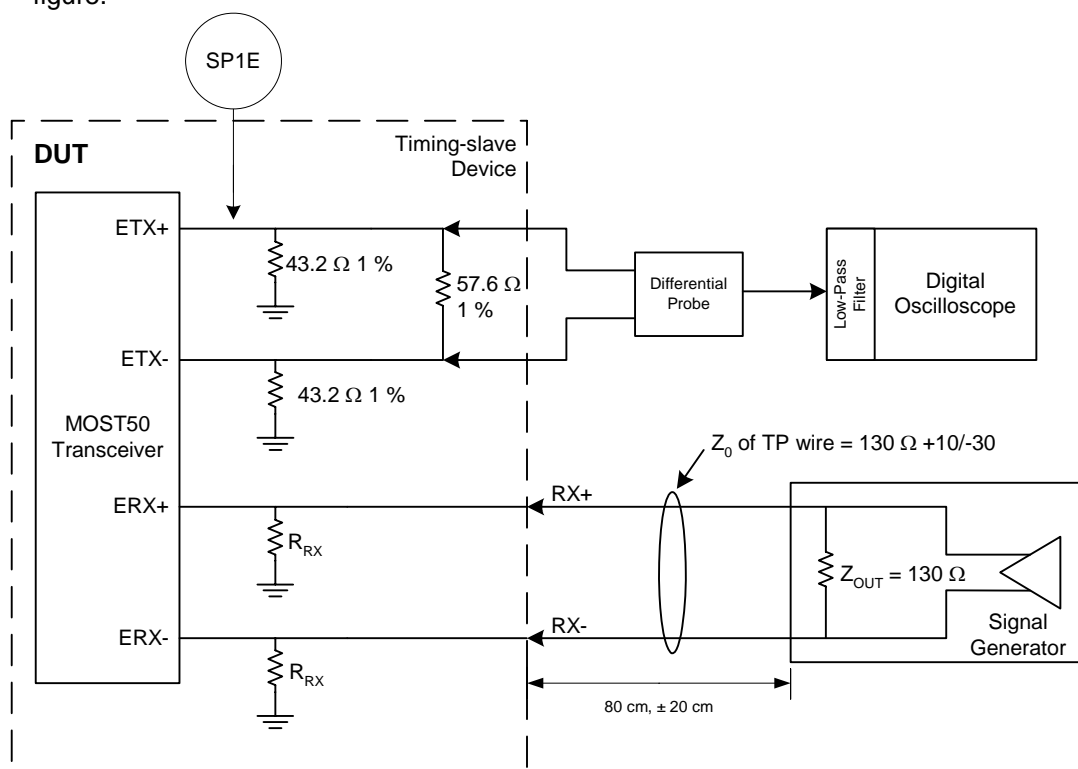


*Figure A-5: NIC Transferred JItter Test Setup (Timing-slave mode)*

## A.2.2 Test Procedure

- If testing a timing-slave DUT, load the *SP1E Transferred Jitter* test data stream, which is provided with the electronic version of this specification, into the signal generator.
- Configure the system as shown in either Figure A-4 or Figure A-5, depending upon the type of DUT submitted for testing.
- Apply power to the DUT and enable the output of the signal generator (if used).
- Ensure that the DUT is locked to the local crystal or signal generator.
- Attach the differential probe as shown in the test setups above.
- Capture enough UI in the eye diagram on the oscilloscope to satisfy the bit-error-rate requirements of the system.
- Generate an ideal clock based upon the captured data.
- Let the Digital Oscilloscope filter the captured data using the low-pass filter characteristics shown in
  Table A-1 and Figure A-3.
- Evaluate each captured data edge against the ideal clock and measure the time deviation from the expected position.  This is the "skew".
- Let the Digital Oscilloscope filter the skew values using the filter characteristics specified in the ePHY specification.
- Let the Digital Oscilloscope calculate the RMS (Root Mean Square) value (standard deviation) of the filtered skew values.  This is the Transferred Jitter in psRMS.
- The signal transmitted from SP1E should satisfy the criteria for Transferred Jitter specified in the ePHY Specification

# A.3 Receiver Tolerance (SP4E)

The following sections explain the test setup and test procedure for SP4E.

## A.3.1 Test Setup

A diagram showing the test setup used to measure the receiver tolerance is shown in Figure A-6.  The Signal Generator, which simulates the worst-case transmitter, transmits the SP4E signal specified in the ePHY Specification.
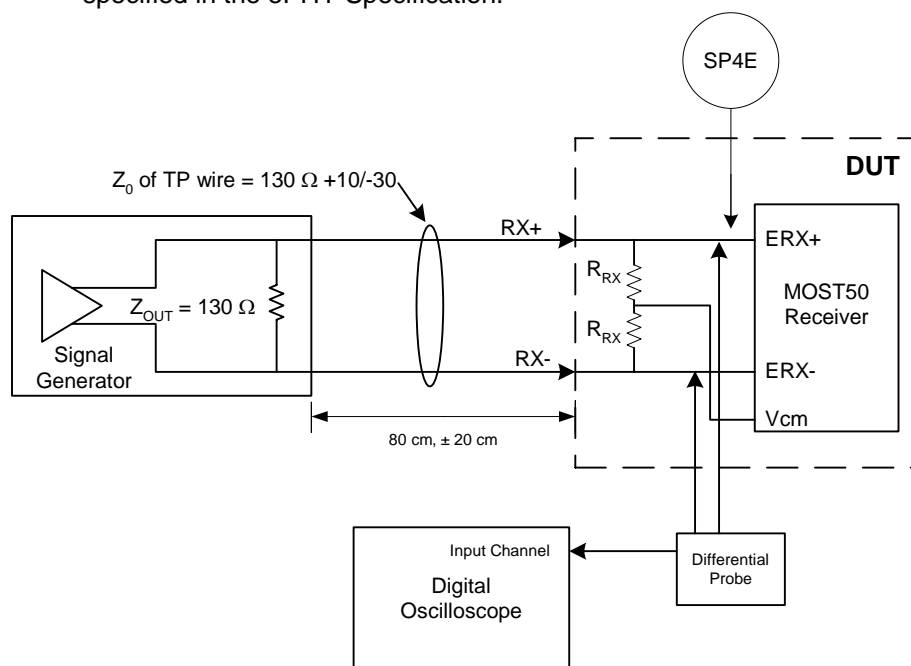


*Figure A-6: NIC Receiver Tolerance Test Setup*

## A.3.2 Test Procedure

- Configure the oscilloscope to capture an eye diagram as detailed in the ePHY Specification using the SP4E eye mask specified in the ePHY Specification.
- Load the *SPE4 Receiver Tolerance* test data stream, which is provided with the electronic version of this specification, into the signal generator.
- Configure the system as shown in Figure A-6 for testing.
- Apply power to the DUT and enable the output of the signal generator.
- Ensure that the DUT is locked to the signal generator.
- Attach the differential probe as shown in the test setup above.
- Capture enough Unit Intervals in the eye diagram on the oscilloscope to satisfy the required bit-error-rate.
- Evaluate the eye diagram against the SP4E eye mask to ensure a proper signal is generated.
- The NIC should be able to receive the signal without any errors.

# Appendix B. Index of Figures

# Appendix C. Index of Tables

Notes: