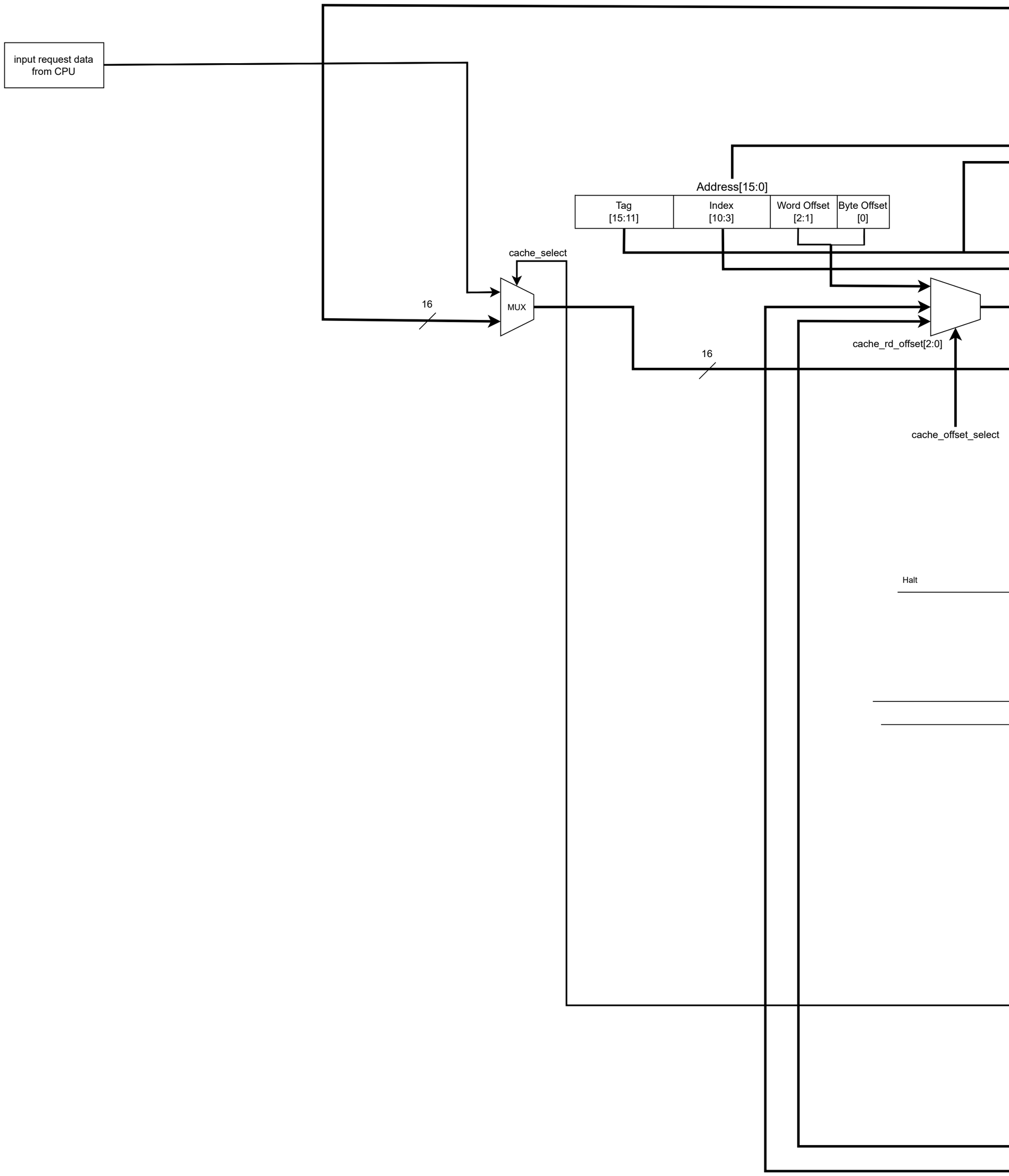
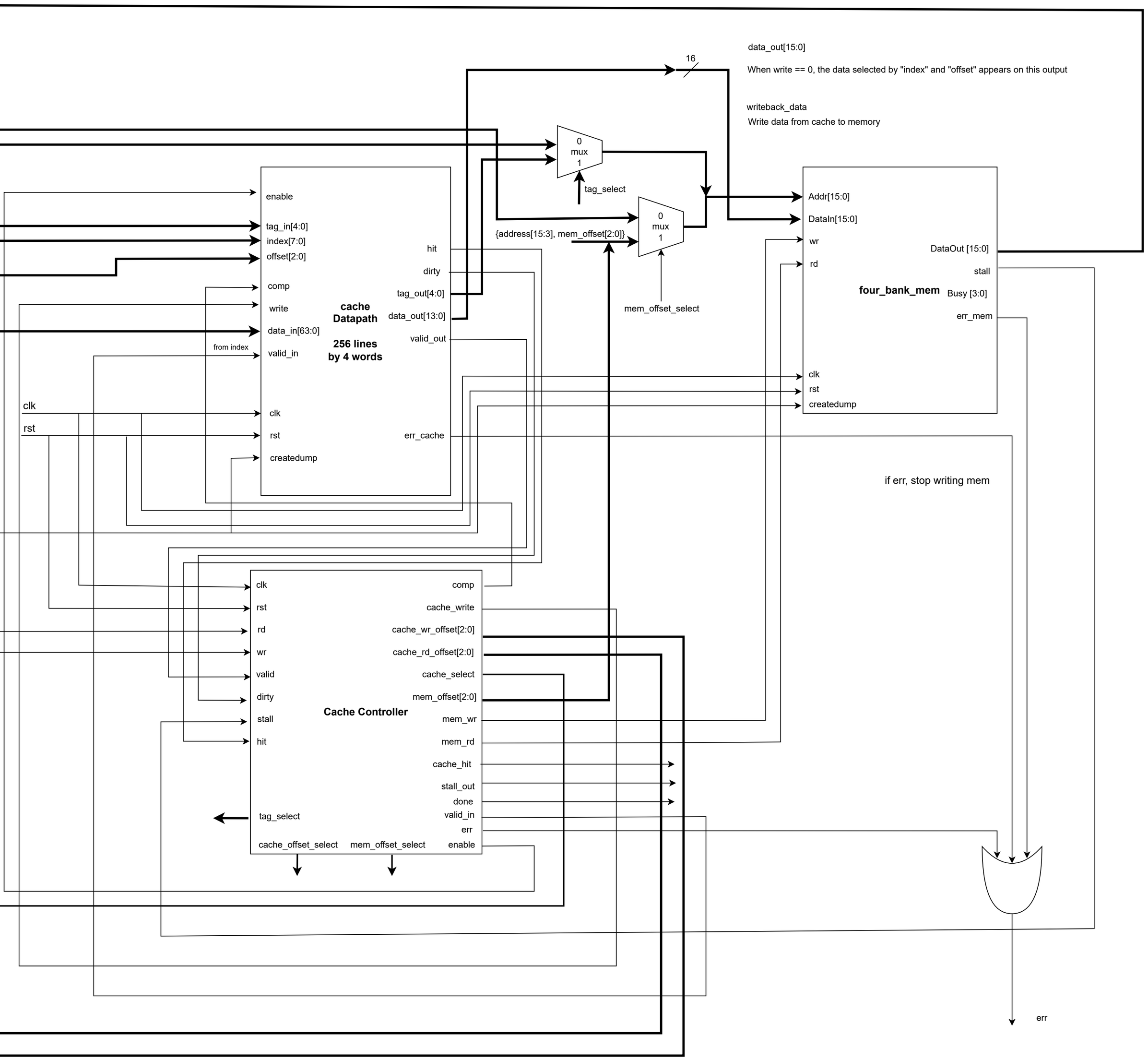

input request data
from CPU
Address[15:0]
Tag
[15:11]
Index
[10:3]
Word Offset
[2:1]
Byte Offset
[0]
cache_select
MUX
16
16
cache_rd_offset[2:0]
cache_offset_select
Halt


data_out[15:0]
When write == 0, the data selected by "index" and "offset" appears on this output
16
writeback_data
Write data from cache to memory
0
mux
1
tag_select
{address[15:3], mem_offset[2:0]}
mem_offset_select
enable
tag_in[4:0]
index[7:0]
offset[2:0]
comp
write
data_in[63:0]
from index
valid_in
clk
rst
createdump
hit
dirty
tag_out[4:0]
data_out[13:0]
valid_out
err_cache
cache
Datapath
256 lines
by 4 words
Addr[15:0]
DataIn[15:0]
wr
rd
DataOut [15:0]
stall
four_bank_mem
Busy [3:0]
err_mem
clk
rst
createdump
if err, stop writing mem
clk
rst
rd
wr
valid
dirty
stall
hit
comp
cache_write
cache_wr_offset[2:0]
cache_rd_offset[2:0]
cache_select
mem_offset[2:0]
Cache Controller
mem_wr
mem_rd
cache_hit
stall_out
done
valid_in
err
enable
tag_select
cache_offset_select
mem_offset_select
err