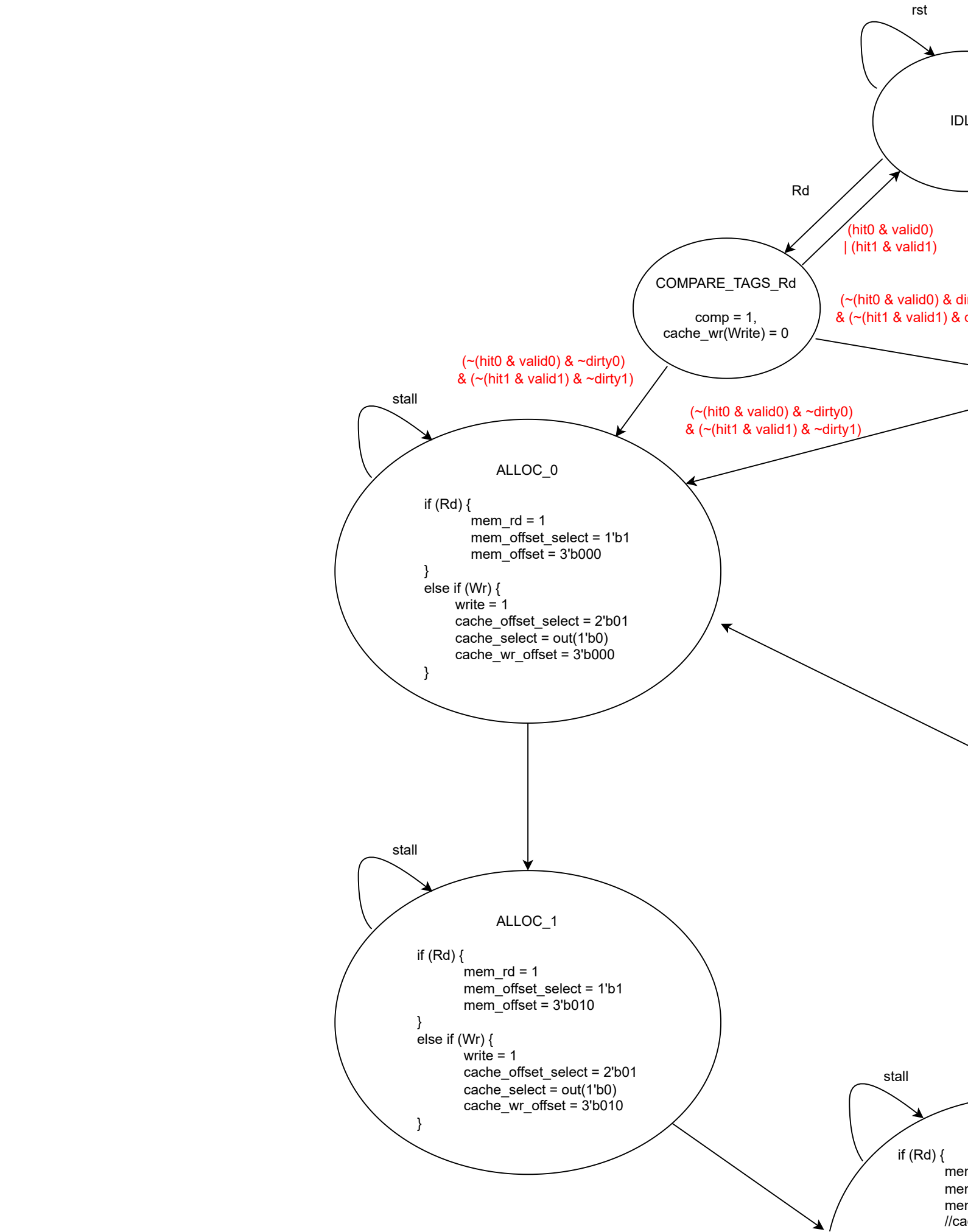
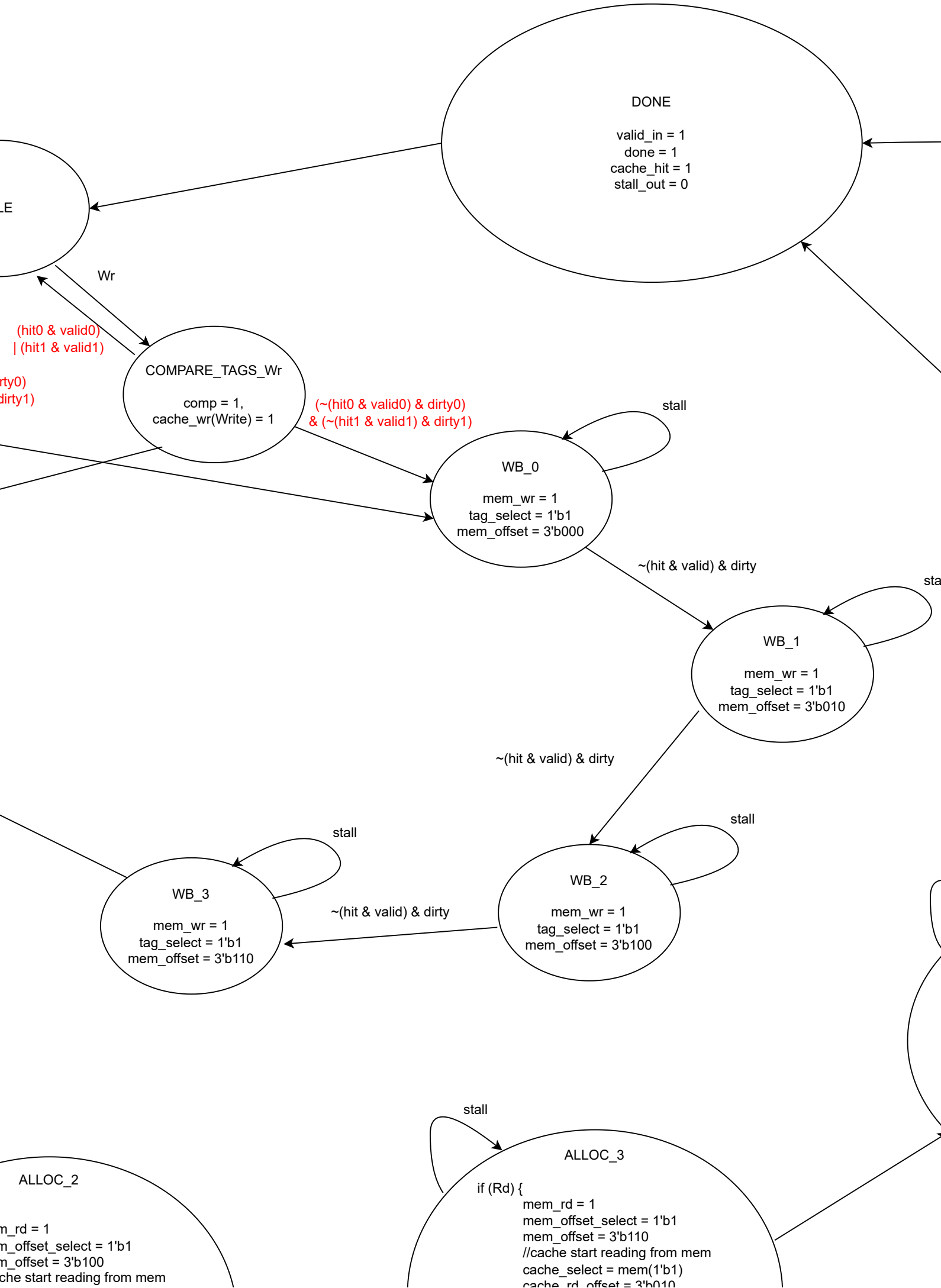
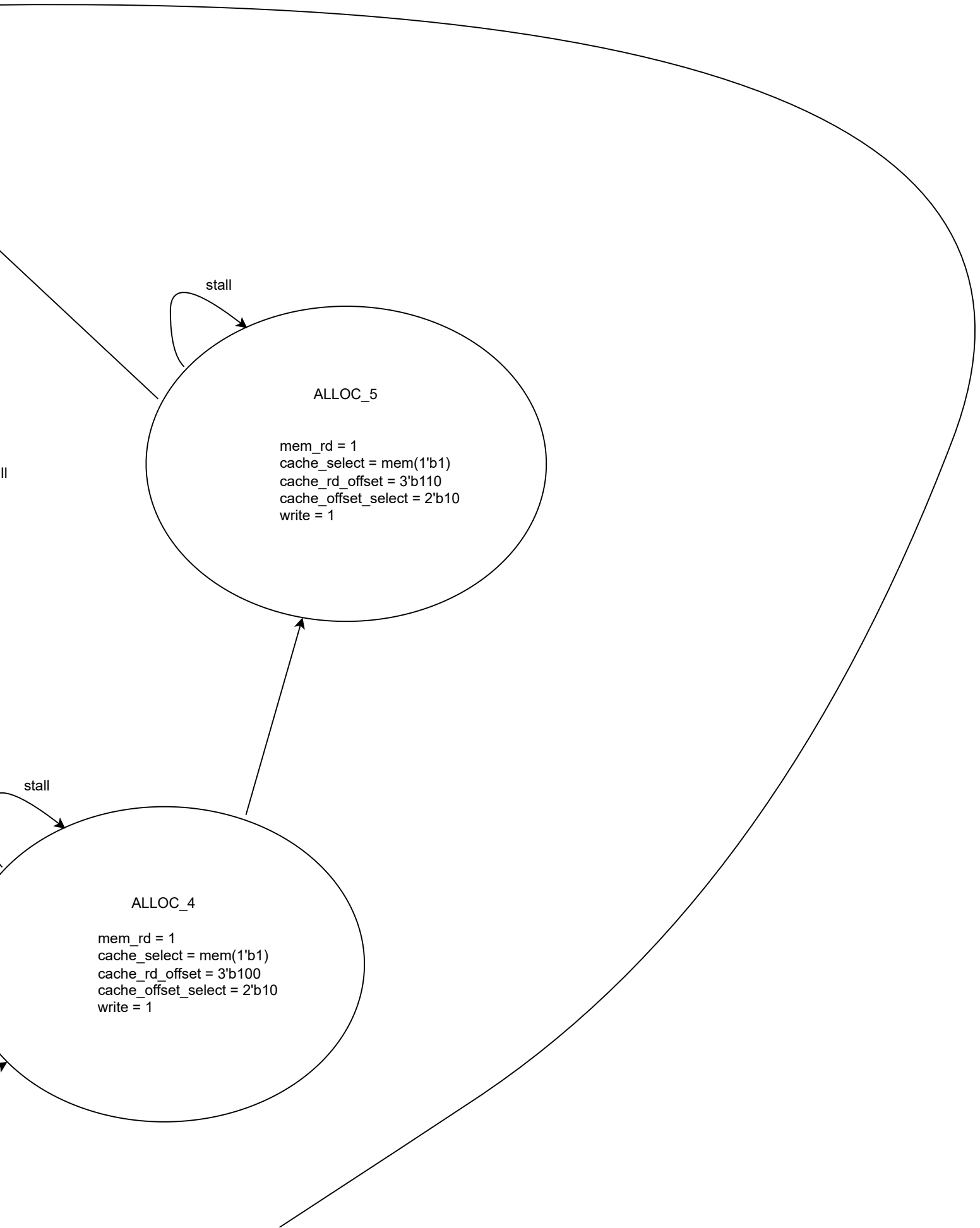
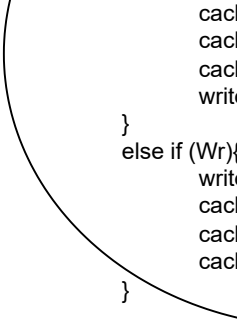
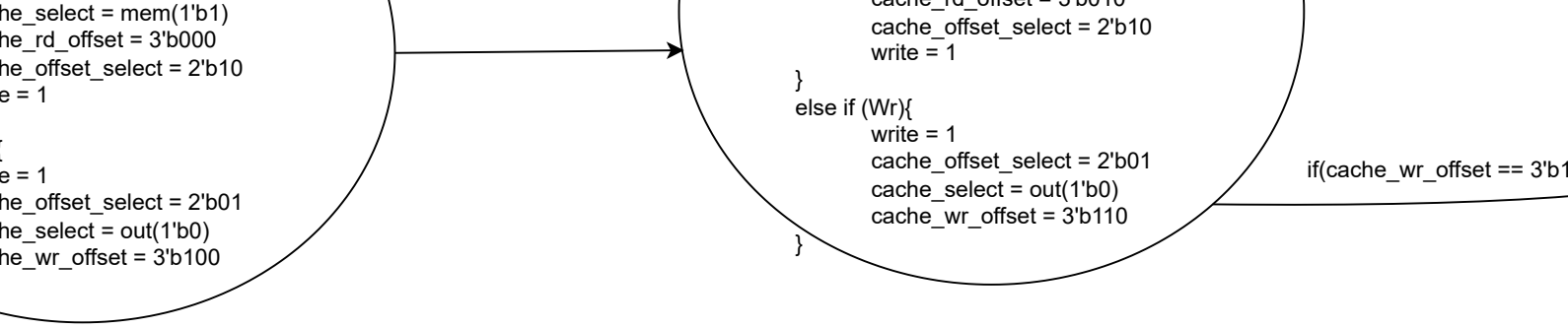
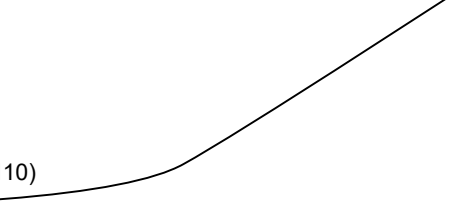

rst
IDL
Rd
(hit0 & valid0)
| (hit1 & valid1)
COMPARE_TAGS_Rd
comp = 1,
cache_wr(Write) = 0
(~(hit0 & valid0) & di
& (~(hit1 & valid1) & c
(~(hit0 & valid0) & ~dirty0)
& (~(hit1 & valid1) & ~dirty1)
stall
(~(hit0 & valid0) & ~dirty0)
& (~(hit1 & valid1) & ~dirty1)
ALLOC_0
if (Rd) {
mem_rd = 1
mem_offset_select = 1'b1
mem_offset = 3'b000
}
else if (Wr) {
write = 1
cache_offset_select = 2'b01
cache_select = out(1'b0)
cache_wr_offset = 3'b000
}
stall
ALLOC_1
if (Rd) {
mem_rd = 1
mem_offset_select = 1'b1
mem_offset = 3'b010
}
else if (Wr) {
write = 1
cache_offset_select = 2'b01
cache_select = out(1'b0)
cache_wr_offset = 3'b010
}
stall
if (Rd) {
mer
mer
mer
//ca


DONE
valid_in = 1
done = 1
cache_hit = 1
stall_out = 0
LE
Wr
(hit0 & valid0)
| (hit1 & valid1)
rty0)
dirty1)
COMPARE_TAGS_Wr
comp = 1,
cache_wr(Write) = 1
(~(hit0 & valid0) & dirty0)
& (~(hit1 & valid1) & dirty1)
stall
WB_0
mem_wr = 1
tag_select = 1'b1
mem_offset = 3'b000
~(hit & valid) & dirty
sta
WB_1
mem_wr = 1
tag_select = 1'b1
mem_offset = 3'b010
~(hit & valid) & dirty
stall
WB_2
mem_wr = 1
tag_select = 1'b1
mem_offset = 3'b100
stall
WB_3
mem_wr = 1
tag_select = 1'b1
mem_offset = 3'b110
~(hit & valid) & dirty
stall
ALLOC_3
if (Rd) {
mem_rd = 1
mem_offset_select = 1'b1
mem_offset = 3'b110
//cache start reading from mem
cache_select = mem(1'b1)
ALLOC_2
m_rd = 1
m_offset_select = 1'b1
m_offset = 3'b100
che start reading from mem


stall
ALLOC_5
mem_rd = 1
cache_select = mem(1'b1)
cache_rd_offset = 3'b110
cache_offset_select = 2'b10
write = 1
stall
ALLOC_4
mem_rd = 1
cache_select = mem(1'b1)
cache_rd_offset = 3'b100
cache_offset_select = 2'b10
write = 1


cach
cach
cach
write
}
else if (Wr){
write
cach
cach
cach
}


he_select = mem(1'b1)
he_rd_offset = 3'b000
he_offset_select = 2'b10
e = 1
e = 1
he_offset_select = 2'b01
he_select = out(1'b0)
he_wr_offset = 3'b100
cache_offset_select = 2'b10
write = 1
}
else if (Wr){
write = 1
cache_offset_select = 2'b01
cache_select = out(1'b0)
cache_wr_offset = 3'b110
}
if(cache_wr_offset == 3'b1


10)