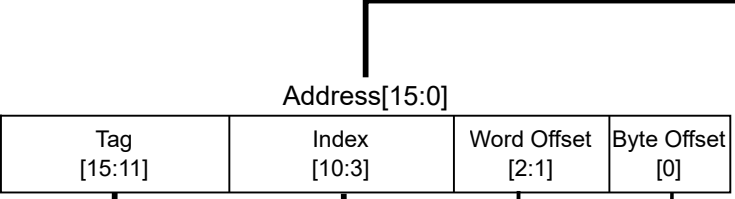


input request data
from CPU



cache_select

MUX

16

16

cache_rd_offset[2:0]

cache_offset_select

Halt

