ECE 752 HW3 Report

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Pre-Test Information

Test Machine: CSL machine

CPU information: Intel Core i5-11500 Processor, due to the website[1], the LLC size is 12MB.

Cache size information: running the command **getconf -a | grep CACHE**

```
LEVEL1_ICACHE_SIZE                 32768
LEVEL1_ICACHE_ASSOC
LEVEL1_ICACHE_LINESIZE             64
LEVEL1_DCACHE_SIZE                 49152
LEVEL1_DCACHE_ASSOC                12
LEVEL1_DCACHE_LINESIZE             64
LEVEL2_CACHE_SIZE                  524288
LEVEL2_CACHE_ASSOC                 8
LEVEL2_CACHE_LINESIZE              64
LEVEL3_CACHE_SIZE                  12582912
LEVEL3_CACHE_ASSOC                 16
LEVEL3_CACHE_LINESIZE              64
```

In summary, L1 cache size is 50KB, L1 cache line size is 64 Byte; L2 cache size is 524KB, L2 cache line size is 64 Byte, L3 cache size is 12MB, L3 cache line size is 64 Byte.

Cache Hierarchy Test Scheme

1. Create a memory space (buffer) with the specific size

2. Perform several random memory accesses with different sizes

3. Record the total time, calculate the average data throughput (kbps)

4. Analyze the relationship between size and throughput, get the cache hierarchy

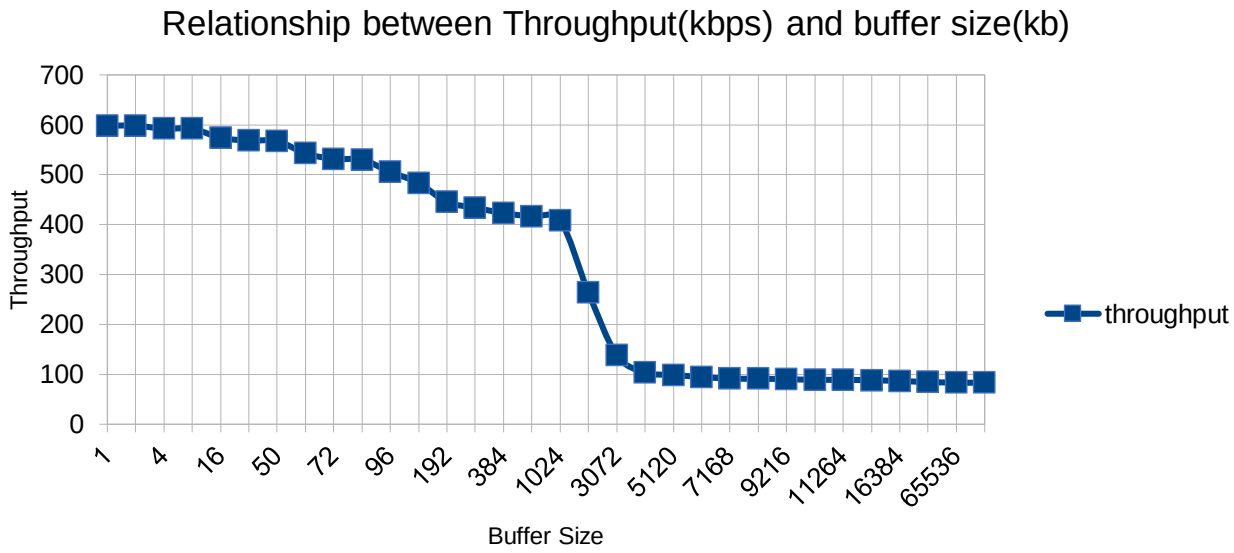

Figure 1

From Figure 1, when the size exceeds the size of certain level of cache, the cache read miss will increase and the throughput will decrease. The figure shows that cache hierarchy has 3 levels.

Cache Line Size Test Scheme

1. Create a memory space (buffer) with the specific size
2. Perform several random memory accesses with different strides
3. Record the total time, calculate the average data throughput (kbps)
4. Analyze the relationship between stride and throughput, get the cache line size

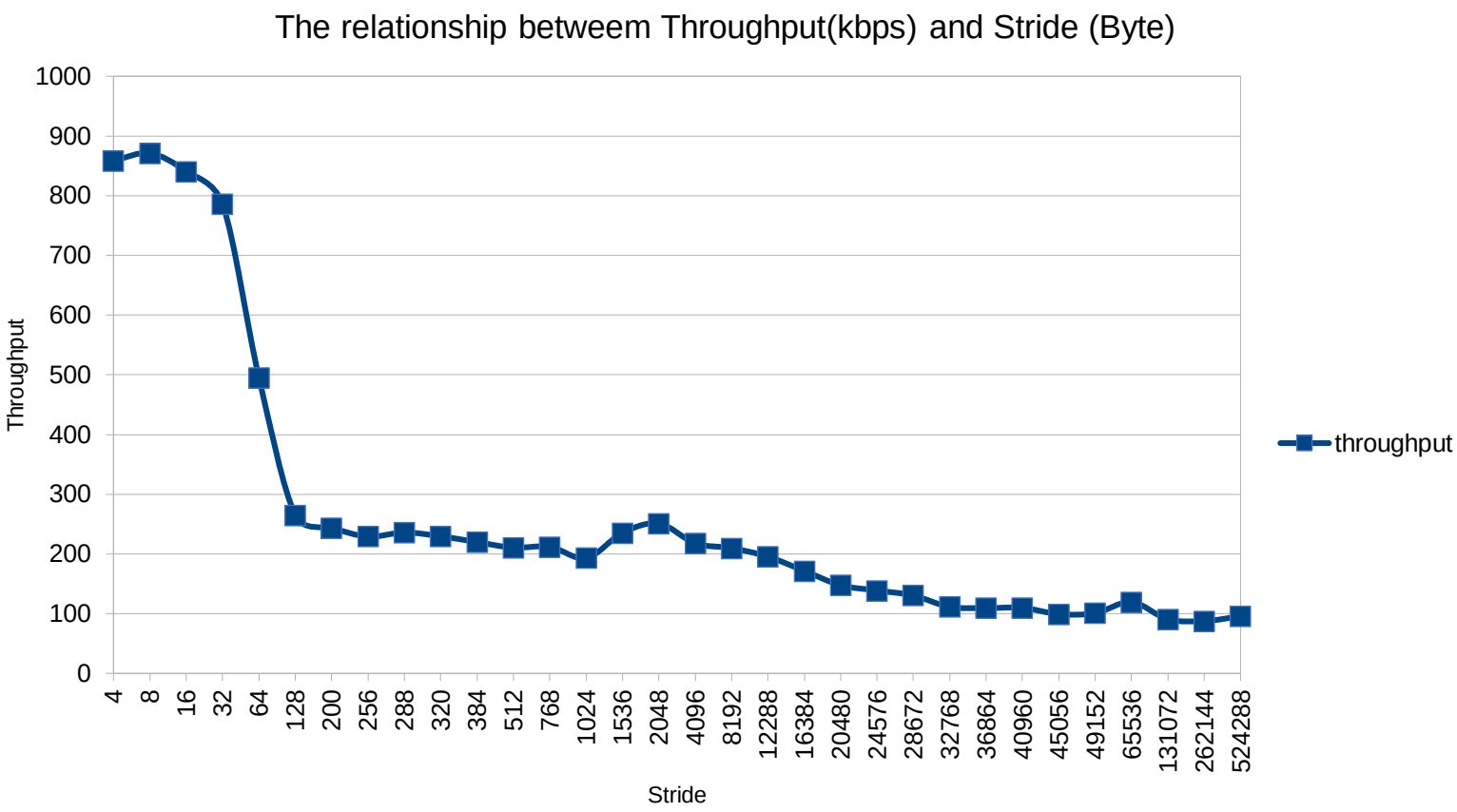

Figure 2

From Figure 2, we try to test L1 cache line size, when stride size exceeds the L1 cache line, all the accesses will miss, the throughput will drop significantly. We can repeat the process to get the L2, L3 cache line size. The figure shows L1 cache size is 64 Byte.

Memory Latency Test Scheme

1. Create a memory space (buffer) with the specific size
2. Perform several random memory accesses with different size
3. Record the total time, calculate the average latency (ms)
4. Analyze the relationship between latency and size, get the memory latency

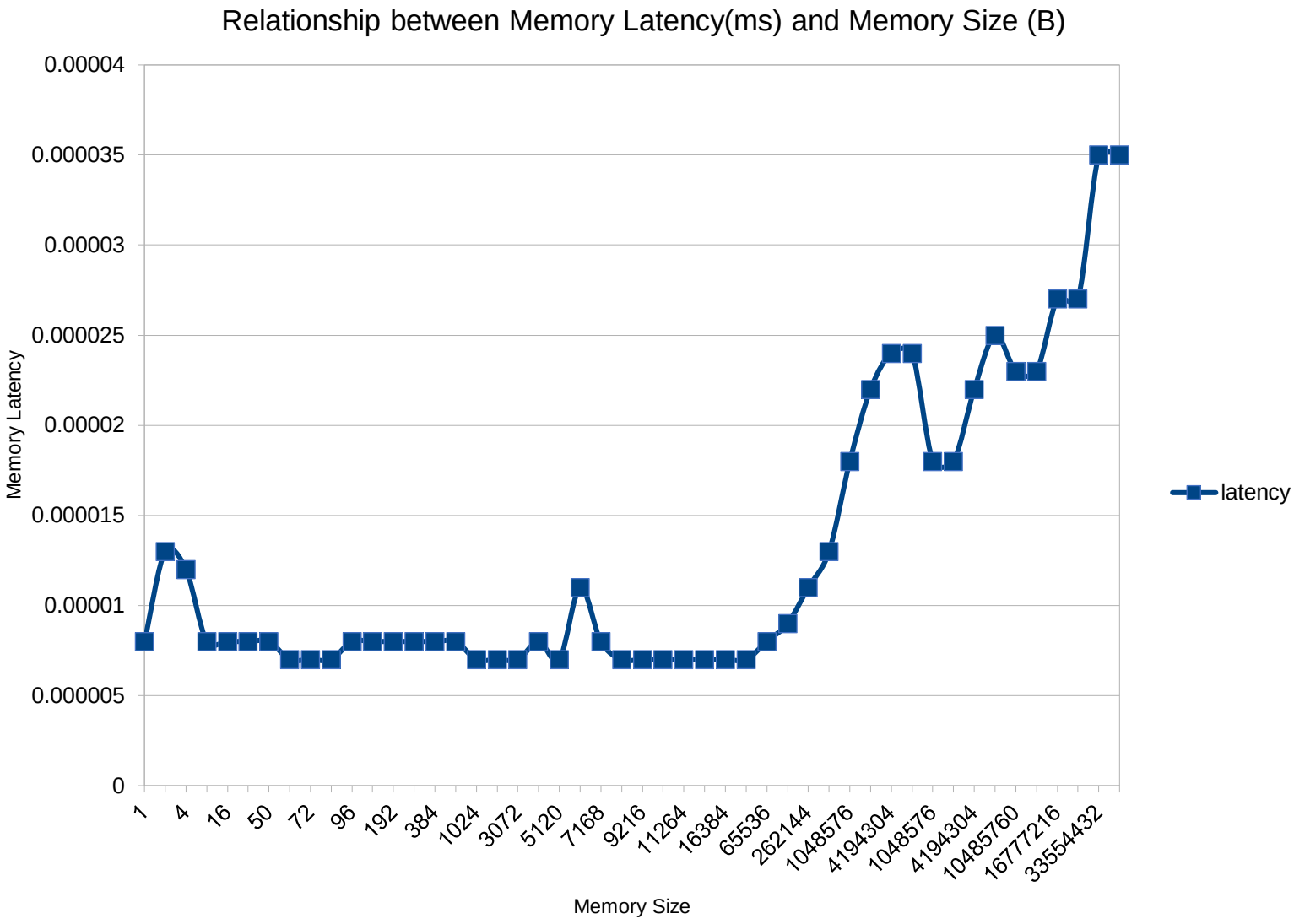

Figure 3

In Figure 3, the memory latency increases when test size increases. When the size is larger than LLC (12MB), the latency increases significantly, because the data access is between CPU and external memory DRAM. The internal memory (SRAM) access time span is approximately 7~8 ns, the external memory (DRAM) access time span is approximately 35 ns. In summary, the DRAM latency is around 5 times larger than SRAM.

Deviation Analysis

In this experiment, since CPU pre-fetch is not disabled, the memory access results are not accurate.

Reference

[1] https://ark.intel.com/content/www/us/en/ark/products/212277/intel-core-i511500-processor-12m-cache-up-to-4-60-ghz.html