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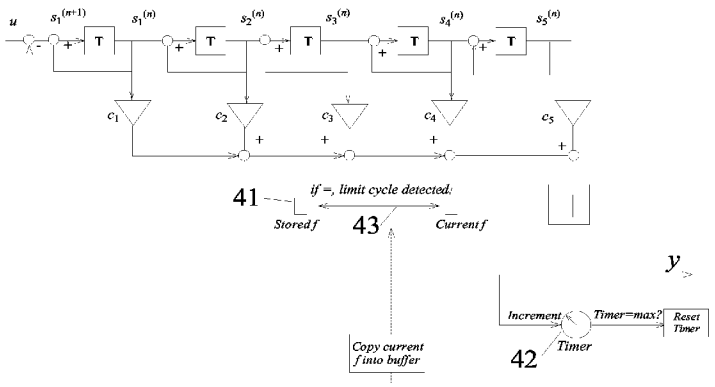

(57) Abstract: A method is provided for detecting limit cycles in a sigma delta modulator having an output signal that varies over a series of time intervals. In this method a first value that is indicative of the level of the modulator output signal after a predetermined time interval is stored in a first memory, and a second value that is indicative of the level of the modulator output signal after a further time interval subsequent to the predetermined time interval is stored in a second memory. The first value stored in the first memory is compared with the second value stored in the second memory, and an output indicative of a tendency for limit cycles to be produced in the modulator output signal is provided in response to such comparison. Such a method is particularly advantageous for detecting limit cycles in a sigma delta modulator as it can be implemented in a straightforward manner and offers a very accurate limit cycle detection mechanism. As a result it only becomes necessary to activate a limit cycle removal mechanism when limit cycle behaviour has been observed, and major changes to design are not normally required to implement the detection mechanism.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Sigma Delta Modulators

This invention relates to sigma delta modulators.

Sigma delta modulation is a popular method of converting electrical signals from analogue to digital form, and vice versa. Such a modulation technique typically involves converting an analogue electrical signal into a low-bit, highly oversampled digital representation. Furthermore the technique benefits greatly from the oversampling in that a feedback path may be used to shape the quantization noise into high frequencies where it is not noticeable. Due to its low circuit complexity and robustness against circuit imperfections, one-bit sigma delta-based analogue-to-digital and digital-to-analogue converters are widely used in audio applications, such as cellular phone technology and high-end stereo systems.

Figure 1 is a circuit diagram showing a generic example of a feedforward sigma delta converter often used in analogue to digital conversion. This converter uses a feedback system having an input line 11 for an analogue input signal to be converted terminating at a loop filter 12 containing a number of integrators corresponding to the order of the sigma delta modulator. Each integrator outputs a state space variable that is multiplied by a suitable coefficient in a respective amplifier 13, the outputs of all the amplifiers 13 being summed in an adder 14. The resulting summed output is quantised to plus or minus one in a quantiser 15, depending on the sign of the sum, and the quantised value is passed to the output line 16 as the output bit, and also subtracted from the input signal supplied on the input line 11.

However, sigma delta modulators may suffer from limit cycles in which the output bits enter a repeating pattern, and current methods of preventing this phenomenon introduce unwanted noise, do not always succeed, and are often implemented when not needed.

Sigma delta modulation, as originally conceived by F. de Jager, "Delta modulation - a method of {PCM} transmission using the one unit code", Philips Research Report, vol. 7, pp. 442-466, 1952, is a well-established technique. However,

theoretical understanding of the concept is limited, as indicated by S. Norsworthy, R. Schreier, and G. Temes, "Delta-Sigma Data Converters", IEEE Press, 1997. The most important progress in the description of sigma delta modulators has been made by L. Risbo, "Sigma-Delta Modulators - Stability Analysis and Optimization," PhD Thesis, Electronics Institute. Lyngby: Technical University of Denmark, 1994, pp. 179, and S. Hein and A. Zakhor, "Sigma Delta Modulators: nonlinear decoding algorithms and stability analysis", New York, Kluwer Academic Publishers, 1993, while a useful linearization technique is described in S. H. Ardalan and J. J. Paulos, "An Analysis of Nonlinear Behavior in Delta-Sigma Modulators", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 34, pp. 593-603, 1987, and further elaborated on by A. J. Magrath, "Algorithms and Architectures for High Resolution Sigma-Delta Converters", PhD Thesis, Electronic Engineering, London, King's College, University of London, 1996. Yet in all these developments, there is no unified description of Sigma delta modulators (SDMs). Instead, several models are provided, each of which describes some aspects of an SDM to a certain accuracy.

Fundamental work on limit cycles in SDMs has usually been constrained to low order SDMs, such work including that of S. I. Mann and D. P. Taylor, "Limit cycle behavior in the double-loop bandpass Sigma Delta A/D converter", IEEE Transactions on Circuits and Systems-II, vol. 46, pp. 1086-1089, 1999, N. Bridgett and C. P. Lewis, "Effect of initial conditions on limit cycle performance of second order sampled data sigma delta modulator", Electronics Letters, vol. 26, pp. 817 - 819, 1990, and V. Friedman, "The Structure of limit cycles in sigma delta modulation", IEEE Trans. Communication, vol. 36, pp. 972-979, 1988, and hence is of little practical value to engineers who use high order noise shaping techniques. Recent work has significantly advanced the theory of limit cycles in sigma delta modulators, such work including J. D. Reiss and M. Sandler, "The harmonic content of a limit cycle in a DSD bitstream", Proceedings of the Audio Engineering Society 116th Convention, Berlin, Germany, 2004, J. D. Reiss and M. B. Sandler, "They Exist: Limit Cycles in High Order Sigma Delta Modulators," Proceedings of the 114th Convention of the Audio Engineering Society, Amsterdam, The Netherlands, 2003, and D. Reefman, J. D. Reiss, E. Janssen, and M. B. Sandler, "Stability Analysis of Limit Cycles in High Order Sigma Delta Modulators", Proceedings of the Audio Engineering Society 115th Convention, New

York, New York, 2003. Most notably, in D. Reefman, J. D. Reiss, E. Janssen, and M. Sandler, "Description of limit cycles in Sigma Delta Modulators", accepted for IEEE Transactions on Circuits and Systems 1, pp. 30, 2004, results were derived concerning the character of limit cycles for a general feedforward (also called interpolative), and on their stability in particular. In D. Reefman, J. D. Reiss, E. Janssen, and M. Sandler, "Description of Limit Cycles in Feedback Sigma Delta Modulators", Proceedings of the Audio Engineering Society 117th Convention, San Francisco, USA, 2004, similar results were obtained for feedback sigma delta modulators.

Limit cycle prevention is typically achieved by adding a signal, with a uniform or triangular probability distribution, just prior to quantisation, as described in S. P. Lipshitz and J. Vanderkooy, "Towards a Better Understanding of 1-Bit Sigma-Delta Modulators", Proceedings of the Audio Engineering Society 110th Convention, Amsterdam, Holland, 2001. When an appropriate dithering sequence is added, an output bit may be flipped (output bit changed from +1 to -1, or from -1 to +1), and the periodic output pattern might be destroyed. However, the dither decreases the signal-to-noise ratio, the stability, and the dynamic range of the sigma delta modulator. Furthermore, it is added when it is not needed, and in many situations may not be sufficient to destroy a limit cycle.

Reference may also be made to the following prior art references that disclose arrangements for avoiding the occurrence of limit cycles, or for providing a stand-alone limit cycle removal mechanism.

CA1078463 discloses a digital filter circuit, but is restricted to second order recursive digital filters that are fundamentally different to sigma delta modulators (of arbitrary order). EP1394942 is concerned with a limit cycle oscillation suppression method that is restricted to digital filters with a specific type of input. It does not apply to sigma delta modulation.

US6825784 relates to a dithering method for sigma-delta analogue-to-digital converters that reduces idle tones (which are distinctly different to limit cycles) and does not have a limit cycle detection window. WO2004004131 discloses a method for

sigma-delta conversion with reduced idle tones using the technique of dithering the quantiser input to remove limit cycles. The method uses an alternate dither generation mechanism. It does not detect limit cycles, and uses a sub-optimal method of limit cycle removal. US6175321 discloses a method for the reduction of periodic noise in a sigma delta modulator by applying dither in the feedback loop, which is preferable to dithering the quantiser. This method does not detect limit cycles.

US2004036636 describes tone-free dithering methods for sigma-delta DAC and applies dithering in (or prior to) the feedback loop to remove limit cycles. The method does not detect the limit cycles. JP55071315 relates to a limit cycle reduction system of a digital filter that will only remove limit cycles that occur when there is no input signal. It also affects the output of the SDM when there is no input but the system is not in a limit cycle. US4321685 is concerned with a circuit for reducing the limit cycle in a digital filter that suffers from the same disadvantages as the circuit of JP55071315.

JP2003273740 relates to a D/A conversion device that suffers from the same disadvantages as the circuits of JP55071315 and US4321685. JP4317224 discloses a sigma-delta modulator for a D/A converter that uses a random value in a bit of one of the quantisers in order to prevent limit cycles from occurring. This does not guarantee that they are removed, and it may not prevent short term limit cycles. Furthermore, it cannot detect the limit cycles.

It is an object of the present invention to provide more effective methods for detecting and removing unwanted limit cycles at the output of a sigma delta modulator.

According to one aspect of the present invention there is provided a circuit for detecting limit cycles in a sigma delta modulator having an output signal that varies over a series of iterations with respect to time, the circuit comprising:

first memory means for storing a first value indicative of the level of the modulator output signal after a predetermined iteration;

second memory means for storing a second value indicative of the level of the modulator output signal after a further iteration subsequent to the predetermined iteration;

comparison means for comparing said first value stored in the first memory means with said second value stored in the second memory means; and

detection means for providing, in response to such comparison, an output indicative of a tendency for limit cycles to be produced in the modulator output signal.

Such a circuit is particularly advantageous for detecting limit cycles in a sigma delta modulator as it can be implemented in a straightforward manner and offers a very accurate limit cycle detection mechanism. As a result it only becomes necessary to activate a limit cycle removal mechanism when limit cycle behaviour has been observed, and major changes to design are not normally required to implement the detection mechanism. Furthermore the detection mechanism can be adapted to detect short-term limit cycles. Compared with conventional methods, sigma delta modulation has less SNR penalty and the mechanism is simple to implement. Moreover, sigma delta modulation has a higher allowed input dynamic range than conventional modulator dithering schemes. Analogue and digital implementations of the limit cycle detection and removal schemes are possible for both feedforward and feedback designs.

Such a circuit may take several forms. In one embodiment of the invention the first and second memory means are arranged to store first and second values of a state space variable of the modulator.

In an alternative embodiment of the invention the first and second memory means are arranged to store the last Q output bits of the output bitstream of the modulator after the associated iteration. Preferably the first and second memory means comprise first and second shift registers for storing the last Q output bits of the output bitstream of the modulator after the associated iteration.

Furthermore, in order to remove the tendency for limit cycles to be produced in the modulator output signal, disturbing means are preferably provided for applying a

disturbance to an input of the modulator in response to an output from the detection means indicative of a tendency for limit cycles to be produced. This novel mechanism requires adding a small disturbance to the input in order to destroy the periodicity of the modulator's output sequence and to thereby remove the limit cycles. The previously suggested dither mechanism referred to in some of the prior art documents mentioned above is a poor method of limit cycle removal and disturbing the input is far more effective.

These limit cycle detection and removal mechanisms may be modified for use with feedback sigma delta modulators. They may be analysed to give quantitative results concerning the probability of false limit cycle detection, the time required for limit cycle removal, and the choice of parameters.

Either detection mechanism referred to above may be used with any method for removing the limit cycles, and the particular removal mechanism referred to above may be operated with (or even without) any detection method.

According to another aspect of the present invention there is provided a circuit for removing limit cycles in a sigma delta modulator having an output signal that varies over a series of iterations with respect to time, the circuit comprising:

detection means for providing an output indicative of a tendency for a limit cycle to be produced in the modulator output signal; and

disturbing means for applying a disturbance to an input of the modulator in response to an output from the detection means indicative of a tendency for limit cycles to be produced, in order to remove the tendency for limit cycles to be produced in the modulator output signal.

According to a further aspect of the present invention there is provided a method of detecting limit cycles in a modulator having an output signal that varies over a series of time intervals, the method comprising:

storing a first value indicative of the level of the modulator output signal after a predetermined time interval;

storing a second value indicative of the level of the modulator output signal after a further time interval subsequent to the predetermined time interval;

comparing said first value stored in the first memory means with said second value stored in the second memory means; and

providing, in response to such comparison, an output indicative of a tendency for limit cycles to be produced in the modulator output signal.

In order that the invention may be more fully understood, reference will now be made, by way of example, to the accompanying drawings, in which:

Figure 1 is a block diagram of a generic feedforward SDM;

Figure 2 is a block diagram of a fifth order SDM ;

Figure 3 is a plot depicting the growth of a disturbance to the state space variables as a function of the clock cycle, for a fifth order SDM;

Figure 4 is a block diagram of a fifth order SDM with a state-space-based limit cycle detector;

Figure 5 is a flow chart depicting the operation of a state-space-based limit cycle detection and removal for an arbitrary SDM;

Figure 6 is a plot of the input to the quantiser as a function of the number of iterations;

Figure 7 is a plot of f as a function of the number of iterations;

Figure 8 is a flow chart depicting the operation of a bitstream-based limit cycle detection and removal mechanism, using shift registers, for an arbitrary SDM;

Figure 9 is a block diagram of a fifth order SDM with a bitstream-based limit cycle detector;

Figure 10 is a plot of the probability of falsely detecting a limit cycle as a function of shift register length;

Figure 11 shows two block diagrams of a third order SDM comparing the standard placement of (a) dither with (b) the proposed limit cycle detection and removal;

Figure 12 is a graph of added disturbance against number of iterations of a fifth order SDM; and

Figure 13 is a block diagram of a third order SDM.

A convenient way to describe the time domain behaviour of an SDM is the state space description. This represents the state of the SDM at any time as a matrix operation applied to the state at the previous clock cycle. The power of the state space description is that it allows a very compact description of the state of the SDM from time t=0 to time t=n to be created.

For an N^{th} order feedforward (or iterative) SDM,

$$\mathbf{s}(n+1) = \mathbf{A}\,\mathbf{s}(n) + (u(n) - y(n))\mathbf{d}. \tag{1}$$

where u is the input at iterate n, and y is the output, plus or minus one, determined by

$$y(n) = \mathrm{sgn}(\sum_{i=1}^{N} c_i s_i(n)) \tag{2}$$

This description gives the state **s** of the SDM, at iterate n, in terms of a transition matrix **A** applied to the previous state vector, and a vector **d** applied to the scalar quantisation error, u(n) - y(n). Figure 2 is an example of a typical fifth order SDM. In operation of such an SDM an input signal u is applied by way of an input 21 to five integrators 25 at iterate n, and an output signal y is obtained at an output 22 representing plus or minus one. Five amplifiers 23 multiply the state space variables outputted by the integrators 25 by coefficients c_1, c_2,...c_N so as to provide outputs that are summed and quantised in a quantiser 24. The coefficients c determine the noise shaping characteristics, and each integrator 25 provides a unitary delay T.

For the fifth order sigma delta modulator shown in Figure 2, $\mathbf{d} = (1,0,0,0,0)^T$ and the transition matrix is

$$\mathbf{A} = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 \end{pmatrix} \tag{3}$$

This compact representation gives the means to directly view the consequences of a limit cycle. If the limit cycle has period P we have, by definition,

$$y(n+P) = y(n) \tag{4}$$

An important assumption in earlier work is that a periodic bit output pattern implies a periodic orbit in state space variables. In D. Reefman, J. D. Reiss, E. Janssen, and M. Sandler, "Description of limit cycles in Sigma Delta Modulators" referred to above, it was proven that, in general, a limit cycle in the output bitstream exists if and only if there is a limit cycle in the state space variables. This means that equation (4) is equivalent to

$$\mathbf{s}(n+P) = \mathbf{s}(n) \tag{5}$$

Although, in its pure definition, a limit cycle is a periodic pattern of infinite duration, in practical situations finite duration periodic sequences can be equally annoying. Thus a limit cycle detection and removal algorithm should be successful even if equation (5) is only true for a finite number of values. It follows that it should be possible to detect and remove limit cycles when equation (4) is approximately true for a finite time.

1. State space-based limit cycle detection

In this section a preferred method for detecting limit cycles in feedforward SDMs in accordance with the invention will now be described.

Equation (5) provides a simple method of determining if a limit cycle exists. At a given iteration which we set to 0, $\mathbf{s}(0)$ may be stored in a buffer. For each successive iteration, 1,2,...i,... up to some value $P_{\max}$, $\mathbf{s}(i)$ is computed. If constant input is applied and, for some i, $\mathbf{s}(i) = \mathbf{s}(0)$, then the theorem described in the previous section guarantees that a limit cycle of period P exists.

This method, while exact, has three drawbacks. Firstly, it requires that a vector of size N be stored. At each time iteration, up to N comparisons must be made. This is unnecessarily complicated. Secondly, and more importantly, this does not allow for a

simple method of making approximate comparisons. When the state space variables are very close to a limit cycle condition, periodic output may be sustained long enough to be problematic. An appropriate measure of the required proximity of the state space variables needed for temporary limit cycle behaviour is not obvious and may not be simple to compute.

To alleviate this difficulty, it is proposed to compute a single scalar quantity at each iteration. It should be noted that the effect of a small change in the state space variables tends, over time, to yield a larger change in the later state space variables. The cumulative nature of the integrators implies that s_N varies far more rapidly than any other state space variable.

If a small perturbation δ is applied to the state space variables, then that perturbation grows at a rate given by

$$\boldsymbol{\delta}(n) = \mathbf{A}^n \boldsymbol{\delta}(0) \tag{6}$$

Repeated application of the transition matrix A yields the binomial coefficients

$$\mathbf{A}_{ij}^n = \begin{cases} 0 & \text{if} \quad i < j \\ \begin{pmatrix} n \\ n-(i-j) \end{pmatrix} & \text{otherwise} \end{cases} \tag{7}$$

Thus, the terms of $\boldsymbol{\delta}(n) = \mathbf{A}^n \boldsymbol{\delta}(0)$ are given by

$$\delta_i(n) = \begin{pmatrix} n \\ n \end{pmatrix} \delta_i(0) + \begin{pmatrix} n \\ n-1 \end{pmatrix} \delta_{i-1}(n) + \ldots + \begin{pmatrix} n \\ n-i+1 \end{pmatrix} \delta_1(n) \tag{8}$$

Thus typically, $\delta_1(n) < \delta_2(n) \ldots < \delta_N(n)$. This is illustrated in Figure 3, which is a graph in which curves 31, 32, 33, and 34 are shown depicting the growth of each of the variables Δs_2, Δs_3, Δs_4, Δs_5, where $\Delta s_i(nP) = s_i(nP) - s_i(0)$ for a small perturbation (10^{-8}) away from a period P=24 limit cycle. Thus, when the system is near a limit cycle,

$s_1, s_2, ...s_{N-1}$ will vary almost periodically, whereas s_N will diverge away from periodic behaviour. This implies that, when the system is near a limit cycle, there may be considerable variability in s_N.

It should be noted that this is independent of the choice of the coefficients $c_1, c_2, ...c_N$. The coefficients typically differ greatly in value. For a low pass sigma delta modulator, $c_1 > c_2 > ... > c_N$. This also implies that s_N may vary greatly with the output bitstream unaffected.

s_N is thus ignored in computing whether we are near a limit cycle. By not comparing s_N, it is possible to find short term limit cycles where the state space variables are not exactly repeating but the output bitstream may remain periodic long enough to be problematic.

Figure 4 is a block diagram of a fifth order SDM with a bitstream-based limit cycle detector. This SDM is similar to the SDM of Figure 2, except that a limit cycle detector has been added. The limit cycle detector stores a first variable value in a buffer 41 indicative of the level of the output signal after a predetermined time interval, compares the first value in the buffer 41 with a second value indicative of the level of the output signal after a further time interval in a comparator 43, and then copies the current value into the buffer 41 after a time determined by the timing circuit 42.

In order to have a scalar quantity for comparison, as well as to take into account the differing sizes of the variables, use is made of a stored variable

$$f(n) = \sum_{i=1}^{N-1} c_i s_i(n) \qquad (9)$$

Thus, if a limit cycle of period P exists,

$$f(n+P) \gg f(n) \qquad (10)$$

For a given iteration n_0, the value $f(n_0)$ is stored and a check is made to determine whether $f(n_0 + i) \gg f(n_0)$ holds for each successive iteration n_0+1, n_0+2, ... n_0+i. If it does, then the limit cycle removal algorithm is applied.

After a number of iterations R, the buffer is reset from $f(n_0)$ to $f(n_R)$. This allows limit cycles to be identified that appear at later iterations. However, it also implies that some limit cycles of period P>R may not be identified. The value of R is quite high, since long period limit cycles are problematic. However, a maximal value should be only a small multiple of the oversampling ratio. Otherwise, a limit cycle with period P<R may sometimes persist for long enough to be problematic. As an example, for an audio signal sampled at 64 x 44.1 kHz (64 times OSR), $R = 320 = 5$xOSR performs well under a wide variety of circumstance.

It is possible that equation (10) may hold when limit cycle behaviour is not happening, but such an occurrence would be very rare. It occurs with a probability of the order of the digital precision of the hardware, e.g., if there are 2^{16} bits precision and f ranges over values from –A to A, then it would occur with a probability close to $1/(2^{17}A)$.

This limit cycle detection procedure may be continued indefinitely. The method is robust to the choice of parameters and may be used to detect any limit cycle. A flow chart depicting this method is given in Figure 5.

As an example, consider the fifth order sigma delta modulator given by D. Reefman, J. D. Reiss, E. Janssen, and M. Sandler, "Description of limit cycles in Sigma Delta Modulators" referred to above

c_1=0.5761069262,c_2=0.1624753515,c_3=0.0276093301,
c_4=0.0028053934,c_5=0.0001360361

With an input of 0.7, and initial conditions s=0, it exhibits limit cycle behaviour. Figure 6 is a plot of the input to the quantiser as a function of the iteration and shows a

time series of the input to the quantiser. The circled points represent those points where limit cycle behaviour has been identified. Clearly, limit cycle behaviour has been correctly identified. The time lag between the start of the limit cycle and the identification of limit cycle behaviour is due to the fact that the limit cycle has been running for approximately 200 iterations before the buffer is reset to a value for f which represents the limit cycle.

This may be contrasted with Figure 7 which is a plot of the function f, as defined in equation (6), as a function of the iteration. It can be seen that, when approximate limit cycle behaviour occurs, although s_N may drift, $f(n)$ remains periodic. The circled points again represent where limit cycle behaviour has been identified.

2. Limit cycle detection at the SDM output

In this section an alternative preferred method for detecting limit cycles in feedforward SDMs in accordance with the invention using only shift registers will now be described.

Shift registers and bit comparisons are often much easier to implement than any circuitry (analogue or digital) for comparison of real numbers. Furthermore, one can conceive of situations where it is easier to access the output bitstream than the state space variables. Thus, it is desirable to consider methods of detecting limit cycles using bit comparisons alone.

A naïve approach would be to implement many shift registers, each one representing periodic output for a different limit cycle. The current output could then be compared with each shift register to see if it appears that limit cycle behavior is occurring. However, this would require of the order of 2^P shift registers, and 2^P comparisons. Since a limit cycle represents a repeating pattern in the bitstream, it suffices to identify bitstream repetition. To do this, the outputs of two shift registers are compared, one representative of the current bitstream output and the other representative of the bitstream output at a previous iteration. For this method, there are

two parameters of importance, namely the shift register length Q and the shift register duration or persistence R (the number of iterations until the stored shift register is reset).

Figure 8 is a flowchart depicting the operation of such a limit cycle detection and removal mechanism, using shift registers, for an arbitrary SDM. The algorithm is as follows:

- Keep a shift register SR of the last Q output bits.
- After every R^{th} iterate, copy the shift register SR into the shift register SR_{stored}.
- If, at any iterate, the samples stored in the two shift registers exactly match, $SR_{current}=SR_{stored}$, then a limit cycle has been detected.

A block diagram of a fifth order SDM with a bitstream-based limit cycle detector, including noise shaping, is shown in Figure 9. The bitstream-based limit cycle detector stores output bits in a shift register at 91, compares the values in the shift register 91 and a current shift register 93, and then copies the value in the current shift register into the shift register 91 after a time determined by the timing circuit 92.

It should be noted that comparison of bits in the shift register, as well as copying of bits between shift registers, can be done in parallel. Thus there is no need for any operation to be performed faster than the sampling frequency of the SDM.

Such a method guarantees that a limit cycle (even a short one) is not detected until after Q iterates. On the other hand, limit cycles of a period longer than Q are still identifiable, since this also requires matching of the recent bitstream with the stored values in the buffer. Thus, Q is typically made smaller than the value R.

The method is robust both to the size of the shift register, and the choice of when the shift register is reset. More significant is the choice of shift register persistence R. If it is supposed that we are in a limit cycle of length P, where $R<P$. At iteration 0 the buffer is set. The sequence will thus be repeated next at time P, but, before that can be identified, the buffer is reset at iteration R. Thus limit cycles of period greater than the buffer duration will not be detected. On the other hand, if we are in a limit cycle of

length $P \leq R$, then, every R iterates, the limit cycle will be detected $\lfloor R/P \rfloor$ times, where $\lfloor \ \rfloor$ denotes the largest integer less than or equal to. Conversely this implies that a limit cycle is detected at most once per period, and at least once every other period.

False detections are very rare. If the output is truly random, then false detections occur with a probability 2^{-Q}. However, the output is far from random. This is partly due to the fact that the input is not random (band limited, with amplitude safely within stability limits), but also because the sigma delta modulation prevents certain sequences from occurring, regardless of input. Figure 10 is a plot of the probability of falsely detecting a limit cycle as a function of buffer length Q incorporating a line 100 corresponding to a random output and lines 101, 102 and 103 corresponding to outputs from 5^{th} order SDMs at 80kHz, 100kHz and 120kHz respectively. In each case, the buffer duration R was set equal to the buffer length Q. Each data point was generated using 100 one million point long sequences (after initial startup transients were removed), where each sequence has as input a sinusoid with a randomly generated frequency between 80 and 130kHz, and random initial conditions. It can be clearly seen that, though the probability of a false detection is far greater than would be the case for a truly random sequence, it is still low enough to be insignificant.

3. Limit cycle removal

In D. Reefman, J. D. Reiss, E. Janssen, and M. Sandler, "Description of limit cycles in Sigma Delta Modulators" referred to above, it was shown that the application of dither at a location 110 just before the quantiser, as shown in the block diagram of a third order SDM of Figure 11a, is a sub-optimal form of limit cycle removal. This is because it has no effect on the state space variables unless it results in a change to the output bitstream. On the other hand, any disturbance applied at the input 111 in response to detection of limit cycles at 112, as shown in the block diagram of a third order SDM of Figure 11b, will affect all state space variables. So a limit cycle may be removed by simply perturbing the internal integrator states of a sigma delta modulator. Furthermore, the perturbation will be shaped according to the noise-shaping characteristics of the SDM. Thus, it is recommended that a small perturbation be added to the input 111 of the sigma delta modulator whenever a limit cycle has been detected.

The choice of the size of the disturbance that is added is a trade-off between the reduction in SNR and instability when a large disturbance is added, and the increased amount of time it may take to destroy a limit cycle when a small disturbance is added. However, this is a minor issue since, within a large range, the size of the disturbance has only a minimal effect on stability, SNR, or the time it takes to destroy the limit cycle. Even a disturbance of the order of 10^{-8} (akin to a change of less than -140dB) is sufficient to eliminate the limit cycle long before it becomes problematic.

Since this modification is both minimal and guaranteed to work, it is preferable to the commonly used alternative of adding dither or noise to the input to the quantiser. The perturbation only needs to be added when a limit cycle has been detected. Furthermore, since the limit cycle is unstable, only a very small disturbance needs to be added.

Compared to conventional dithering techniques that add random noise to the input of the quantizer, this novel limit cycle detection and removal technique and apparatus has a higher allowed input dynamic range and higher signal-to-noise-plus-distortion-ratio (SNDR). It may also be implemented successfully without the use of a limit cycle detector.

Figure 12 demonstrates how the size of the disturbance affects the time it takes to destroy a limit cycle. The number of iterates before a limit cycle is removed as a function of the size of the perturbation applied. This is a worst case scenario where the initial conditions have been set to produce the most stable period 12 limit cycle possible for a fifth order SDM having a corner frequency of 100kHz. Not only have the initial conditions of the modulator been chosen to guarantee that the dynamics fall exactly on a limit cycle, but they have also been chosen so that the initial conditions are as far as possible from those that would produce a bit flip and thus destroy the limit cycle. Nevertheless, even a disturbance of the order of 10^{-6} is sufficient to eliminate the limit cycle long before it becomes problematic.

4. Limit cycle detection in feedback SDMs

A popular alternative design to the feedforward, or interpolative, SDM, is the feedback SDM. This is often used when a superior anti-aliasing effect of the signal transfer function is required. Figure 13 is a block diagram of a third order feedback SDM. This represents a typical SDM design, which is often used in practical designs, such as that disclosed by D. Reefman and E. Janssen, "Signal processing for Direct Stream Digital: A tutorial for digital Sigma Delta modulation and 1-bit digital audio processing," Philips Research, Eindhoven, White Paper 18 December 2002.
We can easily see that, for the modulator presented here,

$$\begin{aligned} \mathbf{s}^{(n+1)} &= \mathbf{A}\,\mathbf{s}^{(n)} + u^{(n)}\mathbf{d} - y^{(n)}\mathbf{c} \\ y^{(n)} &= \mathrm{sgn}(s_N^{(n)}) \end{aligned} \tag{11}$$

where $y(n)$ is the output bit at clock cycle n, and $s_i(n)$ are the integrator outputs, called state variables. The last integrator output, $s_N(n)$, is also the quantiser input signal.

The propagation of the states s can be written in matrix notation as:

$$\mathbf{s}^{(n)} = \mathbf{A}^n\mathbf{s}^{(0)} + [\sum_{i=0}^{n-1} \mathbf{A}^{(n-i-1)}(u^{(i)}\mathbf{d} - y^{(i)}\mathbf{c})] \tag{12}$$

where c is a vector of feedback coefficients, A is an NxN transition matrix for an SDM of order N, and $c=(c_1,\ldots, c_N)^T$ and d describe how the input and feedback respectively are distributed.

It is interesting to compare this with the equivalent feedforward design, where the state space equations are given by equations (1) and (2). For both designs, the placement of the transition matrix A in the state space equations is identical. However, for feedforward designs, the coefficient vector has no direct effect on the state space variables s, and only acts as a weighting term on the quantisation, whereas, for the feedback design, the coefficient vector acts as a constant that is added or subtracted from the state space variables on every iteration. This implies that the dynamics of

feedback and feedforward designs are very similar, but modifications must be made in limit cycle detection and removal mechanisms.

A limit cycle occurs when the input to the quantiser repeats. Here, short period limit cycles are very rare. For state variable-based detection, it is not necessary to identify limit cycles using anything other than the quantiser input.

In the above a method of detecting limit cycles based on the state space variables has been described and a method of detecting limit cycles based only on analysis of the output bitstream has subsequently been described. Either of these methods may be combined with the limit cycle removal method described to yield a highly effective limit cycle detection and removal method that does not require continual dithering. Various implementations are described below by way of example.

The first two implementations described above are preferred embodiments. The following implementations are variations that can also be carried out within the scope of the invention:

a. A one-bit sigma delta modulator, of arbitrary order, arbitrary design (feedforward, feedback or otherwise) and without dither applied to the quantiser, using the method described in Section 2 to detect the occurrence of limit cycles, and the method described in Section 3 to remove the limit cycles.

b. A one-bit feedforward sigma delta modulator, of arbitrary order and without dither applied to the quantiser, using the method described in Section 1 to detect the occurrence of limit cycles, and the method described in Section 3 to remove the limit cycles.

c. A multibit sigma delta modulator, of arbitrary order, arbitrary design (feedforward, feedback or otherwise) and without dither applied to the quantiser, using the method described in Section 2 to detect the occurrence of limit cycles, and the method described in Section 3 to remove the limit cycles.

d. A multibit feedforward sigma delta modulator, of arbitrary order and without dither applied to the quantiser, using the method described in Section 1 to detect the occurrence of limit cycles, and the method described in Section 3 to remove the limit cycles used.

e. Any sigma delta modulator, using the method described in Section 1 to detect the occurrence of limit cycles, regardless of the limit cycle removal mechanism used.

f. Any sigma delta modulator, using the method described in Section 2 to detect the occurrence of limit cycles, regardless of the limit cycle removal mechanism.

CLAIMS:

1. A circuit for detecting limit cycles in a sigma delta modulator having an output signal that varies over a series of iterations with respect to time, comprising:

first memory means for storing a first value indicative of the level of the modulator output signal after a predetermined iteration;

second memory means for storing a second value indicative of the level of the modulator output signal after a further iteration subsequent to the predetermined iteration;

comparison means for comparing said first value stored in the first memory means with said second value stored in the second memory means; and

detection means for providing, in response to such comparison, an output indicative of a tendency for limit cycles to be produced in the modulator output signal.

2. A circuit according to claim 1, wherein the first and second memory means are arranged to store first and second values of a state space variable of the modulator.

3. A circuit according to claim 2, wherein the state space variable is a function of the form $f(n) = \sum_{i=1}^{N-1} c_i s_i(n)$ where N is the order of the modulator comprising a plurality of filter stages, c_i is the noise shaping coefficient of each stage, s_i is the output of each stage, and n is the given iteration.

4. A circuit according to claim 1, wherein the first and second memory means are arranged to store the last Q output bits of the output bitstream of the modulator after the associated iteration.

5. A circuit according to claim 4, wherein the first and second memory means comprise first and second shift registers for storing the last Q output bits of the output bitstream of the modulator after the associated iteration.

6. A circuit according to any preceding claim, wherein reset means are provided for resetting the value stored in the first memory means after a preset number R of iterations following on from the predetermined iteration.

7. A circuit according to claims 5 and 6, wherein the reset means is arranged to copy the contents of the second shift register into first shift register after a preset number R of iterations.

8. A circuit according to any preceding claim, wherein the comparison means is arranged to compare said first value stored in the first memory means with each of said second values stored in the second memory means for a plurality of further iterations following on from the predetermined iteration.

9. A circuit according to any preceding claim, wherein disturbing means are provided for applying a disturbance to an input of the modulator in response to an output from the detection means indicative of a tendency for limit cycles to be produced, in order to remove the tendency for limit cycles to be produced in the modulator output signal.

10. A circuit for removing limit cycles in a sigma delta modulator having an output signal that varies over a series of iterations with respect to time, comprising:

detection means for providing an output indicative of a tendency for a limit cycle to be produced in the modulator output signal; and

disturbing means for applying a disturbance to an input of the modulator in response to an output from the detection means indicative of a tendency for limit cycles to be produced, in order to remove the tendency for limit cycles to be produced in the modulator output signal.

11. A method of detecting limit cycles in a modulator having an output signal that varies over a series of time intervals, the method comprising:

storing a first value indicative of the level of the modulator output signal after a predetermined time interval;

storing a second value indicative of the level of the modulator output signal after a further time interval subsequent to the predetermined time interval;

comparing said first value stored in the first memory means with said second value stored in the second memory means; and

providing, in response to such comparison, an output indicative of a tendency for limit cycles to be produced in the modulator output signal.

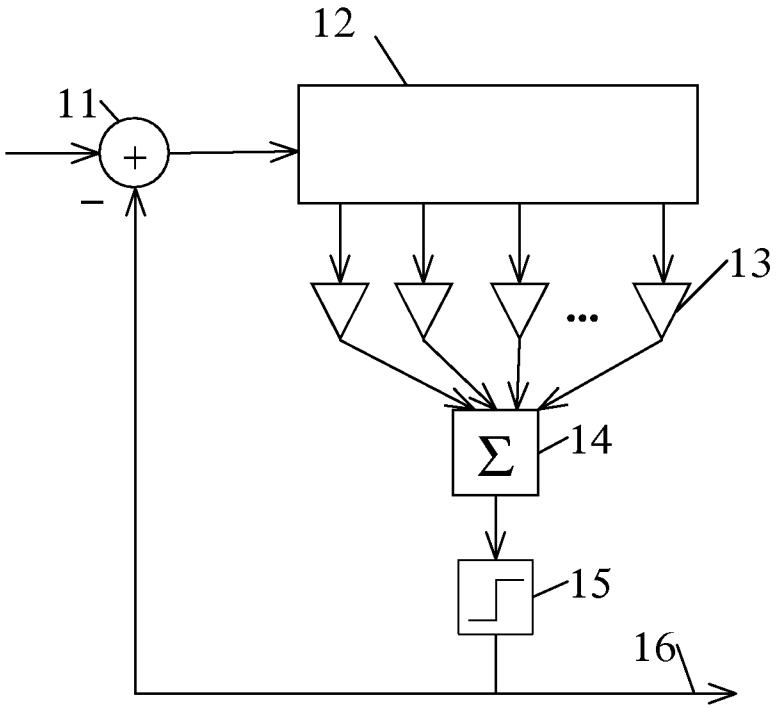

Figure 1

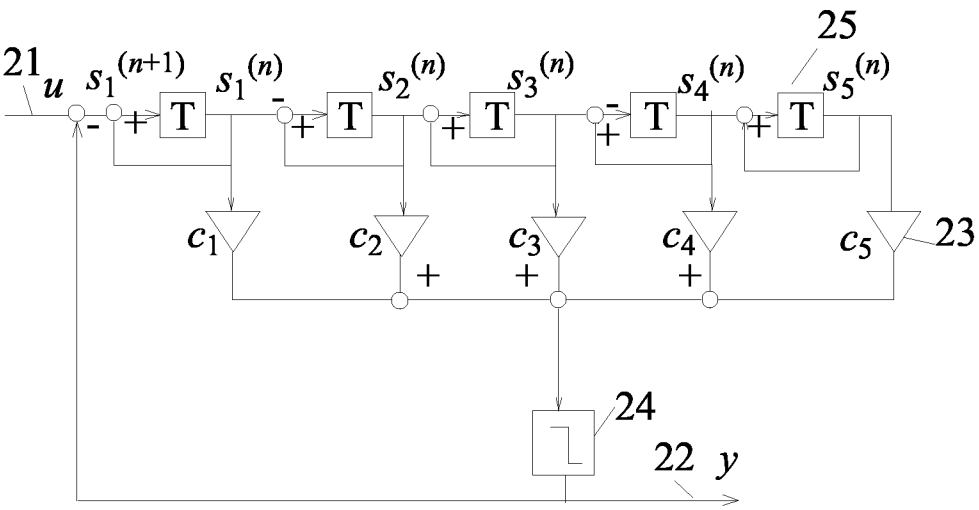

Figure 2

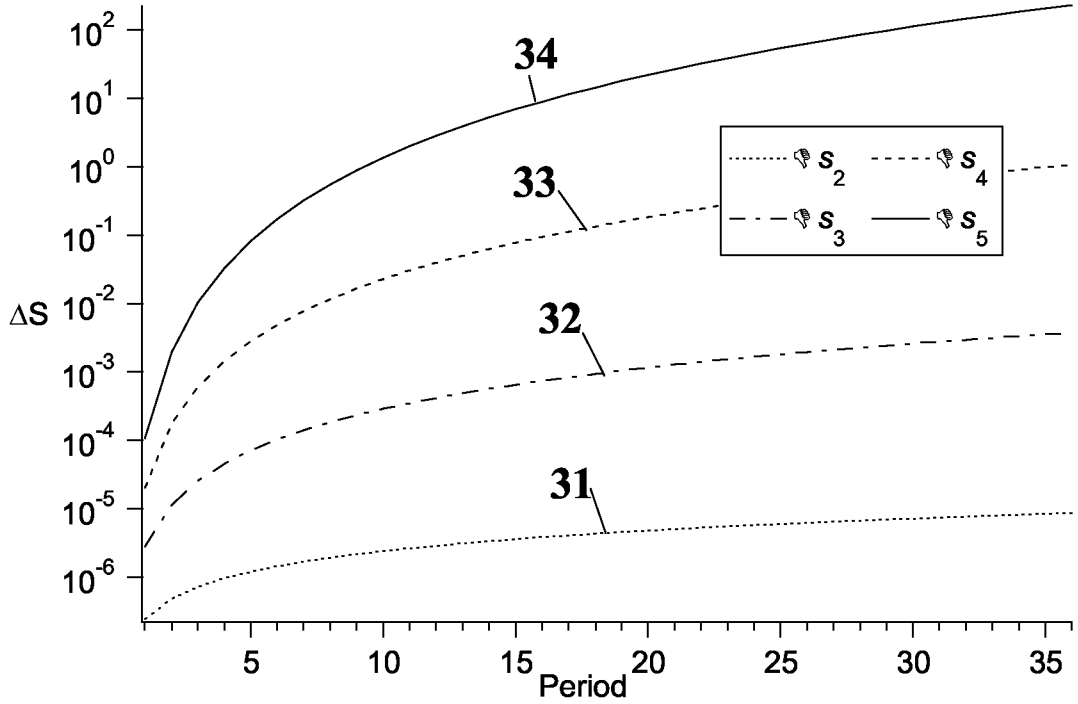

Figure 3

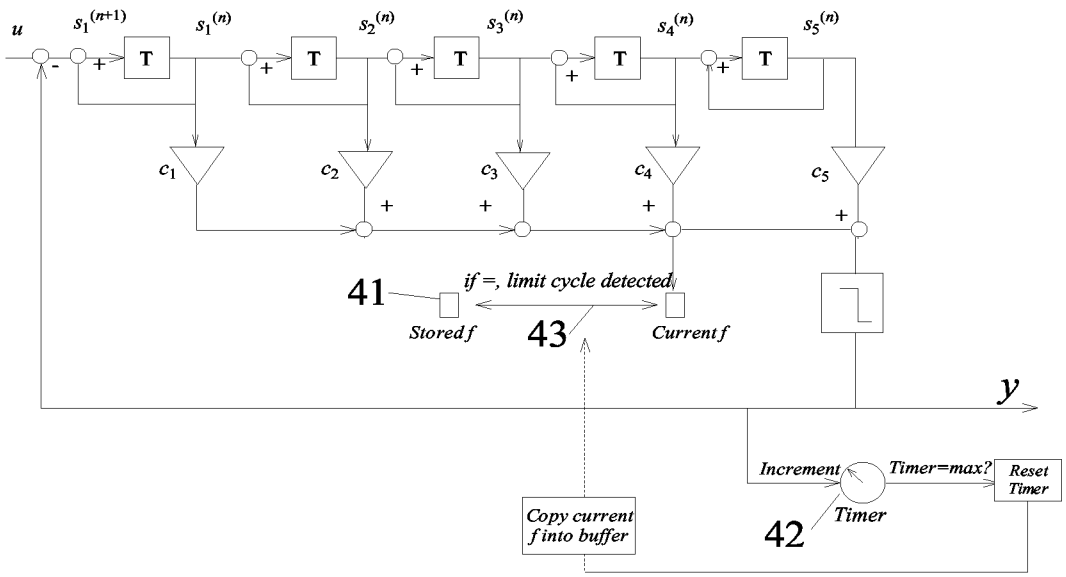

Figure 4

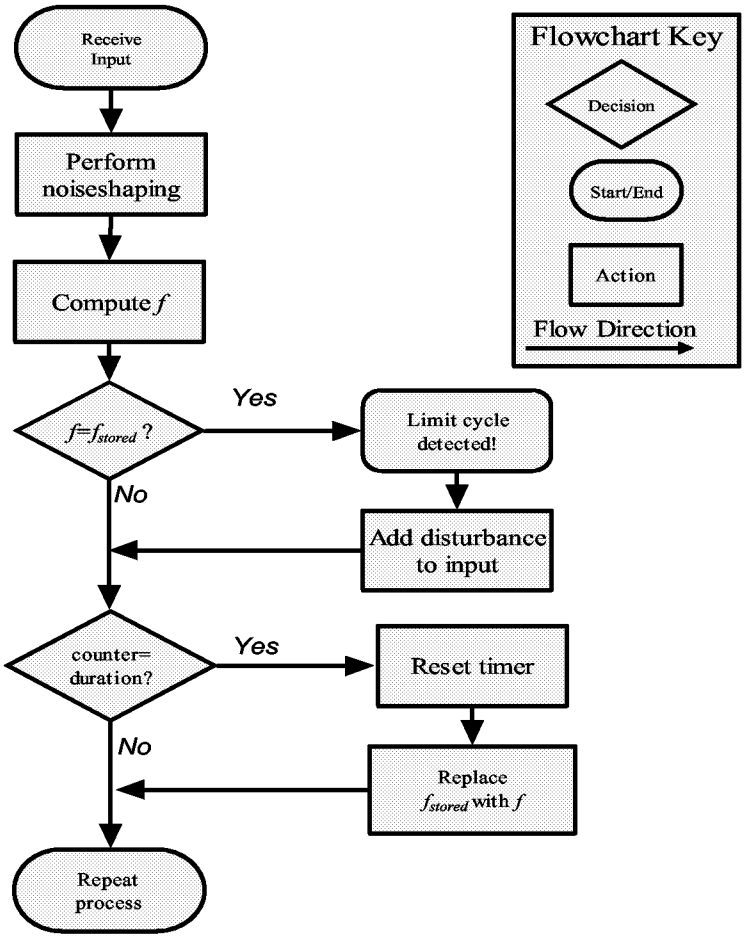
Receive Input
Perform noiseshaping
Compute f
f=f_stored ?
Yes
Limit cycle detected!
No
Add disturbance to input
counter= duration?
Yes
Reset timer
No
Replace f_stored with f
Repeat process
Flowchart Key
Decision
Start/End
Action
Flow Direction

Figure 5

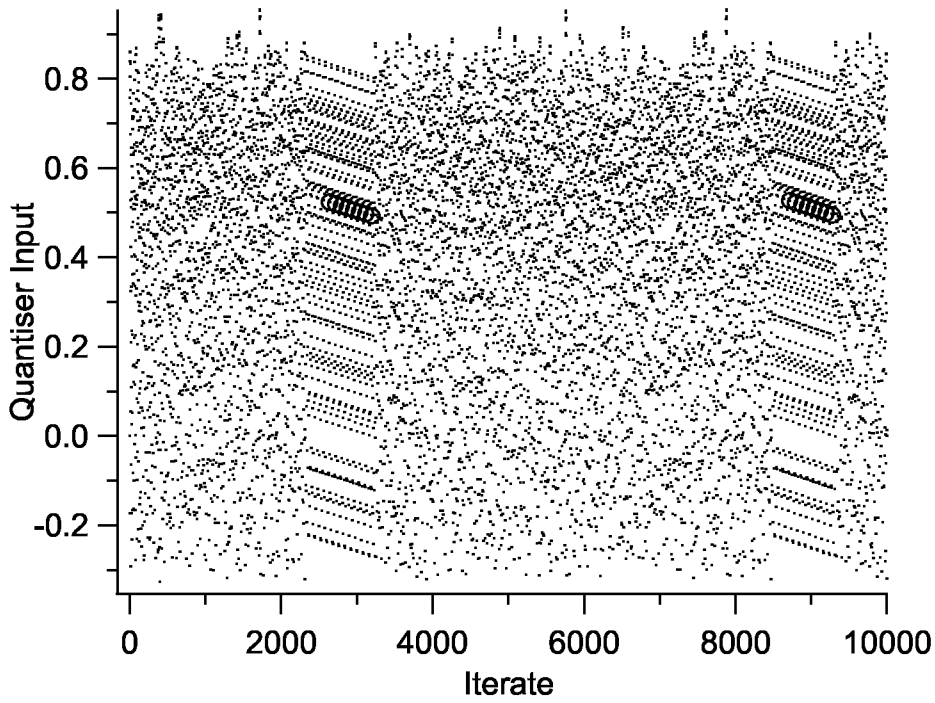

Figure 6

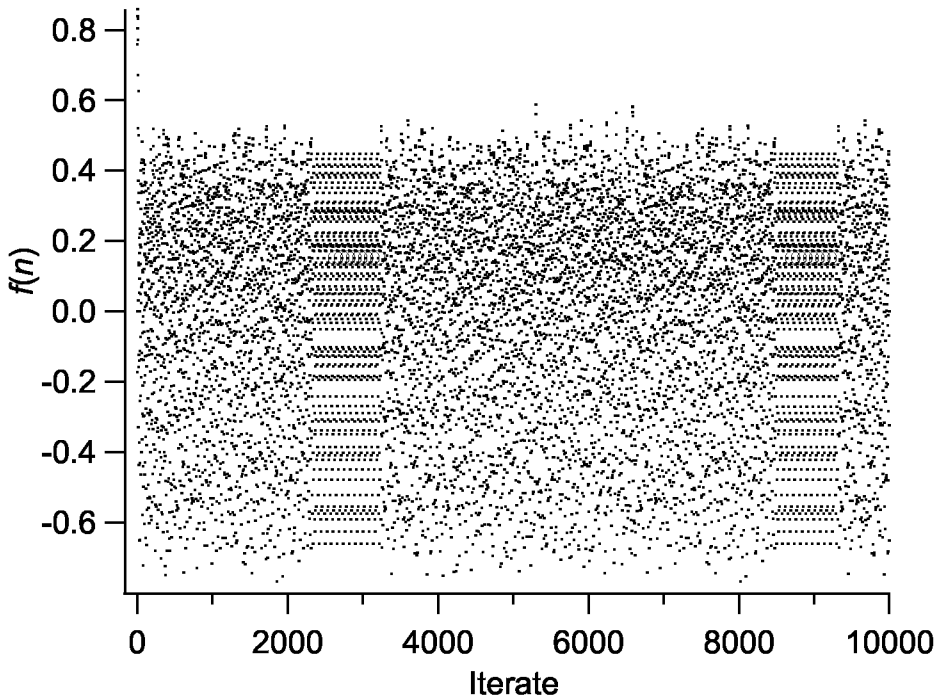

Figure 7

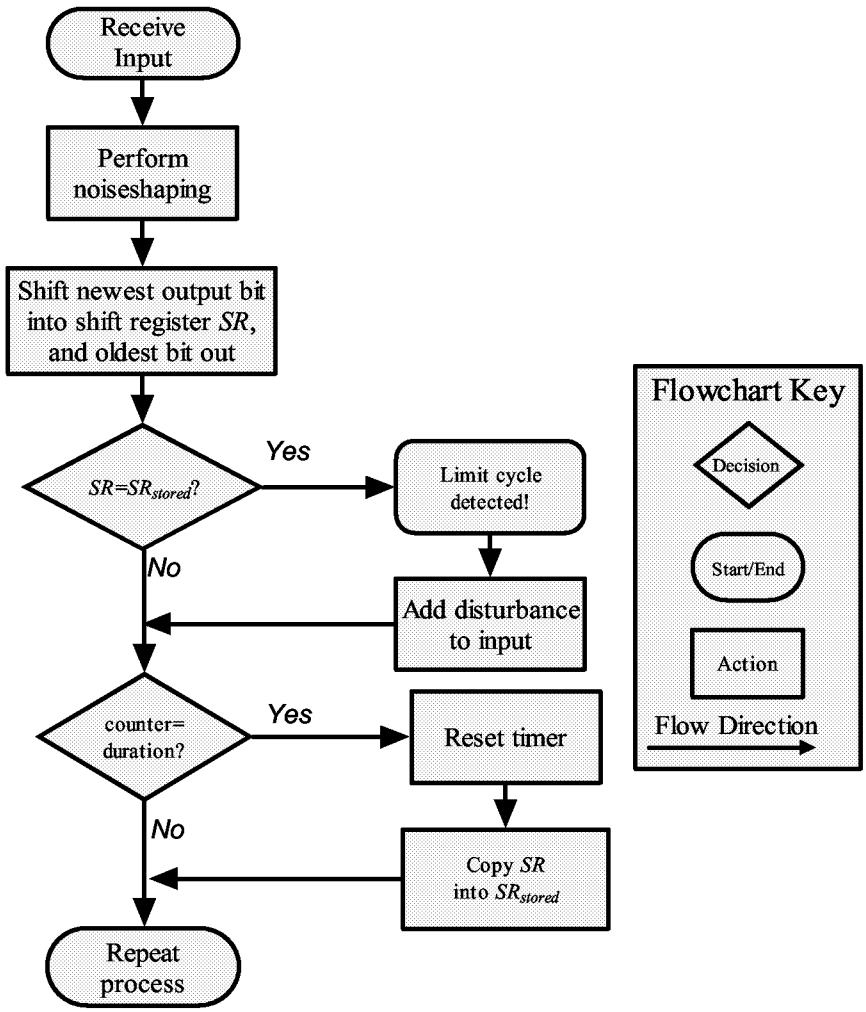
Receive Input
Perform noiseshaping
Shift newest output bit into shift register SR, and oldest bit out
SR=SR_stored?
Yes
Limit cycle detected!
No
Add disturbance to input
counter= duration?
Yes
Reset timer
No
Copy SR into SR_stored
Repeat process
Flowchart Key
Decision
Start/End
Action
Flow Direction

Figure 8

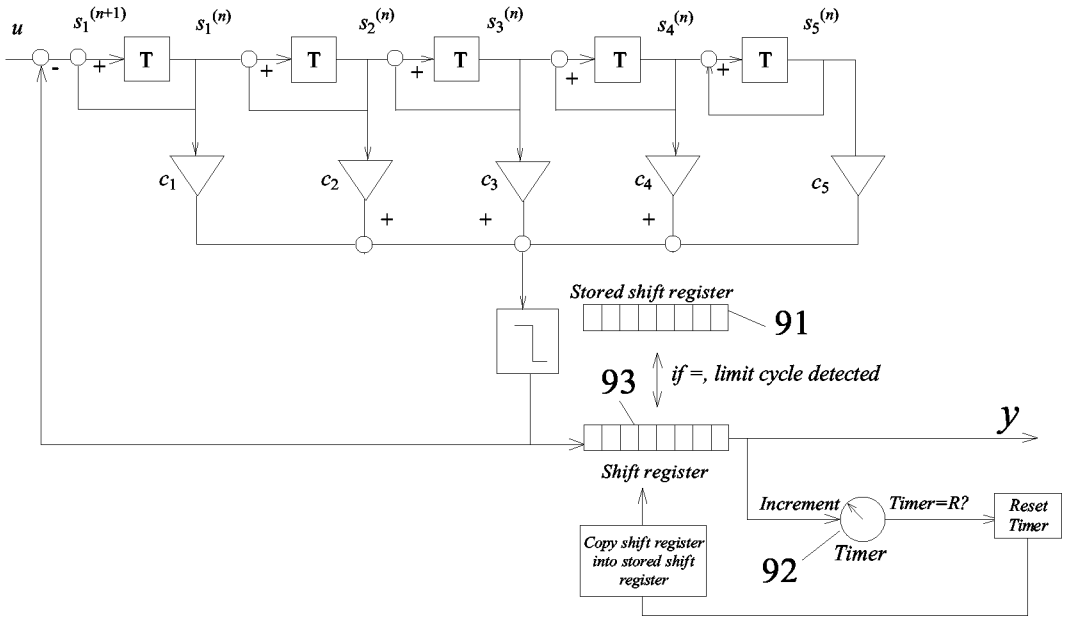

Figure 9

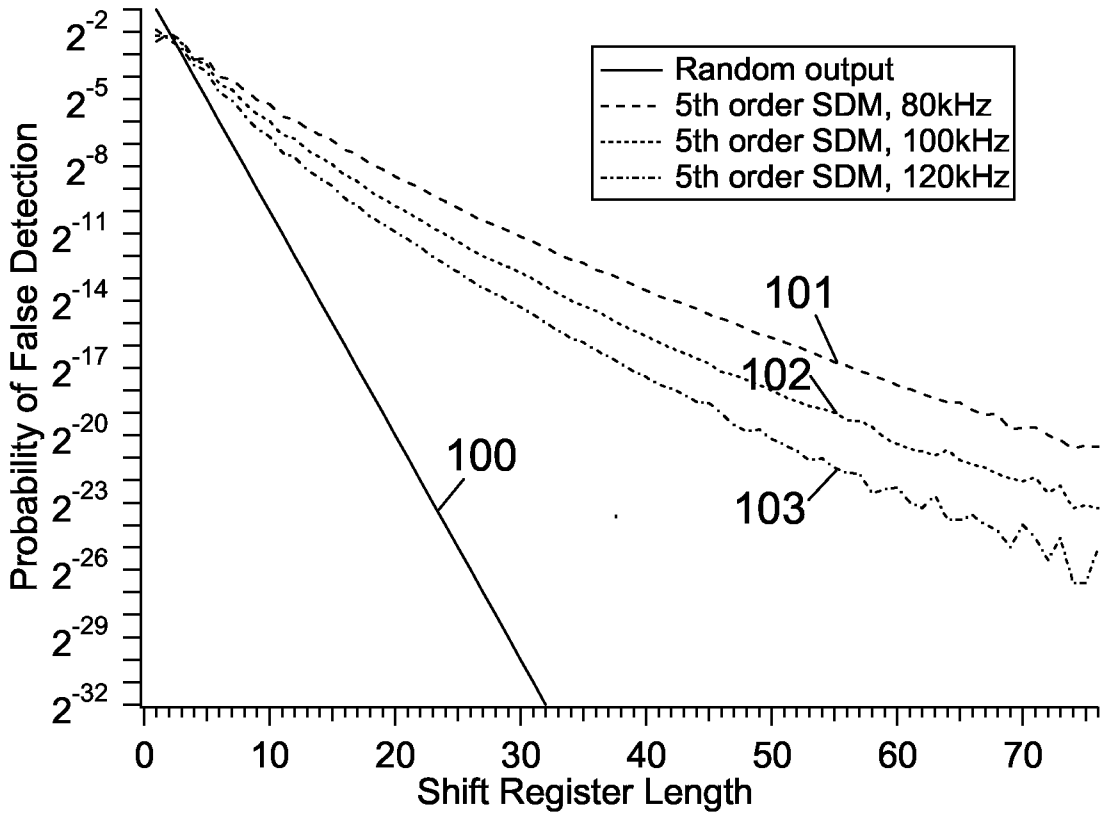

Figure 10

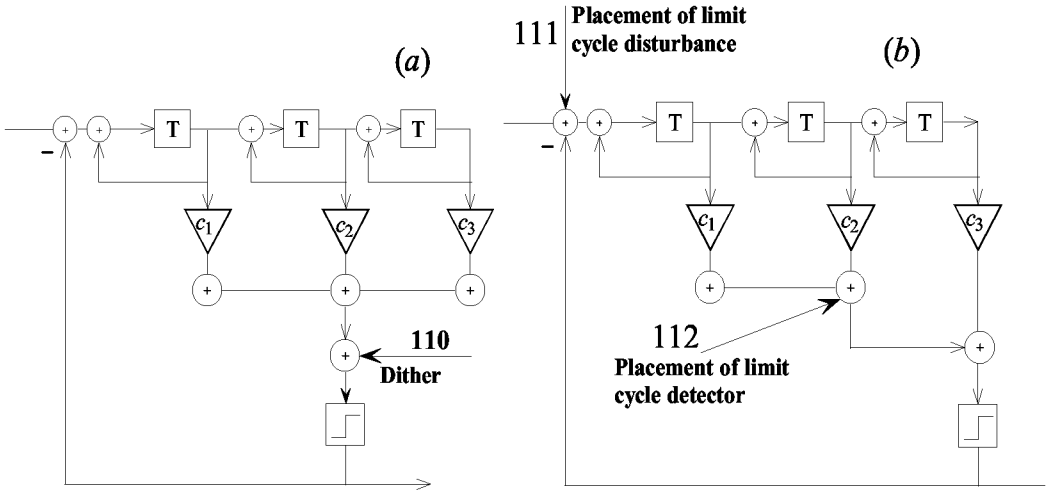

Figure 11

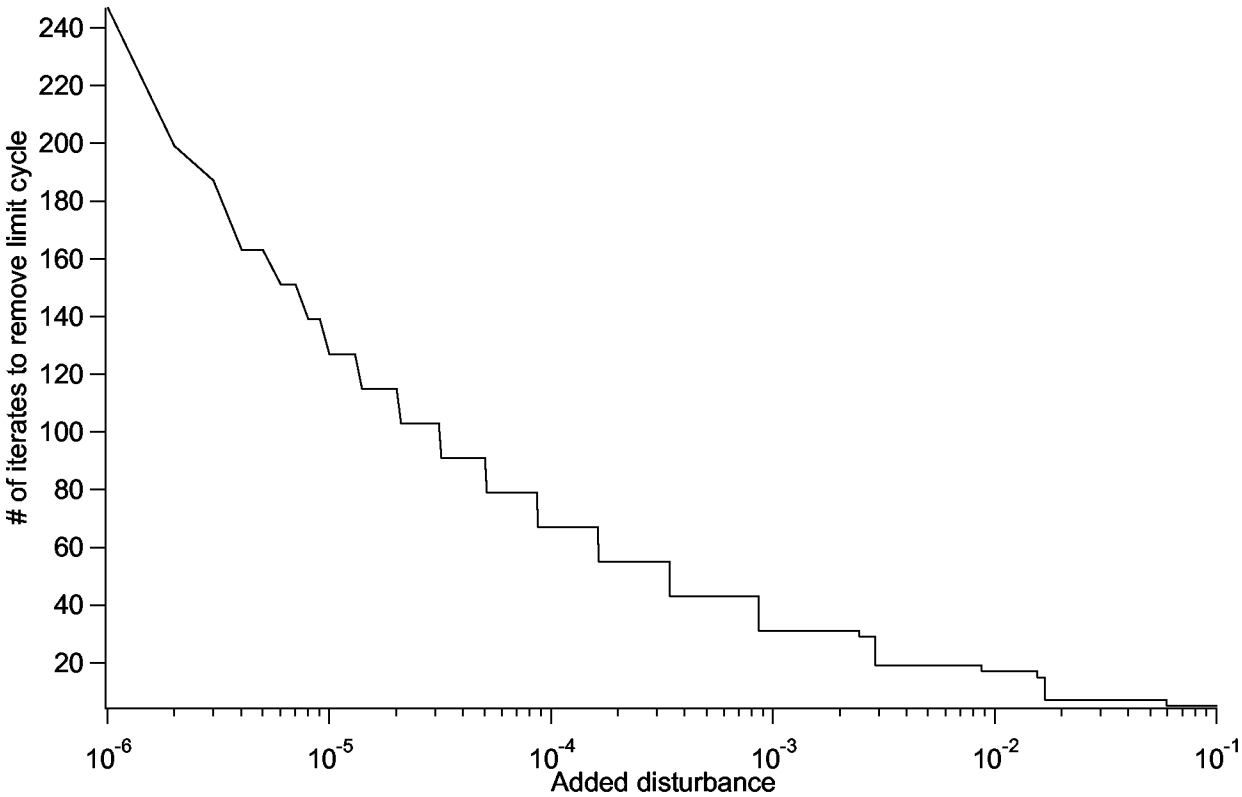

Figure 12

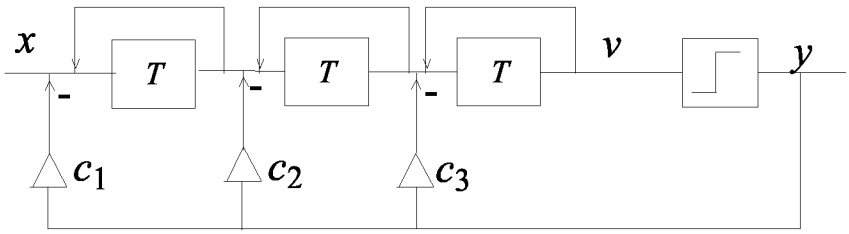

Figure 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2006/050175

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M3/00 H03M7/32 H03M7/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC, COMPENDEX, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 1 202 461 A (STMICROELECTRONICS S.R.L) 2 May 2002 (2002-05-02) abstract; figure 2	1-11
A	REEFMAN D ET AL: "Description of limit cycles in sigma-delta modulators" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART I: REGULAR PAPERS, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 52, no. 6, June 2005 (2005-06), pages 1211-1223, XP007901142 ISSN: 1057-7122 cited in the application section II.A; figure 2; section IV.C, last paragraph; page 1220, lefthand column, lines 52-55	1-11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 October 2006	11/10/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Beindorff, Henk

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2006/050175

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-9,11

   Circuit and method for detecting limit cycles in a sigma delta modulator

   ---

2. claim: 10

   Circuit for removing limit cycles in a sigma delta modulator

   ---

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2006/050175

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1202461 A	02-05-2002	DE 60018573 D1	14-04-2005
		DE 60018573 T2	19-01-2006
		US 2002084924 A1	04-07-2002