ELEC6233 FPGA Implementation of a Complex Number Multiplier

Joshua Tyler
jlt1e16
MSc Embedded Systems
Dr Jeff Reeve

Abstract

1 Introduction

2 Design

Include 'Circuit diagrams' and discussion of design

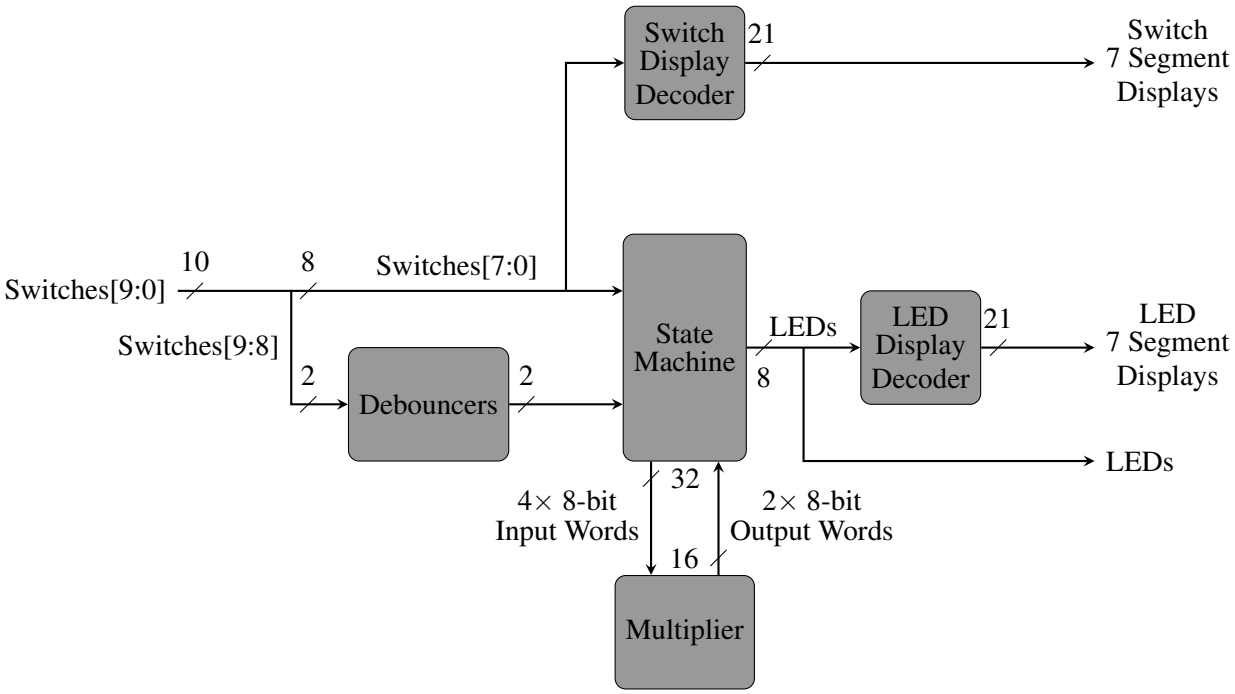

Figure 1: Overall Block Diagram

2.1 Complex Multiplier

2.2 State Machine

3 Verification

Include sample data and results

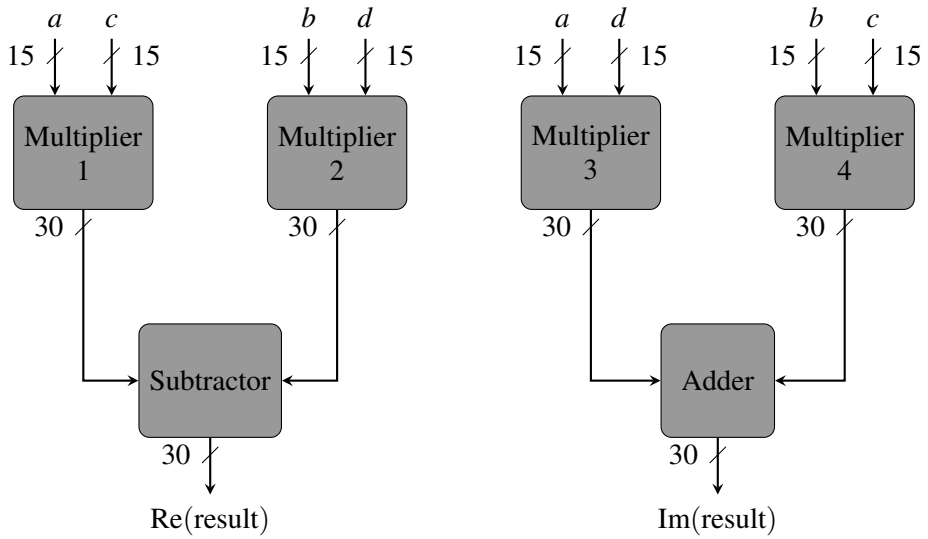

Figure 2: Multiplier architecture

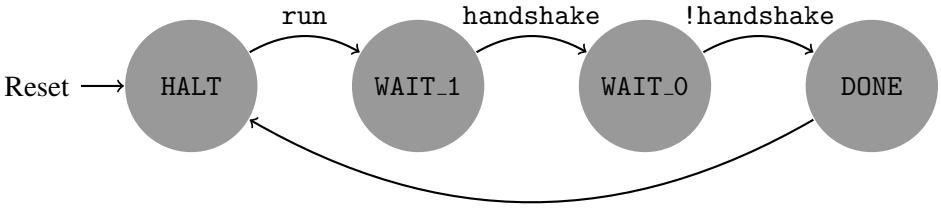

Figure 3: Read state machine state transition diagram

4 Synthesis

Include "Synthesis Result"

5 Conclusion

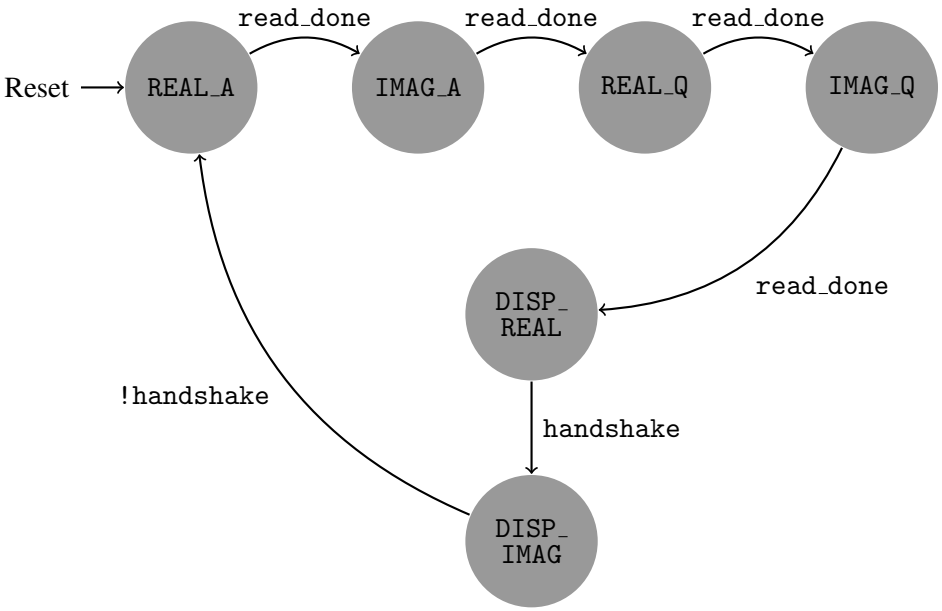

Figure 4: Main state machine state transition diagram

References