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Mercury Delay Line Emulation: Reconstructing Memory for EDSAC

by

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Abstract

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List of Acronyms

EDSAC electronic delay storage automatic calculator.

ENIAC electronic numerical integrator and computer.

PCB printed circuit board.

RAM random access memory.

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Chapter 1

INTRODUCTION

The National Museum of Computing is currently hosting a project to reconstruct a very early computer electronic delay storage automatic calculator (EDSAC) **[cite]** . EDSAC was the first practical digital stored program computer. This means that it was the first practical computer able to accept a program from the user, store it in memory, and execute it on the fly. In contrast to this earlier computers, such as electronic numerical integrator and computer (ENIAC) hard-coded their programs, in the case of ENIAC using 3,600 ten 10-way switches [1]. The only digital stored program computer earlier than EDSAC wa the Manchester small-scale experimental machine. This machine was not intended for general purpose computation however, but rather for testing of a new type of memory [2].

EDSAC ran its first program in May 1949. This poses a significant design challenge for the memory of the machine. Transistors were not commercially available at all until 1951 [3], and valves, whilst available, were physically large, and were fairly expensive. This meant to create a modest amount of storage would not have been feasible. ENIAC used valves, but it also had very little memory. This was not a problem for its intended application, but would have posed a problem for a general purpose computing platform, such as EDSAC[4, p.208].

The solution chosen for EDSAC's storage problem was delay line memory. This was common with other early computers, and works via a fairly simple mechanism. Given a medium able to delay a pulse train by a certain amount, memory can be created by feeding the output of that delay medium back into the input. If the delay time is tuned to be an integer multiple of the system clock frequency, the system is able to store a sequence of bits proportional in length to the delay time. This principle is illustrated in Figure 1.1.

The storage medium used for delay lines exists in various forms, from magnetorestrictive delay lines which function by twisting one end of a coil of wire, then waiting for the stress to propagate to the other end of the wire, to electric delay lines which provide much smaller delays by sending electrical impulses down a length of coaxial wire or printed circuit board (PCB) microstrip trace.

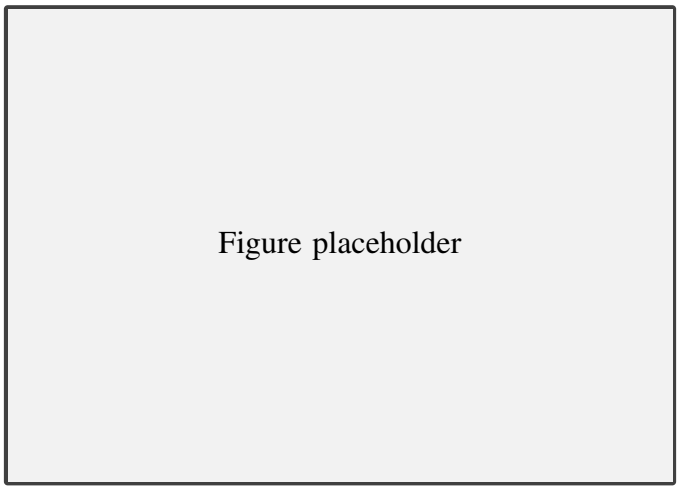

Figure 1.1: Demonstration of the principle of delay line memory

EDSAC used acoustic delay lines in the form of steel tubes, approximately 1.5 m long, and

full of mercury. Impulses were inserted into one end of the tube via a quartz transducer, and reach the other end of the tube after a delay of approximately 1 ms. Here a quartz transducer receives the acoustic impulse and converts it to an electronic impulse.

Creating a faithful reproduction of this system poses challenges, namely: the expense of mercury, the health and safety implications of using mercury in a museum environment, and the technical challenges of the precise machining necessary for the steel tubes. As a result of this the project is currently intending to use magnetorestrictive delay lines [5].

These delay lines are anachronistic for the time, and are very dis-similar in appearance to the original delay lines. In addition to the development of such lines poses its own set of technical challenges. For this reason it was decided to use modern technology to create a replacement for the original delay lines. This replacement is required to be indistinguishable from the original in terms of appearance and electrical interface. The design of this system is the goal of this project.

Chapter 2

TECHNOLOGY REVIEW

This Chapter presents a review of the relevant literature surrounding the delay lines used in EDSAC, and uses it to derive a specification for the recreated delay line. Much of the literature presented comes from original documentation produced by Maurice Wilkes, the man in charge of the original EDSAC project.

2.1 EDSAC Delay Line Specification

As briefly discussed in Chapter 1, EDSAC uses mercury delay lines as memory. These are primarily used in two ways:

1. Short tubes used for the results of calculations.
2. Batteries of longer tubes used as the main memory store, what would be termed random access memory (RAM) in a modern computer.

EDSAC stores words in units of 36 pulses, which is referred to as a minor cycle. 34 pulses are used to store the magnitude of a number, one stores the sign, and one acts as a space between numbers. This system was chosen to allow storage of ten digit numbers.

The shorter tubes are sized to store only a single minor cycle, but the longer tubes are long enough to store 576 pulses (16 minor cycles). The batteries of each of these tubes each contained 16 tubes, and EDSAC originally had two batteries, allowing for a total storage capacity of $16 \times 16 \times 2 = 512$ numbers.

2.1.1 Timing

The memory in EDSAC uses a circulating bit rate of 500 kHz. This is made up of a 0.9 µs pulse, and a 1.1 µs gap for each bit. The pulse is a burst of 13.5 MHz carrier frequency if the bit is a logical 1, or it is 0V if the bit is a logical 0.

In the regeneration portion of the circuitry, the pulses are demodulated from the 13.5 MHz carrier and stretched to approximately 1.9 µs long, i.e. just long enough that each pulse fails to overlap it's neighbour [4, p.212].

This is critical because it means that the pulses that have passed through the delay line are effectively resynchronised to the system clock. If the system did not work in this way, then the delay lines in the the original EDSAC would never have worked. The propagation time of acoustic waves through mercury varies slightly with temperature, and the cumulative effect of this through all the delay lines of the store would mean that pulses would be unlikely to align with the system clock at the other end.

This does imply that the maximum acceptable skew of the delay line from its nominal delay is $\pm$ 0.5 µs. In reality however this doesn't take into account other factors such as the jitter and long term drift of the system clock, and the slew rates of the analogue circuitry. Whilst the demodulating pulse is lengthened to 1.9 µs, it is unlikely to be consistently at it's peak voltage for this time, and so the output pulse is likely to have a better shape if the delay line produces an output in the middle of this period.

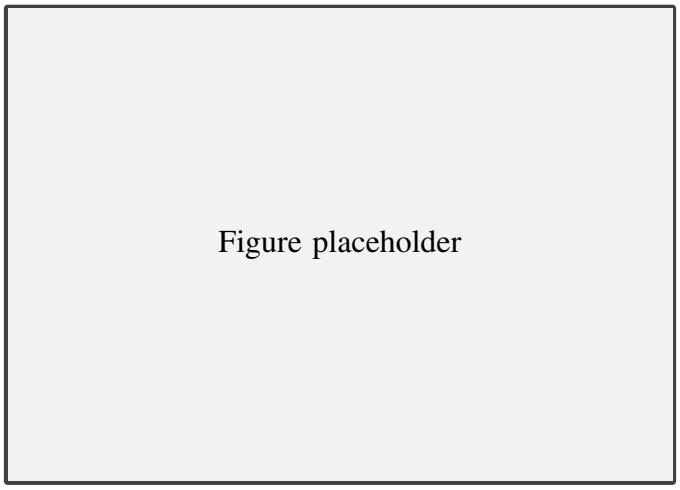

Figure 2.1: EDSAC pulse timing

2.1.2 Electrical

Electrically speaking, EDSAC originally drove the delay lines with a nominal voltage of 25 V peak, through a 70 Ω terminated transmission line. The loss in the delay lines was 69 dB, leading to an output voltage of approximately 10 mV.

Despite this, the recreation project has discovered that the regeneration circuitry actually feed the delay lines with a decreasing voltage as the pulses propagate through the lines. The voltage starts off at approximately 35 V for a signal fed to a delay line at the start of the store, but is reduced to approximately 25 V peak for the tubes at the end of the store.

In addition to this, problems were experienced with amplifying the low signal level output by the delay lines. Because the current wire delay line solution has flexibility in its output voltage, currently the delayed signal is output at 100 mV peak.

2.1.3 Mechanical

The mercury delay lines originally consisted of banks of steel tubes, each tube having an outer diameter of 4.44 cm, and an inner diamter of 2.86 cm [4, p. 213]. The tubes are then held in an array using machined end-plates.

Chapter 3

SPECIFICATION

The research of Chapter 2 has led to the derivation of a specification for the delay line I will produce. This specification is detailed in Table 3.1.

Table 3.1: Delay line specification

Item	Specification	Justification
1	**Must** be capable of producing a delayed copy of the EDSAC pulse train presented to it's input	This is the primary function of the device
2	**Must** have a skew against the nominal delay of **[xx]** , and a jitter of **[xx]**	**[foo]**
3	**Must** be able to accept input voltages in the range of **[xx]** to **[xx]**	This is necessary to mimic the performance of the original delay line
4	**Must** be able to have an adjustable nominal output delay in the range of **[xx]** to **[xx]**	An adjustable output voltage in this range allows compatibility with both the original electrical interface, and that used by the reconstruction effort.

Chapter 4

SYSTEM DEVELOPMENT

4.1 Delay line

4.2 Testbench

4.3 Amplifier

Chapter 5

TESTING AND VERIFICATION

5.1 Delay line

5.2 Testbench

5.3 Amplifier

Chapter 6

PROJECT PLANNING

Chapter 7
CONCLUSION

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Appendix A

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