Task	Timeline
Delay line Testbench Improvement	Week 2 (June)
Visit to TNMoC	Week 4 (June)
Report demonstration	Week 13 (August/September)
Visit to TNMoC	Week 14 (September)
Documentation	Week 1 – Week 14
Creation of report template and ToC draft	Week 1 (June)
Intial draft of technology review and first part of implementation	Week 10 (August)
Review of what has been written to date	Week 12 (August)
Writing implementation	Week 12 (August)
Design report diagrams	Week 12 (August)
Report writing	Week 13
Report writing	Week 13
Report writing	Week 14
Report checking	Week 14
Initial delay line HDL implementation	Week 1 – Week 2
Architecture Research	Week 1
Verilog Implementation	Week 1
Testbench Design	Week 1 – Week 2
Initial test harness HDL implementation	Week 2 – Week 3
Requirements capture and system design	Week 2
Verilog Implementation	Week 2 – Week 3
Testbench Design	Week 2 – Week 3
Initial Test Harness GUI Design	Week 3 – Week 4
Creation of proof-of-concept UART driver program	Week 3
C++ program architecture design	Week 3
C++ implementation	Week 3 – Week 4
Integration of test harness GUI, test harness, and delay line	Week 5
Make improvements to GUI	Week 5 – Week 6
Initial Analogue Design	Week 6 – Week 7
FGPA power investigation	Week 6
Test harness input/output amplifier design	Week 6 – Week 7
Phantom power circuitry design	Week 7
Phantom power investigation	Week 8 – Week 9
Research into how valve design works	Week 8
SPICE simulation of EDSAC output stage, and phantom power draw	Week 8
Redesign of phantom power circuitry	Week 8
Investigation into regeneration input circuitry	Week 9
Building final delay line circuitry	Week 9
Selection of parts to order, and ordering	Week 9
Assembling and testing sub-systems	Week 10 – Week 11
Assembling and testing sub-systems	Week 10 – Week 11
Integration testing and modification	Week 11 – Week 12
Re-implement part of circuit to improve noise crosstalk	Week 12 – Week 13