VIRGINIA TECH

Lecture 2

Package Types and Considerations

January 23, 2025

Reminders & Announcements

- I'll be traveling internationally from the evening of the 27th to the evening of the 31st and may be delayed in responding to emails. I will teach the lectures virtually next week

- Office hours:
  - Wednesday, Jan. 29th, 3:00pm – 4:00pm ET
  - See syllabus and Canvas Calendar for Zoom link

- Quiz #1 next week
  - Canvas Quizzes
  - 5 multiple choice questions
  - Conceptual, no calculations
  - Open book/note, individual work

Lecture 1 Summary

1. What is electronics packaging?
   - Interconnecting, powering, cooling and protecting the system components
2. What are the four functions of a package?
   - Signal and power distribution and integrity, thermal management, protection
3. What are key packaging considerations?
   - Electrical performance, thermal, reliability, size, cost, …
4. What are some components in an electronics package?
   - Die attach, substrate, interconnect, terminals, encapsulant

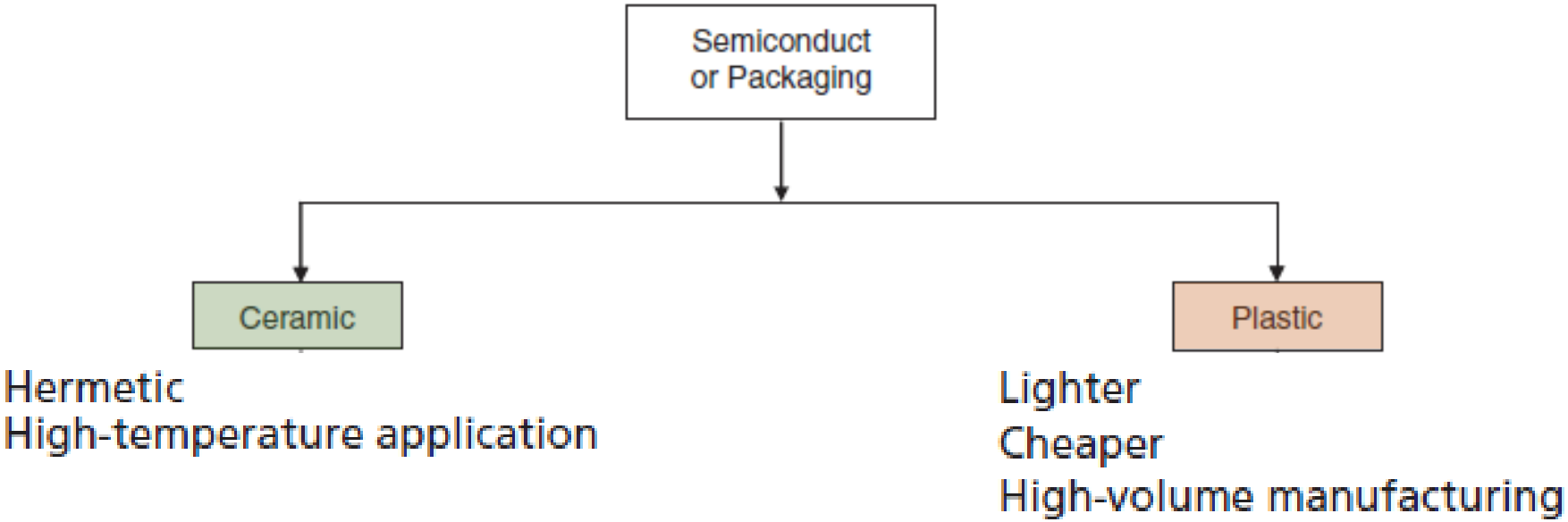
Ceramic and Plastic Packages

Package Type	Advantages	Disadvantages
Ceramic	• Hermetic* • High-temperature • Low CTE** compatible with semiconductor devices • Good thermal conductivity	• Heavy • Brittle • Expensive • Low-volume manufacturing
Plastic	• Lightweight • Cheap • High-volume manufacturing	• Moisture sensitive • Not for high-temperature applications • Low thermal conductivity

*Hermetic – a seal or closure that is airtight.

**CTE = Coefficient of Thermal Expansion

Semiconductor Packaging Schemes



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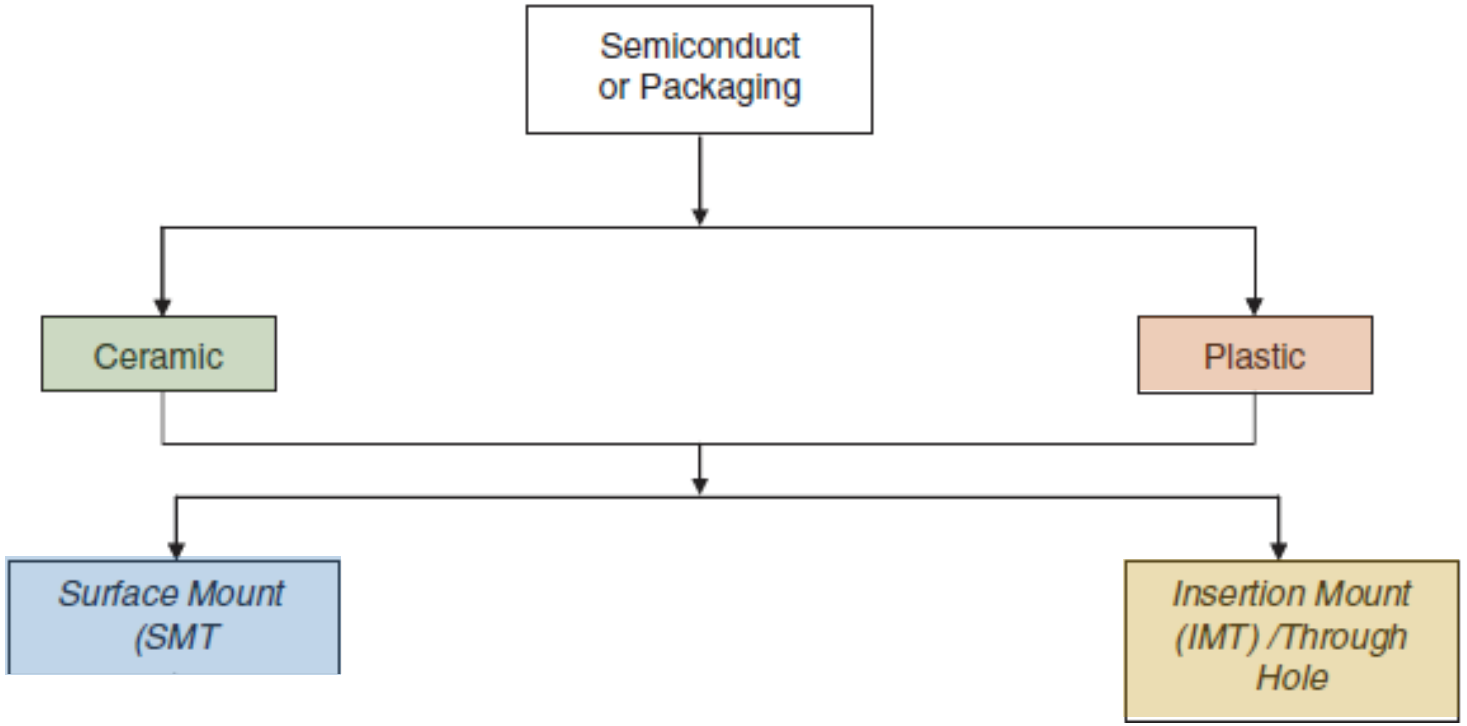
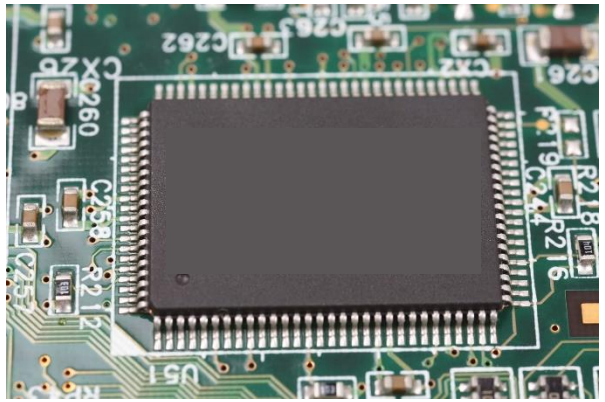
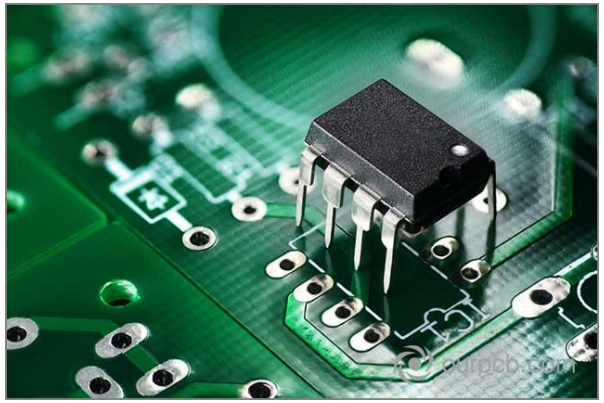




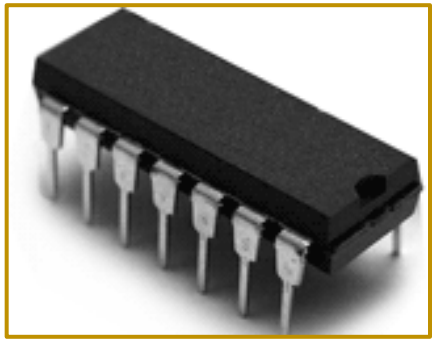
Bonded to the *surface* of a substrate (e.g., PCB, PWB).

Has pins that are inserted *through* holes in a printed circuit board (PCB) or printed wiring board (PWB).



Through-Hole vs Surface Mount

	Through-Hole	Surface Mount (SMT/SMD)
Strengths	• Manufacturability • Testability • Thermal • Mechanical	• Density/size • Electrical performance • Assembly speed and automation



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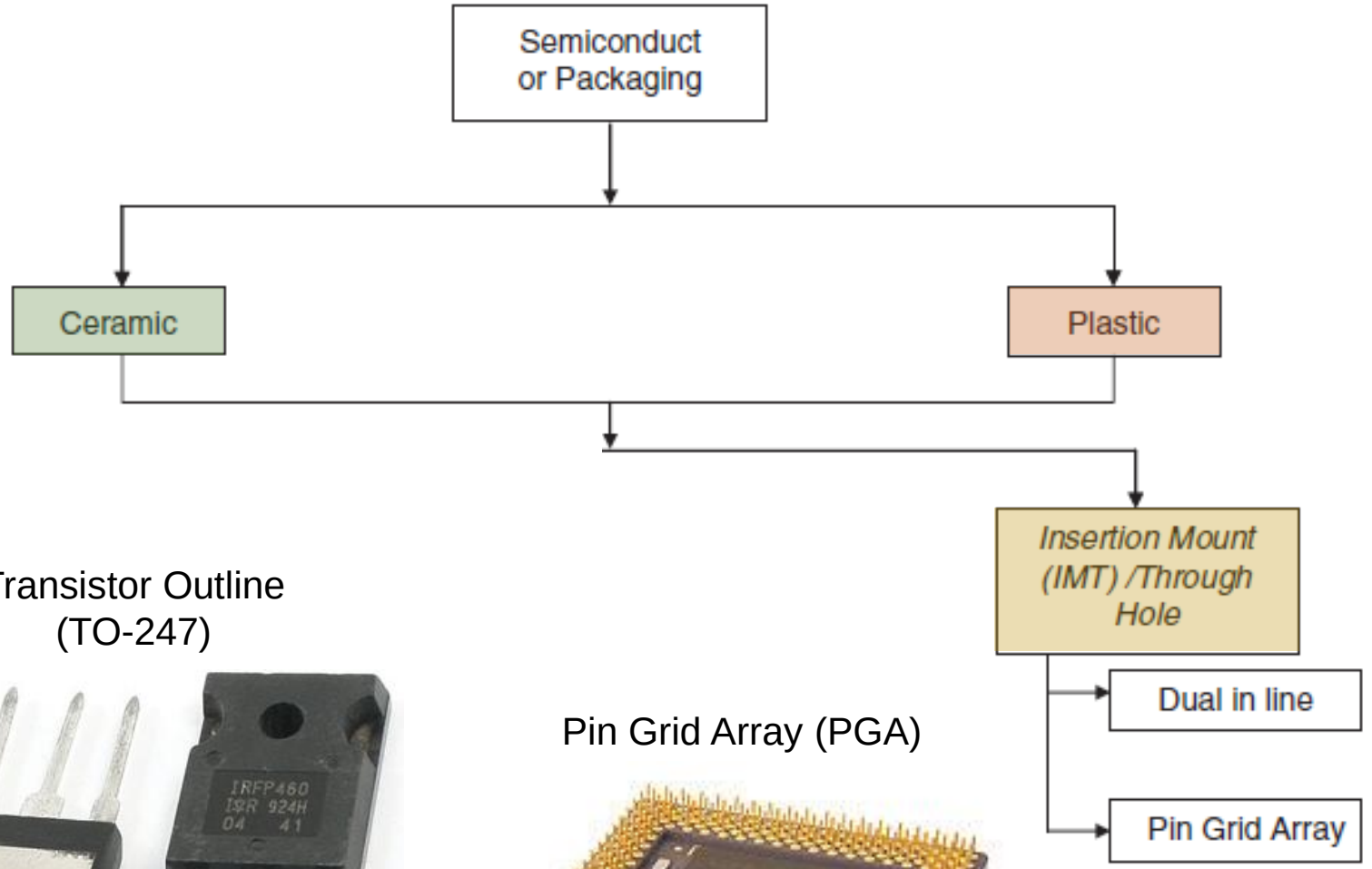
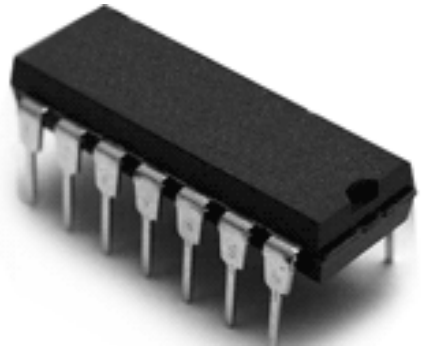
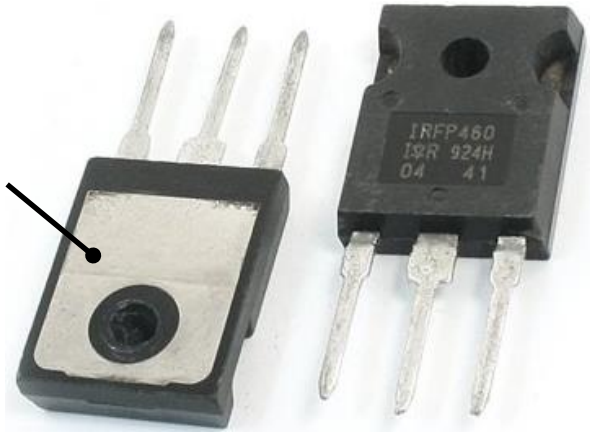


Dual in Package (DIP)



Transistor Outline
(TO-247)

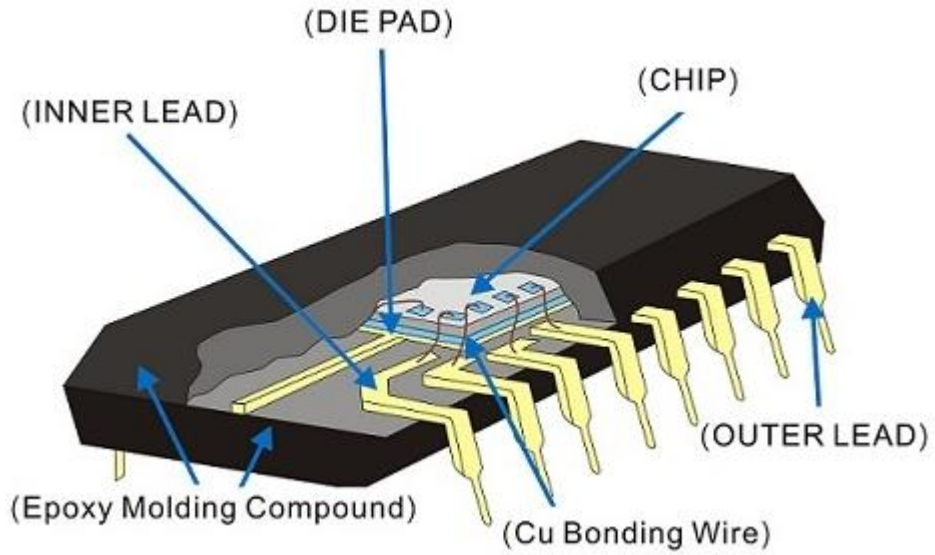
Mount to
heatsink



Pin Grid Array (PGA)

Inside the Package

Dual in Package (DIP)



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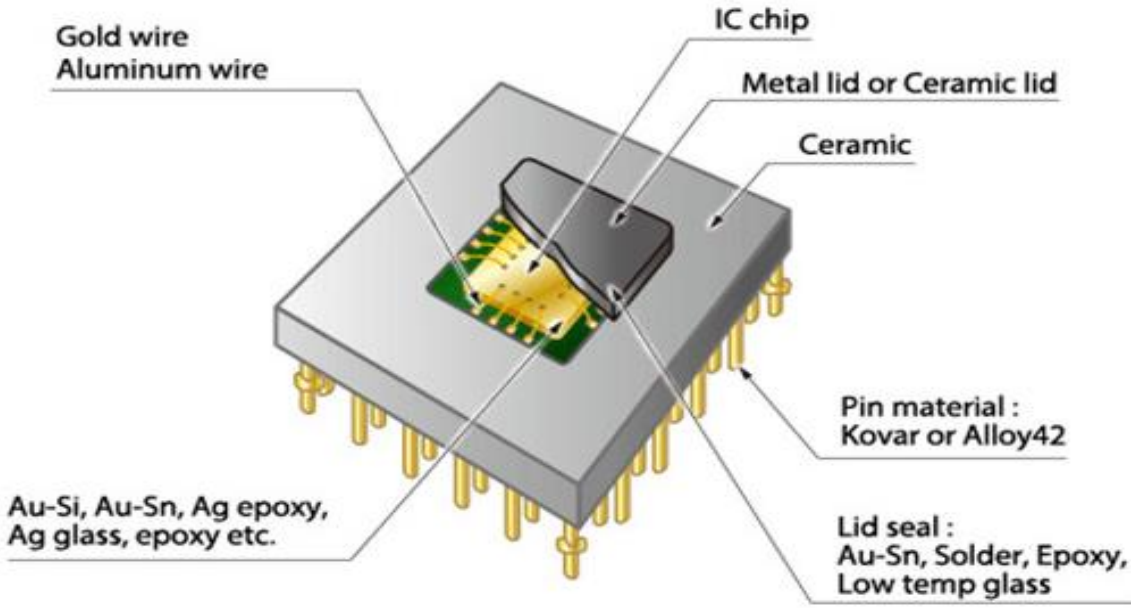

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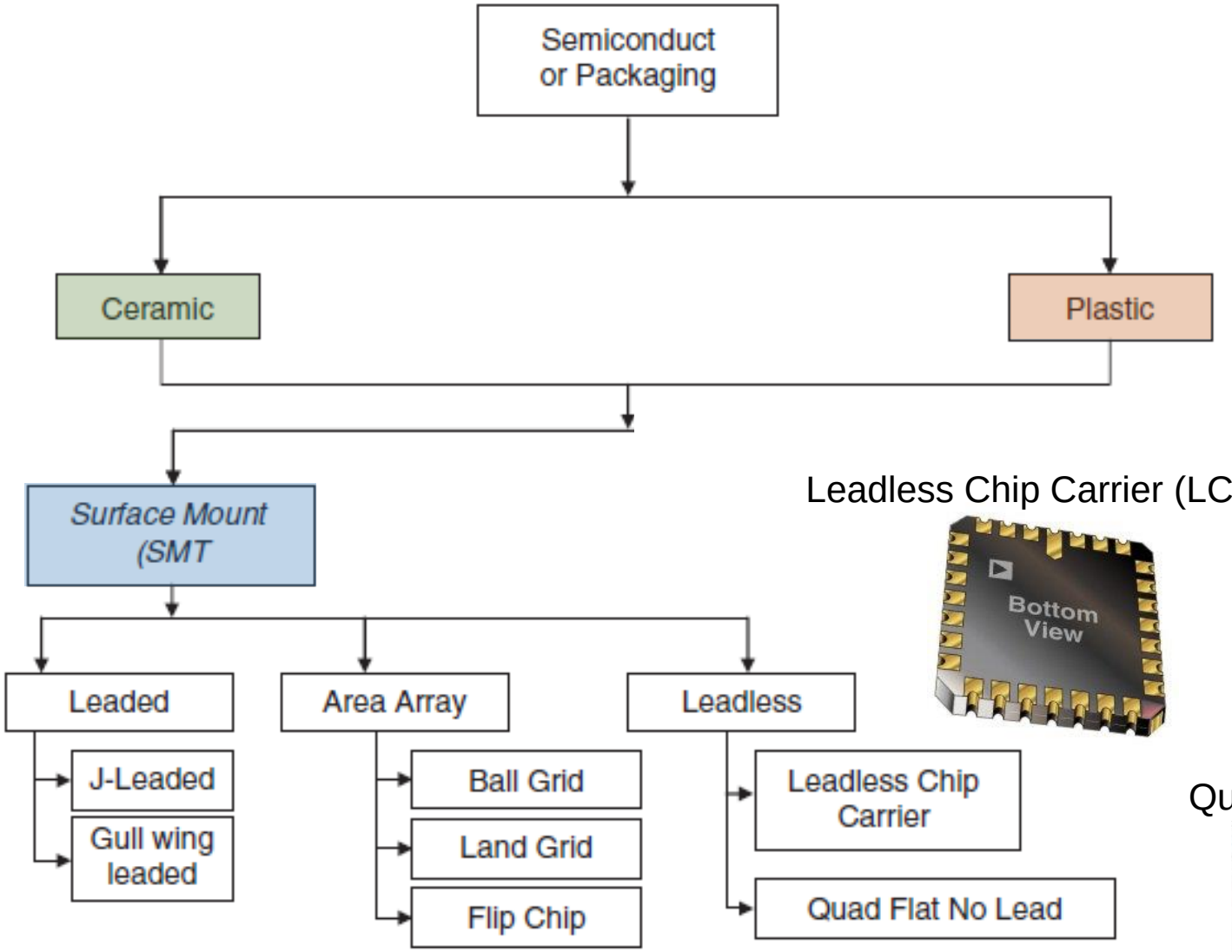
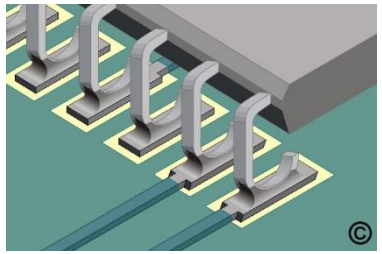
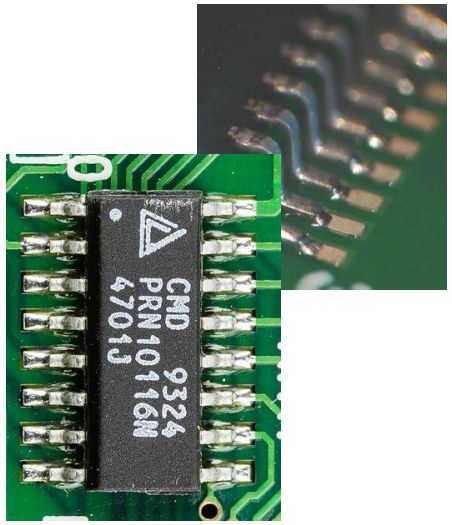


J-Leaded

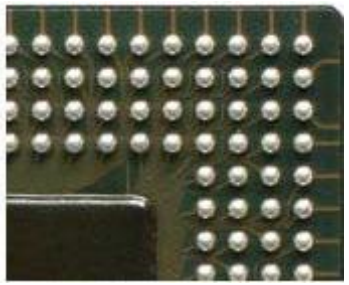


Gull Wing

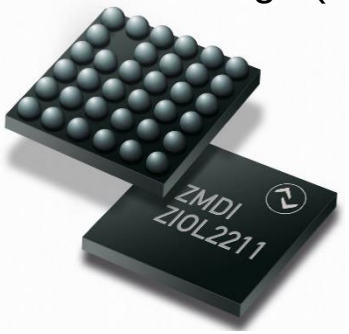


Leadless Chip Carrier (LCC)

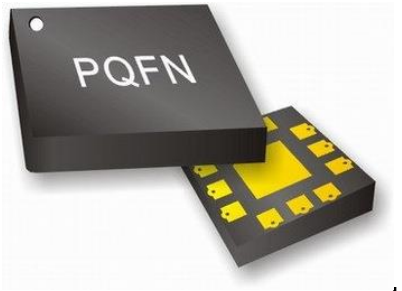
Ball Grid Array (BGA)



Chip-Scale Package (CSP)

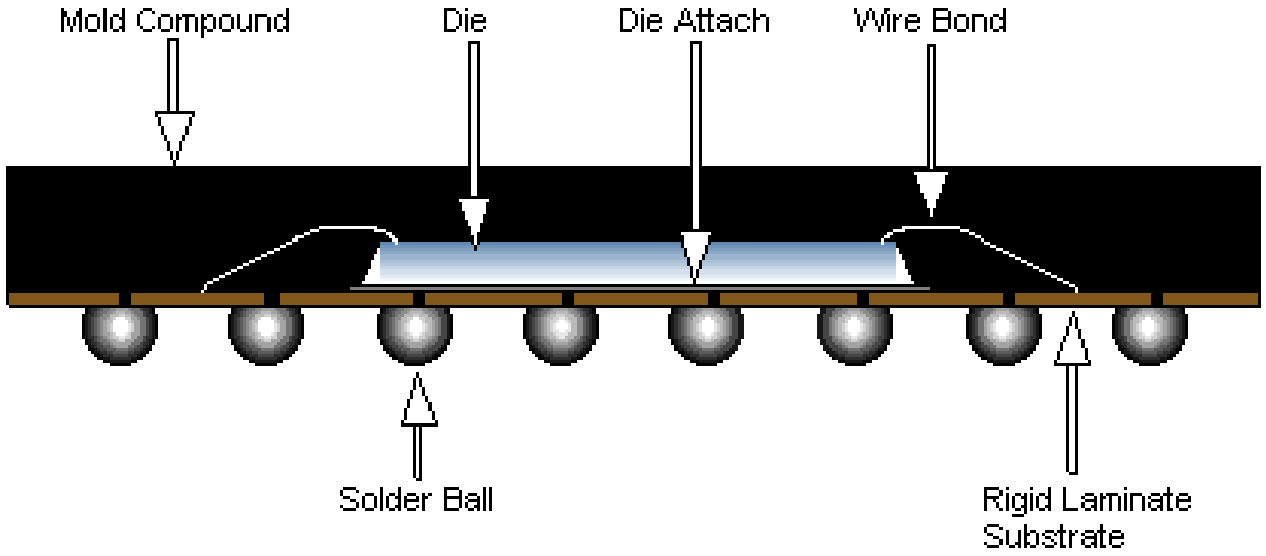


Quad Flat No Lead (QFN)

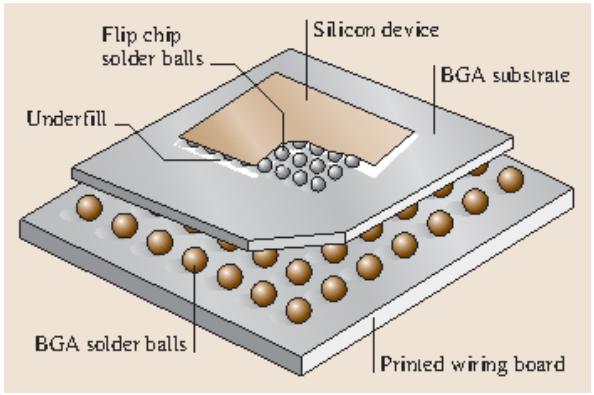


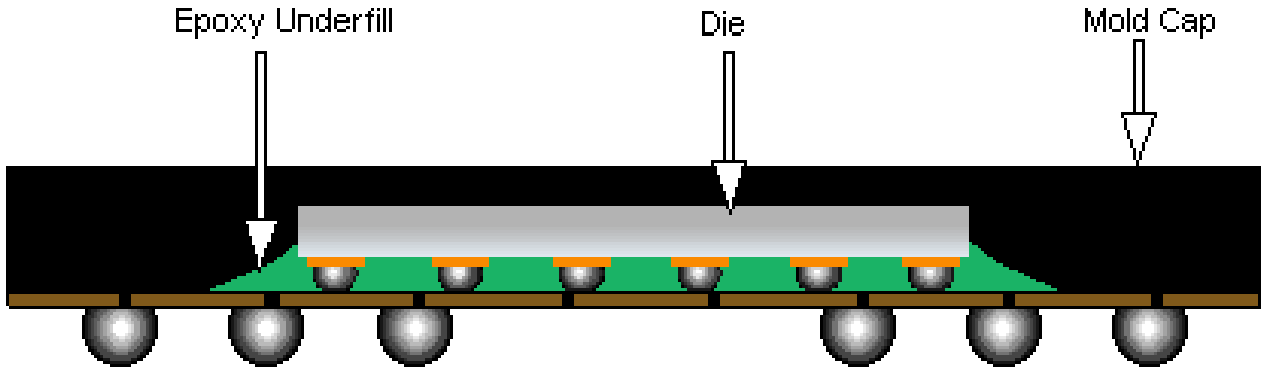
Inside the Package

WIRE BOND

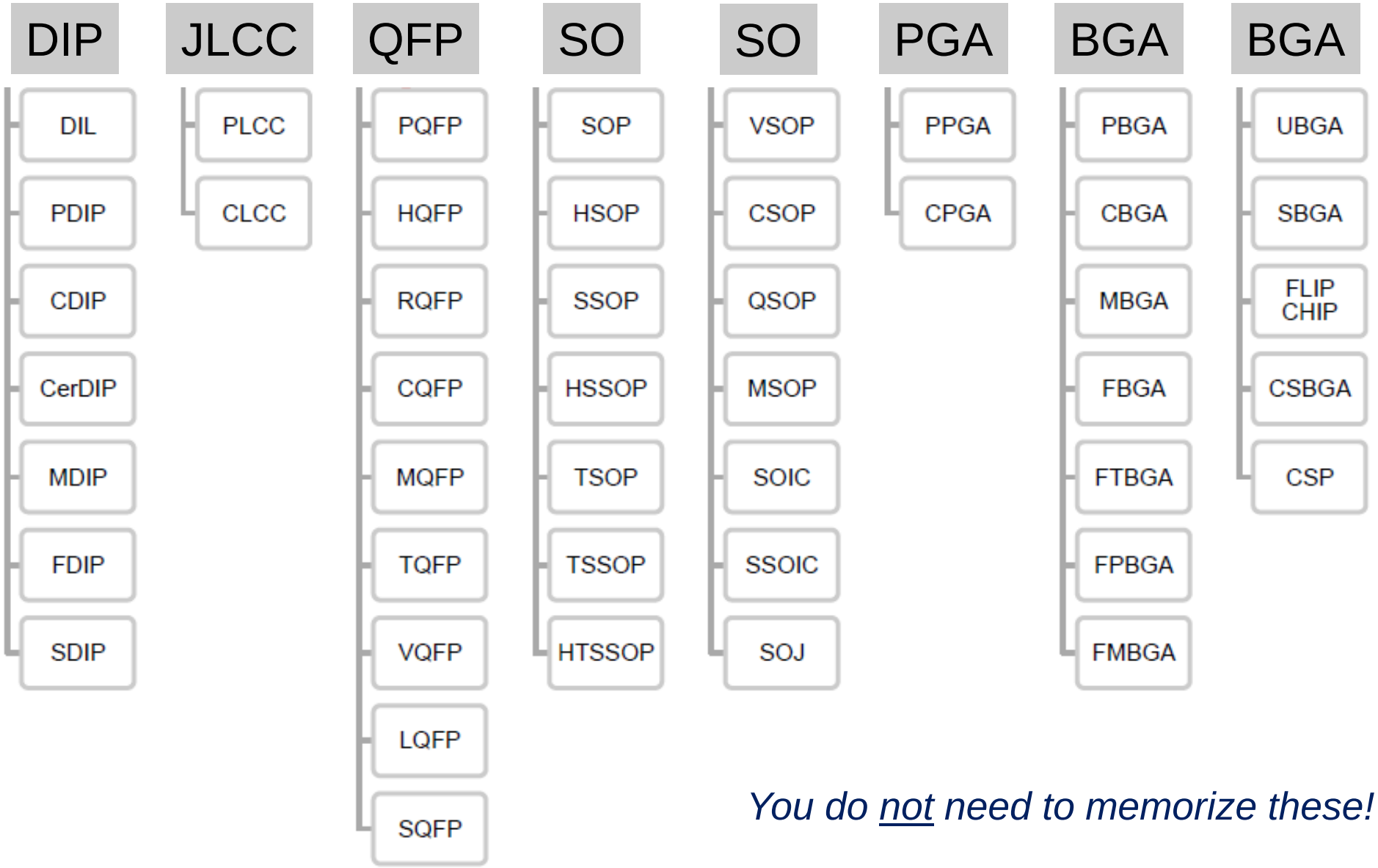


FLIP CHIP

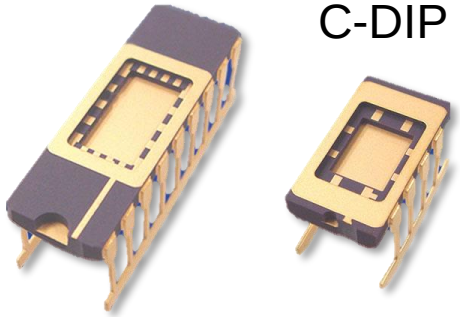
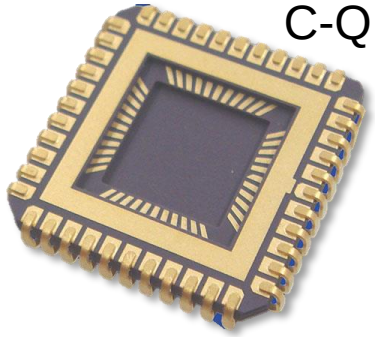
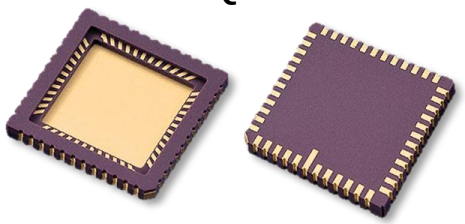
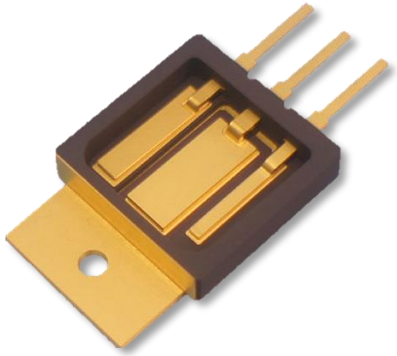
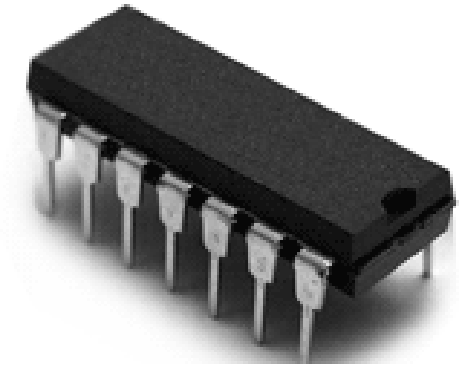
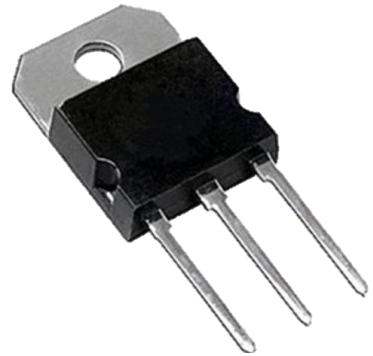




There are Many Types of Packages…



You do not need to memorize these!

Material	Dual in-line Package (DIP)	Quad Flat J-Lead (QFJ)	Quad Flat No Lead (QFN)	Transistor Outline (TO-3P)
Ceramic	 C-DIP	 C-QFJ	 C-QFN	
Plastic				

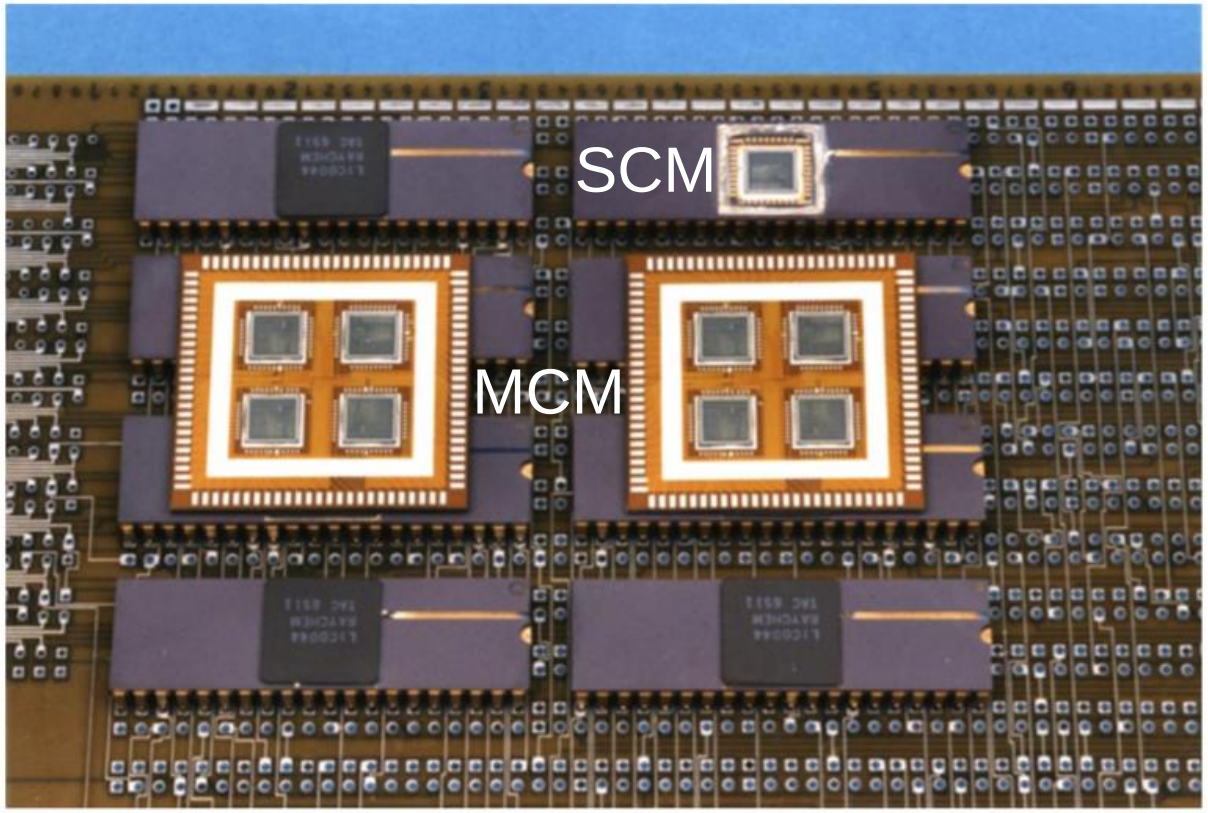
Ceramic:
- Hermetic
- High-temperature
- High-reliability

Plastic:
- Low-cost
- High-volume manufacturing
- Lightweight

Multi-Chip Module (MCM)

- An MCM is a single package containing more than one chip.

- What are the advantages of an MCM over multiple SCMs?
  - Smaller size and weight
  - Better performance (shorter interconnects)
  - Lower cost



Source: Advanced Packaging Systems/ICE, "Roadmaps of Packaging Technology" 16208

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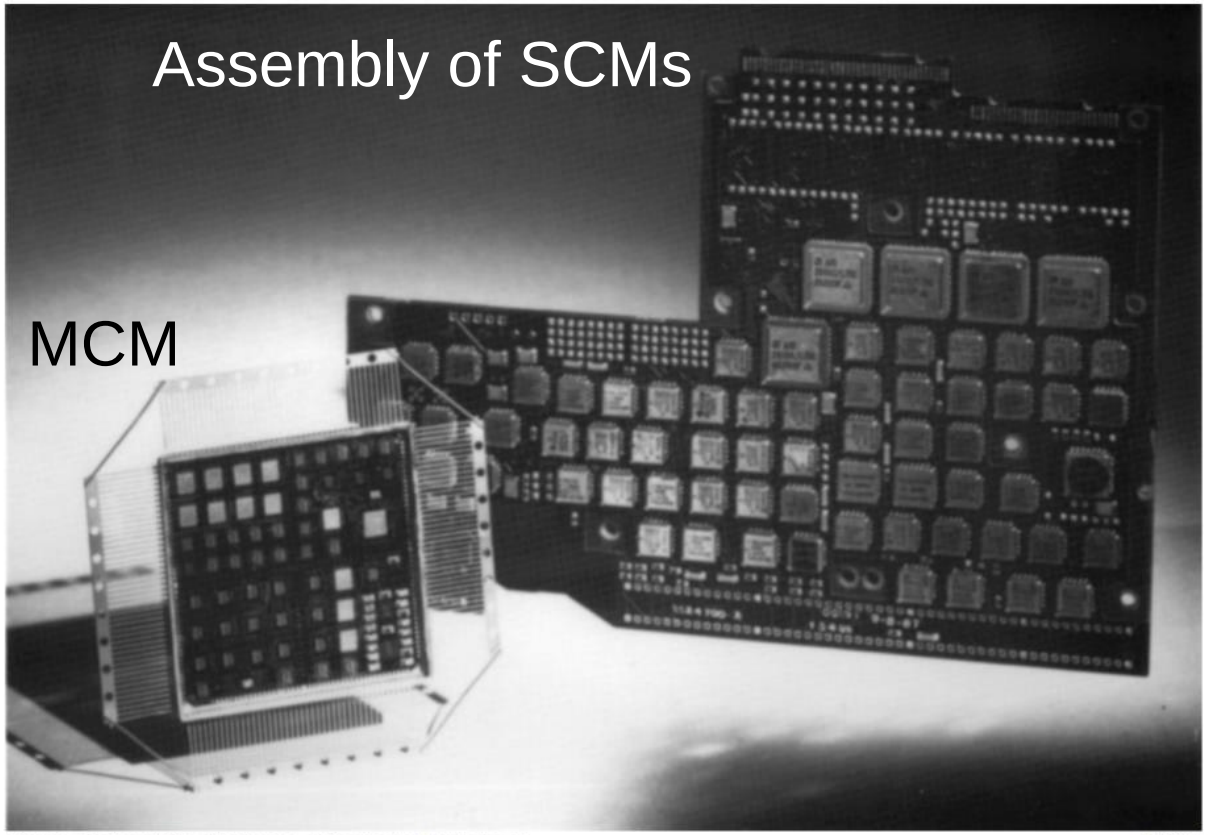


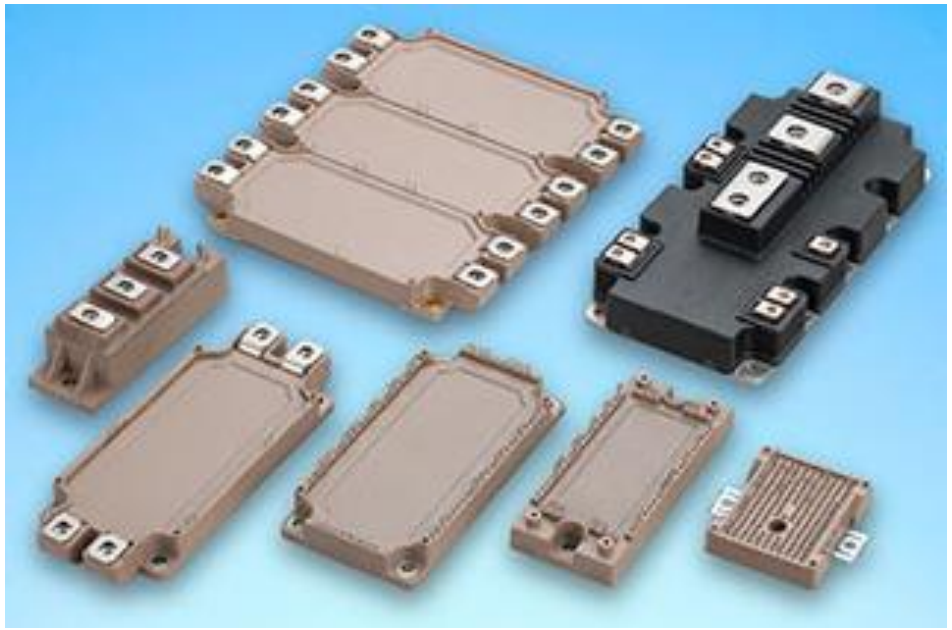
Source: Rockwell/ICE, "Roadmaps of Packaging Technology" 16204

Power Multi-Chip Module

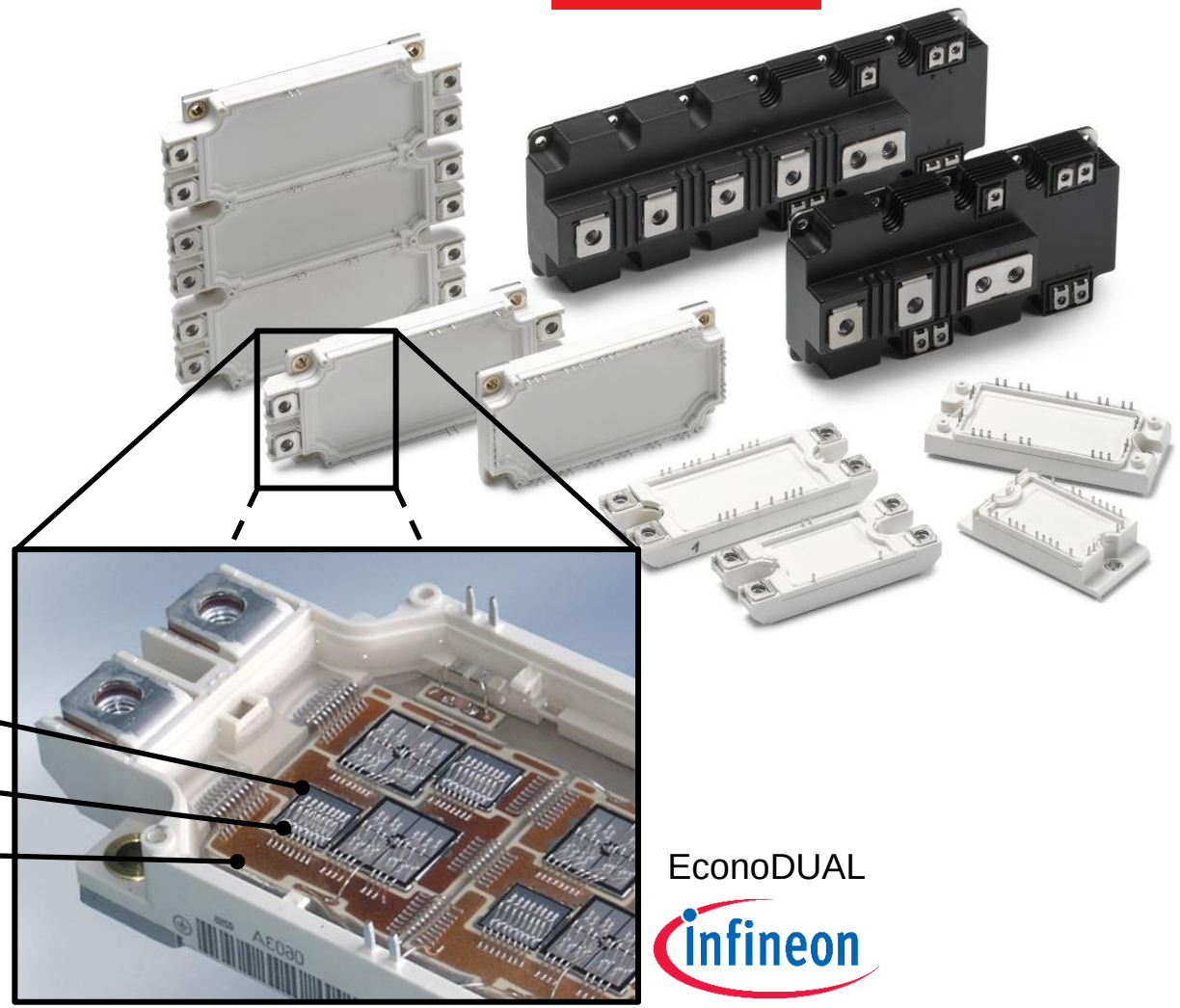
HITACHI
Inspire the Next

Power Multi-Chip Module

Fuji Electric



Danfoss



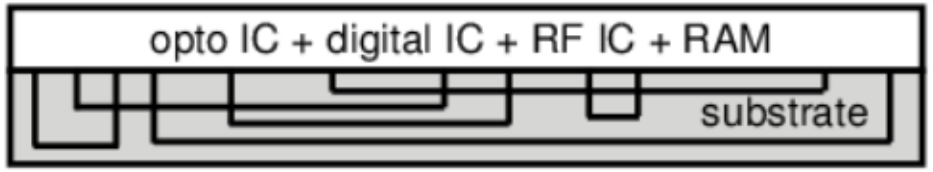
EconoDUAL

infineon

Systems Packaging

System-on-chip

SOC
complete system
on one chip



Multi-chip module

MCM
interconnects
components

System-in-package

SIP
stacked chips
or packages

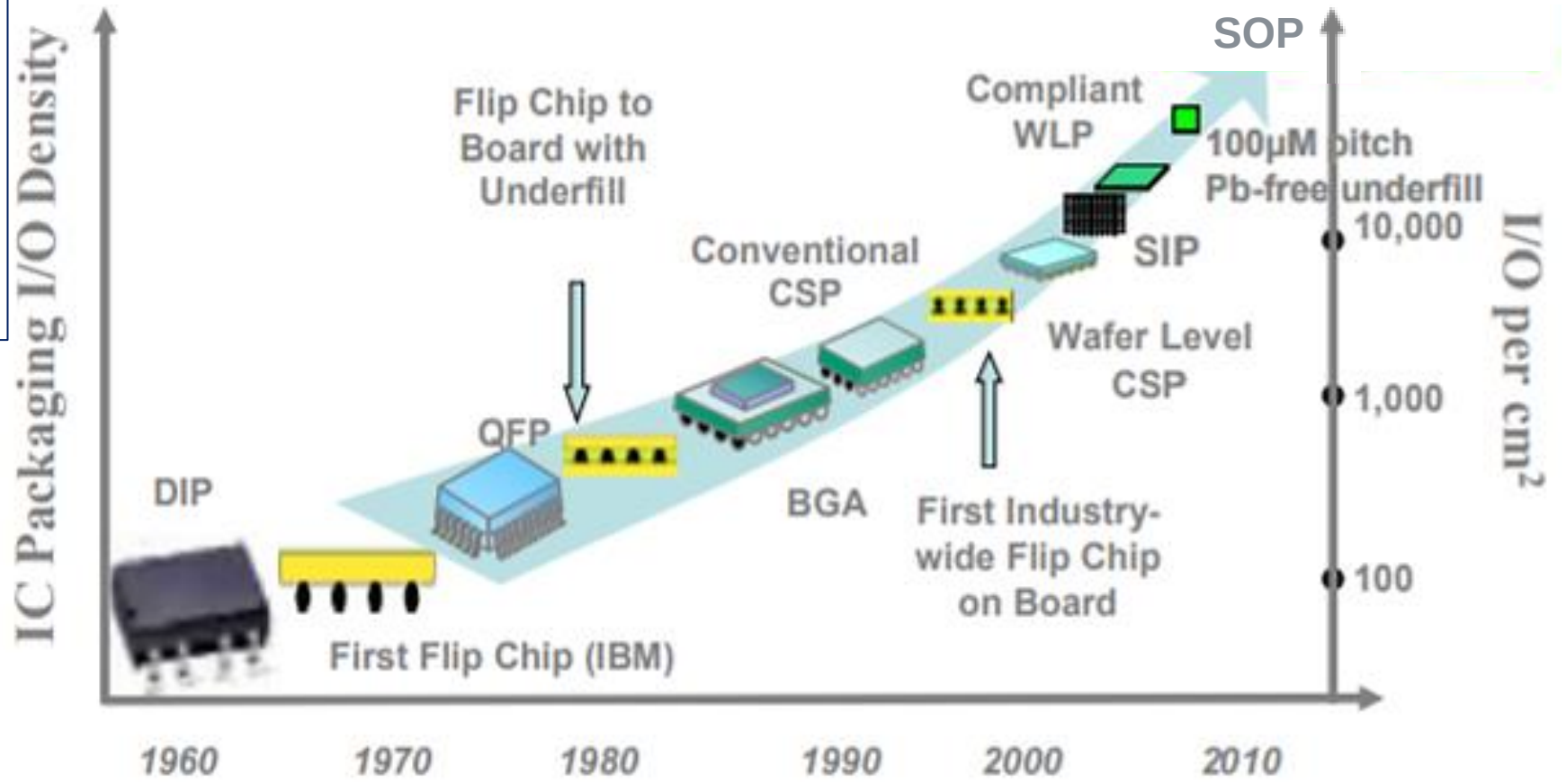
System-on-package

SOP
optimizes btw
chip/package

Packaging Evolution: Package Types & I/O Density

Trends:

1. Increasing packaging I/O density



DIP= dual in line

QFP= quad flat pack

BGA= ball grid array

CSP= chip scale package

WLP= wafer level package

SIP= system in package

Packaging Evolution: Package Size Efficiency

Trends:

1. Increasing packaging I/O density
2. Increasing packaging efficiency

PGA= pin grid array

QFP= quad flat pack

BGA= ball grid array

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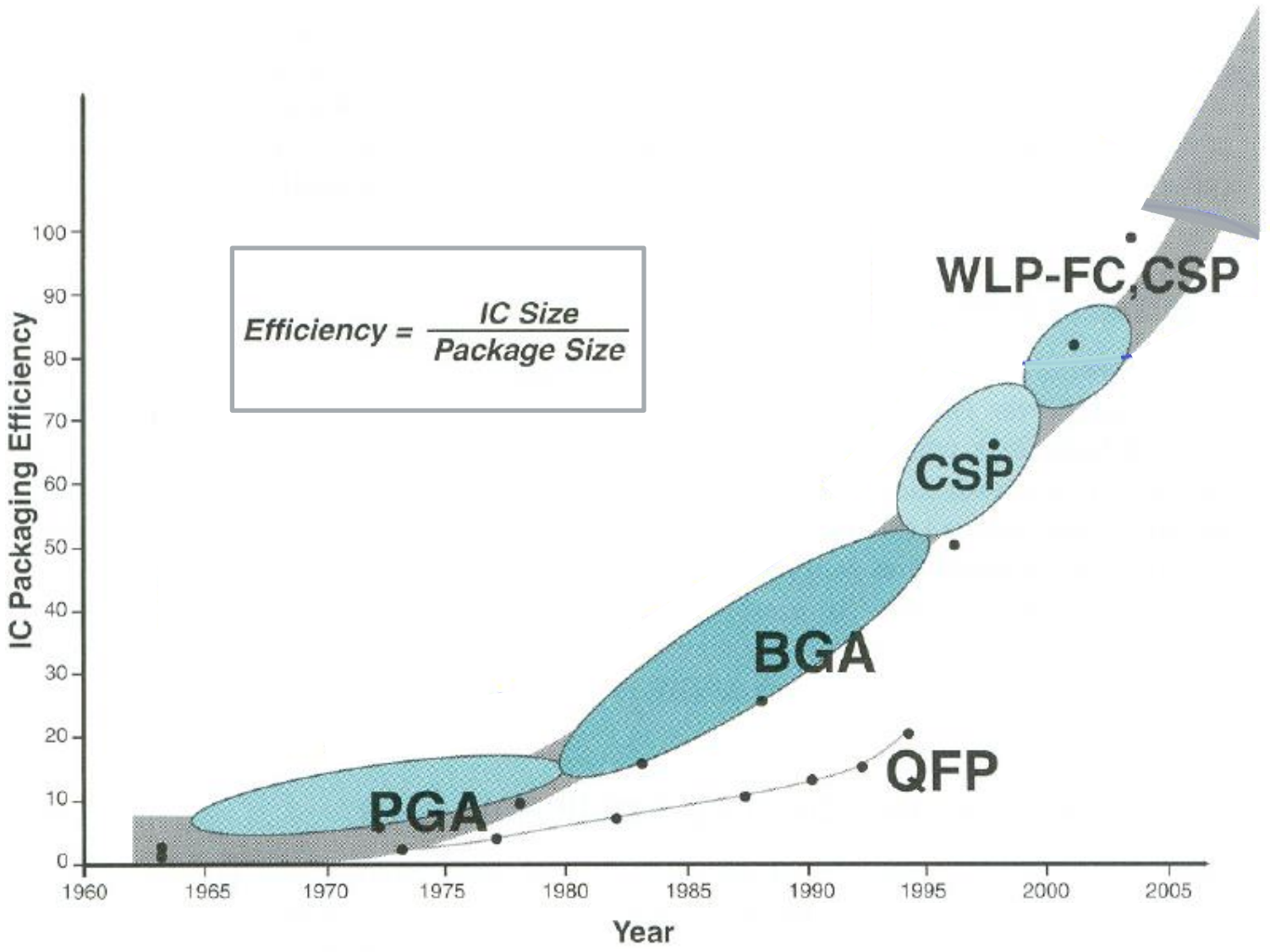


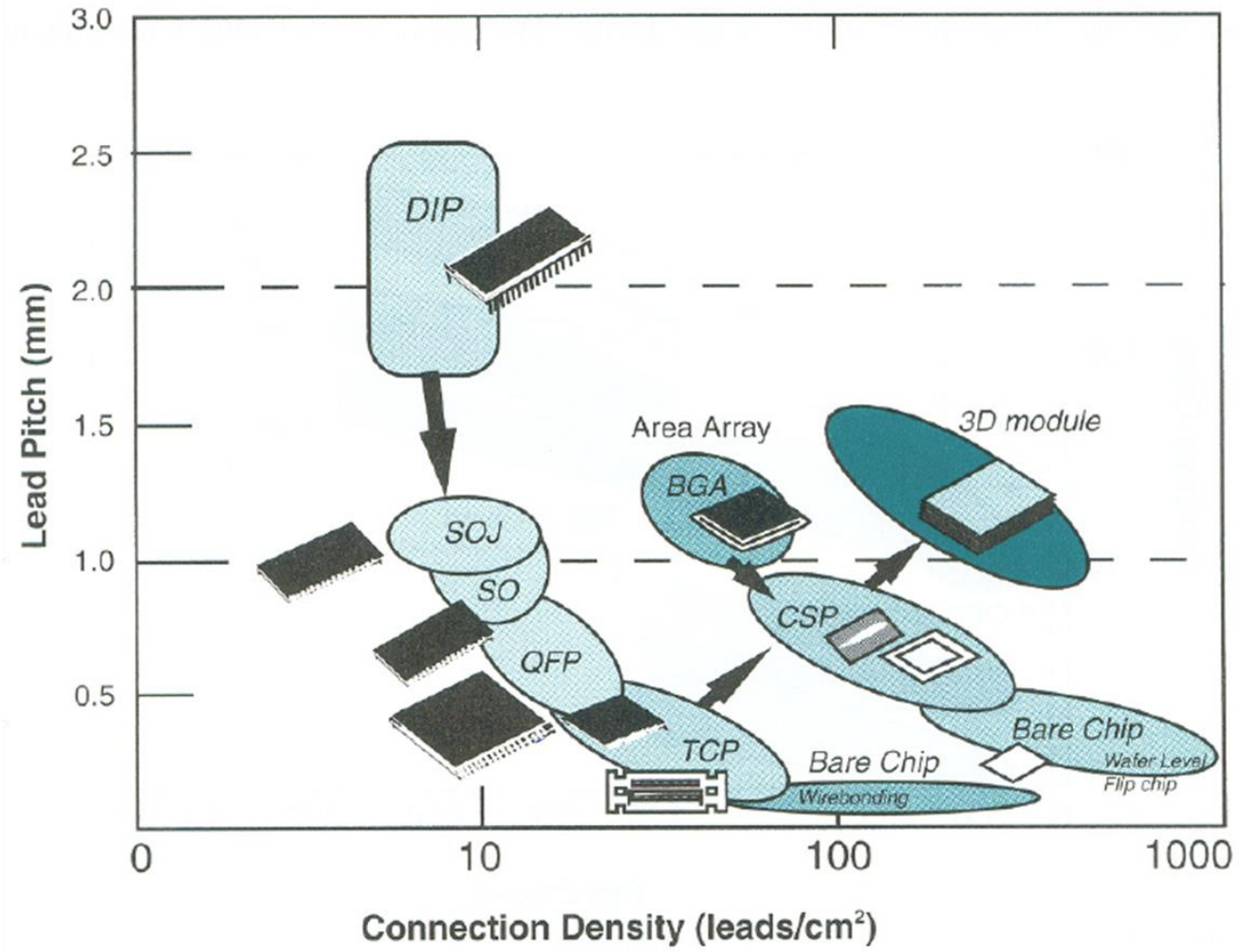
IC packaging efficiency of various single chip packages.

"Fundamentals of MSP" –Rao Tummala

Packaging Evolution: Interconnect & Lead Pitch

Trends:

1. Increasing packaging I/O density
2. Increasing packaging efficiency
3. Decreasing interconnect & lead pitch



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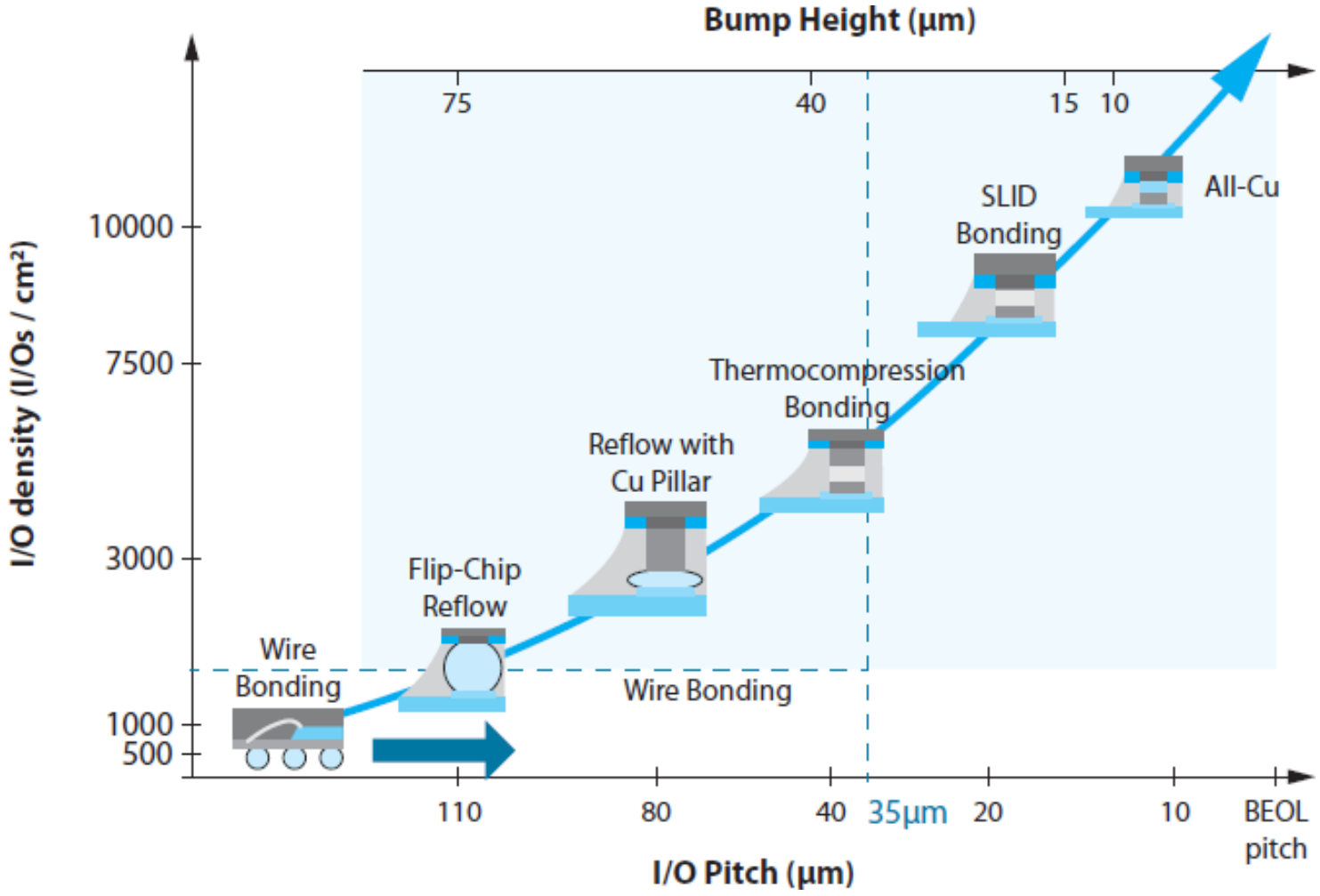

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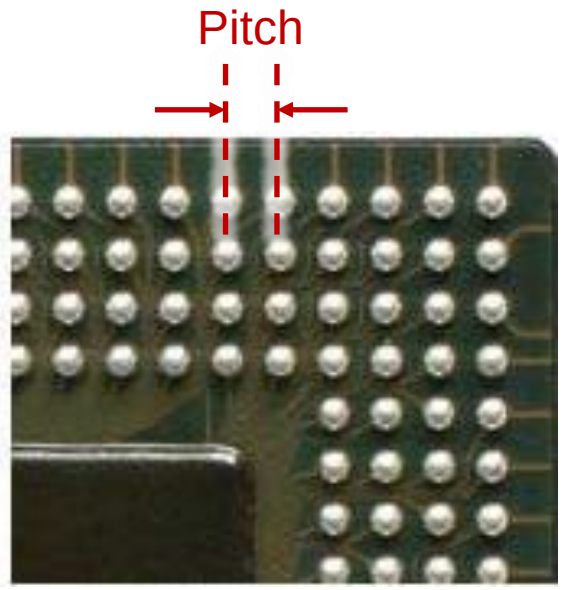
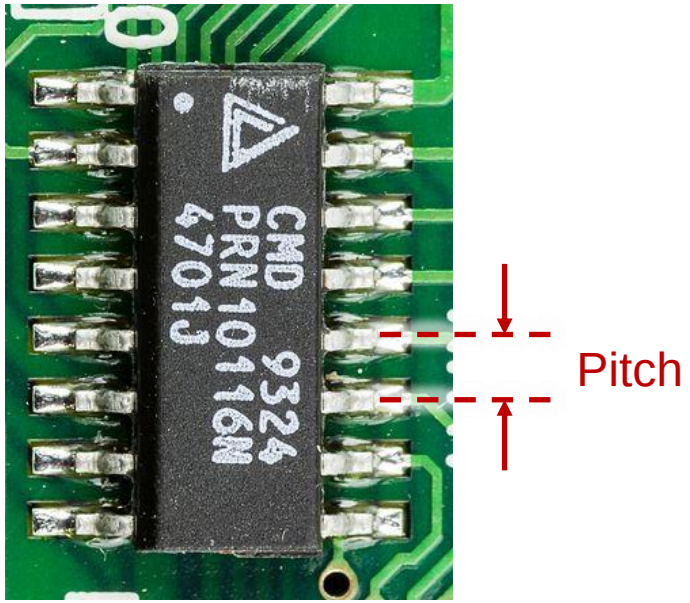
Packaging Evolution: Interconnect & Lead Pitch

- **Pitch** – center-to-center distance between adjacent interconnects, I/Os, or leads
- The I/O pitch is directly related to the **I/O density** – the *finer* the pitch, the *higher* the I/O density
- Reducing interconnect pitch has been key to achieving higher densities and minimizing electronic systems



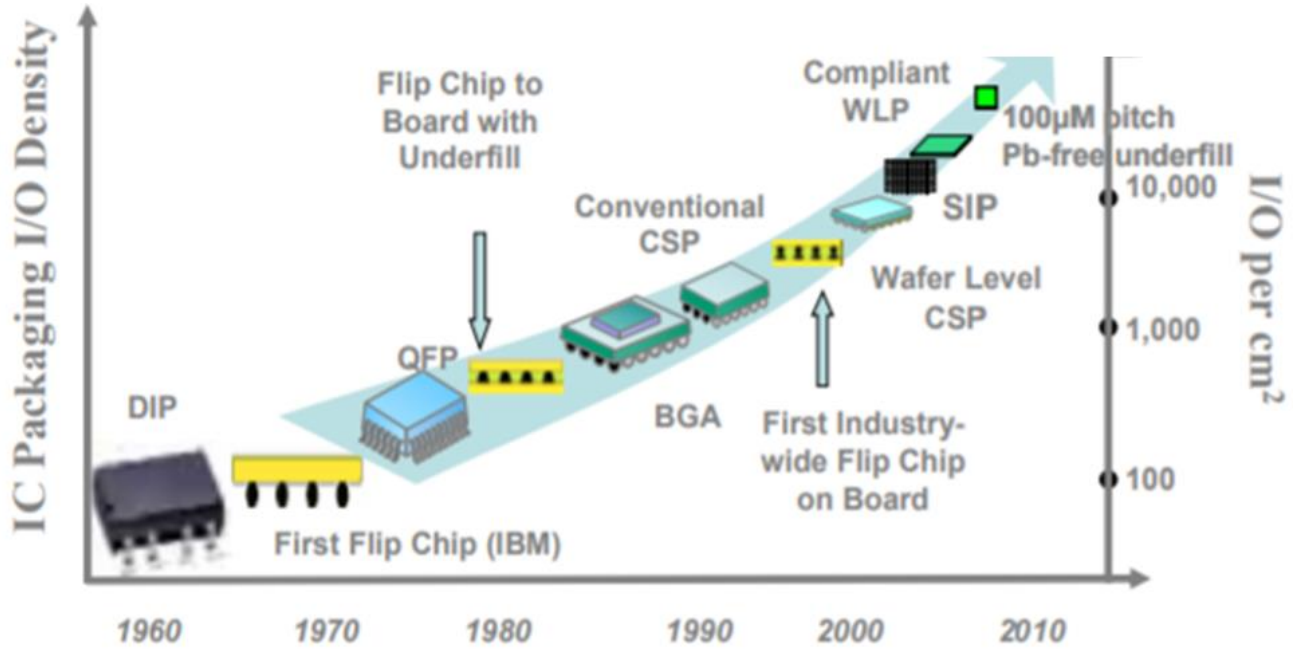


Packaging Considerations

- Electrical
- Thermal
- Mechanical
- Reliability
- Manufacturability
- Testability / Characterization
- Size
- Weight
- Environmental/safety
- Cost
- …

Electrical

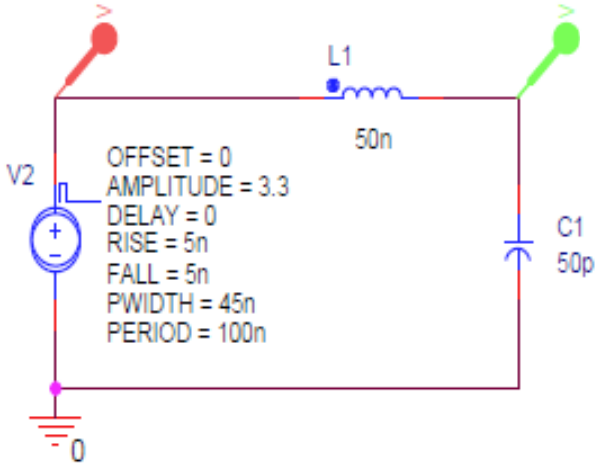
- Objectives
  - Signal distribution & integrity
  - Power distribution & integrity
- Industry trends
  - Increasing switching speeds
  - Decreasing noise margins
  - Increasing I/O density
- Critical components
  - Interconnects
  - Terminals/leads



Electrical

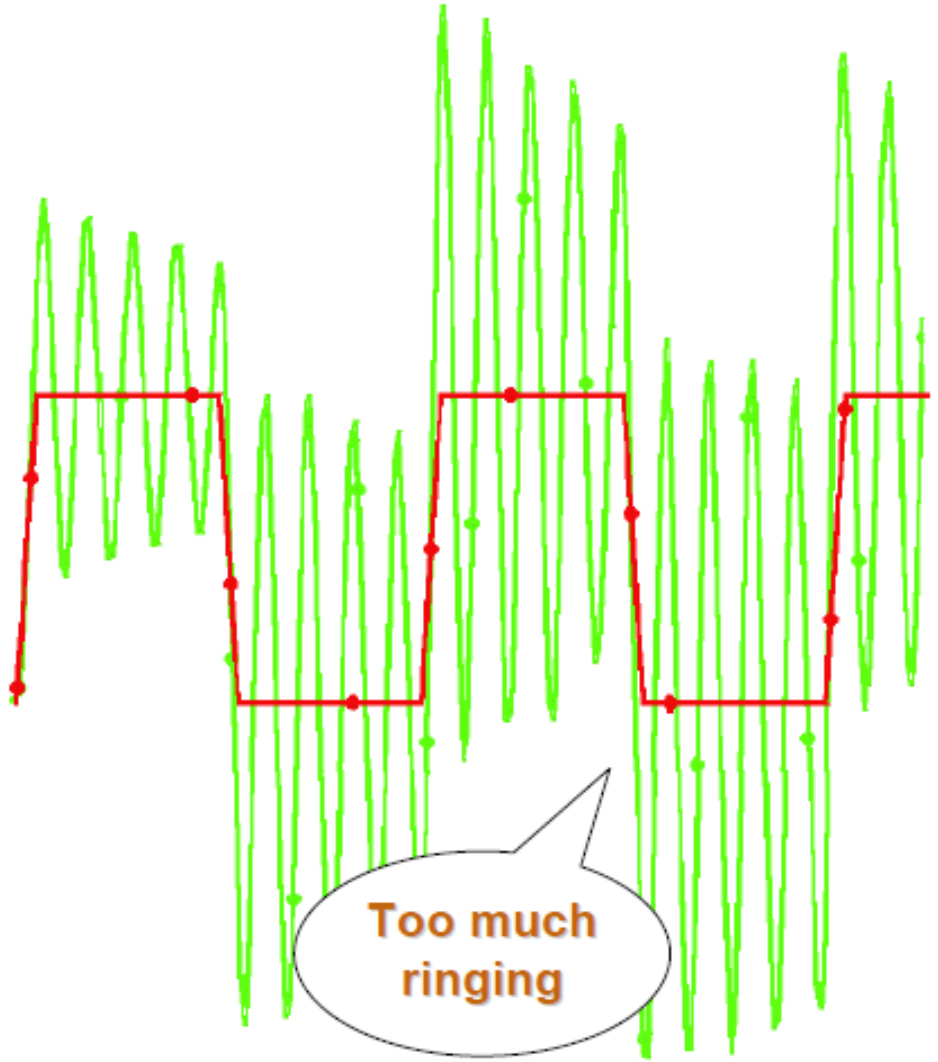
- Challenges
  - Parasitic capacitance, inductance, and resistance
    - Delays, slow speed, distortion, noise, voltage drop, reflection
  - Dielectric loss
  - Electrical insulation
- Solutions
  - Short signal lengths
  - Separated signal and power
  - High electrical conductivity
  - Low dielectric constant
- Consequences
  - Increased heat flux
  - Increased thermal resistance

Impact of Parasitic Inductance and Capacitance

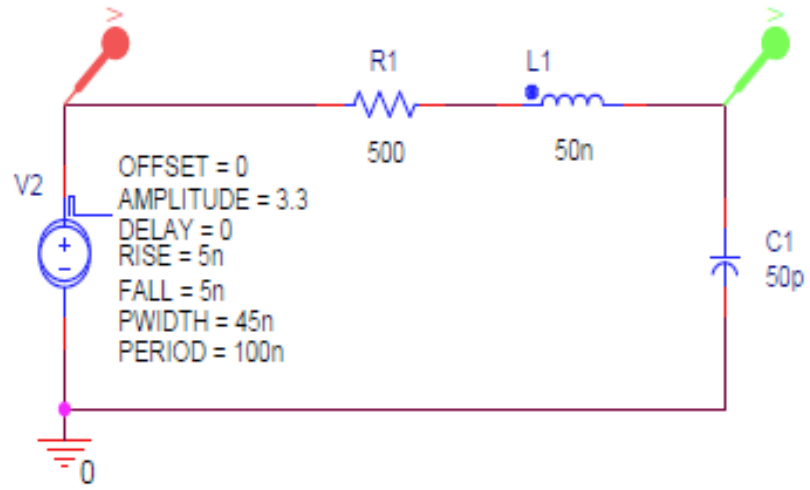


10 MHz square signal with 5 ns fall and rise times

Pin inductance 50 nH, parasitic capacitance 50 pF



Impact of Parasitic Resistance



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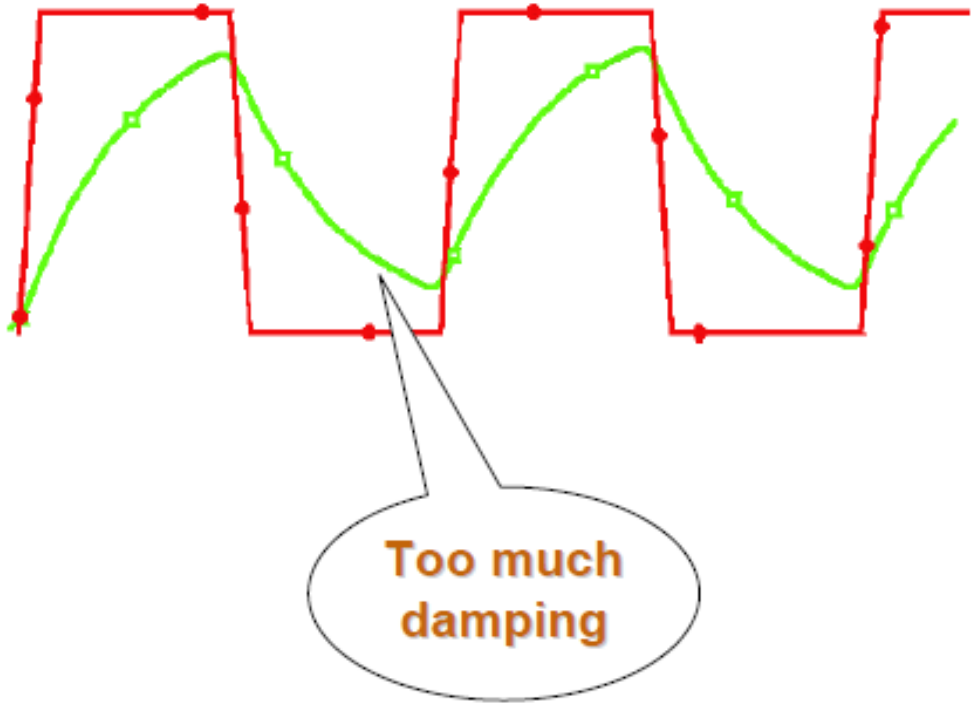
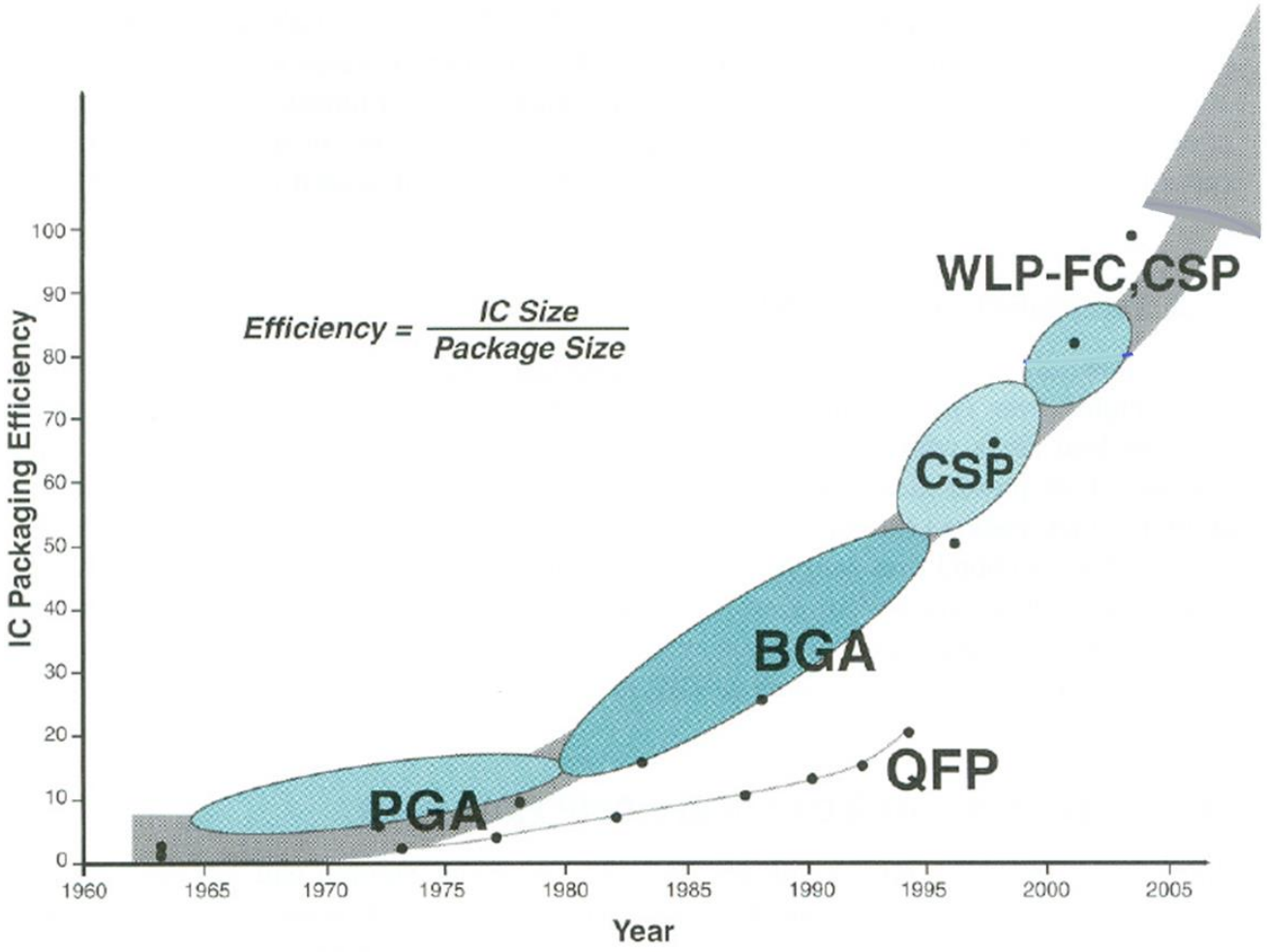


Thermal

- Objective
  - Dissipate heat to keep the chip temperature below the maximum
- Industry trends
  - Decreasing size
  - Increasing power
- Critical components
  - Die attach
  - Substrate
  - Molding



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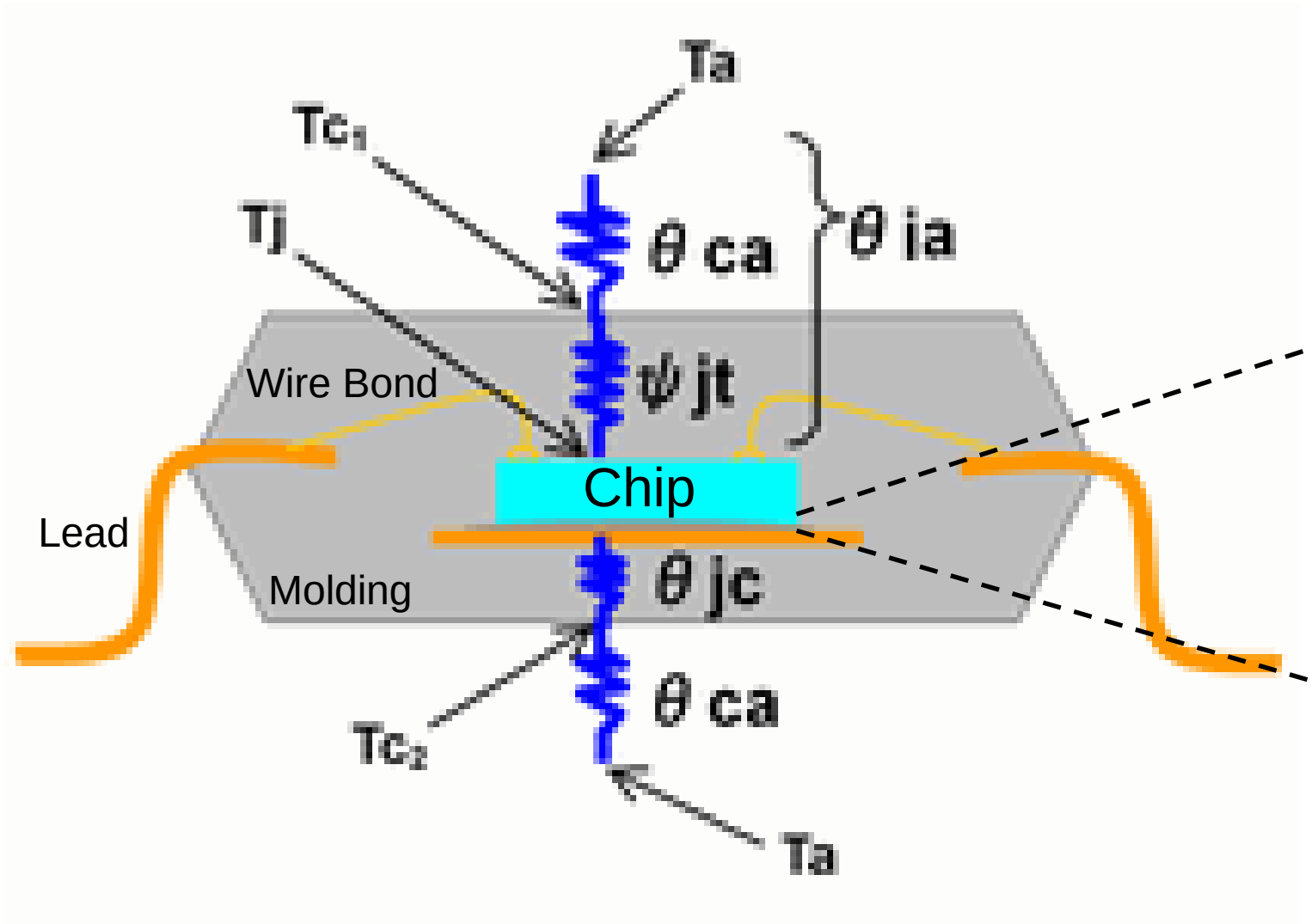
Thermal

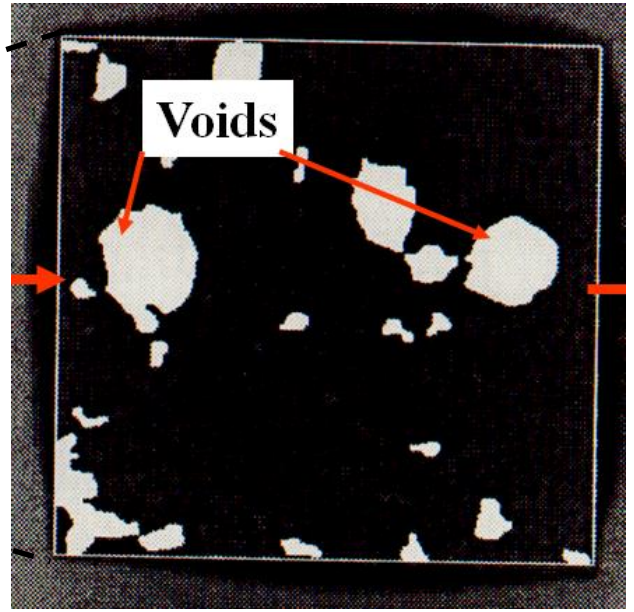
- Challenges
  - Thermal resistance
  - Heat flux
  - Heat spreading
  - Thermal coupling
- Solutions
  - Low defects (e.g., voids)
  - High thermal conductivity materials
  - Increase spacing between chips
- Consequences
  - Higher cost
  - Higher dielectric constant
  - Increased size
  - Reduced speed

Thermal Resistances

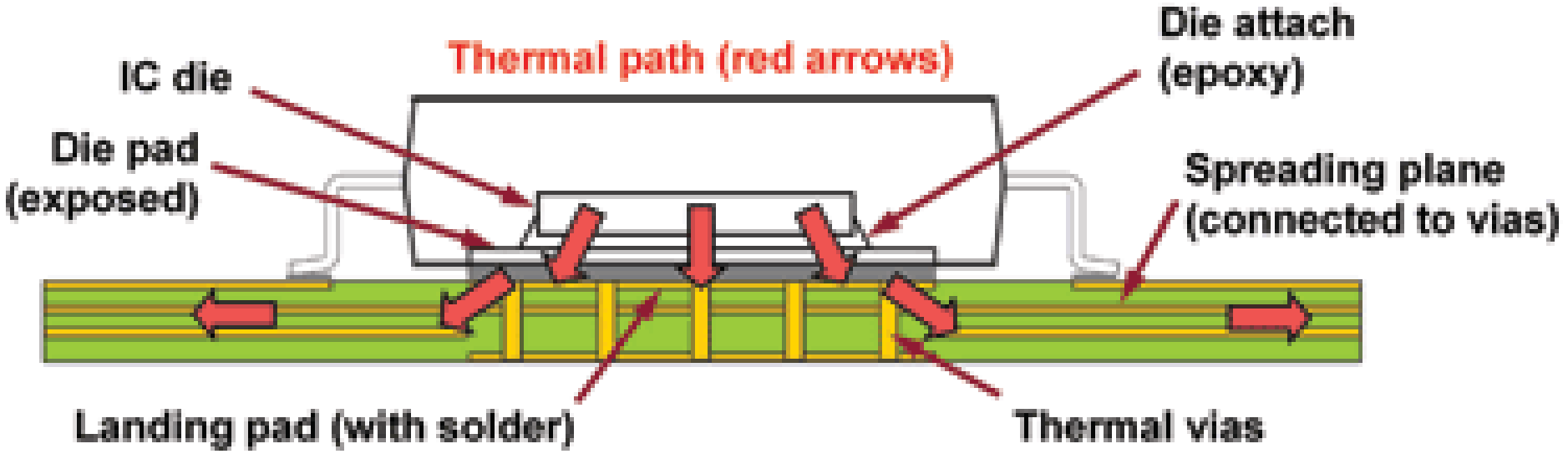
θ = thermal resistance (R_{th})
j = junction (chip temperature)
c = case of package
a = ambient

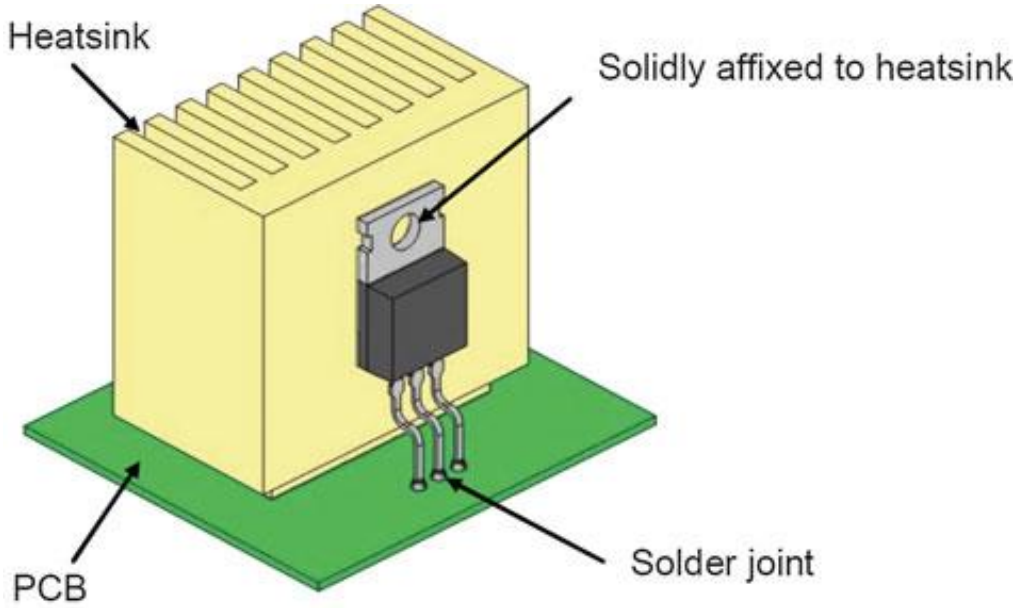


Chip Attach

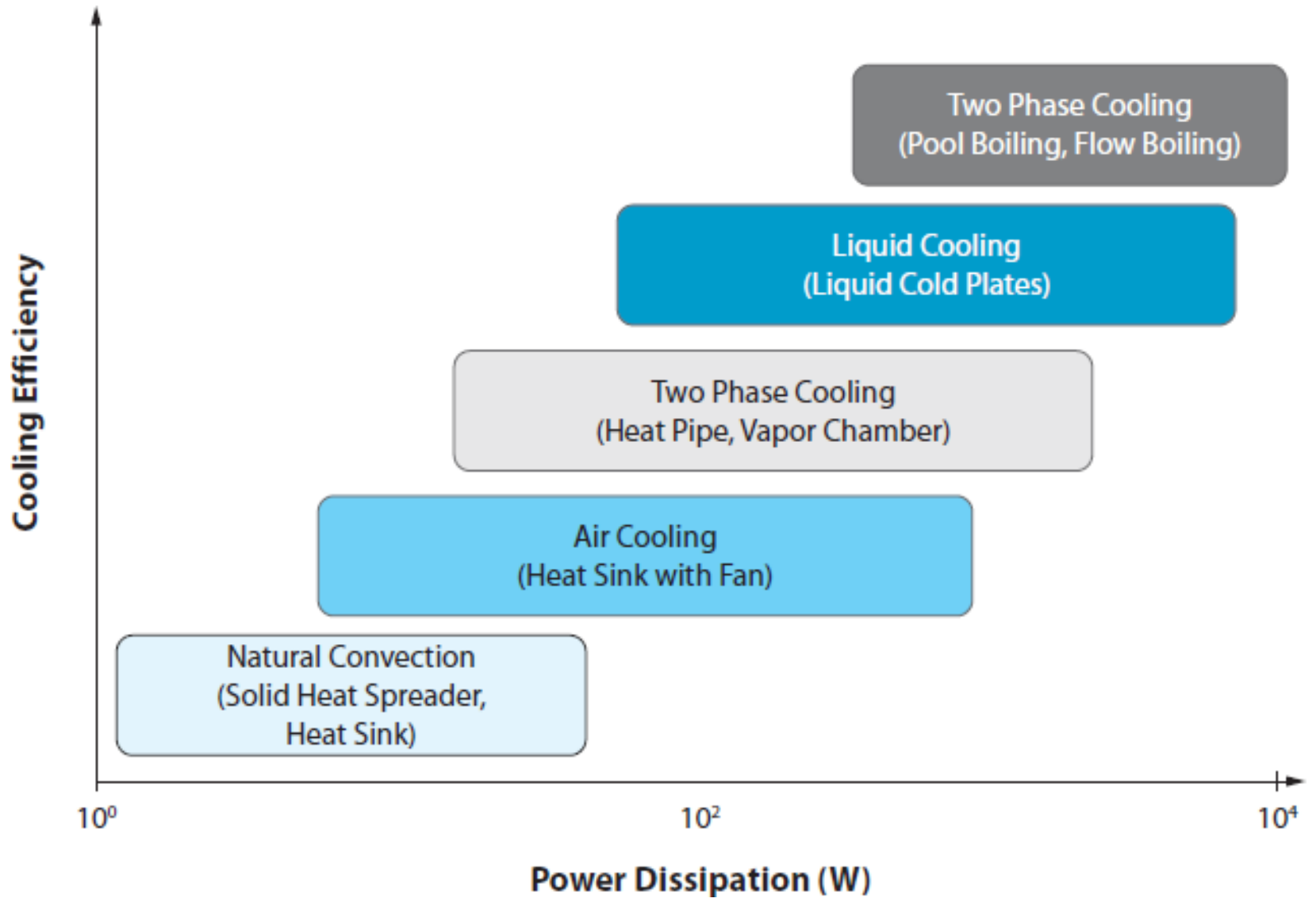


Thermal Management





Thermal Management

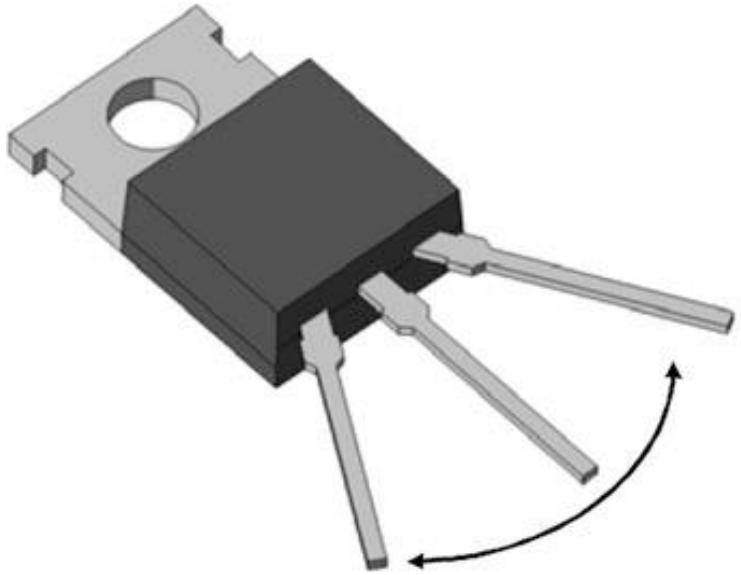


Mechanical

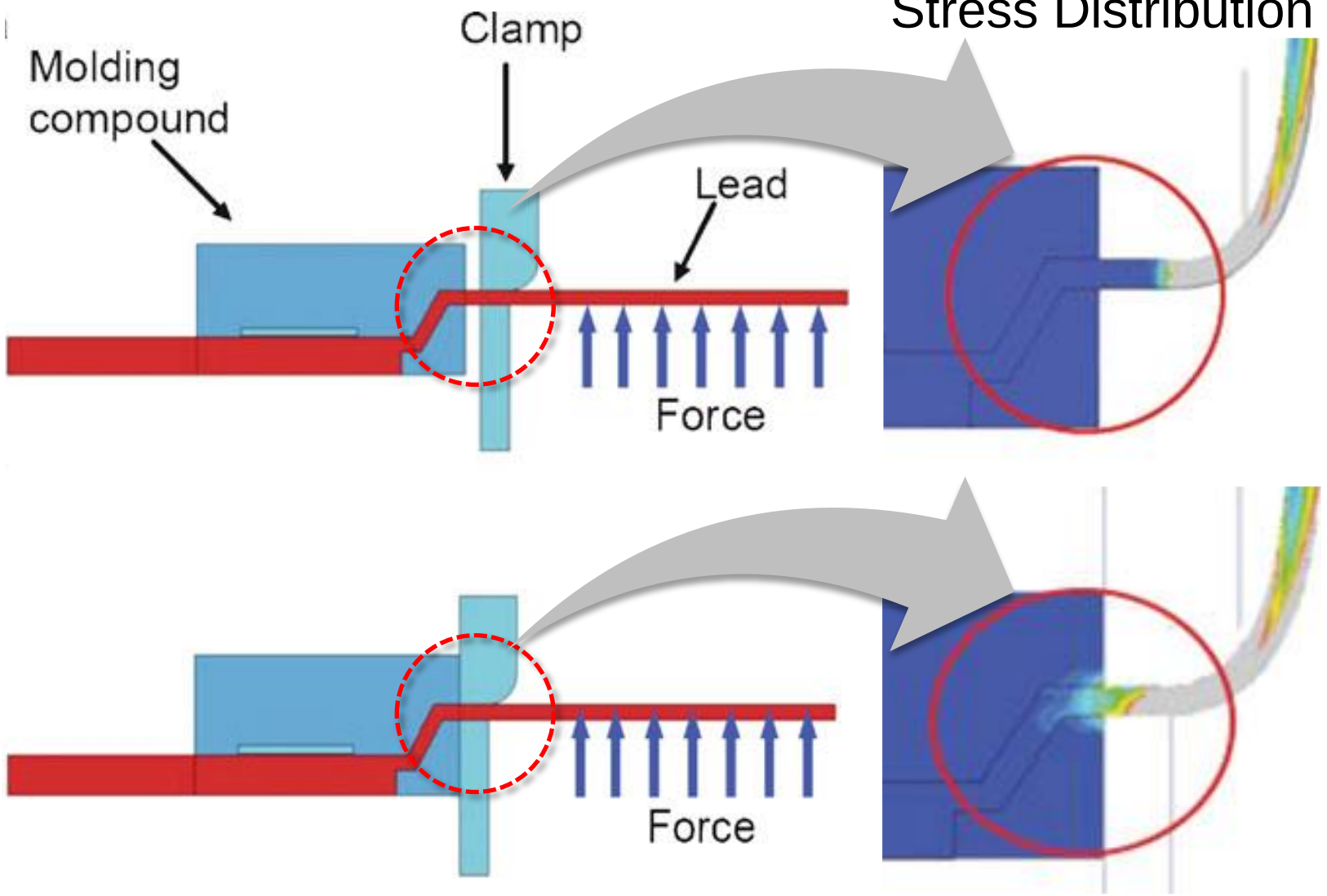
- Objectives
  - Protection
  - Support
  - Durability
- Industry trends
  - Harsh environment
  - Increased density
- Critical components
  - Substrate
  - Molding
  - Terminals
- Challenges
  - Vibration
  - Bending
  - Fracture
- Solutions
  - Materials
  - Geometry
- Consequences
  - Cost
  - Performance
  - Thermal and electrical performance

Mechanical Stress due to Lead Bending

TO-220

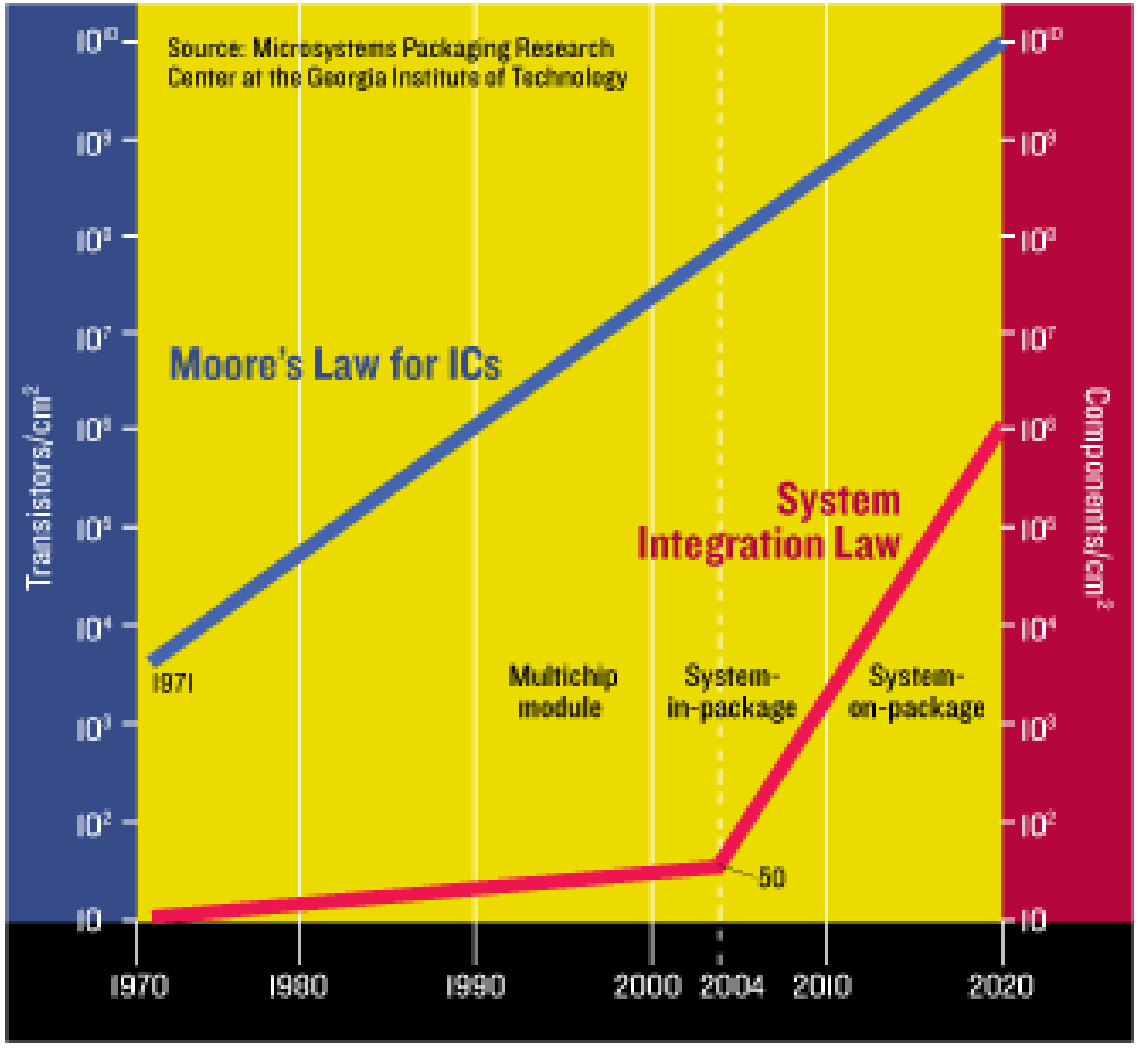


Leads should NEVER be bent laterally



Reliability

- Objective
  - Sufficient product lifetime
- Industry trends
  - More components
  - Increased integration
  - Harsh environment
  - Longer lifetime
- Critical components
  - All (chip attach, substrate, interconnect, molding, terminals)

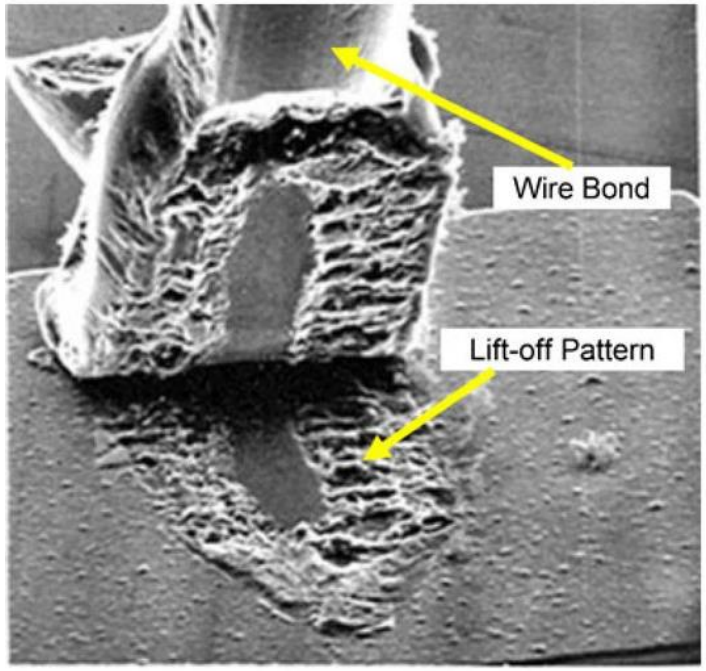


"Moore's Law Meets It's Match" – Tummala

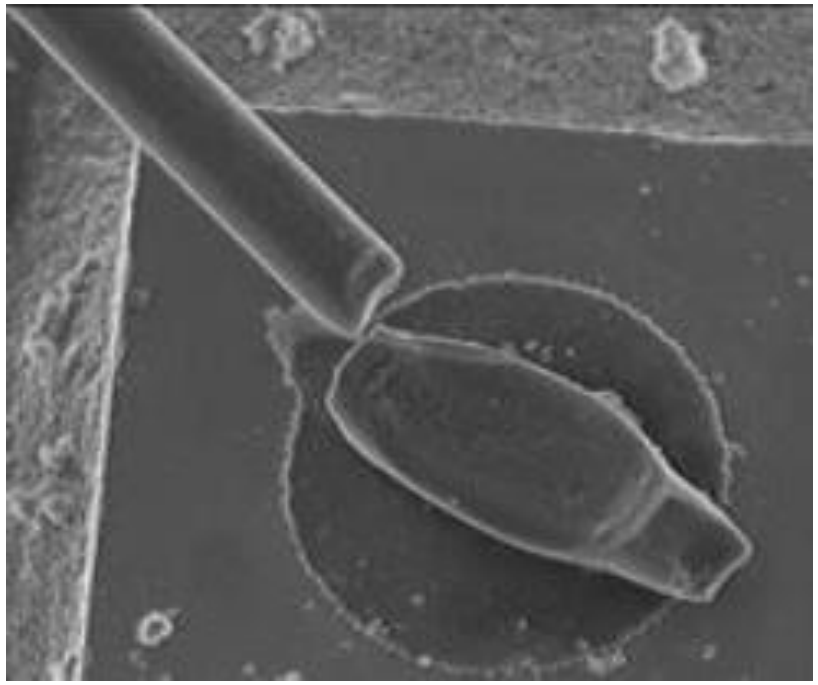
Reliability

- Challenges
  - Integration of different materials
    - Coefficient of thermal expansion (CTE)
    - Elastic modulus
  - High temperature
  - Temperature cycles
  - Humidity
- Solutions
  - Design for reliability
  - CTE matching
  - Increase cooling
  - Accelerated life testing
- Consequences
  - Lower performance
  - Increased cost
  - Longer design cycle

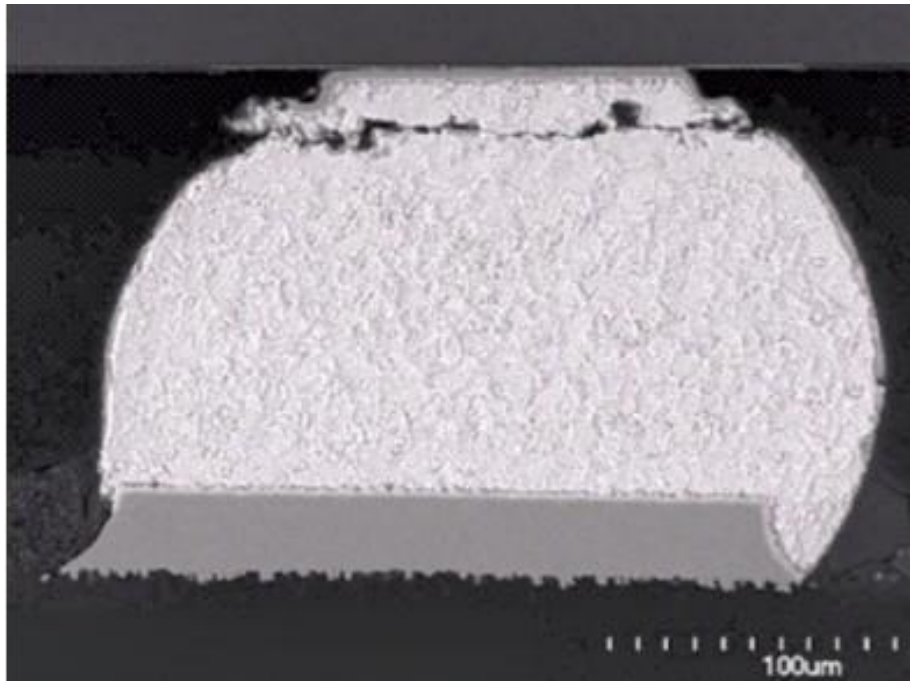
Interconnect Failures



Wire Bond
→ Lift-Off



Wire Bond
→ Heel Crack



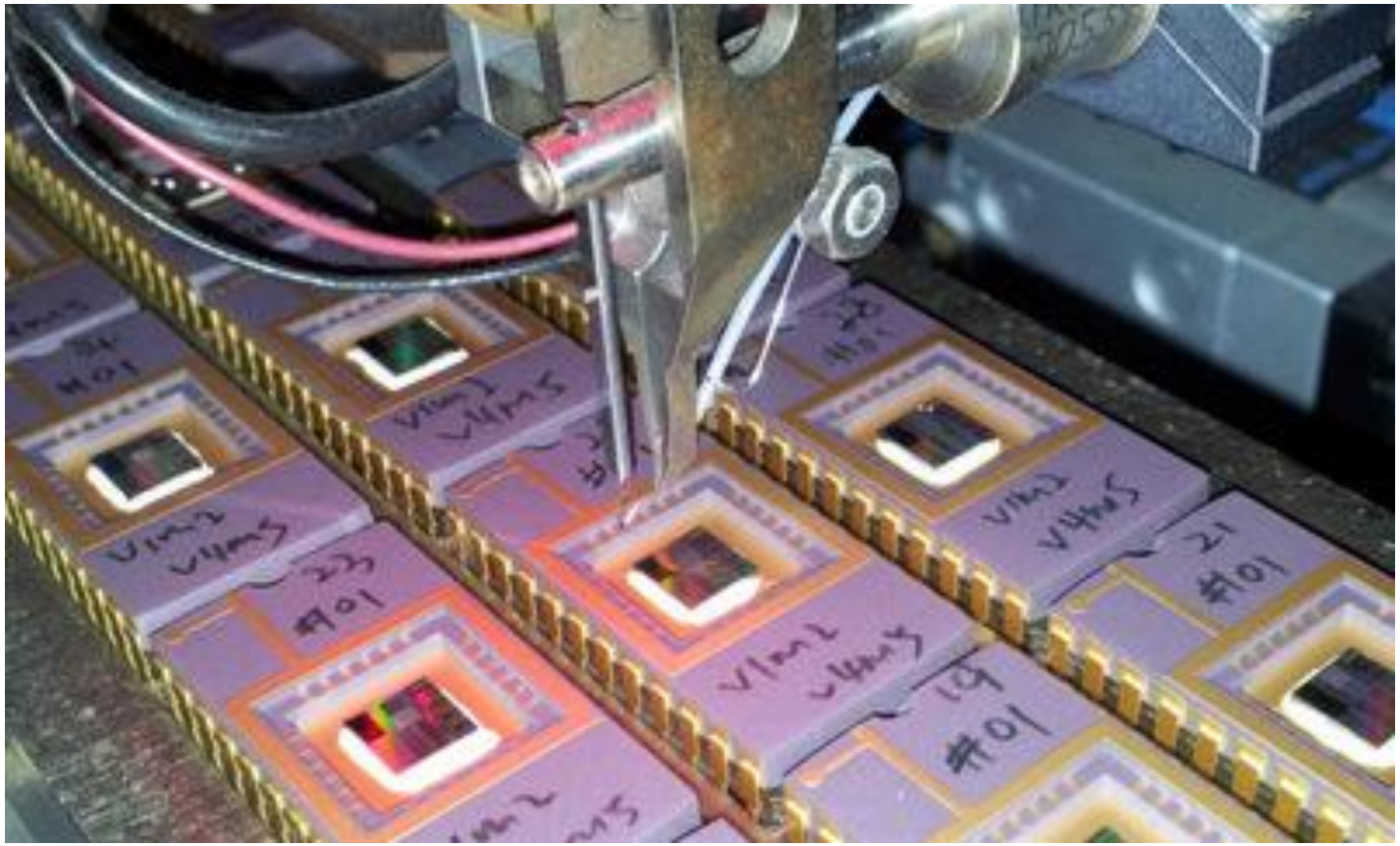
Solder Ball
→ Crack

Thermomechanical stress → degradation → increased electrical resistance
→ thermal stress → open circuit

Manufacturability

- Objectives
  - Low cost
    - High yield and throughput
  - High volume
- Industry trends
  - Cheaper
  - Faster design cycle times
  - Short life spans
- Critical components
  - All
- Challenges
  - Process control
  - Automation
  - Yield
  - Cycle time
  - Rework
- Solutions
  - Design for manufacturability
  - Statistical process control

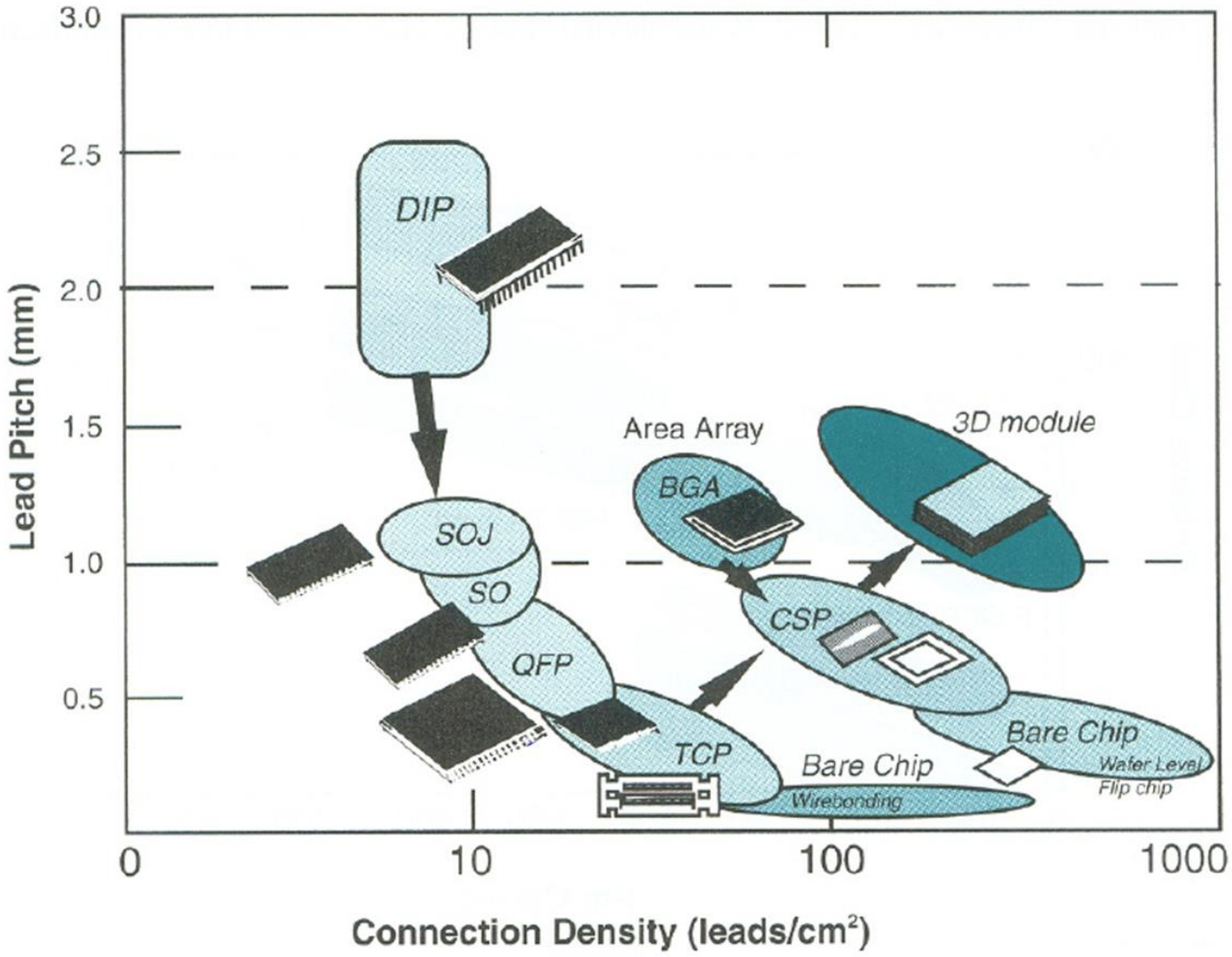
Wire Bonding



- One wire bond at a time
- Spacing between bonds limited by size of tool
- Cheap, lots of supporting infrastructure

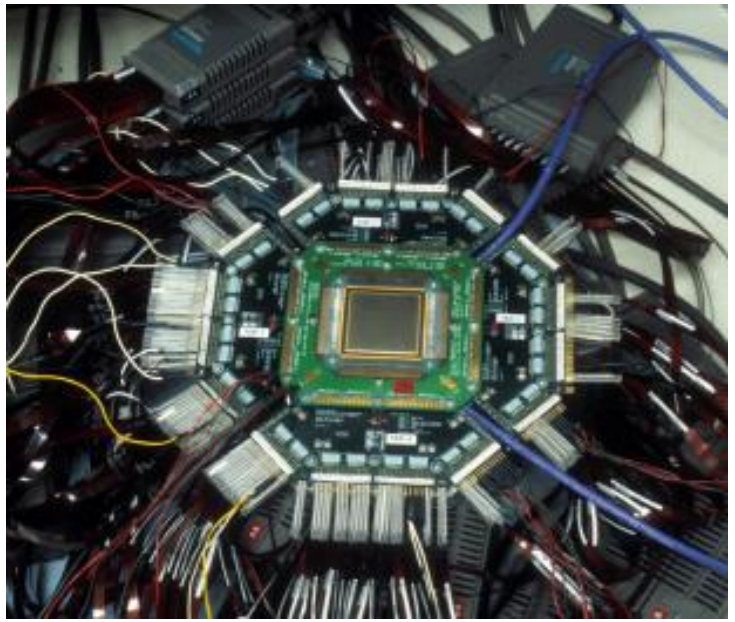
Testability

- Objectives
  - Eliminate defective parts
  - Verify manufacturing
  - Verify new design
  - Predict product performance
- Industry trends
  - Increased I/O density
  - Shorter leads
- Critical components
  - Terminals/leads

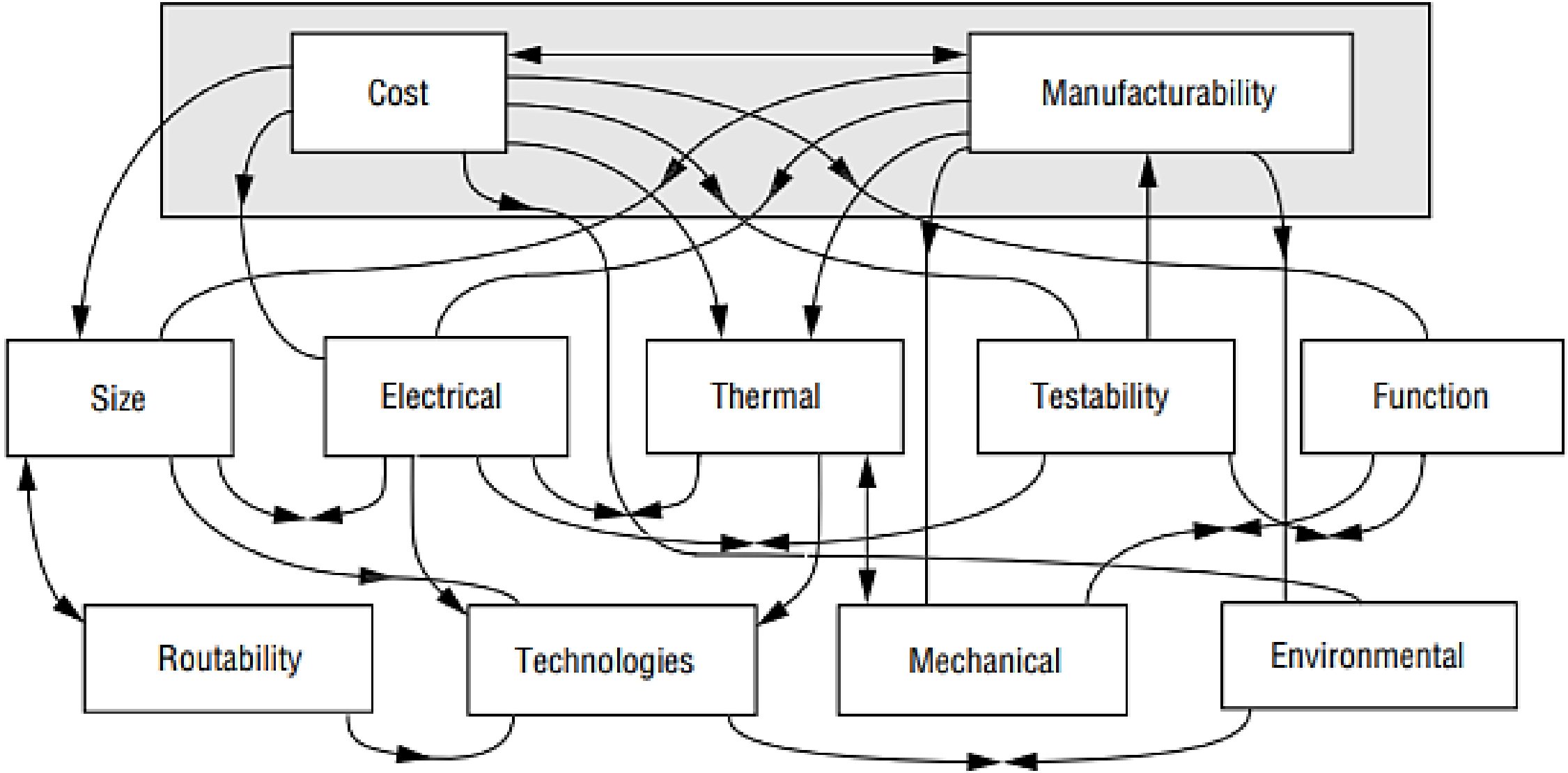


Testability

- Challenges
  - Lead length
  - Lead pitch
  - Visibility
- Solutions
  - Test sockets



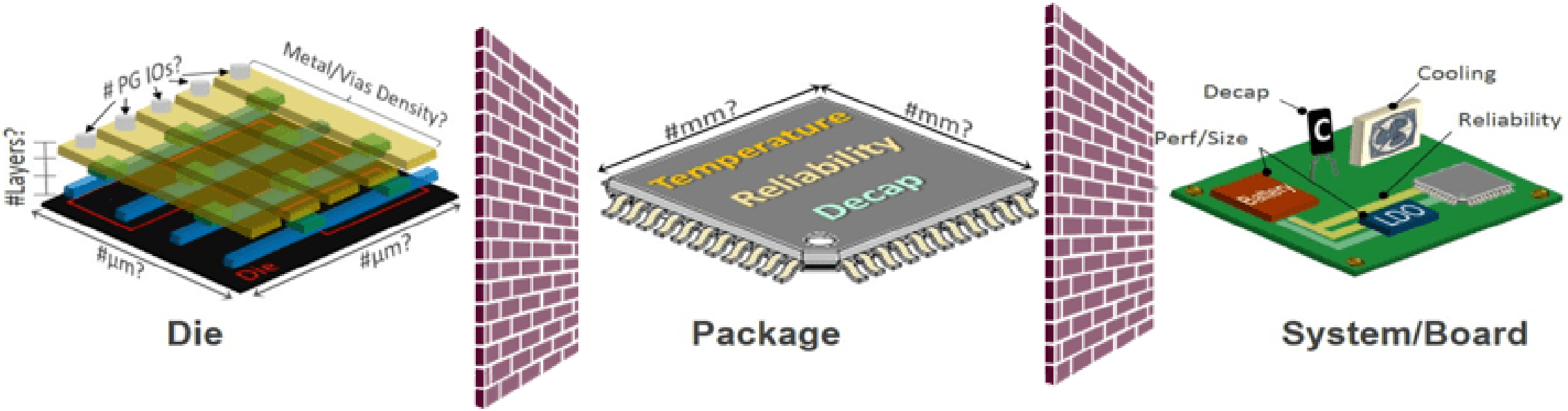
Complex, Interdependent Nature of Packaging



P. Sandborn, M. Vertal, “Analyzing Packaging Trade-Offs During System Design,” IEEE Design & Test of Computers, 1998.

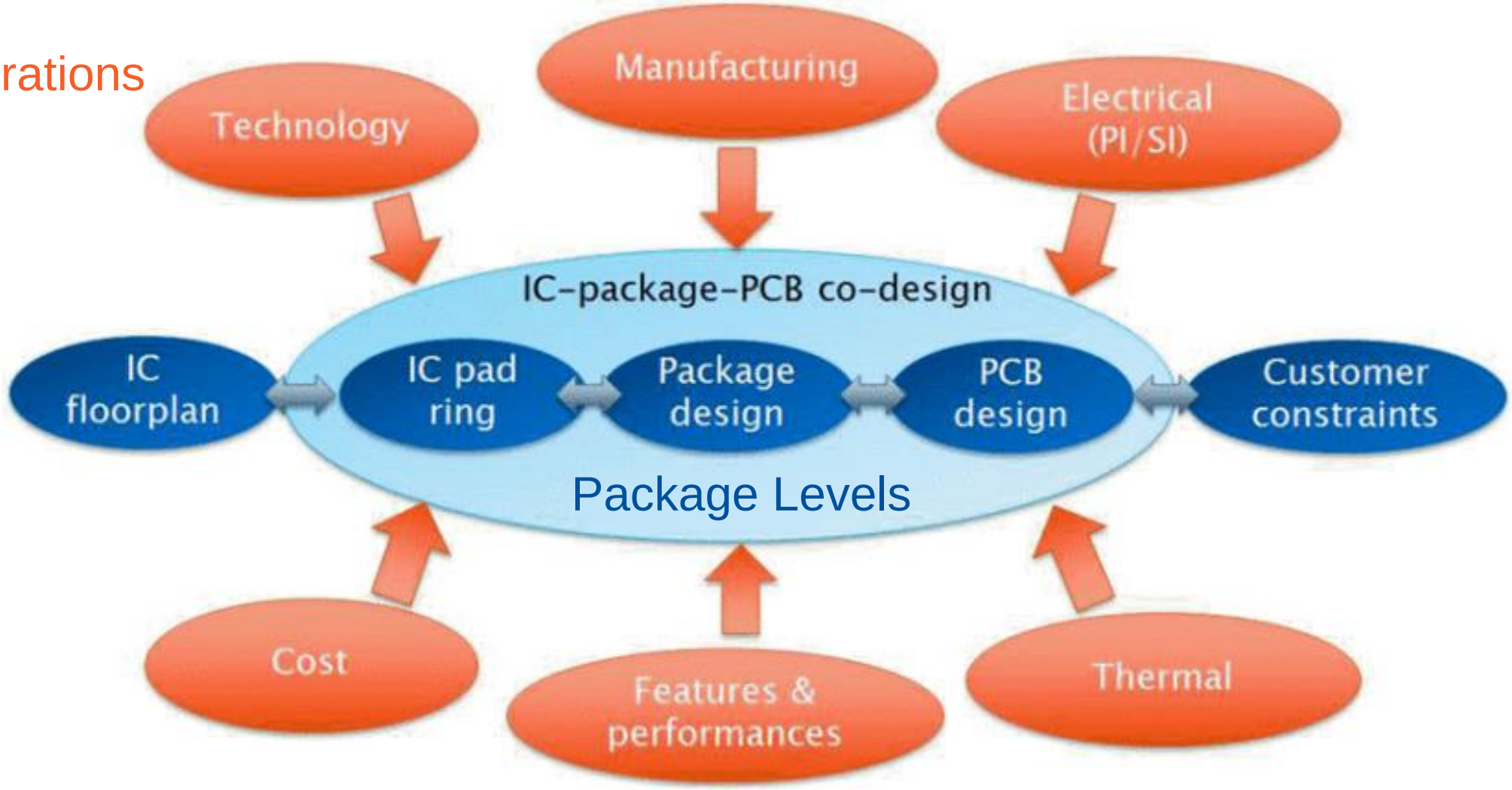
Interaction Between Packaging Levels

Level 0 Level 1 Level 2 …



IC-Package-PCB Co-design

Considerations



Questions

- What are the advantages of an MCM over multiple SCMs?
- What is package size efficiency?
- Which package has a higher I/O density: 1) DIP or 2) BGA?
- Name an electrical packaging challenge.
- Name a thermal packaging challenge.

Course Topics

1. Introduction
2. Electrical → Next class (Chapter 2)
3. Thermal
4. Materials and Processes
5. Characterization and Testing
6. Reliability and Ruggedness
7. Emerging Technologies and Research Topics