Homework #1

Due February 10th, 2025 by 11:59pm

Show all of your work to receive credit. Your solutions should be neat and easy to read and follow. Highlight, underline, or put a box around the final answers. Submit your solutions through the Canvas Assignments page. No late homework will be accepted, unless approved by the instructor prior to the due date. Discussion of the course material with fellow students and the instructor is encouraged, but the homework solutions must be your individual work. You are not allowed to share any part of your solutions with other students.

The Virginia Tech honor code pledge for assignments is as follows: "I have neither given nor received unauthorized assistance on this assignment." The pledge is to be written out on all graded assignments at the university and signed by the student. The honor pledge represents both an expression of the student's support of the honor code and a commitment to uphold the academic standards at Virginia Tech. Please see the Honor System section of the syllabus on Canvas for details.

1. Gold (Au) wire bonds are commonly used for interconnects in microelectronics packaging. Often, the wire bonds are exposed to high temperatures due to the heat generated by the semiconductor device.
    a. Calculate the DC resistance for an Au wire bond with a diameter of 2 mil and a length of 10 mm at 100°C. The resistivity for Au at room temperature is 2.2e-8 Ω·m. The temperature coefficient of resistance for Au is 3.4e-3 /°C.
    b. In your own words, briefly describe the physical phenomena the cause the resistance to increase with temperature. Cite any references used.

2. Conductors carrying high-frequency signals could experience high AC resistance and thus higher losses.
    a. Calculate the AC resistance for the wire bond described in problem 1 at room temperature and at a frequency of 500 MHz.
    b. In your own words, explain the phenomena that cause the AC resistance to be greater than the DC resistance at high frequency. Cite any references used.
    c. List one change that could be made to the interconnect design/selection to reduce the AC resistance (without changing the frequency).

3. Ribbon bonding is an alternative to wire bonding in high-frequency (microwave and RF) applications. It is also sometimes used for power electronics packages and for EV batteries. Calculate the DC and AC resistances of a gold ribbon with a thickness of 1 mil, width of 10 mils, and length of 10 mm at 500 MHz and room temperature. Check that the necessary conditions are met before using the simplified equation provided in the lectures.

4. For an aluminum (Al) wire bond with a 5-mil diameter, plot the self-inductance (in nH) versus length (in mm, from 2 mm to 20 mm). On the same plot, include the inductance according to the rule of thumb shown in the lectures. Label the axes (include units) and include a legend or labels for the two curves. Use appropriate font sizes so that the axes and legend are easy to read (we should not have to zoom into the document to be able to

read the font). Use software (e.g., MATLAB, Excel, etc.) to plot the curves. Include the equations used for the plots in your submitted assignment and upload the code/file to Canvas. Comment on the comparison between the two methods.

5. Calculate and plot the self-inductance (in nH) versus conductor radius (in mils, from 0.5 mils to 5 mils) for an Al wire bond with a length of 10 mm. On the same plot, include the inductance according to the rule of thumb shown in the lectures. Label the axes (include units) and include a legend or labels for the two curves. Use appropriate font sizes so that the axes and legend are easy to read (we should not have to zoom into the document to be able to read the font). Use software (e.g., MATLAB, Excel, etc.) to plot the curves. Include the equations used in your submitted assignment and upload the code/file to Canvas. Comment on the comparison between the two methods.

6. To decrease the resistance and inductance, and increase the current carrying capacity, wire bonds may be put in parallel (electrically and physically). Consider two electrically paralleled, side-by-side Al wire bonds with 10-mm length, and 5-mil diameter each.
    a. Plot the total inductance (in nH) for the two parallel wire bonds versus the spacing between the two wire bonds (in mm, from 1 mm to 10 mm). Also plot the total inductance when the mutual inductance between the two wires is neglected. Plot both curves on the same chart. Label the axes (include units), and include a legend or labels for the two curves. Use software (e.g., MATLAB, Excel, etc.) to plot the curves. Include the equations used in your submitted assignment and upload the code/file to Canvas.
    b. Comment on the influence of the mutual inductance on the total inductance of the two parallel wires.

7. Plot the total inductance (in nH) for the following three cases versus spacing (in mm, from 1 mm to 10 mm) between the conductors: a) two side-by-side wires (one for the signal and one for the return/ground), b) a signal-carrying wire over a ground plane, and c) two parallel planes (one for the signal and one for the ground).
    a. Plot all three curves on one plot. Assume all conductors (wires and planes) are made of Al, and are 10 mm long. Assume the wires each have a diameter of 2 mils, and the planes each have a width of 20 mm. Label the axes (include units), and the three curves. Use software (e.g., MATLAB, Excel, etc.) to plot the curves. Include the equations used in your submitted assignment and upload the code/file to Canvas. Use the equations provided in the lecture slides; do not use the equations in the textbook, as there is an error.
    b. Which arrangement has the lowest total inductance? Why does this arrangement have the lowest total inductance?

8. Consider the DIP package shown in Fig. 1.
    a. Draw the equivalent circuit schematic for the two adjacent wire bonds and leads highlighted in Fig. 1, where one is the signal path and the other is the return (ground) path. Represent the semiconductor die as a capacitive load, and the input as a voltage source. Consider parasitic resistances, self-inductances, and mutual inductances (with polarities/signs). Assume the rise time is sufficiently slow such

that transmission line effects can be neglected. Label all elements included in the circuit such that it is clear which elements in the equivalent circuit correspond to each component in Fig. 1.

b. Using the equivalent circuit, write the equation for the total loop inductance.

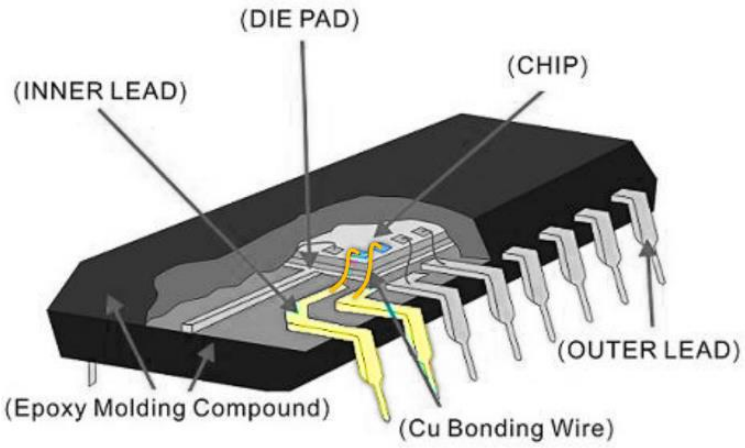

Figure 1: DIP package for problem 9.