



Lectures 6-8

Electrical Design

Ansys Q3D Extractor & LTspice

February 6, 2025

Package Equivalent Circuit

Physical Package Structure

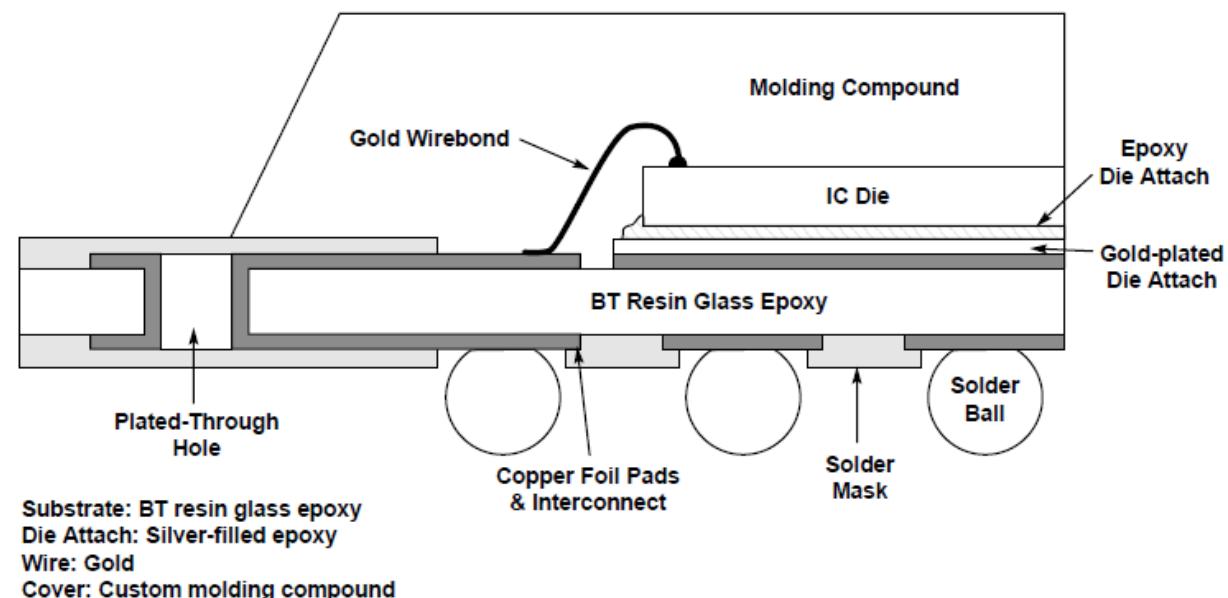


Figure 7-3. OMPAC Ball Grid Array From Motorola

→ Equivalent Electrical Circuit

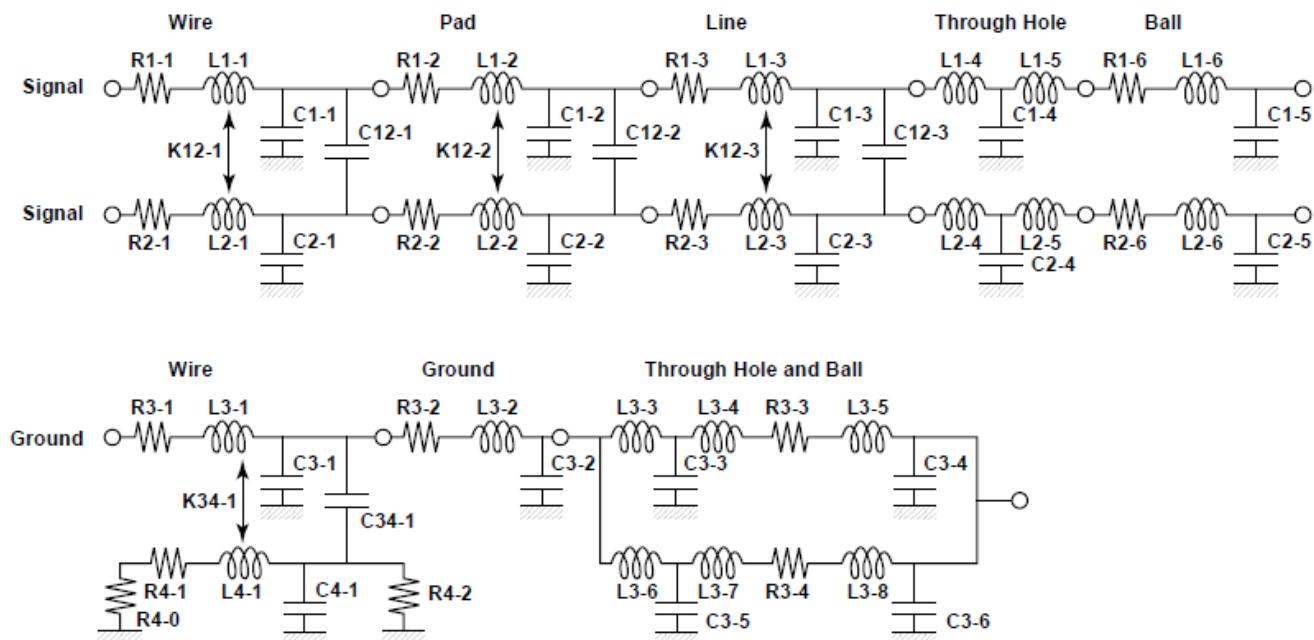
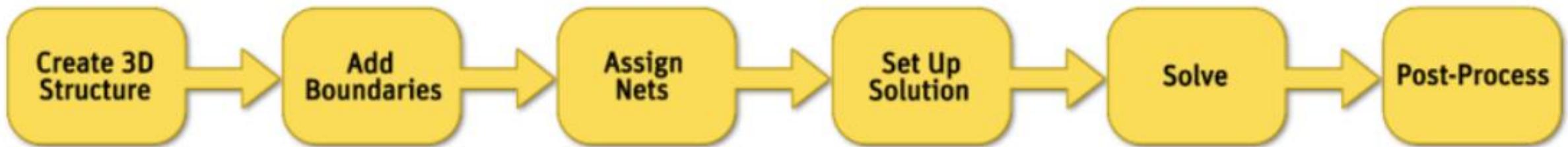


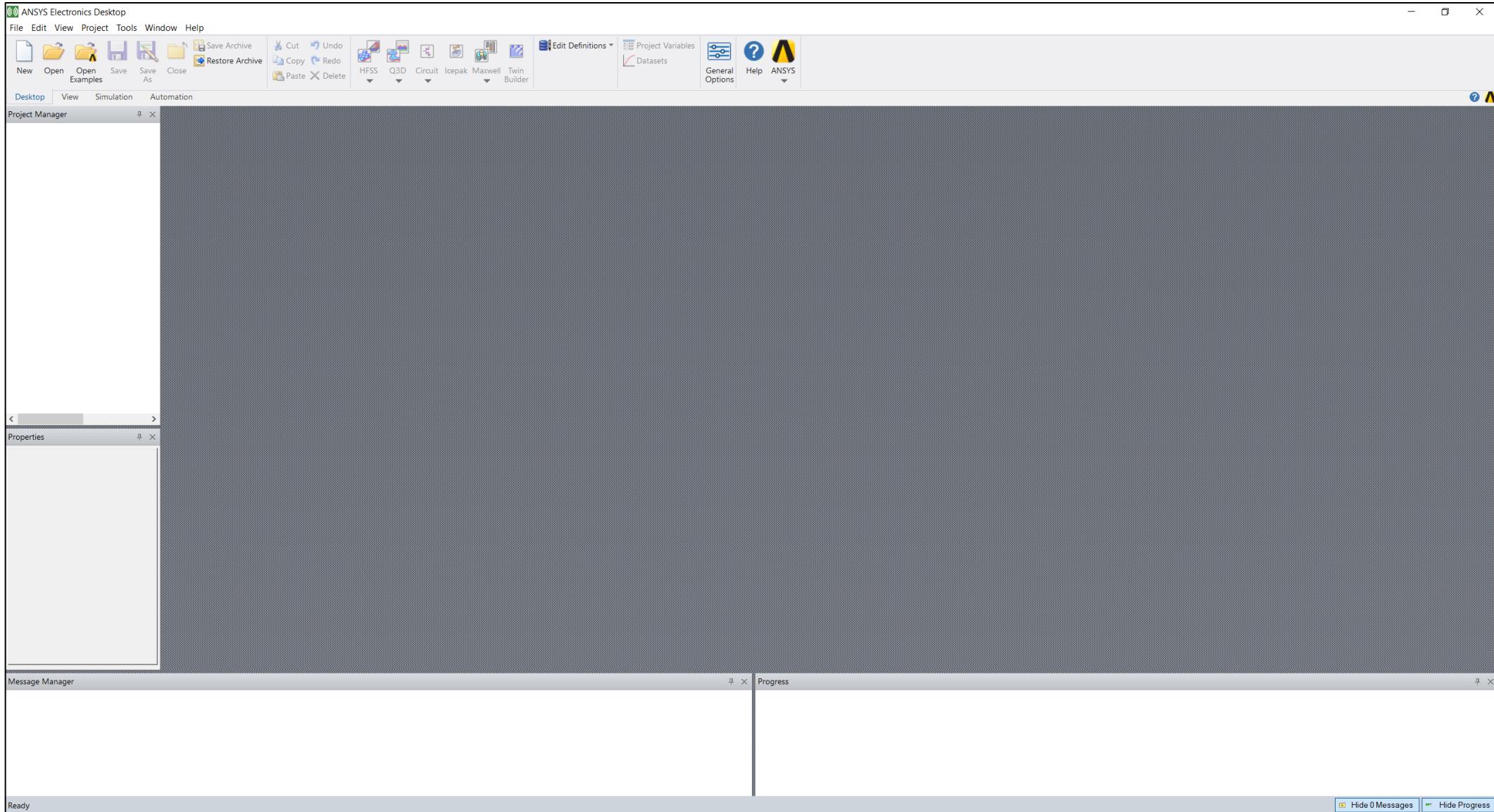
Figure 7-4. The Equivalent Schematic for a BGA Package for Adjacent Signal to Signal Lines and for Ground Lines

ANSYS Q3D Process Flow

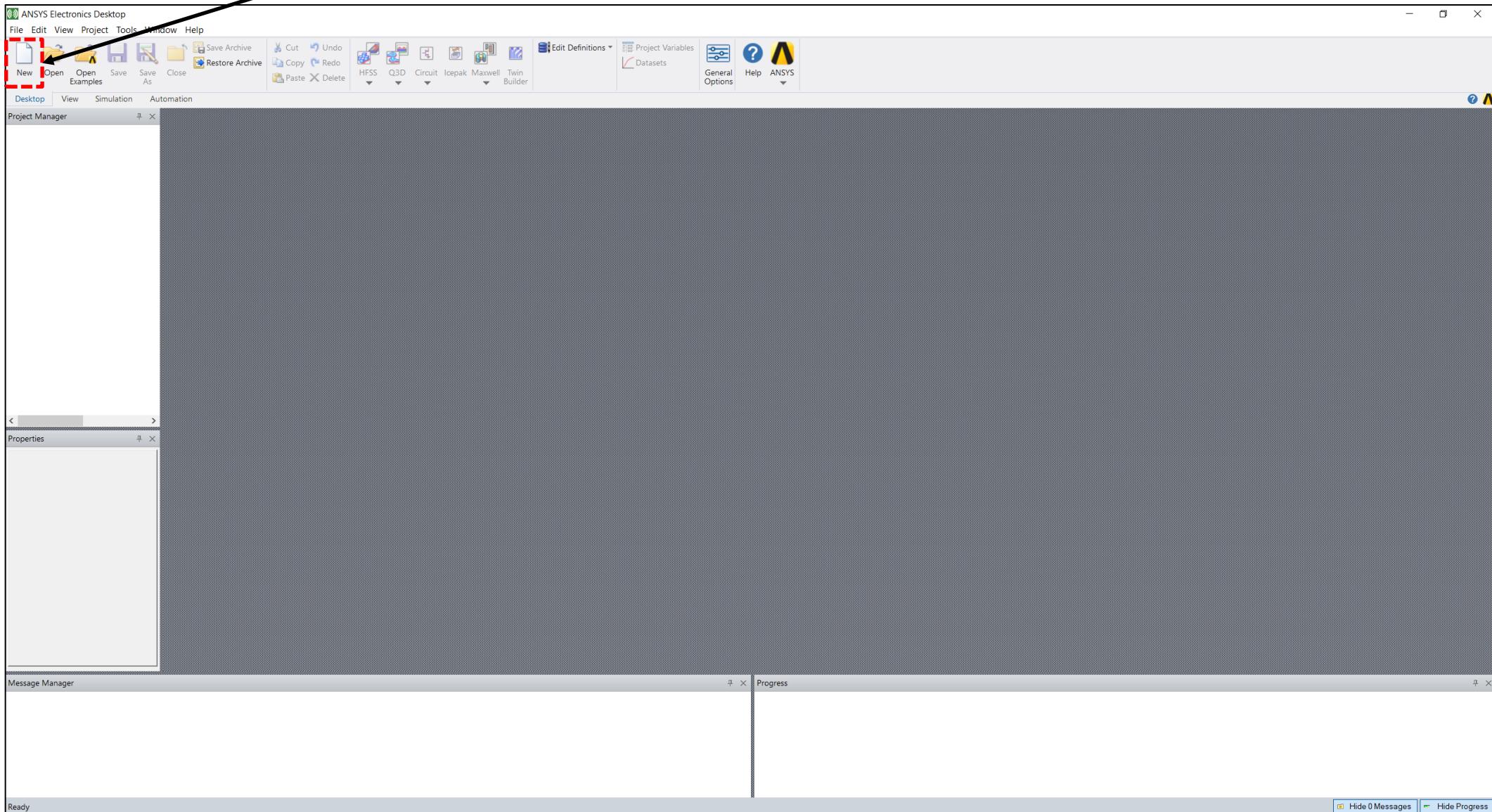




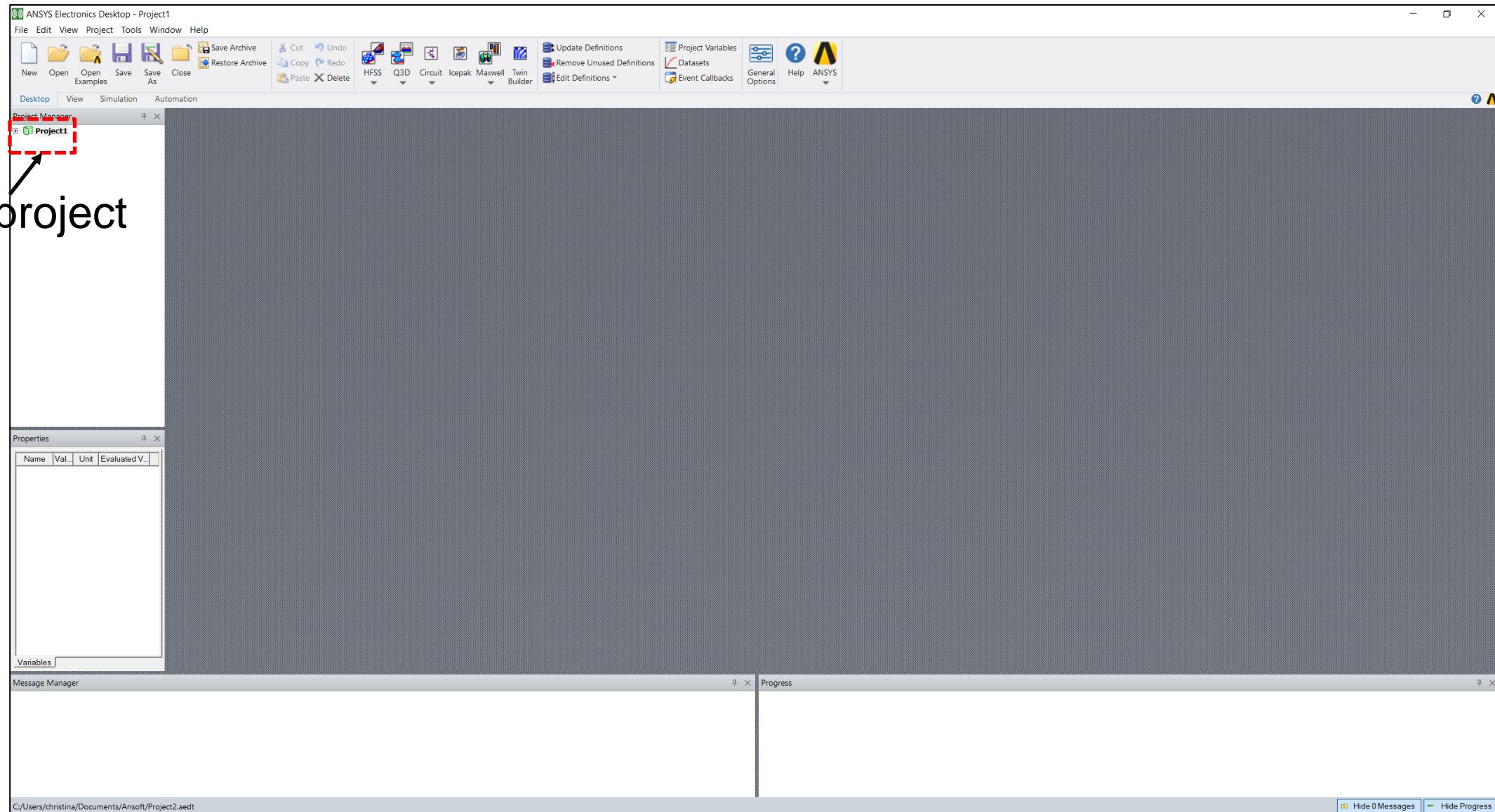
1: Open ANSYS Electronics Desktop



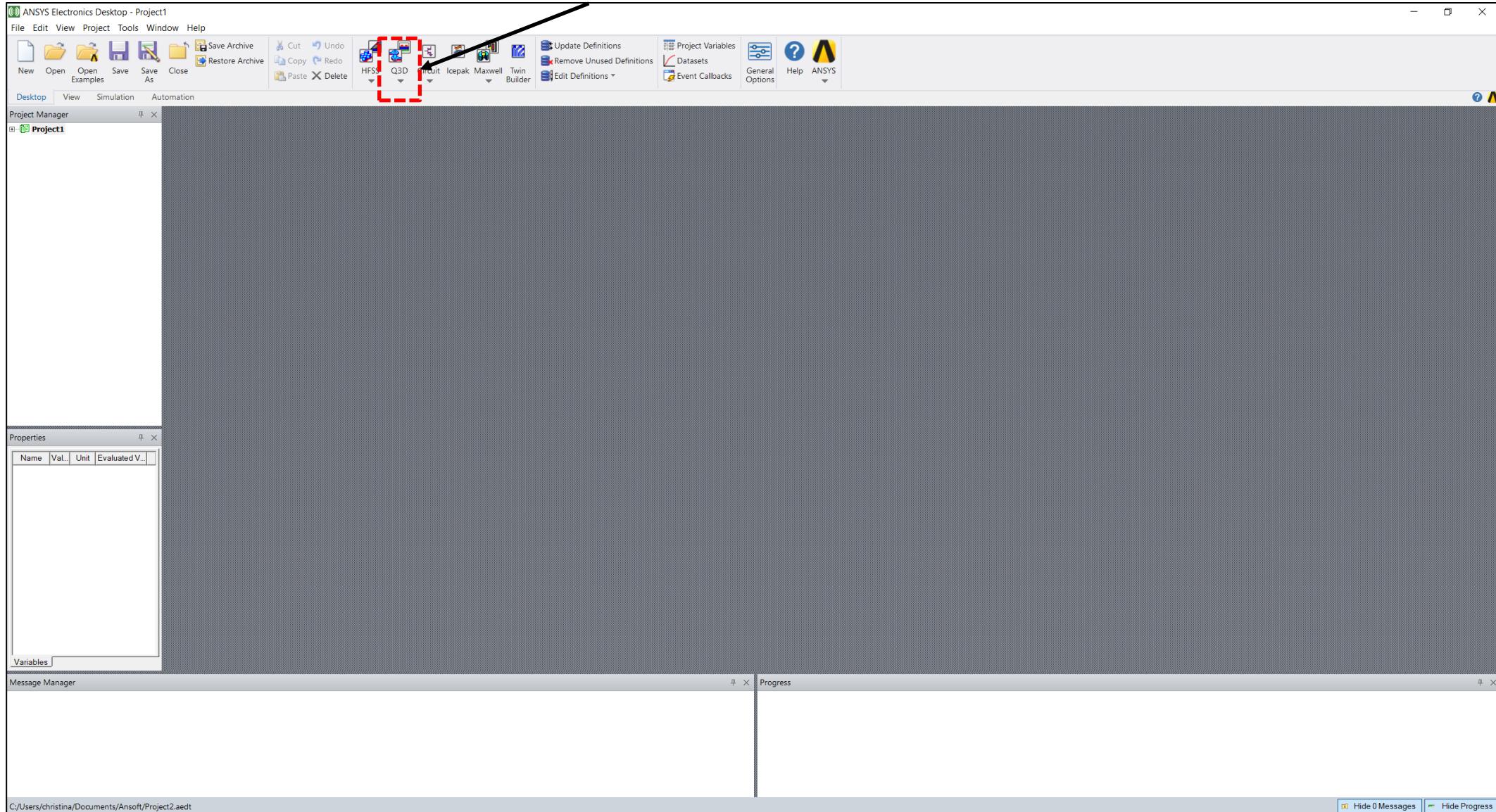
2: Create a New Project



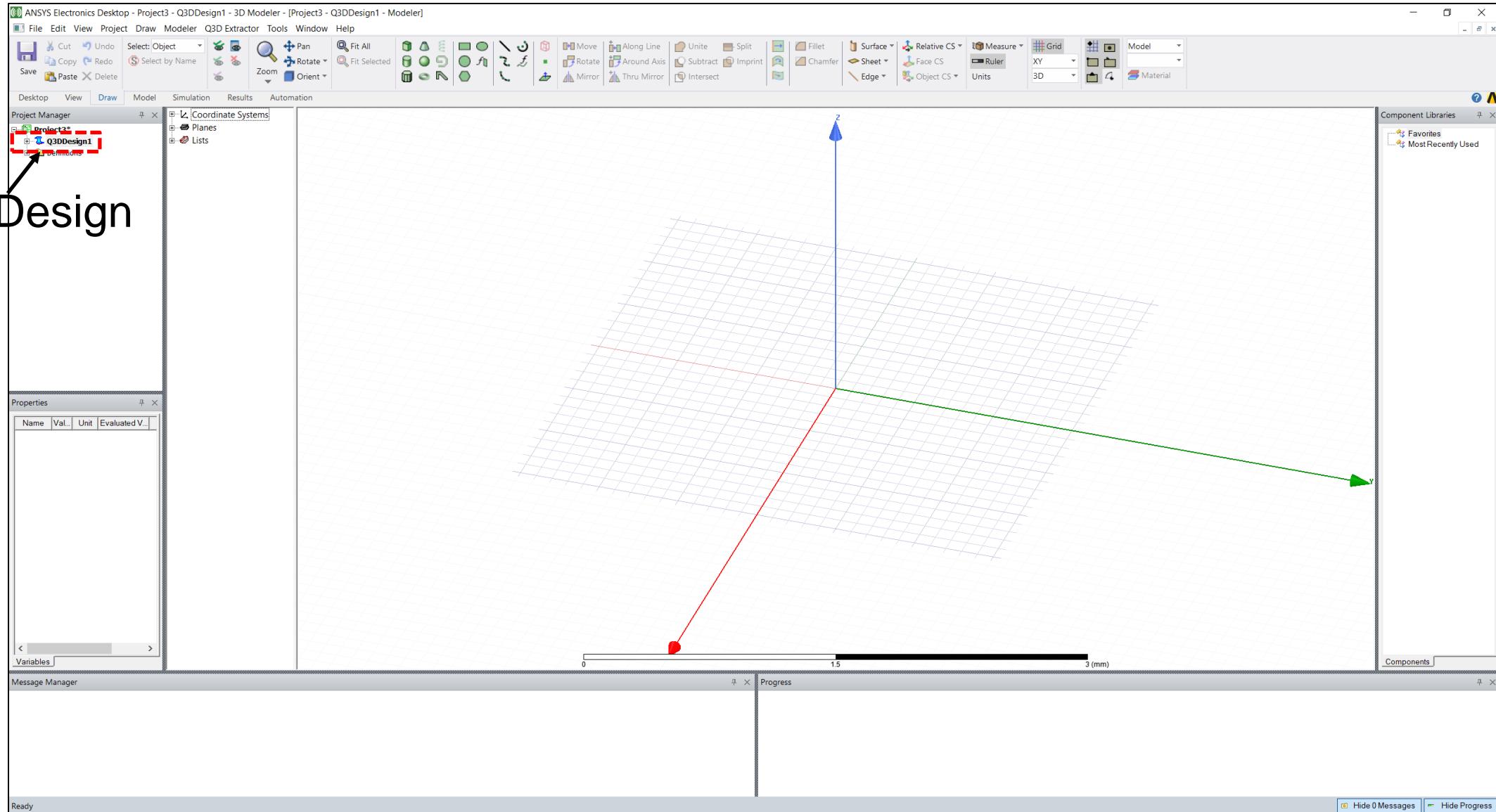
2: Create a New Project



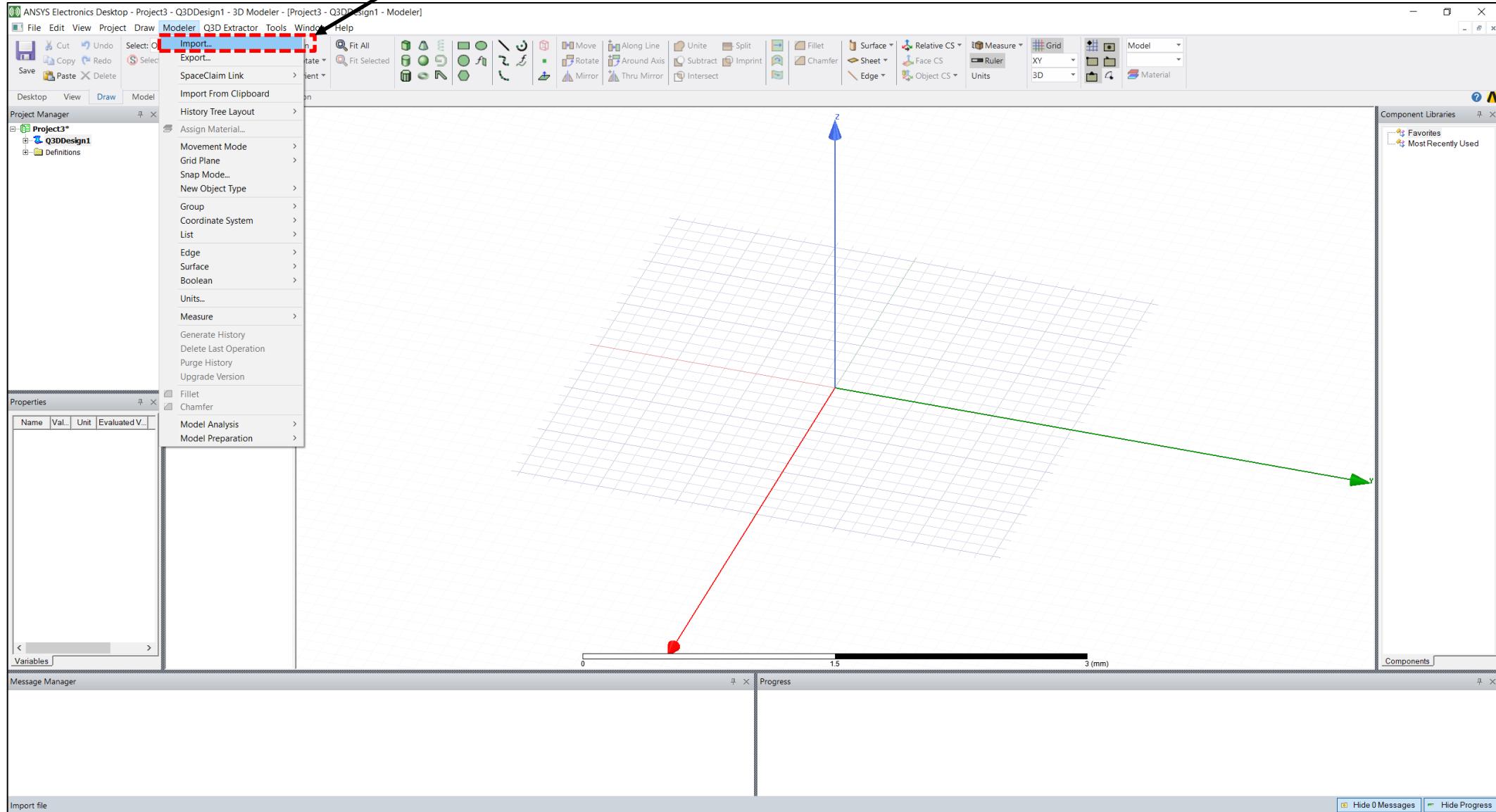
3: Add Q3D Design to the Project



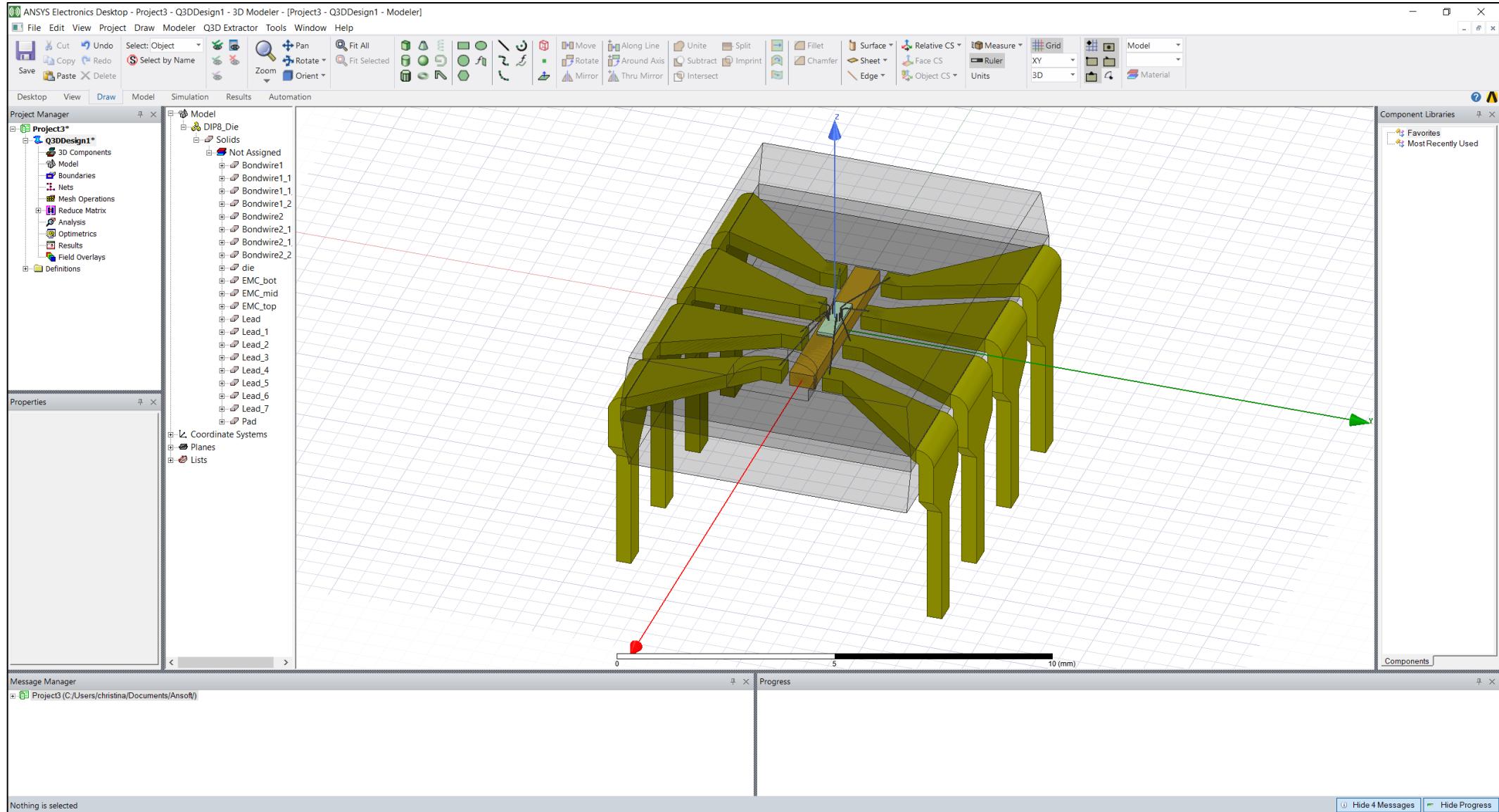
3: Add an Q3D Design to the Project



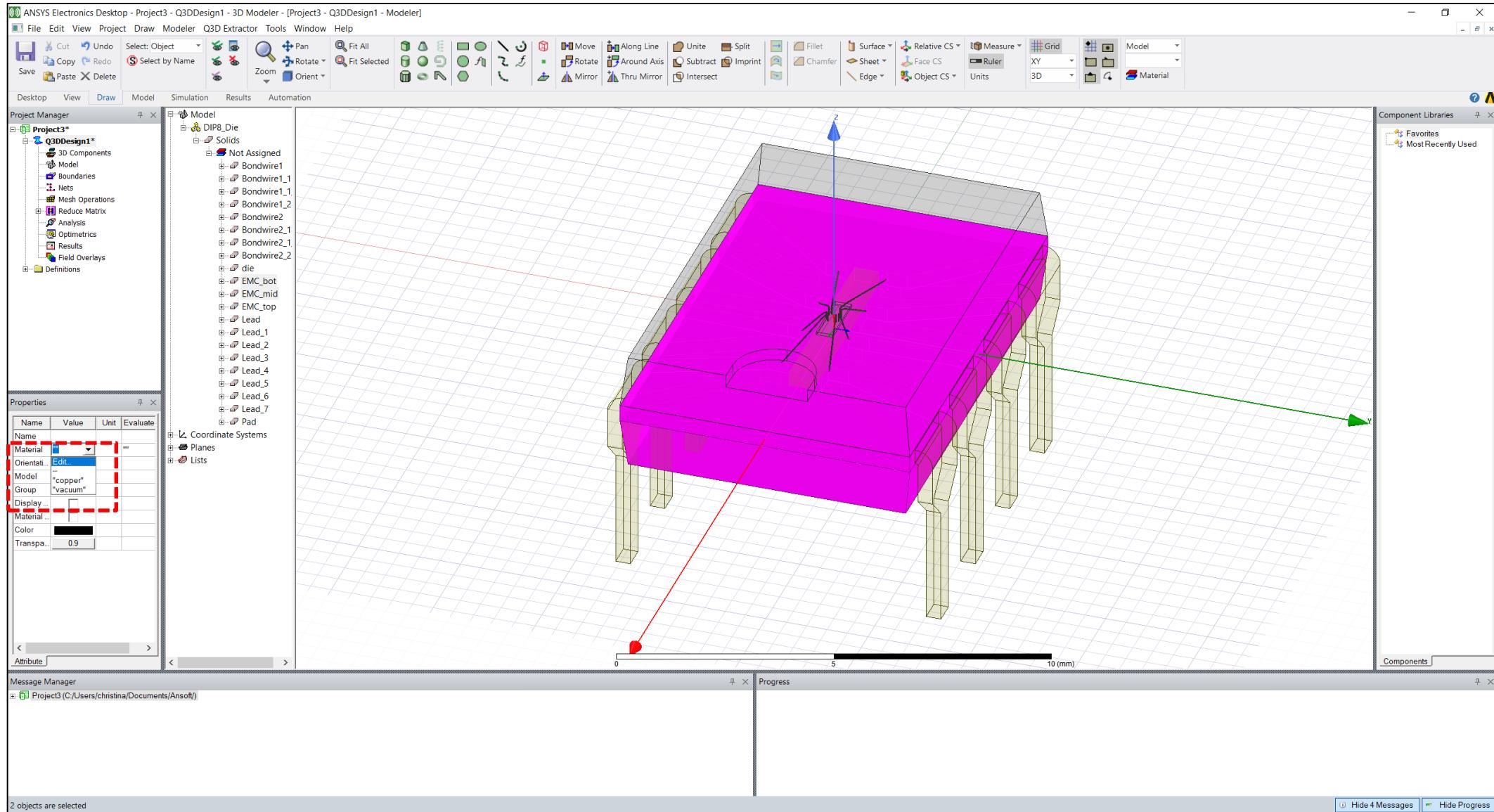
4: Import 3D Model



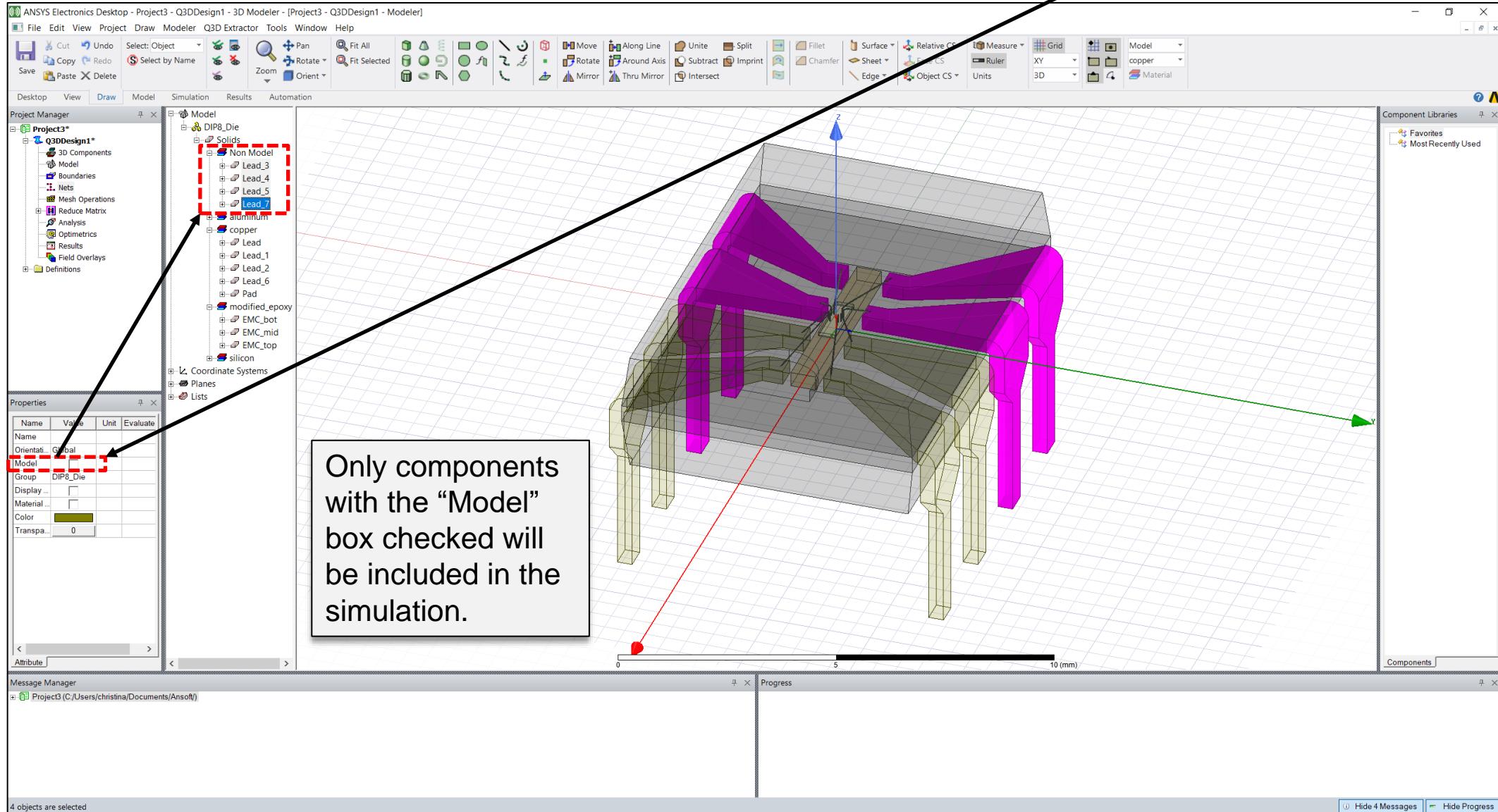
4: Import 3D Model



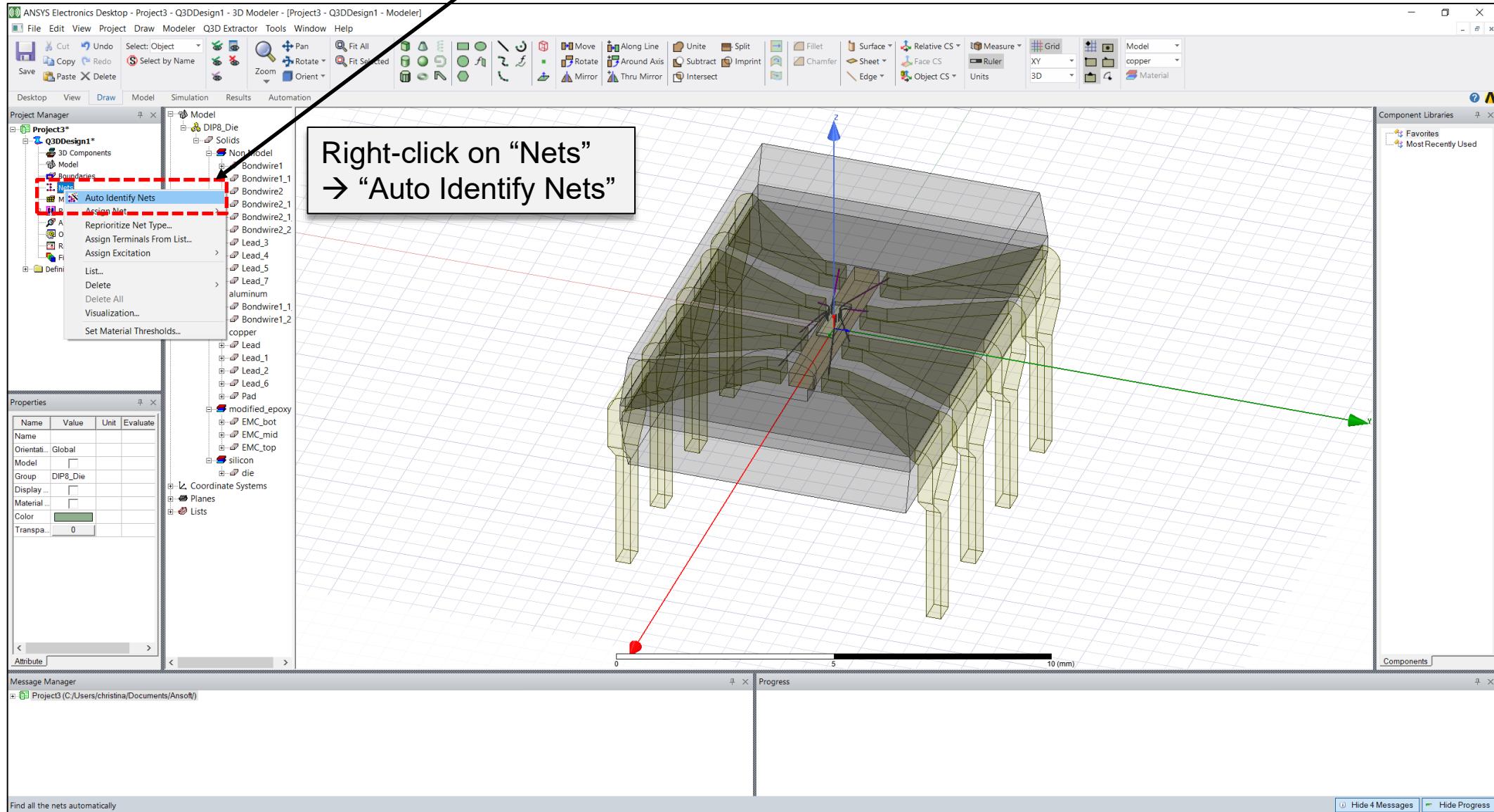
5: Assign Materials to Components



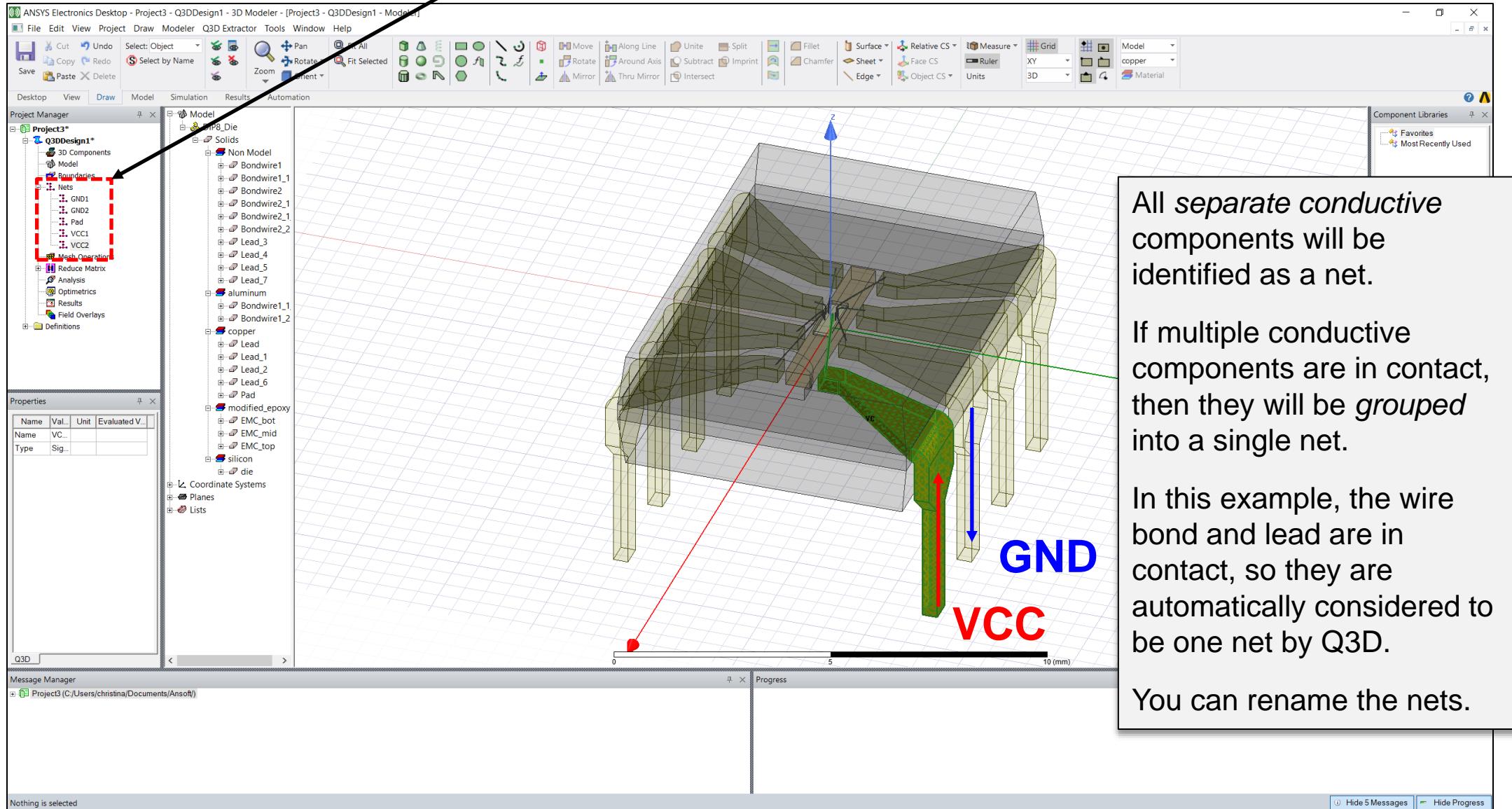
6: Make Irrelevant Components Non-Models



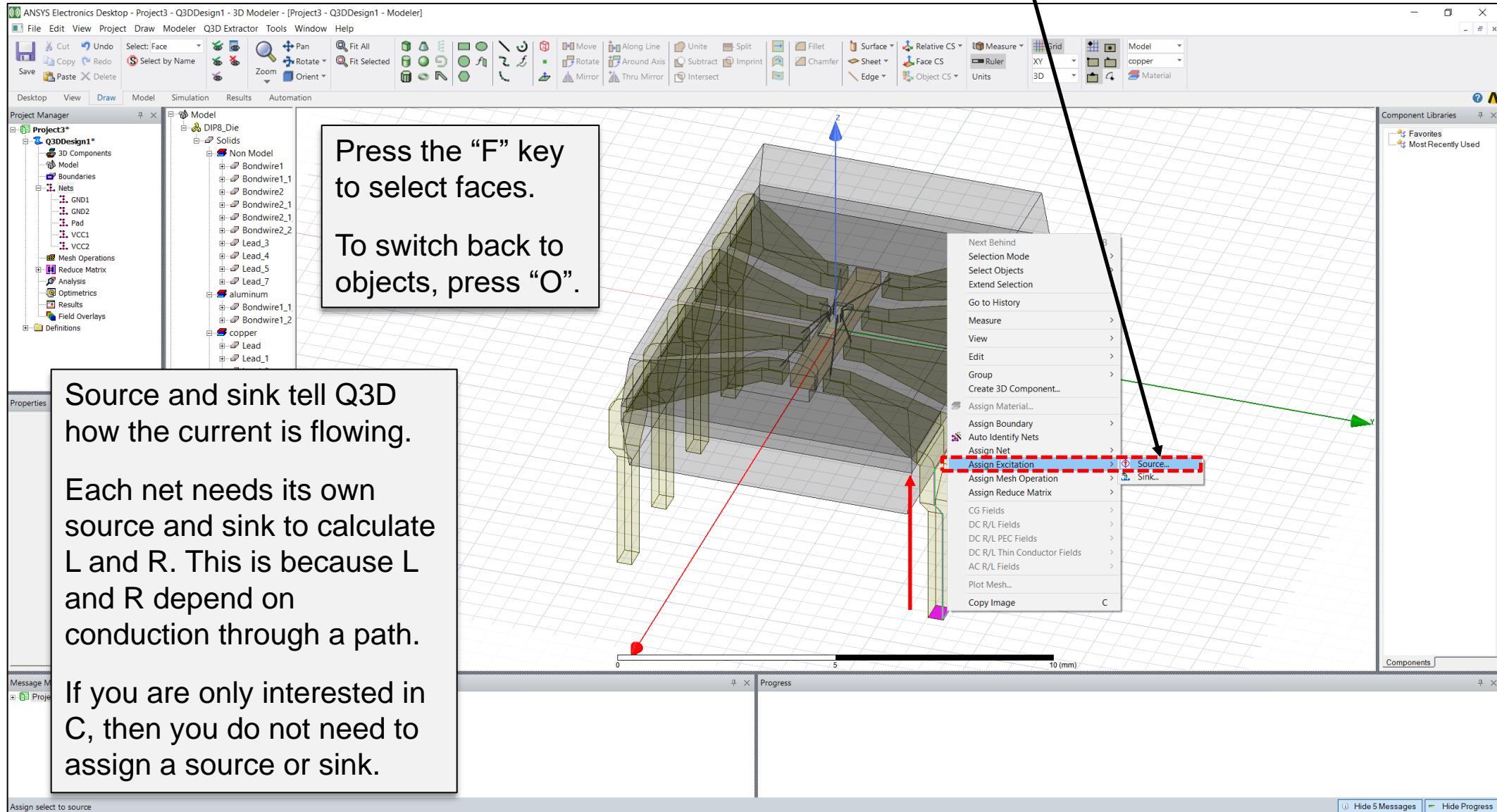
7: Identify Nets



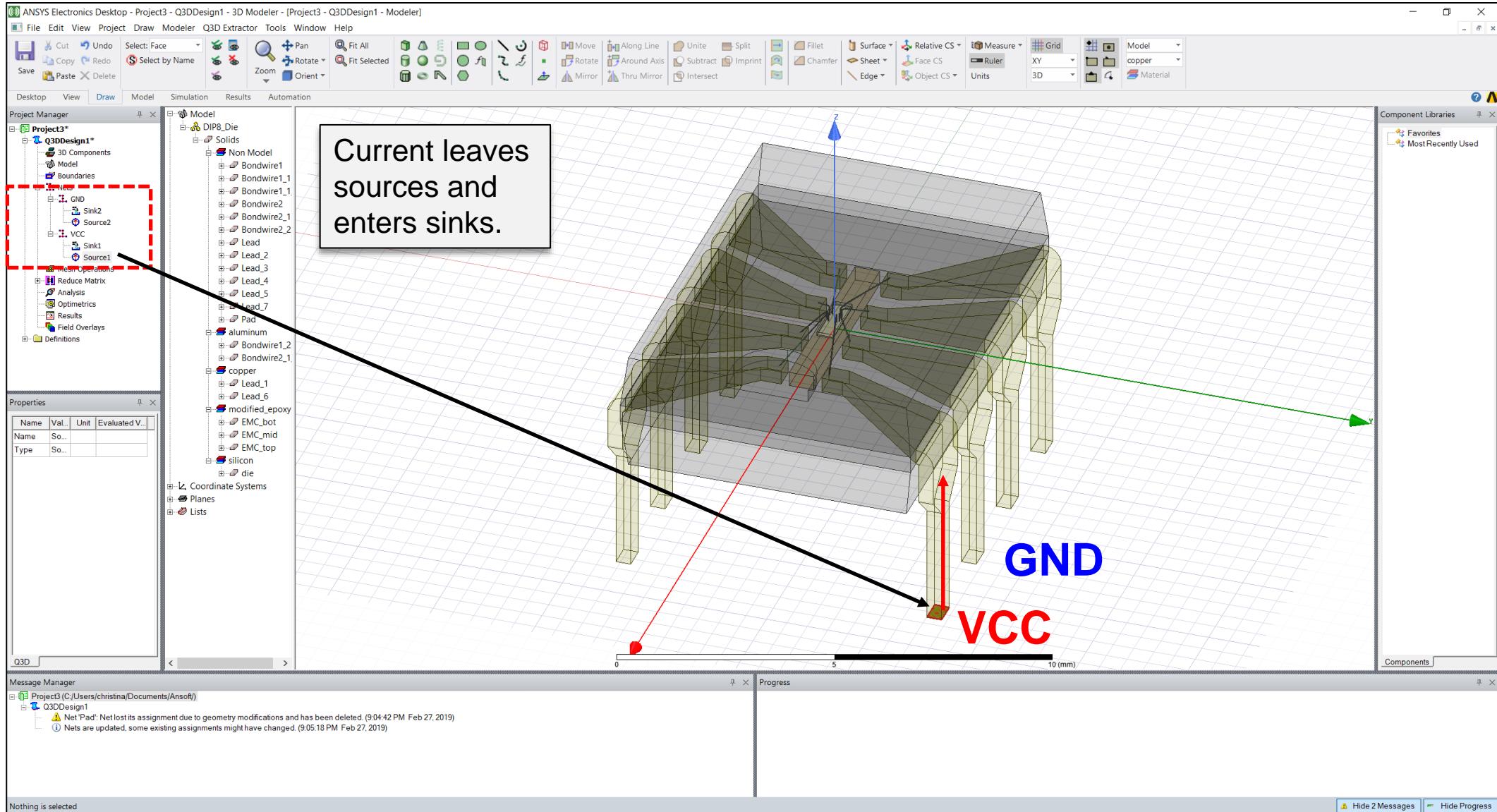
7: Identify Nets



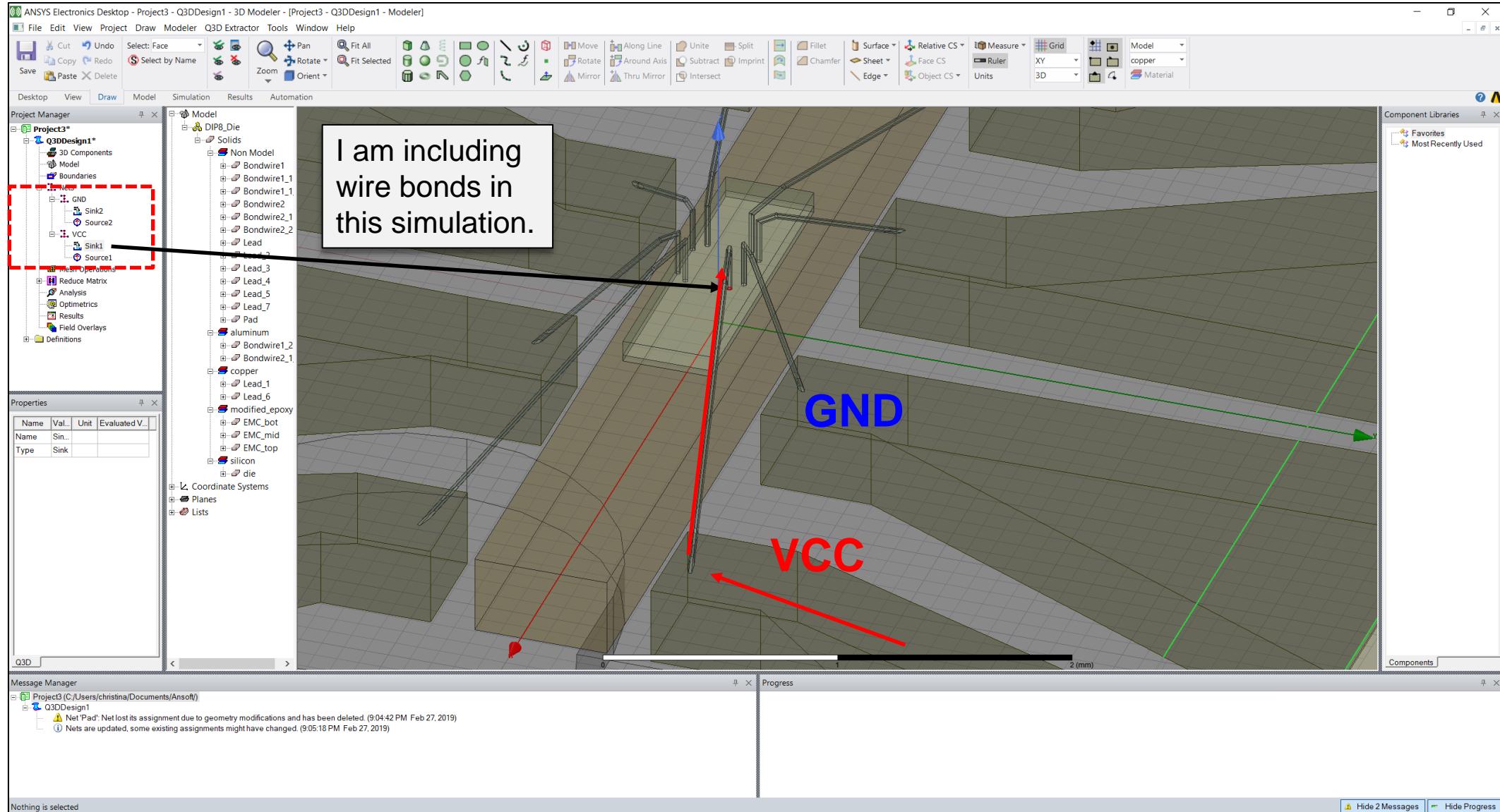
8: Assign Sources and Sinks to the Nets



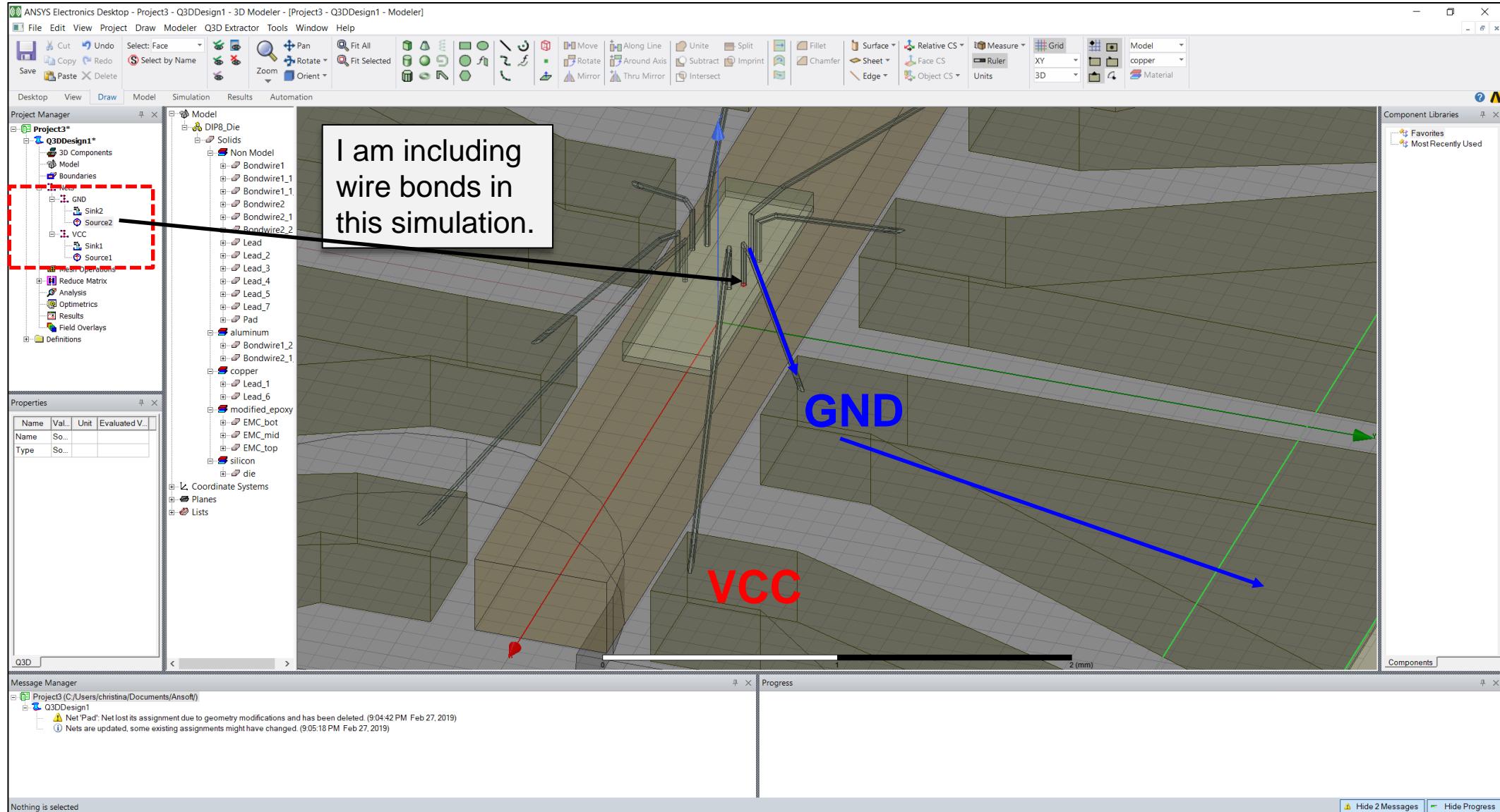
8: Assign Sources and Sinks to the Nets



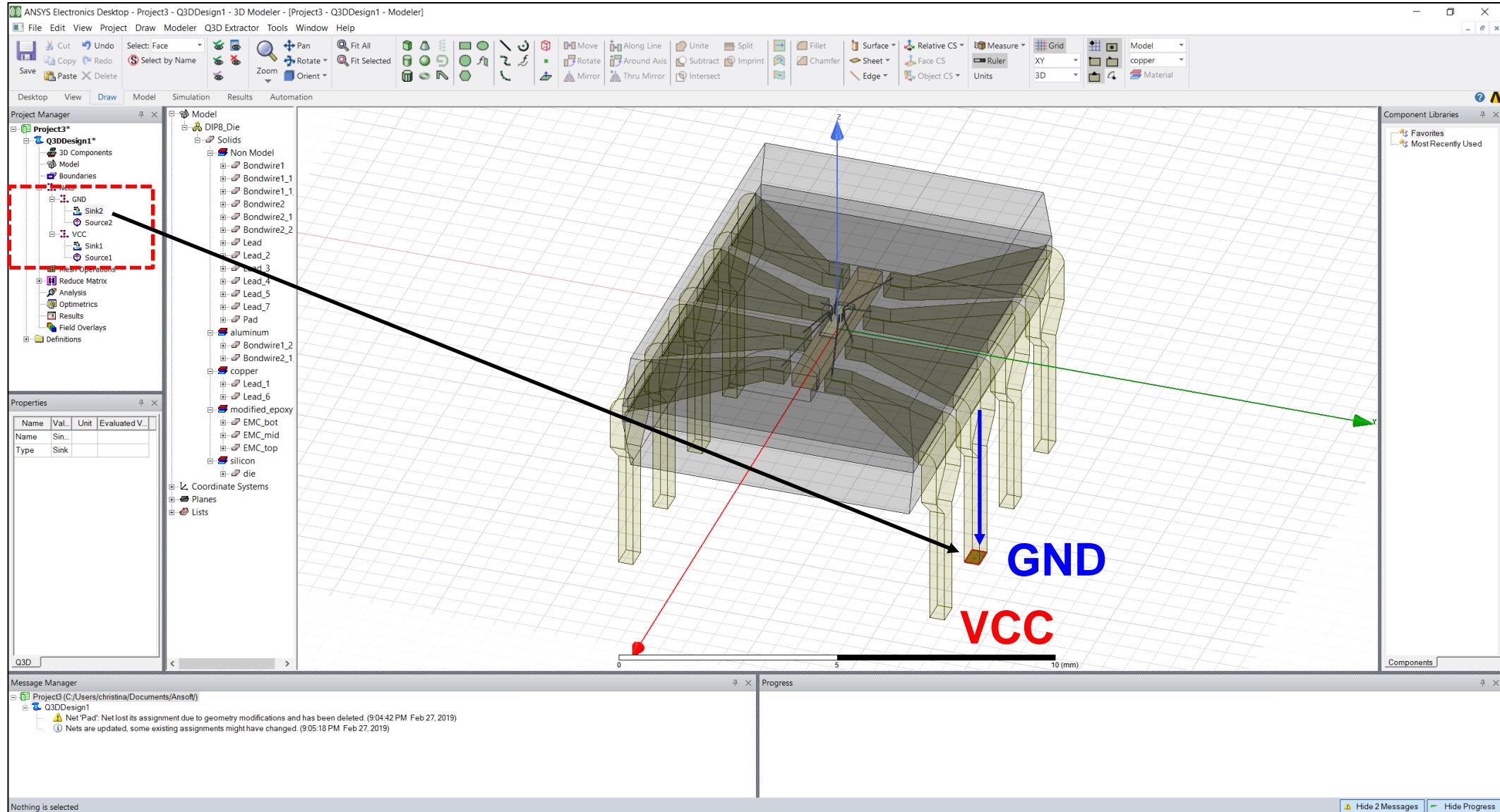
8: Assign Sources and Sinks to the Nets



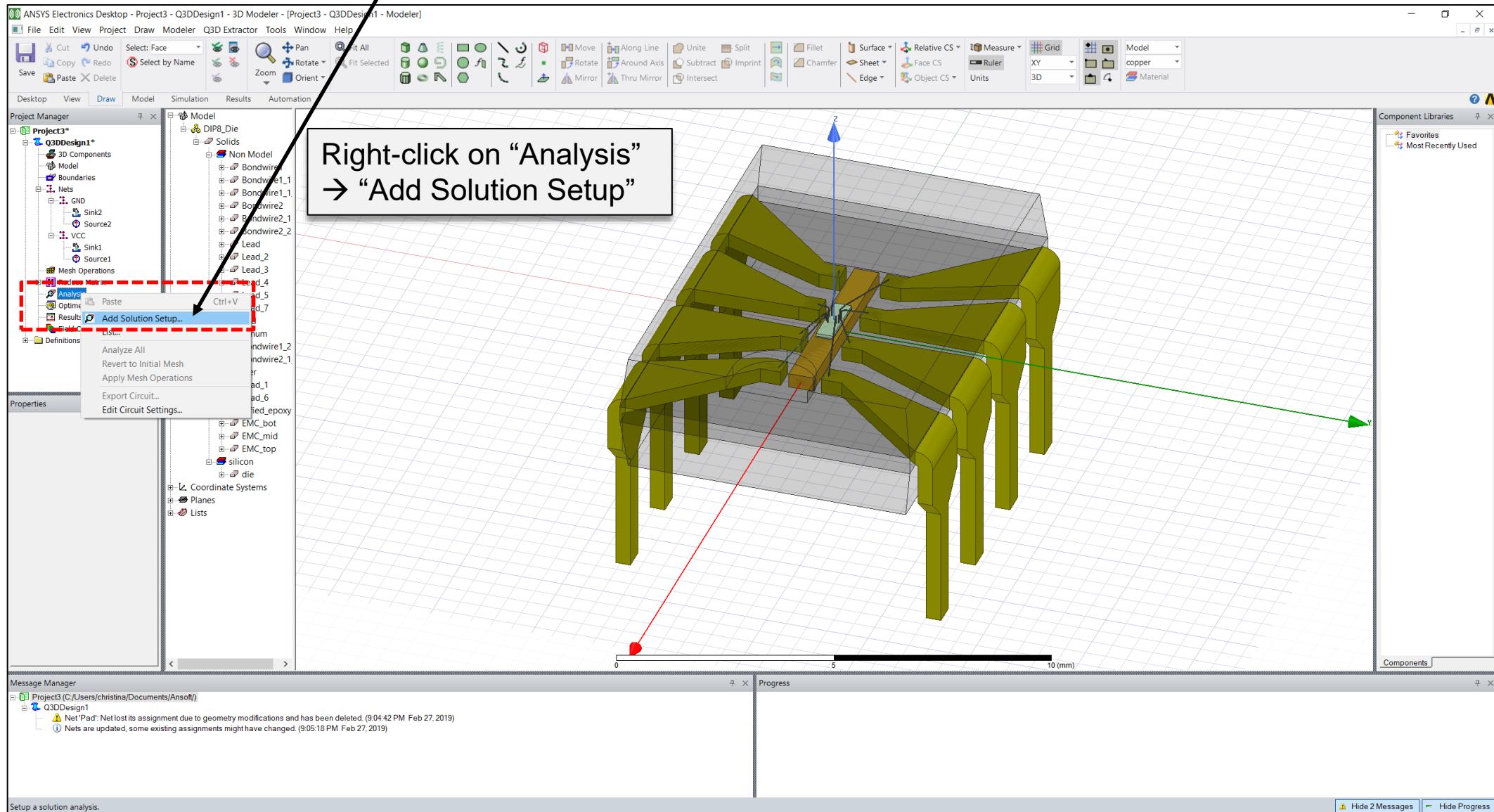
8: Assign Sources and Sinks to the Nets



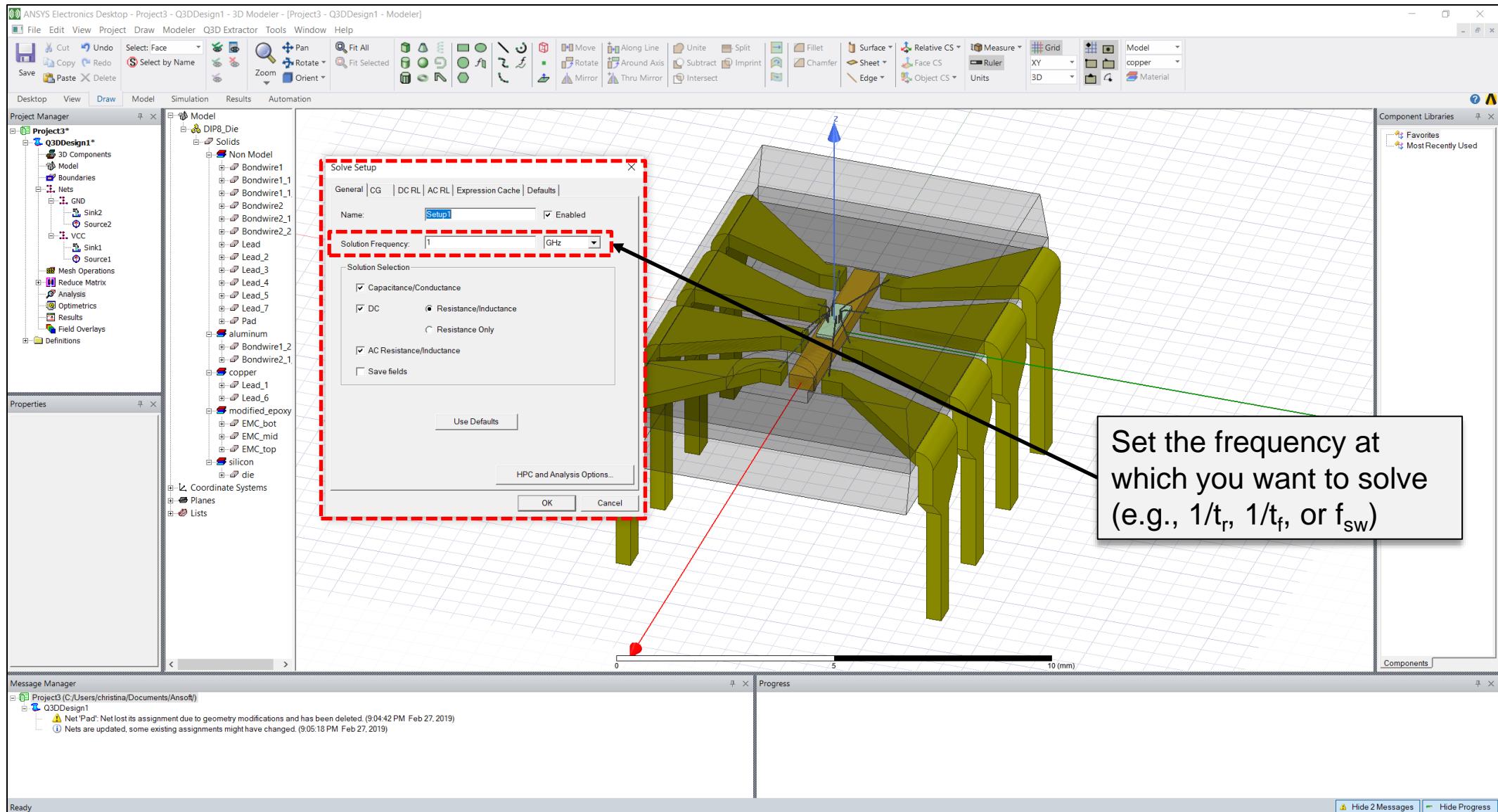
8: Assign Sources and Sinks to the Nets



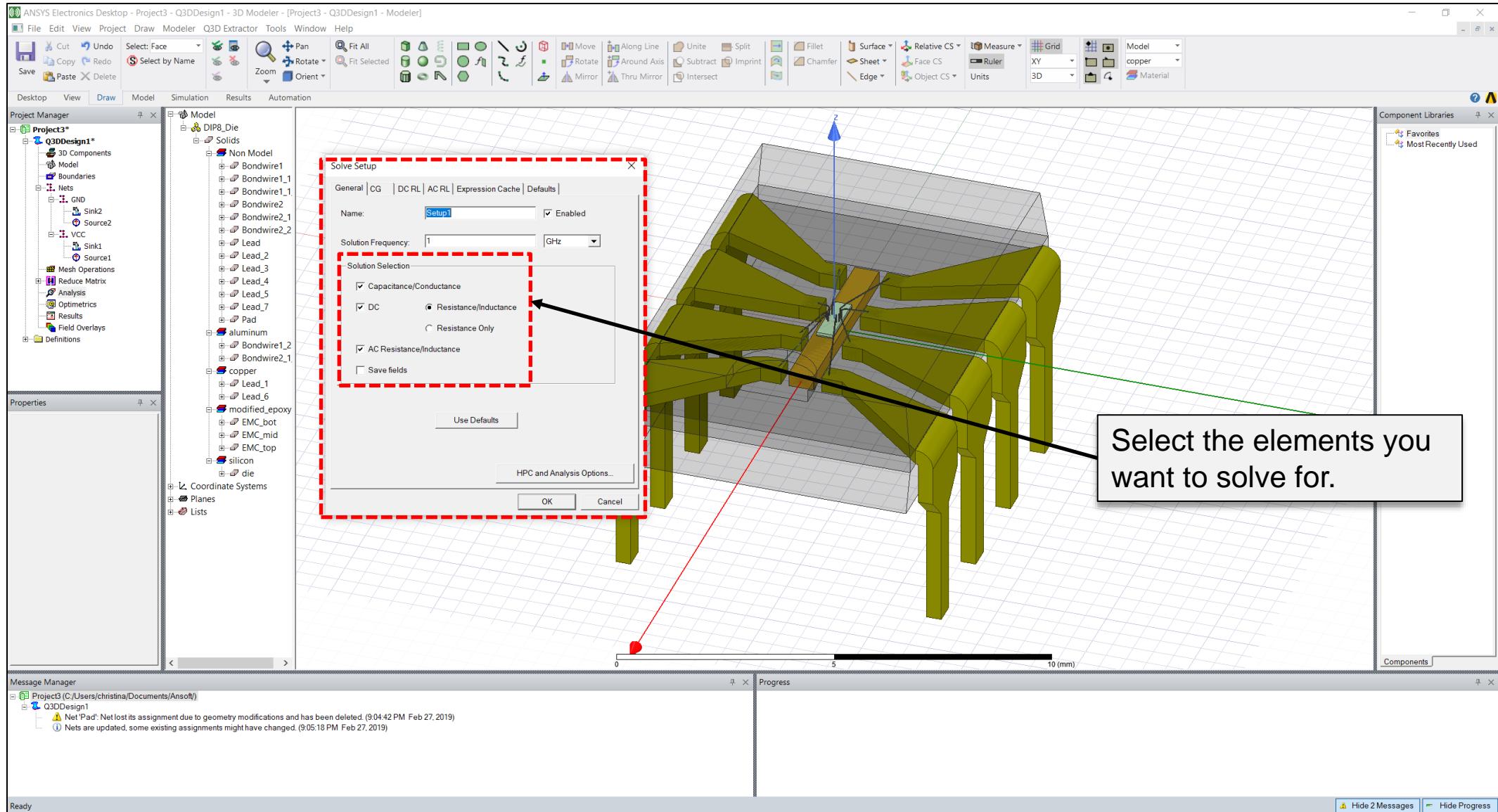
9: Add Solution Setup



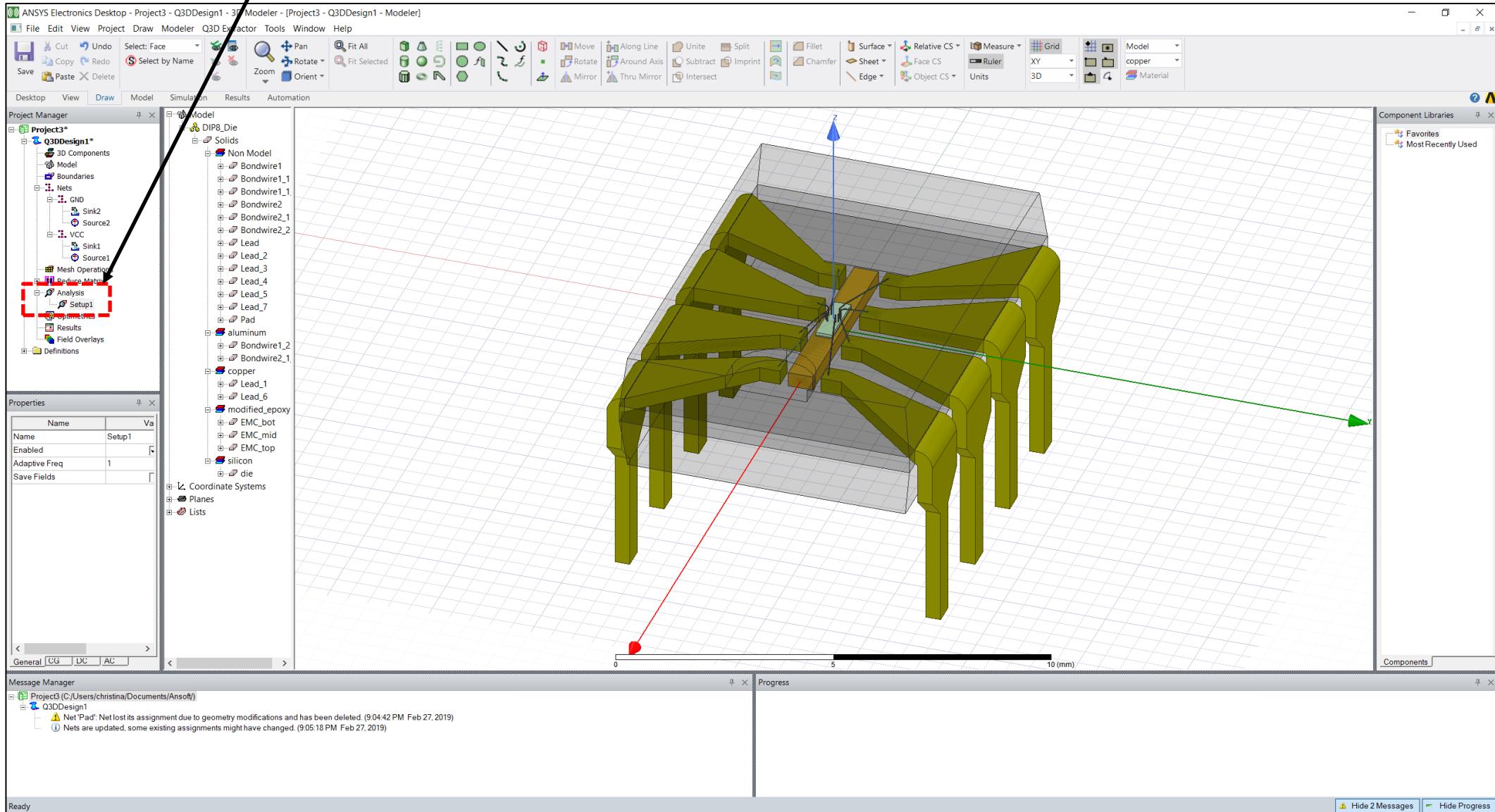
9: Add Solution Setup



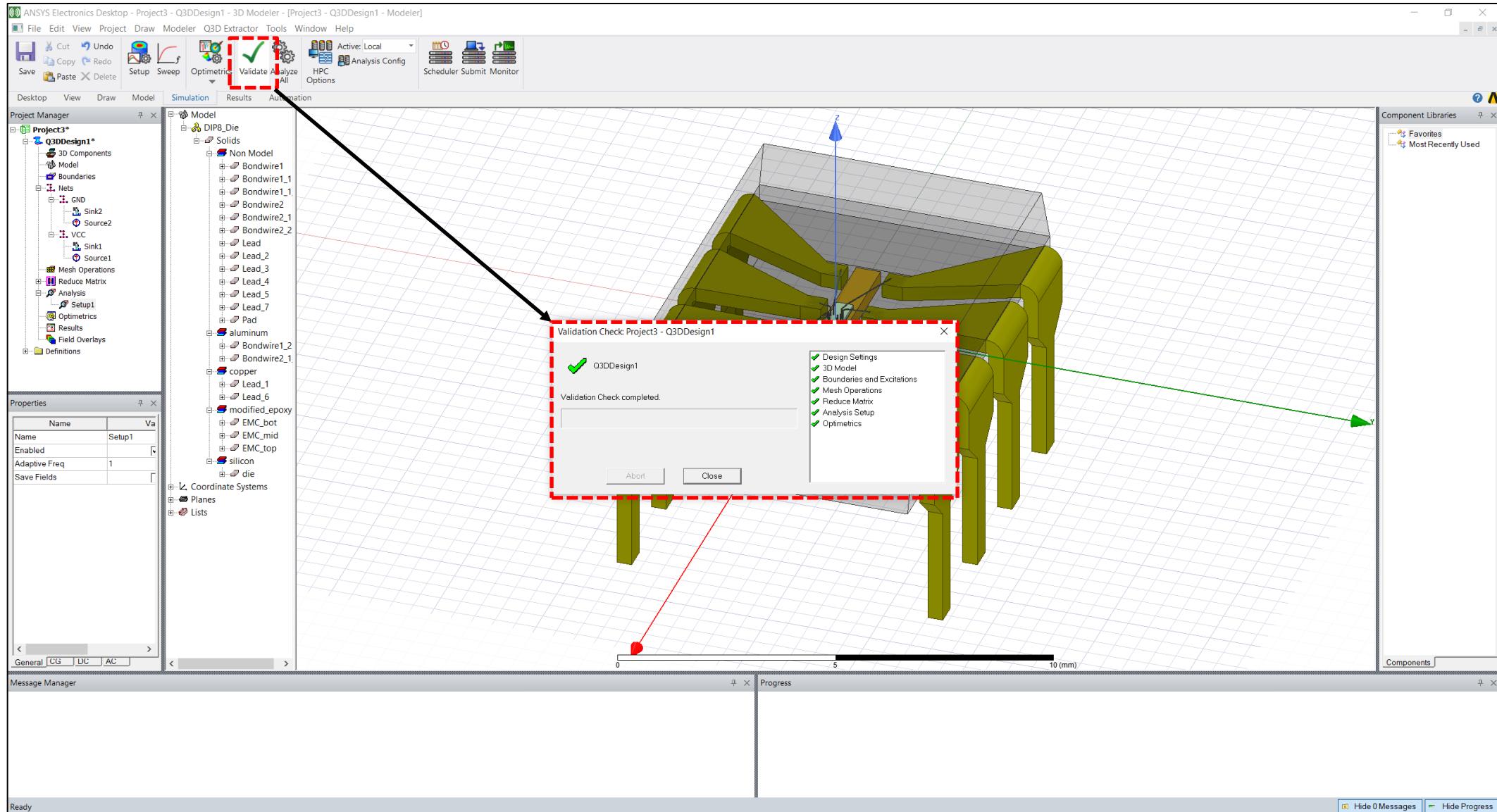
9: Add Solution Setup



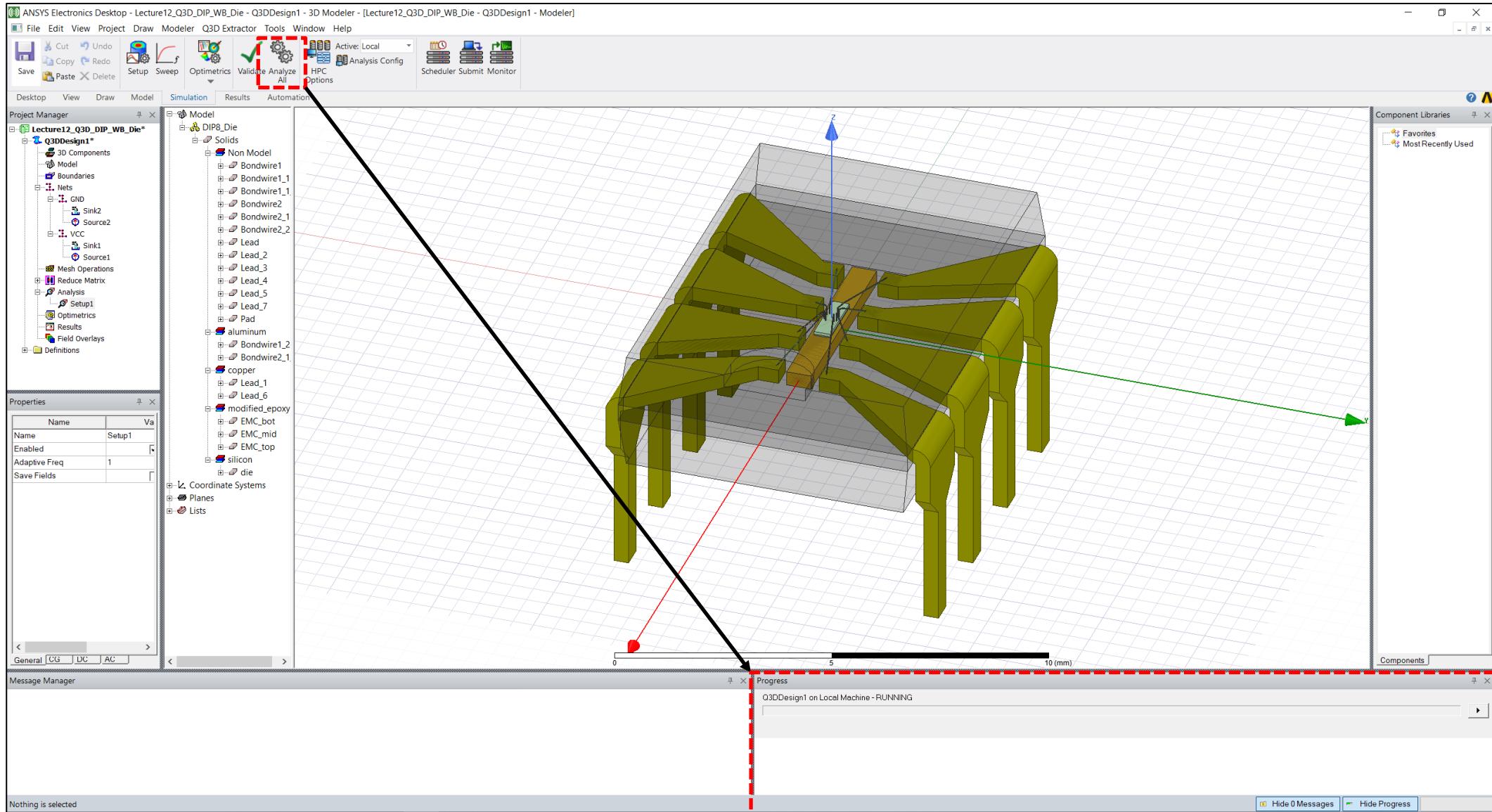
The Setup will Appear in the Project Manager



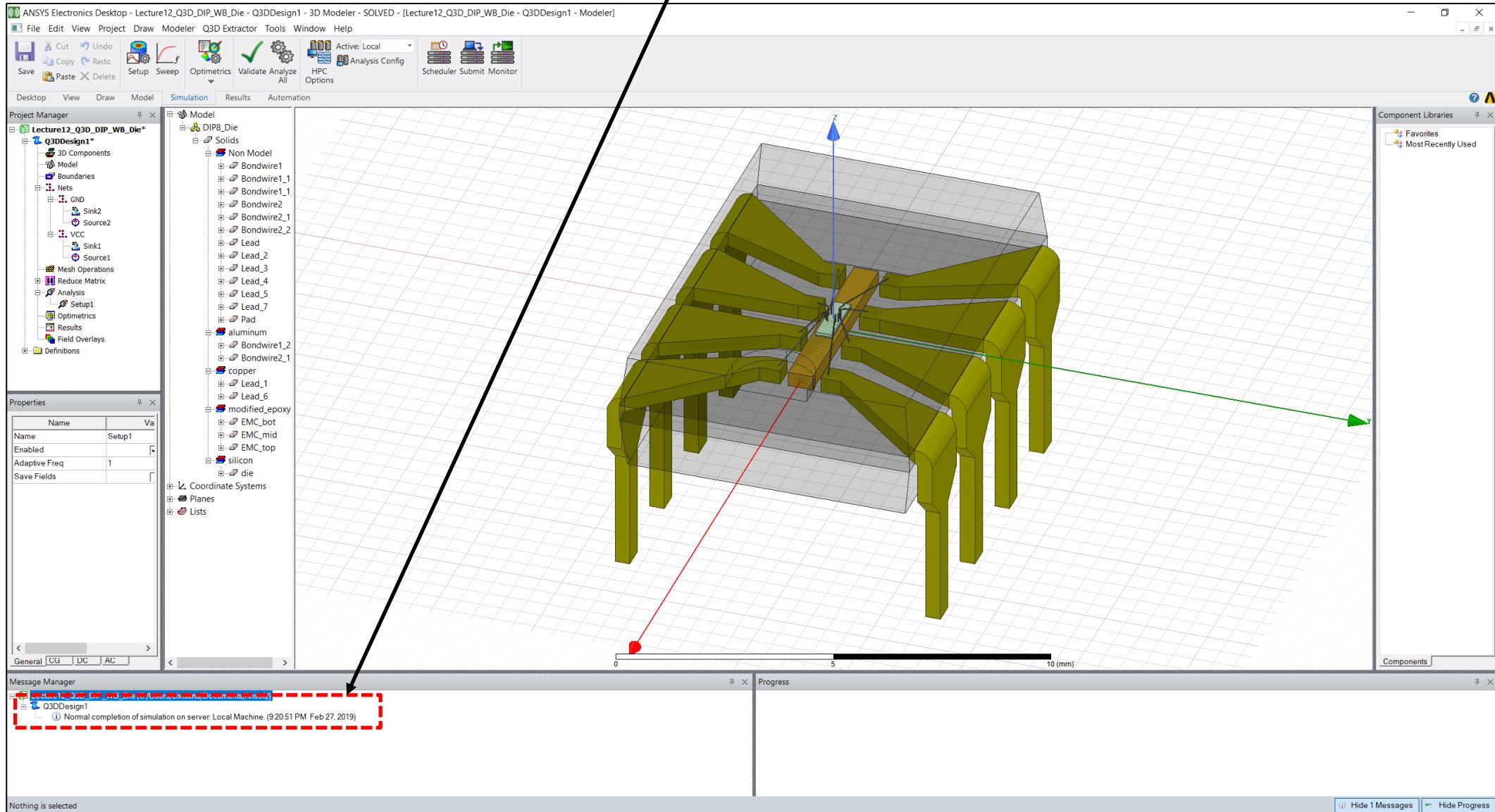
10: Validation Check



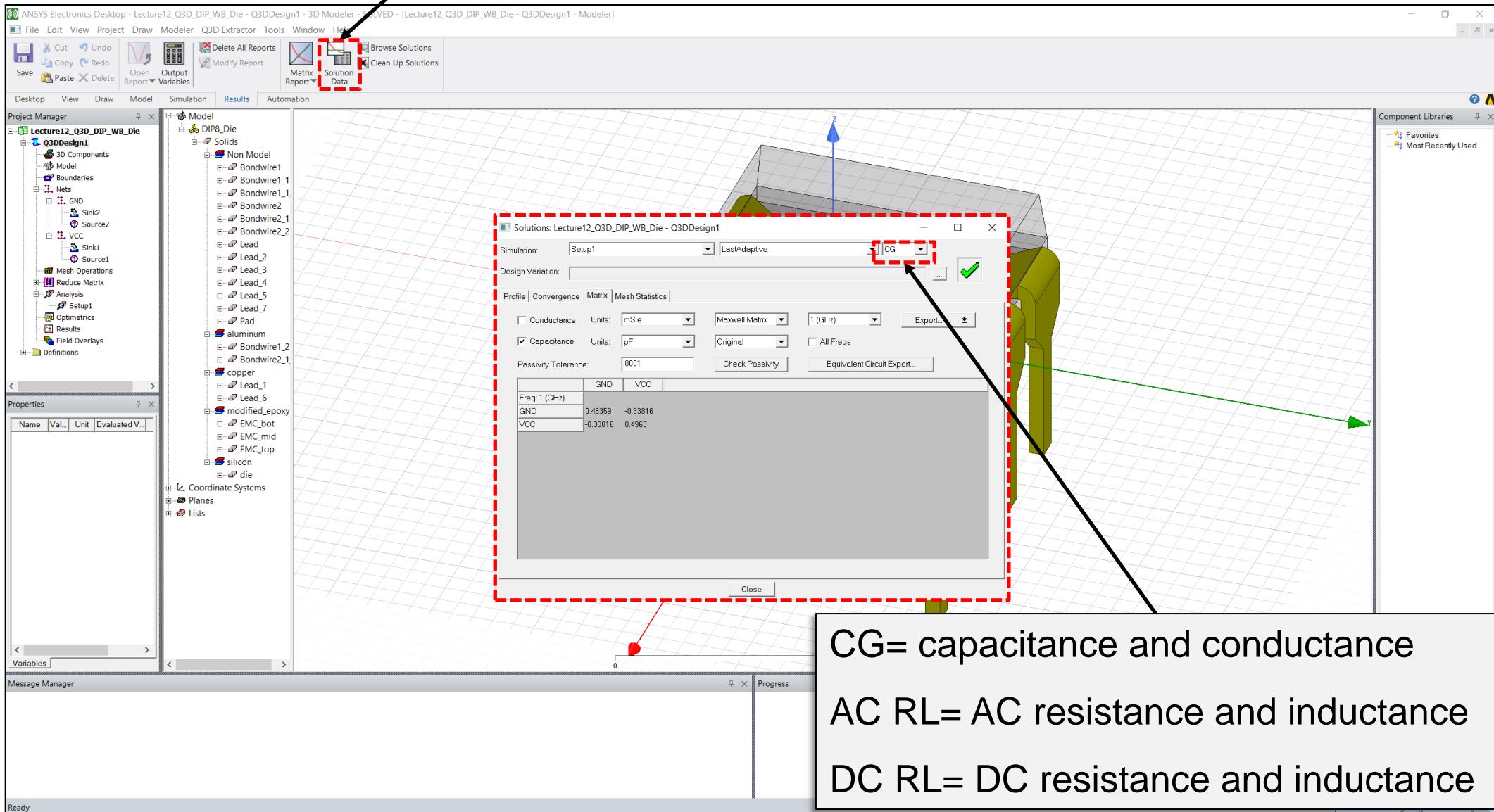
11: Analyze All



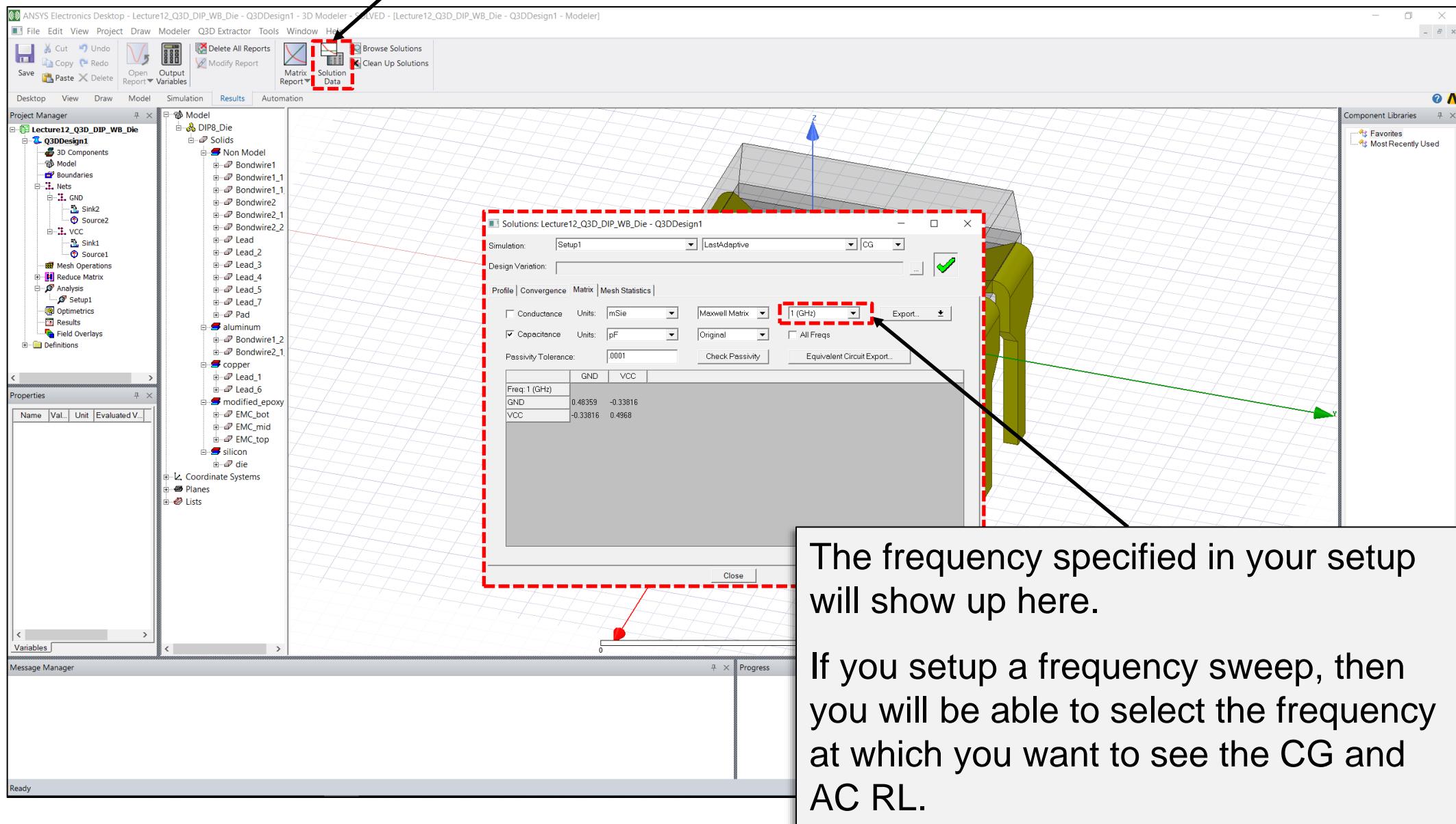
12: Check Message Window for Errors



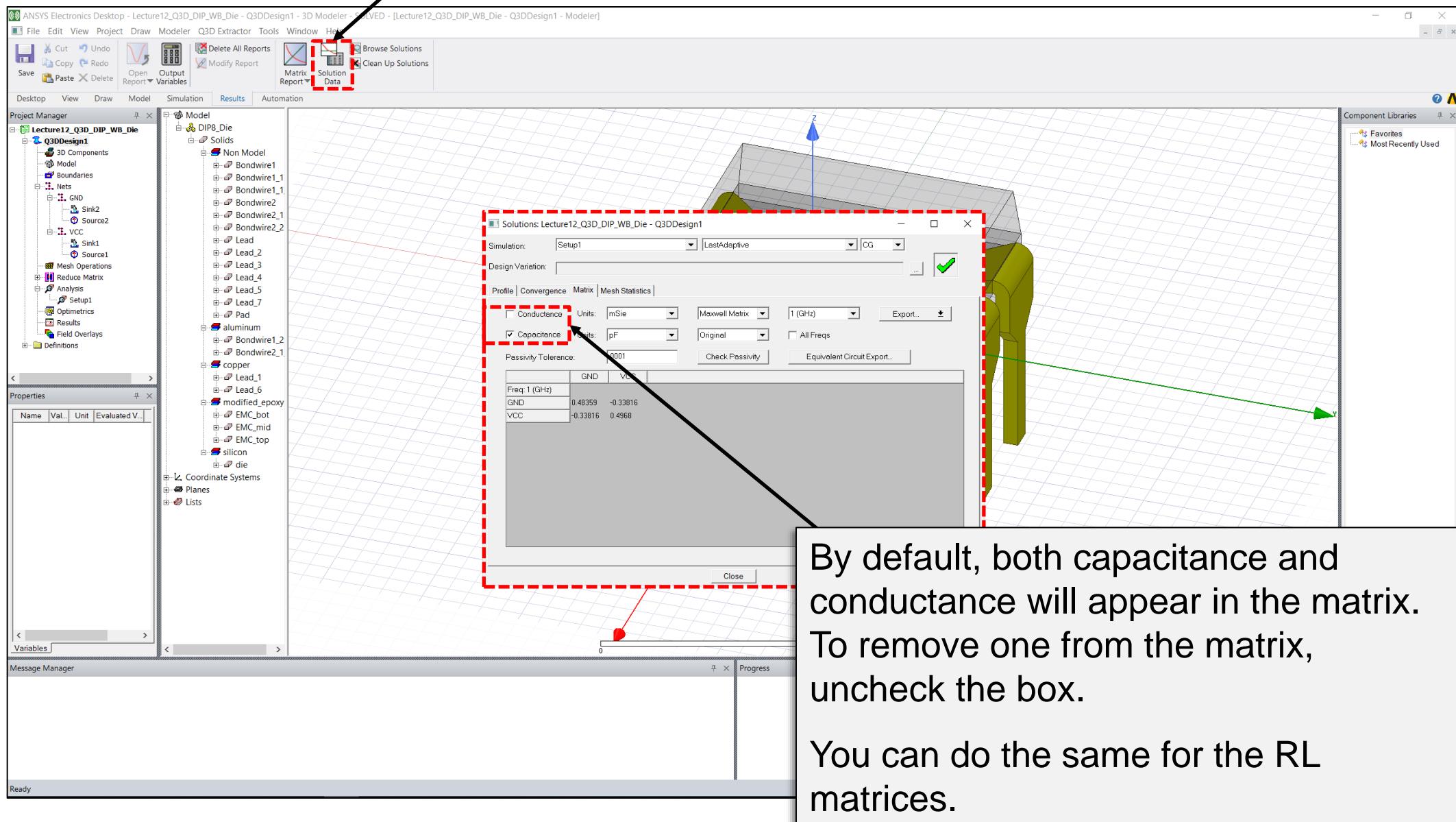
13: View Solution Data



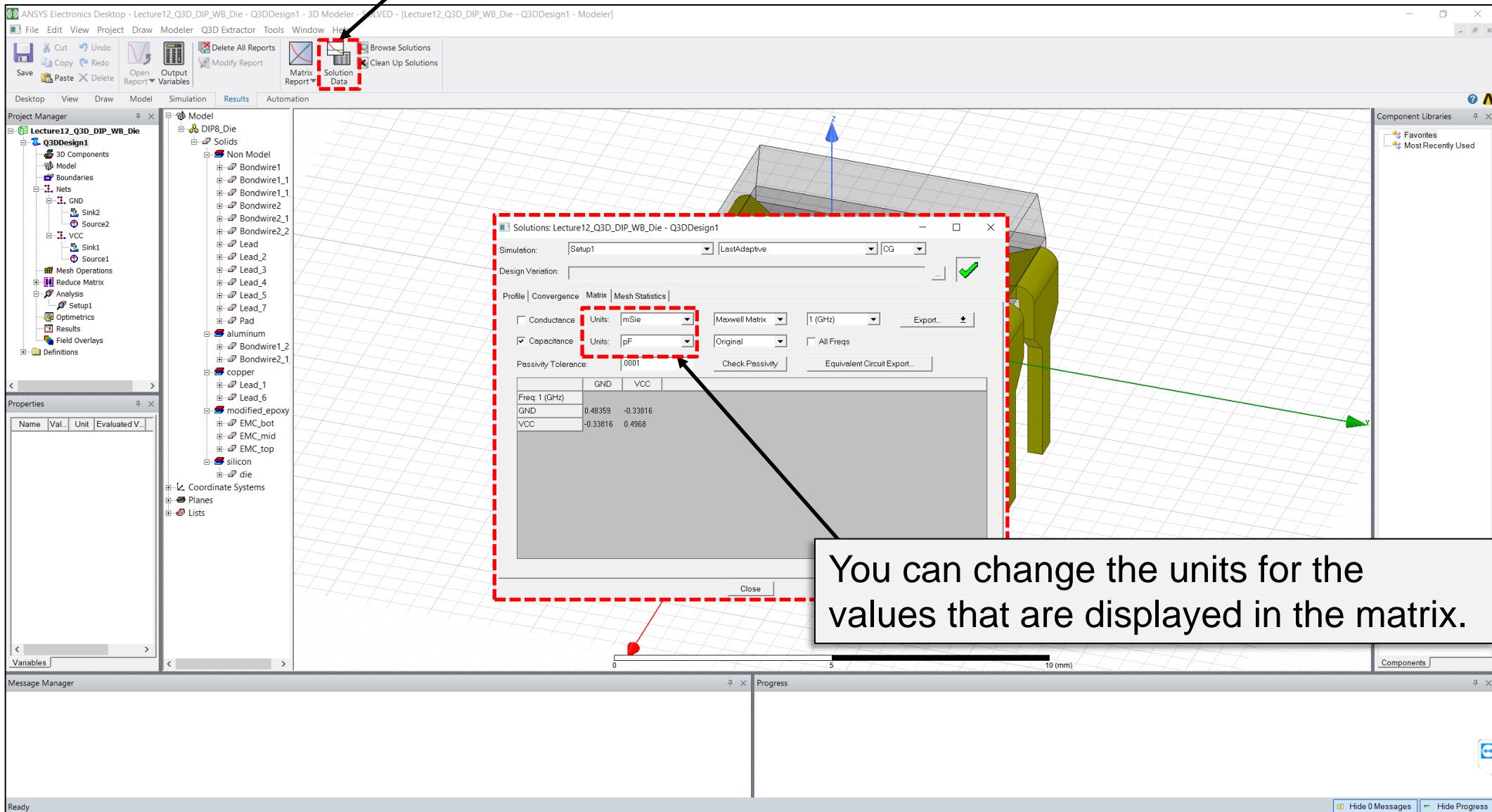
13: View Solution Data



13: View Solution Data



13: View Solution Data



Capacitance Matrix

The screenshot shows the ANSYS Electronics Desktop interface with a 3D model of a DIP8 package. The Project Manager on the left lists components like DIP8_Die, Q3DDesign1, and various bondwires and leads. The main window displays the 3D model with a coordinate system (x, y, z). A red dashed box highlights the 'Matrix' tab in the top menu bar, which is connected by a black arrow to a capacitance matrix window. This window shows the following data:

	GND	VCC
GND	0.48359	-0.33816
VCC	-0.33816	0.4968

Below the matrix, a message box provides the following information:

$C_{GND} = 0.48 \text{ pF}$ } Self-capacitances
 $C_{VCC} = 0.50 \text{ pF}$ }
 $C_{GND-VCC} = 0.34 \text{ pF} \rightarrow \text{Coupling capacitance}$

Inductance Matrix

The screenshot shows the ANSYS Electronics Desktop interface with the 'Matrix' tab selected in the top menu bar. A red dashed box highlights the 'Matrix' tab and the results window. The results window displays the inductance matrix for a single frequency of 1 GHz. The matrix is a 2x2 matrix with the following values:

	GND:Source2	VCC:Source1
Freq: 1 (GHz)		
GND:Source2	4.5241	-1.8495
VCC:Source1	-1.8495	6.3002

Arrows point from the matrix values to the following text boxes:

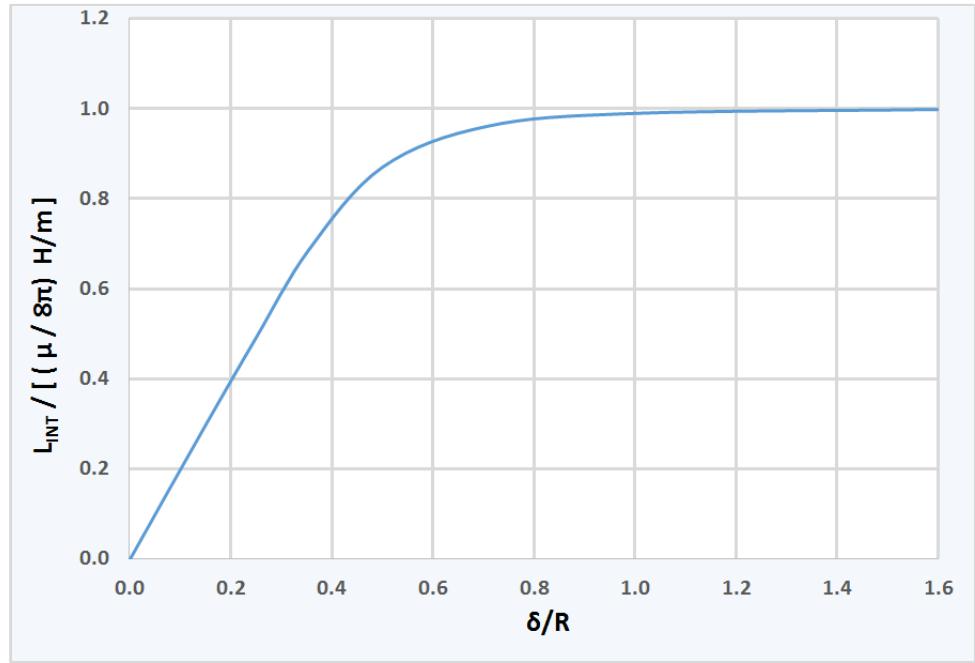
- $L_{GND} = 4.5 \text{ nH}$
- $L_{VCC} = 6.3 \text{ nH}$
- $M_{GND-VCC} = -1.8 \text{ nH} \rightarrow \text{Mutual inductance}$
- Self-inductances – inductance of the net from its source to its sink

ANSYS Q3D Extractor: Resistance

- DC resistance
 - Resistance under DC
 - Independent of frequency
- AC resistance
 - Assumes skin effect is well developed
 - Depends on frequency
- Q3D can add the two when exporting the equivalent circuit
 - “Add DC and AC Resistance”

ANSYS Q3D Extractor: Inductance

- DC inductance
 - No skin effect considered
 - Independent of frequency
- AC inductance
 - Assumes skin effect is well developed
 - Depends on frequency
 - Self-inductance of the conductor decreases as skin depth decreases (as frequency increases)



Equivalent Circuit Export

Solutions: Q3D_dip - Q3DDesign1

Simulation: Setup1 LastAdaptive ACRL

Design Variation:

Profile Convergence Matrix Mesh Statistics

Resistance Units: ohm Inductance Units: nH

Matrix: Original 100 (MHz) All Freqs

Passivity Tolerance: 0001 Check Passivity Equivalent Circuit Export...

	GND:Source2	VCC:Source1
Freq: 100 (MHz)		
GND:Source2	3.5517	1.2664
VCC:Source1	1.2664	3.7563

Export Circuit

Circuit Export

Solution: Setup1 : Sweep1 Variation: File name: C:/Users/christina/Documents/Ansoft/K Model Name: Q3D_dip

Equivalent Circuit Settings

Select Freq: 0.1 GHz Edit Freq... Matrix: Original

Select Matrix Type: Capacitance Conductance
 DC Resistance DC Inductance
 AC Resistance AC Inductance
 Add DC and AC Resistance
 Extract pin names from source names

IBIS Export Number of Cells: 1 Coupling Limits... Include Chip Package Protocol

Preview... Export Circuit... Close

*Note: k is the coupling coefficient

$$k = \frac{M}{\sqrt{L_1 L_2}}$$

Circuit Model Preview

```

* BEGIN ANSOFT HEADER
* node 1 GND:Source2
* node 2 VCC:Source1
* node 3 GND:Sink2
* node 4 VCC:Sink1
* Project: Q3D_dip
* Design: Q3DDesign1
* Format: Ansoft Designer
* Topckt: Q3D_dip
* Left: 1 2
* Right: 3 4
* Creator: Ansoft Electronics Desktop 2018.2.0
* Date: Wed Feb 06 19:40:38 2019
* END ANSOFT HEADER

.subckt Q3D_dip 1 2 3 4
XZhalf1 1 2 5 6 Q3D_dip_half
XY1 5 6 Q3D_dip_parallel
XZhalf2 5 6 3 4 Q3D_dip_half

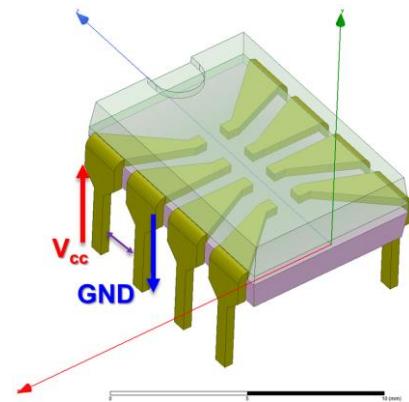
.subckt Q3D_dip_half 1 2 3 4
V1 1 5 dc 0.0
V2 2 6 dc 0.0
R1 5 7 0.000247564777209
R2 6 8 0.000265941019125
L1 7 3 2.02010846459e-09
L2 8 4 2.14453657376e-09
K1_2 L1 L2 0.319048
.ends Q3D_dip_half

.subckt Q3D_dip_parallel 1 2
C1_0 1 0 1.297549e-13
C1_2 1 2 1.727604e-13
C2_0 2 0 1.328548e-13
.ends Q3D_dip_parallel

.ends Q3D_dip

```

Close Export Circuit...

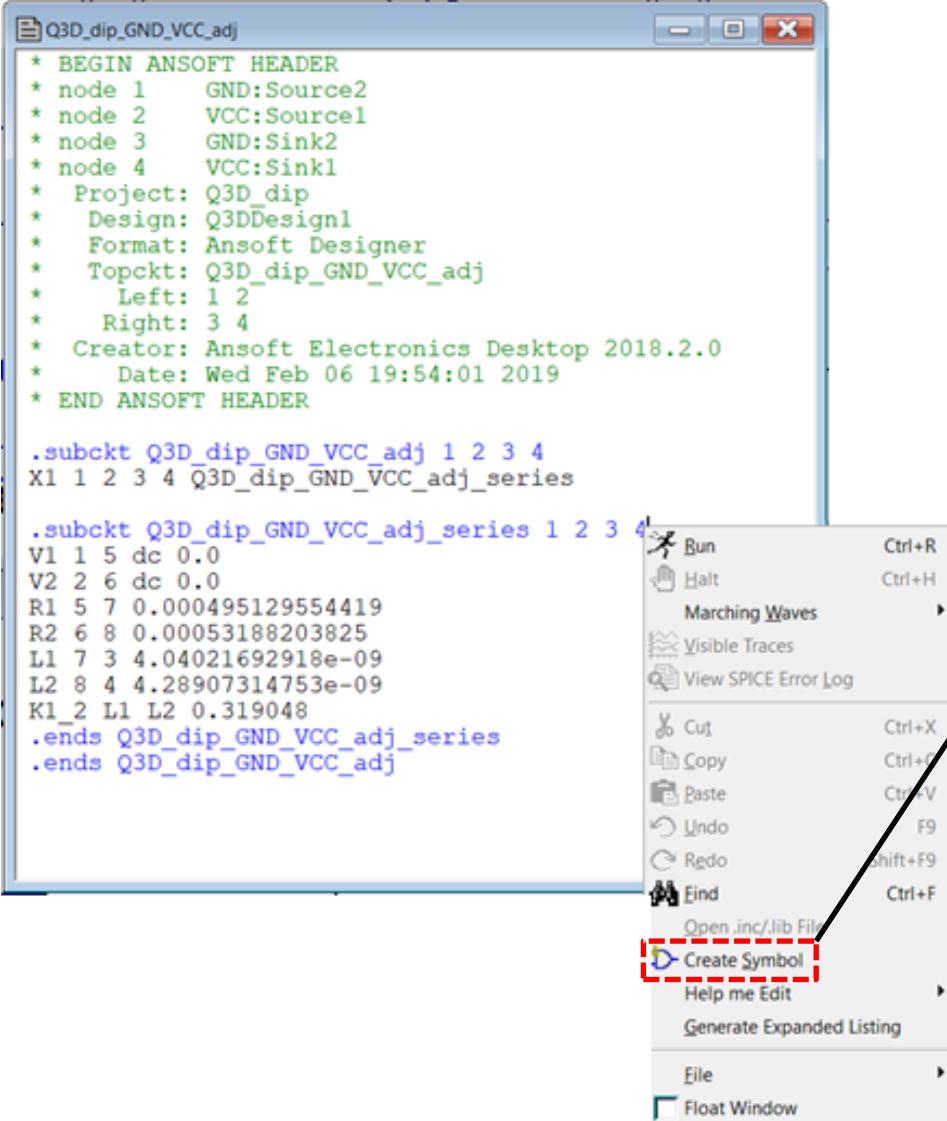


Total Subcircuit

Series R, L, k^*

Capacitance

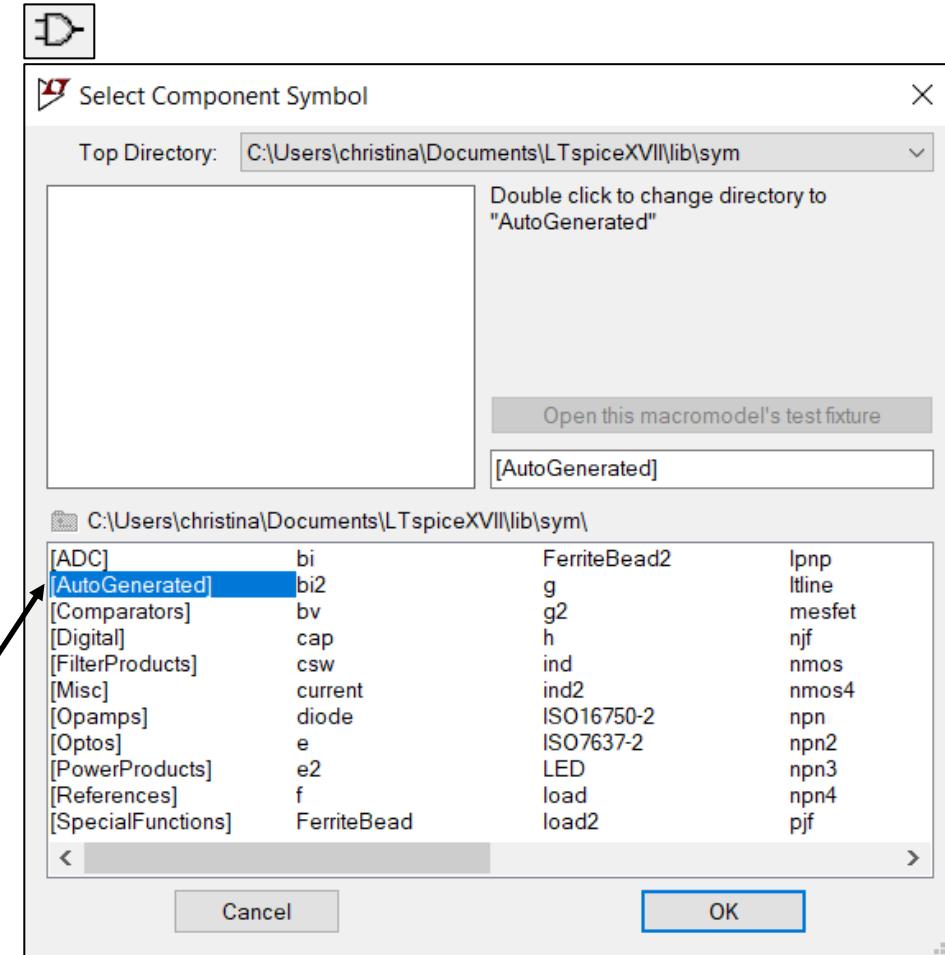
Open in LTspice and Create Symbol



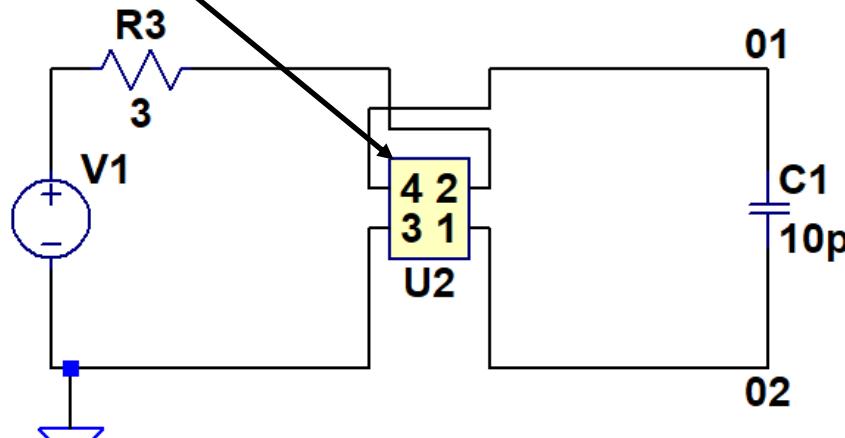
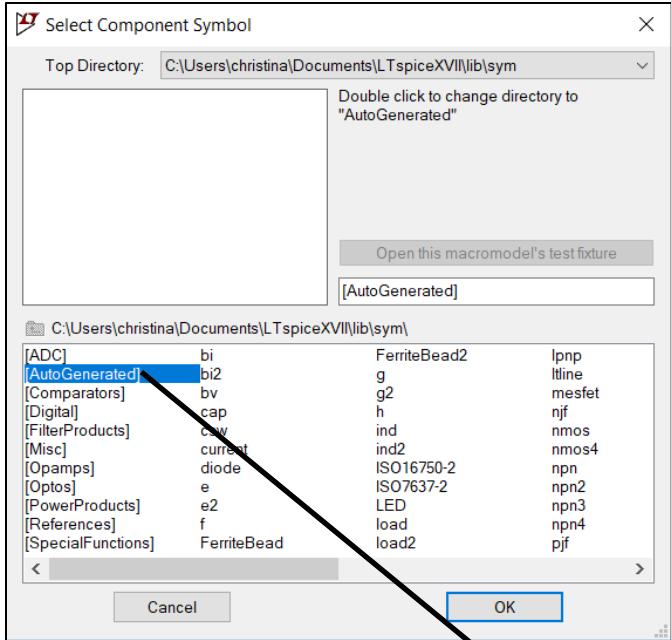
```
* BEGIN ANSOFT HEADER
* node 1 GND:Source2
* node 2 VCC:Source1
* node 3 GND:Sink2
* node 4 VCC:Sink1
* Project: Q3D_dip
* Design: Q3DDesign1
* Format: Ansoft Designer
* Topckt: Q3D_dip_GND_VCC_adj
* Left: 1 2
* Right: 3 4
* Creator: Ansoft Electronics Desktop 2018.2.0
* Date: Wed Feb 06 19:54:01 2019
* END ANSOFT HEADER

.subckt Q3D_dip_GND_VCC_adj 1 2 3 4
X1 1 2 3 4 Q3D_dip_GND_VCC_adj_series

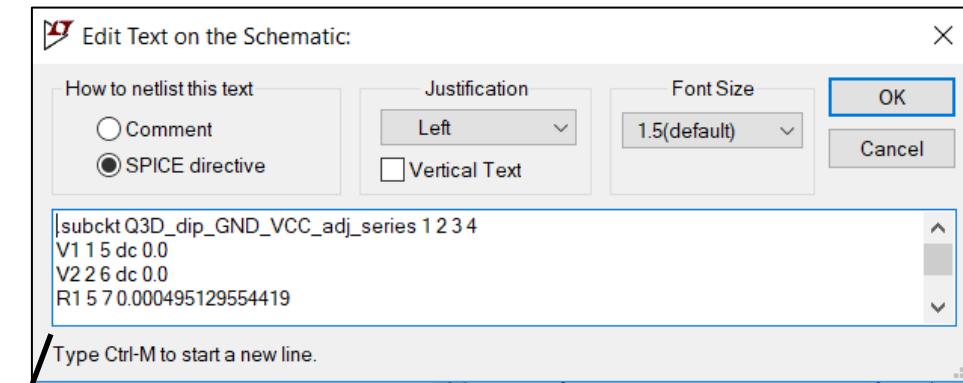
.subckt Q3D_dip_GND_VCC_adj_series 1 2 3 4
V1 1 5 dc 0.0
V2 2 6 dc 0.0
R1 5 7 0.000495129554419
R2 6 8 0.00053188203825
L1 7 3 4.04021692918e-09
L2 8 4 4.28907314753e-09
K1_2 L1 L2 0.319048
.ends Q3D_dip_GND_VCC_adj_series
.ends Q3D_dip_GND_VCC_adj
```



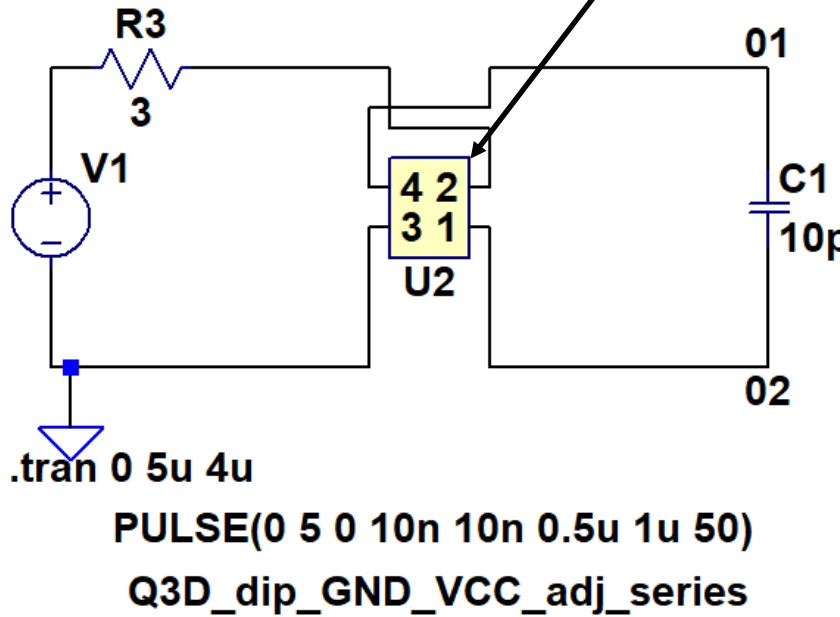
Create Schematic



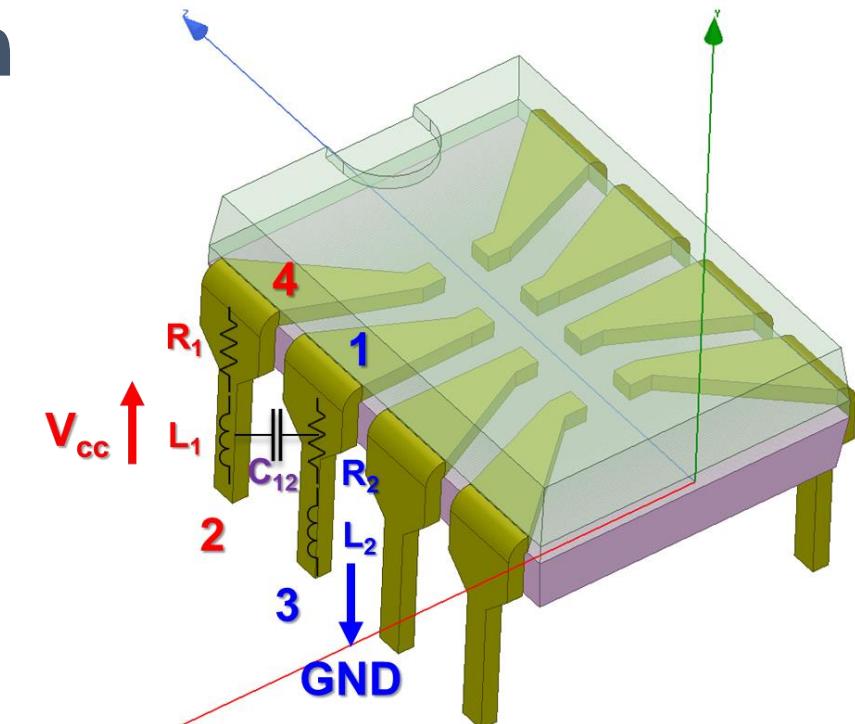
```
PULSE(0 5 0 10n 10n 0.5u 1u 50)
Q3D_dip_GND_VCC_adj_series
```



Node Identification

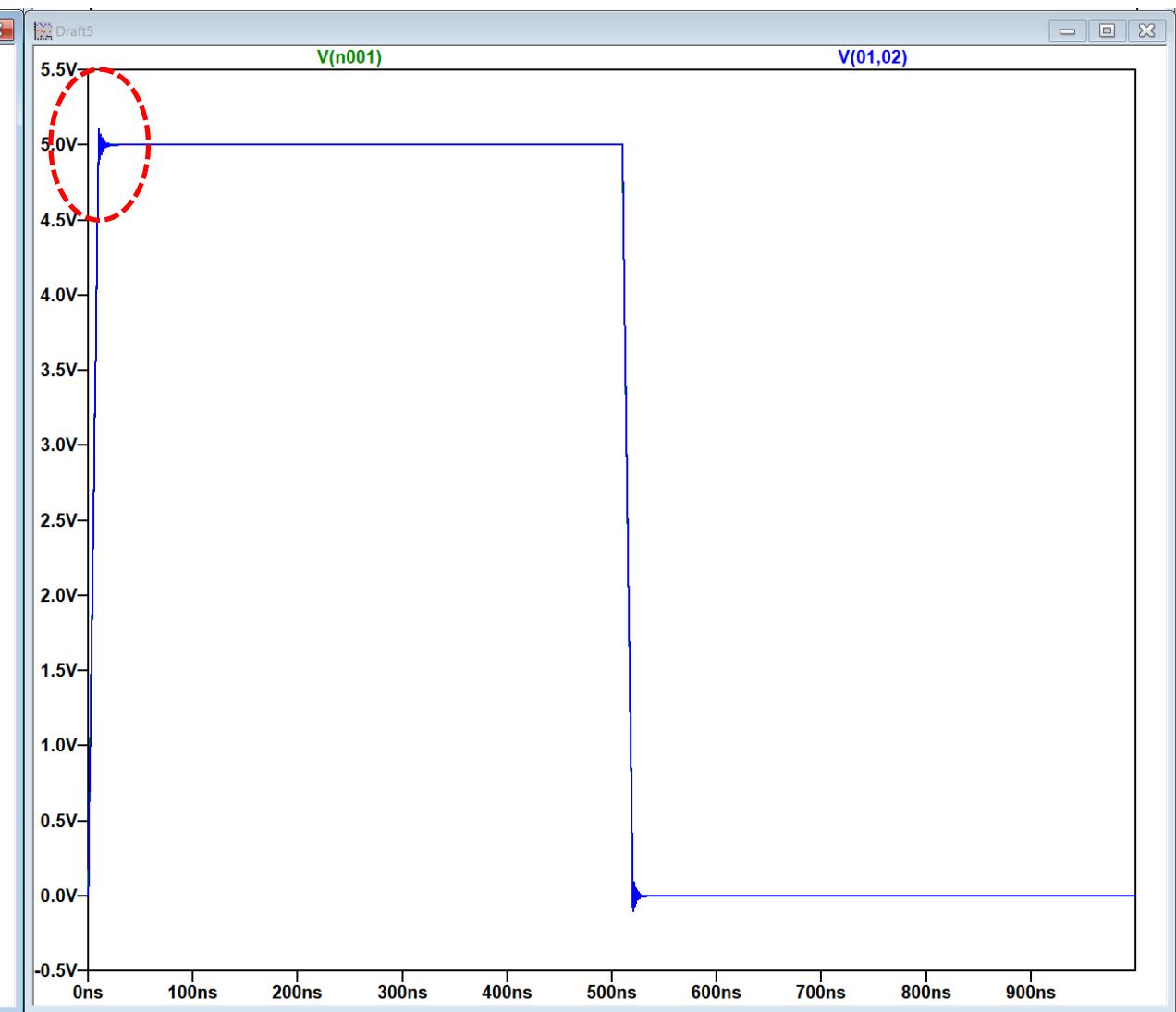
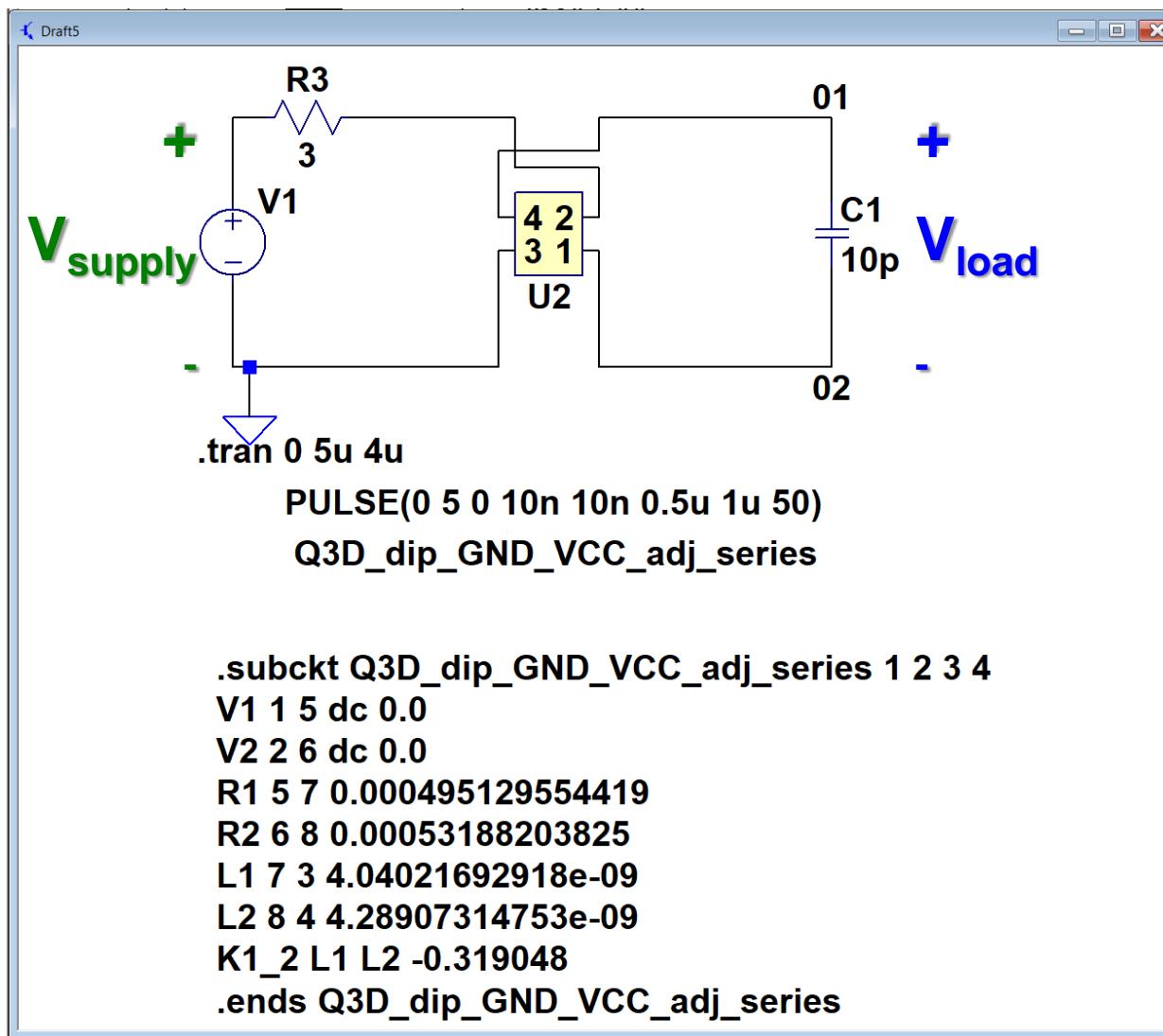


```
Q3D_dip_GND_VCC_adj
* BEGIN ANSOFT HEADER
* node 1 GND:Source2
* node 2 VCC:Source1
* node 3 GND:Sink2
* node 4 VCC:Sink1
```

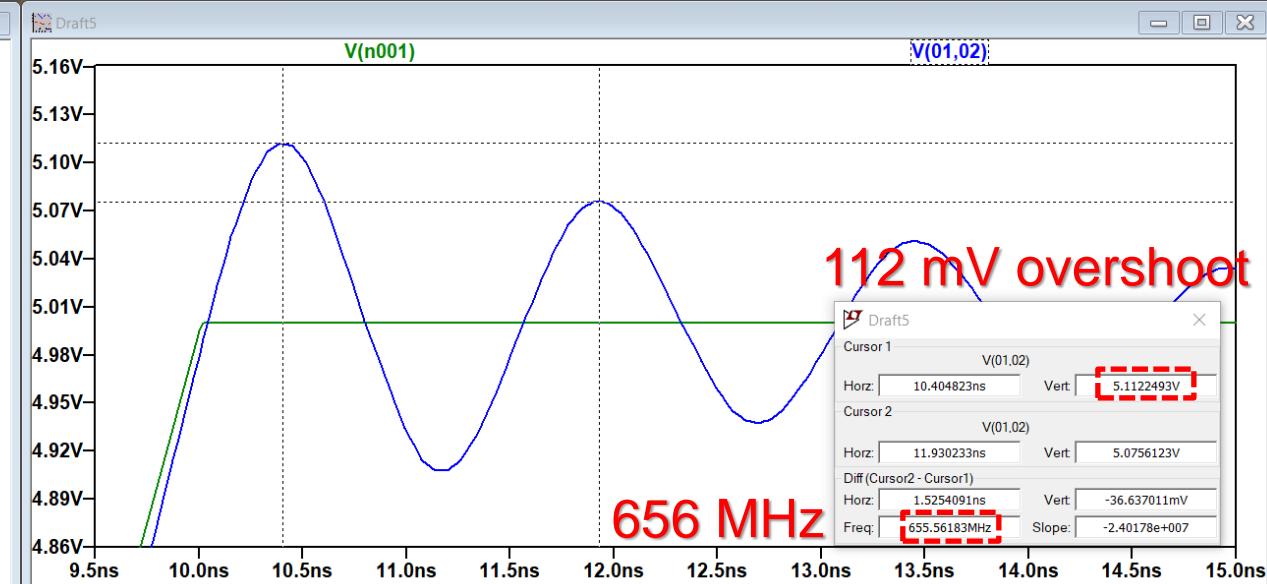
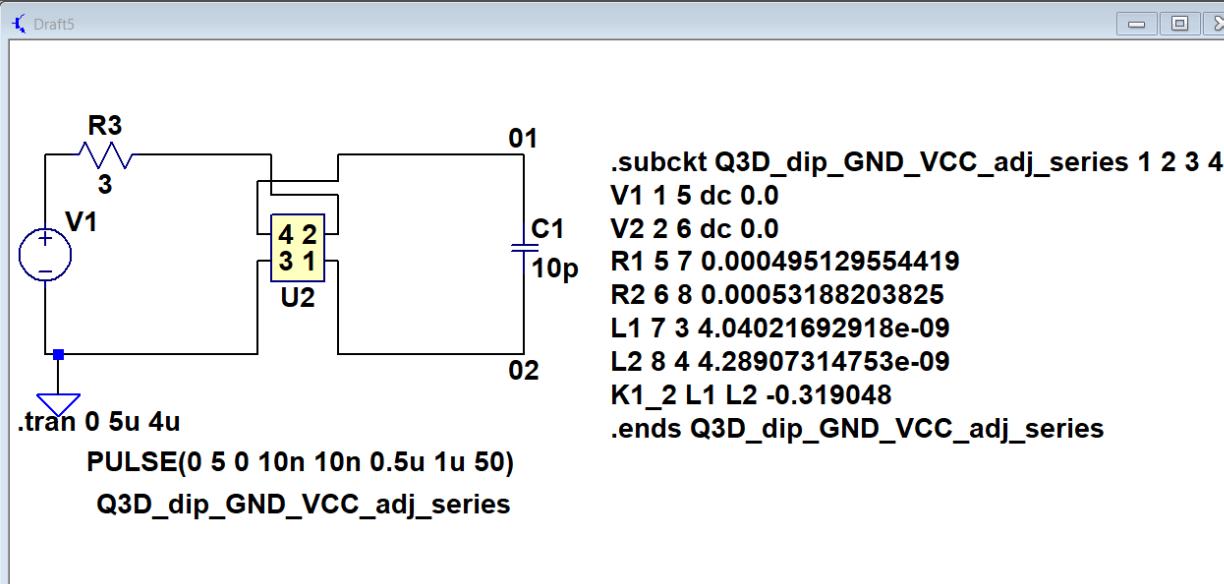
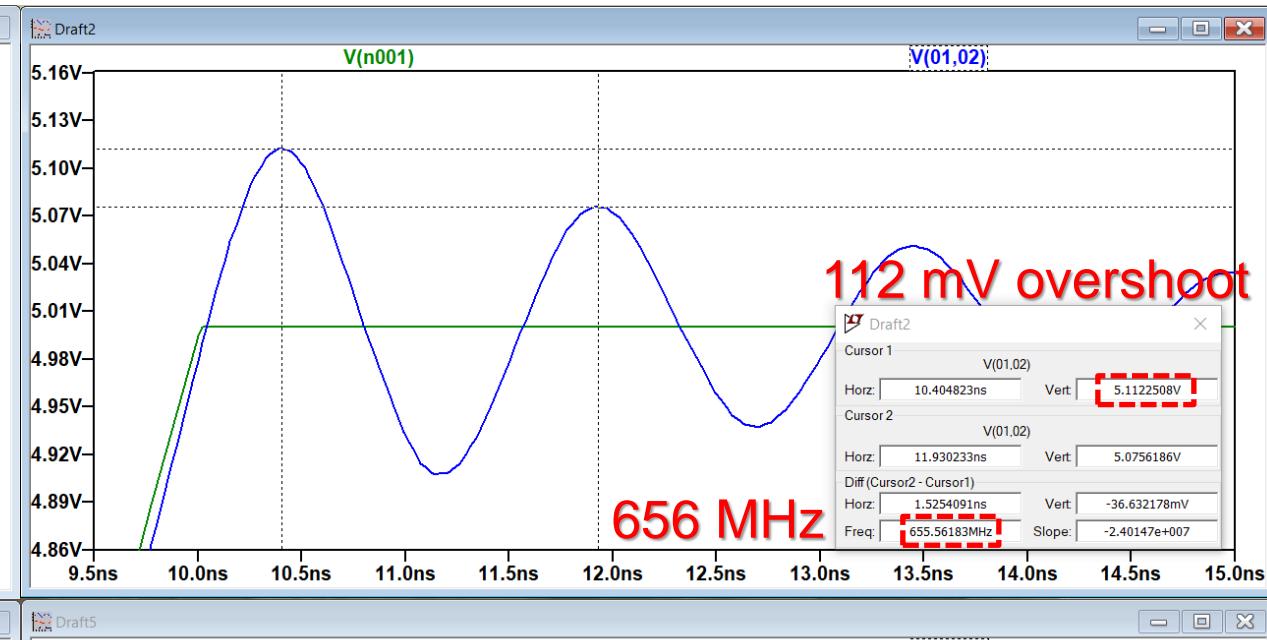
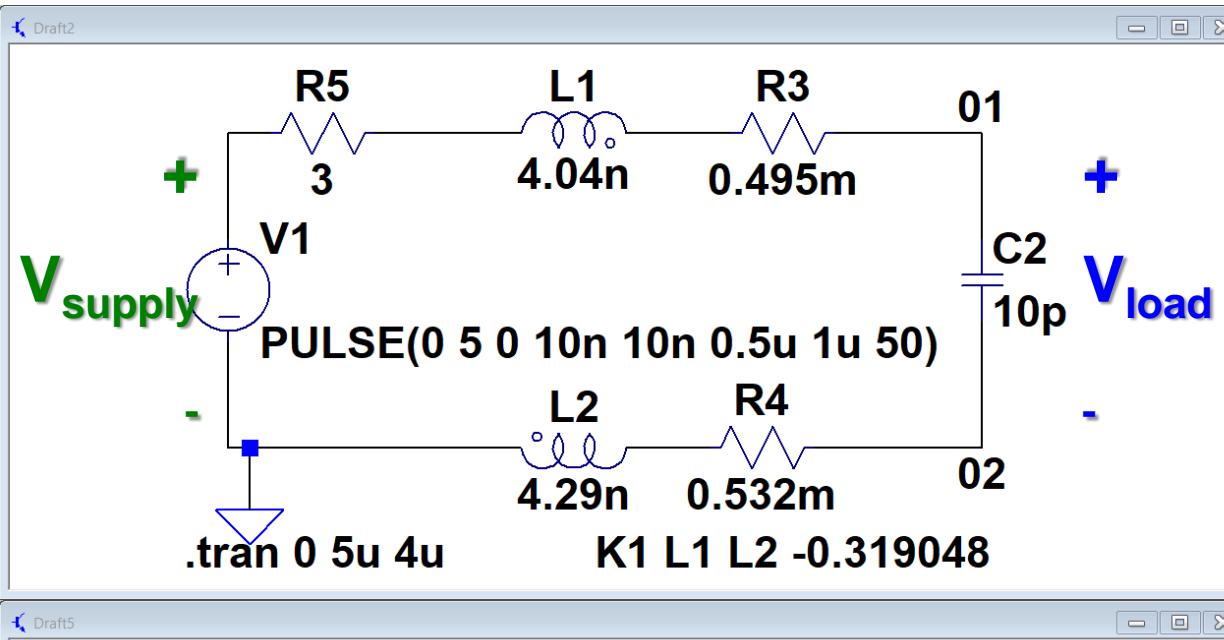


```
.subckt Q3D_dip_GND_VCC_adj_series 1 2 3 4
V1 1 5 dc 0.0
V2 2 6 dc 0.0
R1 5 7 0.000495129554419
R2 6 8 0.00053188203825
L1 7 3 4.04021692918e-09
L2 8 4 4.28907314753e-09
K1_2 L1 L2 -0.319048
.ends Q3D_dip_GND_VCC_adj_series
```

LTspice Simulation



LTspice Simulation: Discrete vs Q3D Subcircuit



Key Points to Remember with ANSYS Q3D

- You must use the VPN to use ANSYS when you are not on the VT campus/network.
- Make components that you do not want to simulate Non-Models by unchecking the Model box.
- When conductors are physically in contact and therefore electrically connected, they are treated as one "net". This is similar to a "node" in LTspice.
- To identify nets or to refresh the nets if you made changes, right click on Nets in the Project Manager panel and click Auto Identify Nets.
- When solving for L or R, each net must have 1 source and 1 sink.
- Sources and sinks can only be 2D faces, they cannot be 3D objects.
- To select faces, click the "F" key on your keyboard. To select objects, click the "O" key on your keyboard.
- To zoom to fit, click Control + D.
- To pan, hold down the Shift key and then click and drag your mouse in the design space.
- To rotate, hold down the Alt key and then click and drag your mouse in the design space.