Lecture 6

Electrical Design

Capacitance

& Intro to ANSYS Q3D

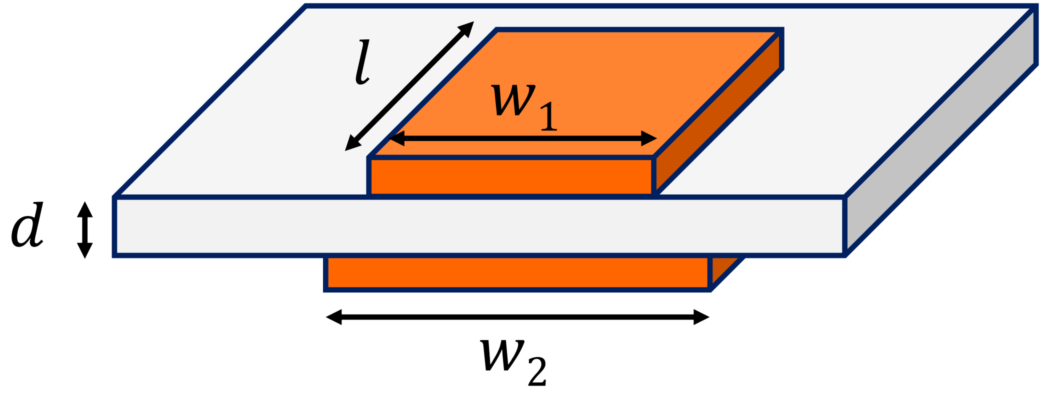
February 6, 2025

Reminders and Announcements

- Office hours: Monday, 3:30pm-4:30pm
- Homework #1 due Monday, Feb. 10th, by 11:59pm (midnight)
  - Reminder: No late assignments will be accepted unless they are approved by the instructor prior to the deadline
- On Tuesday, we will continue the in-class ANSYS Q3D tutorial
  - Bring your laptops with the software installed to class

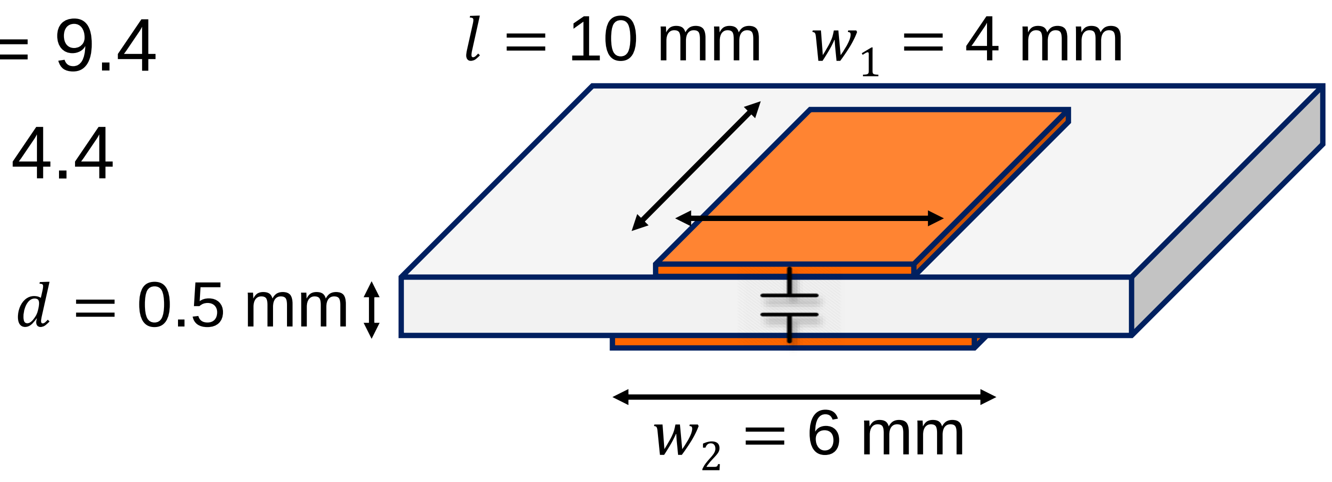
Capacitance (Overlapping Conductors)

- $Q = CV$
- Taking derivative:
  - $I = dQ/dt$
  - $I = C\, dV/dt$
- $C = \varepsilon A/d$
  - $\varepsilon =$ permittivity
    - $\varepsilon = \varepsilon_r \varepsilon_0$
      - $\varepsilon_0 =$ 8.86 x 10^{-12} F/m, permittivity of free space
      - $\varepsilon_r =$ relative permittivity or dielectric constant (material property)
  - $A =$ overlapping area
  - $d =$ distance



Example: Capacitance (Overlapping Conductors)

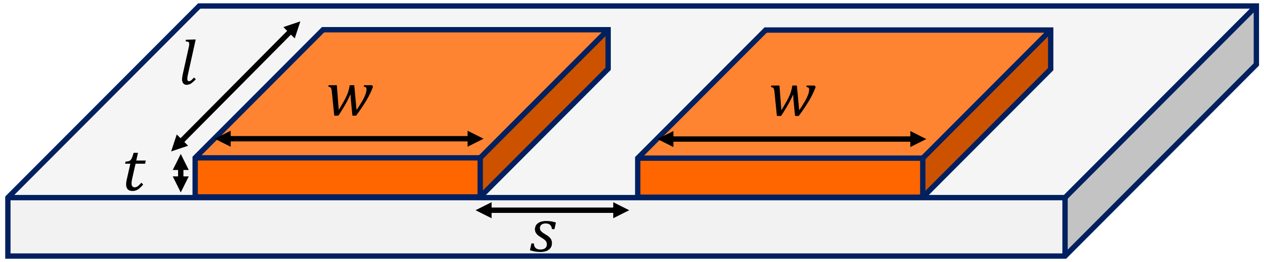
- Al_2O_3 substrate (e.g., DBC): $\varepsilon_r = 9.4$
- FR4 substrate (e.g., PCB): $\varepsilon_r = 4.4$
- $C = \varepsilon A/d = \varepsilon_0 \varepsilon_r A/d$
  - $\varepsilon_0 = 8.86 \times 10^{-12}$ F/m
  - $A = 10$ mm x 4 mm= 40 mm^2
  - $C = (8.86 \times 10^{-12}$ F/m$)(\varepsilon_r)(4 \times 10^{-5}$ m^2) / (0.0005 m)
  - C_{Al2O3} = 6.7 pF (Q3D: 7.7 pF)
  - C_{FR4} = 3.12 pF (Q3D: 3.7 pF)



➢ Substrate materials with higher relative permittivity (dielectric constant) have higher parasitic capacitance

Example: Capacitance (Adjacent Conductors)

- Formula for adjacent conductors with equal widths:
- $C' = 0.122\ t/s + 0.0905\ (1 + \varepsilon_r)a$ [pF/cm]
- $a = \log(1 + 2\ w/s + 2\sqrt{w/s} + w^2 / 200)$
- s = distance between two adjacent conductors, mm
- t = thickness, mm
- w = conductor width, mm
- ε = permittivity
- $C = C'l$
- l = parallel running length, cm



Example: Capacitance (Adjacent Conductors)

- $C' = 0.122\ t/s + 0.0905\ (1+\varepsilon_r)a$ [pF/cm]
- $a = \log\left(1 + 2\ w/s + 2\sqrt{w/s} + w^2 / 200\right)$
- $C = C'l$

Find the capacitance between the adjacent traces.

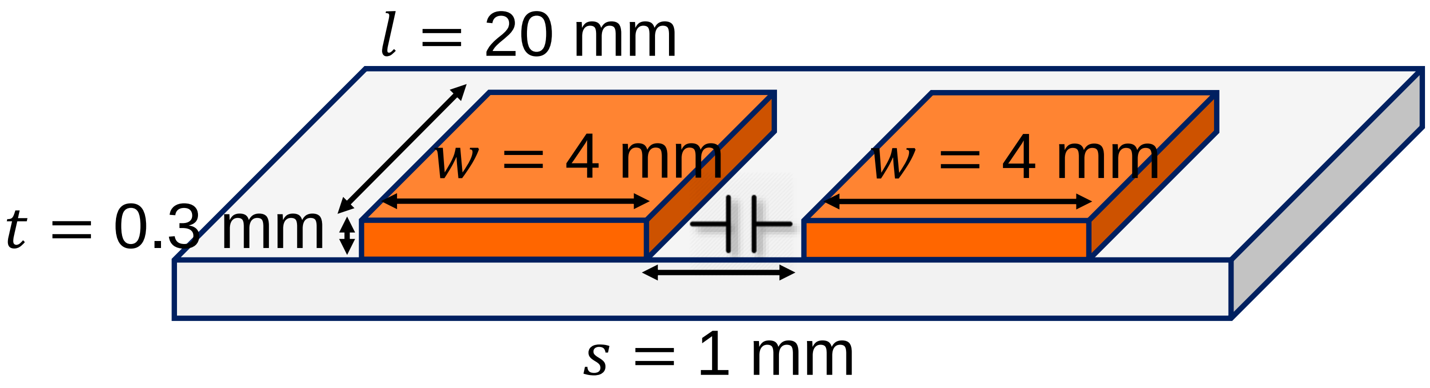
Al_2O_3 substrate (e.g., DBC): $\varepsilon_r = 9.4$

$C' = 1.1$ pF/cm

$C =$ **2.2 pF**

(Q3D: 1.3 pF for $t_{Al2O3} = 1$ mm)

(Q3D: 2.1 pF for $t_{Al2O3} = 5$ mm)



Coupling Capacity vs Spacing

To decrease C:

- Increase spacing between conductors
- Decrease conductor width
- Choose materials with low dielectric constant

➢ These will also impact the L, R, and thermal conductivity

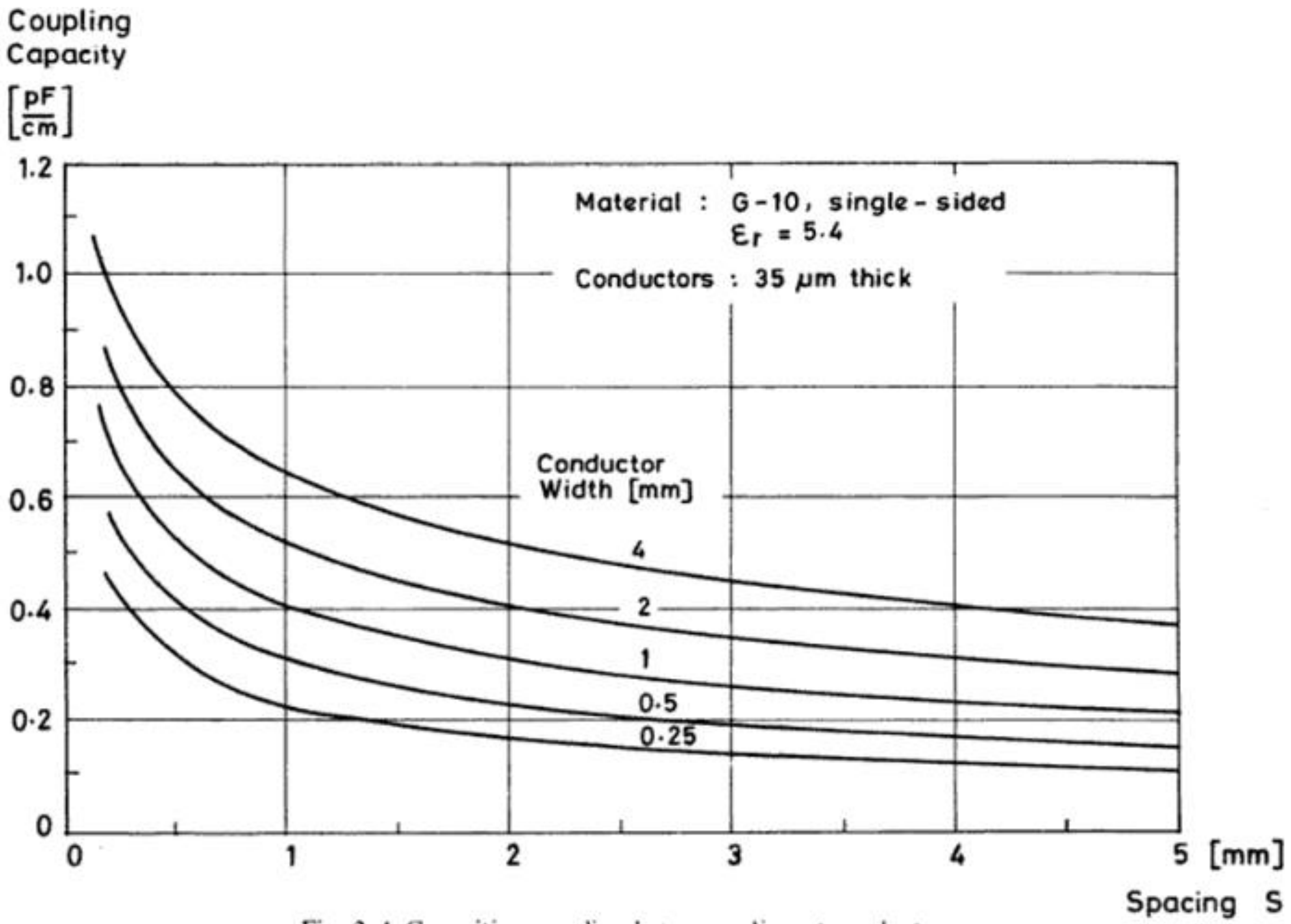
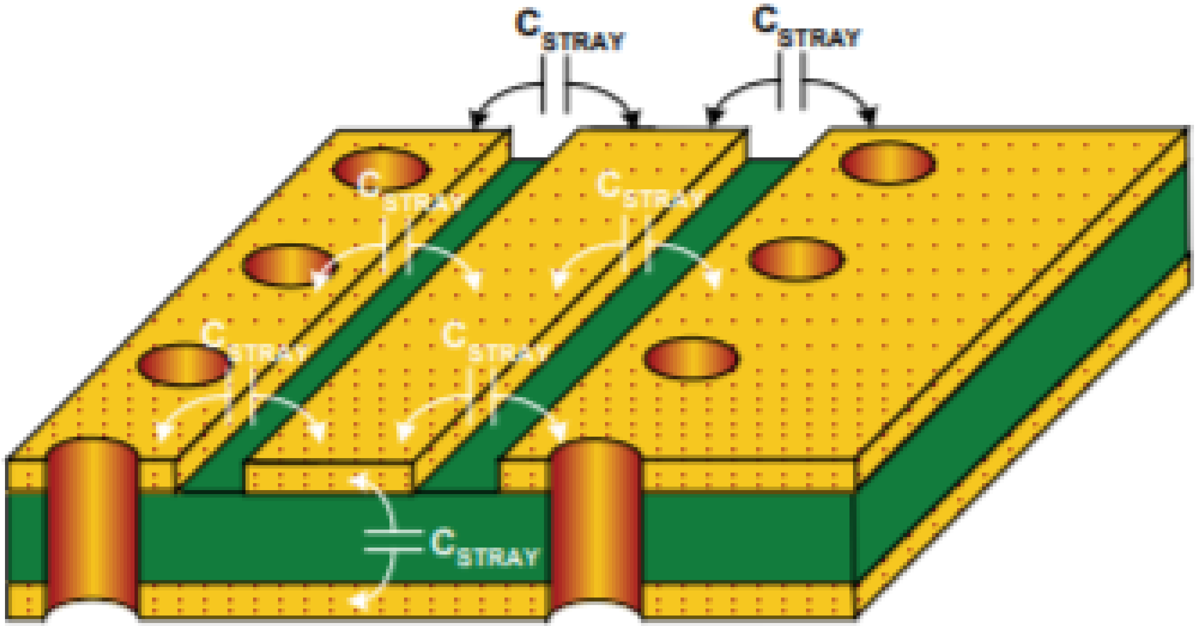


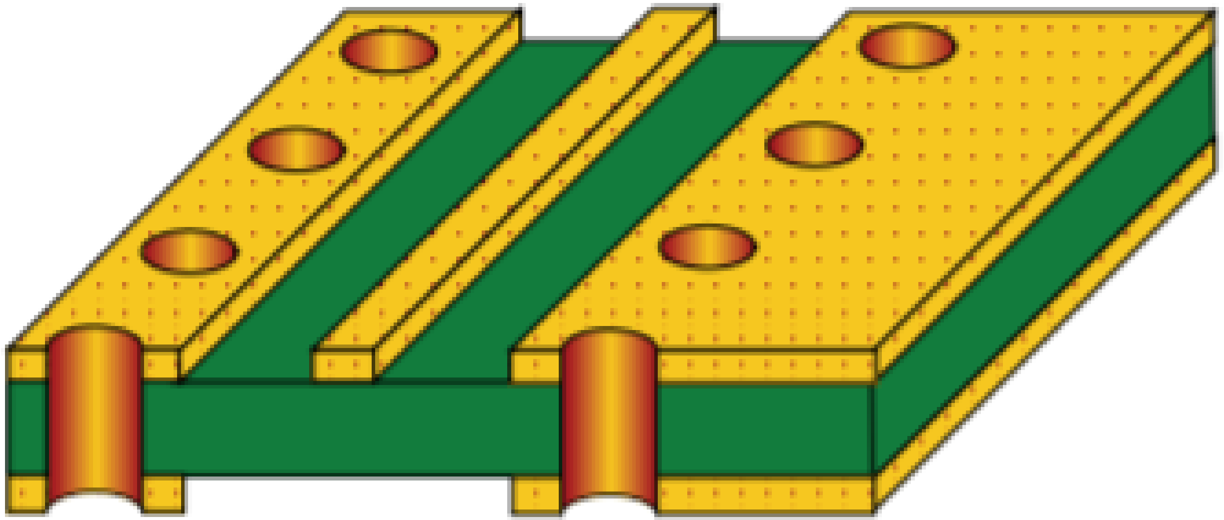
Fig. 2 4 Capacitive coupling between adjacent conductors

High-Capacitance vs Low-Capacitance Layouts

- High parasitic capacitance
  - Wide traces
  - Large overlap area
  - Close adjacent traces



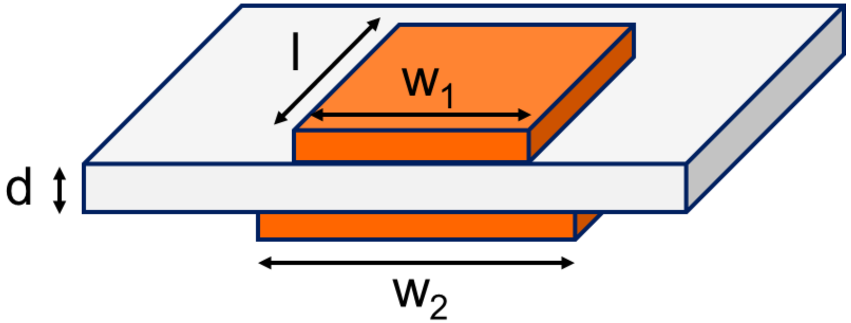
- Low parasitic capacitance
  - Reduced width
  - Eliminate overlap
  - Increase spacing between adjacent traces



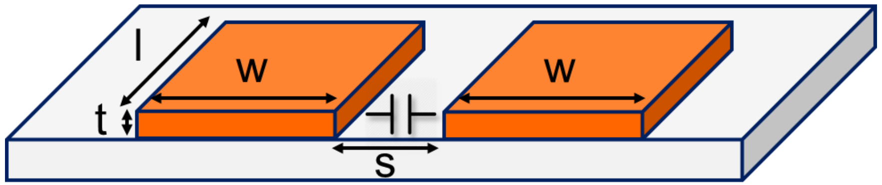
$I = C\, dV/dt$

Summary: Capacitance

- Capacitive delay: $\tau = RC$
- Overlapping conductors:
  - $C = \varepsilon A/d$, where A = overlapping area
  - Decrease by decreasing overlapping area, increasing distance d, or using a material with lower dielectric constant ε_r



- Adjacent conductors:
  - $C' = 0.122\, t/s + 0.0905\, (1 + \varepsilon_r)a$ [pF/cm]
    - $a = \log\left(1 + 2\, w/s + 2\sqrt{w/s} + w^2 / 200\right)$
    - $C = C'l$
  - Decrease by increasing spacing s between conductors, reducing t, w, and l of conductors, or using material with lower ε_r



Summary: Types

- Resistance
  - DC (temperature dependent)
  - AC (skin and proximity effects)
- Capacitance
  - Between overlapping conductors
  - Between adjacent conductors
- Inductance
  - Self/partial inductance
  - Mutual inductance
  - Total/loop/effective inductance

Summary: Consequences

- Resistance
  - Power loss
  - Heating
  - Ground bounce
- Capacitance
  - Delay
  - Noise
  - Oscillation
- Inductance
  - Delay
  - Noise
  - Oscillation
  - Voltage overshoot

Summary: Mitigation Approaches

- Resistance
  - DC – increase conductivity, decrease length, increase area
  - AC – increase circumference/ perimeter, multiple smaller conductors in parallel
- Capacitance
  - Minimize overlapping areas
  - Increase spacing between traces/interconnects
  - Low dielectric constant
- Inductance
  - Reduce loop area
  - Decrease conductor length
  - Decrease spacing between the source and return paths
  - Increase spacing between conductors with same current direction
  - Use decoupling capacitors
  - Arrange conductors perpendicular to minimize unwanted coupling

Finite Element Analysis (FEA)

- Take a complex problem
- Break it into small pieces (a <u>finite</u> number of <u>elements</u>)
- Simplify each piece (simple relationships)
- Re-assemble the pieces (matrix equations)
- Solve the problem (matrix manipulation)

Parasitic Extraction

- The calculation of the parasitic effects: parasitic capacitances, parasitic resistance, and parasitic inductances
- The purpose is to create an accurate analog model of the circuit, so that the simulations better-emulate the circuit behavior
- Behaviors of interest include delay and rise times, oscillations, overshoots, crosstalk, and EMI
- Tools:
  - ANSYS Q3D Extractor (used in this course)
  - FastCap and FastHenry (free tool from MIT)

Package Equivalent Circuit

Physical Package Structure → Equivalent Electrical Circuit

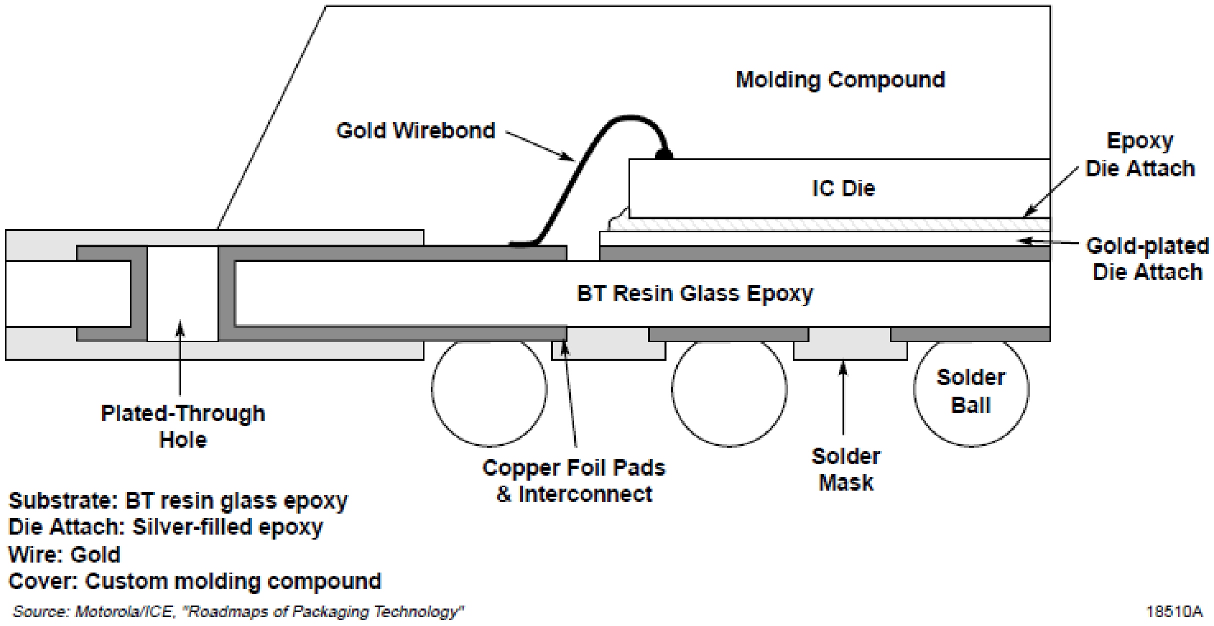


Figure 7-3. OMPAC Ball Grid Array From Motorola

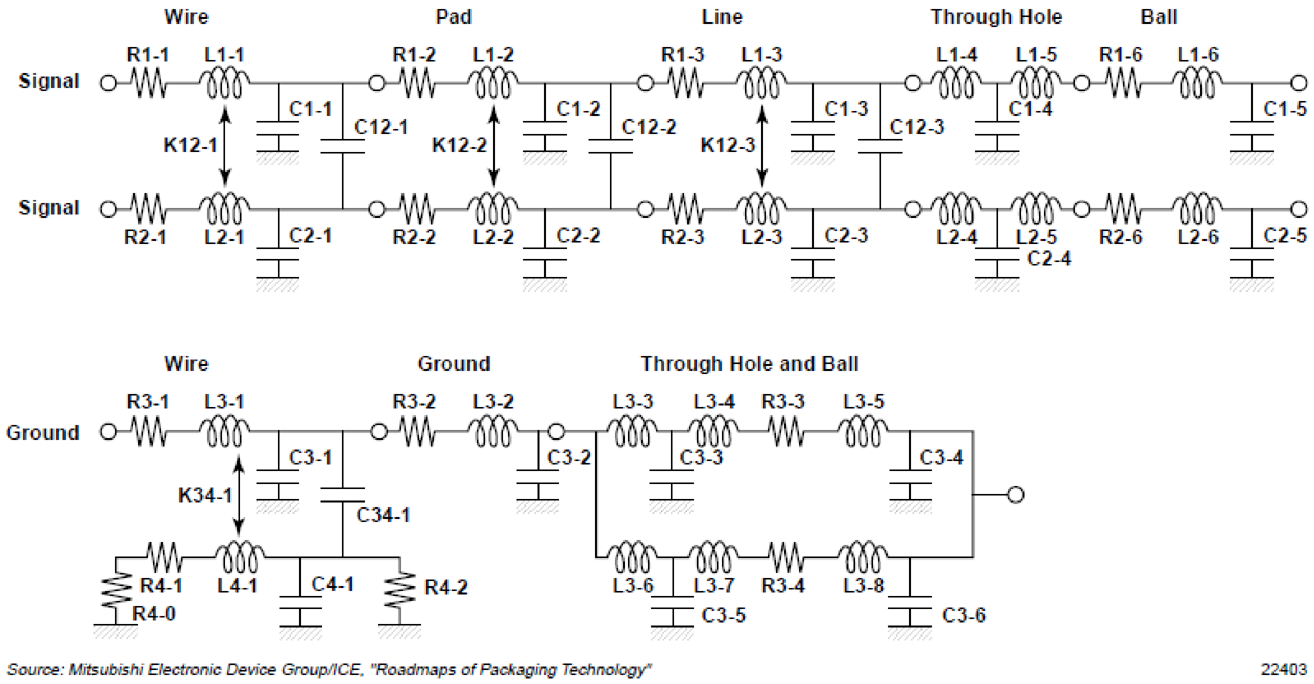
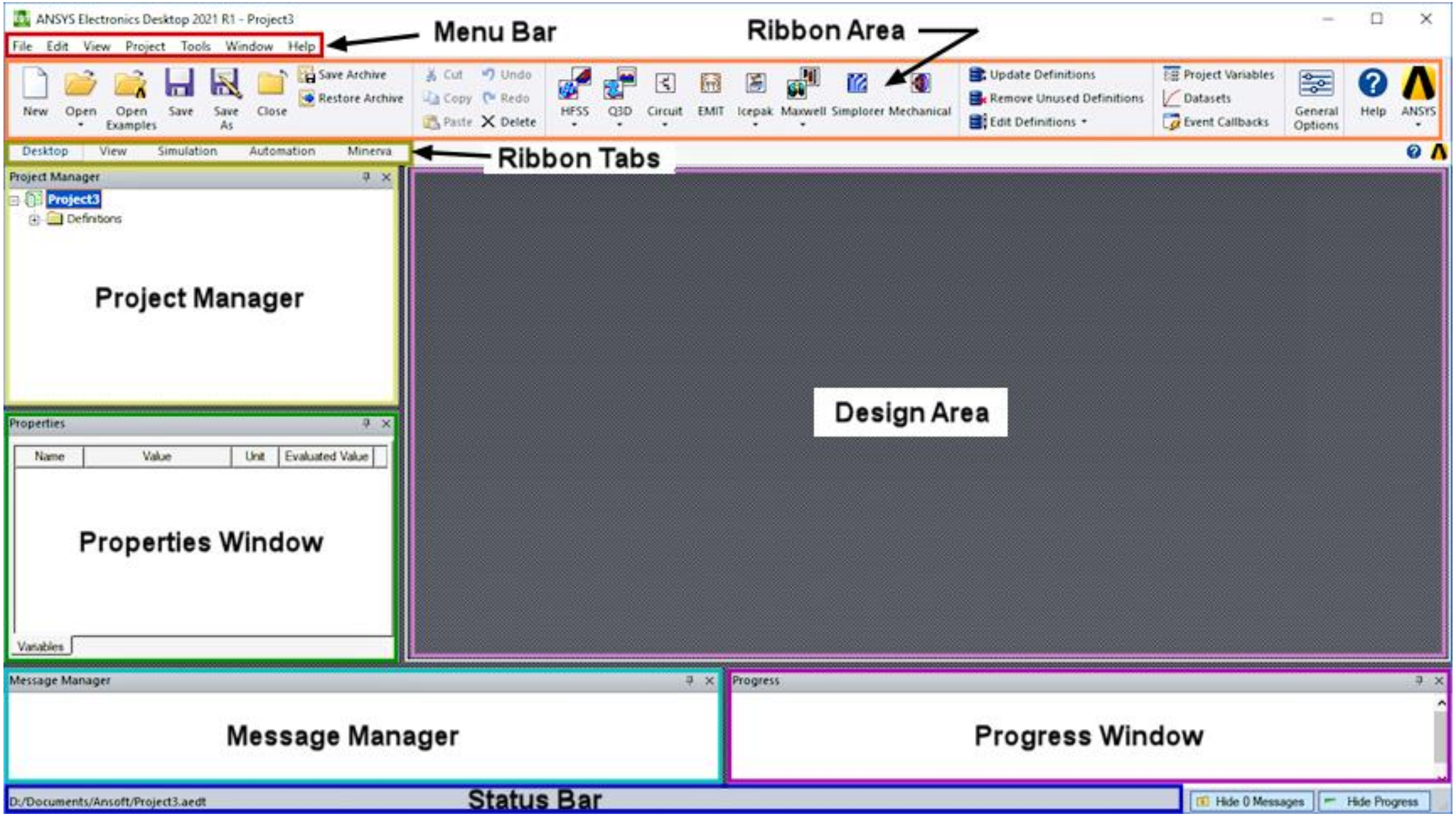


Figure 7-4. The Equivalent Schematic for a BGA Package for Adjacent Signal to Signal Lines and for Ground Lines

ANSYS Electronics Desktop Overview



ANSYS Q3D Extractor

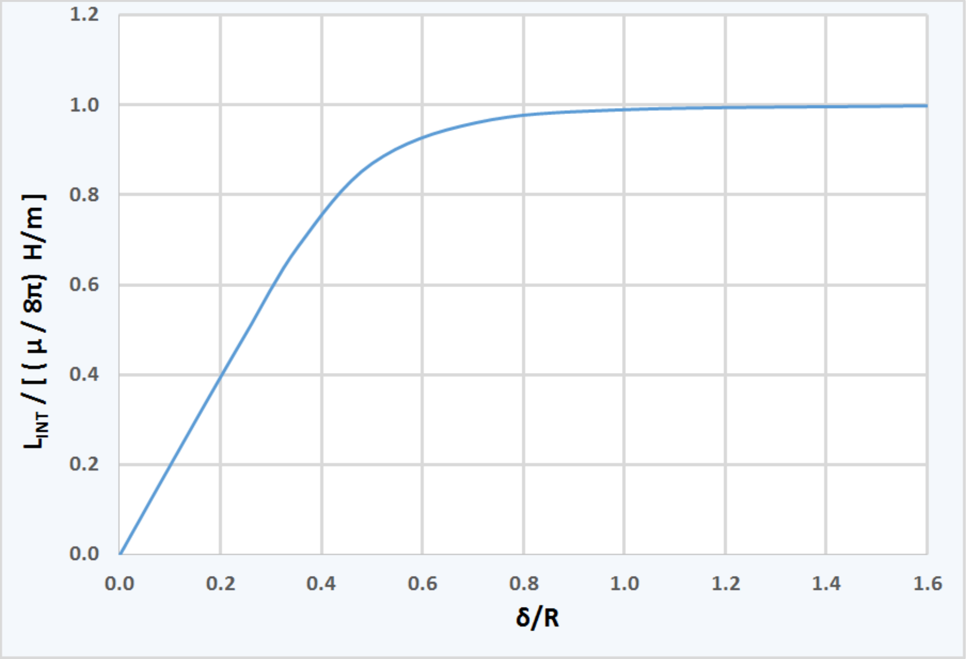
- Quasi-static 3D electromagnetic field analysis
- Uses method of moments (MoM)
  - MoM: solves integral form of Maxwell's equations
- Uses fast multipole method (FMM) to accelerate the solution of the integral equation
- Results include:
  - Proximity effect
  - Skin effect
  - Dielectric and ohmic loss
  - Frequency dependencies
- Extracts lumped RLGC parameters and spice models
  - R = resistance (DC and AC)
  - L = inductance (DC and AC)
  - G = conductance
  - C = capacitance

https://www.ansys.com/products/electronics/ansys-q3d-extractor/q3d-extractor-capabilities

ANSYS Q3D Extractor: Resistance

- DC resistance
  - Resistance under DC
  - Independent of frequency
- AC resistance
  - Assumes skin effect is well developed
  - Depends on frequency
- Q3D can add the two when exporting the equivalent circuit
  - “Add DC and AC Resistance”

ANSYS Q3D Extractor: Inductance



- DC inductance
  - No skin effect considered
  - Independent of frequency

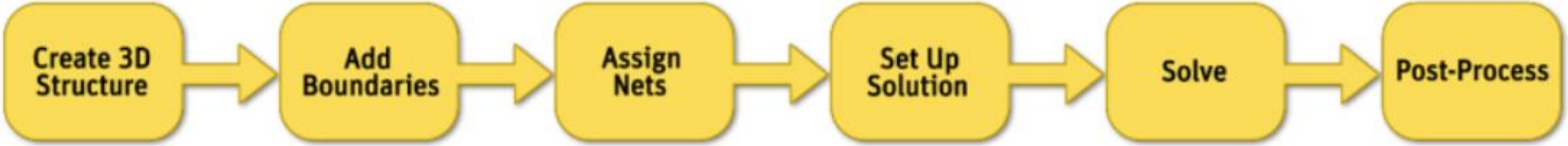
- AC inductance
  - Assumes skin effect is well developed
  - Depends on frequency
  - Self-inductance of the conductor decreases as skin depth decreases (as frequency increases)

ANSYS 2D Extractor

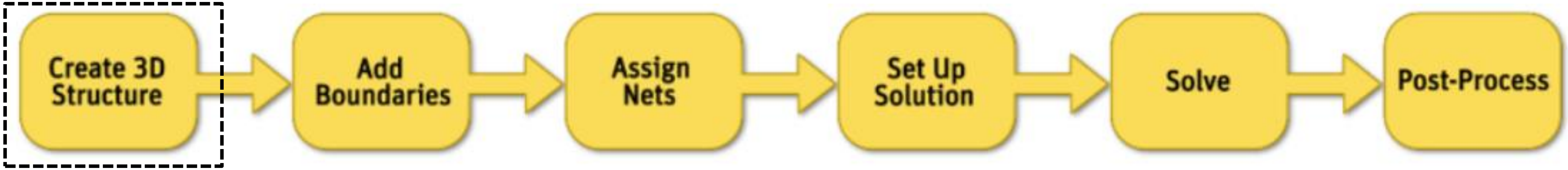
- Quasi-static 2D electromagnetic field analysis
- Used for cables and transmission lines
- Uses finite element method (FEM)
  - Finite element method: divides the system into smaller, simpler parts (finite elements, mesh)
- Results include:
  - Per-unit-length R, L, C, G parameters of transmission lines
  - Characteristic impedance Z_0 matrices
  - Propagation delay
  - Crosstalk

https://www.ansys.com/products/electronics/ansys-q3d-extractor/q3d-extractor-capabilities

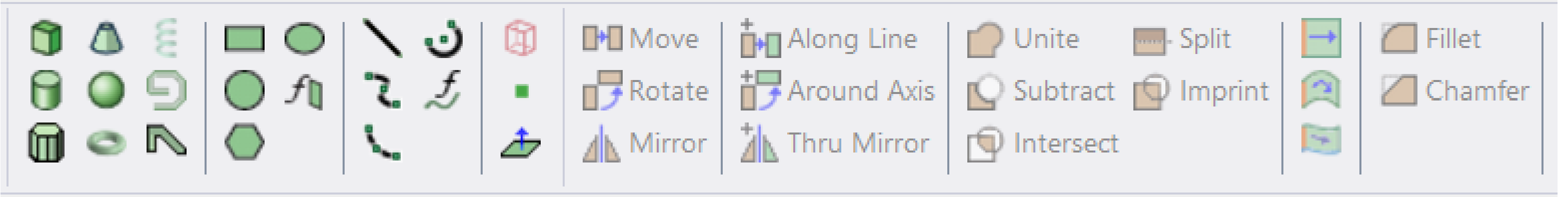
ANSYS Q3D Process Flow



1. Create 3D Structure

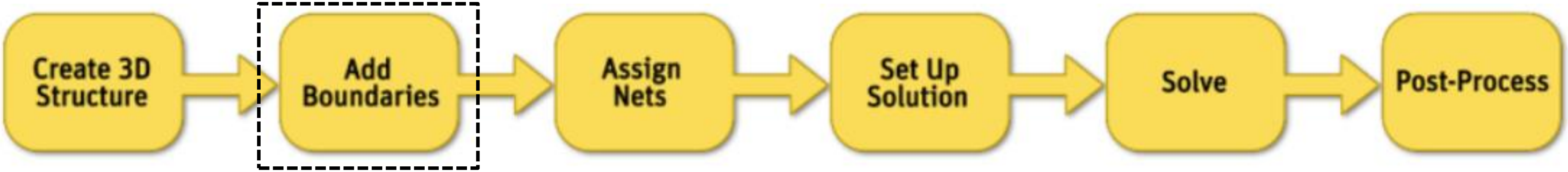


- After you insert a design into the project, you can draw/import a model of the structure to be analyzed
- You can draw the 3D object using the modeler’s Draw commands



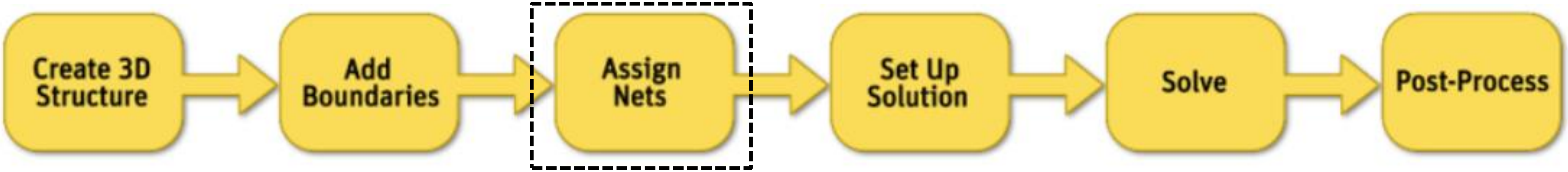
- You can import 3D models
  - Modeler → Import
  - .step file is recommended

2. Add Excitations



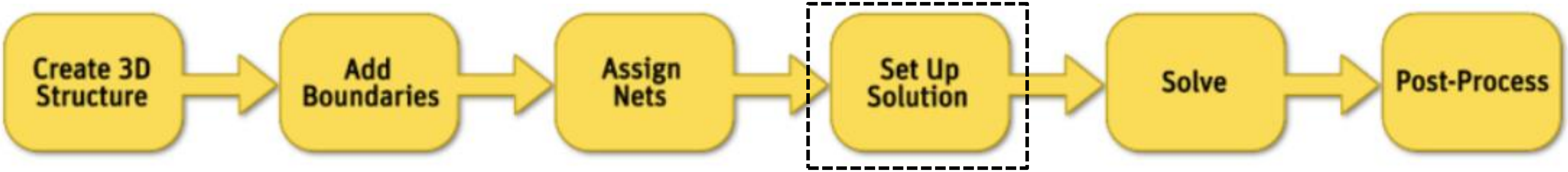
- Assign excitations
  - Select object face (press ‘F’ key) → Right-click → Assign Excitation
  - Types of excitations: source, and sink
    - The sink collects the current injected at the source
    - Required for L and R simulations (not needed for C)
- Boundaries
  - Do not need to be assigned
  - Types of boundaries: infinite ground plane, and thin conductor

3. Assign Nets

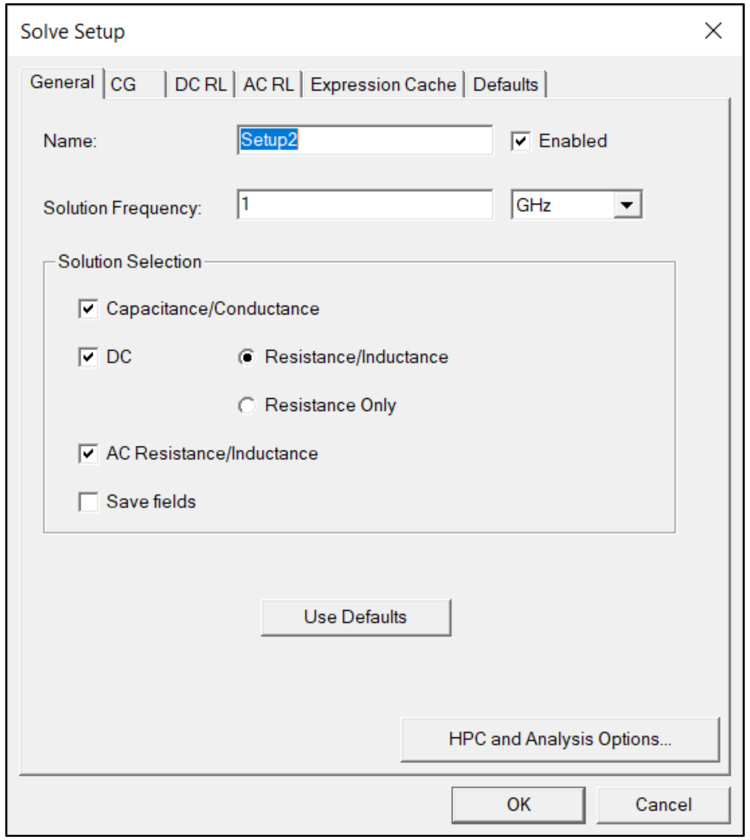


- A net is a collection of touching conductors
- Nets can only be assigned to conductive materials
- Nets can be automatically identified
    - Right-click on Nets → Auto Identify Nets
- Nets can be assigned
    - Right-click on Nets → Assign Net
    - Types of nets: signal, floating, ground

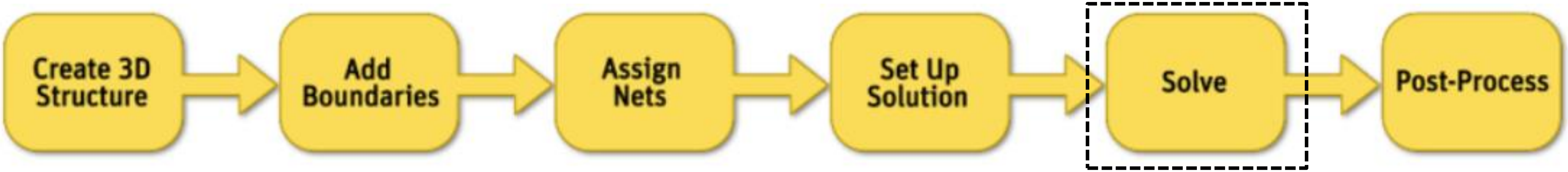
4. Set Up Solution



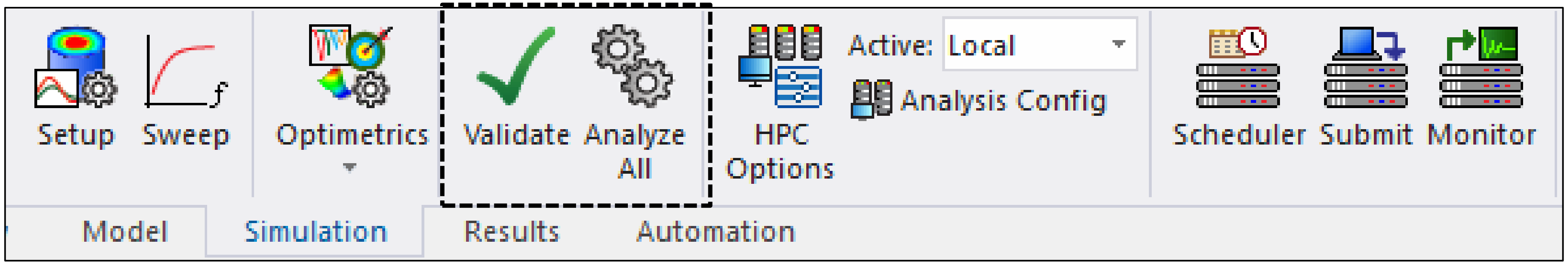
- Solution setup includes:
  - General data about the solution’s generation
    - Solution frequency
    - Solution selection (CG, DC RL, AC RL)
  - Adaptative mesh refinement parameters
- Solution setup must be added to run the analysis
  - Right-click Analysis → Add Solution Setup



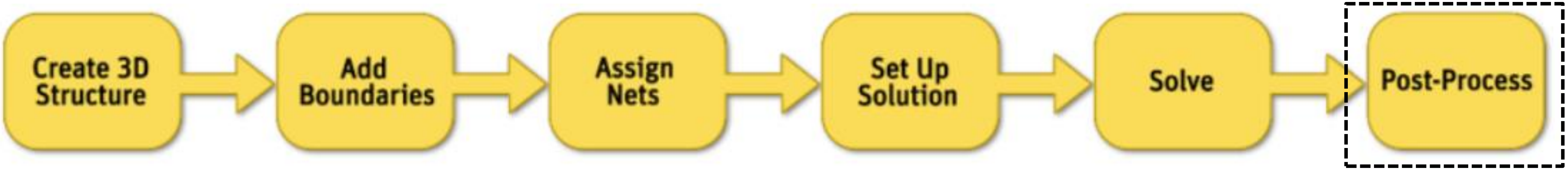
5. Solve



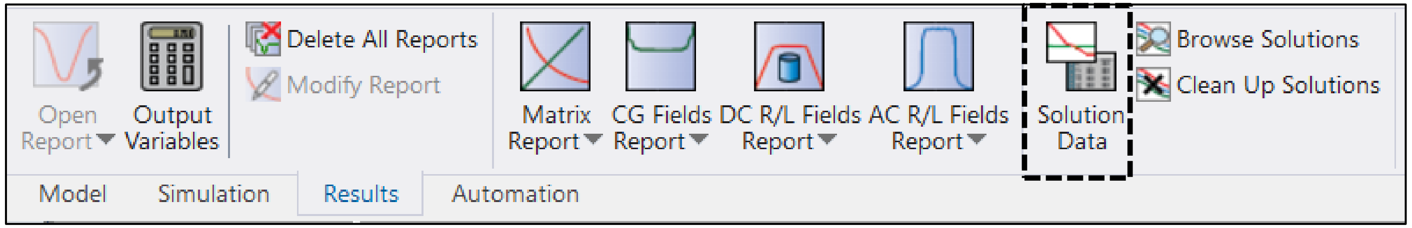
- Validate setup
  - Simulation tab → Validate
- Solve
  - Simulation tab → Analyze All



6. Post Process



- View solution data
  - Convergence information, computing resources used, matrices during each adaptive
- View analysis results
  - Results tab → Solution Data
- Plot field overlays
- Create 2D or 3D reports
- Plot the finite element mesh



ANSYS Help

- [Q3D Extractor Help]