VIRGINIA TECH

Lecture 5

Electrical Design

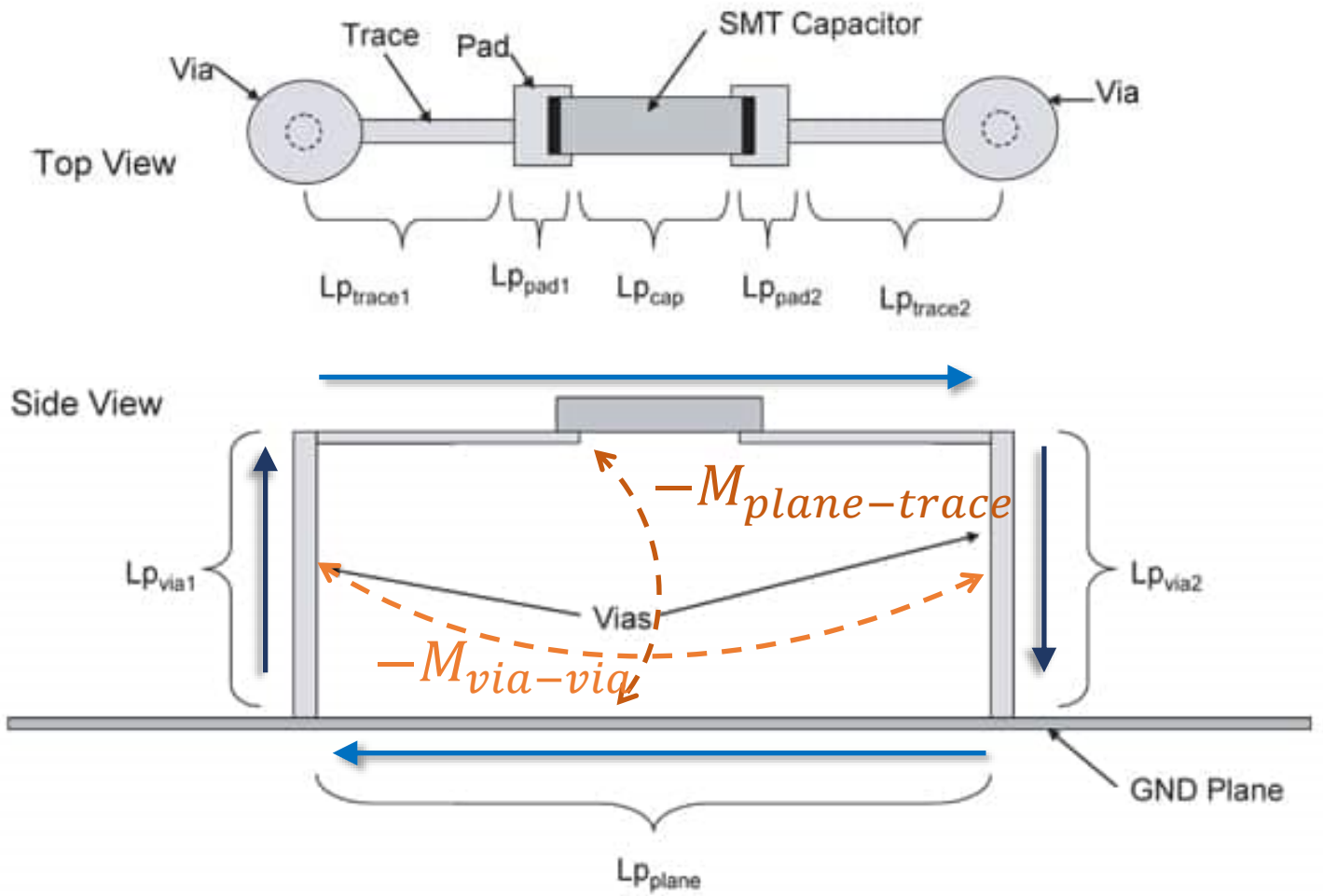
Inductance & Capacitance

February 4, 2025

Reminders and Announcements

- Office hours: Wednesday, 3:30pm-4:30pm
- Homework #1 due Monday, Feb. 10th, by 11:59pm (midnight)
  - Reminder: No late assignments will be accepted unless they are approved by the instructor prior to the deadline
- Download and install ANSYS Electronics Desktop and LTspice and check that you can open them by Thursday
- On Thursday, we will do an in-class ANSYS Q3D tutorial
  - Bring your laptops with the software installed to class

Example: Capacitor Mounted to PCB



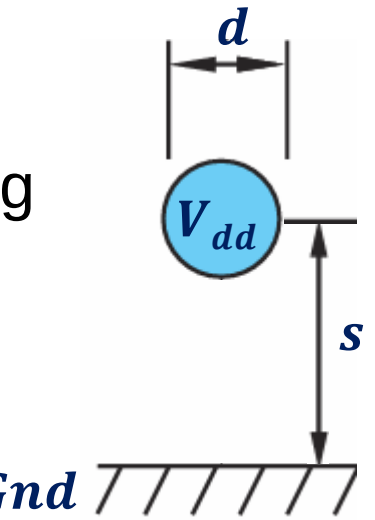
L_p = partial inductance
M = mutual inductance of parallel components

$$L_{total} = Lp_{trace1} + Lp_{pad1} + Lp_{cap} + Lp_{pad2} + Lp_{trace2} + Lp_{via2}$$
$$+Lp_{plane} + Lp_{via1} - 2M_{via-via} - 2M_{plane-trace}$$

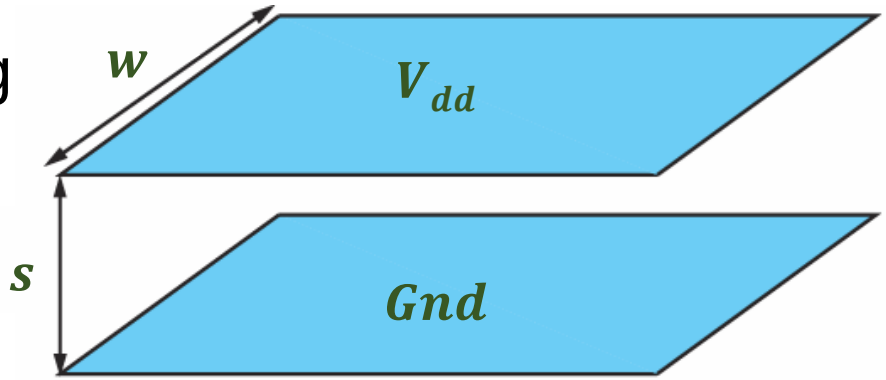
Effective Inductances for Different Structures

*Note: Tummala textbook 2nd Ed. shows 4π in the denominator, which is incorrect.

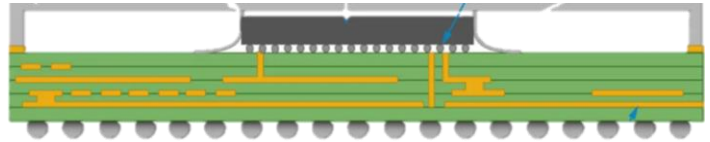
- Wire above a ground plane
  - $L_{eff} = \frac{\mu l}{2\pi^*}\cosh^{-1}\left(\frac{2s}{d}\right)$, where l= length, d= diameter, s= spacing
  - Package examples: TAB, QFP w/ ground plane
  - Typical inductance range: 1 – 10 nH
  - Assumes $s \ll l$, and $d \ll s$



- Parallel planes
  - $L_{eff} = \frac{\mu l s}{w}$, where l= length, w= width, s= spacing
  - Package examples: PGA, BGA
  - Typical inductance range: 0.25 – 1 nH
  - Assumes $s \ll l$

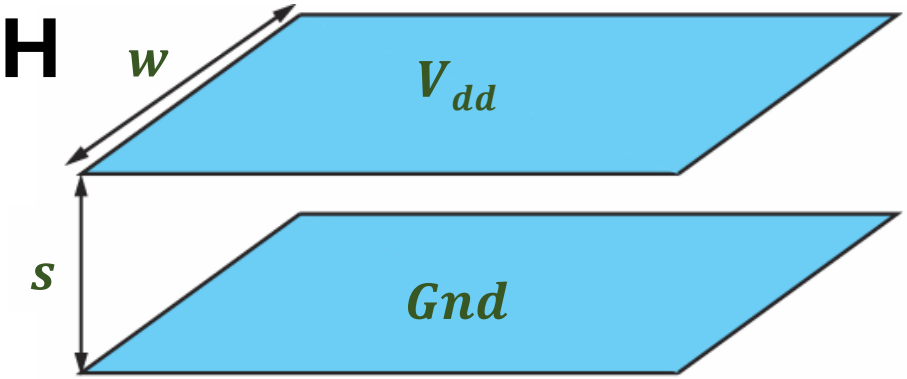


Example: Parallel Planes



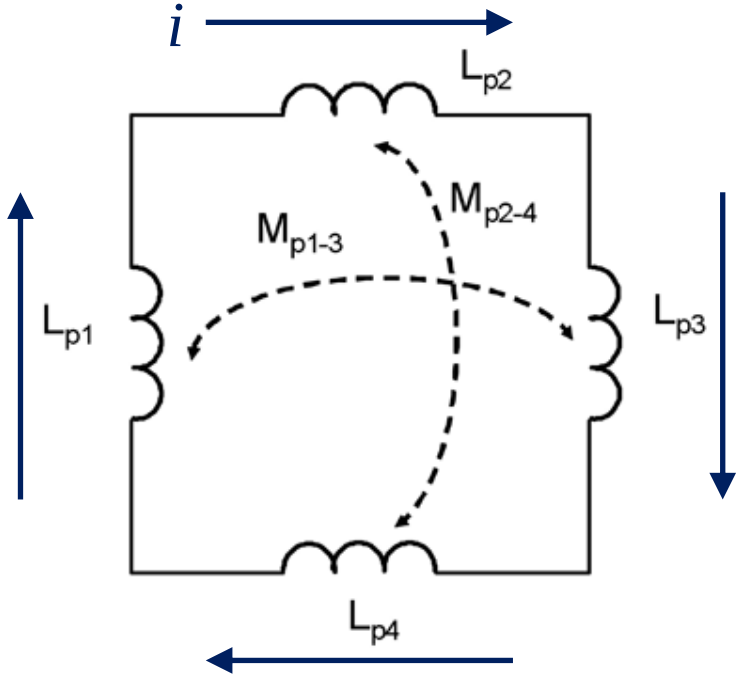
A multi-layer ball grid array (BGA) package has plane layers used to supply both the V_{dd} and the ground (GND). Find the effective inductance for a pair of planes with dimensions of 1 cm by 1 cm, and a spacing of 6 mils.

- $L_{eff} = \frac{\mu l s}{w}$, where $l = w =$ 1 cm = 0.01 m, $s =$ 6 mils = 1.5e-4 m
- $\mu = \mu_0 \mu_r \approx 4\pi \times 10^{-7}\text{H/m}$ =1.26e-6 H/m
- L_{eff} =(1.26e-6 H/m)(1.5e-4 m) = **0.19 nH**



$V = L\,dI/dt$

Summary: Inductance

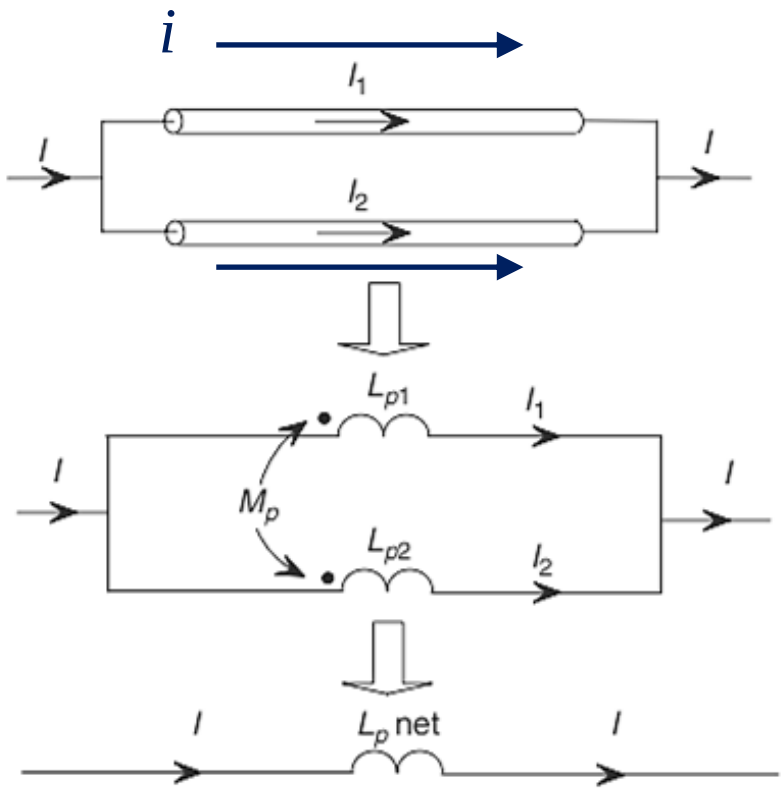


- Inductive delay: $\tau = L/R$
- Self inductance: L_p
  - Example: $L_{p1},\ L_{p2},\ L_{p3},\ L_{p4}$
- Mutual inductance: M
  - Example: $-M_{p1-3}$, $-M_{p2-4}$
  - Subtractive: current flowing in opposite directions (this example)
- Loop inductance: L_{total}
- Example: $L_{total} = L_{p1} + L_{p2} + L_{p3} + L_{p4} - 2M_{p1-3} - 2M_{p2-4}$

$V = L\, dI/dt$

Summary: Inductance

- Example 2: Additive
  - Two parallel wires with current in the same direction
  - Self inductance: $L_{p1},\ L_{p2}$
  - Mutual inductance: M
    - Positive
    - If $s << l$: $M = \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{s}\right) - 1\right]$
  - Total inductance if $L_{p1} = L_{p2}$:
    - $L_{parallel} = (L_p + M)\ /\ 2$



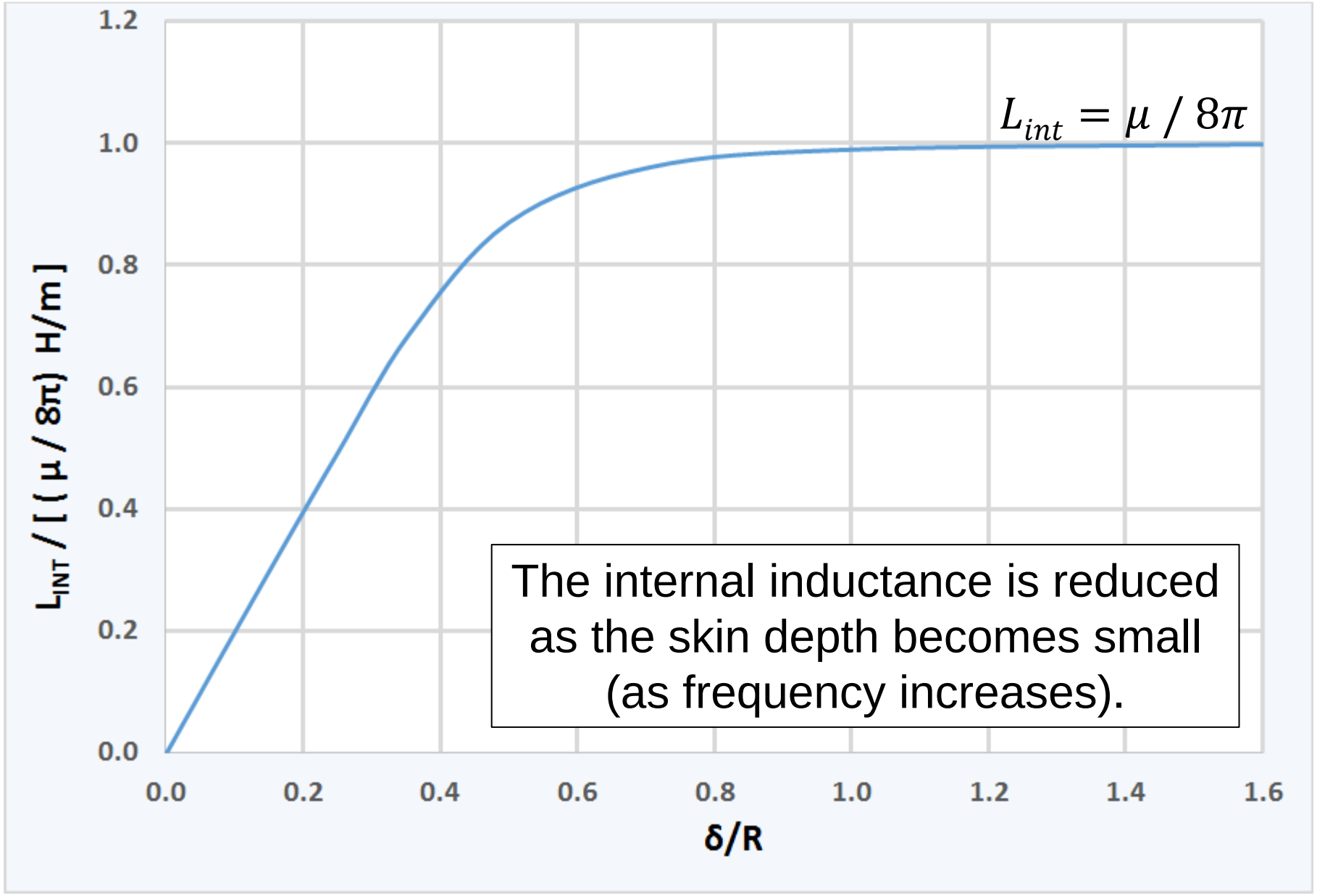
References on Inductances

- F. W. Grover, “Inductance calculations: working formulas and tables,” https://nvlpubs.nist.gov/nistpubs/bulletin/08/nbsbulletinv8n1p1_A2b.pdf
- Xiaoning Qi, “High frequency characterization and modeling of on-chip interconnects and RF IC wire bonds,” http://www-tcad.stanford.edu/tcad/pubs/theses/qi.pdf
- Clayton R. Paul, “Partial and internal inductance,” https://ieeexplore.ieee.org/document/6507331
- Eric Bogatin, “Roadmaps of packaging technology,” Chapter 7: Electrical Performance, ISBN: 1-877750-61-1, 1997.

Skin and Proximity Effects

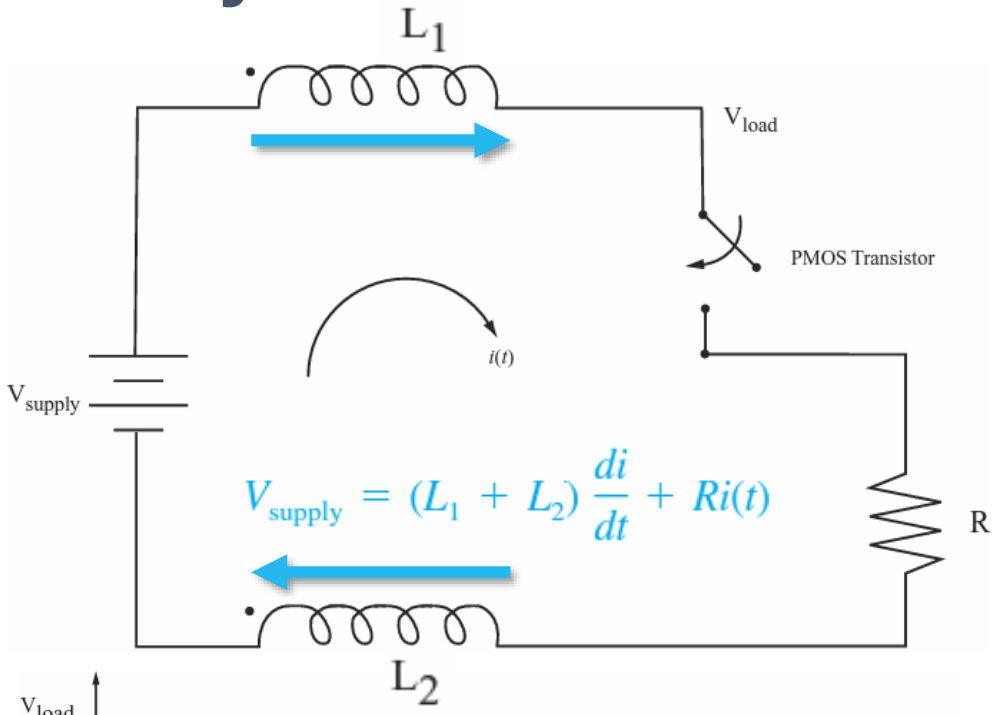
- Skin effect reduces the *internal* wire inductance at high frequencies
- Internal inductance is due to the internal magnetic flux of a conductor
- Internal inductance is typically much less than the external inductance, which is due to external magnetic flux
- Proximity effect reduces the wire inductance by redistributing the currents to form a smaller current loop
- The skin and proximity effect eddy currents superimpose to form the total eddy current distribution

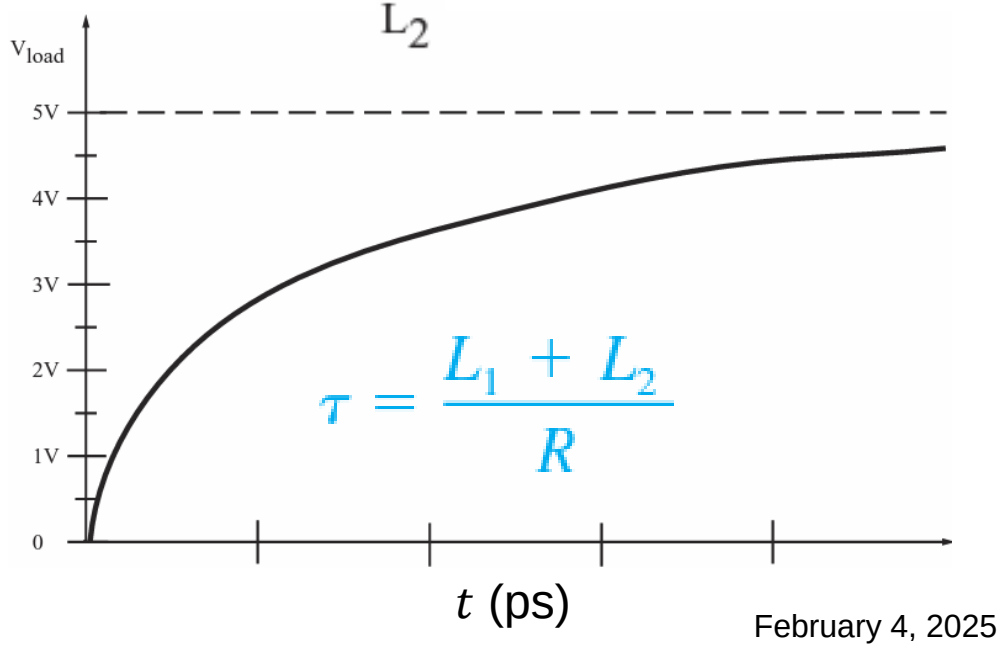
Internal Inductance vs. Skin Depth/Radius



Example: Inductive Delay

- Assume a 5 V supply is feeding a 50 Ω load. The source and return paths between the supply and the load each have 5 nH parasitic inductance. What is the time constant caused by the parasitic inductance?
- $V_{dd} = 5$ V, $R = 50\ \Omega$, $L_1 = L_2 = 5$ nH
- $L_{total} = 5$ nH + 5 nH = 10 nH
- $\tau = L_{total}/R = 10$ nH / 50 Ω = **0.2 ns**
- It will take 0.2 ns for the load voltage to reach 3.2 V (63 % of the applied voltage)

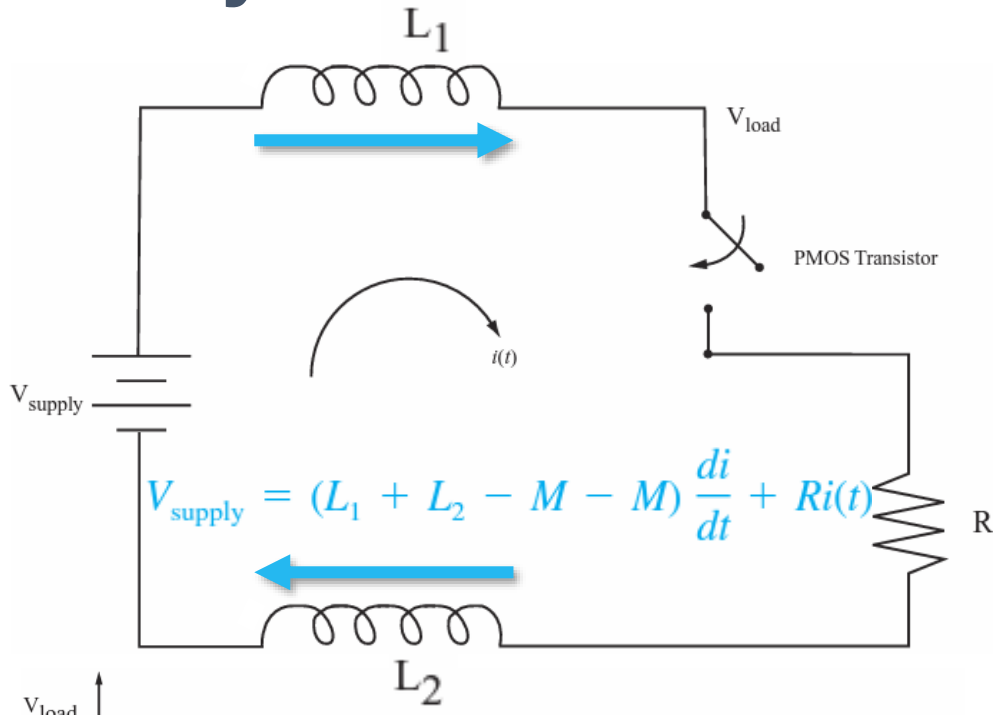


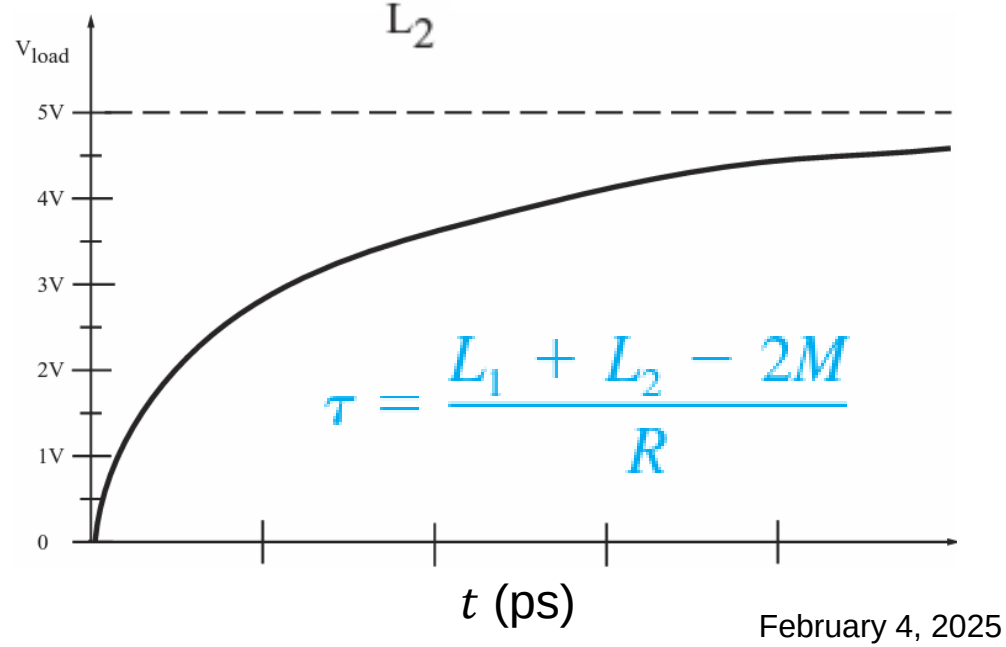


Example: Inductive Delay

- Assume that the source and return paths are close enough such there is 2 nH of mutual inductance between them.
- $V_{dd} = 5$ V, $R = 50\ \Omega$, $L_1 = L_2 = 5$ nH, $\boldsymbol{M = 2}$ **nH**
- $L_{total} = (2)(5\text{ nH}) - (2)(2\text{ nH}) = 6$ nH
- $\tau = L_{total}/R = 6\text{ nH} / 50\ \Omega =$ **0.1 ns**

➢ Subtractive M reduces L_{eff} and τ





dI/dt or ΔI Noise

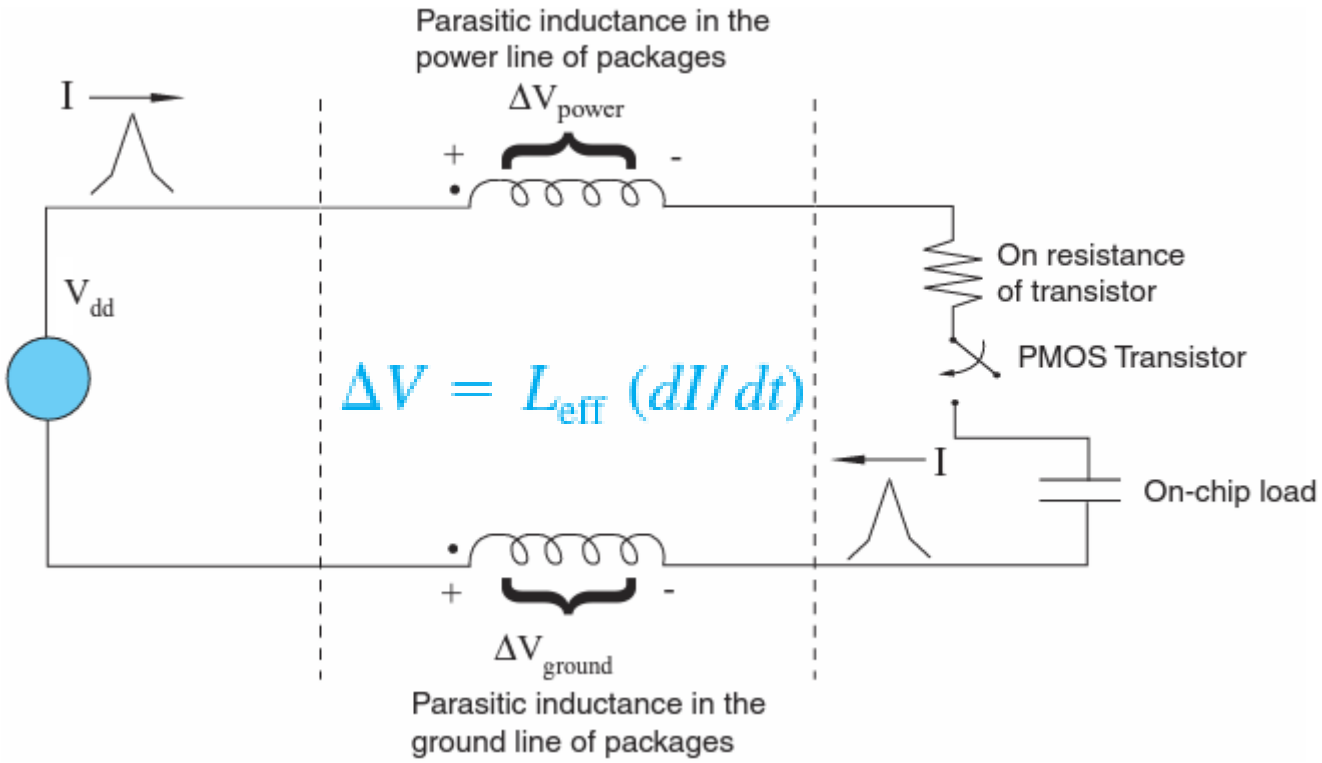
- Transient currents (through interconnects, leads, traces) cause voltage fluctuations on power supply rails due to parasitic inductances
- This is *simultaneous switching noise (SSN)* or dI/dt noise or ΔI noise
- Required charge to energize load to supply voltage V_{dd}: $Q = C \cdot V_{dd}$
- Current draw: $\Delta I = C \cdot V_{dd} / \Delta t$
- If there are N gates switching simultaneously, the current draw from the power supply becomes $\Delta I = N \cdot C \cdot V_{dd} / \Delta t$
- $\Delta V = L\left(\frac{dI}{dt}\right) \rightarrow \Delta I = \Delta V \cdot \Delta t / L_{max}$
- Maximum acceptable inductance: $L_{max} = \Delta t^2 \cdot \Delta V / (N \cdot C \cdot V_{dd})$

Example: dI/dt Noise

- A power supply is supplying 5 CMOS chips with 1 pF load each and a switching time of 1 ns. What is the maximum allowable parasitic inductance L_{max} between the power supply and the chips to achieve a variation in the power supply voltage V_{dd} of ≤ 1 %?
- $L_{max} \leq \Delta t^2 \, \Delta V \; / \; N \; C \; V_{dd}$
- $L_{max} \leq (1\text{ ns})^2(0.01)(V_{dd}) \; / \; ((5)(0.001\text{ nF})V_{dd}) = \mathbf{2\text{ nH}}$

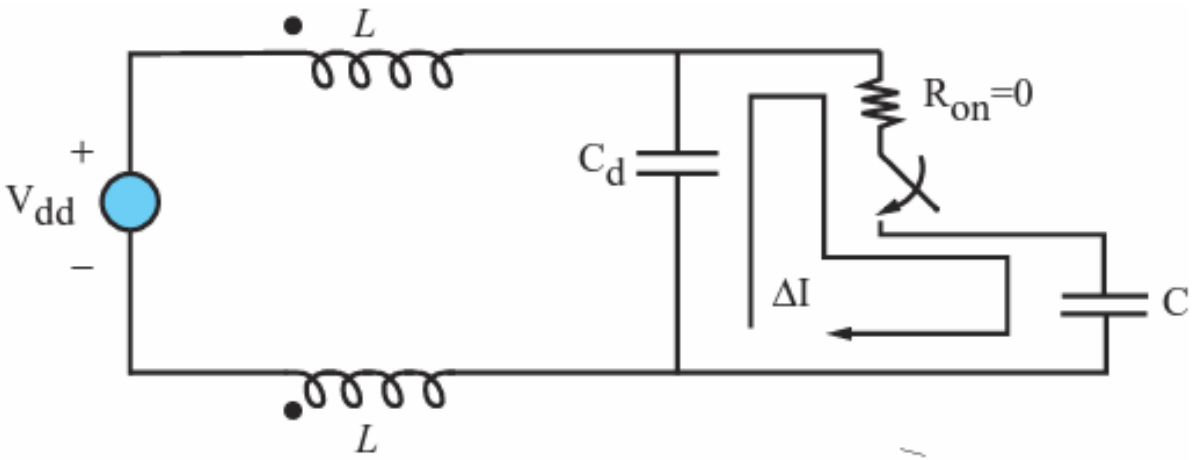
What if the chip is a single power device with load of 1 nF and 10 ns switching, and ≤ 10 % V_{dd} variation is acceptable?

- $L_{max} \leq (10\text{ ns})^2(0.1)(V_{dd}) \; / \; ((1\text{ nF})V_{dd}) = \mathbf{10\text{ nH}}$

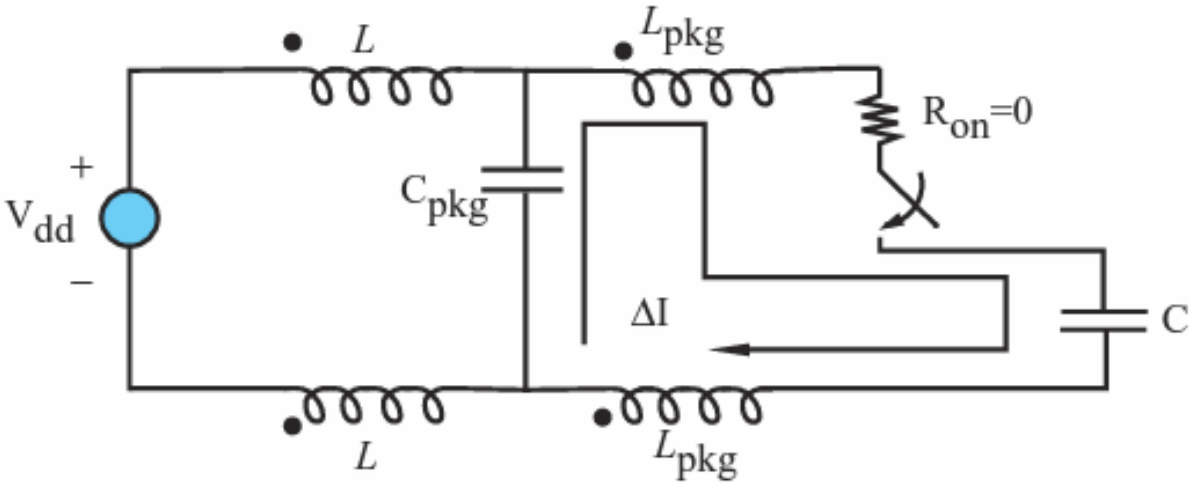


Decoupling Capacitors

On Chip



On Package



Example: L_{eff} = 10 pH, 1000 circuits draw 10 A in 0.25 ns.

Find the noise voltage.

- ΔV = **400 mV**

$$\Delta V = L_{\text{eff}}\,(dI/dt)$$

Design C_{pkg} to reduce the noise voltage to *200 mV*.

$$C = \Delta I\ \Delta t / \Delta V$$

- C_{pkg} = **12.5 nF**

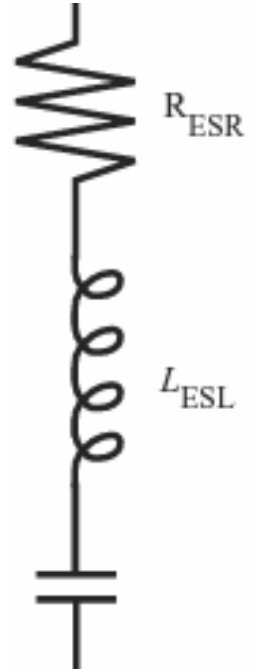
If L_{eff} = 5 pH, find the frequency above which C_{pkg} loses effectiveness.

$$f_{\max} = \frac{1}{2\pi\sqrt{2L_{\text{pkg}}C_{\text{pkg}}}}$$

- f_{max} = **637 MHz**

Limitation of Decoupling Capacitors

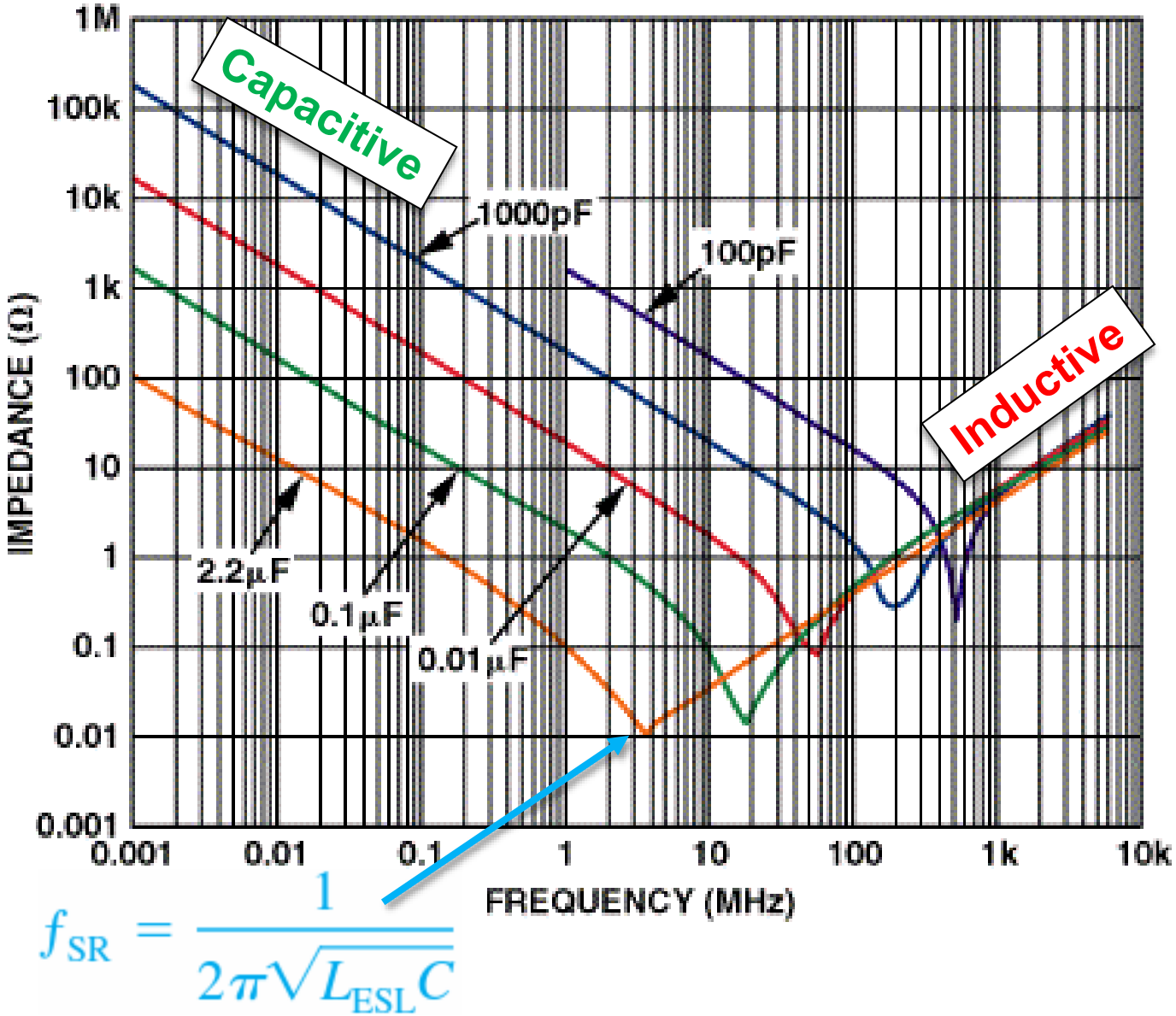
More realistic capacitor model:



$ESR =$ equivalent series R

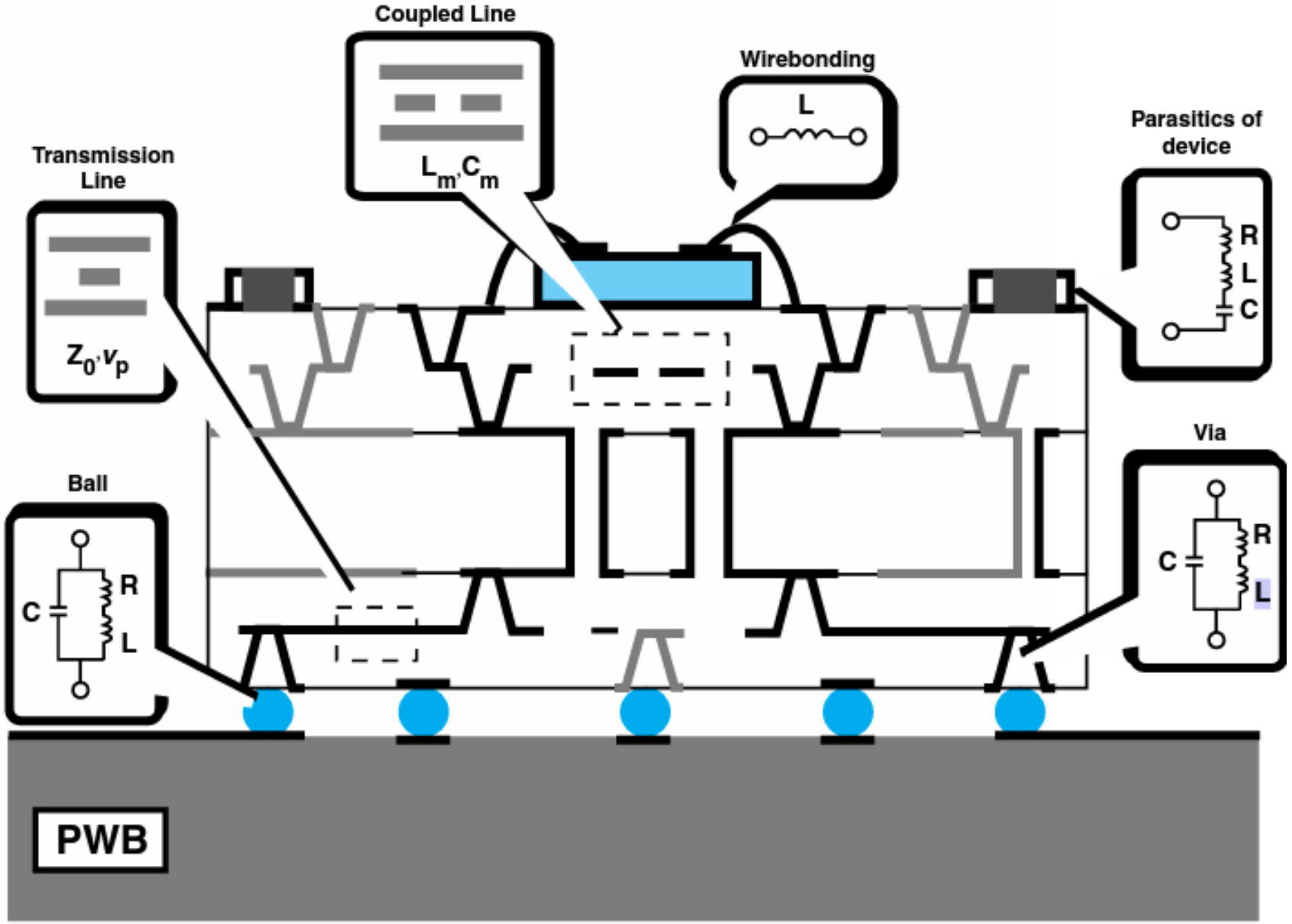
$ESL =$ equivalent series L

$f_{SR} =$ self-resonant frequency



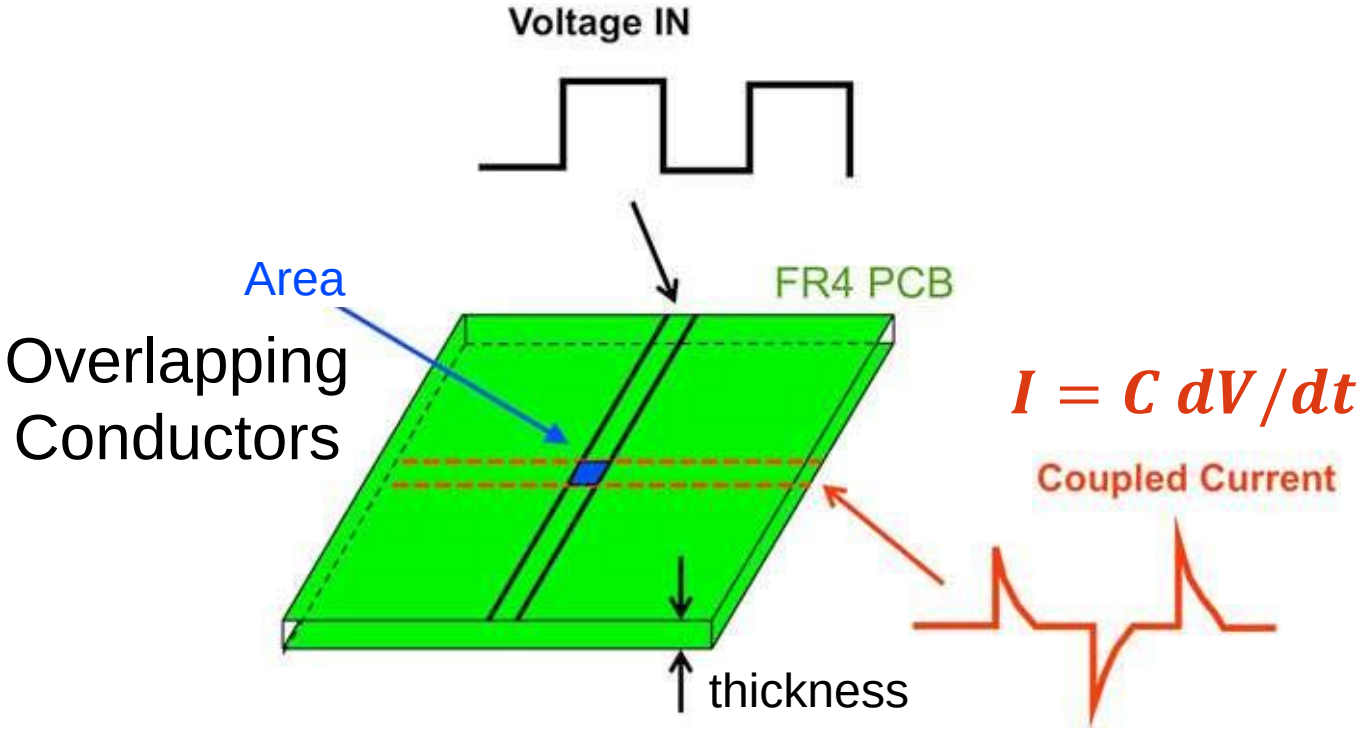
$$f_{SR} = \frac{1}{2\pi\sqrt{L_{ESL}C}}$$

Package Parasitics

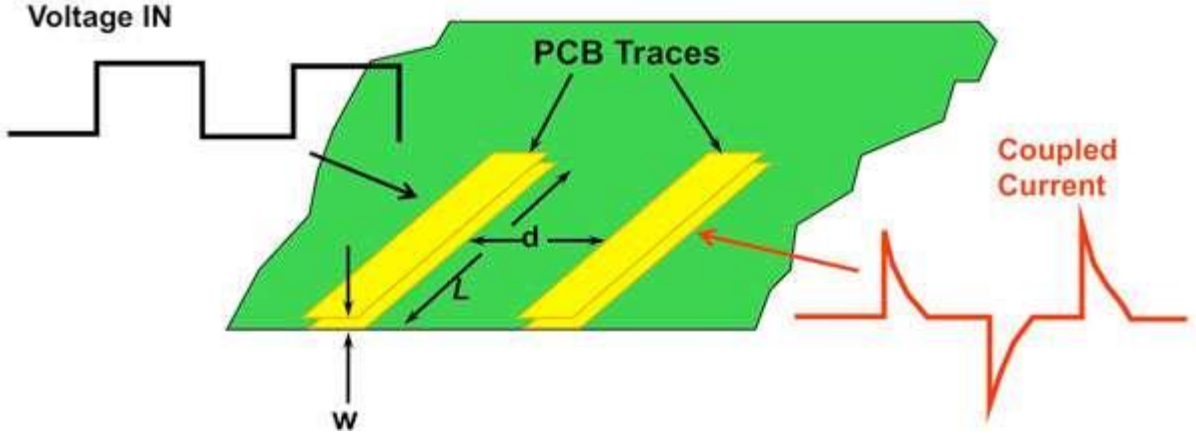


Effects of Parasitic Capacitance

- Delays
- Oscillations
- Ground currents
- Crosstalk

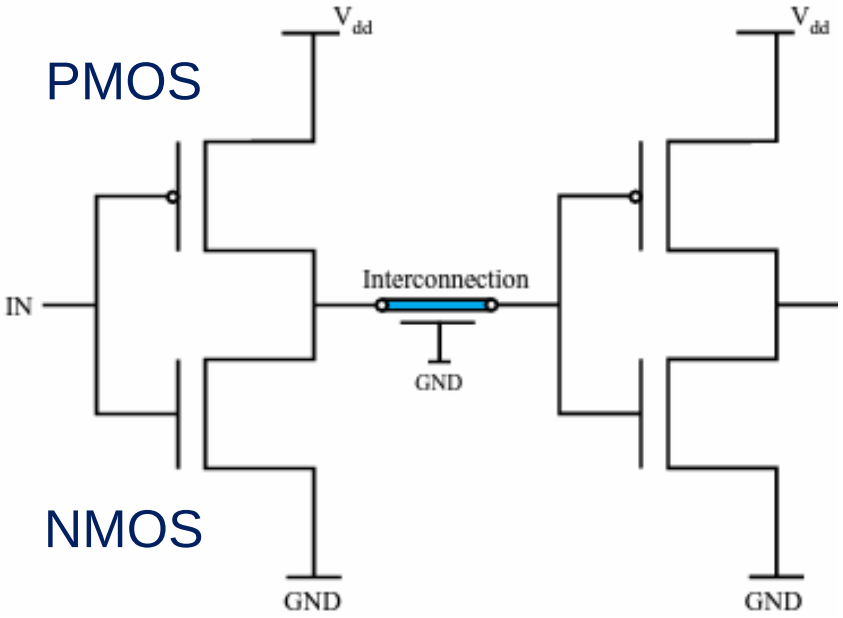


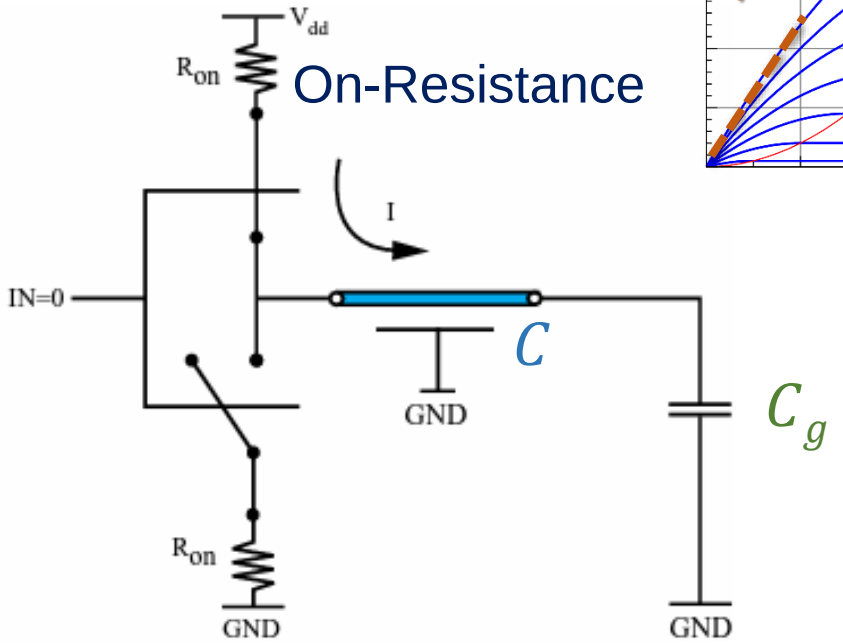
Adjacent Conductors

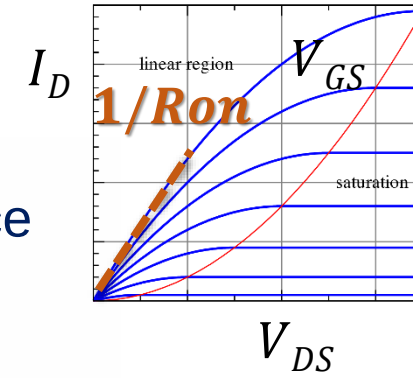


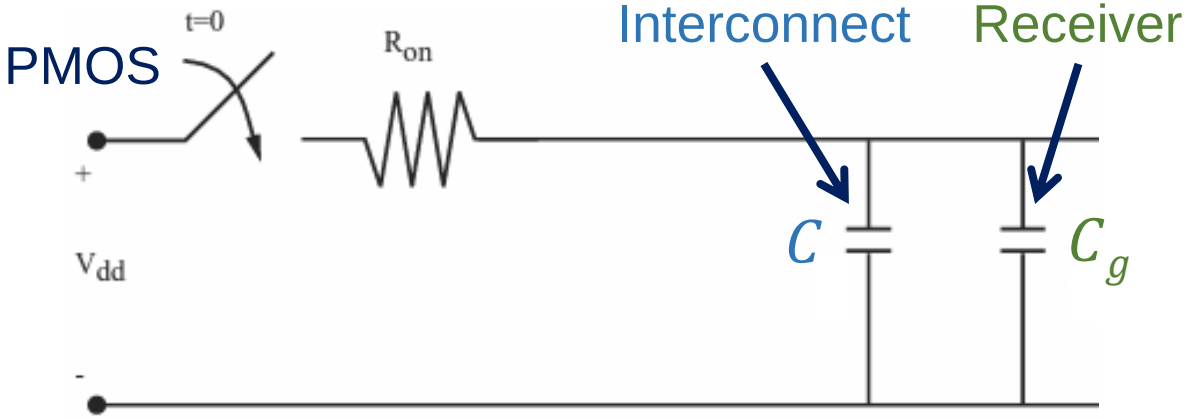
$$I = C\ dV/dt$$

Capacitive Delay

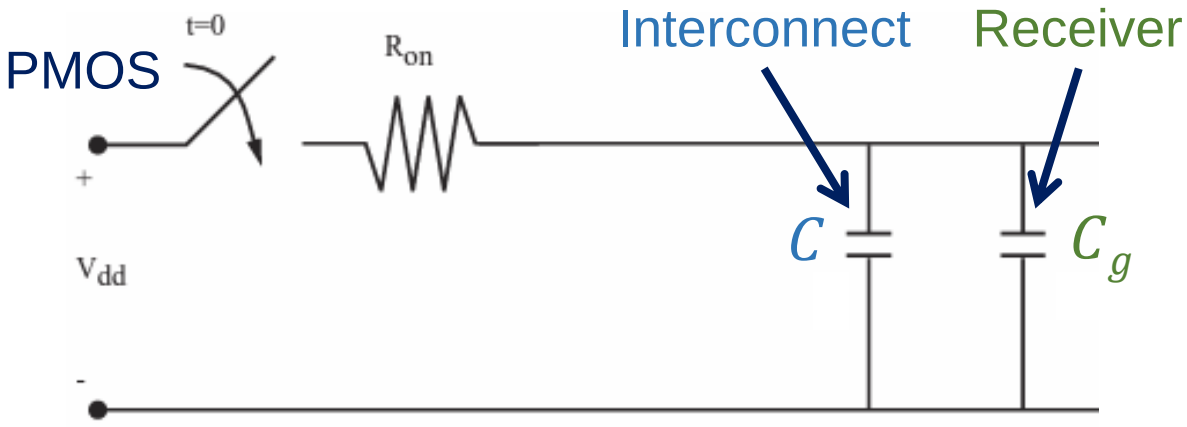






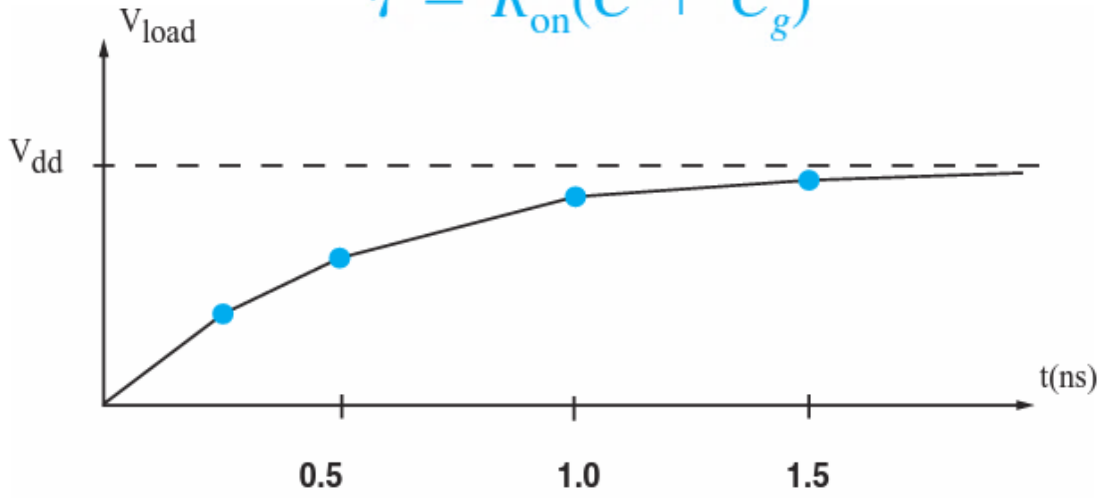


Capacitive Delay



$$V_{\text{load}}(t) = V_{dd}[1 - e^{-t/\tau}]$$

$$\tau = R_{\text{on}}(C + C_g)$$

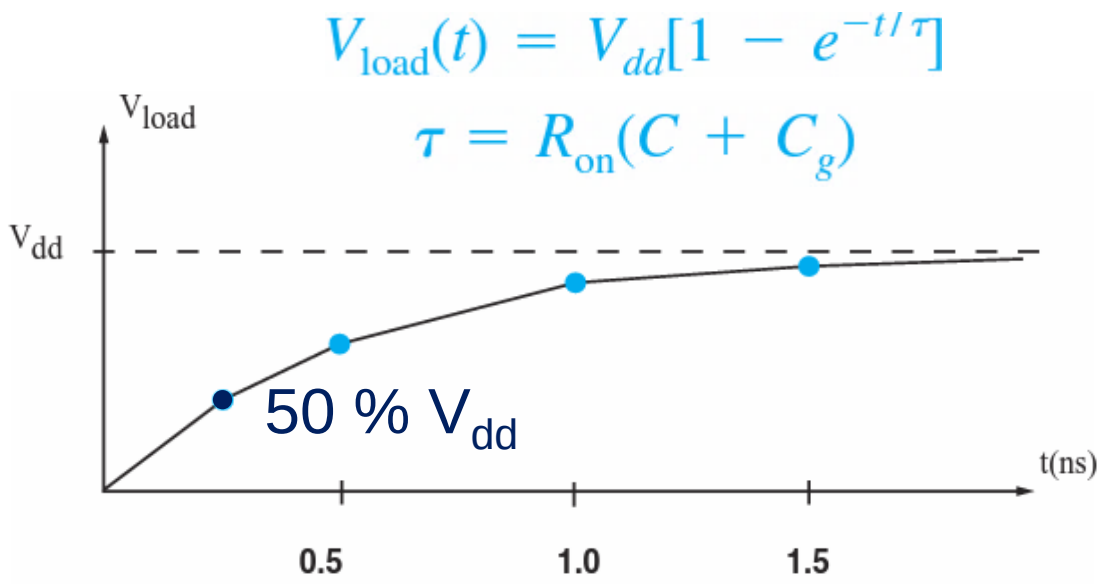


Example: Capacitive Delay

- $V_{dd} = 5$ V; $R_{on} = 50\ \Omega$; $C + C_g = 10$ pF
- $\tau = RC_{total} = (50\ \Omega)(10\text{ pF}) =$ **0.5 ns**

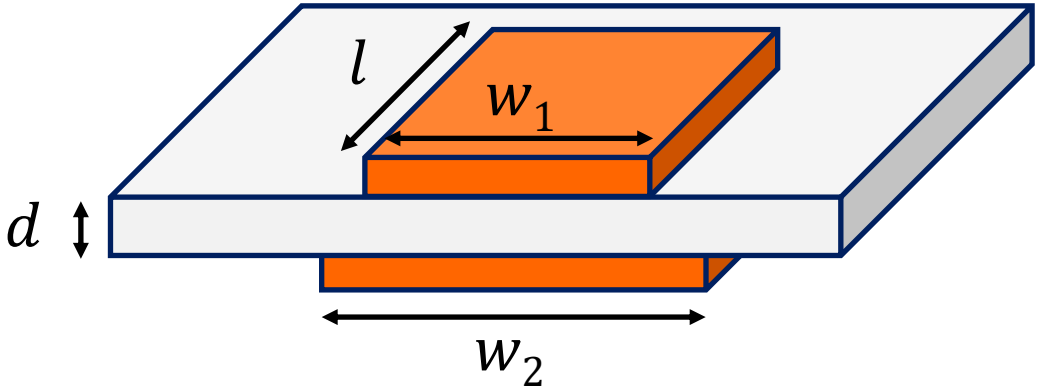
How long will it take for V_{load} to rise to 50 % of V_{supply}?

- $V_{load}(t) = V_{dd}[1 - e^{-t/\tau}]$
- $-\ln(1 - (0.5)(5\text{ V})/5\text{ V}) = 0.69$
- $t_{50\%} = 0.69\tau =$ **0.35 ns**
- $t_{90\%} = 2.3\tau =$ **1.15 ns**



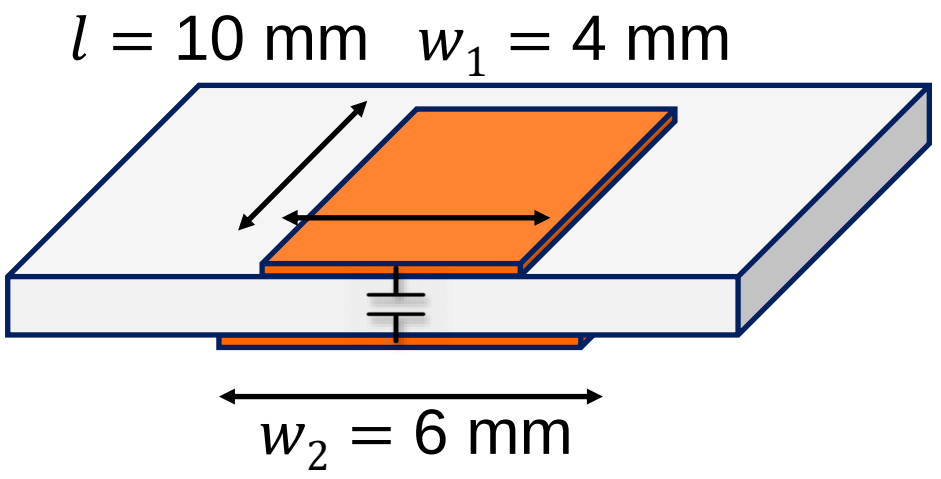
Capacitance (Overlapping Conductors)

- $Q = CV$
- Taking derivative:
  - $I = dQ/dt$
  - $I = C\ dV/dt$
- $C = \varepsilon A/d$
  - ε = permittivity
    - $\varepsilon = \varepsilon_r \varepsilon_0$
      - $\varepsilon_0 = 8.86 \times 10^{-12}$ F/m, permittivity of free space
      - ε_r = relative permittivity or dielectric constant (material property)
  - A = overlapping area
  - d = distance



Example: Capacitance (Overlapping Conductors)

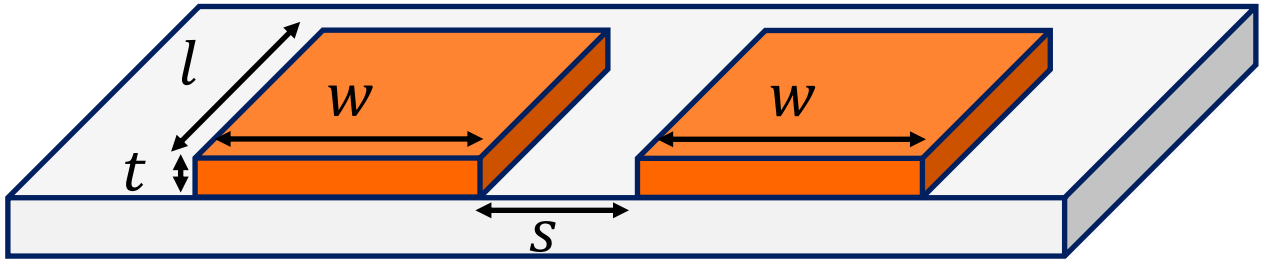
- Al_2O_3 substrate (e.g., DBC): $\varepsilon_r = 9.4$
- FR4 substrate (e.g., PCB): $\varepsilon_r = 4.4$
- $C = \varepsilon A/d = \varepsilon_0 \varepsilon_r A/d$
  - $\varepsilon_0 = 8.86 \times 10^{-12}$ F/m
  - $A = 10$ mm x 4 mm= 40 mm^2
  - $C = (8.86 \times 10^{-12}$ F/m$)(\varepsilon_r)(4 \times 10^{-5}$ m$^2)$ / (0.0005 m)
  - C_{Al2O3} = 6.7 pF (Q3D: 7.7 pF)
  - C_{FR4} = 3.12 pF (Q3D: 3.7 pF)



➢ Substrate materials with higher relative permittivity (dielectric constant) have higher parasitic capacitance

Example: Capacitance (Adjacent Conductors)

- Formula for adjacent conductors with equal widths:
- $C' = 0.122\ t/s + 0.0905\ (1 + \varepsilon_r)a$ [pF/cm]
- $a = \log(1 + 2\ w/s + 2\ \sqrt{w/s} + w^2 / 200)$
- s = distance between two adjacent conductors, mm
- t = thickness, mm
- w = conductor width, mm
- ε = permittivity
- $C = C'l$
- l = parallel running length, cm



Example: Capacitance (Adjacent Conductors)

- $C' = 0.122\ t/s + 0.0905\ (1 + \varepsilon_r)a$ [pF/cm]
- $a = \log(1 + 2\ w/s + 2\ \sqrt{w/s} + w^2 / 200)$
- $C = C'l$

Find the capacitance between the adjacent traces.

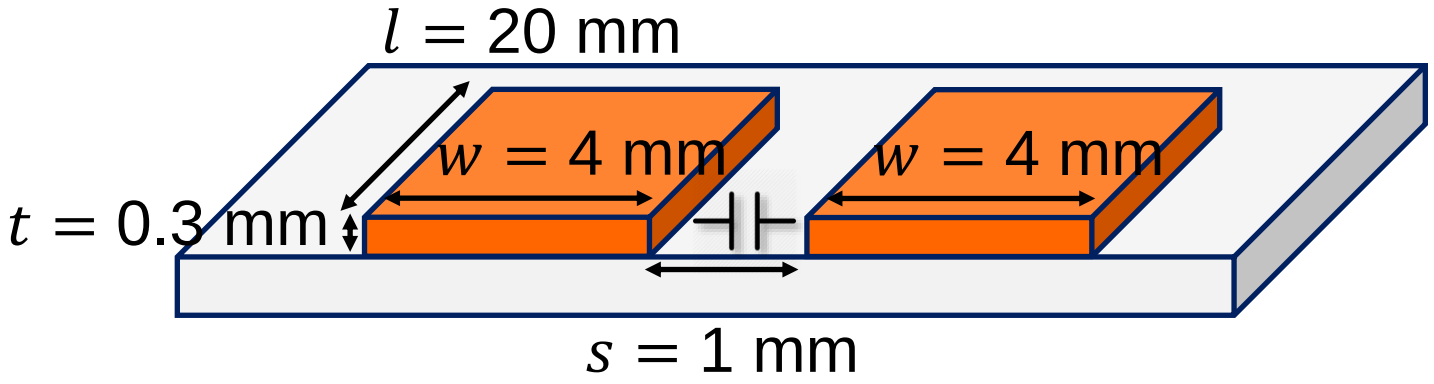
Al_2O_3 substrate (e.g., DBC): $\varepsilon_r = 9.4$

$C' = 1.1$ pF/cm

$C =$ **2.2 pF**

(Q3D: 1.3 pF for t_{Al2O3} = 1 mm)

(Q3D: 2.1 pF for t_{Al2O3} = 5 mm)



Coupling Capacity vs Spacing

To decrease C:

- Increase spacing between conductors
- Decrease conductor width
- Choose materials with low dielectric constant

➢ These will also impact the L, R, and thermal conductivity

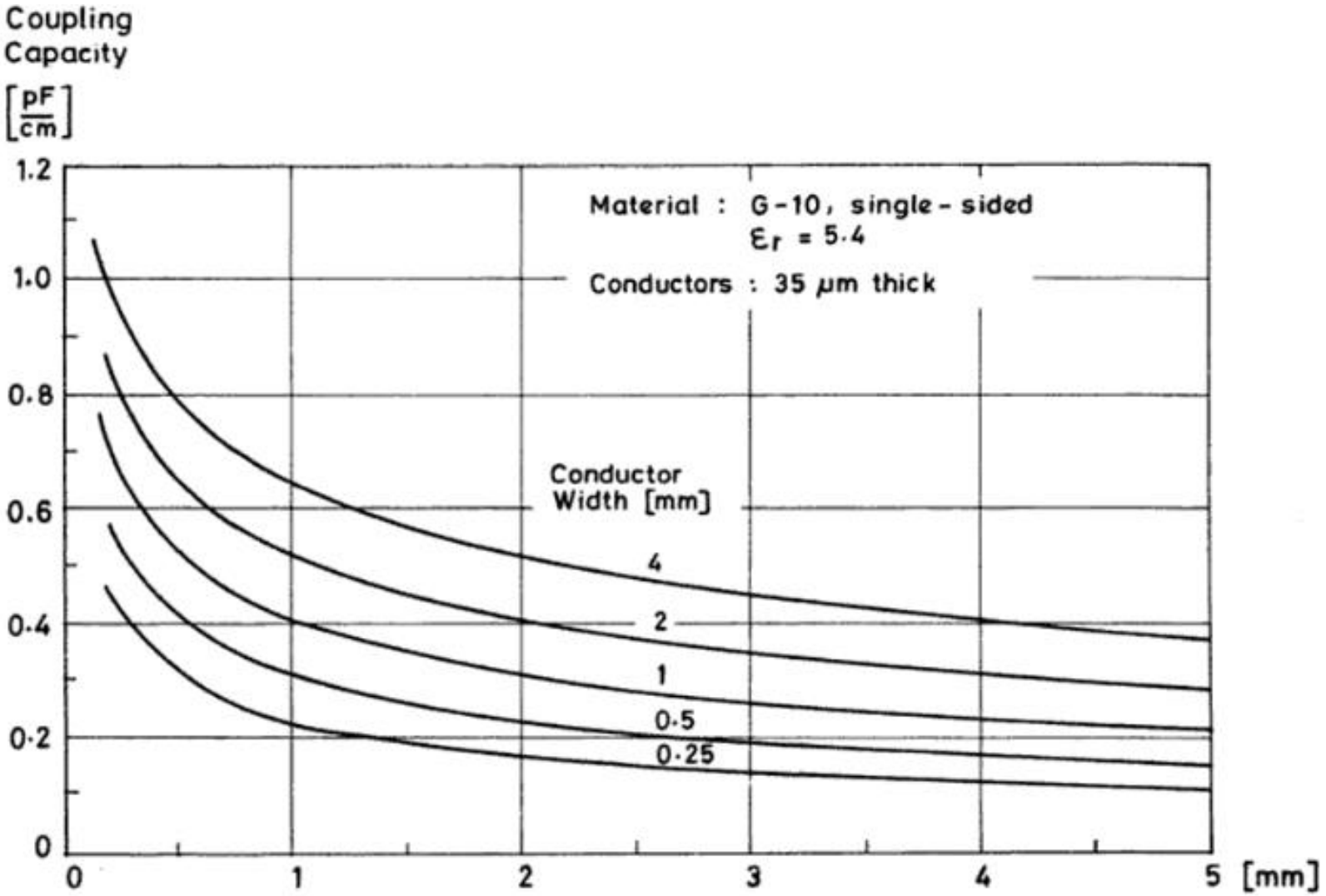
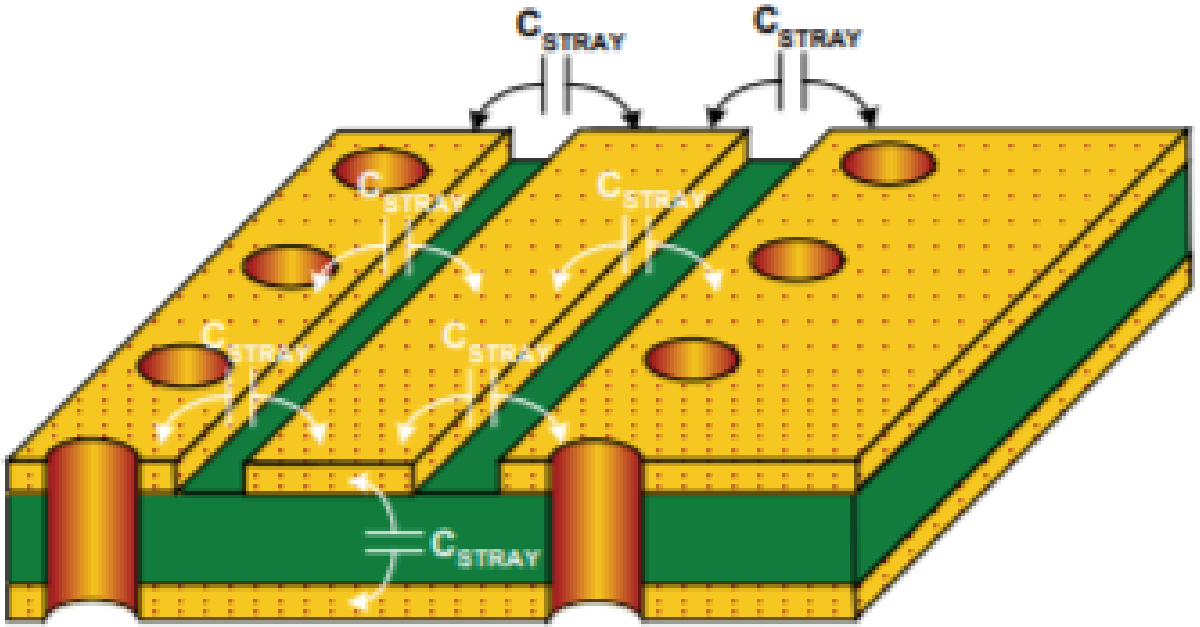


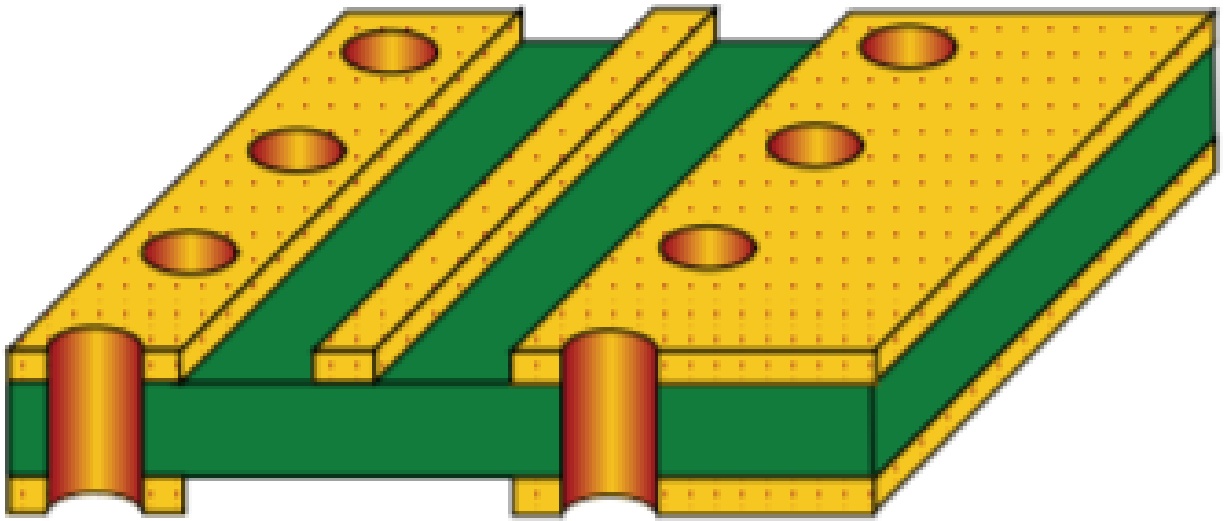
Fig. 2 4 Capacitive coupling between adjacent conductors

High-Capacitance vs Low-Capacitance Layouts

- High parasitic capacitance
  - Wide traces
  - Large overlap area
  - Close adjacent traces



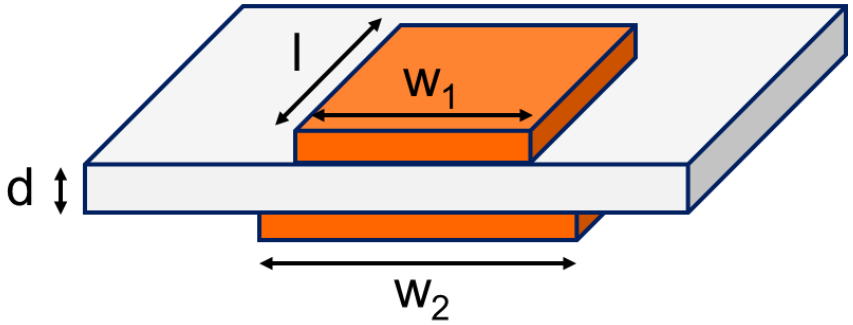
- Low parasitic capacitance
  - Reduced width
  - Eliminate overlap
  - Increase spacing between adjacent traces



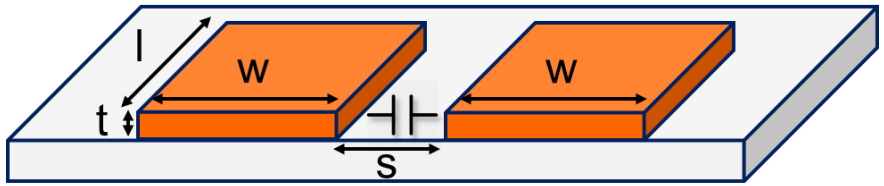
$I = C\,dV/dt$

Summary: Capacitance

- Capacitive delay: $\tau = RC$
- Overlapping conductors:
  - $C = \varepsilon A/d$, where A = overlapping area
  - Decrease by decreasing overlapping area, increasing distance d, or using a material with lower dielectric constant ε_r



- Adjacent conductors:
  - $C' = 0.122\ t/s + 0.0905\ (1 + \varepsilon_r)a$ [pF/cm]
    - $a = \log(1 + 2\ w/s + 2\sqrt{w/s} + w^2\ /\ 200)$
    - $C = C'l$
  - Decrease by increasing spacing s between conductors, reducing t, w, and l of conductors, or using material with lower ε_r



Summary: Types

- Resistance
  - DC (temperature dependent)
  - AC (skin and proximity effects)
- Capacitance
  - Between overlapping conductors
  - Between adjacent conductors
- Inductance
  - Self/partial inductance
  - Mutual inductance
  - Total/loop/effective inductance

Summary: Consequences

- Resistance
  - Power loss
  - Heating
  - Ground bounce
- Capacitance
  - Delay
  - Noise
  - Oscillation
- Inductance
  - Delay
  - Noise
  - Oscillation
  - Voltage overshoot

Summary: Mitigation Approaches

- Resistance
  - DC – increase conductivity, decrease length, increase area
  - AC – increase circumference/ perimeter, multiple smaller conductors in parallel
- Capacitance
  - Minimize overlapping areas
  - Increase spacing between traces/interconnects
  - Low dielectric constant
- Inductance
  - Reduce loop area
  - Decrease conductor length
  - Decrease spacing between the source and return paths
  - Increase spacing between conductors with same current direction
  - Use decoupling capacitors
  - Arrange conductors perpendicular to minimize unwanted coupling

Next Class

- Electrical Design (Chapter 2)
  - Intro to Finite Element Analysis (FEA) and ANSYS Q3D
  - Start Q3D in-class tutorial