Lecture 14

Review

Note: these slides are a summary of most of the topics we have covered during the course, but they may not cover all topics/problems that could appear on the midterm exam

March 18, 2025

Reminders and Announcements

- Office hours:
  - Wednesday, March 19th, 5pm-6pm
  - Thursday, March 20th, 9am-10am

- Midterm: Thursday, March 20th, 5:00pm-6:15pm

Midterm: Thursday, March 20th, 5:00pm-6:15pm

- If you are located in Blacksburg, then you should take the exam in-person in TORG 1050, even if you are enrolled in the virtual section of the course
- If you are enrolled in the *virtual campus*, please email me by March 5th indicating if you will take the exam virtually or in-person in Arlington or Blacksburg
- Will cover the topics in lectures 1-6 (packaging overview and electrical design) and 9-13 (transmission lines and thermal design)
- The lecture on March 18th will be a review session → come ready with questions or topics you would like to cover
- You will <u>not</u> be asked to do any simulations for the midterm
- The problems will be a mix of conceptual short response and calculation problems
- Things to bring to the exam: writing utensils & *non-programmable* calculator
- An equation/reference sheet and extra paper will be provided by the proctor
- The reference sheet will be uploaded to Canvas next week; you do <u>not</u> need to print out the reference sheet

R, C, L Overview

- Resistance, R
  - Unit: Ohms, Ω
  - Effects: damping, voltage drop, loss ($P = I^2R$)
  - Types: DC & AC (skin effect)
  - Ohm's Law: $V = IR$
- Capacitance, C
  - Unit: Farad, F
  - Definition: amount of charge stored per volt
  - Effects: coupling, resonance
  - $I = C\frac{dV}{dt}$
- Inductance, L
  - Unit: Henry, H
  - Definition: ratio of magnetic flux linked by a loop of current to the current
  - Effects: coupling, resonance, voltage drop/overshoot
  - $V = L\frac{dI}{dt}$
- Every current-carrying conductor has some R and L

Summary: Types

- Resistance
  - DC (temperature dependent)
  - AC (skin and proximity effects)
- Capacitance
  - Between overlapping conductors
  - Between adjacent conductors
- Inductance
  - Self/partial inductance
  - Mutual inductance
  - Total/loop/effective inductance

Summary: Consequences

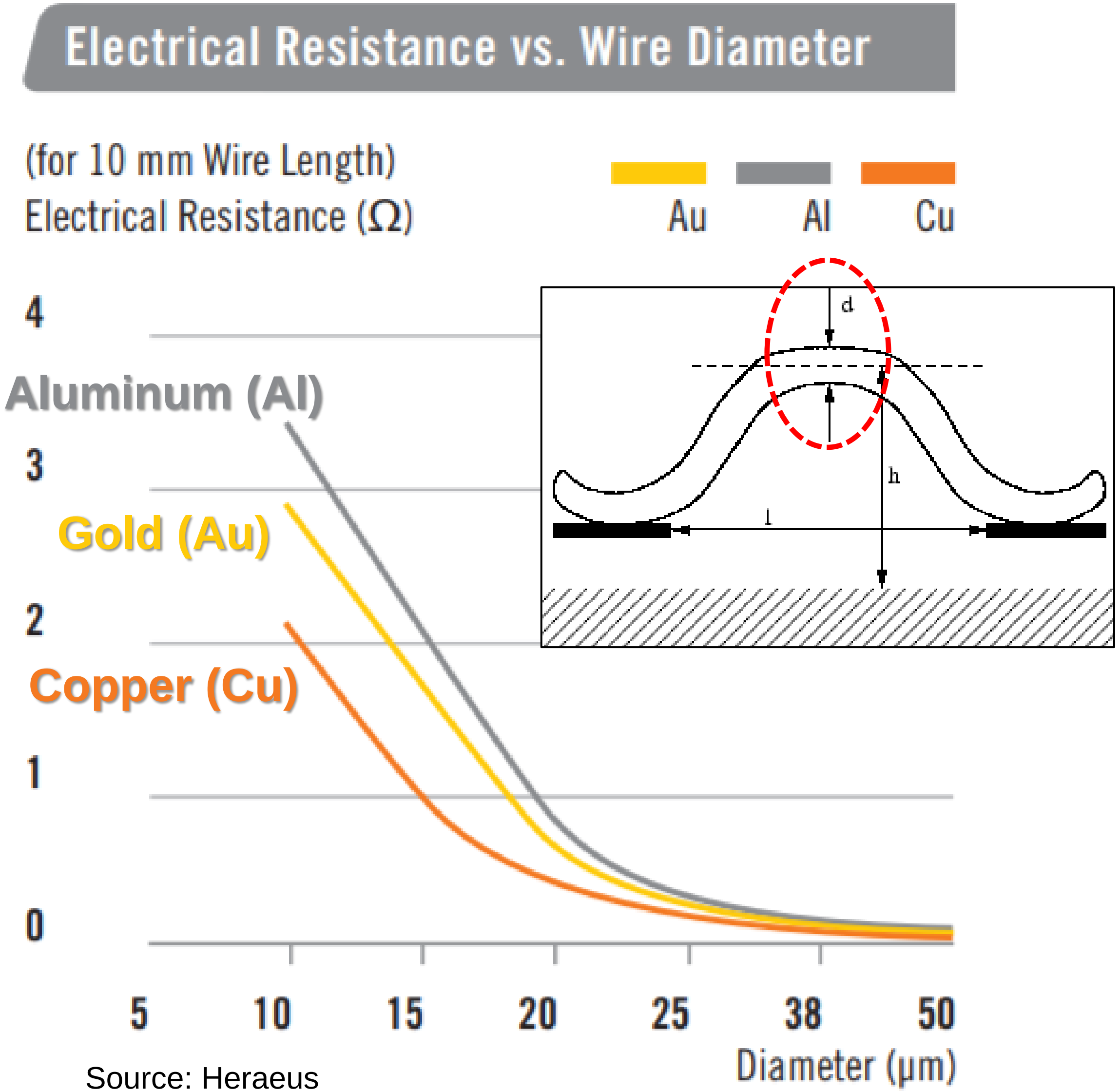
- Resistance
  - Power loss
  - Heating
  - Ground bounce
- Capacitance
  - Delay
  - Noise
  - Oscillation
- Inductance
  - Delay
  - Noise
  - Oscillation
  - Voltage overshoot

Summary: Mitigation Approaches

- Resistance
  - DC – increase conductivity, decrease length, increase area
  - AC – increase circumference/ perimeter, multiple smaller conductors in parallel
- Capacitance
  - Minimize overlapping areas
  - Increase spacing between traces/interconnects
  - Low dielectric constant
- Inductance
  - Reduce loop area
  - Decrease conductor length
  - Decrease spacing between the source and return paths
  - Increase spacing between conductors with same current direction
  - Use decoupling capacitors
  - Arrange conductors perpendicular to minimize unwanted coupling

DC Resistance

- Critical components
  - Interconnects
  - Substrate traces/vias
  - Terminals
- $V = I\boldsymbol{R}$, $P = I^2\boldsymbol{R}$
- $R = \frac{\rho l}{A_c}$
  - $\rho =$ resistivity, Ω·m
  - $\sigma = 1/\rho =$ conductivity, S/m
  - $l =$ length, m
  - $A_c =$ cross-sectional area, m^2



Source: Heraeus

Example: DC Resistance of Wire Bond

- 50 µm (2 mil*) gold wire bond with 10 mm length
- $\rho_{gold@25\mathrm{C}}$= 2.2 x 10^{-8} Ω·m
- What is the resistance of the wire bond at room temperature?

$$\boldsymbol{R_{25\mathrm{C}} = \rho_{25\mathrm{C}} l / A_c}$$

$$l = 10 \text{ mm} = 0.01 \text{ m}$$

$$A_c = \pi r^2 = \pi(2.5 \text{ x } 10^{-5} \text{ m})^2$$

$$R_{25\mathrm{C}} = (2.2 \text{ x } 10^{-8}\ \Omega\cdot\text{m}) \cdot (0.01 \text{ m}) / (\pi(2.5 \text{ x } 10^{-5} \text{ m})^2) = \mathbf{0.11\ \Omega}$$

- What if you have 5 wire bonds in parallel?

$$R_{eq} = R / 5 = 0.11\ \Omega / 5 = 0.022\ \Omega = \mathbf{22\ m\Omega}$$

*1 mil = 0.001 inch

Example: DC Resistance of PCB Trace

- 200-mm-long, 0.1-mm-wide PCB trace with 1 oz* copper
- $\rho_{copper@25C}$ = 1.7 x 10^{-8} Ω·m
- 1 oz copper = 1.37 mils = 0.00137 in = 0.034798 mm
- What is the resistance of the copper trace at room temperature?

$$\boldsymbol{R_{25C} = \rho_{25C} l / A_c}$$

$$l = 200 \text{ mm} = 0.2 \text{ m}$$

$$A_c = t \cdot w = (3.5 \times 10^{-5} \text{ m}) \cdot (1 \times 10^{-4} \text{ m}) = 3.5 \times 10^{-9} \text{ m}^2$$

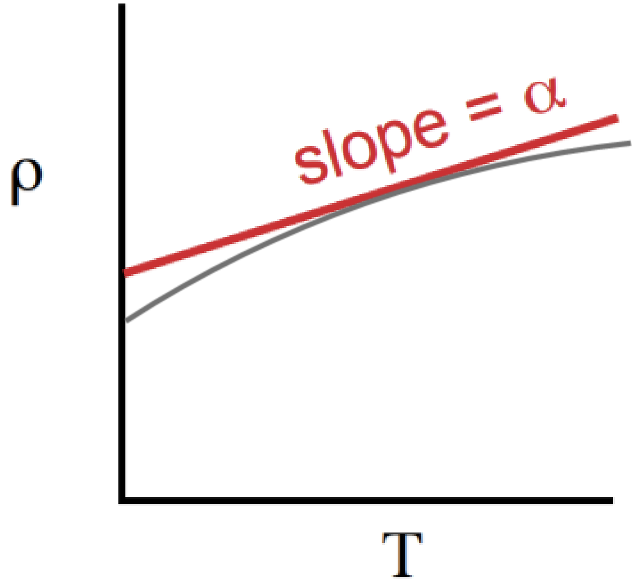
$$R_{25C} = (1.7 \times 10^{-8}\ \Omega \cdot \text{m}) \cdot (0.2 \text{ m}) / (3.5 \times 10^{-9} \text{ m}^2) = \mathbf{0.97\ \Omega}$$

… at room temperature

*1 oz of copper rolled out over 1 sq. ft.

Temperature Dependence of DC Resistance

- Resistance of conductors increases with temperature
- The fractional change in resistance is proportional to the change in temperature:
- $R_1 = R_0 \cdot [1 + \alpha(T_1 - T_0)]$
  - R_0 = resistance at T_0, Ω
  - T_1 = temperature of interest, K or °C
  - α = temperature coefficient, 1/K or 1/°C
- This linear approximation can be used if α does not change much with T and $\alpha \Delta T \ll 1$
- When T_0 is room temperature,



$$R_1 = \rho_{25\mathrm{C}} l / A_c \cdot [1 + \alpha(T_1 - 25°\mathrm{C})]$$

Temperature Coefficient of Resistance, α

$$R_1 = R_0 \cdot [1 + \alpha(T_1 - T_0)]$$

- Gold: $\alpha = 3.4 \times 10^{-3}$ /°C
- Silver: $\alpha = 3.8 \times 10^{-3}$ /°C
- Aluminum: $\alpha = 3.9 \times 10^{-3}$ /°C
- Platinum: $\alpha = 3.9 \times 10^{-3}$ /°C
- Copper: $\alpha = 4.0 \times 10^{-3}$ /°C

Example: DC Resistance of PCB Trace at 100 °C

- 200-mm-long, 0.1-mm-wide PCB trace with 1 oz copper

$$\boldsymbol{R_1 = \rho_{25C} l/A \cdot [1 + \alpha(T_1 - 25°C)]}$$

$$R_{25C} = \frac{\rho_{25C} l}{A} = (1.7 \times 10^{-8}\ \Omega\cdot m) \cdot (0.2\ m) / (3.5 \times 10^{-9}\ m^2) = \mathbf{0.97\ \Omega}$$

- What is the resistance of the copper trace *at 100°C*?

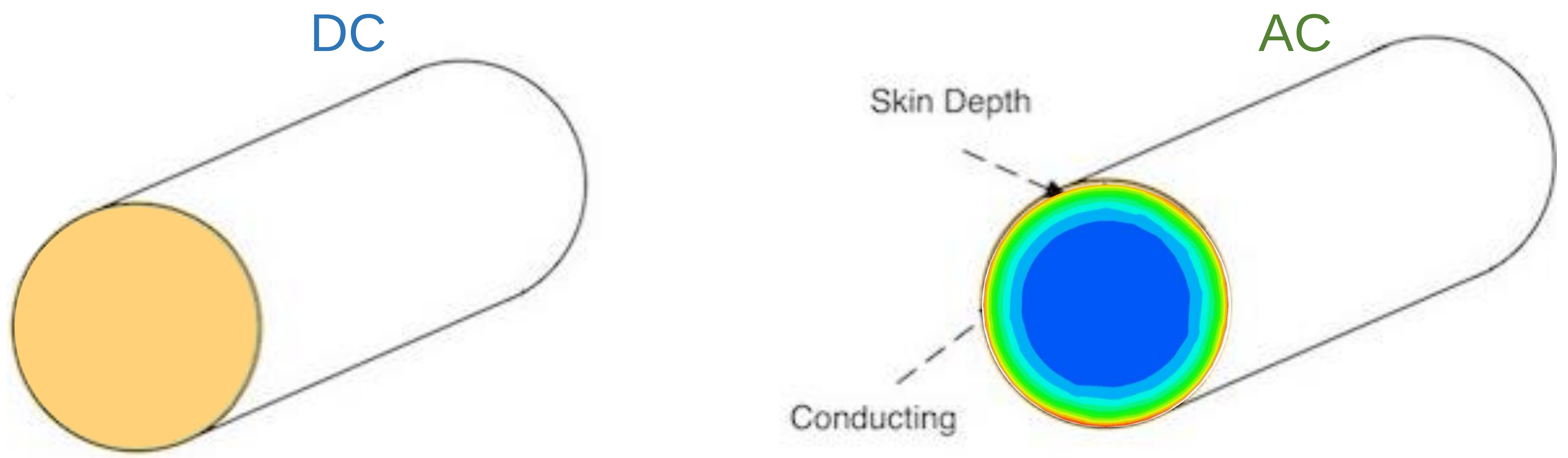
$$\alpha_{copper} = 4.0 \times 10^{-3}\ /°C$$

$$R_{100C} = R_{25C} \cdot [1 + (4.0 \times 10^{-3}\ /°C)(100°C - 25°C)] = \mathbf{1.25\ \Omega}$$

➢ **30 % increase!**

DC and AC Resistance

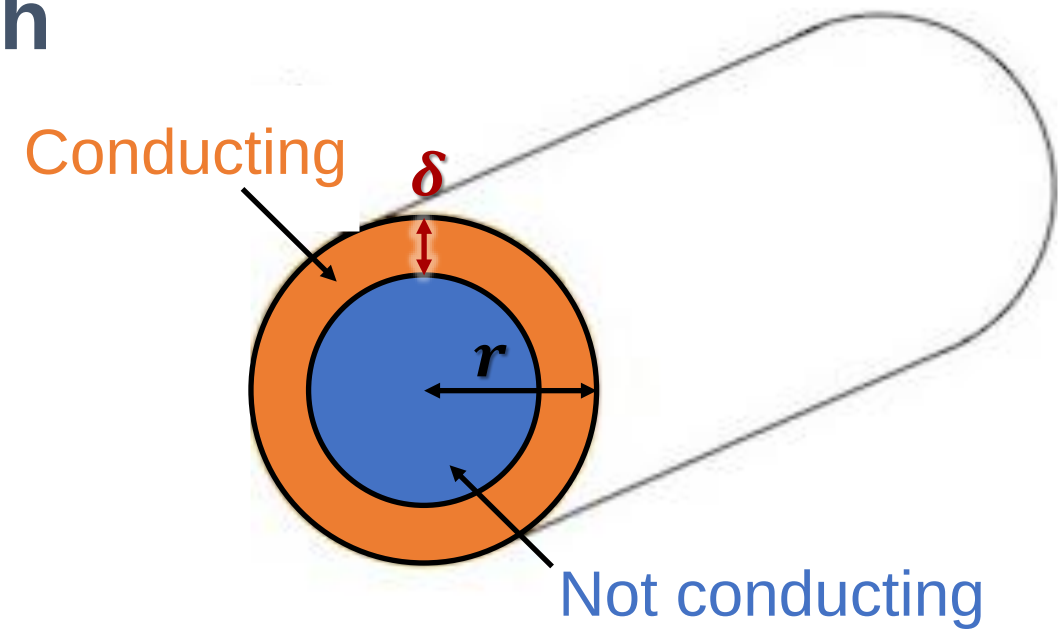
- Direct current (DC) flows uniformly in a conductor
- With high-frequency alternating current (AC), current crowds along the conductor surface
- Current density = flow of charge per unit area [Amps / m^2]



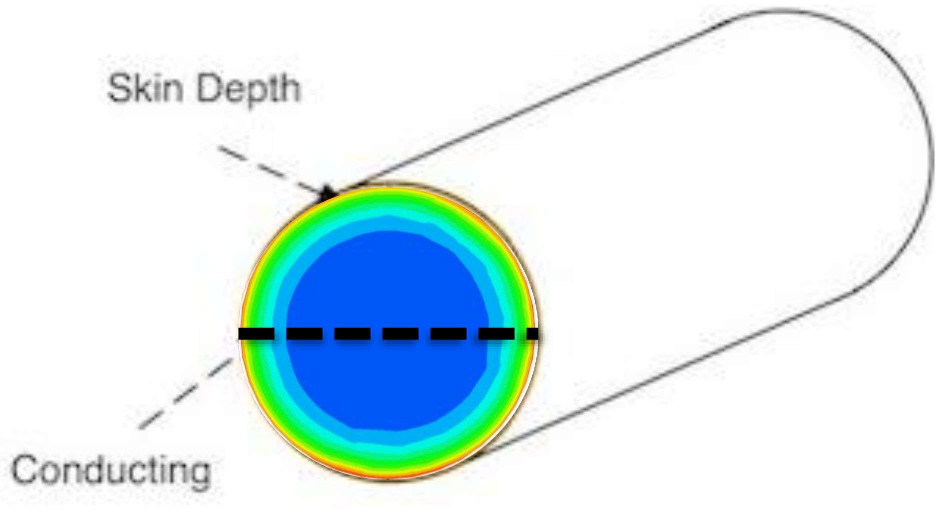
Skin Depth

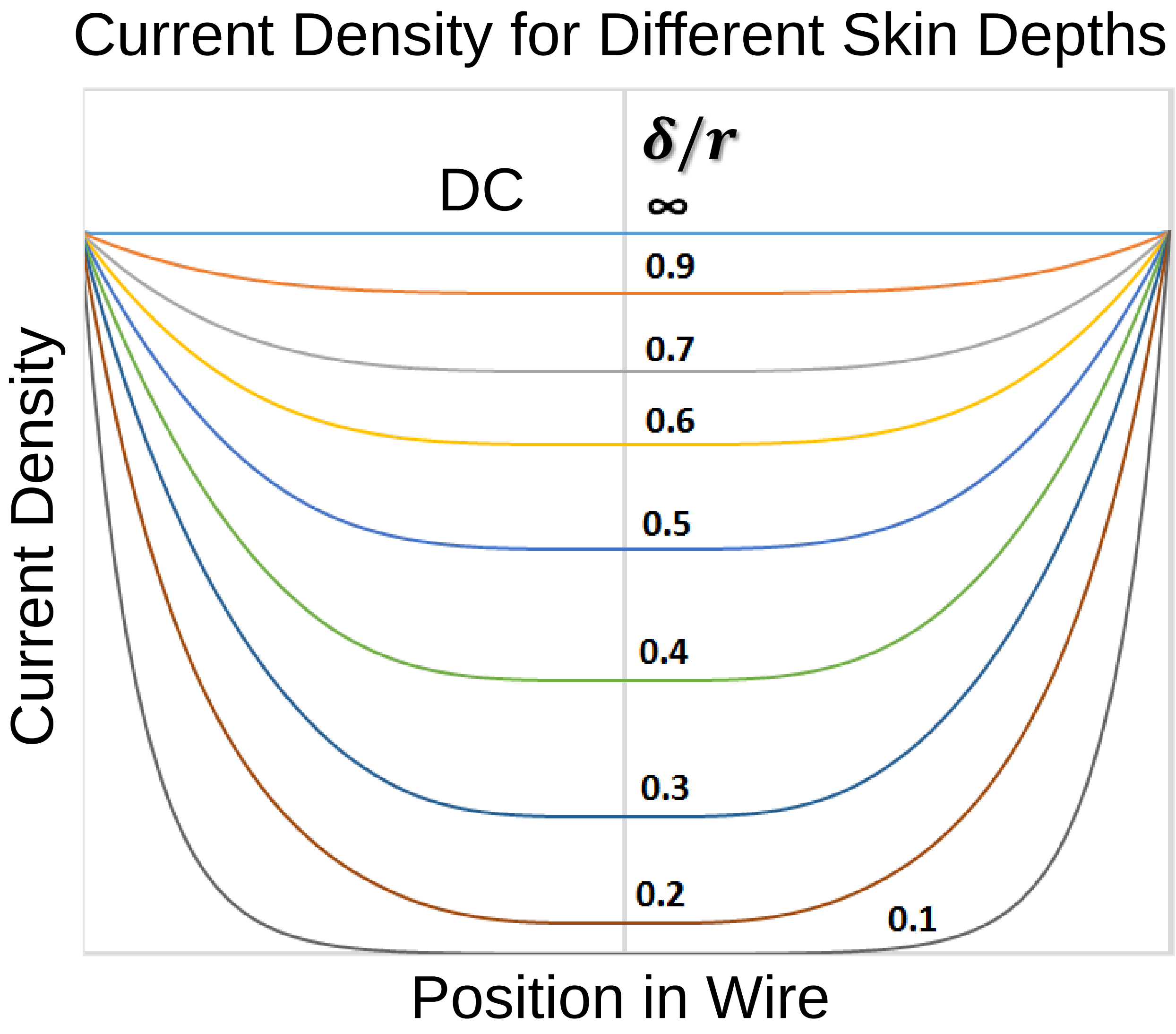
- $\boldsymbol{R_{AC}} = \boldsymbol{\rho l / A_{eff}}$
- $A_{eff} = \pi(d\,\boldsymbol{\delta} - \boldsymbol{\delta}^2)$, when $r \gg \delta$
  - A_{eff} = effective cross sectional area
  - d = diameter, m
  - δ = skin depth, m
- $\delta = \sqrt{(\rho\ /\ (\pi\ f\ \mu))}$
  - ρ = resistivity, Ω·m
  - f = frequency, Hz
  - μ = permeability, H/m
    - μ_0 = permeability of free space ≈ 4π x 10^{-7} H/m
    - μ_r = relative permeability

$$\left.\begin{array}{l} \mu_0 \\ \mu_r \end{array}\right\} \mu = \mu_0 \mu_r$$



Why do we need $r \gg \delta$ for the (simple) A_{eff} equation?





Example: AC Resistance of Wire Bond

- 50 µm (2 mil*) gold wire bond with 10 mm length
- ρ_{gold}= 2.2 x 10^{-8} Ω·m
- What is the AC resistance of the wire bond at 150 MHz?

$$\boldsymbol{R_{AC} = \rho l / A_{eff}}$$

$$\boldsymbol{\delta = \sqrt{(\rho \,/\, (\pi\, f\, \mu))}}$$

$$= \sqrt{(2.2 \cdot 10^{-8}\ \Omega \cdot \mathrm{m} / \ (\pi\ (150\mathrm{MHz})(4\pi * 10^{-7}\mathrm{H/m})))} = \mathbf{6.095 \cdot 10^{-6} m}$$

$$\boldsymbol{A_{eff} = \pi(d\,\delta - \delta^2)}$$

$$= \pi\left(\left(5 \cdot 10^{-5}\mathrm{m}\right)6.095 \cdot 10^{-6}\mathrm{m} - \left(6.095 \cdot 10^{-6}\mathrm{m}\right)^2\right) = \mathbf{8.41 \cdot 10^{-10} m^2}$$

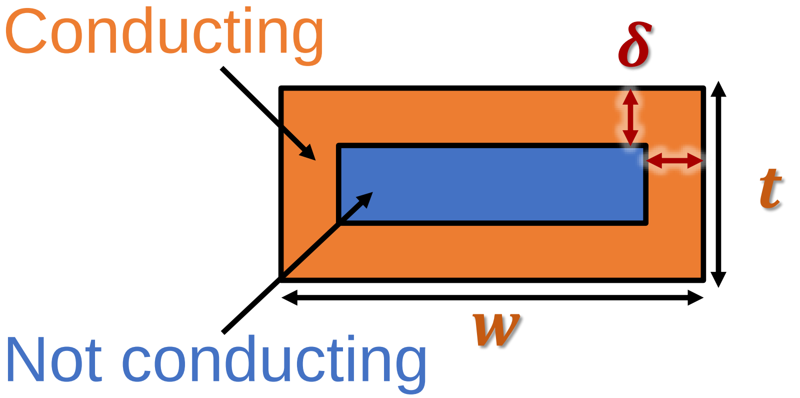
R = (2.2 x 10^{-8} Ω·m) · (0.01 m) / (8.41 x 10^{-10} m^2) = **0.26 Ω**

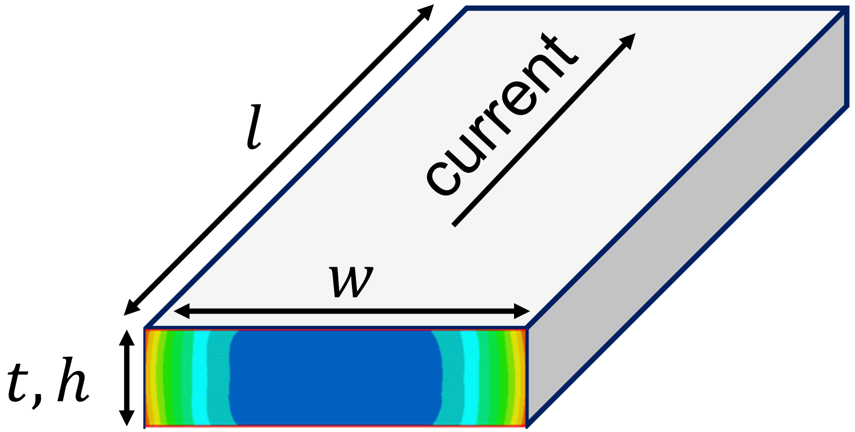
→ 2.3x higher than the DC resistance

*1 mil = 0.001 inch

AC Resistance of Rectangular Conductors
(First-Order Approximation)

- E.g., ribbon bonds, PCB traces
- $R_{AC} = \rho l / A_{eff}$
- When $2\delta \ll w$ and t
  - $A_{eff} = wt - (w - 2\delta)(t - 2\delta)$
  - $A_{eff} = 2w\delta + 2t\delta - 4\delta^2$
  - $\boldsymbol{A_{eff} = 2\delta(w + t - 2\delta)}$
- $\delta = \sqrt{(\rho / (\pi f \mu))}$
- When $2\delta \geq w$ or t
  - $A_{eff} = wt$





Keller, R.B. (2023). Skin Effect. In: Design for Electromagnetic Compatibility--In a Nutshell. Springer, Cham. https://doi.org/10.1007/978-3-031-14186-7_10

Example: AC Resistance of PCB Trace

- 200-mm-long, 0.1-mm-wide PCB trace with 1 oz* copper
- ρ_{copper} = 1.7 x 10^{-8} Ω·m
- 1 oz copper = 1.37 mils = 0.00137 in = 0.034798 mm
- What is the AC resistance of the copper trace at 150 MHz?

$$\boldsymbol{R_{AC} = \rho l / A_{eff}}$$

$$\boldsymbol{\delta = \sqrt{(\rho\ /\ (\pi\ f\ \mu))}}$$

$$= \sqrt{(1.7 \cdot 10^{-8}\ \Omega \cdot \mathrm{m}/\ (\pi\ (150\mathrm{MHz})(4\pi * 10^{-7}\mathrm{H/m})))} = \mathbf{5.36 \cdot 10^{-6}m}$$

$$\boldsymbol{A_{eff} = 2\delta(w + t - 2\delta)}$$

$$= 2(5.36 \cdot 10^{-6}\mathrm{m})(1 \cdot 10^{-4}\mathrm{m} + 3.5 \cdot 10^{-5}\mathrm{m} - 2(5.36 \cdot 10^{-6}\mathrm{m}))$$

$$= \mathbf{1.33 \cdot 10^{-9}m^2}$$

R_{AC} = (1.7 x 10^{-8} Ω·m) · (0.2 m) / (1.33 x 10^{-9} m^2) = **2.56 Ω**

→ 2.6x higher than the DC resistance

Resistance Reduction Methods

DC Resistance

$$R_1 = \rho_0 l/A \cdot [1 + \alpha(T_1 - T_0)]$$

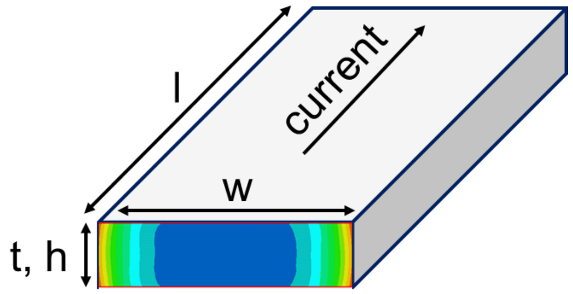
- Material
  - High electrical conductivity (low electrical resistivity)
- Geometry
  - Increase cross-sectional area
  - Decrease length
  - Parallel conductors
- Application
  - Decrease temperature
  - Decrease current

AC Resistance

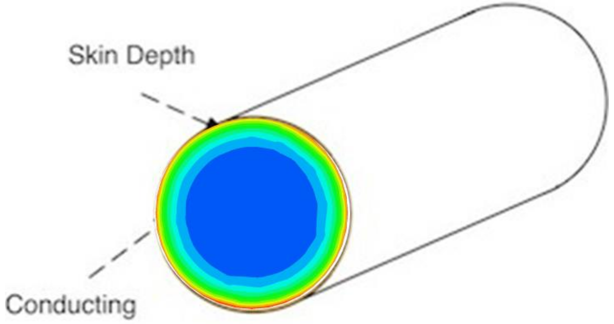
$$\delta = \sqrt{(\rho \,/\, (\pi\, f\, \mu))}$$

- Material
  - Conductors with low permeability and low resistivity
- Geometry
  - Increase circumference/perimeter
  - Use wide flat conductor
  - Parallel smaller conductors
- Application
  - Decrease frequency

Summary: Resistance



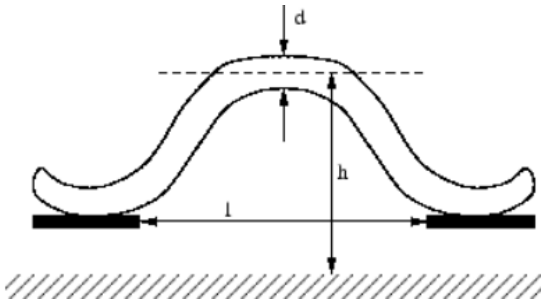
- DC resistance at room temperature: $R = \rho l / A$
- Temperature correction: $R = R_0 \cdot [1 + \alpha\,(T - T_0)]$
- AC resistance



  - Skin effect: $\delta = \sqrt{(\rho / (\pi f \mu))}$
    - AC current → alternating magnetic field → opposing EMF → opposes current flow in center of wire → majority of current flows through outer surface
  - Related to circumference, ρ, and μ of conductor, and frequency
  - Effective area for circular conductors: $A_{eff} = \pi(d\delta - \delta^2)$, when $\delta \ll r$
  - Effective area for rectangular conductors: $A_{eff} = 2\delta(w + t - 2\delta)$, when $2\delta \ll w$ and t

Self Inductance: Wire (Round Conductor)

- $L_{self} = \frac{\mu}{2\pi} l \left[\ln\left(\frac{l}{r} + \sqrt{1 + \frac{l^2}{r^2}} \right) - \sqrt{1 + \frac{r^2}{l^2}} + \frac{r}{l} + \frac{1}{4} \right]$
    - l = length in meters
    - r = radius in meters
    - $\mu = \mu_0 \mu_\mathrm{r} \approx$ (4π x 10^{-7} H/m)(1) $\approx$ (4π x 10^{-7} H/m) (for non-ferromagnetic conductors)
    - For straight wires (does not consider curvature)



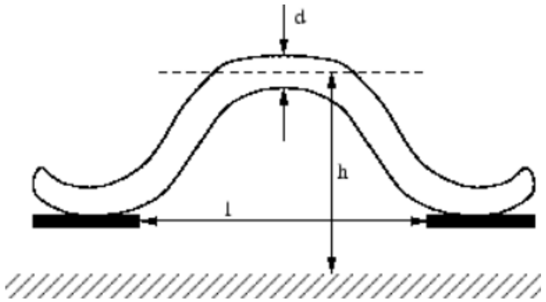
Self Inductance: Wire (Round Conductor)

When $l \gg r$:

- $L_{self} = 0.002l\left[\ln\left(\frac{2l}{r}\right) - \frac{3}{4}\right]$

  (µH) (cm)

  - $l =$ length in centimeters
  - $r =$ radius in centimeters
  - For straight wires (does not consider curvature)



- Rule of thumb for inductance of a wire per unit length:
  - Self inductance ~25 nH/in (~1 nH/mm = 10 nH/cm = 0.01 µH/cm)

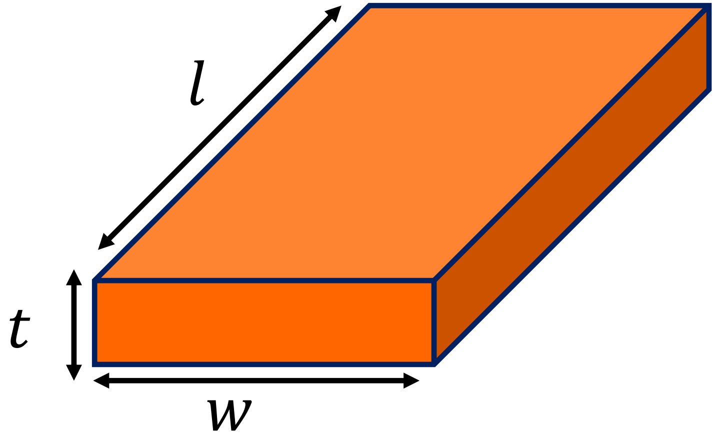
Self Inductance: Rectangular Conductor

- In case of DC, low frequency, or a thin rectangular conductor, Grover gives the following self inductance formula:

- $L_{self} = 0.002l\left(\ln\left(\frac{2l}{w+t}\right) + 0.50049 + \frac{w+t}{3l}\right)$

  (μH) (cm)

  - w = width in centimeters
  - l = length in centimeters
  - t = thickness in centimeters



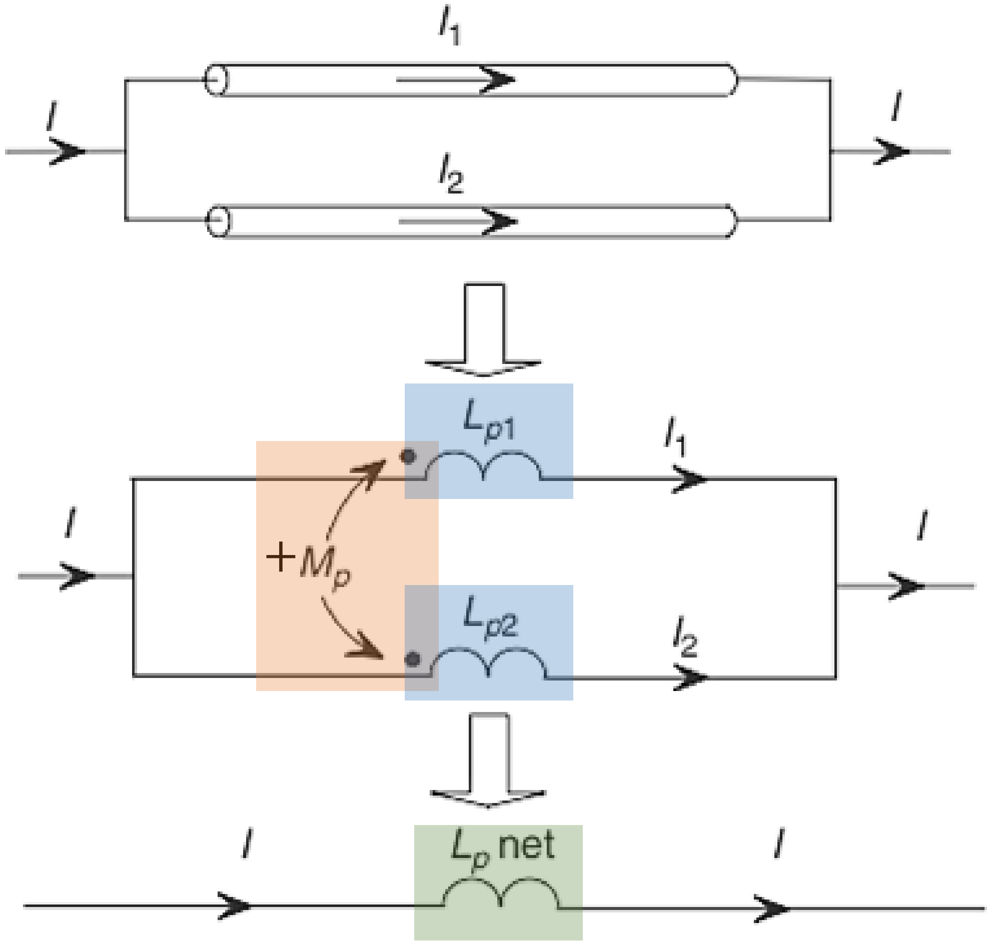
Example: Inductance of Parallel Wire Bonds

- If we have two identical wire bonds in parallel (electrically and physically), would $L_{eq} = L_p/2$?
  - Only if the wires are far apart!
  - If the wires are close together, there will be mutual inductance, M

$$L_{parallel} = \frac{L_{p1}L_{p2} - M^2}{L_{p1} + L_{p2} - 2M}$$

If $L_{p1} = L_{p2} = L_p$,

$$L_{parallel} = \frac{L_p + M}{2}$$



Mutual Inductance

- M = mutual inductance
  - Measure of shared field lines per amp of current in one conductor
- Crosstalk
  - Δi in one conductor induces V in the other
- Can increase total L for conductors carrying current in the same direction
- Return path cancellation could reduce total L

$$V_{induced} = M\frac{dI}{dt}$$

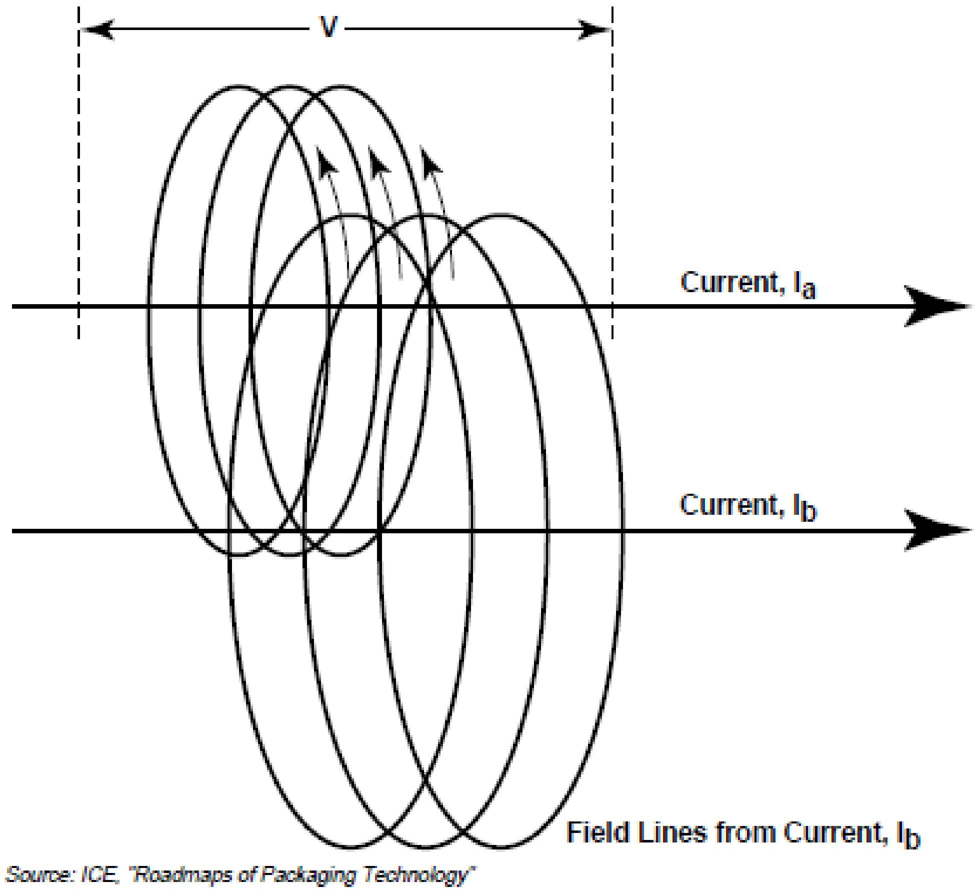


Figure 7-24. Origin of Mutual Inductance

Mutual Inductance

(μH)

- $M = 0.002l\left[\ln\left(\frac{l}{s}+\sqrt{1+\left(\frac{l}{s}\right)^2}\right)-\sqrt{1+\left(\frac{s}{l}\right)^2}+\frac{s}{l}\right]$

(cm)

  - $l =$ length in centimeters
  - $s =$ conductor spacing in centimeters

- When $s \ll l$: $M = \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{s}\right)-1\right]$

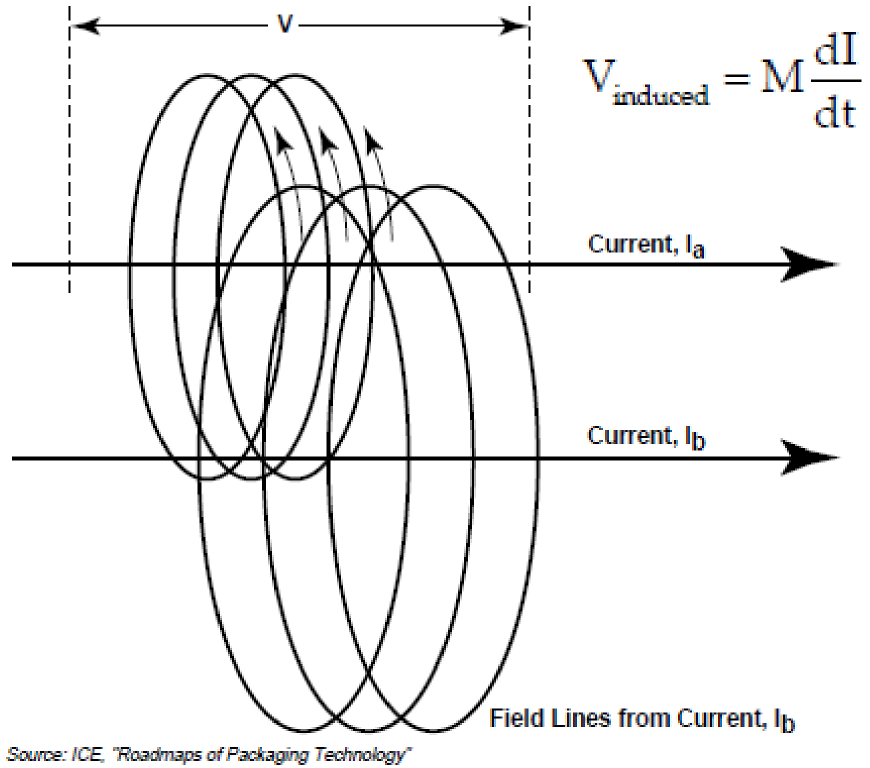


Figure 7-24. Origin of Mutual Inductance

Mutual Inductance

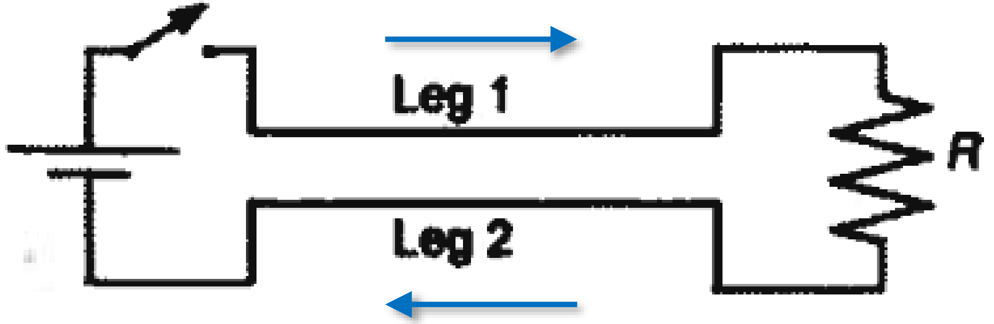
(μH)

- $M = 0.002l\left[\ln\left(\frac{l}{s} + \sqrt{1 + \left(\frac{l}{s}\right)^2}\right) - \sqrt{1 + \left(\frac{s}{l}\right)^2} + \frac{s}{l}\right]$

(cm)

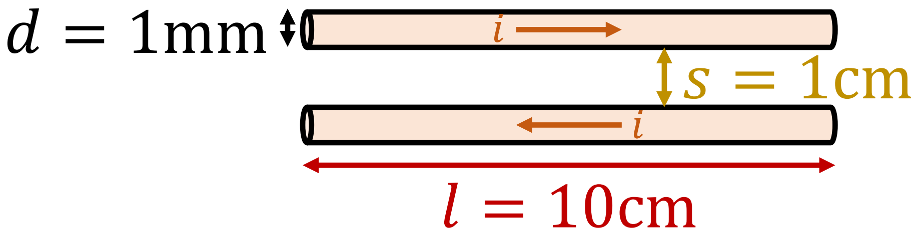
  - $l =$ length in centimeters
  - $s =$ conductor spacing in centimeters

- $V = L_1 \frac{dI}{dt} - M_{12}\frac{dI}{dt} + IR + L_2\frac{dI}{dt} - M_{12}\frac{dI}{dt}$
- $V = (L_1 + L_2 - 2M_{12})\frac{dI}{dt} + IR$



Example: Inductance of Adjacent Wires

- Find the equivalent inductance of two adjacent wires carrying current in opposite directions with 1-mm diameter, 10-cm length, and spaced 10 mm apart.



- For $r \ll l$ ($0.05\text{cm} \ll 10\text{cm}$), the self inductance of each wire is:

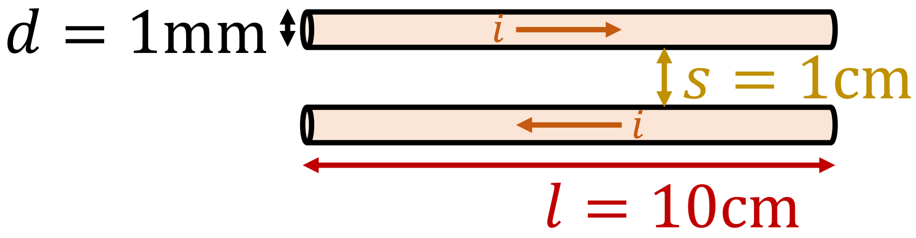
$$L(\mu H) = 0.002(10\text{cm})\left[\ln\frac{(2)(10\text{cm})}{0.05\text{cm}} - \frac{3}{4}\right] = 0.02[5.99 - 0.75] = \mathbf{0.105\ \mu H}$$

- For $s \ll l$ ($1\text{cm} \ll 10\text{cm}$), the mutual inductance is:

$$M = 0.002(10\text{cm})\left[\ln\left(\frac{2(10\text{cm})}{(1\text{cm})}\right) - 1\right] = \mathbf{0.040\ \mu H}$$

Example: Inductance of Adjacent Wires

- Find the equivalent inductance of two adjacent wires carrying current in opposite directions with 1-mm diameter, 10-cm length, and spaced 10 mm apart.



- Total inductance for the return circuit:

$$L_{eq} = L_1 + L_2 - 2M_{12}$$

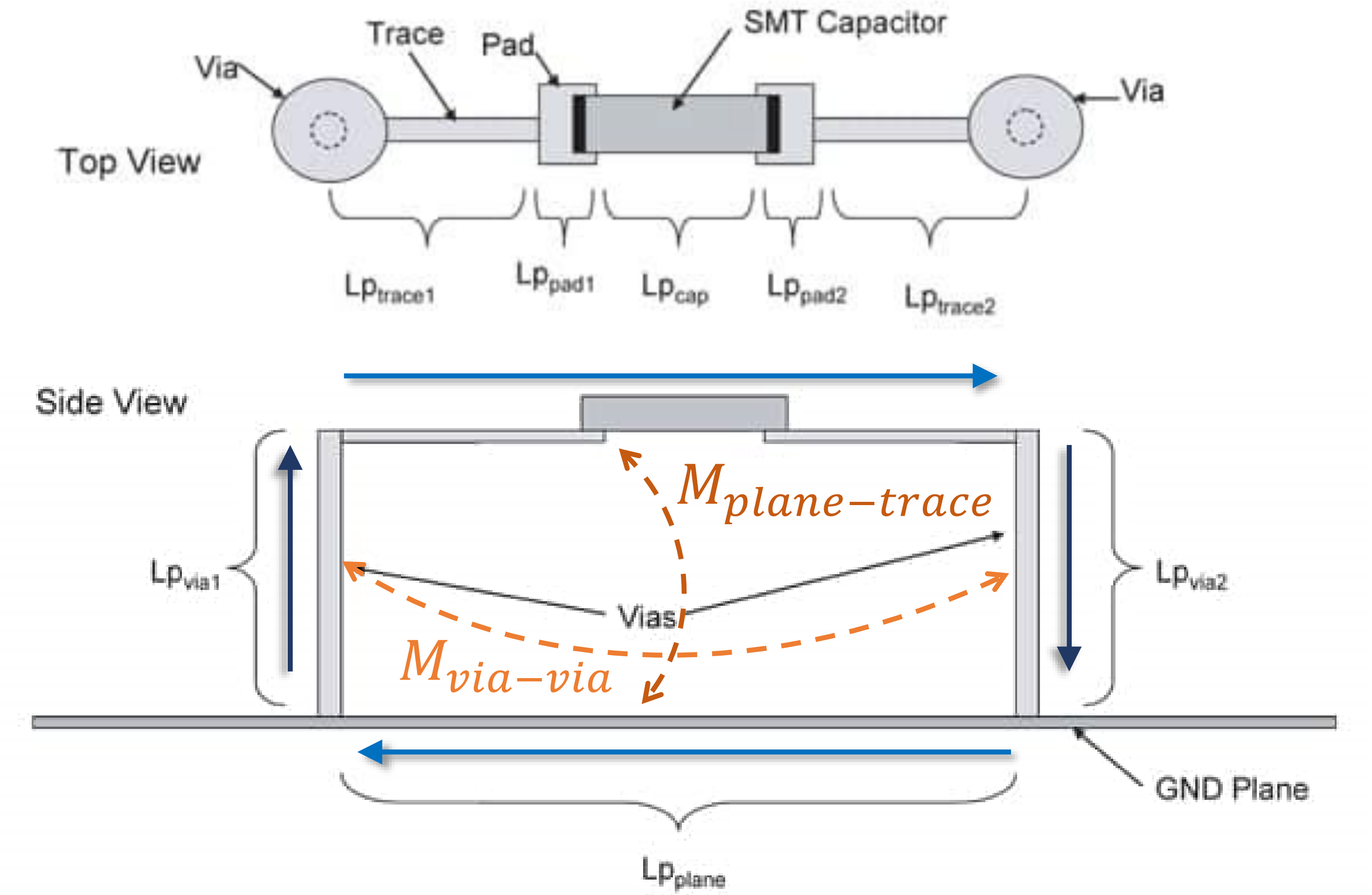
$$= 2(0.105\ \mu\text{H}) - 2(0.042\ \mu\text{H})$$

$$= \mathbf{0.126\ \mu H}$$

If s is very large such that M_{12} is negligible, then $L_{tot} = 2(0.105\ \mu\text{H})$

→ 40% reduction in L_{tot} due to M_{12}

Example: Capacitor Mounted to PCB

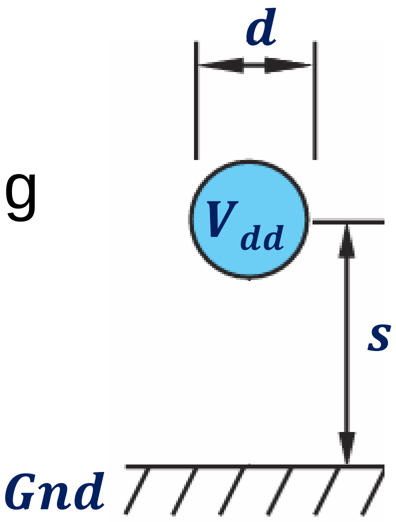


L_p = partial inductance
M = mutual inductance of parallel components

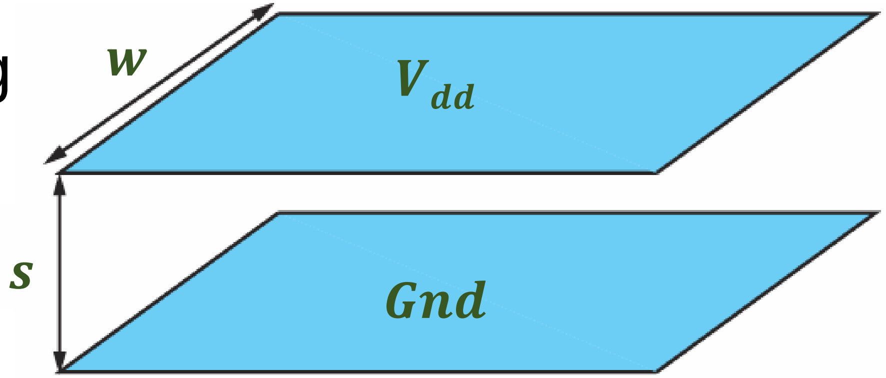
$$L_{total} = Lp_{trace1} + Lp_{pad1} + Lp_{cap} + Lp_{pad2} + Lp_{trace2} + Lp_{via2}$$
$$+ Lp_{plane} + Lp_{via1} - 2M_{via-via} - 2M_{plane-trace}$$

Effective Inductances for Different Structures

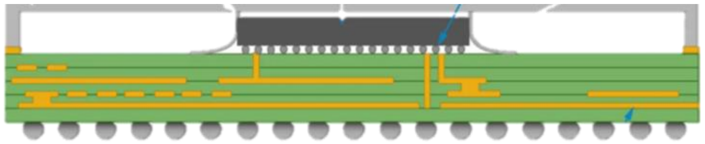
- Wire above a ground plane
  - $L_{eff} = \frac{\mu l}{2\pi} \cosh^{-1}\left(\frac{2s}{d}\right)$, where l= length, d= diameter, s= spacing
  - Package examples: TAB, QFP w/ ground plane
  - Typical inductance range: 1 – 10 nH
  - Assumes $s \ll l$, and $d \ll s$



- Parallel planes
  - $L_{eff} = \frac{\mu l s}{w}$, where l= length, w= width, s= spacing
  - Package examples: PGA, BGA
  - Typical inductance range: 0.25 – 1 nH
  - Assumes $s \ll l$

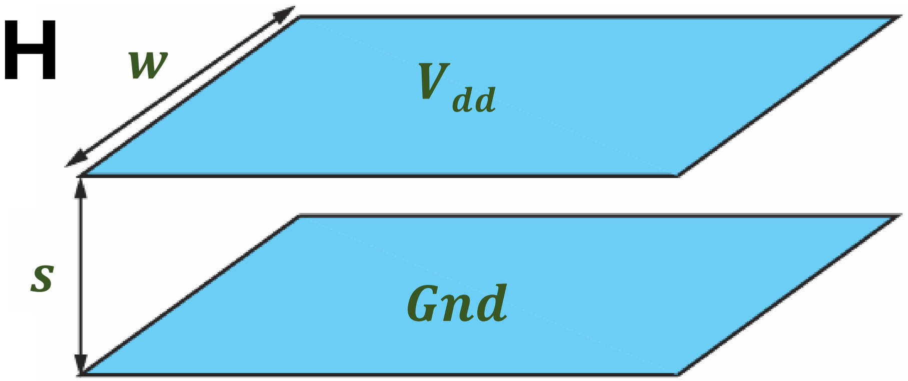


Example: Parallel Planes



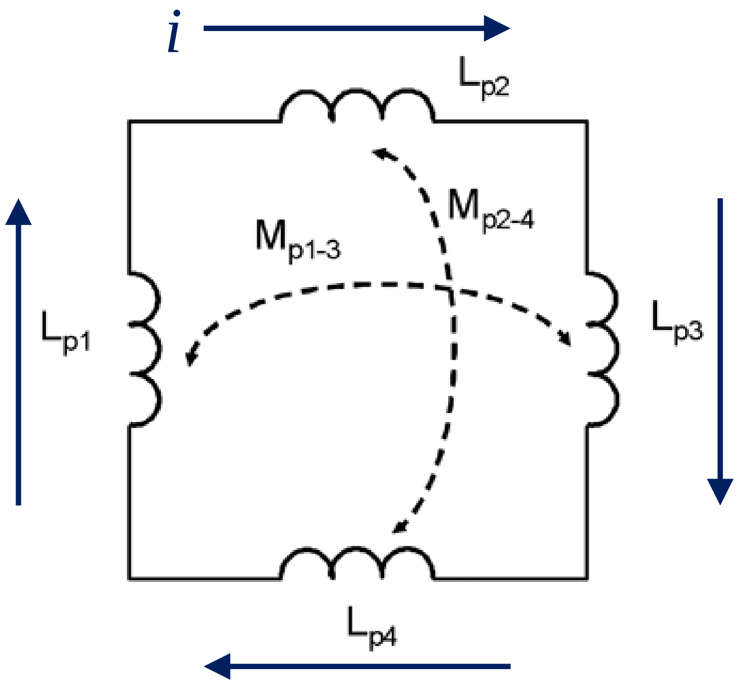
A multi-layer ball grid array (BGA) package has copper plane layers used to supply both the V_{dd} and the ground (GND). Find the effective inductance for a pair of planes with dimensions of 1 cm by 1 cm, and a spacing of 6 mils.

- $L_{eff} = \frac{\mu l s}{w}$, where $l = w = 1$ cm $= 0.01$ m, $s = 6$ mils $= 1.5$e-4 m
- $\mu = \mu_0 \mu_r \approx 4\pi \times 10^{-7}\mathrm{H/m}$ =1.26e-6 H/m
- L_{eff} =(1.26e-6 H/m)(1.5e-4 m) $=$ **0.19 nH**



$V = L\, dI/dt$

Summary: Inductance

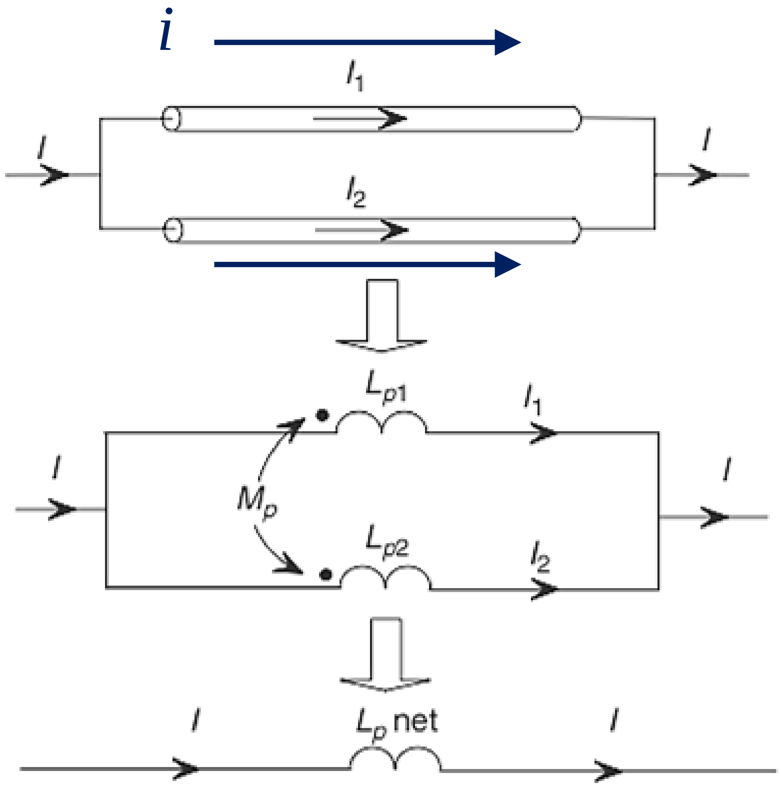


- Inductive delay: $\tau = L/R$
- Self inductance: L_p
  - Example: $L_{p1},\ L_{p2},\ L_{p3},\ L_{p4}$
- Mutual inductance: M
  - Example: $-M_{p1-3}\,, -M_{p2-4}$
  - Subtractive: current flowing in opposite directions (this example)
- Loop inductance: L_{total}
- Example: $L_{total} = L_{p1} + L_{p2} + L_{p3} + L_{p4} - 2M_{p1-3} - 2M_{p2-4}$

$\boxed{V = L\, dI/dt}$

Summary: Inductance

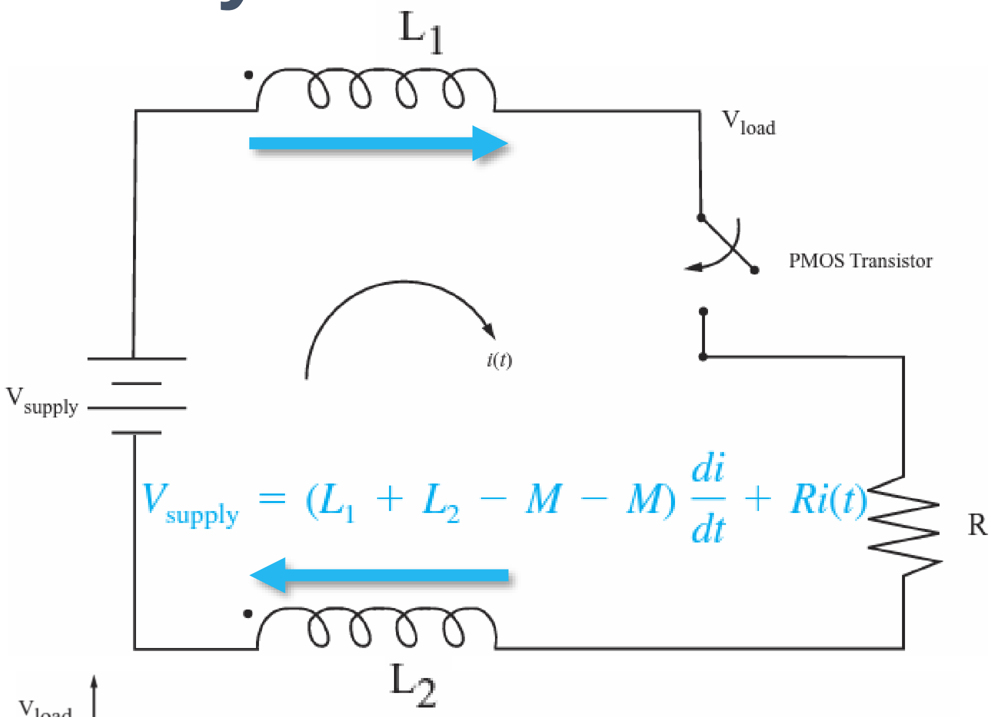
- Example 2: Additive
  - Two parallel wires with current in the same direction
  - Self inductance: $L_{p1},\ L_{p2}$
  - Mutual inductance: M
    - Positive
    - If $s \ll l$: $M = \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{s}\right) - 1\right]$
  - Total inductance if $L_{p1} = L_{p2}$:
    - $L_{parallel} = (L_p + M)\ /\ 2$

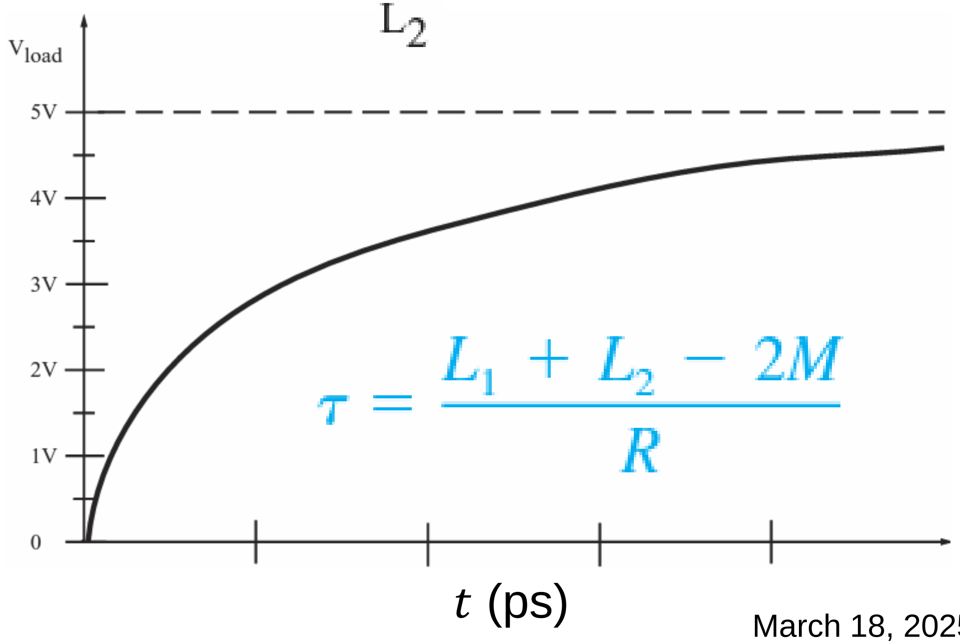


Example: Inductive Delay

- Assume that the source and return paths are close enough such there is 2 nH of mutual inductance between them.
- $V_{dd} = 5$ V, $R = 50\ \Omega$, $L_1 = L_2 = 5$ nH, $\boldsymbol{M}$ **= 2 nH**
- L_{total} = (2)(5 nH) – (2)(2 nH)= 6 nH
- $\tau = L_{total}/R$ = 6 nH / 50 Ω = **0.1 ns**

➢ Subtractive M reduces L_{eff} and τ





dI/dt or ΔI Noise

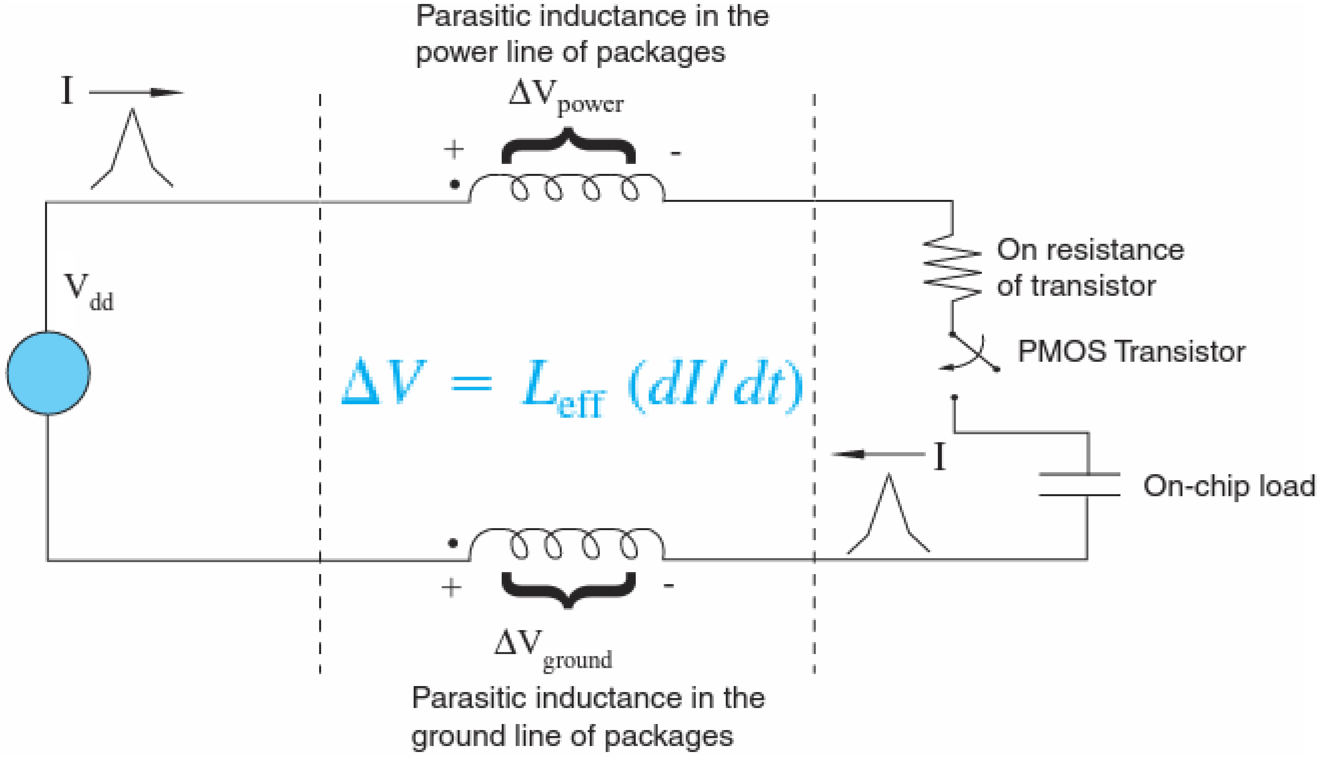
- Transient currents (through interconnects, leads, traces) cause voltage fluctuations on power supply rails due to parasitic inductances
- This is *simultaneous switching noise (SSN)* or dI/dt noise or ΔI noise
- Required charge to energize load to supply voltage V_{dd}: $Q = C \cdot V_{dd}$
- Current draw: $\Delta I = C \cdot V_{dd} / \Delta t$
- If there are N gates switching simultaneously, the current draw from the power supply becomes $\Delta I = N \cdot C \cdot V_{dd} / \Delta t$
- $\Delta V = L\left(\frac{dI}{dt}\right) \rightarrow \Delta I = \Delta V \cdot \Delta t / L_{max}$
- Maximum acceptable inductance: $L_{max} = \Delta t^2 \cdot \Delta V / (N \cdot C \cdot V_{dd})$

Example: dI/dt Noise

- A power supply is supplying 5 CMOS chips with 1 pF load each and a switching time of 1 ns. What is the maximum allowable parasitic inductance L_{max} between the power supply and the chips to achieve a variation in the power supply voltage V_{dd} of ≤ 1 %?
- $L_{max} \leq \Delta t^2 \, \Delta V \;/\; N \, C \, V_{dd}$
- $L_{max} \leq (1\,\mathrm{ns})^2 (0.01)(V_{dd}) \;/\; ((5)(0.001\,\mathrm{nF})V_{dd})$ = **2 nH**

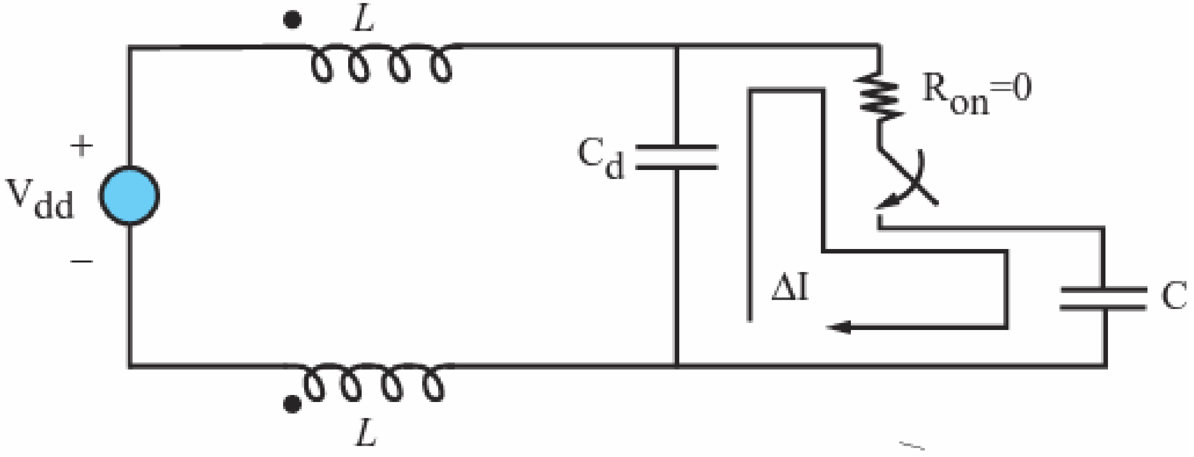
What if the chip is a single power device with load of 1 nF and 10 ns switching, and ≤ 10 % V_{dd} variation is acceptable?

- $L_{max} \leq (10\,\mathrm{ns})^2 (0.1)(V_{dd}) \;/\; ((1\,\mathrm{nF})V_{dd})$ = **10 nH**

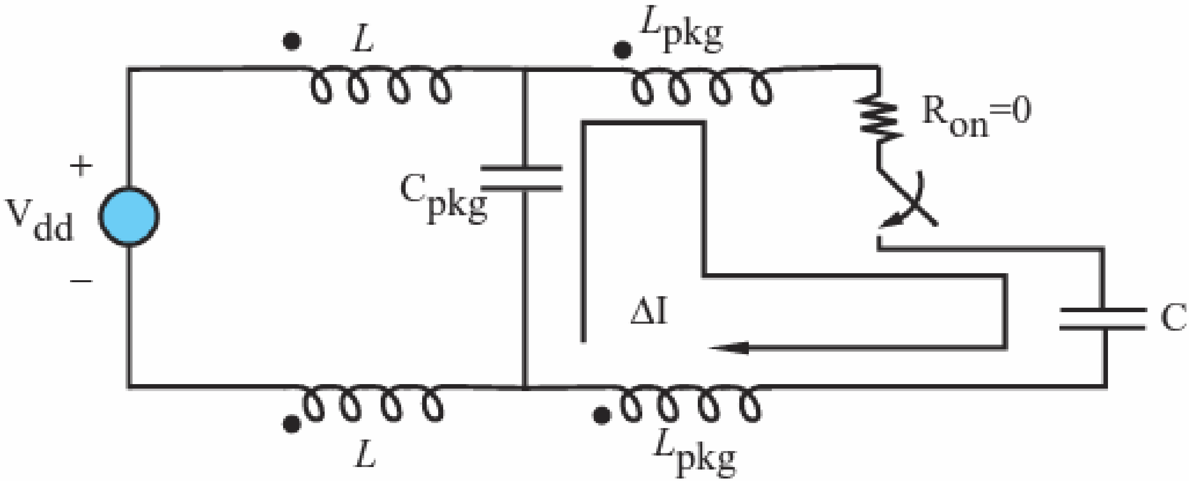


Decoupling Capacitors

On Chip



On Package



Example: $L = 10$ pH, 1000 circuits draw 10 A in 0.25 ns.

Find the noise voltage.

- ΔV = **400 mV**

$$\Delta V = L_{\text{eff}}\,(dI/dt)$$

Design C_{pkg} to reduce the noise voltage to *200 mV*.

$$C = \Delta I\,\Delta t/\Delta V$$

- C_{pkg} = **12.5 nF**

If $L_{pkg} = 5$ pH, find the frequency above which C_{pkg} loses effectiveness.

$$f_{\text{max}} = \frac{1}{2\pi\sqrt{2L_{\text{pkg}}C_{\text{pkg}}}}$$

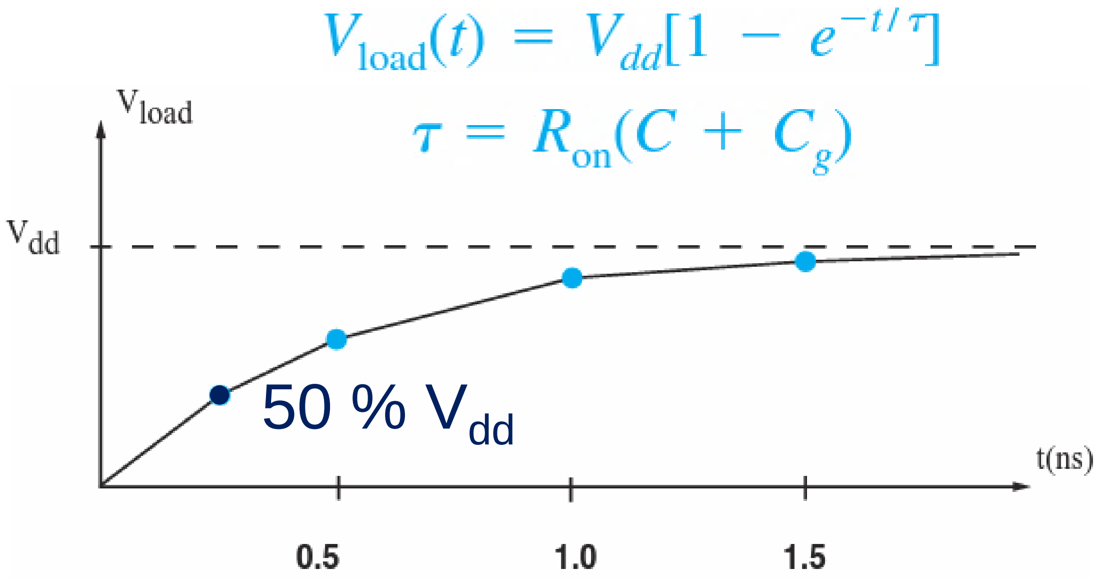
- f_{max} = **637 MHz**

Example: Capacitive Delay

- V_{dd} = 5 V; R_{on} = 50 Ω; $C + C_g$ = 10 pF
- $\tau = RC_{total}$ = (50 Ω)(10 pF) = **0.5 ns**

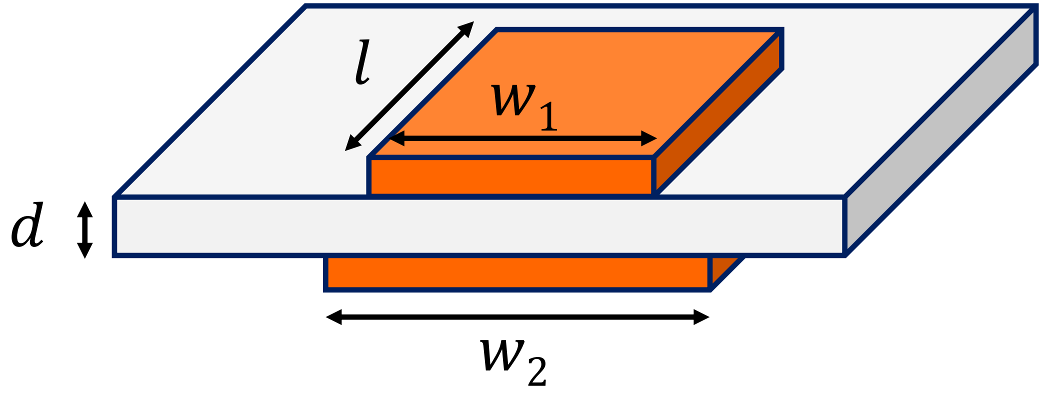
How long will it take for V_{load} to rise to 50 % of V_{supply}?

- $V_{load}(t) = V_{dd}[1 - e^{-t/\tau}]$
- $-\ln$ (1 – (0.5)(5 V)/5 V) = 0.69
- $t_{50\%}$ = 0.69τ = **0.35 ns**
- $t_{90\%}$ = 2.3τ = **1.15 ns**



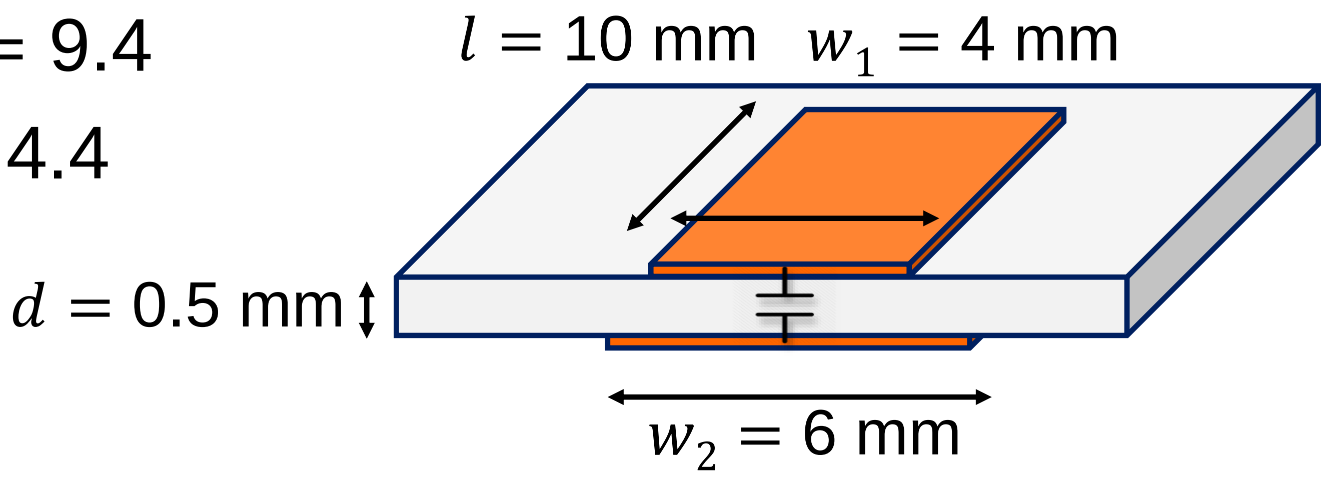
Capacitance (Overlapping Conductors)

- $Q = CV$
- Taking derivative:
  - $I = dQ/dt$
  - $I = C\,dV/dt$
- $C = \varepsilon A/d$
  - $\varepsilon =$ permittivity
    - $\varepsilon = \varepsilon_r \varepsilon_0$
      - $\varepsilon_0 =$ 8.86 x 10^{-12} F/m, permittivity of free space
      - $\varepsilon_r =$ relative permittivity or dielectric constant (material property)
  - $A =$ overlapping area
  - $d =$ distance



Example: Capacitance (Overlapping Conductors)

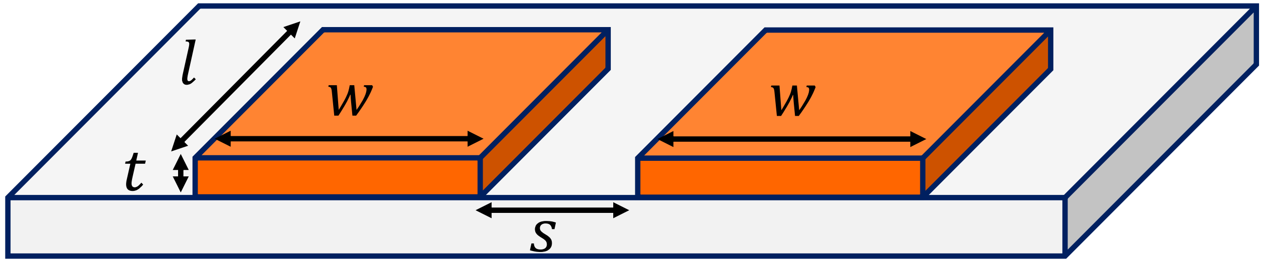
- Al_2O_3 substrate (e.g., DBC): $\varepsilon_r = 9.4$
- FR4 substrate (e.g., PCB): $\varepsilon_r = 4.4$
- $C = \varepsilon A/d = \varepsilon_0 \varepsilon_r A/d$
  - $\varepsilon_0 = 8.86 \times 10^{-12}$ F/m
  - $A = 10$ mm x 4 mm= 40 mm^2
  - $C = (8.86 \times 10^{-12}$ F/m$)(\varepsilon_r)(4 \times 10^{-5}$ m$^2)$ / (0.0005 m)
  - C_{Al2O3} = 6.7 pF (Q3D: 7.7 pF)
  - C_{FR4} = 3.12 pF (Q3D: 3.7 pF)



➢ Substrate materials with higher relative permittivity (dielectric constant) have higher parasitic capacitance

Example: Capacitance (Adjacent Conductors)

- Formula for adjacent conductors with equal widths:
- $C' = 0.122\ t/s + 0.0905\ (1 + \varepsilon_r)a$ [pF/cm]
- $a = \log\left(1 + 2\ w/s + 2\sqrt{w/s} + w^2/200\right)$
- s = distance between two adjacent conductors, mm
- t = thickness, mm
- w = conductor width, mm
- ε = permittivity
- $C = C'l$
- l = parallel running length, cm



Example: Capacitance (Adjacent Conductors)

- $C' = 0.122\ t/s + 0.0905\ (1 + \varepsilon_r)a$ [pF/cm]
- $a = \log\left(1 + 2\ w/s + 2\sqrt{w/s} + w^2 / 200\right)$
- $C = C'l$

Find the capacitance between the adjacent traces.

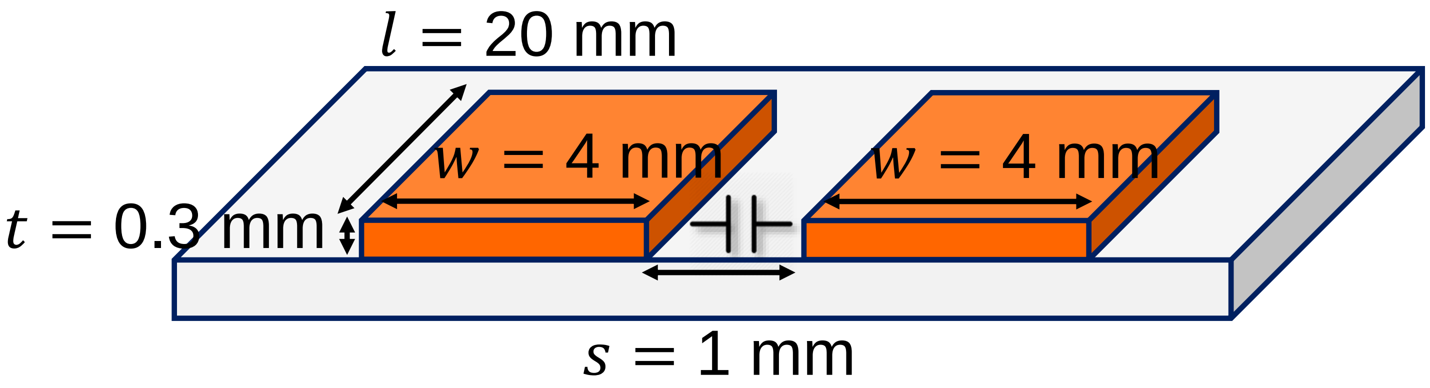
Al$_2$O$_3$ substrate (e.g., DBC): $\varepsilon_r = 9.4$

$C' = 1.1$ pF/cm

$C =$ **2.2 pF**

(Q3D: 1.3 pF for t_{Al2O3} = 1 mm)

(Q3D: 2.1 pF for t_{Al2O3} = 5 mm)



Transit Time of Electrical Signal

- Electrical signals propagate at the speed of light (3×10^8 m/s in air)
- Kirchhoff's Laws neglect the finite velocity of electrical signals, and therefore fail when the time delay or phase shift due to that finite velocity becomes significant
- E.g., in air, there is ~1 ns time delay per 1 ft of travel
  - This is significant if the clock rate of the circuit is 1 GHz
- Transmission line theory accounts for this delay
- Speed of light is slower in dielectric packaging materials than in air

Propagation Delay & Time Delay

- The propagation velocity of any electrical signal in a material is

$$v_p = \frac{c}{\sqrt{\varepsilon_r \mu_r}} \quad [\mathrm{m/s}]$$

where $c = 2.998 \times 10^8\ \mathrm{m/s}$ (speed of light in a vacuum) and $\frac{1}{\sqrt{\varepsilon_r \mu_r}}$ is the velocity factor; for non-magnetic media, the expression simplifies to $\frac{c}{\sqrt{\varepsilon_r}}$

- The propagation delay is $\frac{\sqrt{\varepsilon_r \mu_r}}{c} \quad [\mathrm{s/m}]$
- The time delay is the propagation delay times the length: $\frac{\sqrt{\varepsilon_r \mu_r}}{c} \times l \quad [\mathrm{s}]$
- Wavelength: $\lambda = c/f$ in air, where f is the frequency in Hertz
- The wavelength λ of a single-frequency signal in a medium with parameters ε_r and μ_r:

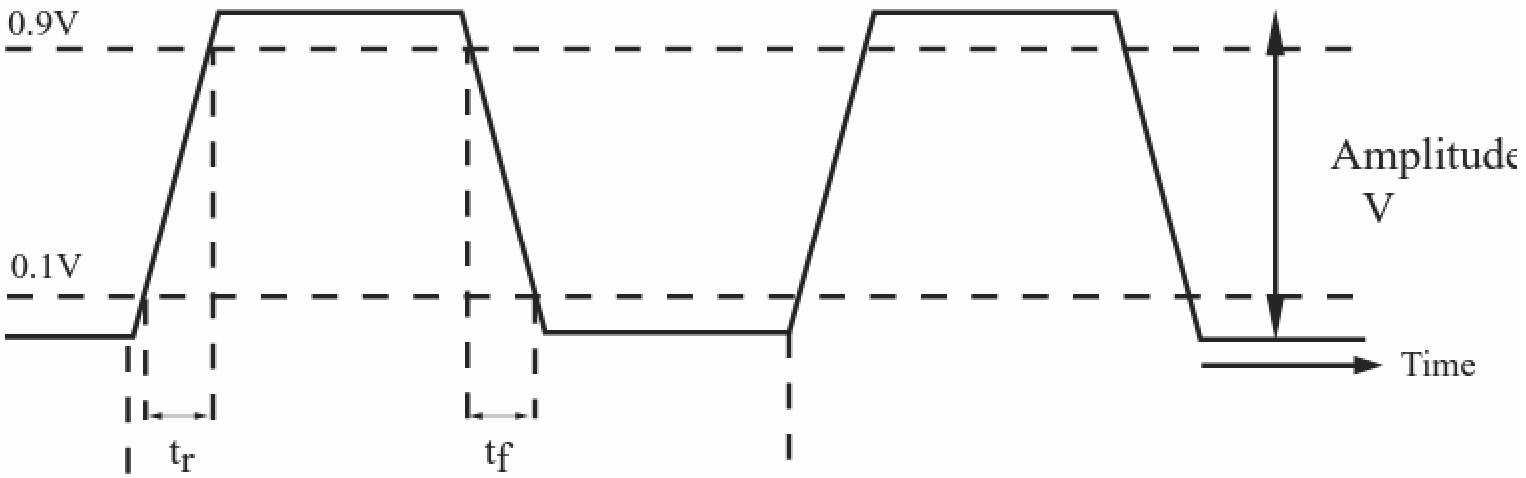
$$\lambda = \frac{c}{f\sqrt{\varepsilon_r \mu_r}} \quad [\mathrm{m}]$$

Transmission Line Consideration

- The propagation delay for package interconnects may not be negligible if the signal rise times t_r are *fast*
- Transmission line effects should be considered if the time delay of the interconnect is *greater* than the rise time of the signal
- Another way to think about it: the wavelength λ of the signal should be *greater* than the length of the interconnect l (the length the signal needs to travel)
- Check for transmission line effects by comparing:

Time delay to rise time t_r or Wavelength λ to length l

Consider Transmission-Line Effects When…



Waveforms are "fast" or Interconnects are "long"

$$t_r \leq (33.3\ \mathrm{ps/cm})\sqrt{\varepsilon_r} \times 2l$$

round-trip length

$$l > \frac{0.5\ t_r}{(33.3\ \mathrm{ps/cm})\sqrt{\varepsilon_r}}$$

where t_r = signal rise time (ps) ; l = interconnect length (cm)

- For an interconnect to behave as a transmission line, $\boldsymbol{t_r}$ has to be **less than** the **round-trip ($2l$) time delay** of the interconnect.

Example: Transmission Line Check

For 500 MHz clock with a rise time of 200 ps and 2 cm interconnect in $\varepsilon_r = 4$, should the transmission line effects be considered?

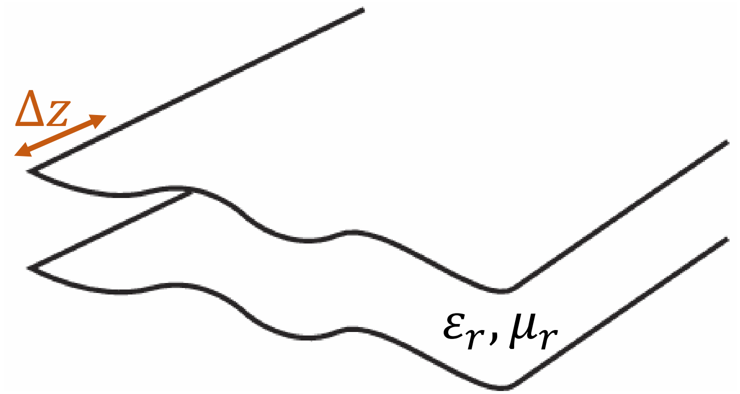
- Time approach: $t_r \leq (33.3\ \mathrm{ps/cm})\sqrt{\varepsilon_r} \times 2l$
  - $t_r = 200$ ps
  - $t_r \leq 33.33\sqrt{4}$ (2)(2 cm) = **266 ps** → $t_r = $ **200 ps < 266 ps**

- Length approach: $l > \dfrac{0.5\ t_r}{(33.3\ ps/cm)\sqrt{\varepsilon_r}}$
  - $l > 0.5(200\ \mathrm{ps}) / (33.33)\sqrt{4}$ = **1.5 cm** → $l = $ **2 cm > 1.5 cm**

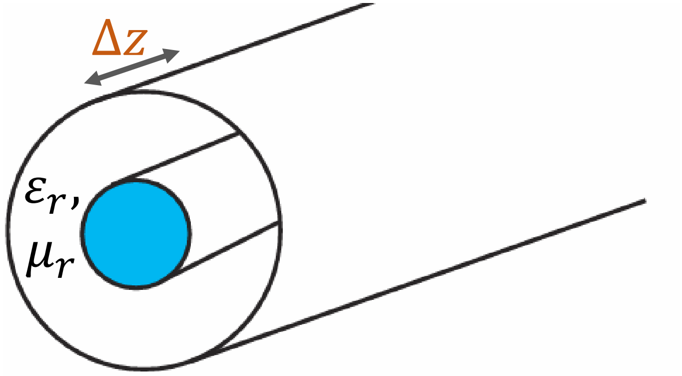
➢ Yes, transmission line effects should be considered!

Transmission Line Equivalent Circuit

Parallel Conducting Strips



Coaxial Cable

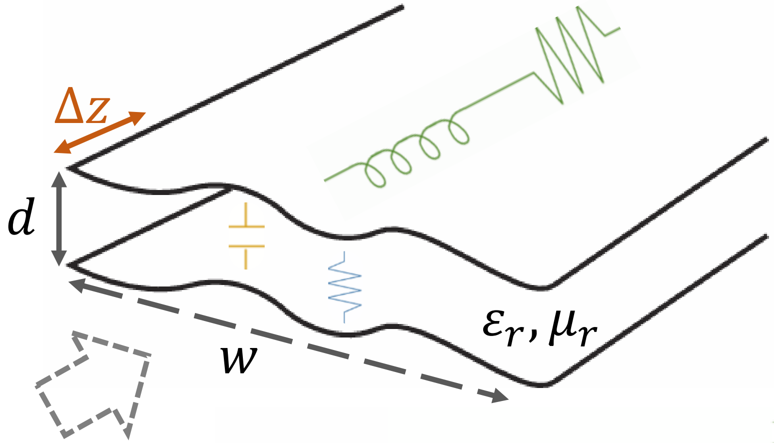


- We can draw the equivalent circuit for a short section Δz of the transmission line, where $\Delta z << \lambda$
- The equivalent circuit for section Δz will provide the time delay and phase shift
- Using circuit theory, we can assume that the Δz equivalent circuits provide a direct connection from one end to the other
- This equivalent circuit can be treated using KVL and KCL

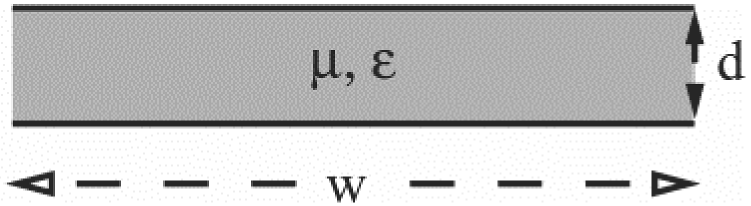
Tummala, 2.3.3

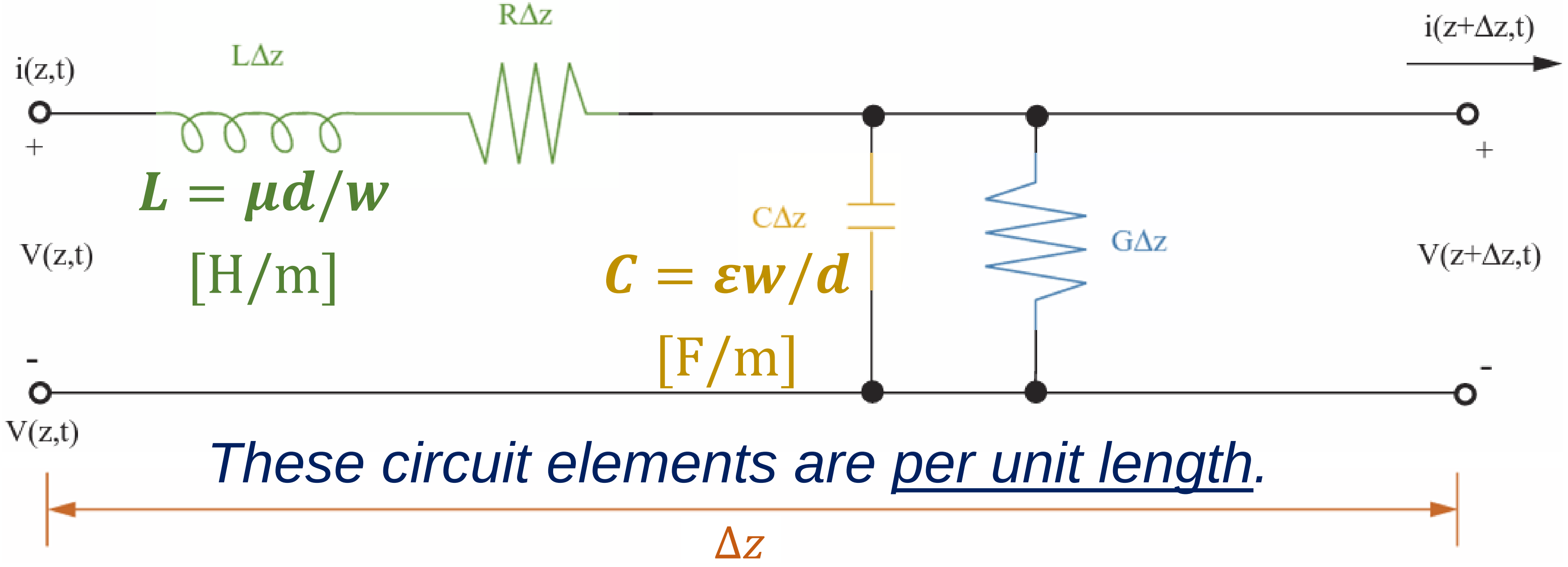
Transmission Line Equivalent Circuit

(Ideal) Parallel Conducting Strips



Front View





$$L = \mu d / w$$

[H/m]

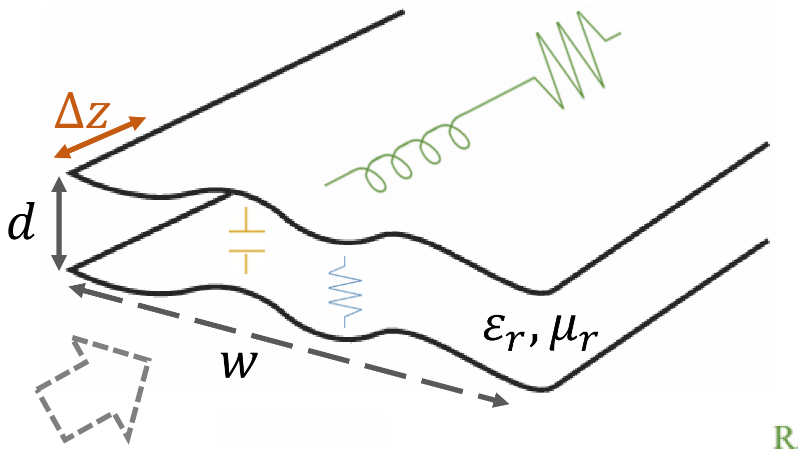
$$C = \varepsilon w / d$$

[F/m]

These circuit elements are <u>per unit length</u>.

Example

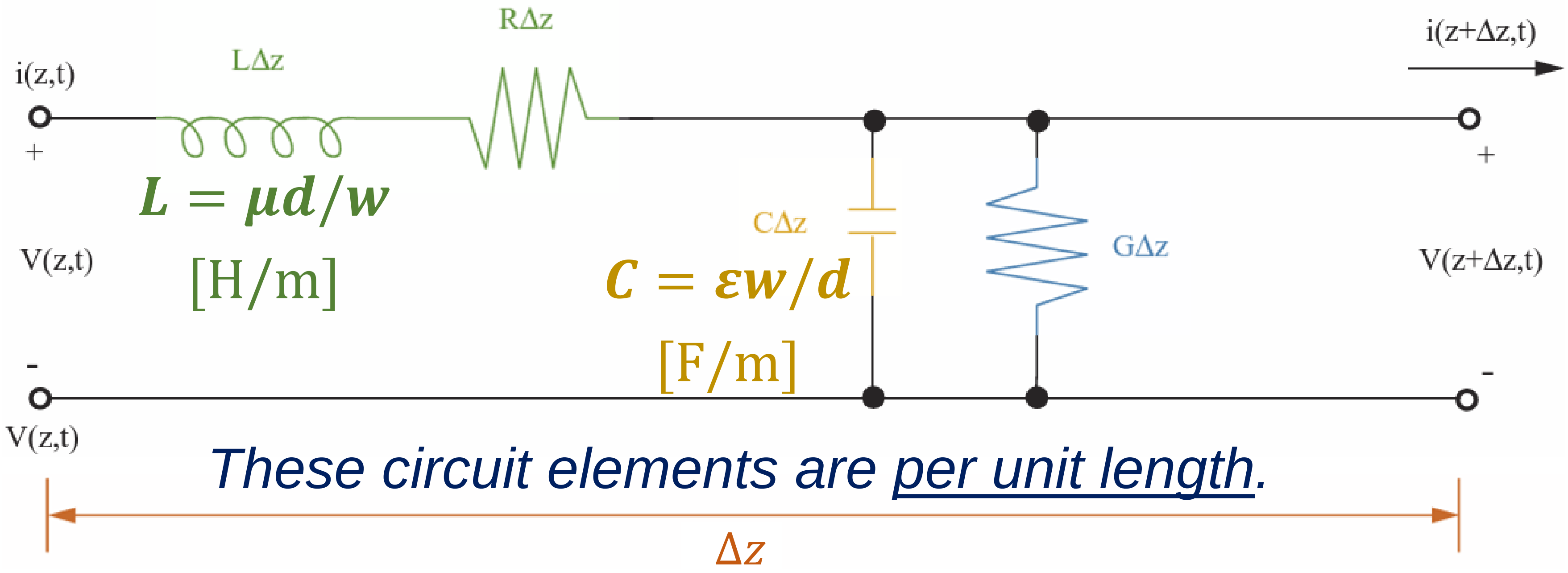
(Ideal) Parallel Conducting Strips



The total interconnect length is 1 cm, and Δz is 0.1 µm such that it satisfies $\Delta z \ll \lambda$.

Find the number of Δz segments.

- $l/\Delta z = 1\ \mathrm{cm}/0.1\mathrm{\mu m} = \mathbf{100,000\ segments}$



$L = \mu d/w$ [H/m]

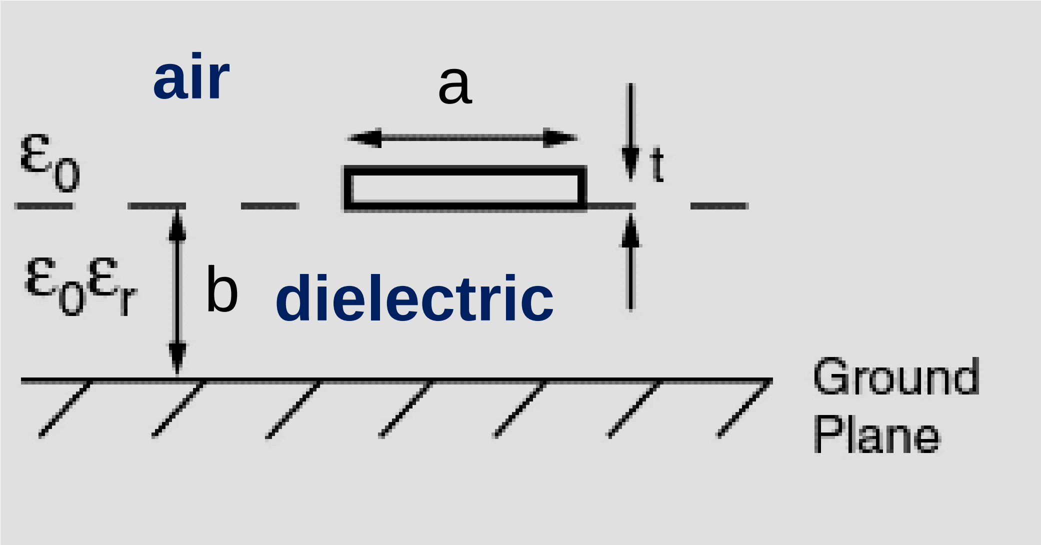
$C = \varepsilon w/d$ [F/m]

These circuit elements are <u>per unit length</u>.

Tummala, 2.3.5

Microstrip Transmission Line

Microstrip Structure



Transmission Line Formulas

$$\varepsilon_{\text{eff}} = \varepsilon_0 \left[\frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12b/a}} \right]$$

$$v_p = \frac{1}{\sqrt{\mu \varepsilon_{\text{eff}}}}$$

$$Z_0 = \frac{1}{2\pi} \sqrt{\frac{\mu}{\varepsilon_{\text{eff}}}} \ln\left(\frac{8b}{a} + \frac{a}{4b}\right) \qquad a < b$$

$$Z_0 = \sqrt{\frac{\mu}{\varepsilon_{\text{eff}}}} \frac{1}{\frac{a}{b} + 1.393 + 0.667 \ln\left(\frac{a}{b} + 1.444\right)} \qquad a > b$$

Effective permittivity, ε_{eff}

$\varepsilon = \varepsilon_0 \varepsilon_r$, where ε_r = relative dielectric constant and $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm

$\mu = \mu_0 \mu_r$, where μ_r = relative permeability and $\mu_0 = 4\pi \times 10^{-9}$ H/cm

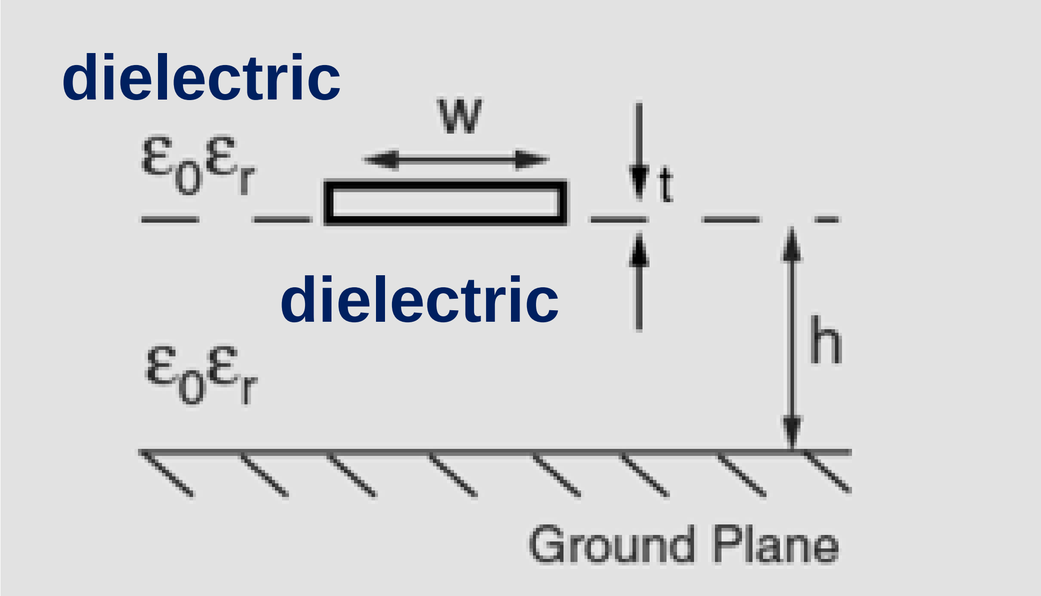
Propagation velocity, v_p in cm/s

Characteristic impedance, Z_0 in Ω

a and *b* in cm

Embedded Microstrip Transmission Line

Embedded Microstrip Structure



Transmission Line Formulas

$$v_p = \frac{1}{\sqrt{\mu\varepsilon}}$$

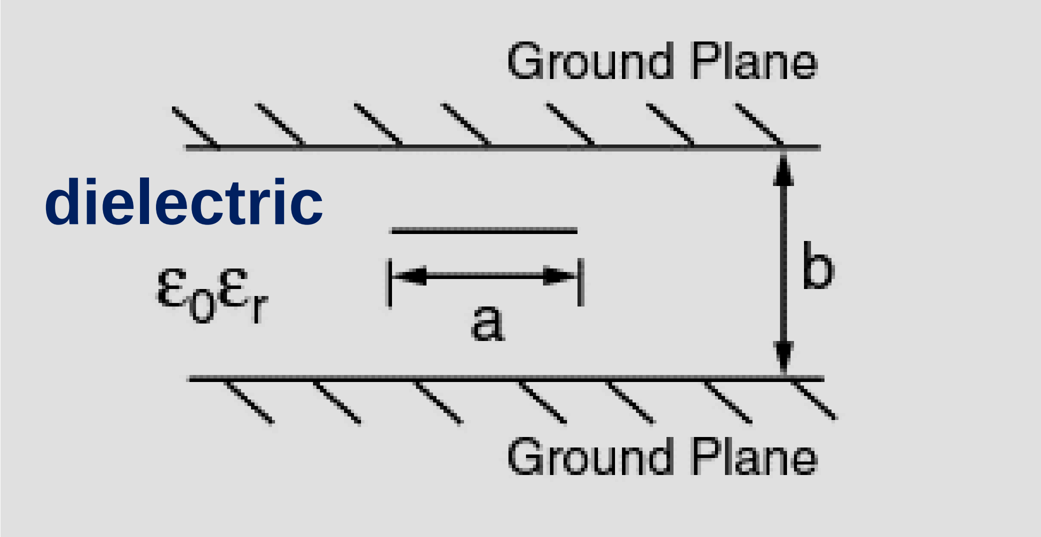
$$Z_0 = \frac{60}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

$\varepsilon = \varepsilon_0\varepsilon_r$, where ε_r = relative dielectric constant and $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm
$\mu = \mu_0\,\mu_r$, where μ_r = relative permeability and $\mu_0 = 4\pi \times 10^{-9}$ H/cm
Propagation velocity, v_p in cm/s
Characteristic impedance, Z_0 in Ω
h, t, and *w* in cm

Tummala, 2.3.5

Stripline Transmission Line

Stripline Structure



Transmission Line Formulas

$$v_p = \frac{1}{\sqrt{\mu\varepsilon}}$$

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{b}{a_{\text{eff}} + 0.441b}$$

$$a_{\text{eff}} = \begin{cases} a & a > 0.35b \\ a - \left(0.35 - \frac{a}{b}\right)^2 b & a < 0.35b \end{cases}$$

Effective dimension, a_{eff} in cm

$\varepsilon = \varepsilon_0\varepsilon_r$, where ε_r = relative dielectric constant and $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm

$\mu = \mu_0\, \mu_r$, where μ_r = relative permeability and $\mu_0 = 4\pi \times 10^{-9}$ H/cm

Propagation velocity, v_p in cm/s

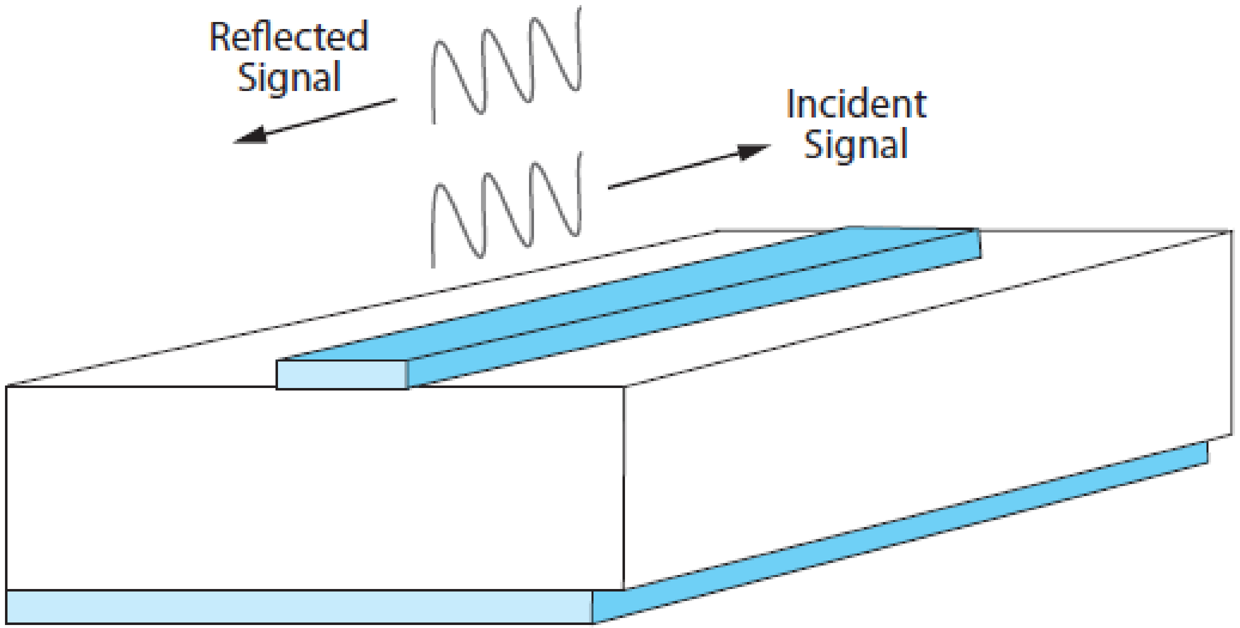
Characteristic impedance, Z_0 in Ω

a and *b* in cm

The stripline is centered between the two ground planes

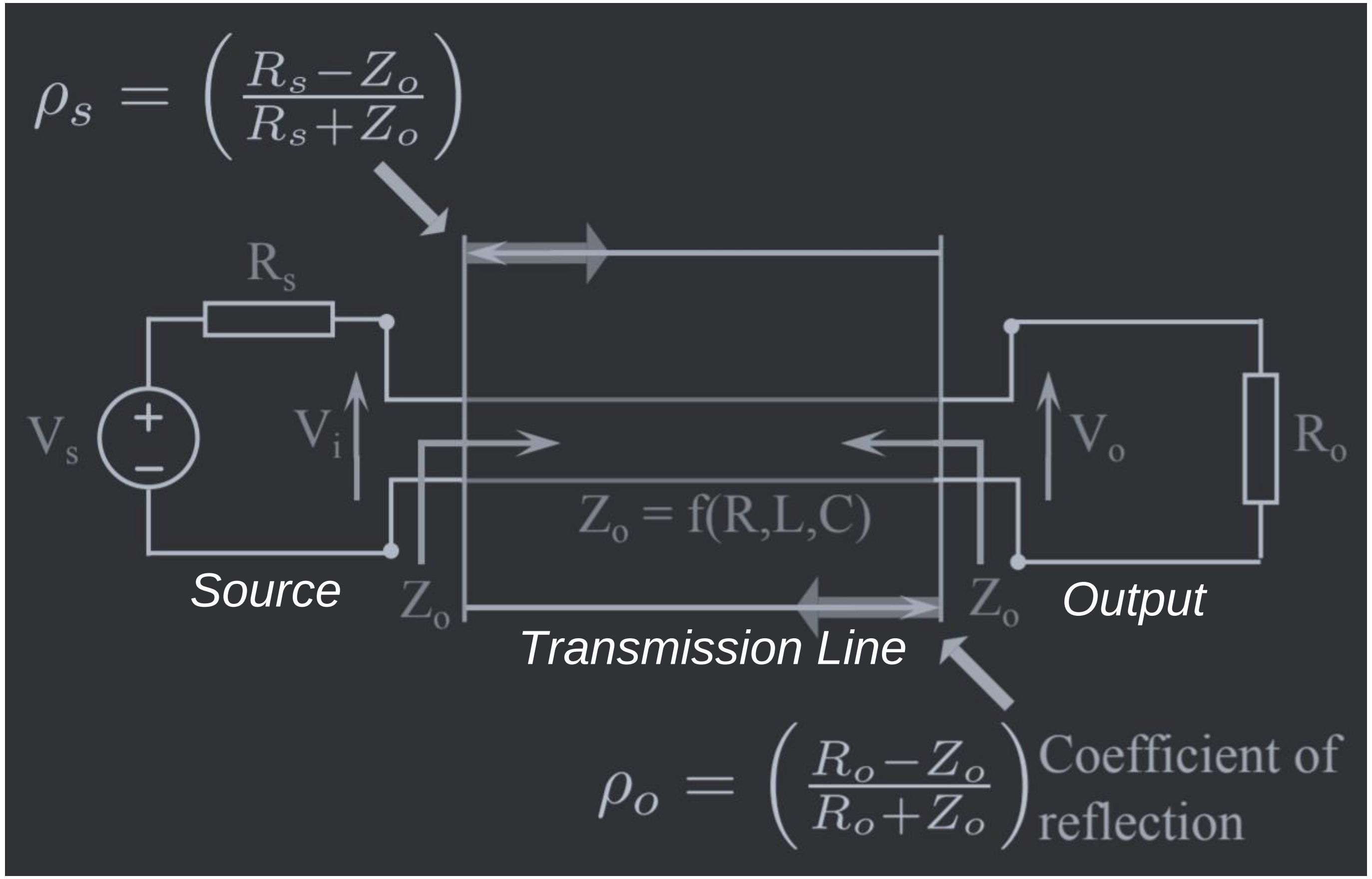
Reflection

- When a signal traveling in a transmission line encounters a change in impedance, a reflected signal is generated
- Any mismatch in impedance (e.g., from a termination) will generate a reflection
- For RF or microwave designs, reflections and standing waves are minimized by terminating the line with an impedance equal to the line wave impedance



Reflection

- When a signal traveling in a transmission line encounters a change in impedance, a reflected signal is generated
- ρ = reflection coefficient
- When $R_s = Z_0$, $\rho_s = 0$
- When $R_o = Z_0$, $\rho_o = 0$



Reducing Transmission Line Effects

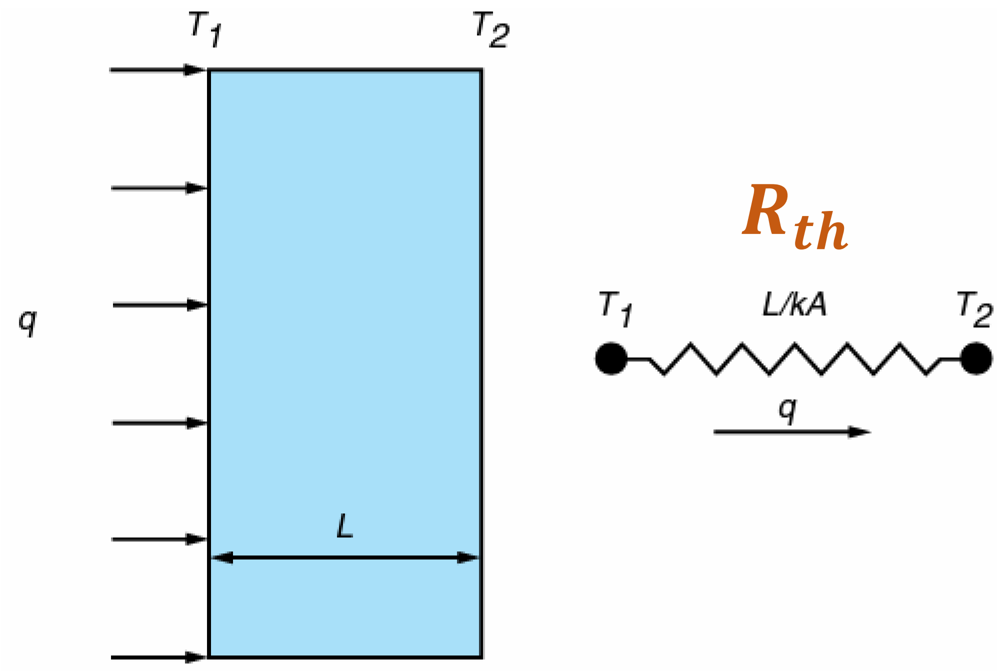
- Slow down rise times such that $t_r > (33.3\ \mathrm{ps/cm})\,\sqrt{\varepsilon_r} \times 2l$
  - Minimizes impact of the line delay on the circuit performance
- Use materials with low dielectric constant ε_r
  - Increases propagation velocity/reduces delay $v_p = 1/\sqrt{LC}$
- Reduce length of the line such that $l < 0.5\, t_r/(33.3\ \mathrm{ps/cm})\,\sqrt{\varepsilon_r}$
  - Minimizes impact of the line delay on the circuit performance
  - Reduces transmission line losses
- Match impedances
  - Reduces reflection
  - Vary parasitic L and C by changing the line geometry $Z_0 = \sqrt{L/C}$

Modes of Thermal Transport

- **Conduction** $$q = \frac{kA_c \Delta T}{L}$$
  - Flow of heat from a region of higher temperature to a region of lower *temperature* ***within a solid, stationary liquid,*** *or* ***static gaseous medium***
  - Direct energy exchange among molecules
- **Convection** $$q = hA_s \Delta T$$
  - Transfer of heat from a solid to a ***fluid in motion***
  - Mechanisms:
    - Exchange among nearly-stationary molecules adjacent to the solid surface (as in conduction)
    - Transport of heat away from the solid surfaces by the bulk motion of the fluid
- **Radiation** $$Q = \varepsilon \sigma F_{12} A_s \left(T_1^4 - T_2^4\right)$$
  - Heat transfer is a result of the ***emission and absorption*** of the energy contained in the electromagnetic waves or photons
  - Can occur across a vacuum or any medium that is transparent to infrared wavelengths
  - Not linearly dependent on the temperature difference

Thermal Resistance R_{th}

- Fourier's Law is analogous to Ohm's Law:
  - Heat $q \rightarrow$ current I
  - Temperature drop $\Delta T \rightarrow$ voltage drop ΔV
  - Thermal resistance $R_{th} \rightarrow$ electrical resistance R



Thermal:

$$\Delta T = qR_{th} \rightarrow R_{th} = \frac{\Delta T}{q} \quad \left[\frac{\mathrm{K}}{\mathrm{W}}\right]$$

Electrical:

$$\Delta V = IR \rightarrow R = \frac{\Delta V}{I} \quad [\Omega]$$

Thermal and Electrical Conduction

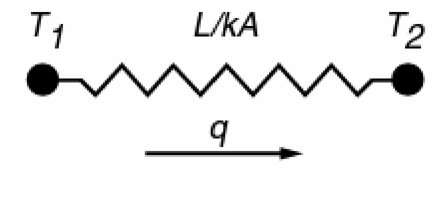
Thermal Conduction	Electrical Conduction
$q = \dfrac{kA_c \Delta T}{L}$ [W]	$I = \dfrac{\sigma A_c \Delta V}{L}$ [A]
k is a material property	σ is a material property
$R_{th} = \dfrac{L}{kA_c}$ [K/W]	$R = \dfrac{L}{\sigma A_c}$ [Ω]
Depends on: Material (k) Length (L) Cross-sectional Area (A_c)	Depends on: Material (σ) Length (L) Cross-sectional Area (A_c)
Series: algebraic sum Parallel: sum of inverses	Series: algebraic sum Parallel: sum of inverses

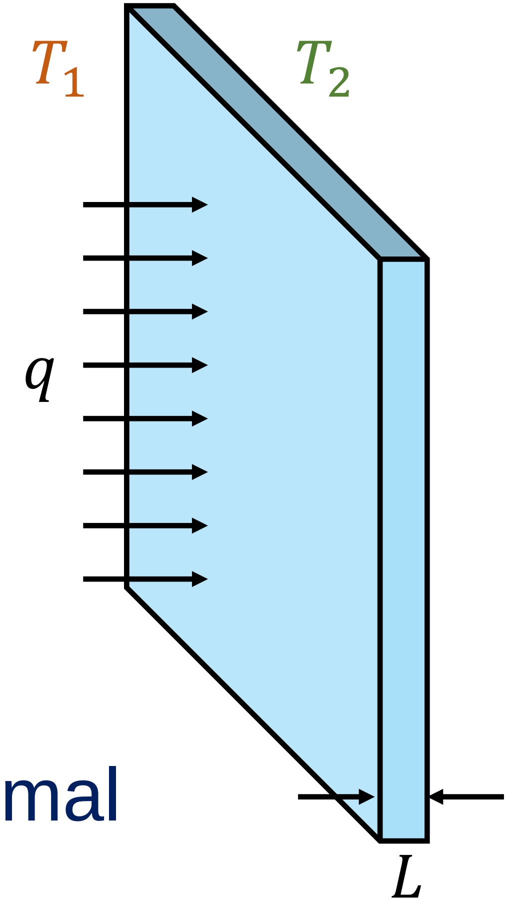
Example: Heat Conduction

Calculate the temperature difference across a 1-mm-thick layer of thermal grease with $k = 1$ W/(m·K). Assume a 1 W heat source spread *uniformly* over a 1 cm² area.

- $q = 1$ W
- $L = t_{TG} = 1$ mm = 0.001 m
- $k_{TG} = 1$ W/(m·K)
- $A_c = 1$ cm² = 1 x 10⁻⁴ m²
- $T_1 - T_2 = \frac{qL}{kA_c} = \frac{(1\ \mathrm{W})(0.001\mathrm{m})}{\left(1\frac{\mathrm{W}}{\mathrm{m\cdot K}}\right)(1\times10^{-4}\mathrm{m}^2)} = \mathbf{10°C}$

$$T_1 - T_2 = \frac{qL}{kA_c}$$



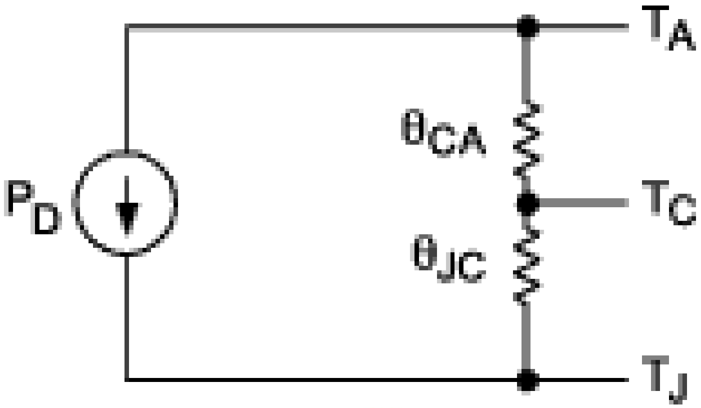


➤ T_2 is 10°C lower than T_1 due to the high R_{th} of the thermal grease

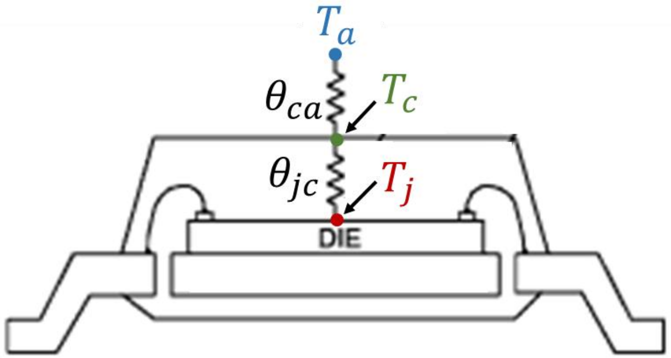
Package Thermal Resistance

- θ_{ja} can be separated into two parts:
  - Junction-to-case, θ_{jc}
  - Case-to-ambient, θ_{ca}

$$\boxed{\theta_{ja} = \theta_{jc} + \theta_{ca}}$$

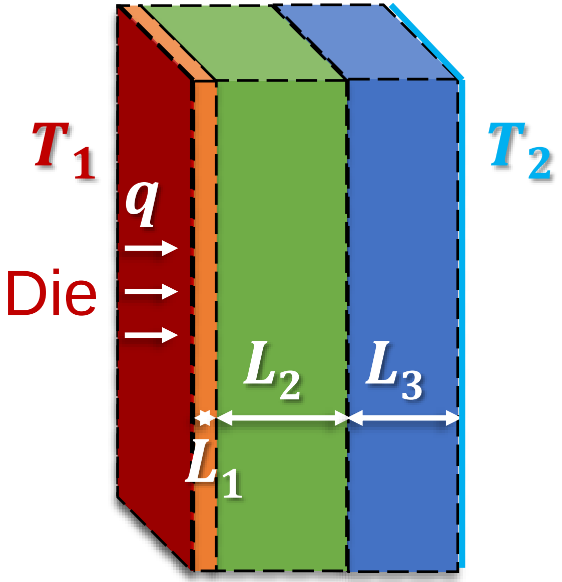


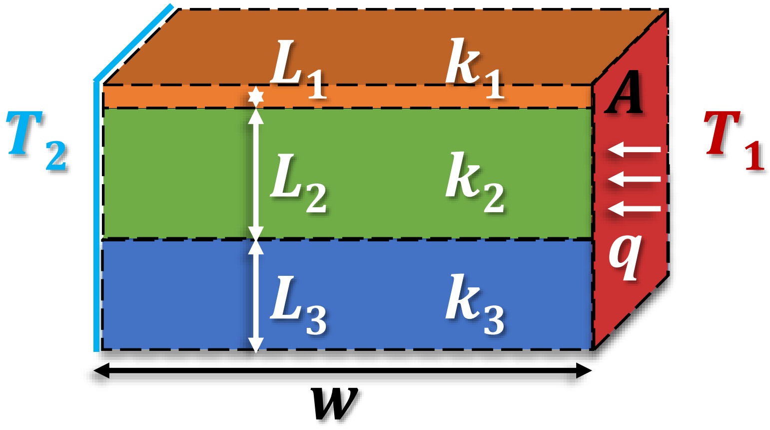
- Junction-to-case, θ_{jc}
  - Depends on the internal construction of the package
  - Depends on length, cross-sectional area, and k

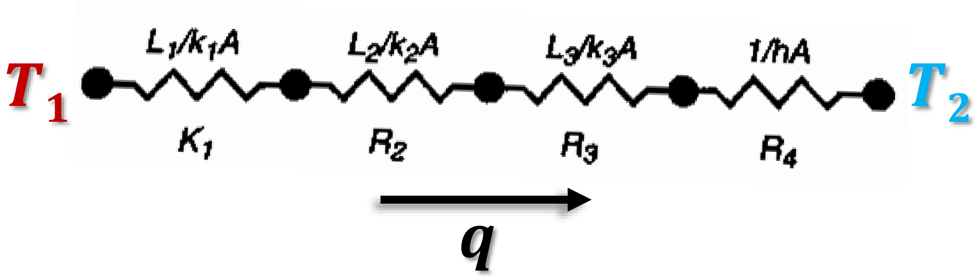


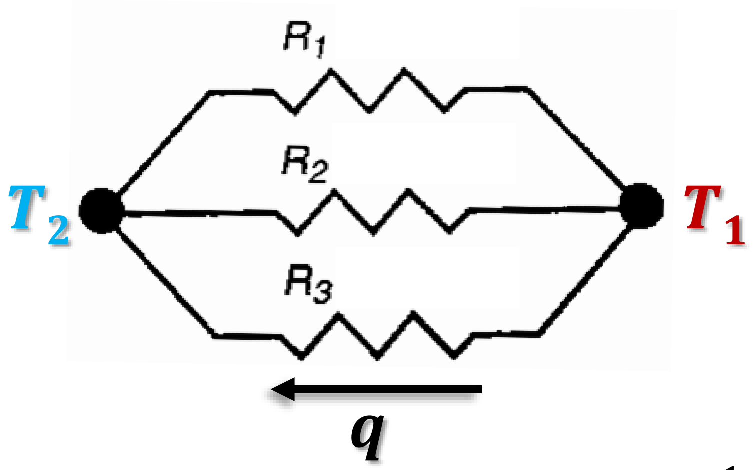
- Case-to-ambient, θ_{ca}
  - Depends on the mounting and cooling techniques
  - Depends on wetted surface area and h

Thermal Resistances in Series and Parallel







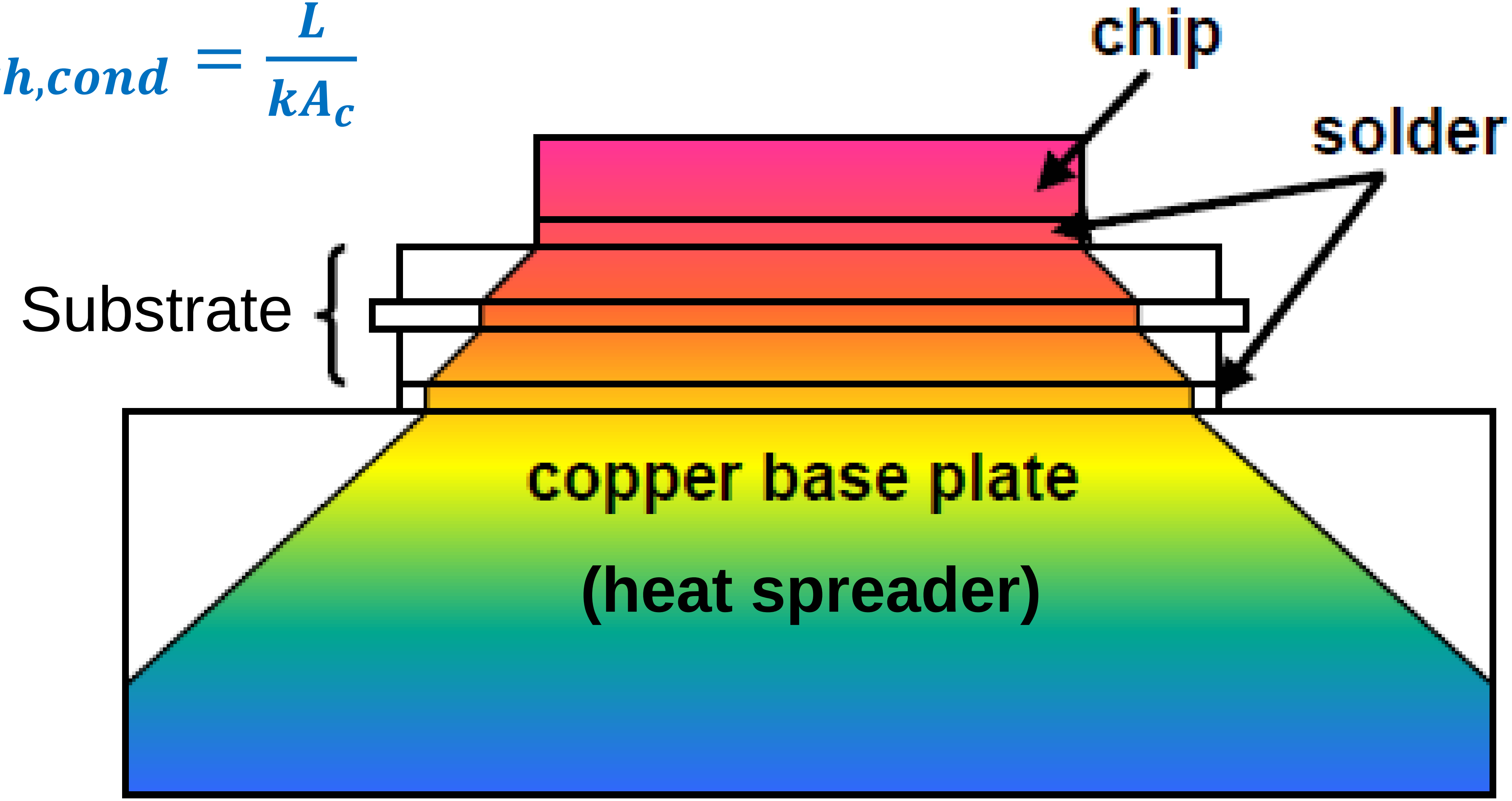


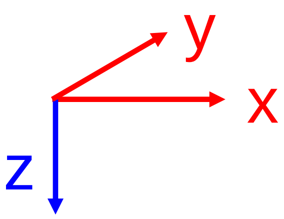
$$R_{th,1-2} = R_1 + R_2 + R_3 + R_4$$

$$R_{th,1-2} = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)^{-1}$$

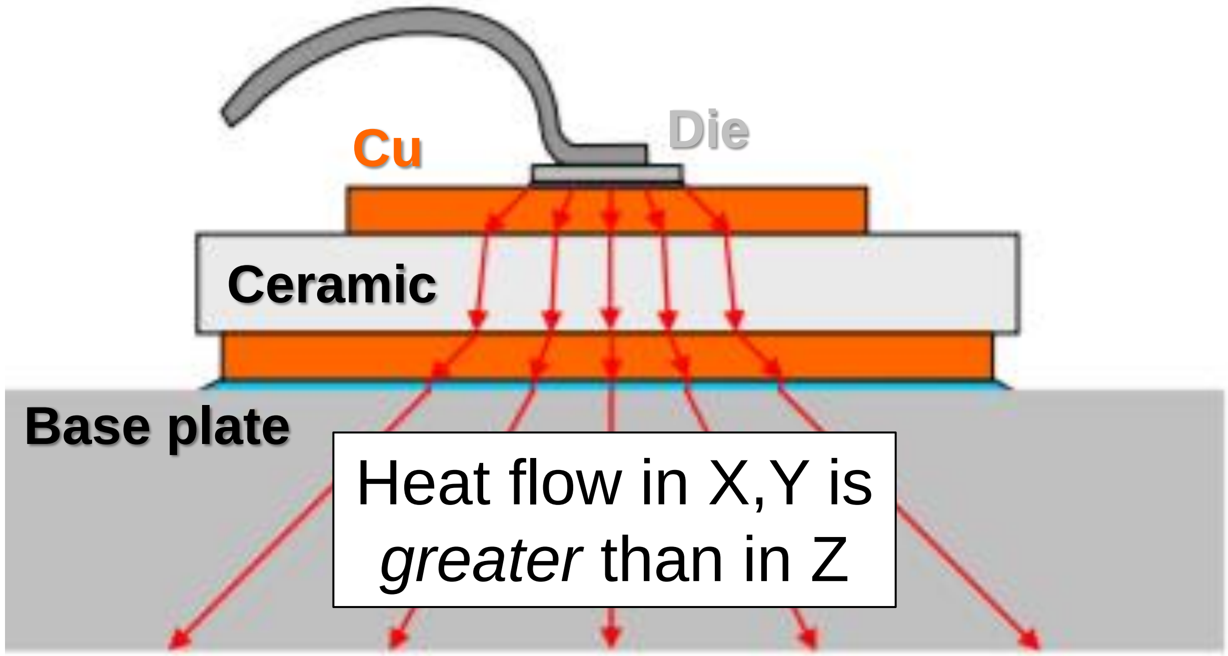
Lateral Heat Spreading

$$R_{th,cond} = \frac{L}{kA_c}$$

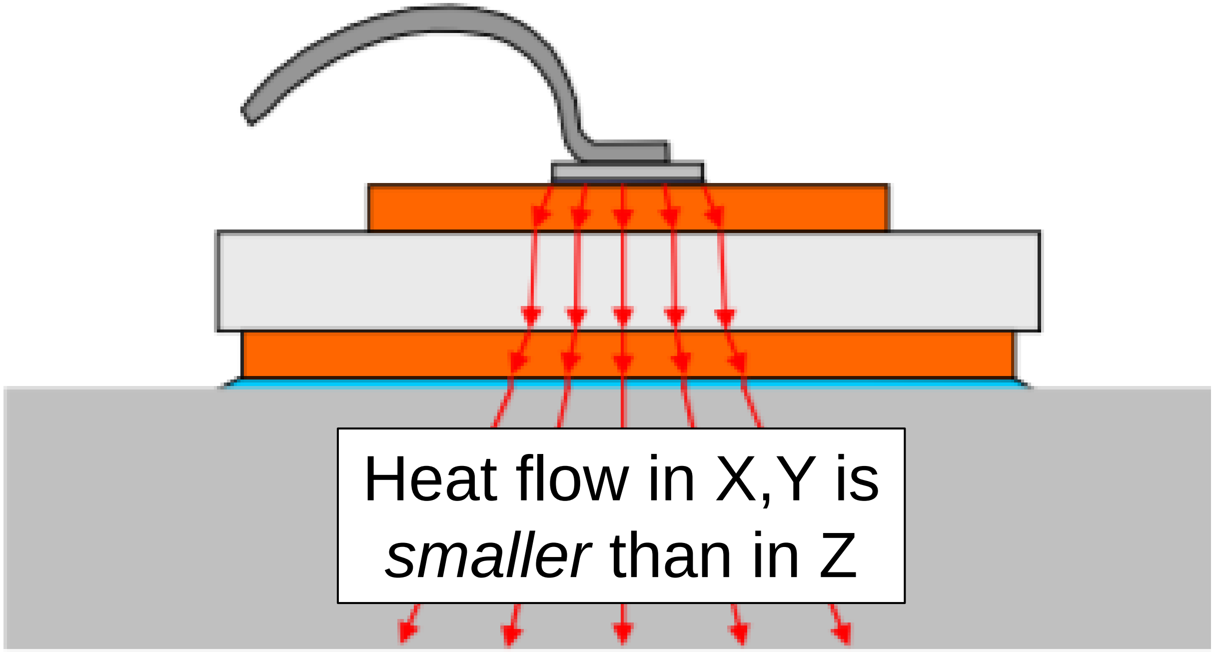




Heat Spreading

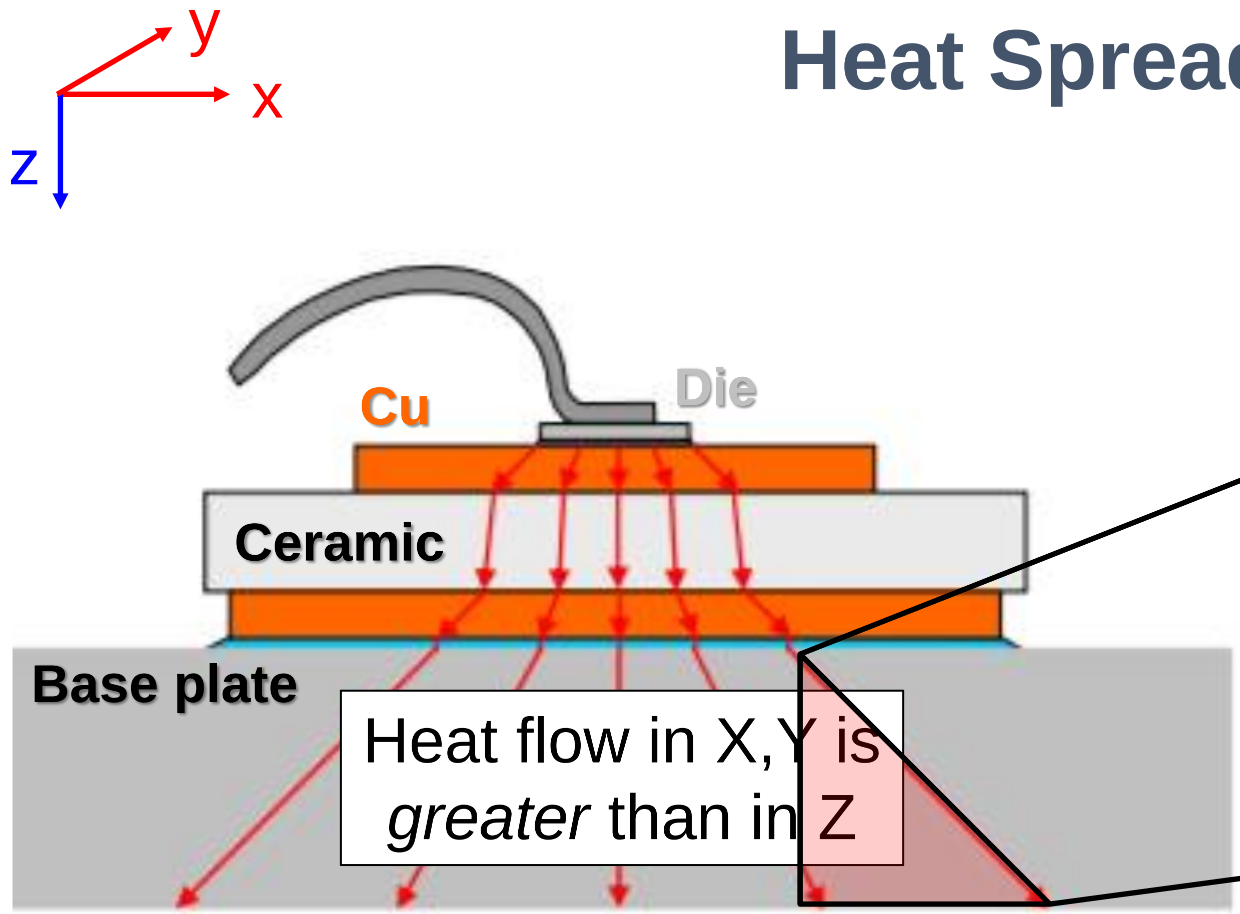


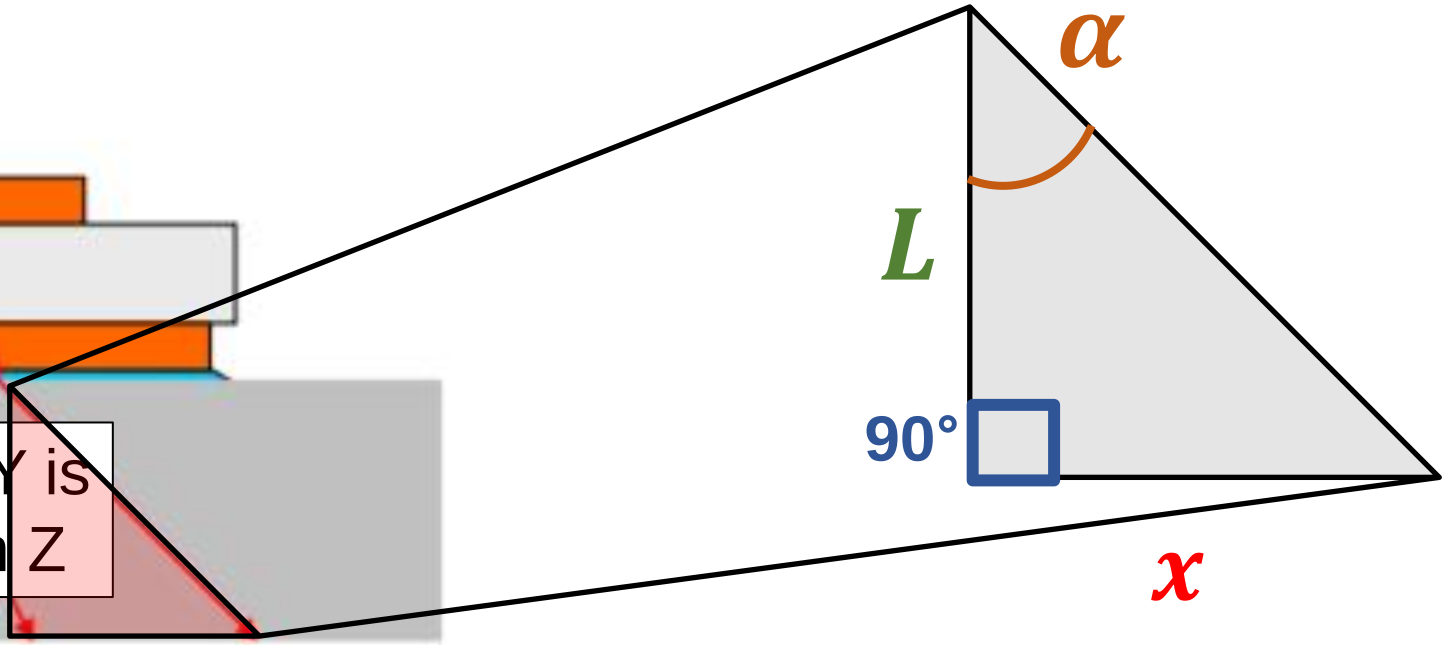
- Heatsink thermal resistance is *high*
- *Low* h (e.g., natural convection)
- Heatsink has *low* k



- Heatsink thermal resistance is *low*
- *High* h (e.g., forced liquid cooling)
- Heatsink has *high* k

Heat Spreading Angle α



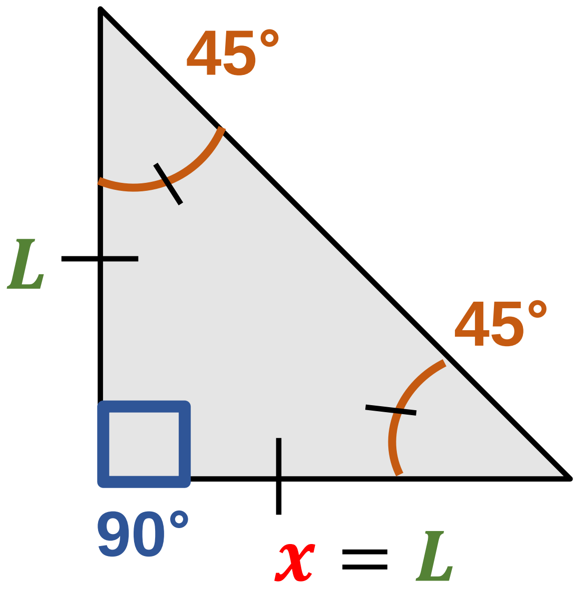


- Heatsink thermal resistance is *high*
- *Low* h (e.g., natural convection)
- Heatsink has *low* k

$$R_{th,cond} = \frac{L}{kA_c}$$

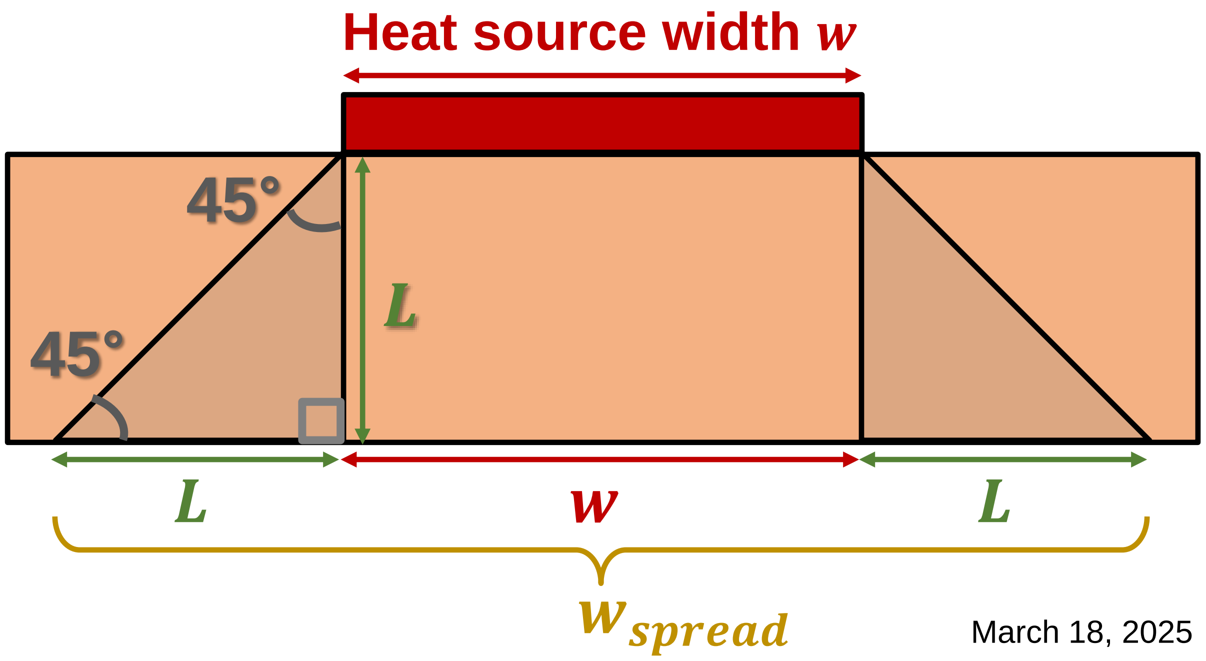
Heat Spreading Approximation

- A **45°** spreading angle is a common approximation/ simplification for heat spreading in materials with high thermal conductivity



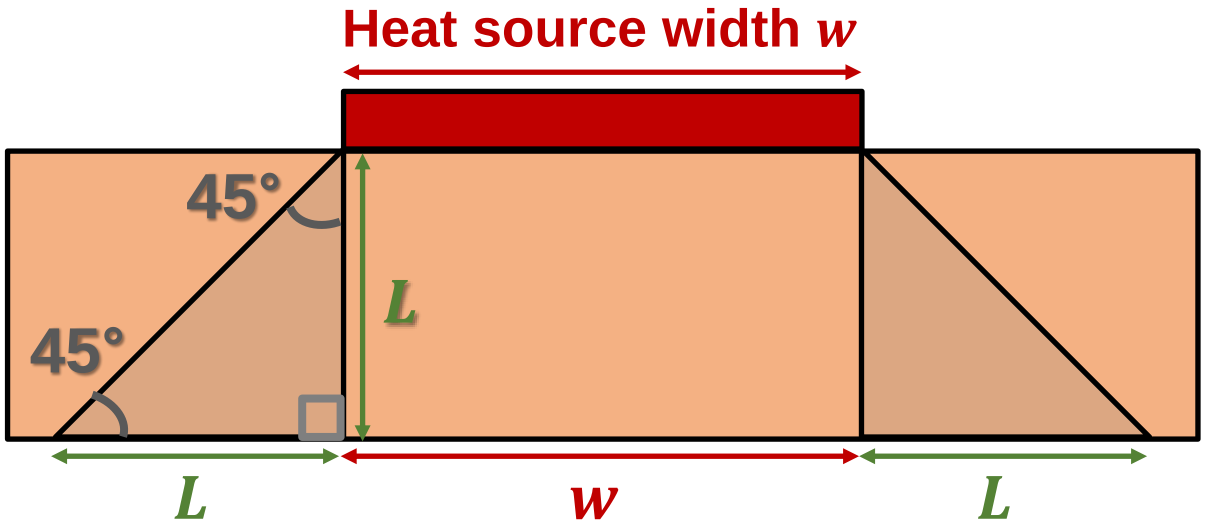
- For a 45° spreading angle, the width at the base of the heat spreading is

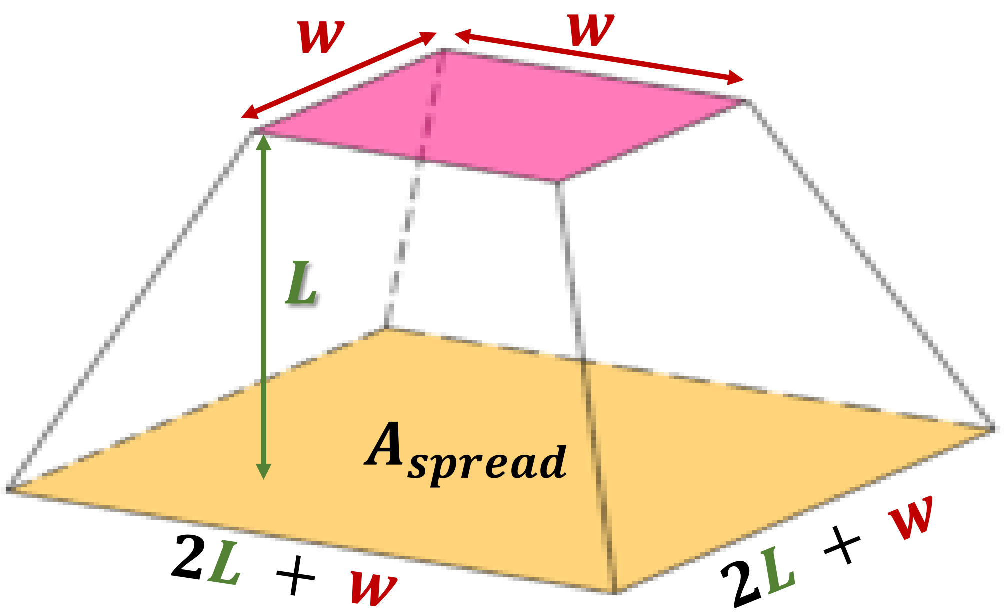
$$w_{spread} = 2L + w$$



Heat Spreading Approximation

- If the heat source is square, then the base area of the heat spreading is



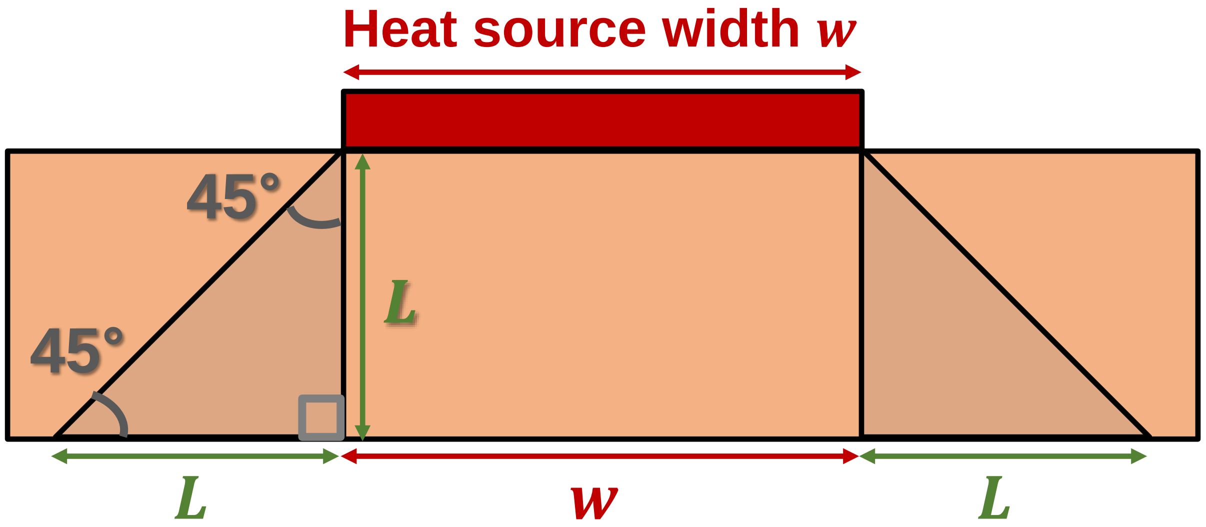


$$A_{spread} = w_{spread} \times w_{spread}$$

$$= (2L + w)(2L + w)$$

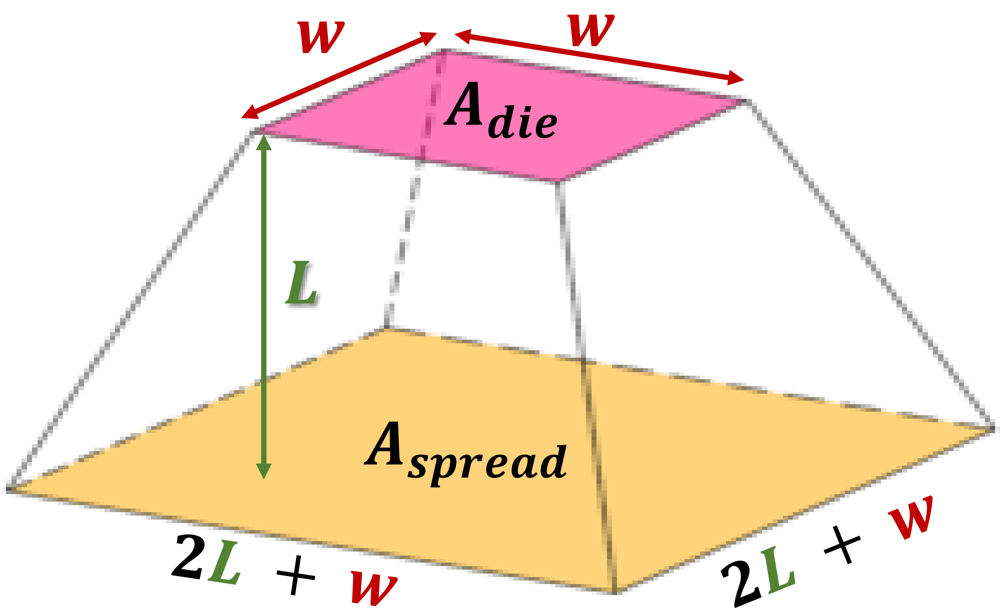
Heat Spreading Approximation

- The effective area A_{eff} for the heat flow through this layer can be approximated by averaging the heat source area A_{die} and the base area A_{spread}:



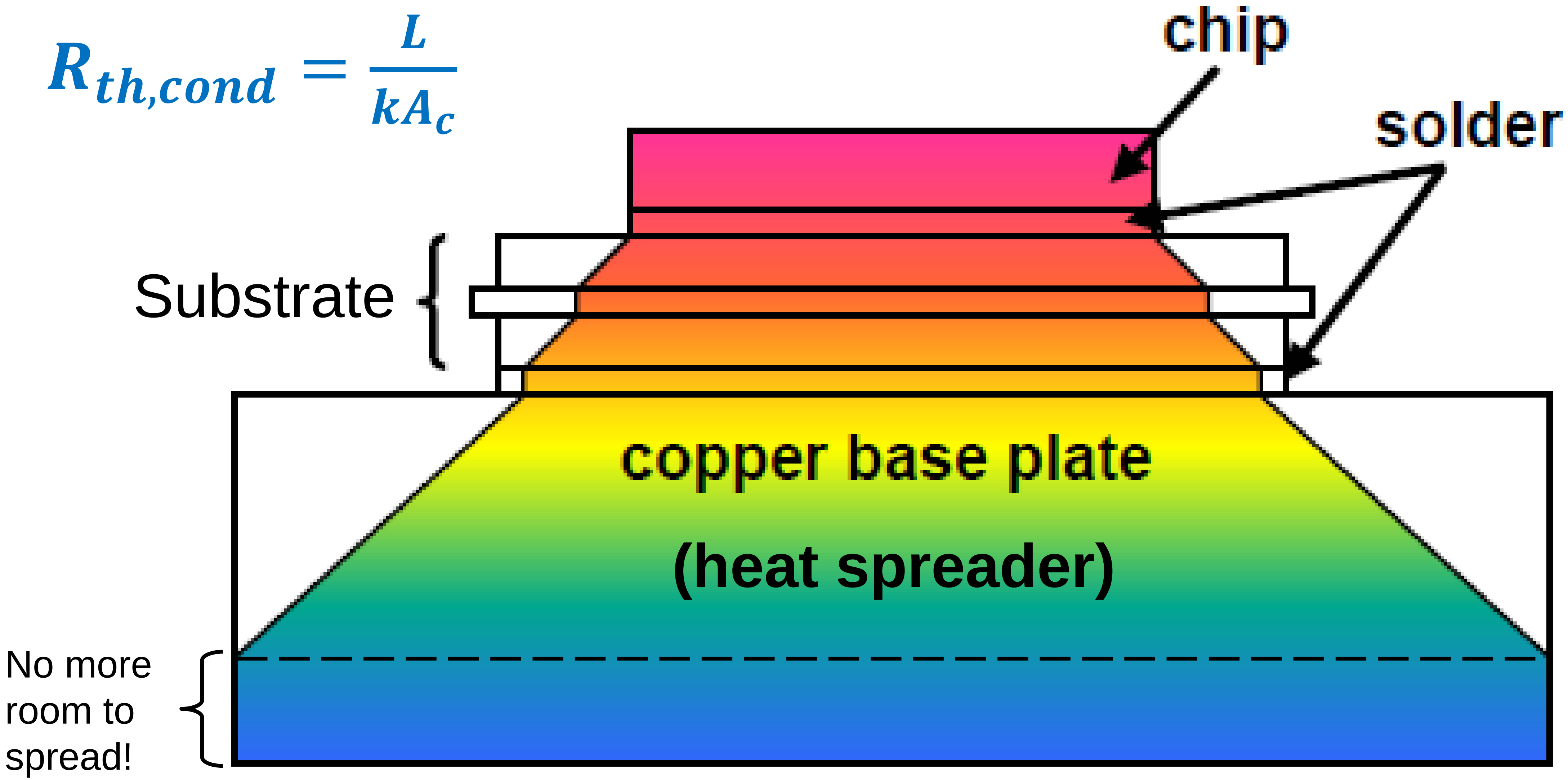
$$\boldsymbol{A_{eff}} = (\boldsymbol{A_{spread}} + \boldsymbol{A_{die}})\ /\ \mathbf{2}$$

$$= [(\mathbf{2}\boldsymbol{L} + \boldsymbol{w})(\mathbf{2}\boldsymbol{L} + \boldsymbol{w}) + (\boldsymbol{w} \times \boldsymbol{w})]\ /\ \mathbf{2}$$



Lateral Heat Spreading

$$R_{th,cond} = \frac{L}{kA_c}$$

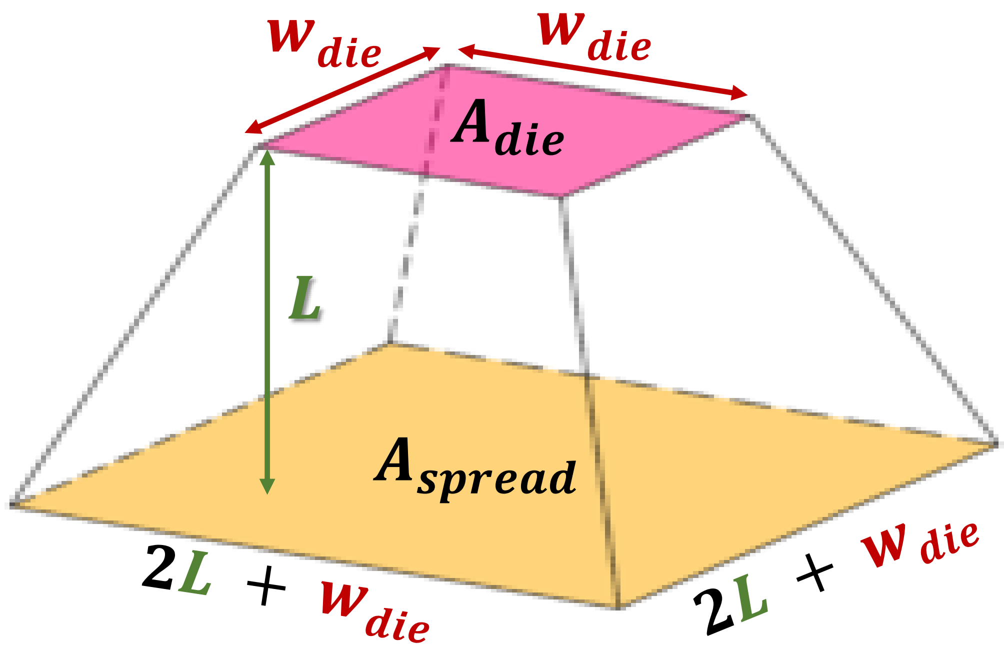


➢ Choose base plate width & thickness such that the base plate width ≈ heat spreading width at the base

Example: Heat Spreading

Find the thermal resistance of a copper base plate with dimensions of 15 x 15 x 4 mm^3. The dimensions of the heat-generating component (die) on top of the base plate are 5 x 5 x 1 mm^3. Assume a heat spreading angle of 45°.

- w_{die} = 5 mm
- A_{die} = 5 mm x 5 mm = 25 mm^2
- L_{BP} = 4 mm
- w_{BP} = 15 mm



Check that $w_{spread} \leq w_{BP}$:

- $w_{spread} = (2L + w_{die})$ = 2(4mm) + 5mm = **11 mm** < 15 mm

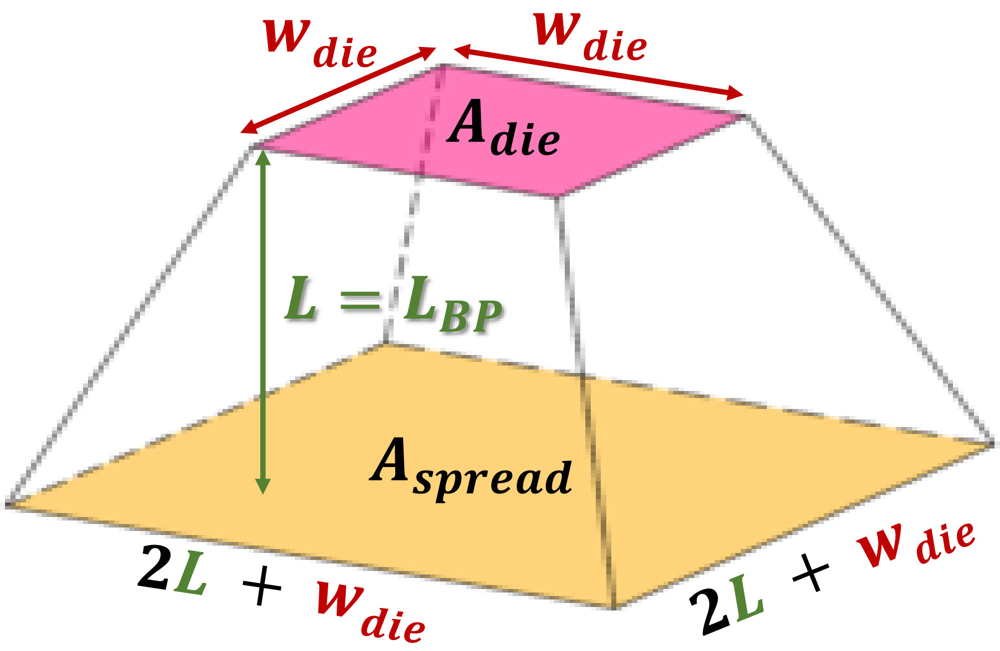
Example: Heat Spreading

Find the thermal resistance of a copper base plate with dimensions of 15 x 15 x 4 mm^3. The dimensions of the heat-generating component (die) on top of the base plate are 5 x 5 x 1 mm^3. Assume a heat spreading angle of 45°.

- $w_{die} = 5$ mm
- $A_{die} = 5$ mm x 5 mm = 25 mm^2
- $L = L_{BP} = 4$ mm
- $A_{spread} = (2L_{BP} + w_{die})(2L_{BP} + w_{die})$

$= (2(4\text{mm}) + 5\text{mm})(2(4\text{mm}) + 5\text{mm})$

$=$ **169 mm^2**



Example: Heat Spreading

Find the thermal resistance of a copper base plate with dimensions of 15 x 15 x 4 mm³. The dimensions of the heat-generating component (die) on top of the base plate are 5 x 5 x 1 mm³. Assume a heat spreading angle of 45°.

- $A_{eff} = (A_{spread} + A_{die})$ / 2

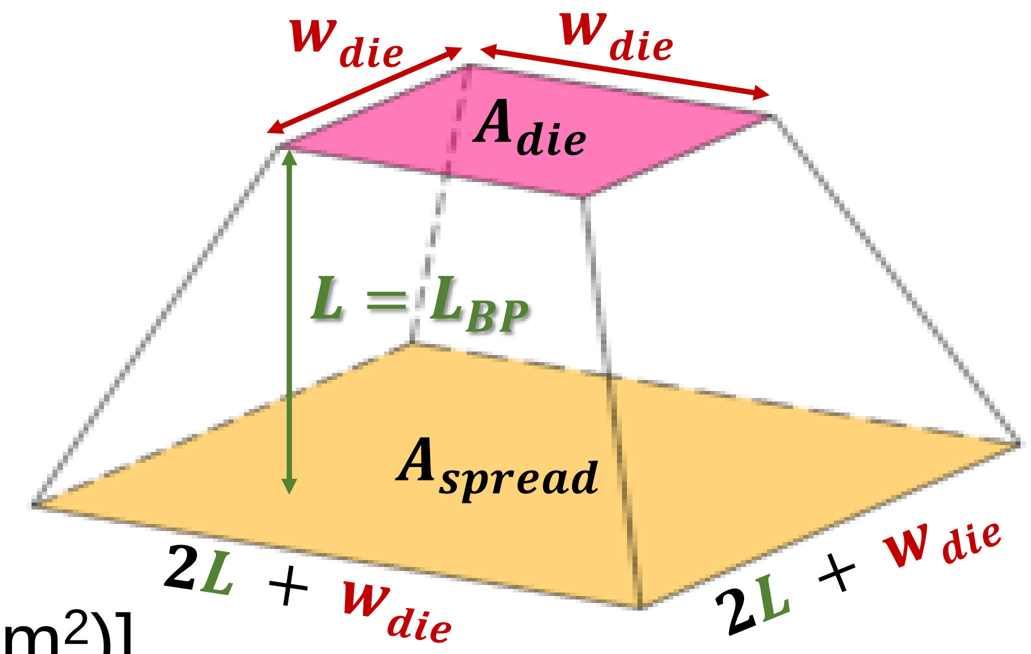
  = (169 mm² + 25 mm²) / 2

  = 97 mm² = 0.000097 m²

- $R_{th,BP} = L_{BP}$ / $(k_{BP}\, A_{eff})$

  = 0.004 m / [(390 W/(mK))(9.7e-5 m²)]

  = **0.106 K/W**



Example: Smaller Base Plate Area

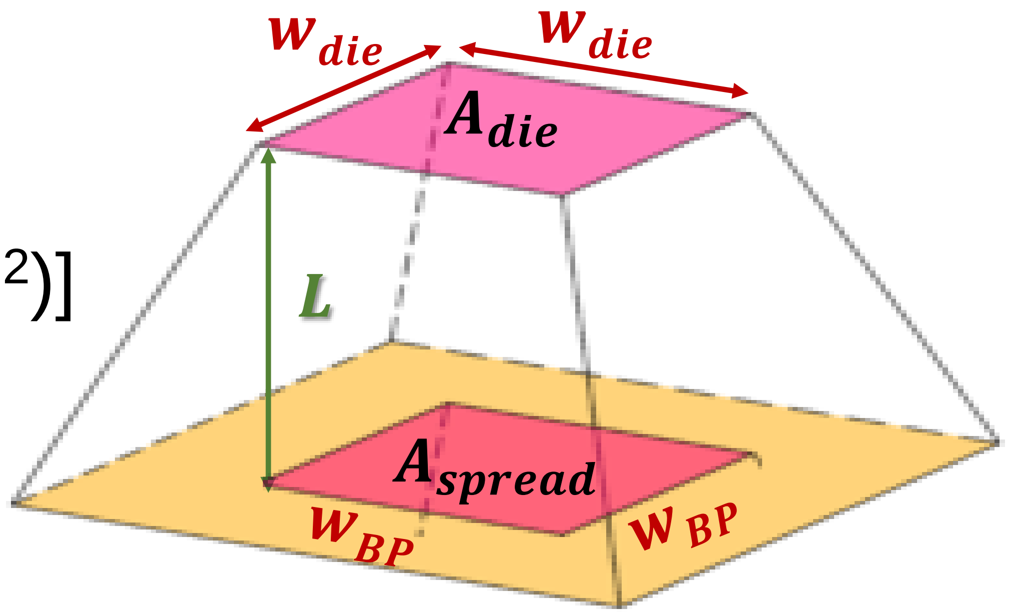
- Silicon die: 5 x 5 x 1 mm
- Copper baseplate: *5* x *5* x 4 mm
- Find the thermal resistance of the base plate.

- $A_{spread} = A_{BP} = A_{die}$

- $R_{th,BP} = L_{BP} \,/\, (k_{BP}\, A_{BP})$

  $= 0.004\text{ m} / [(390\text{ W/(mK)})(2.5e\text{-}5\text{ m}^2)]$

  $=$ **0.410 K/W**



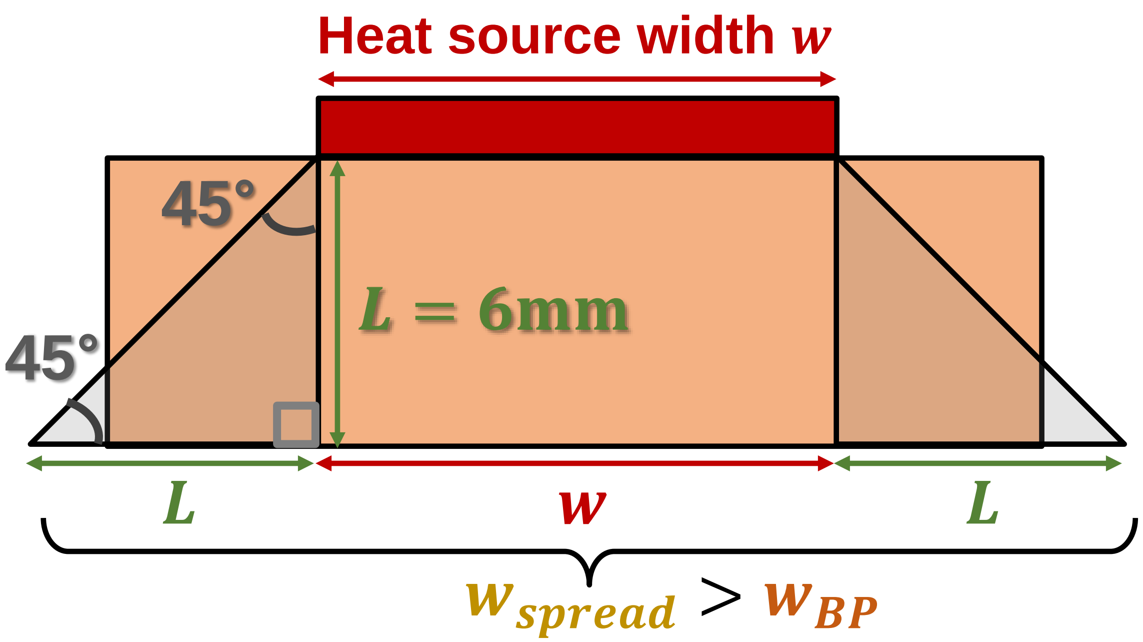
➢ $R_{th,BP}$ increases by **4x** because there is no room for heat spreading (A_{BP} is smaller)

Example: Thicker Base Plate Area

- Silicon die: 5 x 5 x 1 mm
- Copper baseplate: 15 x 15 x *6* mm

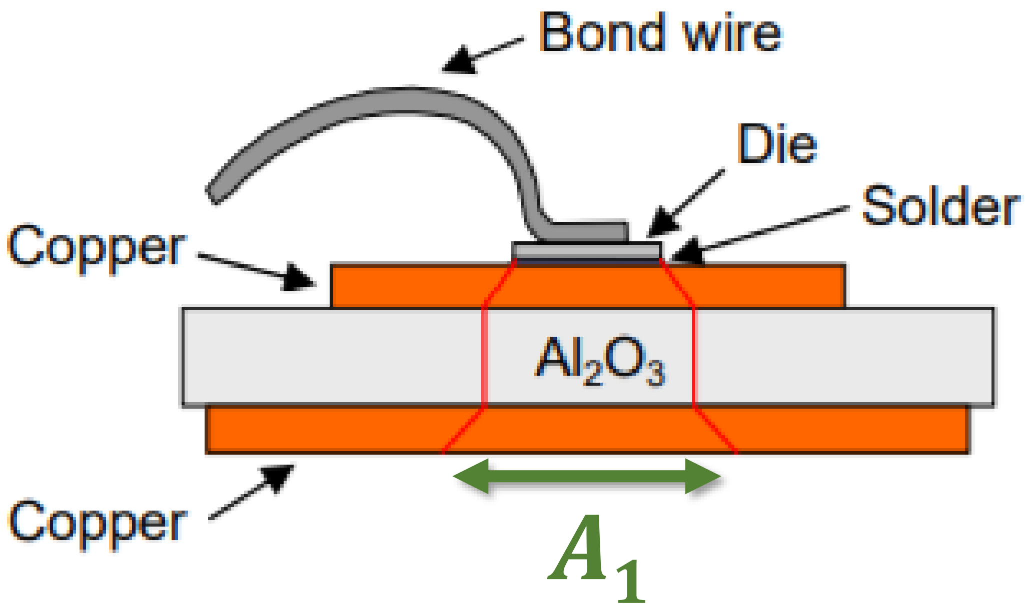
Check that $w_{spread} \leq w_{BP}$:

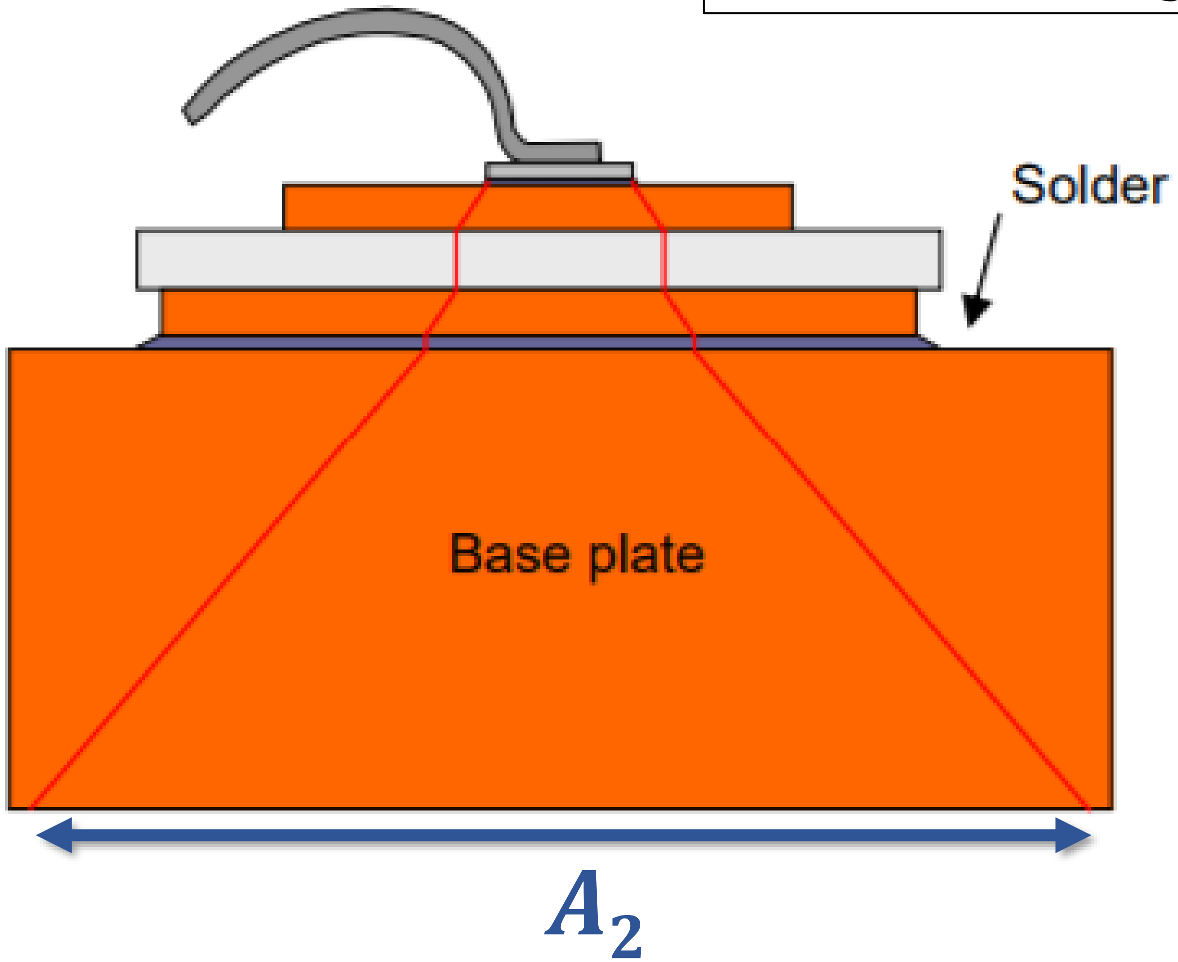
- $w_{spread} = (2L + w_{die})$ = 2(6mm) + 5mm = **17 mm** > 15 mm !
- The bottom of the base plate is not helping with the heat spreading



Base Plate/Heat Spreader

$$R_{th,conv} = \frac{1}{hA_s}$$





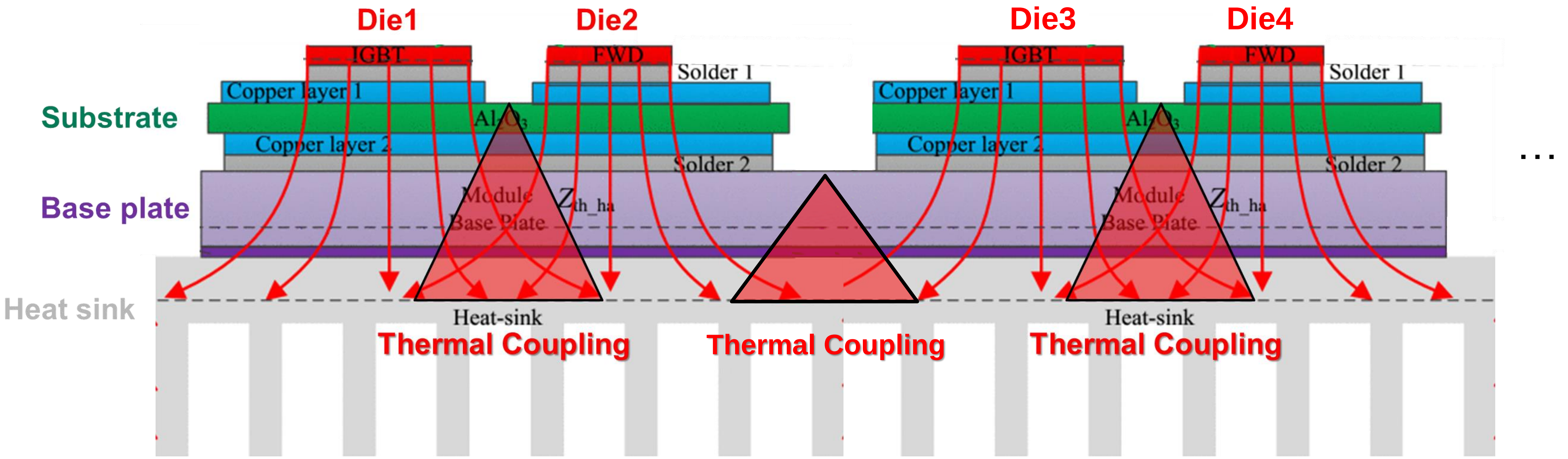
For the same h,

$$R_{th,convA_1} > R_{th,convA_2}$$

*note: if h is high, then Z heat flow > X,Y heat flow, so heat spreading is low and the baseplate becomes less effective.

https://www.power-mag.com/pdf/feature_pdf/1319729749_Vincotech_Layout_1.pdf

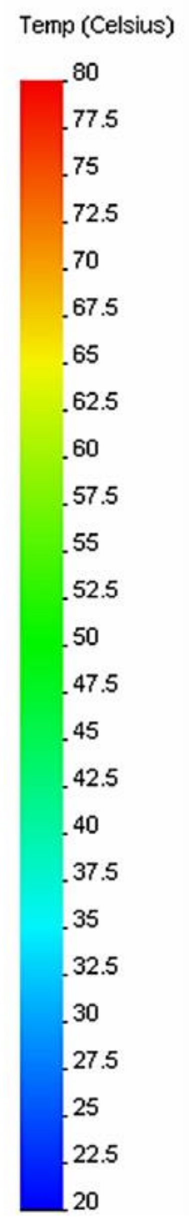
Heat Spreading in MCM = Thermal Coupling: Common Base Plate

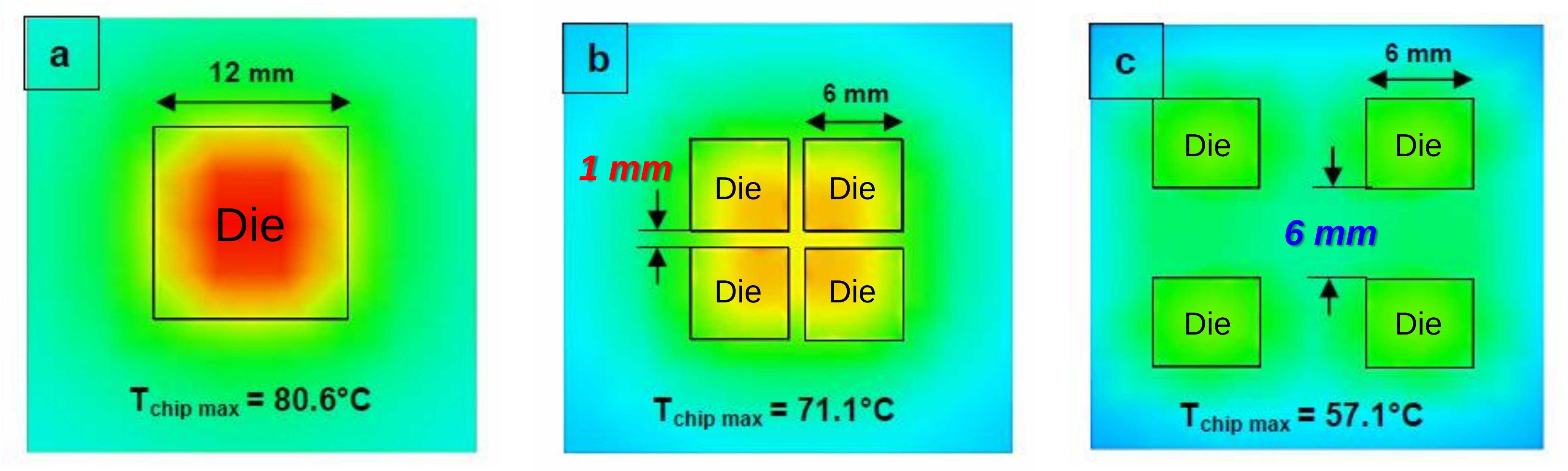


https://ieeexplore.ieee.org/abstract/document/7581086

MCM = Multi-Chip Module

Impact of Thermal Coupling





- **Large dies** may have **greater ΔT** across the area, and therefore **worse thermal spreading** than smaller dies
- **Several smaller dies** with the same overall area have a **lower R_{th}**
- If the **spacing between chips is small**, the **chips heat up one another** (thermal coupling)
- **Greater spacing** between chips further **lowers R_{th}**

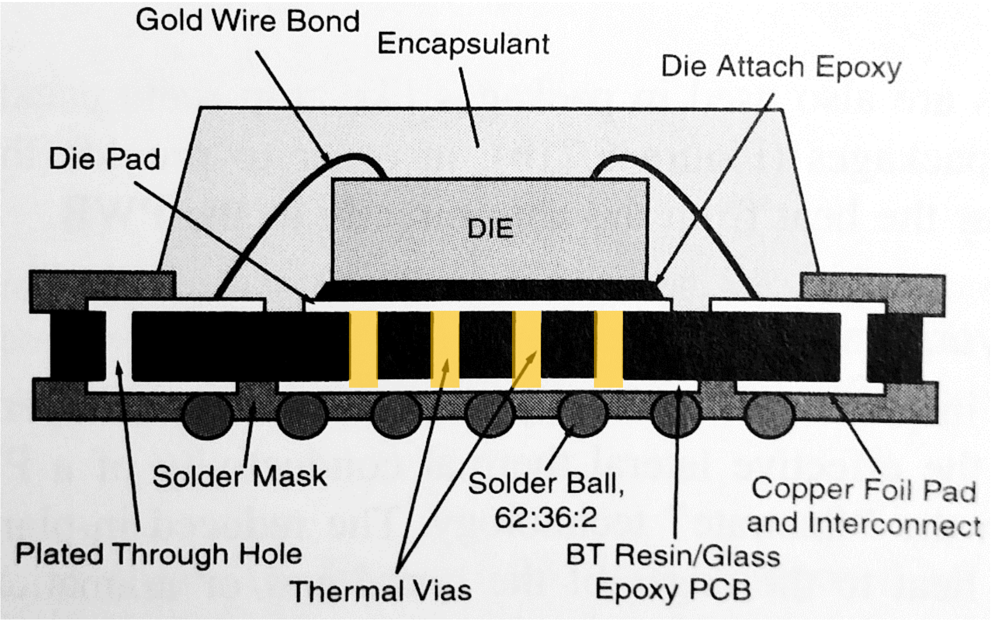
Thermal Vias

- Vias can reduce the vertical R_{th}
- The equivalent vertical (Z-direction) thermal conductivity is:

$$k_{zz} = k_m a_m + k_i(1 - a_m)$$

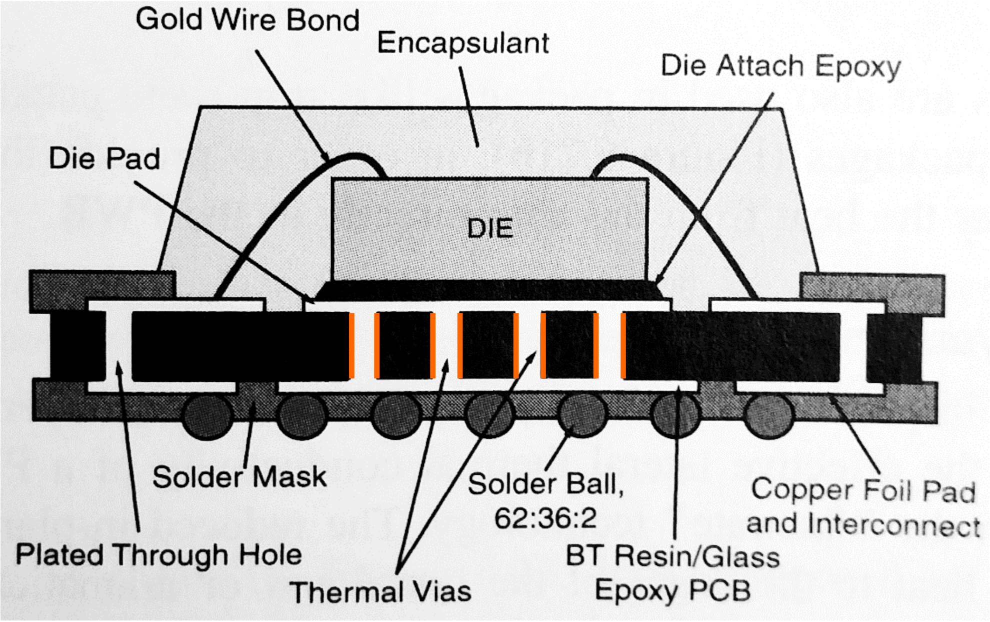
where

- $k_m = k$ of metal
- $a_m =$ fraction of the *cross-sectional area* occupied by the metal vias
- $k_i = k$ of the insulator



Example: Thermal Vias

PCB has a through-hole via density of 25 per cm^2 of board area. The via hole diameter is 0.43 mm, and its inner surface is plated with 15-µm-thick copper. Calculate the equivalent thermal conductivity value k_{zz} for this PCB. Use $k_{Cu} = 390$ W/mK and $k_i = 0.2$ W/mK.



Example: Thermal Vias

- Equivalent thermal conductivity in Z direction:

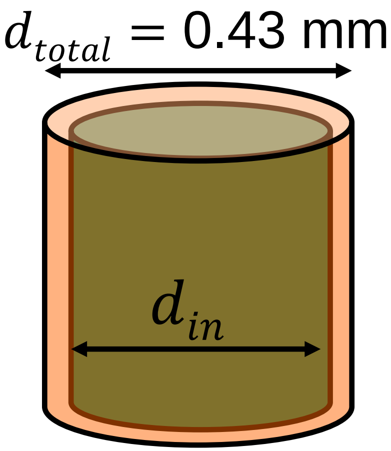
$$k_{zz} = k_m a_m + k_i(1 - a_m)$$

- Need a_m (fraction of the cross-sectional area occupied by the via metal)
- To find a_m, need the effective conducting area for each via
  - Via hole diameter = 0.43 mm
  - Via copper plating = 0.015 mm
  - Effective via conducting area = Total via area – non-conductive via area

$$A_{cond} = \pi\left(\frac{0.43\text{mm}}{2}\right)^2 - \pi(0.43\text{mm}/2 - 0.015\text{mm})^2 = 0.01956\text{mm}^2$$

  - $a_m = 25\,\frac{\text{vias}}{\text{cm}^2} \times 0.0001956\text{cm}^2 = 0.004889$

- $k_{zz} = 390\,\frac{\text{W}}{\text{m}\cdot\text{K}}(0.004889) + 0.2\,\frac{\text{W}}{\text{m}\cdot\text{K}}(1 - 0.004889) = \mathbf{2.11}\,\frac{\mathbf{W}}{\mathbf{m\cdot K}}$



d_{in} = 0.43 mm – 2(0.015 mm)

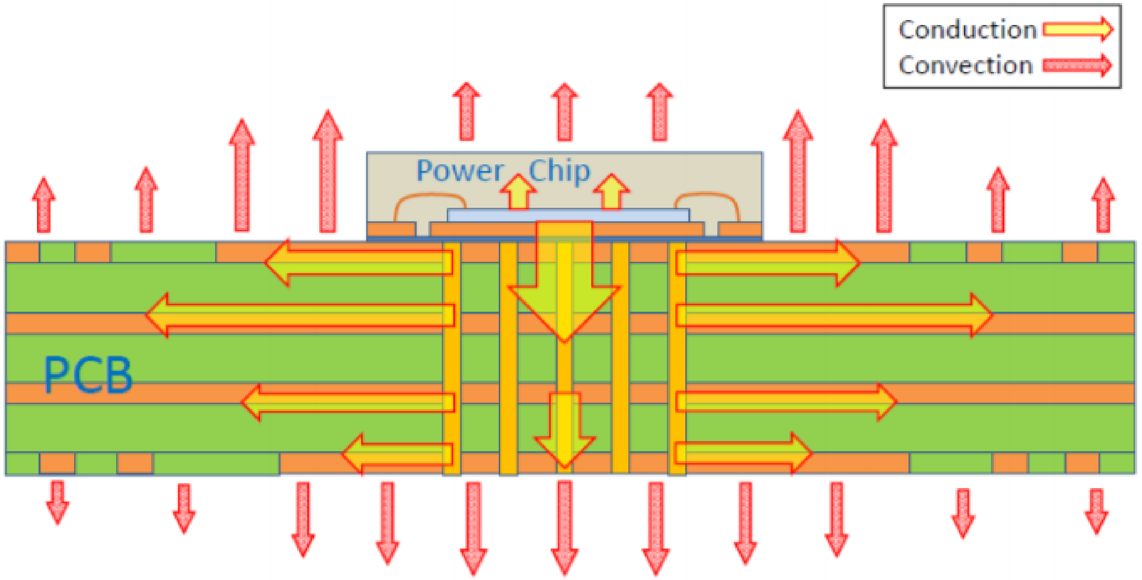
Metal Planes

- Metal planes can reduce the lateral R_{th} by increasing the effective thermal conductivity in the XY plane:

$$k_{xy} = k_m t_m + k_i(1 - t_m)$$

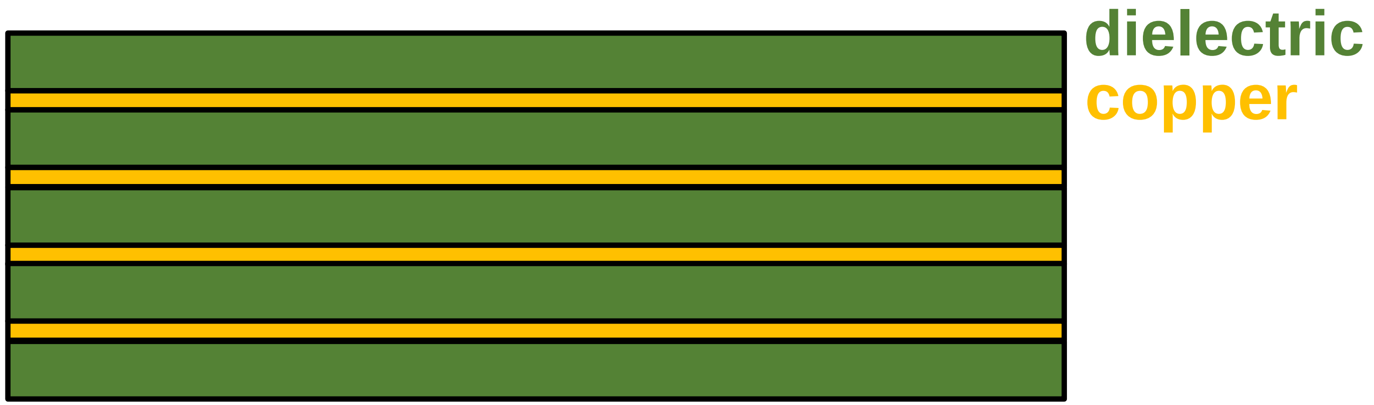
where

- $k_m = k$ of metal
- $t_m =$ fraction of the *thickness* occupied by the metal planes
- $k_i = k$ of the insulator



Example: Metal Planes

A PCB has two power layers and two ground layers, each with a 50-µm-thick copper plane. The power and ground layers are separated by 200-µm-thick dielectric (insulator) layers. Calculate the equivalent thermal conductivity value k_{xy} for this PCB. Use $k_{Cu} = 390$ W/mK and $k_i = 0.2$ W/mK.



Example: Metal Planes

- Equivalent thermal conductivity in XY direction:

$$k_{xy} = k_m t_m + k_i(1 - t_m)$$

- Need t_m (fraction of the thickness area occupied by the metal planes)
  - Total metal thickness = 50 µm/layer x 4 layers = 200 µm
  - Total insulator thickness = 200 µm/layer x 5 layers = 1000 µm
  - $t_m = \frac{200\mu\text{m}}{1200\mu\text{m}} = 0.167$
- $k_{xy} = 390\,\frac{\text{W}}{\text{m}\cdot\text{K}}(0.167) + 0.2\,\frac{\text{W}}{\text{m}\cdot\text{K}}(1 - 0.167) = \mathbf{65.17}\,\frac{\mathbf{W}}{\mathbf{m}\cdot\mathbf{K}}$

- Note: if there are unfilled vias cutting through the plane, the XY thermal conductivity will be reduced

Example: Metal Planes

- If $L = w$ for the PCB, the equivalent thermal resistance in XY direction:

$$R_{th,xy} = \frac{L}{k_{xy}A} = \frac{1}{\left(65.17\,\frac{\mathrm{W}}{\mathrm{m}\cdot\mathrm{K}}\right)(0.0012\mathrm{m})} = \mathbf{12.8\ K/W}$$

- Alternatively, could find the thermal resistance of the copper layer in XY and the insulator layer in XY and then use the parallel rule:

- $R_{th,xy,Cu} = \frac{L}{k_{Cu}A} = \frac{1}{\left(390\frac{\mathrm{W}}{\mathrm{m}\cdot\mathrm{K}}\right)(0.00005\mathrm{m})} = 51.2\,\frac{\mathrm{K}}{\mathrm{W}}$ per layer → $\div\, 4 = \mathbf{12.8}\,\frac{\mathbf{K}}{\mathbf{W}}$

- $R_{th,xy,i} = \frac{L}{k_{xy}A} = \frac{1}{\left(0.2\frac{\mathrm{W}}{\mathrm{m}\cdot\mathrm{K}}\right)(0.0002\mathrm{m})} = 25000\,\frac{\mathrm{K}}{\mathrm{W}}$ per layer → $\div\, 5 = \mathbf{5000}\,\frac{\mathbf{K}}{\mathbf{W}}$

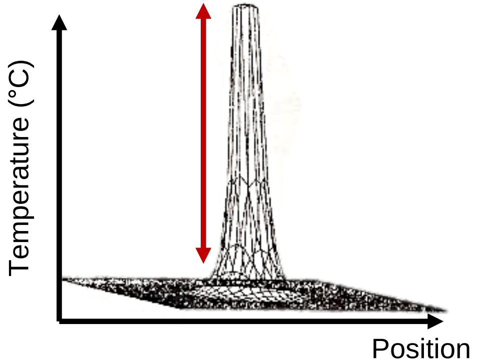
- $R_{th,xy,Cu} \parallel R_{th,xy,i} = \left(\frac{1}{12.8\mathrm{K/W}} + \frac{1}{5000\mathrm{K/W}}\right)^{-1} = \mathbf{12.8\ K/W}$

Metal Planes

- Metal planes spread heat laterally, which reduces local temperature rises
- FEA simulation of 7.5 mm^2 chip dissipating 1 W on different PCBs
  - Adding a plane of **1 oz** copper reduces the maximum ΔT by **86 %**
  - **1 oz** → **2 oz** reduces ΔT_{max} by **35 %**
  - **2 oz** → **4 oz** reduces ΔT_{max} by **35 %**

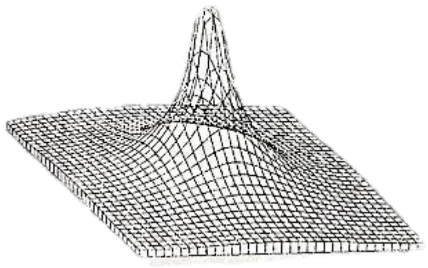
No Metal:

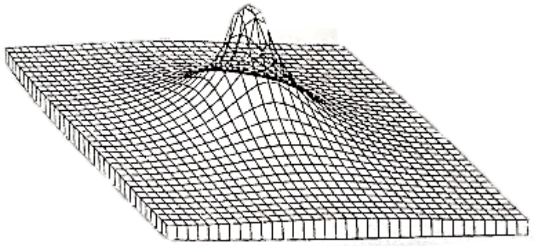
$\Delta T_{max} = 160\ °C$



1 oz Copper:

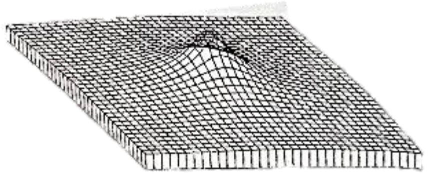
$\Delta T_{max} = 22\ °C$





2 oz Copper:

$\Delta T_{max} = 14\ °C$



4 oz Copper:

$\Delta T_{max} = 9\ °C$

Convection

- Transfer of heat between the surface of a body and a fluid in motion
- Newton's Law of Cooling:

$$\boldsymbol{q = hA_s(T_s - T_f)}$$

- q = heat (W)
- h = convective heat transfer coefficient (W/(m^{2}K))
- A_s = wetted surface area (m^2)
- T_s = surface temperature (°C)
- T_f = bulk temperature of fluid (°C)
- Rearranging the above equation:

$$\boldsymbol{\frac{1}{hA_s} = \frac{(T_s - T_f)}{q} \rightarrow R_{th,conv} = \frac{1}{hA_s}}$$

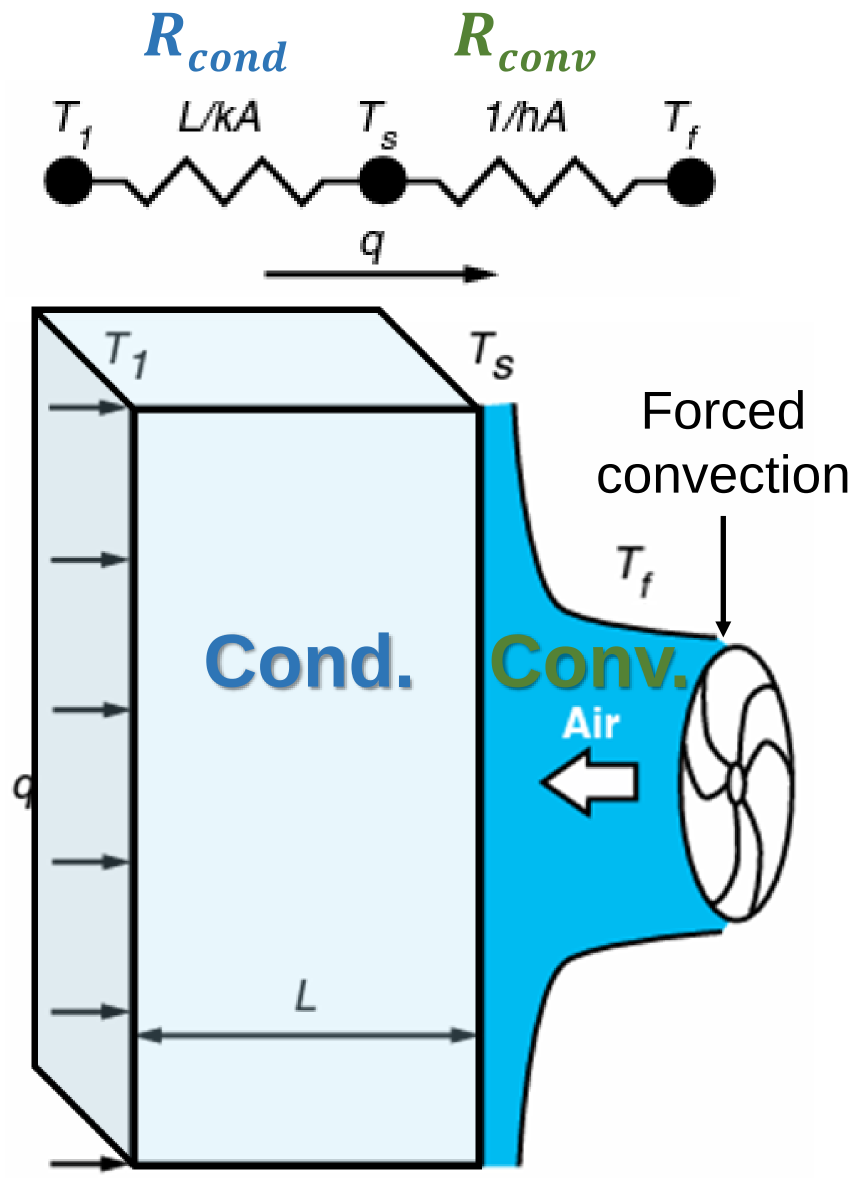
Conduction & Convection Thermal Resistances

$$q = \frac{kA_c(T_h - T_c)}{L} \qquad R_{th,cond} = \frac{L}{kA_c}$$

q = heat (W)
k = thermal conductivity (W/(m·K))
A_c = cross-sectional area (m^2)
L = length q needs to travel (m)
T_h = hot temperature (°C)
T_c = cold temperature (°C)

$$q = hA_s(T_s - T_f) \qquad R_{th,conv} = \frac{1}{hA_s}$$

h = heat transfer coefficient (W/(m^2K))
A_s = wetted surface area (m^2)
T_s = surface temperature (°C)
T_f = bulk temperature of fluid (°C)



Convection Heat Transfer Coefficient h

$$q = hA_s(T_s - T_f)$$

- h depends on the properties of the fluid, the velocity of the fluid, and the surface geometry
- h can be determined empirically or analytically

Cooling Method	h (W/(m^{2}K))
Free (natural) convection	5 – 25
Forced convection, air	25 – 250
Forced convection, water	100 – 10,000
Boiling water	1,000 – 50,000
Condensing steam	5,000 – 100,000

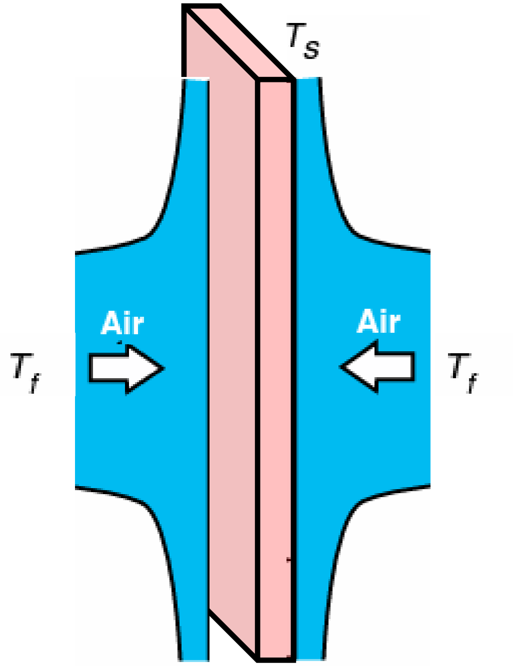
Types of Convection

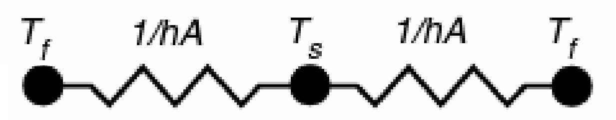
- **Free** (or natural)
  - Occurs due to buoyancy effects: hotter fluid adjacent to a hot surface rises, leading to the transfer of heat from the hot surface
- **Forced**
  - Occurs when heat is transported from a hot surface by a fluid stream moved by an external stimulant (e.g., fan, pump)
- **Mixed** (combination of free and forced)
  - Occurs when the forced fluid velocity is low such that heat transfer due to free and forced convection are of similar magnitudes

Example: Convection

Calculate the average temperature of a 20 cm x 20 cm PWB dissipating 10 W cooled by natural convection in air at 35 °C from both sides.

- $q = 10$ W
- $h = 5$ W/m²K
- $A_s = 20$ cm x 20 cm= 0.04 m² (per side)
- $R_{th,conv,total} = \left(\frac{1}{hA_s}\right) || \left(\frac{1}{hA_s}\right) = \frac{1}{2hA_s}$
- $T_f = 35$ °C
- $T_s = \left(\frac{q}{2hA_s}\right) + T_f = \frac{(10\ \mathrm{W})}{2\left(5\frac{\mathrm{W}}{\mathrm{m}^2\mathrm{K}}\right)(0.04\ \mathrm{m}^2)} + 35°\mathrm{C} = \mathbf{60°C}$



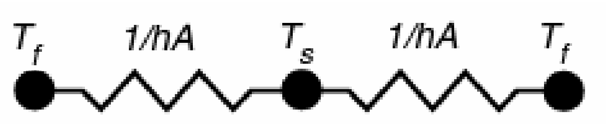


$q = hA_s(T_s - T_f)$

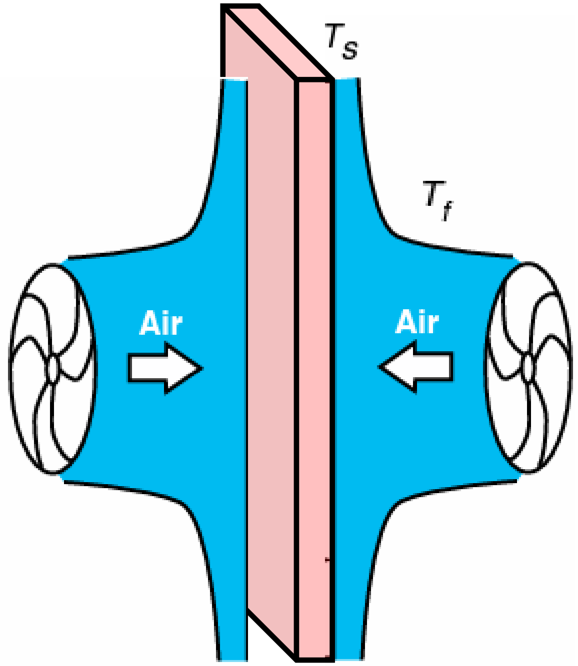
Example: Convection

Estimate the power dissipation from the same PWB to maintain the same average temperature if it were cooled using air in two-sided forced convection, flowing at a sufficiently high velocity (4–5 m/s) across the surface of the PWB to yield an h of 25 W/m²K.

- $T_s = 60$ °C
- $T_f = 35$ °C
- $h = 25$ *W/m²K*
- $A_s = $ (20 cm x 20 cm)= 0.04 m² (per side)
- $q = ?$



$$q = hA_s(T_s - T_f)$$



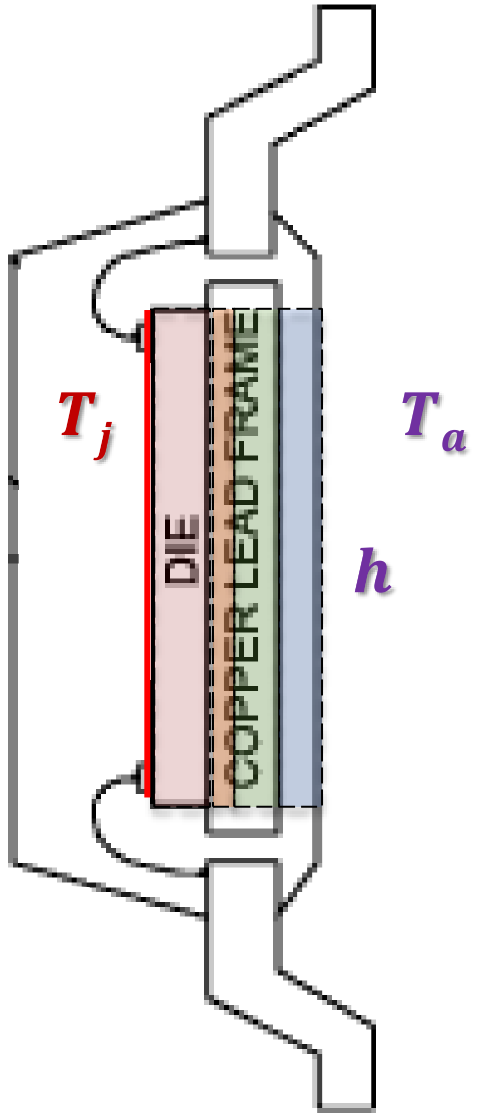
- $q = 2h(A_s)(T_s - T_f) = 2\left(25\,\frac{\mathrm{W}}{\mathrm{m^2K}}\right)(0.04\ \mathrm{m}^2)(60°\mathrm{C} - 35°\mathrm{C}) = \mathbf{50\ W}$

➢ 5x higher power dissipation with forced convection

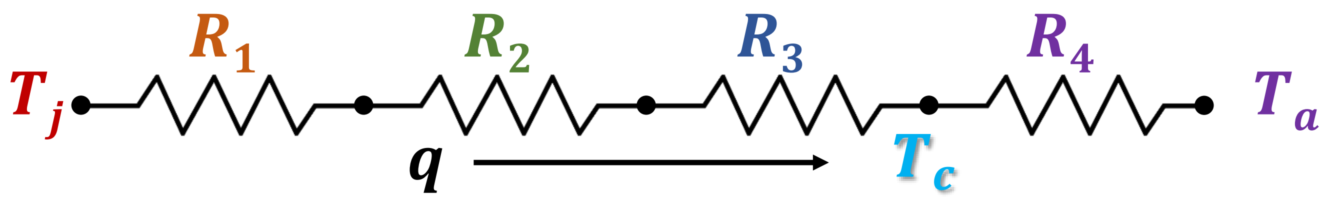
Example: Package Thermal Resistance

Find the junction temperature, T_j, of the die if it dissipates 1 W of heat and has the below specifications.

- $T_a = 25$ °C
- $A_c = 10$ x 10 mm^2 (for all components)
- Solder die attach: $k_1 = 50$ W/(m·K), $L_1 = 0.1$ mm
- Cu lead frame: $k_2 = 390$ W/(m·K), $L_2 = 1$ mm
- EMC: $k_3 = 0.23$ W/(m·K), $L_3 = 1$ mm
- Forced convection (bottom): $h = 200$ W/m^{2}K
- Assume other sides are thermally insulated, that the die is at a uniform temperature, and that the heat flow is uniformly distributed in each layer.



Example: Package Thermal Resistance



$$\boldsymbol{R_{th,cond} = \frac{L}{kA_c}}$$

$$\boldsymbol{R_{th,conv} = \frac{1}{hA_s}}$$

- $T_j - T_a = qR_{th,j-a}$
- $R_{th,j-a} = R_1 + R_2 + R_3 + R_4$
- $R_1 = \frac{L_1}{k_1 A} = \frac{100\times10^{-6}\mathrm{m}}{\left(50\frac{\mathrm{W}}{\mathrm{mK}}\right)(1\times10^{-4}\mathrm{m}^2)} = 0.02\ \mathrm{K/W}$
- $R_2 = \frac{L_2}{k_2 A} = \frac{1\times10^{-3}\mathrm{m}}{\left(390\frac{\mathrm{W}}{\mathrm{mK}}\right)(1\times10^{-4}\mathrm{m}^2)} = 0.03\ \mathrm{K/W}$
- $R_3 = \frac{L_3}{k_3 A} = \frac{1\times10^{-3}\mathrm{m}}{\left(0.23\frac{\mathrm{W}}{\mathrm{mK}}\right)(1\times10^{-4}\mathrm{m}^2)} = \mathbf{43\ K/W}$
- $R_4 = \frac{1}{hA} = \frac{1}{\left(200\frac{\mathrm{W}}{\mathrm{m^2K}}\right)(1\times10^{-4}\mathrm{m}^2)} = \mathbf{50\ K/W}$