Homework #3

Due Thursday, March 6th, by 11:59pm

Show all of your work to receive credit. Your solutions should be neat and easy to read and follow. Highlight, underline, or put a box around the final answers. Submit your solutions through the Canvas Assignments page. Submit one file with all of the problem solutions to Canvas; do not submit multiple files each with a solution to a different problem or upload a .zip folder (this increases grading time and may result in us missing solutions to some problems). No late homework will be accepted, unless approved by the instructor prior to the due date. Discussion of the course material with fellow students and the instructor is encouraged, but the homework solutions must be your individual work. You are not allowed to share any part of your solutions with other students.

The Virginia Tech honor code pledge for assignments is as follows: "I have neither given nor received unauthorized assistance on this assignment." The pledge is to be written out on all graded assignments at the university and signed by the student. The honor pledge represents both an expression of the student's support of the honor code and a commitment to uphold the academic standards at Virginia Tech. Please see the Honor System section of the syllabus on Canvas for details.

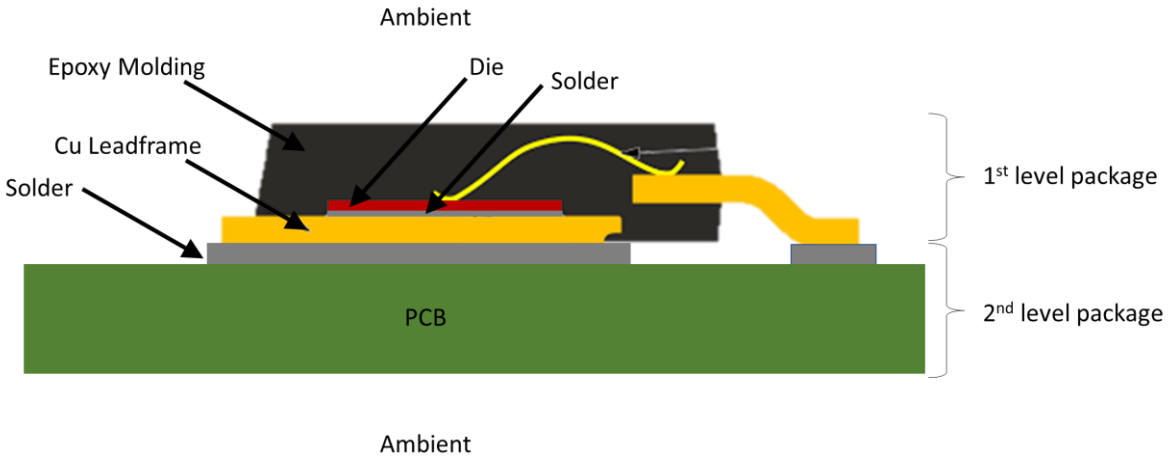

Figure 1: Package for problem 1.

1. For the package shown in Figure 1:
    a. Draw the junction-to-ambient thermal resistance network for the package (consider the 1st and 2nd level packages together as one network). Include a thermal resistance for each layer. Assume that the heat only flows through the top and bottom of the package and that the heat is generated in the die and that the die is at a uniform temperature. Neglect interface thermal resistances (i.e., resistances at the interfaces between the labeled materials/layers) and heat transfer due to radiation. Label each resistance appropriately so that it is clear which component it corresponds to. Also label the junction, case (top and bottom for the 1st level package), and ambient temperature nodes in the network.

b. Write an equation for the total junction-to-ambient thermal resistance for the package (consider the 1st and 2nd level packages together as one network) based on the thermal resistance network drawn in part a. Label each resistance appropriately so that it is clear which component it corresponds to.

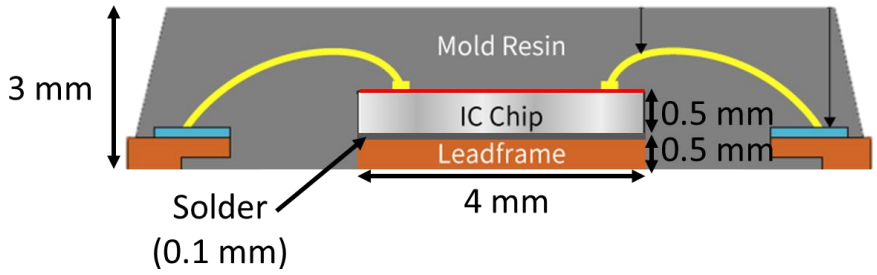

Figure 2: Package for problem 2.

2. Calculate the junction-to-case thermal resistance through i) the bottom and ii) the top of the package in Figure 2. The leadframe is made of copper and has a thermal conductivity of 390 W/mK, the epoxy molding compound has a thermal conductivity of 0.25 W/mK, the solder die attach has a thermal conductivity of 50 W/mK, and the silicon die has a thermal conductivity of 120 W/mK. Assume the heat is generated at the top surface of the die (indicated by the red line at the top of the die). Consider the die in the thermal resistance calculation. The die and the leadframe each have dimensions of 4 mm × 4 mm × 0.5 mm. The solder die attach is 4 mm × 4 mm × 0.1 mm. The epoxy is 3 mm thick. Since the epoxy has a low thermal conductivity, you can assume that the heat does not spread in the epoxy.
    a. Will most of the heat flow through the top or bottom of the package? Explain why this is with details related to the package structure, materials, etc.
    b. How could the junction-to-case thermal resistance be reduced? Give two ways and briefly explain your answers.

3. Assume there is a heat-generating chip with a size of 3 mm × 3 mm that is attached to a copper base plate with a size of 5 mm × 5 mm. Assume all of the heat is dissipated down through the base plate (i.e., that there is negligible heat flow through the top or sides).
    a. Calculate the thermal resistance of the base plate when the base plate thickness is: (i) 0.5 mm, (ii) 1 mm, and (iii) 3 mm. Assume the chip has a uniform temperature and the heat spreading angle in the copper base plate is 45 degrees. The thermal conductivity of copper is 390 W/(m·K). For each case, draw a 2D view of the die and base plate and indicate the heat spreading in the base plate. Drawing the image to scale is recommended to properly show the heat spreading.
    b. For the chip and base plate areas given in this problem, what would be an optimal base plate thickness? Derive an equation for calculating this optimal thickness and explain why this would be an optimal thickness. Consider the impact on conductive and convective heat transfer. Explain your answer.

4. Two chips are attached to the same copper base plate. One of the chips has an area of 2 mm × 2 mm and the other has an area of 5 mm × 5 mm. The copper base plate is 2 mm thick.

a. What is the minimum distance that the two chips should be spaced (edge-to-edge) to prevent thermal coupling between them? Assume a heat spreading angle of 45 degrees.
b. What is the minimum width that the base plate should be to prevent thermal coupling between the two chips while still enabling the heat to fully spread to the edge of the base plate? Assume a heat spreading angle of 45 degrees.
c. Give two negative consequences of increasing the spacing between chips in a multi-chip module. Briefly explain your answers.

5. Plot the thermal resistance versus percent voiding content (from 10 % to 90 %) for a solder joint. The thermal conductivity of the solder is 50 W/mK and the thermal conductivity of the voids is 0.024 W/mK (air). The thickness of the solder joint is 100 µm and the area is 20 mm^2. Assume uniform heating throughout the solder joint (i.e., neglect heat spreading). Show the equations and work used for the plot. Label the axes (include units) and use appropriate font sizes so that the axes are easy to read (we should not have to zoom into the document to be able to read the font).

6. A PCB with 4 layers of copper and 5 layers of dielectric is being designed. The thermal conductivity of the dielectric is 0.25 W/mK, and each dielectric layer is 215 µm thick. The thermal conductivity of copper is 390 W/mK. It is desired to achieve a minimum equivalent thermal conductivity in the xy plane of 60 W/mK for the entire PCB.
   a. What is the minimum copper thickness (in µm) required per layer to achieve this minimum equivalent thermal conductivity? Assume that all of the copper layers are the same thickness and assume uniform heat flow (i.e., neglect heat spreading).
   b. Table I lists the standard oz copper options available for PCBs. What standard oz copper should be selected to meet the thermal requirements for this PCB.

Table I: PCB Copper Thickness [1]

oz	1	1.5	2	3	4	5	6	7	8	9
mils	1.37	2.06	2.74	4.11	5.48	6.85	8.22	9.59	10.96	12.33
inch	0.00137	0.00206	0.00274	0.00411	0.00548	0.00685	0.00822	0.00959	0.01096	0.01233
mm	0.0348	0.0522	0.0696	0.1044	0.1392	0.1740	0.2088	0.2436	0.2784	0.3132
µm	34.80	52.20	69.60	104.39	139.19	173.99	208.79	243.59	278.38	313.18

References

[1] https://pcbprime.com/pcb-tips/how-thick-is-1oz-copper/