Homework #2

Due Wednesday, February 26th, 2025 by 11:59pm

Show all of your work to receive credit. Your solutions should be neat and easy to read and follow. Highlight, underline, or put a box around the final answers. Submit your solutions through the Canvas Assignments page. No late homework will be accepted, unless approved by the instructor prior to the due date. Discussion of the course material with fellow students and the instructor is encouraged, but the homework solutions must be your individual work. You are not allowed to share any part of your solutions with other students.

The Virginia Tech honor code pledge for assignments is as follows: "I have neither given nor received unauthorized assistance on this assignment." The pledge is to be written out on all graded assignments at the university and signed by the student. The honor pledge represents both an expression of the student's support of the honor code and a commitment to uphold the academic standards at Virginia Tech. Please see the Honor System section of the syllabus on Canvas for details.

1. Using ANSYS Q3D Extractor, draw a wire bond using the Draw Bondwire tool on the Draw tab. Use the JEDEC 4-point type wire bond. Set the material as gold, diameter to 2 mil, h1 (the loop height) to 3 mm, and h2 (the height offset between the first and second bonds) to 0 mm. Leave the default number of facets (6). To make the total length (including the loop) equal to 10 mm, set the distance to 6.3 mm (expand them model tree, select CreateBondwire, and type "6.3" into the "Distance" cell in the Properties window). Use the faces at either end of the wire bond for the source and sink. Simulate the DC resistance and AC resistance at 500 MHz. Enter the values into rows 1 and 2, column 3 ("ANSYS Q3D"), of Table I. Calculate the percent error between the simulated results and the calculated results from problems 1 and 2 of homework #1 (already provided in rows 1 and 2, column 2 "Calculation"; note: the values have been adjusted to use the same resistivity value as ANSYS Q3D uses). Assume that the calculated values are the estimates and the simulated values are the actual. Enter the percent error into column 4 of Table I. Include screenshots of the wire bond and solution matrix.

2. Using ANSYS Q3D Extractor, draw a flat ribbon bond using the Draw Box tool on the Draw tab. Set the material as gold, thickness to1 mil, width to 10 mil, and the length to 10 mm. Use the faces at either end of the ribbon for the source and sink. Simulate the DC resistance and AC resistance at 500 MHz. Enter the values into column 3, rows 3 and 4 of Table I. Calculate the percent error between the simulated results and the calculated results from problem 3 of homework #1 (already provided in rows 3 and 4, column 2 "Calculation"; note: the values have been adjusted to use the same resistivity value as ANSYS Q3D uses). Assume that the calculated values are the estimates and the simulated values are the actual. Enter the percent error into column 4 of Table I. Include screenshots of the flat ribbon and solution matrix.

Table I: Calculation and ANSYS Q3D Comparison

Component and Parameter	Calculation*	ANSYS Q3D**	Percent Error (%)
Wire bond DC resistance	120.4 mΩ		
Wire bond AC resistance at 500 MHz	467.2 mΩ		
Ribbon DC resistance	37.8 mΩ		
Ribbon AC resistance at 500 MHz	127.4 mΩ		

*These values are the results from homework #1 at room temperature and with the resistivity value adjusted to be the same as used in ANSYS Q3D.

**Enter these values from the ANSYS Q3D simulations performed in problems 1 and 2 in this homework assignment.

3. Using ANSYS Q3D Extractor, draw a wire bond using the Draw Bondwire tool on the Draw tab. Use the JEDEC 4-point type wire bond. Set the material as aluminum, diameter to 5 mil, h1 (the loop height) to 3 mm, and h2 (the height offset between the first and second bonds) to 0 mm. Leave the default number of facets (6). Use the faces at either end of the wire bond for the source and sink. Simulate the DC self-inductance for total lengths (including the loops) of 10 mm, 15 mm, and 20 mm (set the "distance" to 6.3, 11.5, 16.7, respectively).
    a. Plot the self-inductance (in nH) versus length (in mm). On the same plot, include a curve using the rule of thumb (1 nH/mm), and the simplified self-inductance equation for a wire (problem 4 from homework #1). Label the axes (include units), and the three curves. The axes and labels must be legible. Include screenshots of the wire bonds and solution matrix.
    b. What is the reason for the discrepancy between the calculated and simulated values? Use ANSYS Q3D to provide justification for your answer.

4. Consider that a chip is packaged in the quad-flat package (QFP) with 32 leads shown in Figure 1. The leads are all made of copper, and epoxy molding compound (EMC) is used for the housing and encapsulant. Figure 2 shows three arrangements for the supply (V_{cc}) and ground (*GND)* lead assignments. For all cases, there is only one voltage source V_{cc} and only one ground *GND*. For (b) and (c), there are two leads in parallel for the V_{cc} and *GND*. The leads all go to the same chip/load.
    a. Draw the equivalent circuit schematics for each of the cases shown in Figure 2. Include the resistances, self-inductances, and mutual inductances for the leads. Only include the mutual inductances for adjacent leads. Neglect the parasitic capacitances. Only the leads that are highlighted in Figure 2 are to be considered (i.e., no wire bonds). Represent the input as a voltage source and the semiconductor die (not pictured) as a capacitive load. Clearly label each of the elements in the circuit such that it is clear which QFP lead they correspond to.
    b. Rank the three cases shown in Figure 2 in order from lowest to highest total inductance for the supply–ground loop for the leads. Explain your reasoning for the proposed ranking. *Optional*: you can use the provided .step file of the QFP package on Canvas to simulate the three cases to verify your answer, though an explanation must still be provided.

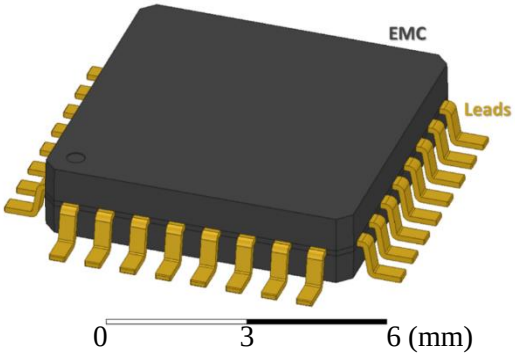
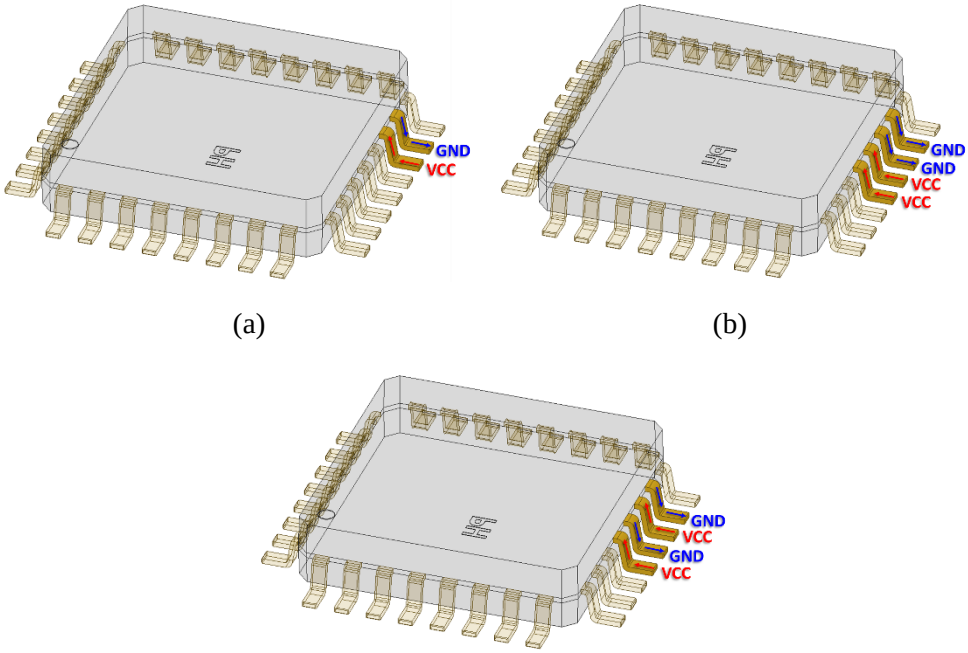


Figure 1: Quad-flat pin (QFP) package with 32 leads.



(a) (b)

(c)

Figure 2: Three cases to be considered in problem 4: (a) one supply (V_{cc}) lead adjacent to one return (*GND*) lead, (b) two parallel supply (V_{cc}) leads adjacent to two parallel return (*GND*) leads, (c) two parallel supply (V_{cc}) leads interleaved with two parallel return (*GND*) leads. Red arrows indicate the direction of the current in the supply (V_{cc}) lead(s). Blue arrows indicate the direction of the current in the return (*GND*) leads.

5. A signal with a 1 GHz clock frequency and a rise time of 100 ps is going through an interconnect with a length of 1 cm. The interconnect is routed through a PCB substrate made of FR4 epoxy. FR4 epoxy has a dielectric constant of 4.4. Should transmission line effects be considered? Explain why or why not.

6. A packaging technology has the following rules: line width = 150 µm, signal line thickness = 20 µm, and dielectric thickness = 200 µm from the nearest ground plane. The dielectric

constant of the insulator is 4.0. You can assume the relative permeability for the conductor is 1. Calculate the characteristic impedance Z_0 and the velocity of propagation v_p if these rules are used to construct a 1) microstrip line, 2) an embedded microstrip line, and 3) strip line. Which structure has the highest propagation velocity? Why?