VIRGINIA TECH

Lecture 1

Introduction to Electronics Packaging

January 21, 2025

ECE 4254/5224: Principles of Electronics Packaging

- **Instructor**: Dr. Christina DiMarino
- **Lectures**: Tu/Th 5:00pm – 6:15pm
  - All lectures will be recorded and uploaded to Canvas (Media Gallery)
  - Note: the captions have errors, especially for technical terms
- **Office Hours**: Check the Canvas calendar, as office hours may vary certain weeks
  - Typical times: MW 3:30pm-4:30pm
- **Grading**: homework (40 %), group project (30 %), midterm (20 %), quizzes & in-class small-group work (10 %)

Who is in this course?

- ECE 4254 (undergraduate)
  - Computer engineering
  - Electrical engineering
  - Energy & power electronics systems
  - Micro/nano systems
  - Space systems

→ Location: Blacksburg

- ECE 5224 (graduate)
  - MEng, MS, PhD
  - Computer engineering
  - Electrical engineering
  - Materials science & engineering

→ Locations: Blacksburg, NCR, and Virtual

Course Topics

1. Introduction (10%)
2. Electrical (20%)
3. Thermal (20%)
4. Materials and Processes (25%)
5. Reliability and Failure Mechanisms (10%)
6. Characterization and Testing (10%)
7. Emerging Technologies (5%)

+ Software and lab demos (677/678 WHIT & 5-021 VTRC)

Course Software

1. LTspice

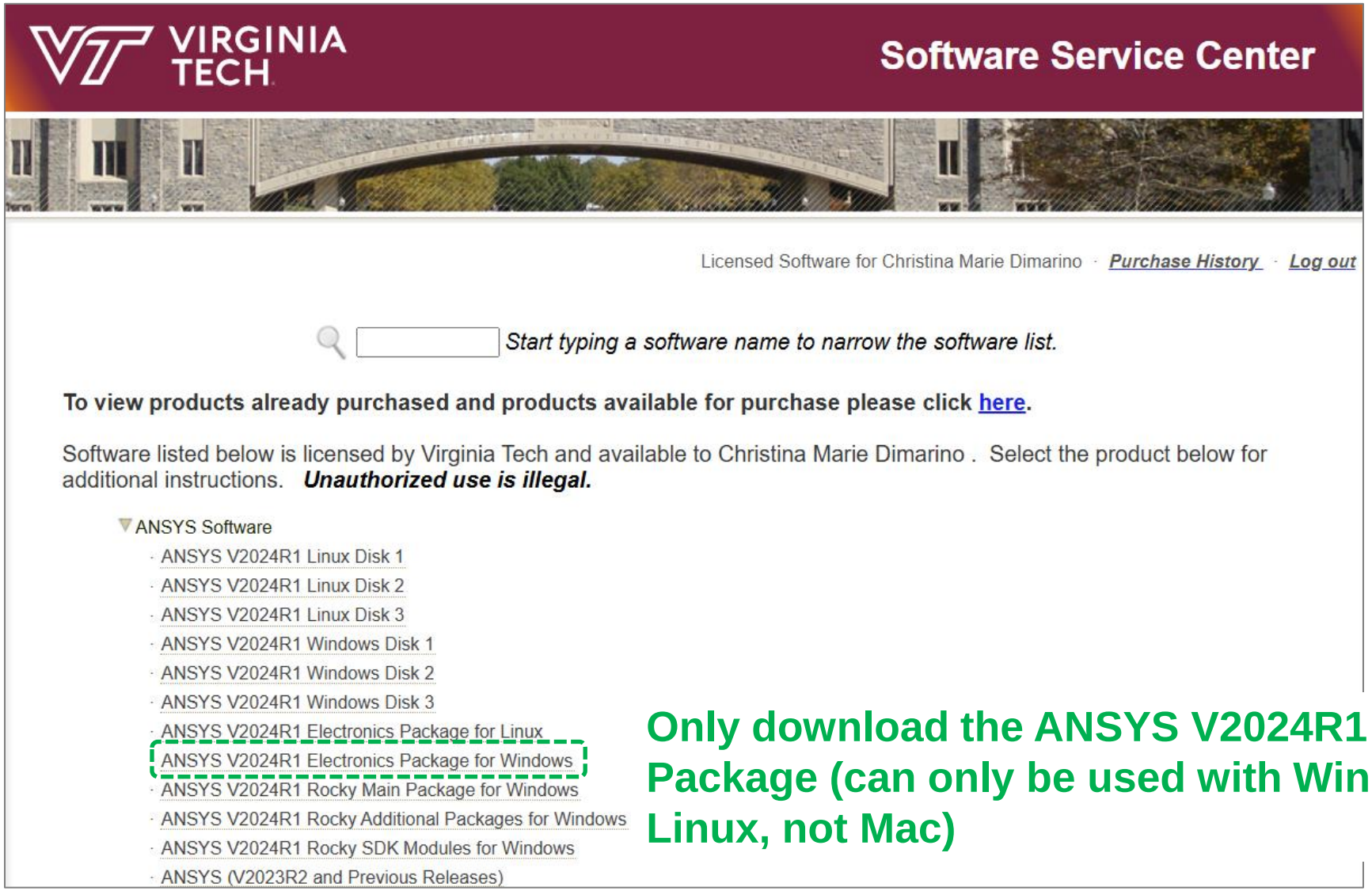
- Circuit simulator
- Free download: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

2. ANSYS V2024R1 Electronics Package

- Electrical and thermal finite element analysis (FEA) software
- Download: https://onecampus.vt.edu/task/all/network-software
- Download and installation instructions on the following slides

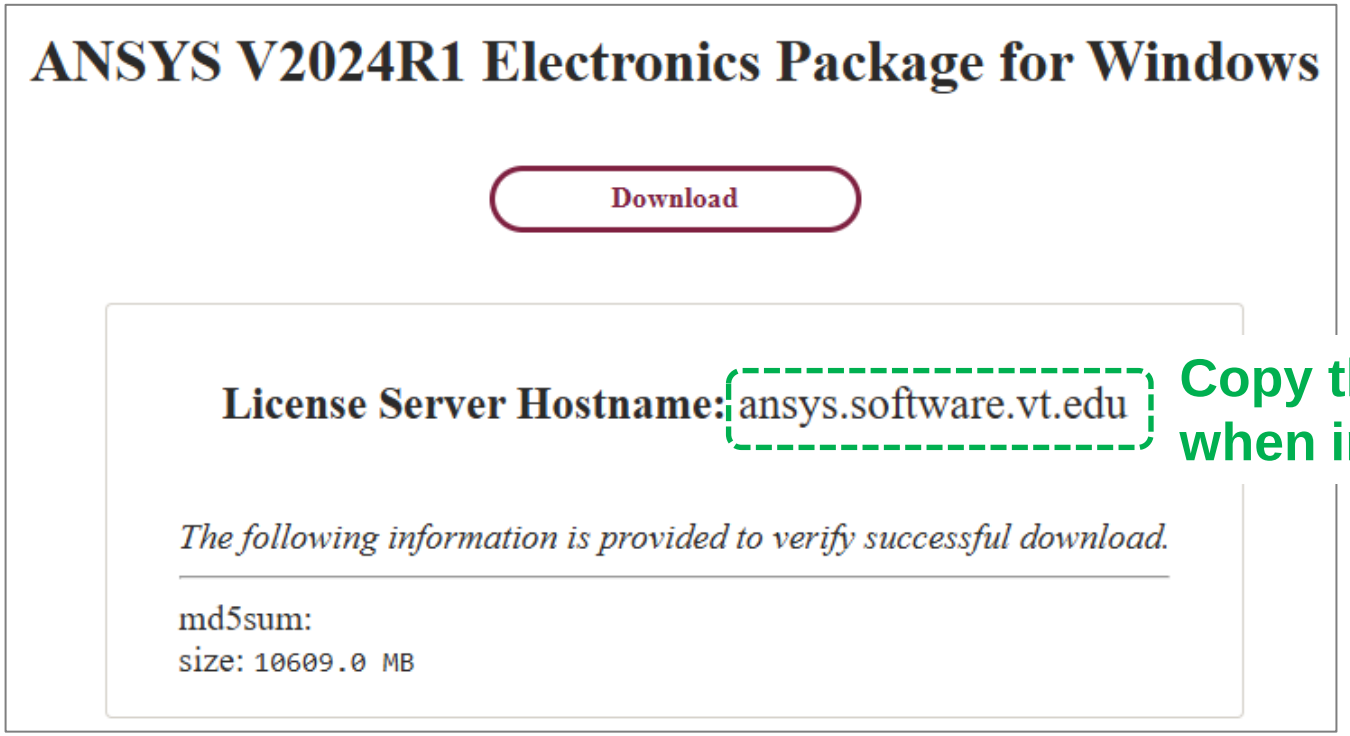
ANSYS Electronics Package Download

https://onecampus.vt.edu/task/all/network-software



Only download the ANSYS V2024R1 Electronics Package (can only be used with Windows or Linux, not Mac)

ANSYS Electronics Package Download



Copy this. You will need it when installing ANSYS.

ANSYS Electromagnetics Suite Installation

ANSYS Installation

***For Windows 8 usernames** we would suggest creating a new Local User Account that matches the PID, logging in, and installing ANSYS on that account. This can be done through Control Panel -> User Accounts -> Manage another account -> Add a new user.

Note: For ANSYS to activate correctly, it must be installed on the C:\ drive and the windows username must match the student's VT PID.

Changing Windows 7 & 10 Username

1. Find the "*Run...*" box or the "*Search*" box.
2. Enter compmgmt.msc
3. System Tools -> Local Users and Groups -> Users
4. Right click on your username and select "*Rename*"
5. Enter your Virginia Tech PID exactly and hit enter.
6. Exit the Computer Management tool and logout of your modified user account.
7. Restart the computer.

To connect to the license server off-campus, you must use VPN. See link below for setup instructions.

https://vt4help.service-now.com/sp?id=kb_article&sys_id=d5496fca0f8b4200d3254b9ce1050ee5

CPES Packaging Lab (677/678 WHIT)

- Substrate patterning and cutting (laser, etcher)
- Die attach (soldering, sintering)
- Interconnect (wire bonding)
- Encapsulation (degassing, curing)

https://cpes.vt.edu/about/facilities

CPES Packaging Lab (677/678 WHIT)

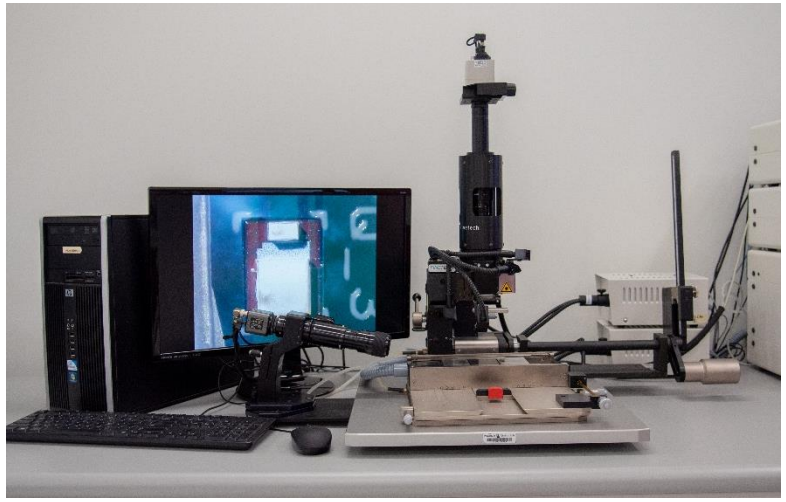
- Bond tester (die shear test, wire bond pull test)
- Static electrical characterization (curve tracer)
- Reliability (thermal cycling chamber)

https://cpes.vt.edu/about/facilities

CPES

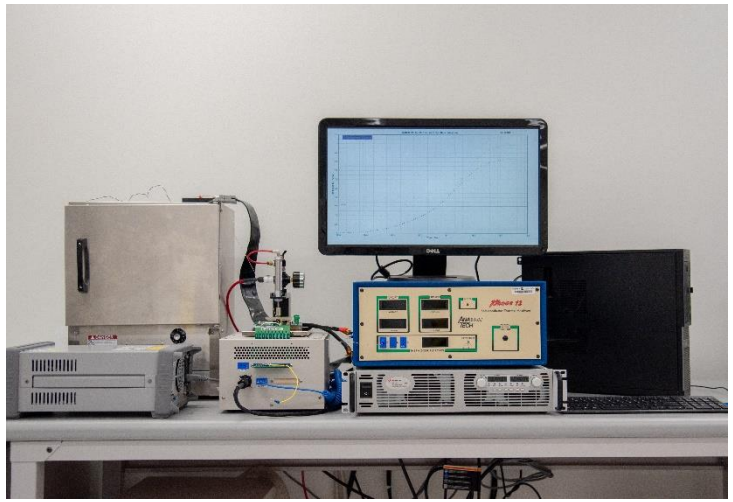
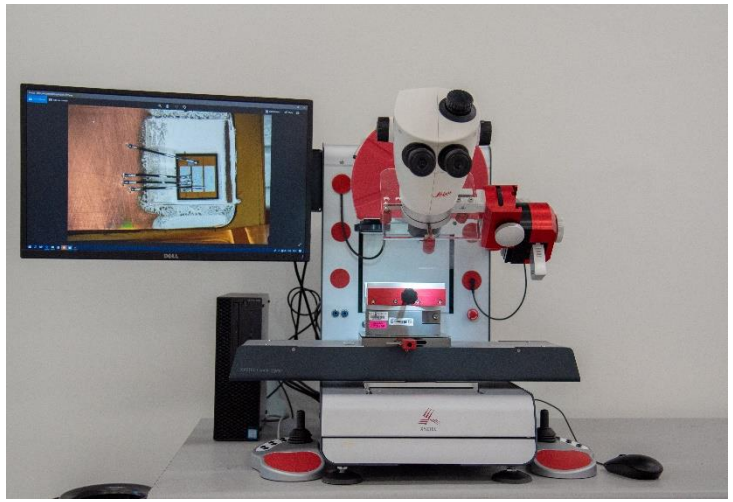
CPES Packaging Lab in Arlington, VA

CPES Packaging Lab in Arlington, VA







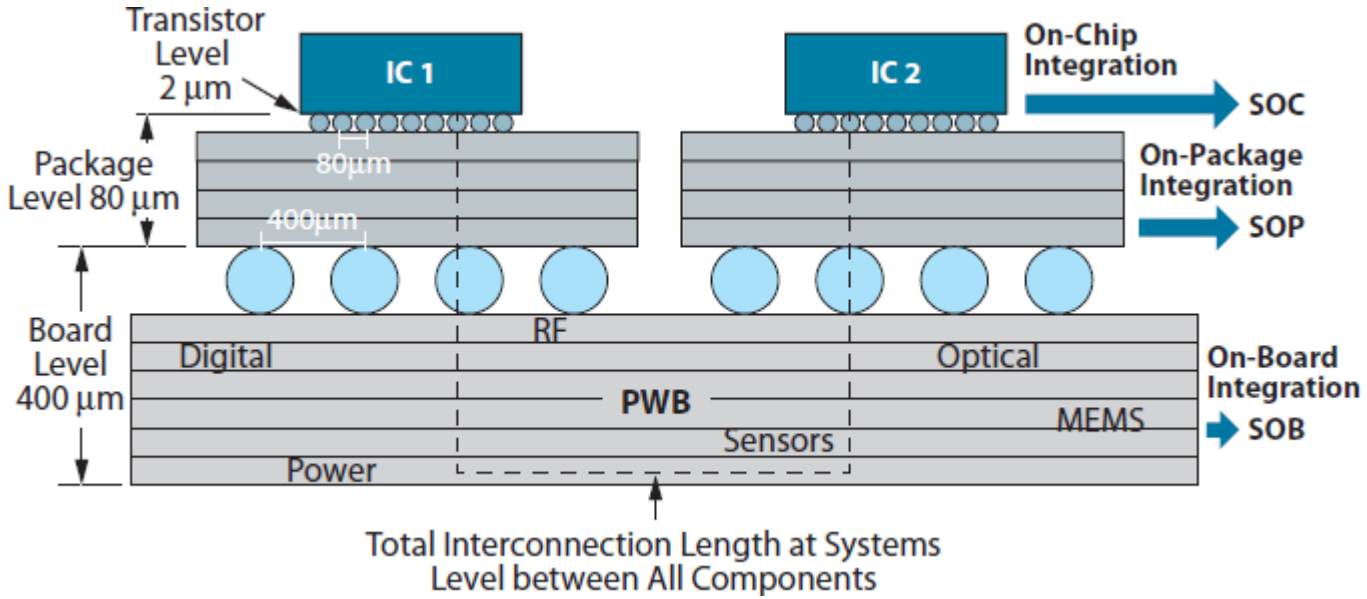

Flip-chip die bonder, pressure sintering, wire bonding, profilometry,
3D printing, thermal resistance measurements and power cycling, bond testing, optical imaging

For More Information…

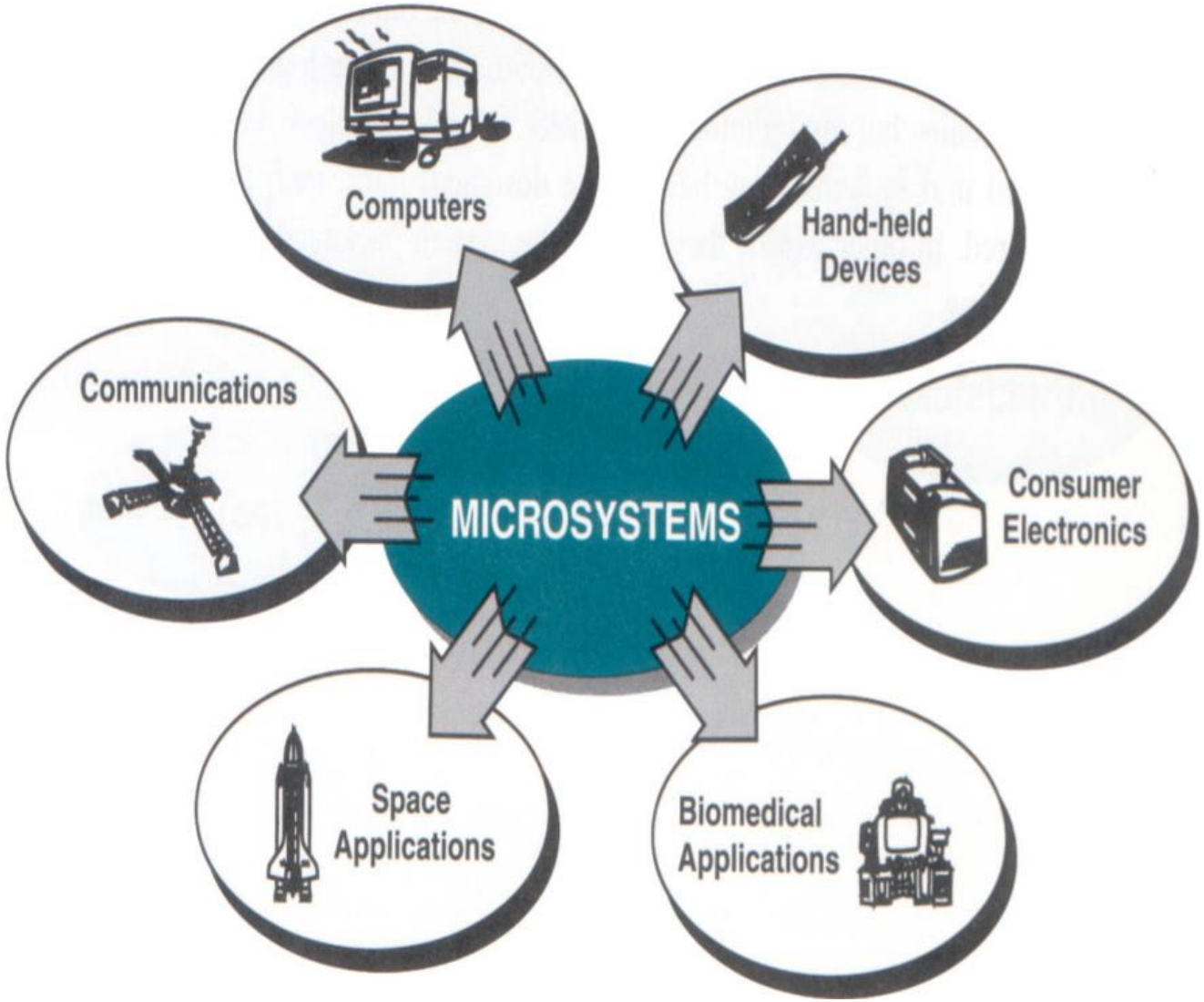
- Fundamentals of Device and Systems Packaging: Technologies and Applications, 2nd edition, Tummala, 2019
  - Fundamentals of Microsystems Packaging, 1st edition, Tummala, 2001
- Essentials of Electronic Packaging, Viswanadham, 2011
- Power Electronic Packaging, Liu, 2012
- *IEEE Transactions on Components, Packaging and Manufacturing Technology* (CPMT)
- IEEE Electronics Packaging Society (EPS)
- International Microelectronics Assembly and Packaging Society (IMAPS)
- Power Sources Manufacturers Association (PSMA)
- International Technology Roadmap for Semiconductors (ITRS)
- Heterogeneous Integration Roadmap (HIR)

Electronics

- Electronics is one of the largest industry segments in the world, and is growing.
- Wide range of applications, spanning defense, consumer, computer, communications, transportation, and medical industries.
- Every electronic product or system includes semiconductor devices, packaging, and system-level assemblies.



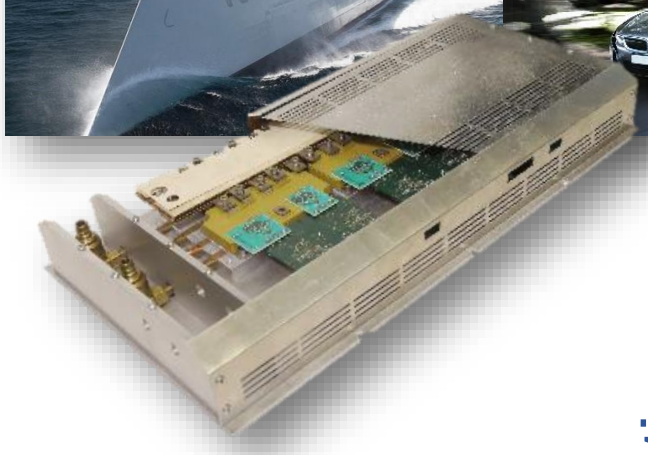
Microelectronics Applications



These applications have different requirements for the package.

Power Applications

Transportation



Electric Grid

Information Technology

Industrial Automation

Example Application Requirements

Category	Operating temperature range (°C)	Design life range (years)
1 Auto—under the hood	(-85 °F) −65 to +150 (300 °F)	5–10
2 Industrial auto	−55 to +95	10 or more
3 Military avionics	−55 to +95	5 or more
4 Commercial avionics	−55 to +95	10 or more
5 Military—ground/marine	−55 to +95	5 or more
6 Space geo/LEO	−40 to +85	5–20
7 Telecommunications	−40 to +85	7–20
8 Computer	+15 to +60	5 or more
9 Consumer/portable	0 to +60	1–3

Automobile — Under the Hood

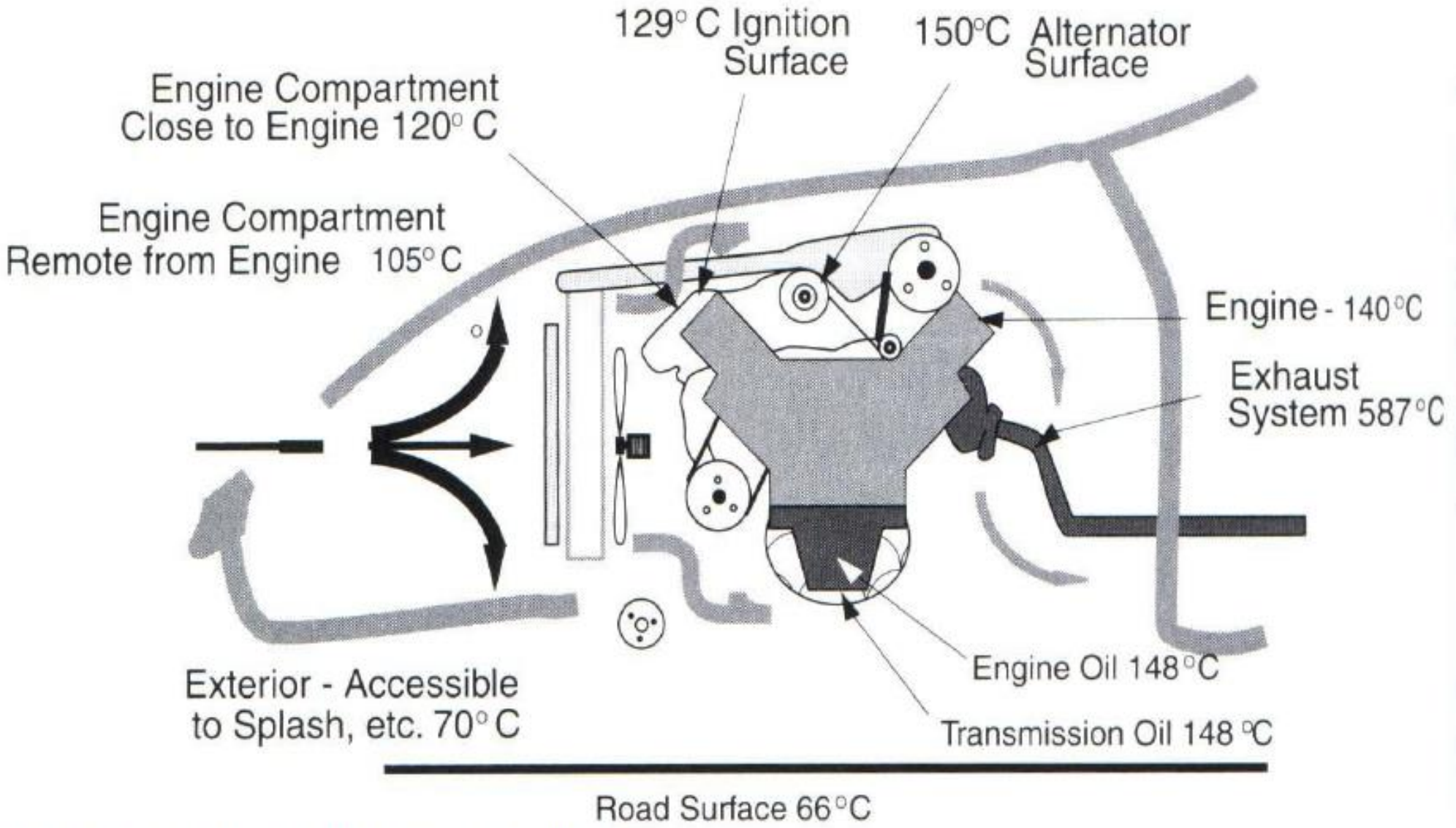


Figure from "Fundamentals of Microelectronics Sys Packaging" Rao Tummala

What is Electronics Packaging?

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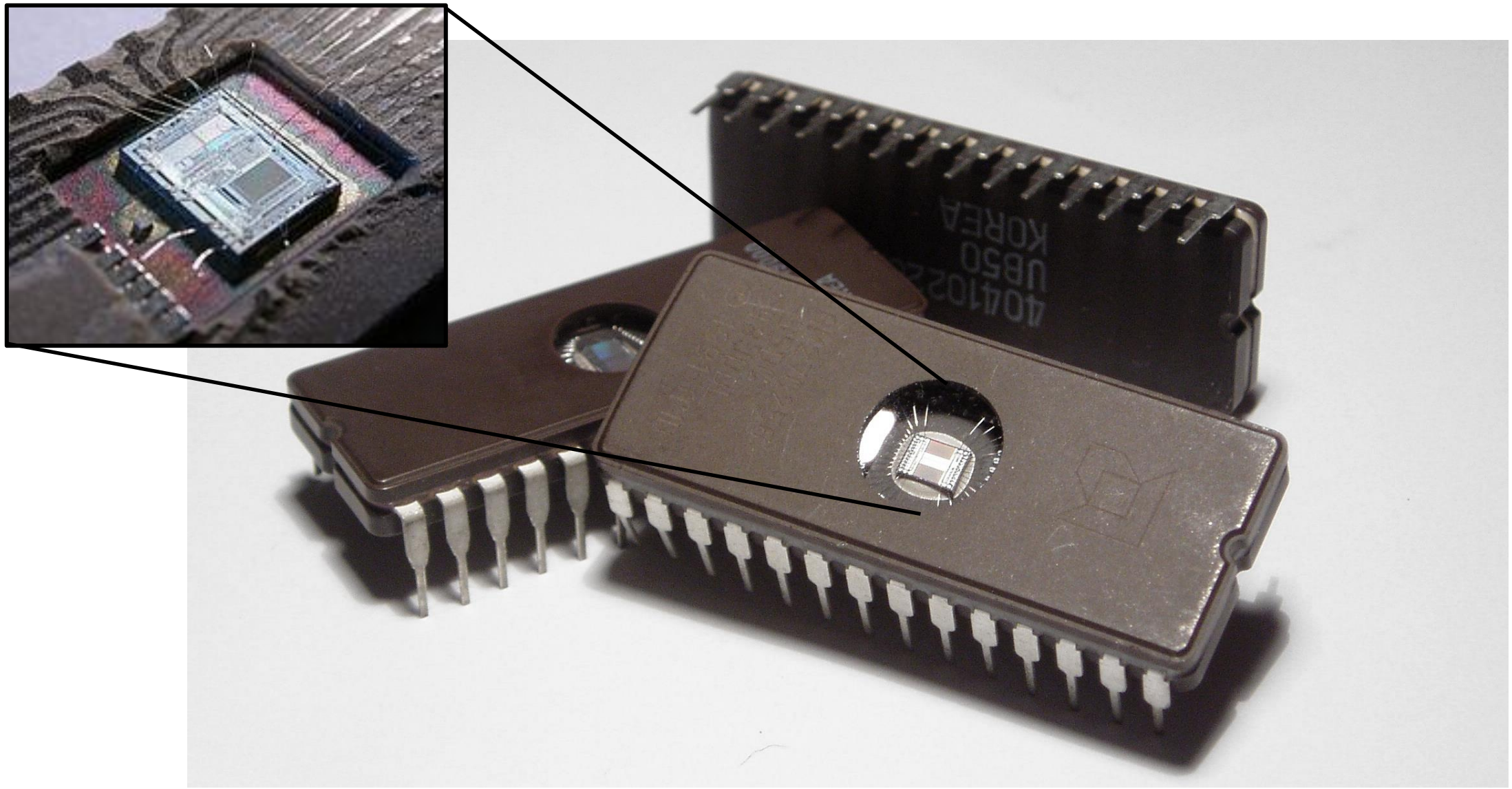
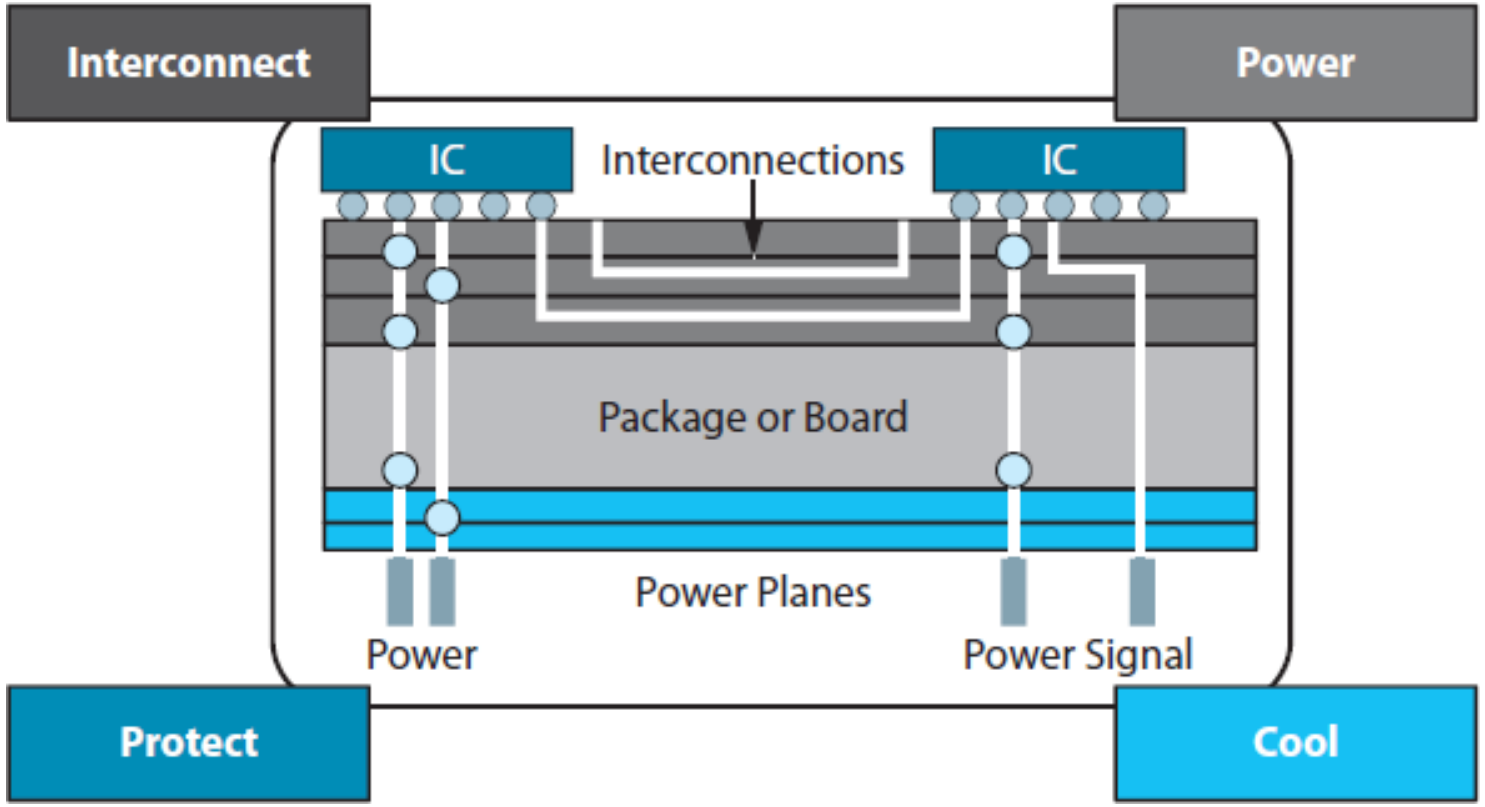


What is Electronics Packaging?

What is Electronics Packaging?

- Interconnecting, powering, cooling, and protecting the semiconductor devices and other system components [so that they perform reliably over a period of time]



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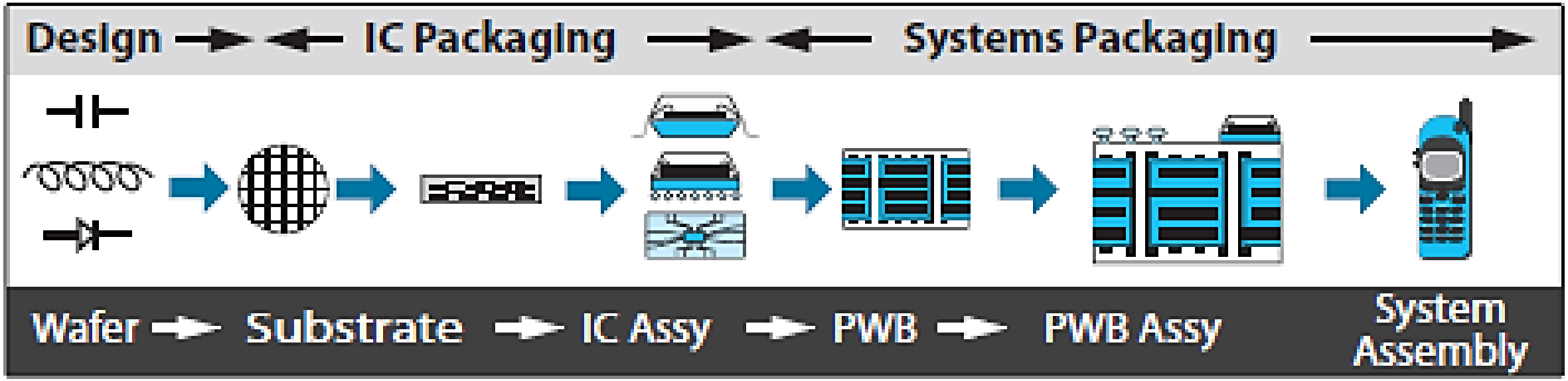


PWB = printed wiring board

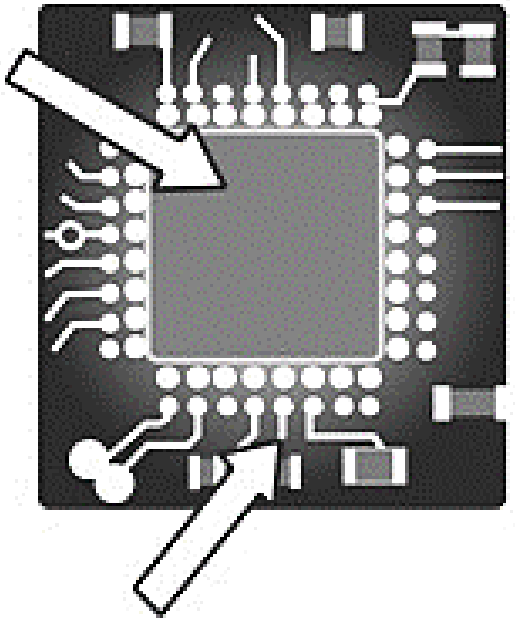
An Analogy…

Brain

IC

Body/Packaging* Controls:

- Size
- Weight
- Performance
- Reliability
- Cost*



Body Packaging

Human

Electronic System

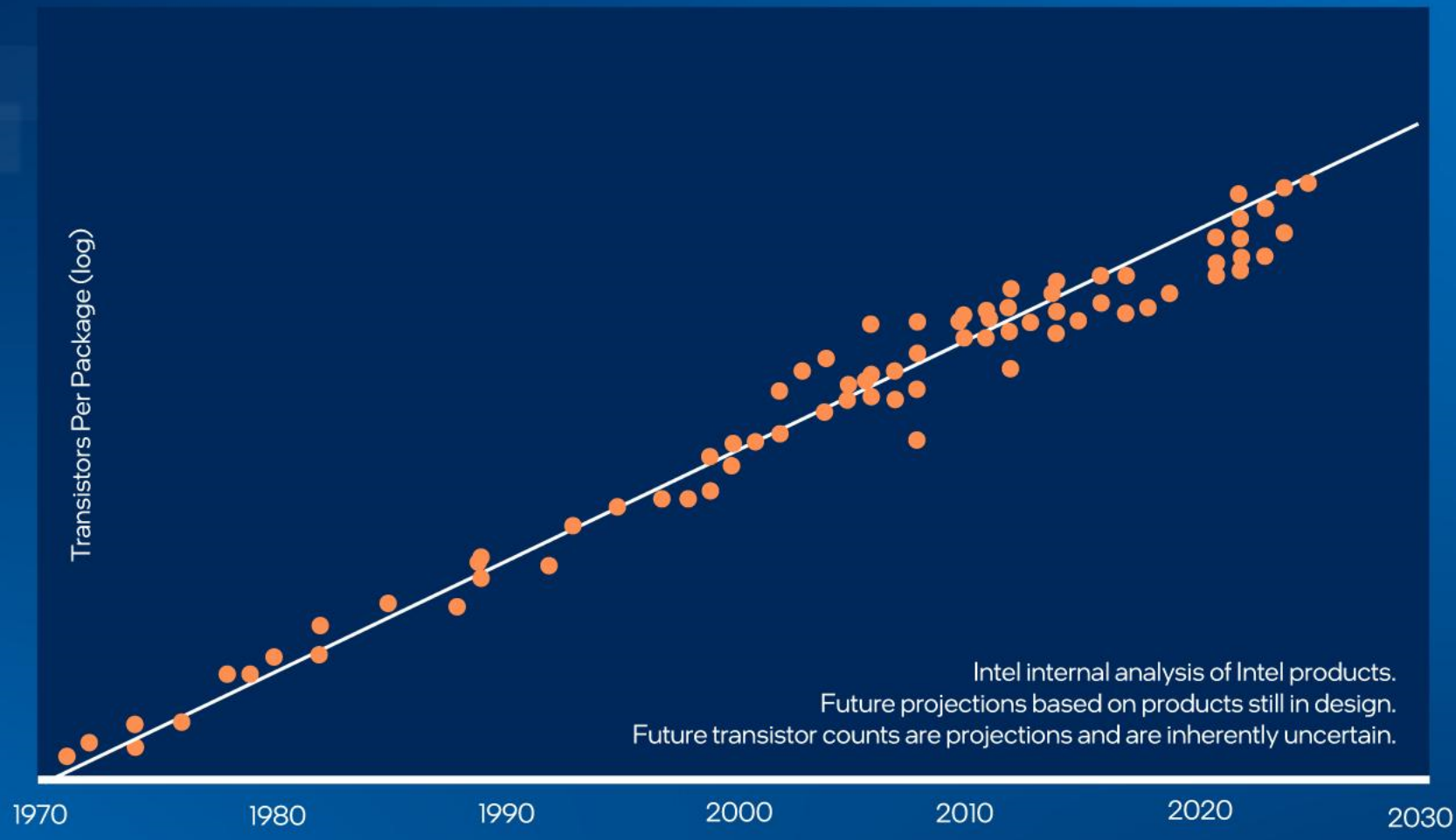
Why is Packaging Important?

- There are **>100 billion** ICs and devices manufactured worldwide, *all of which need to be packaged.*

- Packaging directly impacts the *electrical performance, cost, size, and reliability*.

- Semiconductor packaging market valued at $28B in 2019, and expected **>$40B by 2025** by Mordor Intelligence.

Continuing Moore's Law



Aspiring to

1 Trillion

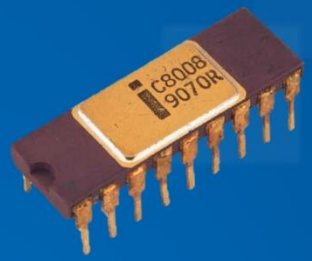
transistors in 2030

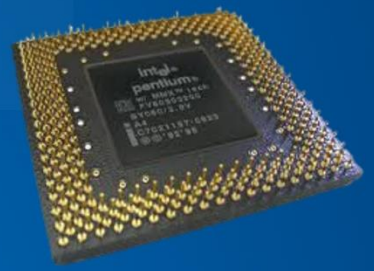
- ✓ RibbonFET
- ✓ PowerVia
- ✓ High NA
- ✓ 2.5D/3D packaging

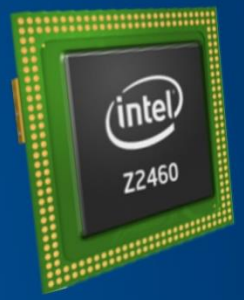
"Advanced packaging gives architects and designers new tools in their pursuit of Moore's Law," — Dr. Kelleher, EVP & General Manager of Technology Development at Intel

intel

intel







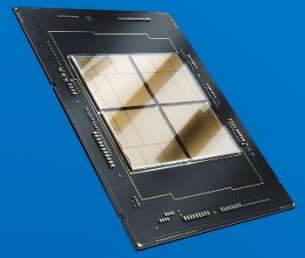
Leadframe / Wirebond

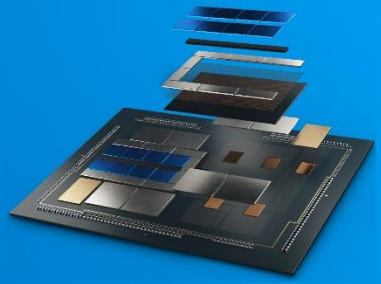
Flip Chip Ceramic

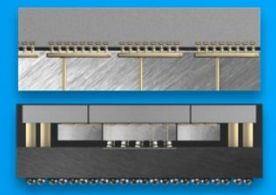
Flip Chip Organic & Multi Chip Pkg

Package main function:
provide power and signaling from motherboard to die

Advanced packaging era







2.5D EMIB

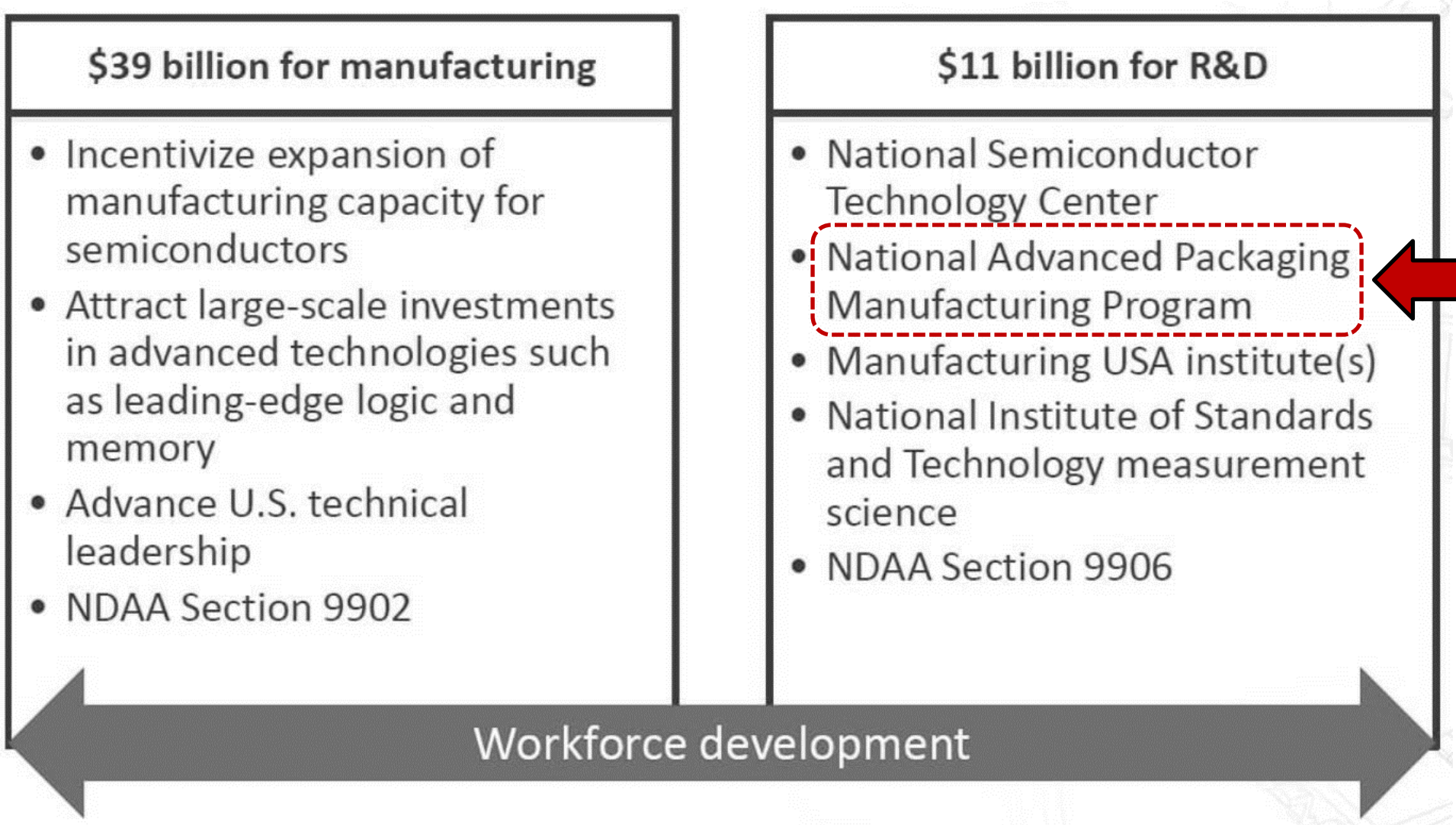
3D Foveros

2.5D EMIB + 3D Foveros

3D Foveros Direct & Omni

Added Package value:
high density interconnects that enable larger die complexes from multiple process nodes

U.S. CHIPS and Science Act



$3B allocated for advanced packaging

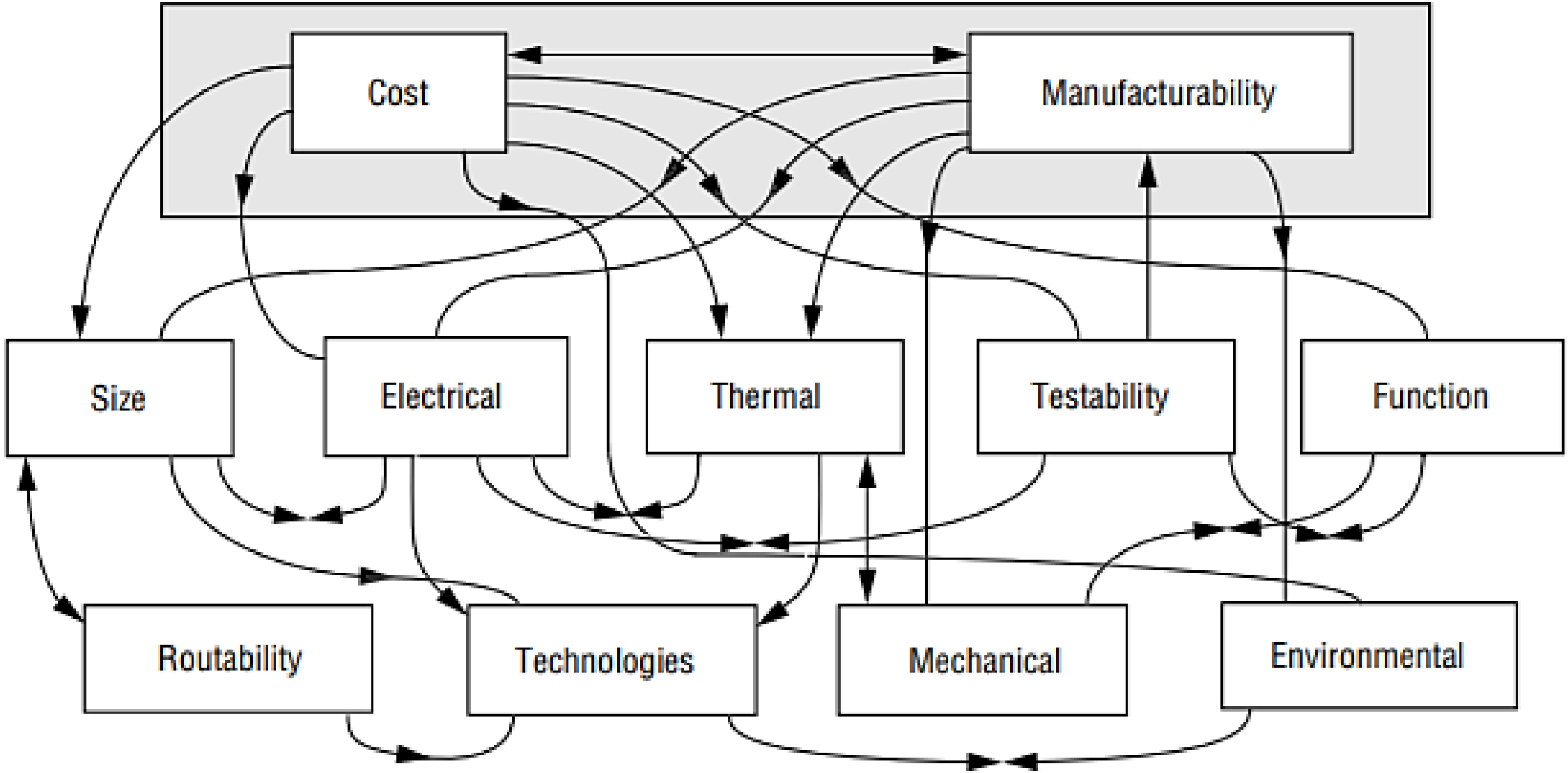
Why is Packaging Needed?

- Package Functions:
  1. Signal distribution & integrity
  2. Power distribution & integrity
  3. Thermal management/heat dissipation
  4. Protection
     - Mechanical
     - Chemical
     - Environmental
     - Electrical
- Impacts:
  1. Performance (e.g., speed)
  2. Cost
  3. Size
  4. Reliability
     - Electrical
     - Mechanical
     - Thermomechanical

Packaging Considerations

- Electrical
- Thermal
- Mechanical
- Reliability
- Manufacturability
- Testability
- Size
- Weight
- Environmental/safety
- Cost
- …

Complex, Interdependent Nature of Packaging

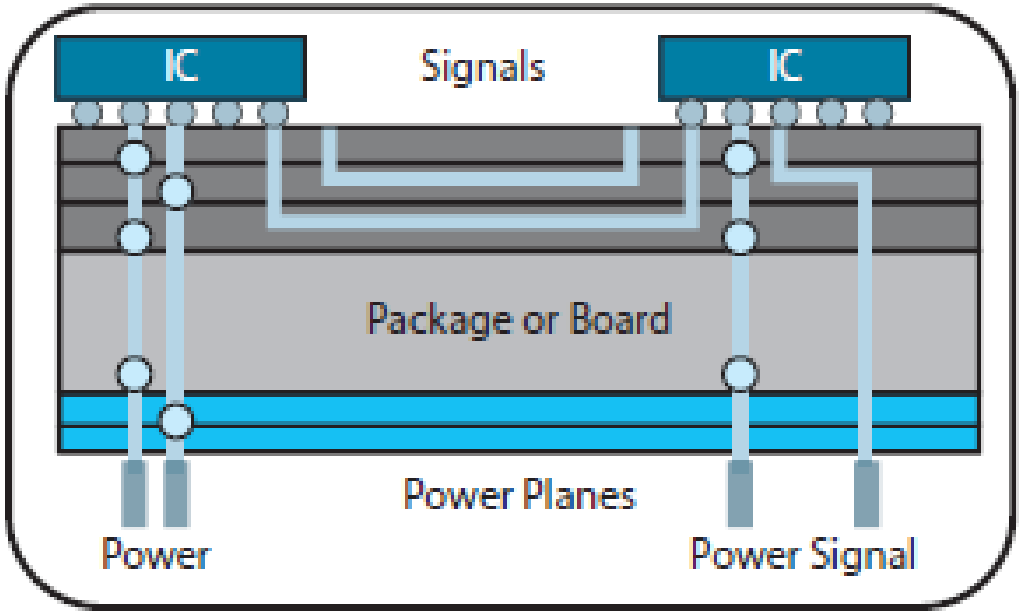


P. Sandborn, M. Vertal, “Analyzing Packaging Trade-Offs During System Design,” IEEE Design & Test of Computers, 1998.

Packaging is an Interdisciplinary Field

Electrical Sciences
- Signal Integrity
- Power Integrity
- EMI

Material Sciences
- Dielectrics
- Conductors
- Magnetics
- Encapsulants
- C, L, R, Materials



Mechanical Sciences
- Thermomechanical Reliability
  - Fatigue and Creep
  - Warpage
- Heat Transfer

Chemical Sciences
- Lithographic Processes
- Microstructure vs. Properties

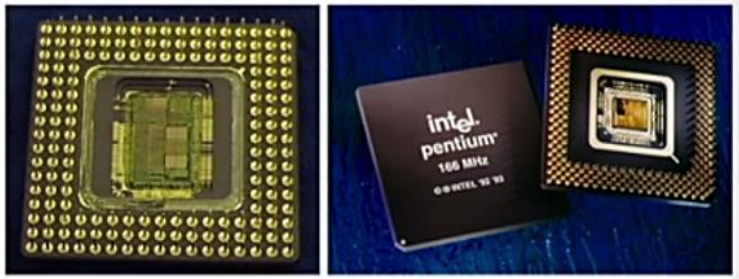
Bioelectronics
- Biocompatible
- Components
- Interconnections

"Quiet" Revolutions in Packaging

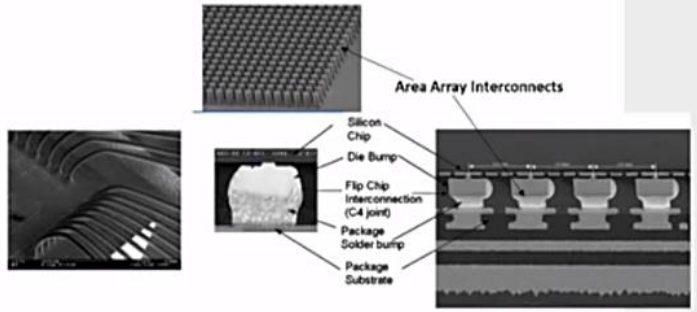
1990s : Packaging revolutionized by launch of the **first flip-chip organic substrate**; A New Package Industry is born

2000s : Copper Pillar Bumps on die are introduced as an extension on Cu backend; Intel leads the industry by deploying **fully lead & halogen free packages**; High Pin Count Land Grid Sockets Become Mainstream; Drive to greater adoption of Ball Grid Arrays enables "Small and Thin"

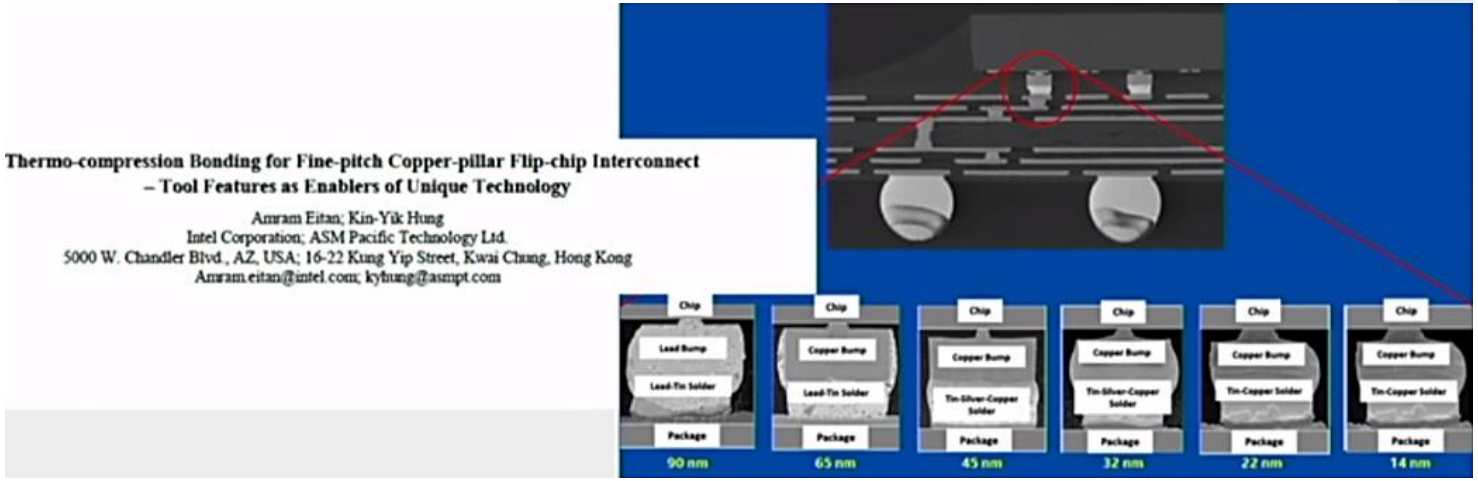
2010s : Thermo-Compression Bonding Tools enable Fine Pitch Flip-Chip; **Multiple Breakthrough 2D Multi-Chip Packaging Technologies (CoWOS, EMIB, FOCOS)** Introduced : **HBM, Foveros, SOIC open up the 3rd Dimension**



Ceramic Packaging → Organic Packaging

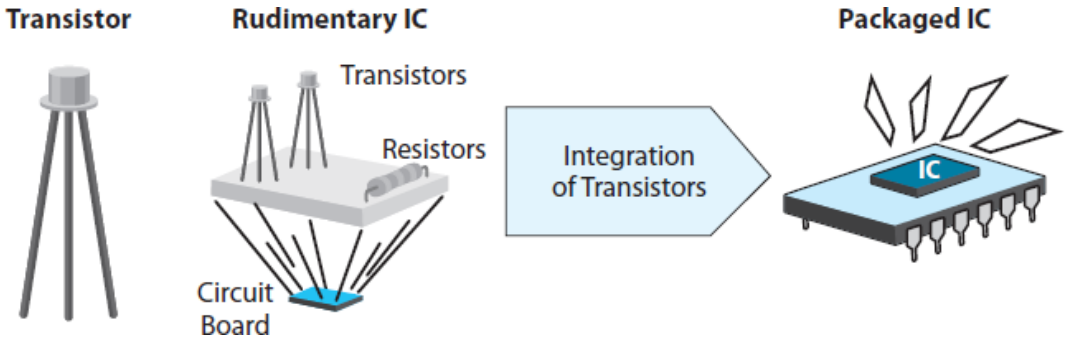


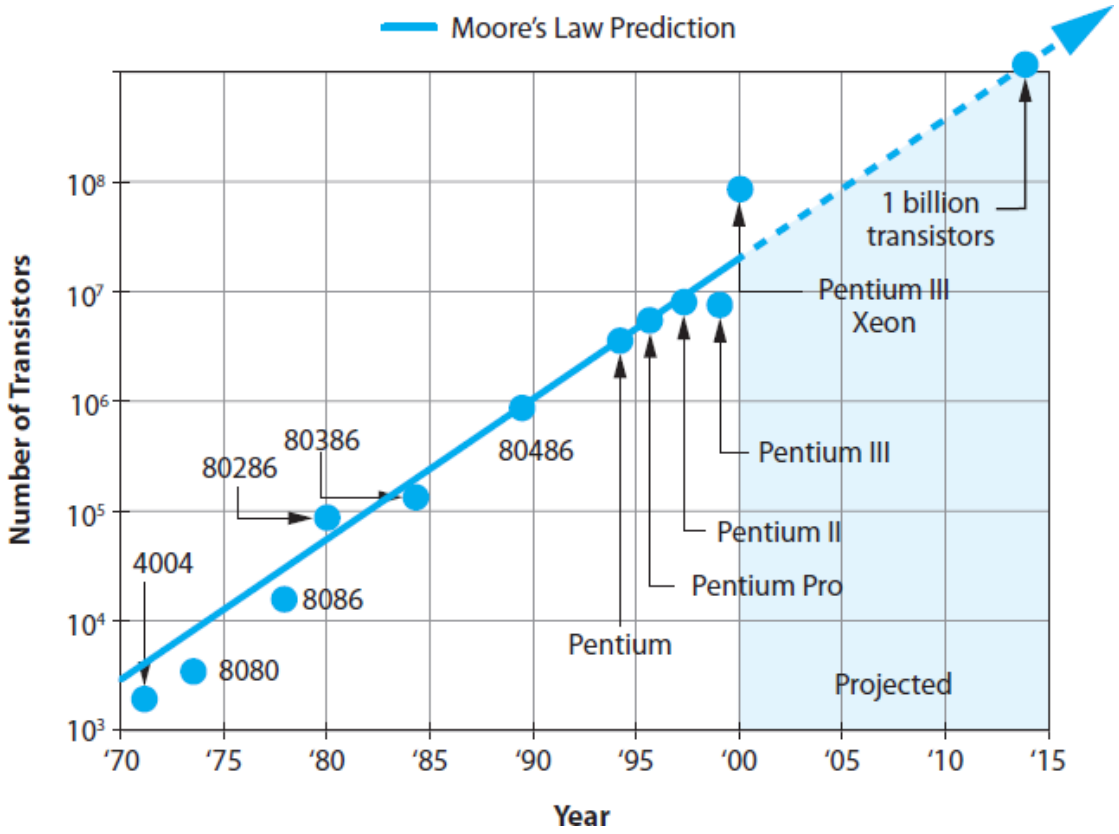
Wire-Bond → Organic Flip-Chip



Technology Waves

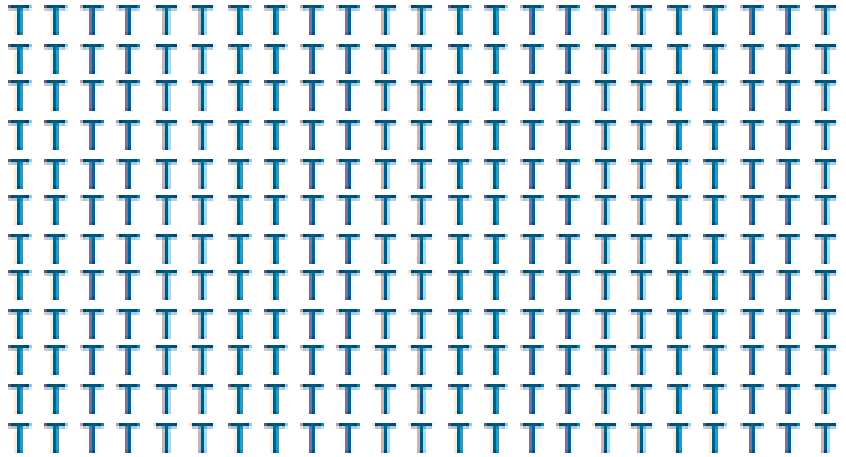
1. Microelectronics
2. RF and Wireless
3. Photonics
4. Micro-electro-mechanical Systems (MEMS)
5. Quantum





Moore's Law

Moore's Law for ICs

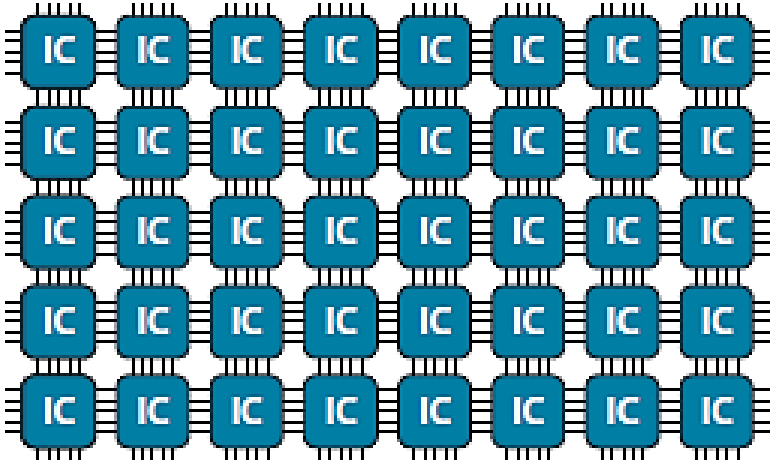


Large IC

Largest IC with smallest transistors at low performance and high cost

- 5-30 Billion transistors
- 30-50 miles of wiring
- Low transistor performance
- High RC interconnect delays
- High design and manufacturing cost

Moore's Law for Packaging

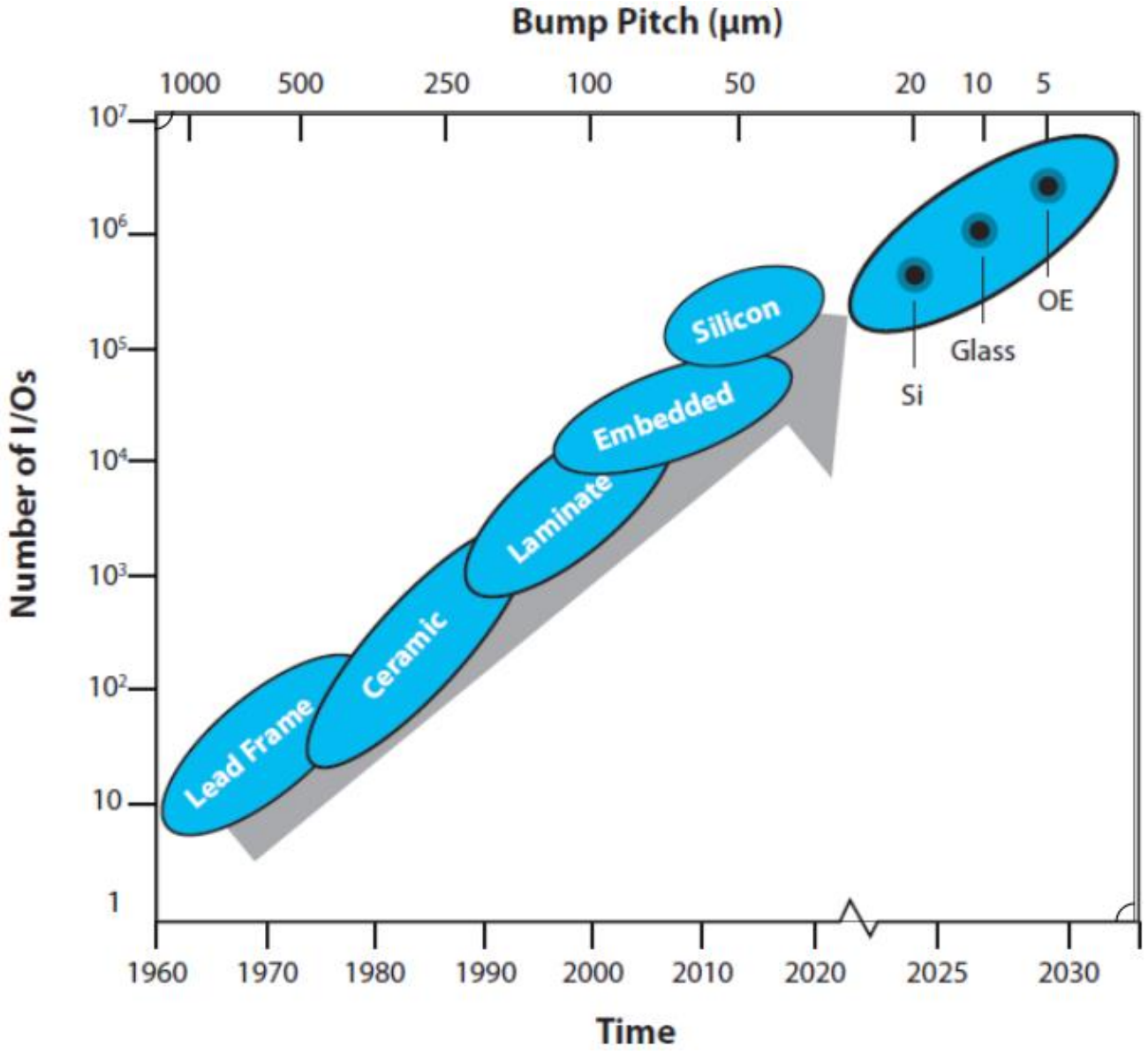


Large Package

Large package with small ICs with transistors and interconnects at high performance and low cost

- 5-30 Billion transistors
- <30 miles of wiring
- High transistor performance
- Low RC interconnect delays
- Low design and manufacturing cost

Moore's Law for Packaging: Number of I/Os



Why Take a Class on Electronics Packaging?

- Growing demand for well-trained packaging engineers

- Most packaging engineers in industry are self-taught, acquiring experience on the job
  - As a result, most books/textbooks are authored by industry professionals
  - Strong focus on application and technologies and less on theory

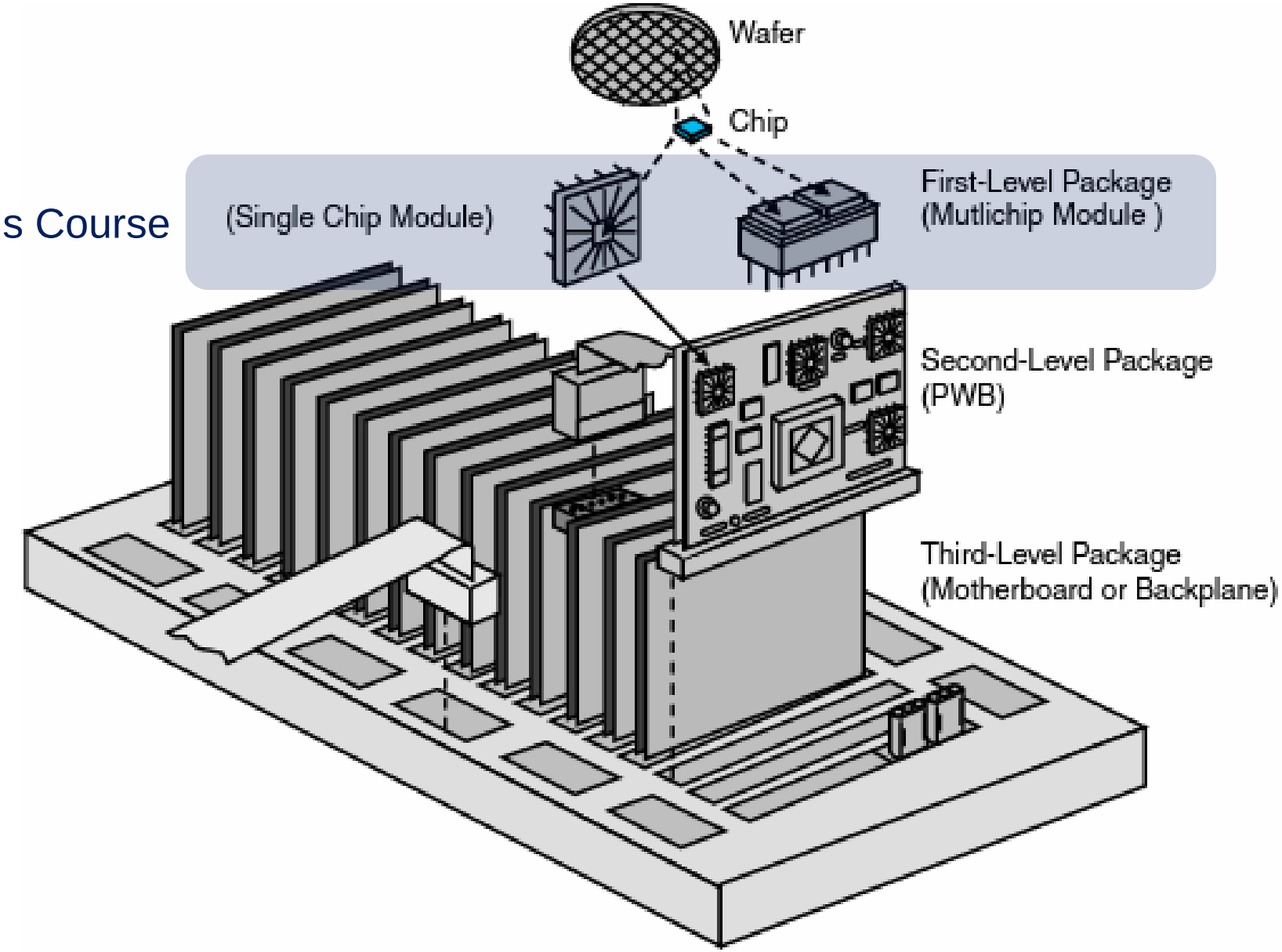
- Understand electrical-thermal-mechanical trade-offs

Companies with Electronics Packaging

- IBM
- Intel
- TSMC
- GlobalFoundries
- HP
- ASE
- Amkor
- Kyocera
- Samsung
- Motorola
- Nokia
- ON Semiconductor
- Texas Instruments
- STMicroelectronics
- Cree / Wolfspeed
- Infineon
- Mitsubishi
- Hitachi
- General Electric
- Raytheon Technologies
- Lockheed Martin
- BAE Systems
- BorgWarner
- …

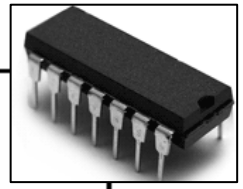
Packaging Levels

This Course

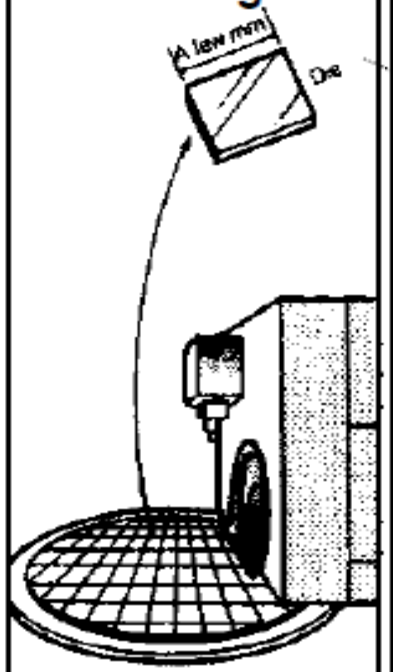


Example of Level 1 Packaging

Dual In-Line (DIP)

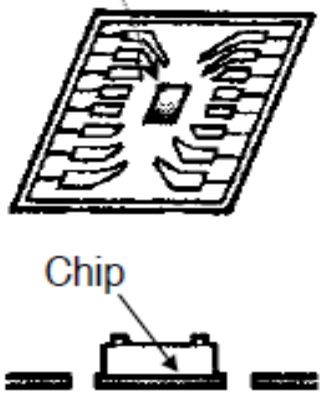


Dicing



The wafer is separated into chips by a diamond grind-stone. A fully automatic dic-ing saw is used for dicing.

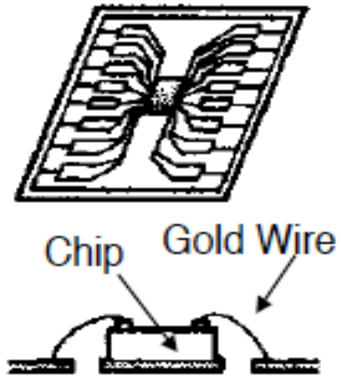
Die Bonding



The separated IC chip (die) is bonded into the center of a lead frame or package.

Wire Bonding

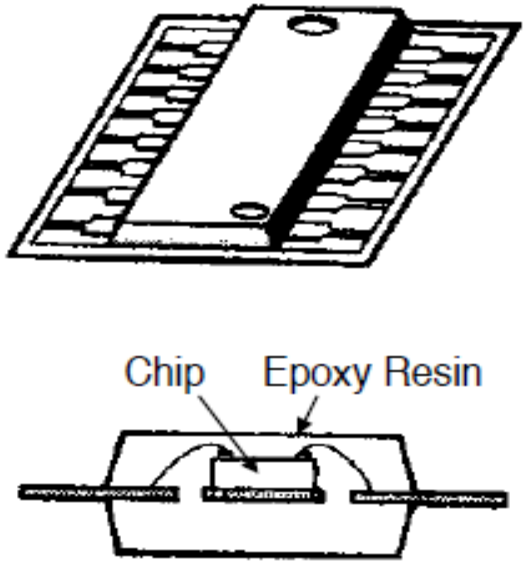
(Interconnection)



The pads on the IC chip and adjoining terminals on the lead frame are connected, one-by-one, with gold wire.

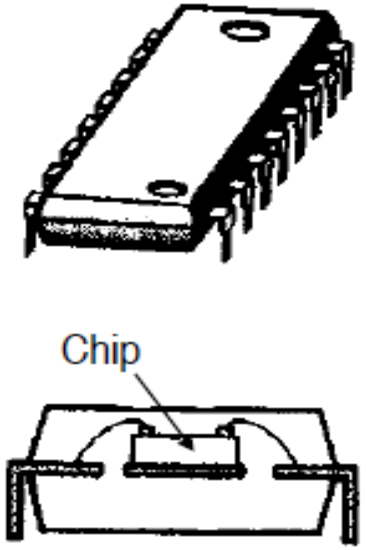
Molding

(encapsulation)



The chip is sealed with a macro-molecule plastic, like epoxy resin, thus finishing the plastic package container.

Forming & Marking



The lead frame is cut, and leads are bent thus forming the package. The manufacturer's name and model number are stamped on top.

Package Components

Component	Description/Purpose	Examples
Chip (die, device, semiconductor)	Device being packaged	IC, transistor, diode
Die attach	Bonds the chip to the substrate	Solder (paste, preform, ball), conductive epoxy
Substrate (chip carrier)	Mechanical foundation and electrical routing/wiring	Laminate, ceramic
Interconnect	Forms electrical connections within the package	Wire bonds, solder balls
Encapsulation (molding)	Protects the chip(s) and package	Epoxy, silicone gel
Terminals	Provides electrical connection to the next level	Lead frame, pins, solder balls, screws