Group Project

Due Friday, May 2nd, by 11:59pm

In this group project, your team will design and analyze a package for a gallium nitride (GaN) power high-electron-mobility transistor (HEMT). You must complete all aspects of the project within your team. The Virginia Tech honor code pledge for assignments is as follows: "I have neither given nor received unauthorized assistance on this assignment." The honor pledge represents both an expression of the student's support of the honor code and a commitment to uphold the academic standards at Virginia Tech. Please see the Honor System section of the syllabus on Canvas for details. By submitting your report, you accept the honor code pledge.

Each team will submit one typed report as a PDF to Canvas and the final Q3D and LTspice simulation files. The report should follow the guidelines on the last page of this document. The report should be concise, and include relevant information and sound reasoning to support the selections, methods, and results. Detailed calculations, data sheets, and other work that would interrupt the flow of the report should be put in the appendices rather than in the body of the report. The grading guidelines are provided at the end of this document. At the end of the project report, each team member must have a brief statement of their personal contributions to the project and report. Each team member must also submit a peer evaluation form (this will be submitted through a separate, individual assignment on Canvas).

All team members will get the same grade for the project, unless there are extenuating circumstances (e.g., a team member does not sufficiently contribute to the project or report). If a team member is unresponsive, late on their assigned tasks, or if other issues that are impeding the project progress occur, then the other team members should contact the instructor (before the submission deadline). All team members are responsible for what is submitted in the report; individual grades will not be assigned (e.g., a student that worked on a section that got full marks will not get a higher grade than a student that worked on a section that got fewer marks). It is expected that team members check over sections done by others and provide feedback or make revisions as needed. Further, packaging is an iterative process (e.g., if it is determined that the thermal performance of the designed package is not sufficient, then the design should be modified accordingly), so it is expected that the team members are working together to understand how the package design and materials selections impact the electrical and thermal performance metrics and that they are revising accordingly.

No late reports will be accepted, unless approved by the instructor prior to the due date.

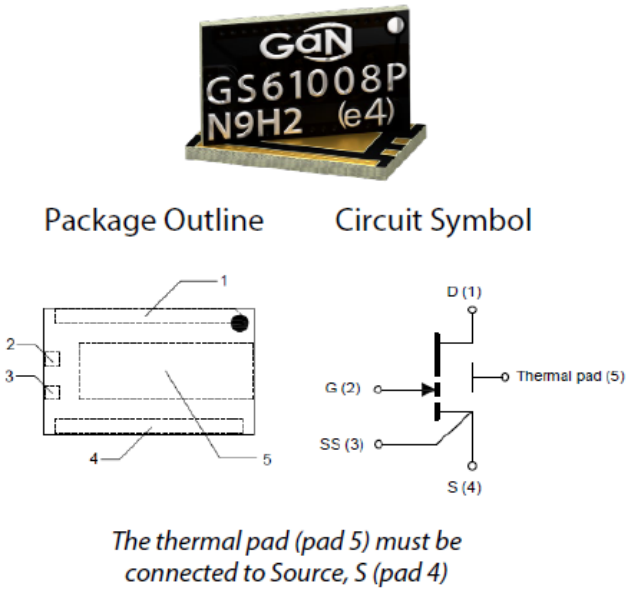

Figure 1: GS61008P 100-V enhancement mode GaN HEMT in a GaNPX® package [1].

I. Overview

A 100 V power GaN high-electron-mobility transistor (HEMT) in a GaNPX® package (**Figure 1**) can be used in a number of applications, such as data centers and automotive. The specifications for the selected GaN HEMT can be found in the technical data sheet and the 3D model for this package can be found on the manufacturer website [1]. Assume that the GaN die is 6 mm x 2 mm x 0.3 mm.

A. Project Objectives

- To review the literature to understand the package, its specifications, and its operation
- To select the materials and processes for package components
- To analyze the electrical and thermal performance of the package
- To evaluate different soldering and wire bonding profiles in the CPES packaging laboratory

B. Application Background

To meet the growing power demands of cloud and artificial intelligence (AI) computing, server rack architectures are moving from 12 V to 48 V [2]. Increasing the voltage enables higher power while maintaining high efficiency. This move requires 48 V to 12 V power converters to support the legacy 12 V backplanes and voltage regulators. The power demands of electric and hybrid-electric vehicles are also increasing, resulting in a potential shift to a 48-V network to improve performance. Similar to the server case, 48 V to 12 V power converters are needed to support legacy 12 V loads [3].

II. Literature Review

Review the technical data sheet and application notes on the GaN HEMT manufacturer's website [1] to understand the package layout and specifications, and search the literature to understand the usage of this package for server and automotive (or other) applications and the critical requirements of these applications (e.g., reliability, efficiency, power density, cost, etc.).

Provide a brief summary of the package and key specifications. In your own words, briefly summarize how this package could be used in server and EV (or other) applications. Select one of these two applications to focus on for this project. Provide a more detailed explanation of how this package could be beneficial for the selected application, what the critical requirements are for that application, and how these requirements translate to specifications for the package. Cite key references used.

III. Design

Identify/select materials, manufacturing processes, and dimensions for components in the package. These components include the conductor, insulator, plating, die attach, and gate, source, and drain interconnects. In making your selections, you should consider the requirements for the package (determined in Part II) and compatibility of the components to one another. The outer package dimensions and footprint (pad layout) should not change; only the internal structure is being designed.

You should identify a suitable material for the GaN HEMT die pads (i.e., for the gate, drain, and source pads of the die) that is compatible with the interconnects and die attach that you select; you do not need to provide information on the process for plating the GaN HEMT pads (we can assume this plating is done during the GaN HEMT fabrication and is not the responsibility of the packaging engineer).

This type of package uses vias for the interconnects. You should select the via diameter, quantity, and spacing. The selected interconnect for the source must be able to conduct at least 80 A. Create a 3D model of the final package (you may modify the one provided on the manufacturer website [1]). Include a figure of the 3D rendering in the report; ensure the interconnects are visible.

Summarize your material and process selections for each of the components in a table(s). Provide key properties, specifications, and/or conditions for the respective components, and justification for each of these selections. Explain how these selections relate to the specifications for the package that were determined in part II by the application requirements and the MOSFET data sheet. Cite references and use sound reasoning to support your selections and justifications.

IV. Electrical Analysis

Use ANSYS Q3D Extractor to simulate the parasitic DC inductance of the power loop (from the drain to the source) and gate loop (from the gate to the Kelvin source (labeled SS in **Figure 1**)) of the package. This package has an additional connection to the source (called a Kelvin connection), which is used as the reference potential for the gate driving voltage for the device. The Kelvin connection enables faster switching (and thus lower switching losses) as it decouples the driving

signal and power paths thereby reducing the impact of voltage variation from the parasitic source inductance on the gate driving voltage [4].

Also simulate the DC for the gate, kelvin source (SS), source, and drain paths of the package. Explain and use figures to show how you performed the simulation (i.e., where the nets, sources, and sinks were placed and why). Use tables to show your results.

Export the DC inductance and DC resistance from Q3D and place the equivalent circuit in the LTspice schematic provided on Canvas. The LTspice schematic includes a buck converter with a 48 V input, 12 V output, 750 W power, and 200 kHz switching frequency. You should import the GaN HEMT LTspice model provided by the manufacturer [1]. Use the model labeled "L1". Connect the GaN HEMT model and ANSYS Q3D equivalent circuit to the converter and run the simulation.

Show the schematic (label it appropriately so that the connections can be clearly understood) and waveforms (drain-source voltage, gate-source voltage, and drain current at the GaN HEMT model terminals, as well as the output voltage and current). Measure the voltage overshoot and ringing frequency in the GaN HEMT drain-source voltage, gate-source voltage, and drain current waveforms. Measure the loss in the GaN HEMT. The loss can be measured in LTspice by running the simulation, and then holding down the Alt key and clicking on the device model (a thermometer symbol will show up when hovering over the device model). A new waveform will appear that shows the device power loss. Change the waveform window to show 10 switching cycles during steady state, then hold the Ctrl key and click on the power loss waveform title (an equation with voltage and current being multiplied). A window will pop up with the average loss. Vary the gate resistance in the schematic. How does this impact the waveforms and GaN HEMT loss? Select an optimal gate resistance and justify your selection.

Use tables to list the key values measured in the simulations. Explain how the simulation was set up and provide an analysis of the simulation results.

V. Thermal Analysis

Calculate the junction-to-case thermal resistance ($R_{thj\text{-}c}$) through the top and bottom of the package. Show the key equations, dimensions, and material properties used for these calculations and provide a brief explanation of the calculations and any assumptions made. Do not put the detailed calculations in the body of the report. The detailed calculations should go in the appendix. Put the thermal resistances for each layer into a table. Include the $R_{thj\text{-}c}$ values provided in the data sheet.

This package is meant to be soldered to a PCB. Design the PCB and thermal management needed to ensure the junction temperature of the high-side MOSFET does not exceed the maximum (150°C). Use the MOSFET average power loss determined in part IV. Assume forced air at 25°C is available for cooling the package. Use standard PCB layer stackups and thicknesses. These can be found on PCB manufacturer websites [5],[6].

Explain your design process and final PCB and thermal management design. Use figures to show your designs and tables to list key dimensions and properties. Use calculation and/or simulation to verify that your design has met the target specification. Cite key references used.

VI. Experimental Evaluation

This part of the project is separate from the others and is not related to the package shown in **Figure 1**. A lab procedure document and sign-up sheet will be provided on Canvas. At least two team members must participate in the hands-on lab session.

Wire Bonding

Use the HB30 wire bonder in the CPES packaging laboratory to wedge bond 10-mil aluminum wire on a substrate. The substrate and wire bonder settings will be provided in the lab. Two different profile settings will be evaluated. Make at least 5 wire bonds per profile. Measure the bond strength of each wire bond using the wire bond pull tester in the lab.

Briefly explain the wedge wire bonding process, the profile settings used, and the results. Use figures and tables to show the results. Cite key references used.

Review the MIL-STD-883 method 2011.9 on wire bond pull testing [7]. Identify the minimum bond pull limit for 10 mil aluminum wire. Indicate which of the wire bonds and profiles met this minimum requirement and identify the failure categories.

Soldering

Use the solder reflow belt to solder semiconductor dies to substrates. The dies, substrates, solder paste, and profiles will be provided in the lab. After cleaning the components, you will use a squeegee and stencil to stencil-print the paste onto the substrate, then place the die onto the printed paste and put it on the solder reflow belt. Two different reflow profiles will be evaluated. Solder at least 2 dies per profile. Measure the bond strength of each soldered die using the shear tester in the lab.

Briefly explain the soldering process, the profiles used, and the results. Use figures and tables to show the results. Cite key references used.

Review the MIL-STD-883 method 2019.9 on die shear testing [8]. Identify the minimum force in kilograms for the bonded die. Indicate which of the samples met this minimum requirement and identify the separation categories.

References

[1] GaN Systems, GS61008P 100V Enhancement Mode GaN Transistor, 80 V, BSC021N08NS5, https://gansystems.com/gan-transistors/gs61008p/

[2] M. D. P. Emilio, “48-V power architecture supports next-generation AI processors,” Power Electronics News, 2021, https://www.powerelectronicsnews.com/48-v-power-architecture-supports-next-generation-ai-processors/

[3] M. D. P. Emilio, “Electric vehicles: 48V is the new 12V,” Power Electronics News, 2020, https://www.powerelectronicsnews.com/electric-vehicles-48v-is-the-new-12v/

[4] F. Stueckler, E. Vecino, “CoolMOSTM C7 650V Switch in a Kelvin Source Configuration,” Application Note AN 2013-05, V1.0, May 2013. https://www.infineon.com/dgdl/Infineon+-

+Application+Note+-+TO-247-4pin+-+650V+CoolMOS+C7+Switch+in+a+Kelvin+Source+Configuration.pdf?fileId=db3a30433e5a5024013e6a9908a26410

[5] Advanced Circuits, Multi-Layer PCB Stackup: .062 Finished Thickness, https://www.4pcb.com/pcb-stack-ups-0.062.html

[6] PCBcart, Layer Stackup, https://www.pcbcart.com/pcb-capability/layer-stackup.html

[7] xyztec, MIL-STD-883 method 2011.9 – Bond strength (destructive bond pull test), https://www.xyztec.com/knowledgecenter/guidelines/mil-std-883-method-2011-9-bond-strength-destructive-bond-pull-test/

[8] xyztec, MIL-STD-883 method 2019.9 – Die shear strength, https://www.xyztec.com/knowledgecenter/guidelines/mil-std-883-method-2019-9-die-shear-strength/

Grading

Technical: 85%

- Correctness and clarity of the approach, assumptions, results, explanations, and analyses
- Usage and explanation of figures, tables, and equations to convey the work and results
- Use of references to support the claims, assumptions, explanations, and analyses
- Completeness of explanations and analyses

Grammar and Style: 15%

- Grammar, spelling, and vocabulary
- Structure and organization
- Visual appearance and referencing of report, figures, tables, and equations

Project Report Guideline

The report should be concise, contain sound reasoning, justifications, and analyses, and sufficiently document the work done. Use the template provided on Canvas; follow the formatting instructions provided in the template. The report should include the following:

Abstract

I. Introduction

- Overview of the project, background, literature review, and summary of the content of the report.

II. Package Design

III. Electrical Analysis

IV. Thermal Analysis

V. Experimental Evaluation

VI. Summary and Conclusion

- Summary of the design and key results, and conclusions.

Appendix

- Any material that could help in understanding the details of your analysis or results, but which would obstruct the flow of the main report (e.g., calculations, derivations, simulation details, datasheets, etc.).

References

Biographies

- Brief biography of each team member.
- Brief (1-3 sentences) overview of each member's contributions to the project and report.