Assignment 1 Report
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Steps for 4-Bit Counter: It is obvious that since the requirement is a 4-bit counter, we require 4 D flip-flops. First, we place a pin to represent the clock input into D1 as input. We then link the 4 flip-flops by taking the complement output from one and feeding it into the next flip-flops Clock input. For example: D1 gives Q' to D2, D2 gives Q' to D3, and so on. We also take the complement output and feed it back into the Data slot of itself. For example: D1 gives Q' to D1, D2 gives Q' to D2, and so on. Coming out of each of the flip-flops Q output we give to a separate output pin to represent where we will feed info into the controller. We also take the Q outputs of D2, D3, D4 as we wish to reset the counter at 14, which in binary is 1110. These three inputs feed into the Counter Reset module which we will now discuss. It is worth noting that this module outputs one and only one wire into all four D flip-flops in its Clear pin. Then when the counter reaches 1110, all flip flops are reset to 0000. Below is the truth table, for which we will include the reset module as it is simplistic in nature. LET US SAY THAT D1=W, D2=X, D3=Y, D4=Z.

W	X	Y	Z	RESET	COUNT (REVERSED BINARY)	RESET-OUTPUT	X AND Y	(X AND Y) AND Z
0	0	0	0	0	0	0	0	0
1	0	0	0	0	1000	0	0	0
0	1	0	0	0	0100	0	0	0
1	1	0	0	0	1100	0	0	0
0	0	1	0	0	0010	0	0	0
1	0	1	0	0	1010	0	0	0
0	1	1	0	0	0110	0	1	0
1	1	1	0	0	1110	0	1	0
0	0	0	1	0	0001	0	0	0
1	0	0	1	0	1001	0	0	0
0	1	0	1	0	0101	0	0	0
1	1	0	1	0	1101	0	0	0
0	0	1	1	0	0011	0	0	0
1	0	1	1	0	1011	0	0	0
0	1	1	1	1	0111	1	1	1

Let us digress for a moment and talk about the construction of the controller as it will ease the explanation of the controller's truth table.

Steps for Controller:

The controller takes the PIN-OUTPUT from above as 4-bit input and puts it into a 4-bit decoder. This includes NOT as well as AND gates. The pattern for ANDing each of the inputs (So we know which signal to let through) is by having the AND gates set up ascending from left to right, starting with 1 being 1000 (Yes each of the binary values are reversed), and stopping at 13 being 1011. There is no need to include 0, 2, or 12 here since we never do anything with those outputs. This is to save circuit space. We then take all 11 outputs from the AND gates and we put them through 5 OR gates which represent each of the states of the DFA. These are connected per the rules of the assignment. The OR gates produce 5 outputs, which in the main circuit link to the LEDs of the lights. Here is the truth table for the Controller.

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COUNT	AND 1	AND 3	AND 4	AND 5	AND 6	AND 7	AND 8	AND 9	AND 10	AND 11	AND 13	STATE 1	STATE 2	STATE 3	STATE 4	STATE 5
0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1000	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0100	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1100	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0
0010	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0
1010	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0
0110	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0
1110	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0
0001	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0
1001	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1
0101	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1
1101	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1
0011	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1011	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Boolean Functions:

ALL COUNTS = W’X’Y’Z’ + WX’Y’Z’ + W’XY’Z’ + WXY’Z’ +W’X’YZ’ + WX’YZ’ + W’XYZ’ + WXYZ’ + W’X’Y’Z + WX’Y’Z + W’XY’Z + WXY’Z + W’X’YZ + WX’YZ

W’(X’Y’Z’ + XY’Z’ + X’YZ’ + XYZ’ + X’Y’Z + XY’Z + X’YZ) + W(X’Y’Z’ + XY’Z’ + X’YZ’ + XYZ’ + X’Y’Z + XY’Z + X’YZ)

It is obvious there are no ways to simplify this down, as we would just continue to divide the equation into smaller parts, but with no way to eliminate terms. Let us move on,

RESET MODULE = W’XYZ → This is as simple as it gets.

AND 1 = WX’Y’Z’

AND 3 = W’XY’Z’

AND 4 = WXY’Z’

AND 5 = WX’YZ’

AND 6 = W’XYZ’

AND 7 = WXYZ’

AND 8 = W’X’Y’Z

AND 9 = WX’Y’Z

AND 10 = W’XY’Z

AND 11 = WXY’Z

AND 13 = WX’YZ

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STATE 1 = WX'Y'Z' + W'XY'Z' + WXY'Z' + W'X'YZ' + WX'YZ' + W'XYZ' + WXYZ' + W'X'Y'Z + WX'Y'Z + W'XY'Z + WXY'Z + W'X'YZ + WX'YZ

SIMPLIFICATION FOR STATE 1:

W (X'Y'Z' + XY'Z' + X'YZ' + XYZ' + X'Y'Z + XY'Z + X'YZ) + W' (XY'Z + X'YZ' + XYZ' +X'Y'Z + XY'Z + X'YZ)

W (X' (Y'Z' + YZ' + Y'Z + YZ) + XY'Z' + XYZ' + XY'Z) + W' (X' (YZ' + Y'Z + YZ) + XY'Z + XYZ' + XY'Z))

W (X' (Y' (Z' + Z) + Y (Z' + Z)) + X (Y'Z' + YZ' + Y'Z)) + W' (X' (Y (Z' + Z) + Y'Z) + X (Y'Z + YZ' + Y'Z))

W (X' (Y' (1) + Y (1)) + X (Y' (Z' + Z) + YZ')) + W' (X' (Y (1) + Y'Z) + X (Y'Z + YZ')))

W (X' (Y' + Y) + X (Y' + YZ')) + W' (X' (Y + Y'Z) + X (Y $\oplus$ Z))

W (X' + X (Y' + YZ')) + W' (X' (Y + Y'Z) + X (Y $\oplus$ Z))

This appears to be the simplest reduction of STATE 1.

STATE 2 = WXY'Z' + W'X'YZ + WXY'Z + WX'YZ

SIMPLIFICATION FOR STATE 2:

W (XY'Z' +XY'Z + X'YZ) + W'X'YZ

W (Z (XY' + X'Y) + XY'Z') + W'X'YZ

W (Z (X $\oplus$ Y) + XY'Z') + W'X'YZ

WZ(X $\oplus$ Y) + XY'Z' + W'X'YZ

This is the simplest reduction for STATE 2

STATE 3 = WX'YZ' + W'XYZ' + WXY'Z + WX'YZ

SIMPLIFICATION FOR STATE 3:

W (X'YZ' + XY'Z + X'YZ) + W'XYZ'

W (Z (XY' + X'Y) + X'YZ') + W'XYZ'

W (Z (X $\oplus$ Y) + X'YZ') + W'XYZ'

WZ(X $\oplus$ Y) + X'YZ' + W'XYZ'

This is the simplest reduction for STATE 3

STATE 4 = WXYZ' + W'X'Y'Z + WXY'Z + WX'YZ

SIMPLIFICATION FOR STATE 4:

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W (XYZ’ + XY’Z + X’YZ) + W’X’Y’Z

W (X (YZ’ + Y’Z) + X’YZ) + W’X’Y’Z

W (X (Y ⊕ Z) + X’YZ) + W’X’Y’Z

WX(Y ⊕ Z) + X’YZ + W’X’Y’Z

This is the simplest reduction for STATE 4

STATE 5 = WX’Y’Z + W’XY’Z + WXY’Z + WX’YZ

SIMPLIFICATION FOR STATE 5:

W (X’Y’Z + XY’Z + X’YZ) + W’XY’Z

W (Z (X’Y’ + XY’ + X’Y)) + W’XY’Z

W (Z (X’Y’ + (X ⊕ Y))) + W’XY’Z

WZ(X’Y’ + (X ⊕ Y)) + W’XY’Z

This is the simplest reduction for STATE 5

Now we will represent all of this using a DFA: