MERU UNIVERSITY OF SCIENCE AND TECHNOLOGY

SCHOOL OF ENGINEERING AN
ARCHITECTURE

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

BACHELOR OF TECHNOLOGY IN ELECTRICTRAL AND ELECTRONIS ENGINEERING

TITLE: LAB REPORT: Traffic Control System Simulation Using Intel 8085 Microprocessor (Assembly Language)

https://github.com/joshuamuthenya/microprocessors.git

NAME: JOSHUA MUTHENYA WAMBUA

REG NO: EG209/109705/22

UNIT CODE: 3400

DESCRIPTION: MICROPROCESSOR ARCHITECTURE AND INTERFACING

DATE:05/12/2025

Introduction

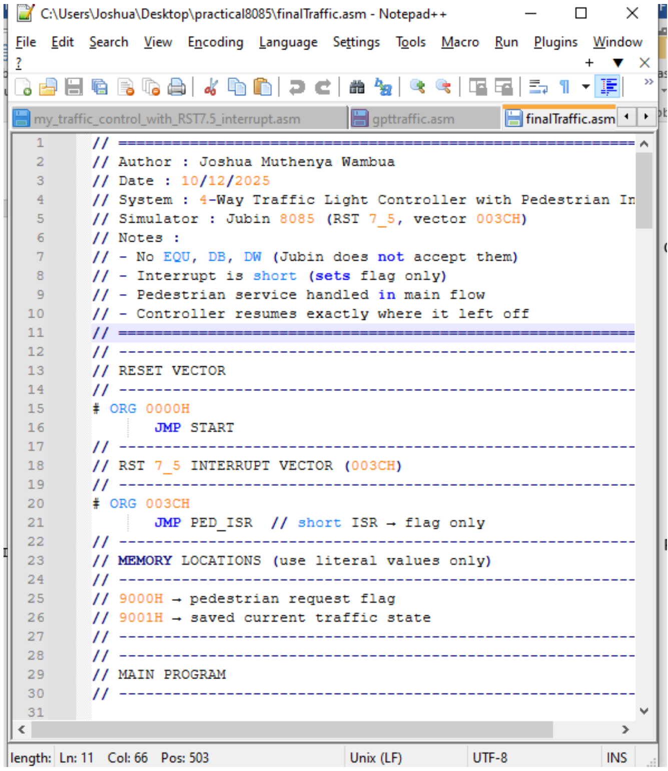
https://github.com/joshuamuthenya/microprocessors.git

Objectives

Softwares/Kits used.

Procedure

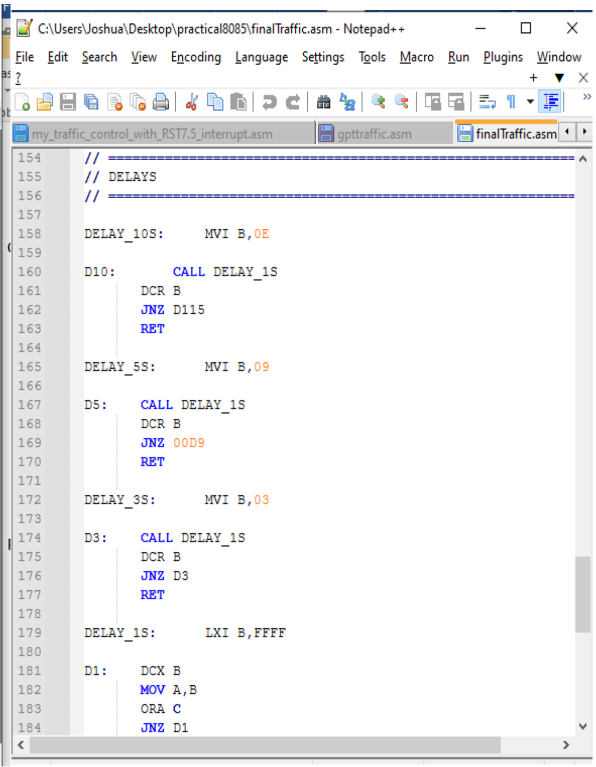
https://github.com/joshuamuthenya/microprocessors.git


C:\Users\Joshua\Desktop\practical8085\finalTraffic.asm - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
my_traffic_control_with_RST7.5_interrupt.asm
gpttraffic.asm
finalTraffic.asm

```
// ===========================================================
// Author : Joshua Muthenya Wambua
// Date : 10/12/2025
// System : 4-Way Traffic Light Controller with Pedestrian In
// Simulator : Jubin 8085 (RST 7_5, vector 003CH)
// Notes :
// - No EQU, DB, DW (Jubin does not accept them)
// - Interrupt is short (sets flag only)
// - Pedestrian service handled in main flow
// - Controller resumes exactly where it left off
// ===========================================================
// -----------------------------------------------------------
// RESET VECTOR
// -----------------------------------------------------------
# ORG 0000H
       JMP START
// -----------------------------------------------------------
// RST 7_5 INTERRUPT VECTOR (003CH)
// -----------------------------------------------------------
# ORG 003CH
       JMP PED_ISR  // short ISR → flag only
// -----------------------------------------------------------
// MEMORY LOCATIONS (use literal values only)
// -----------------------------------------------------------
// 9000H → pedestrian request flag
// 9001H → saved current traffic state
// -----------------------------------------------------------
// -----------------------------------------------------------
// MAIN PROGRAM
// -----------------------------------------------------------

```

length: Ln: 11 Col: 66 Pos: 503 Unix (LF) UTF-8 INS


C:\Users\Joshua\Desktop\practical8085\finalTraffic.asm - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
my_traffic_control_with_RST7.5_interrupt.asm
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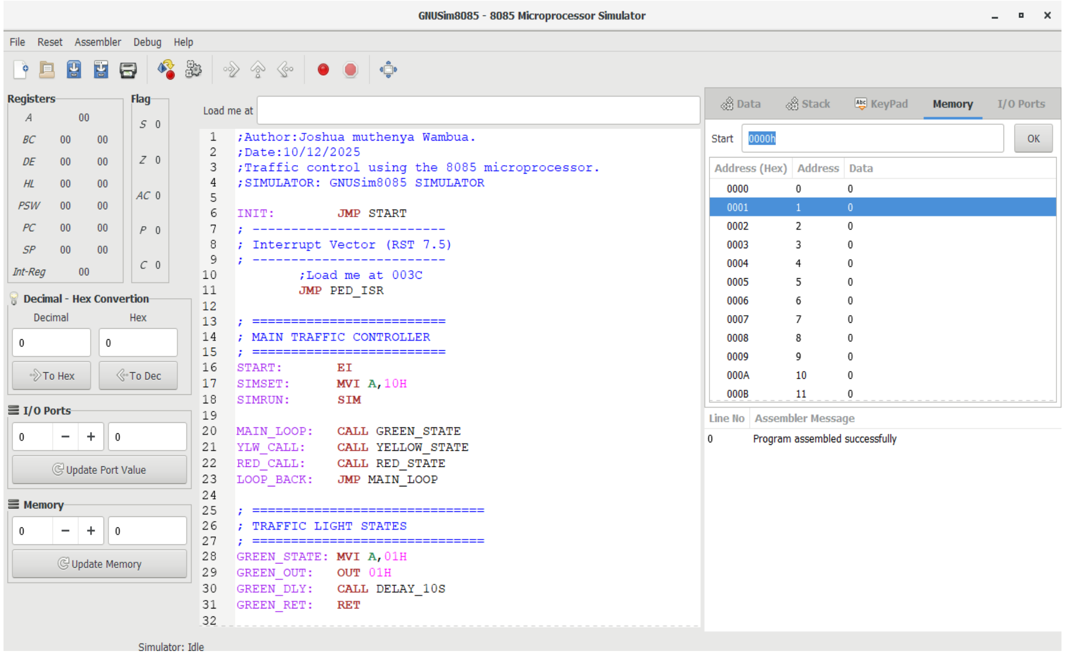
finalTraffic.asm

```
// ===========================================================
// DELAYS
// ===========================================================

DELAY_10S:     MVI B,0E

D10:        CALL DELAY_1S
       DCR B
       JNZ D115
       RET

DELAY_5S:      MVI B,09

D5:    CALL DELAY_1S
       DCR B
       JNZ 00D9
       RET

DELAY_3S:      MVI B,03

D3:    CALL DELAY_1S
       DCR B
       JNZ D3
       RET

DELAY_1S:      LXI B,FFFF

D1:    DCX B
       MOV A,B
       ORA C
       JNZ D1
```

Results



A	00	
BC	00	00
DE	00	00
HL	00	00
PSW	00	00
PC	00	00
SP	00	00
Int-Reg	00	

S	0
Z	0
AC	0
P	0
C	0

Decimal	Hex
0	0

I/O Ports: 0 | 0

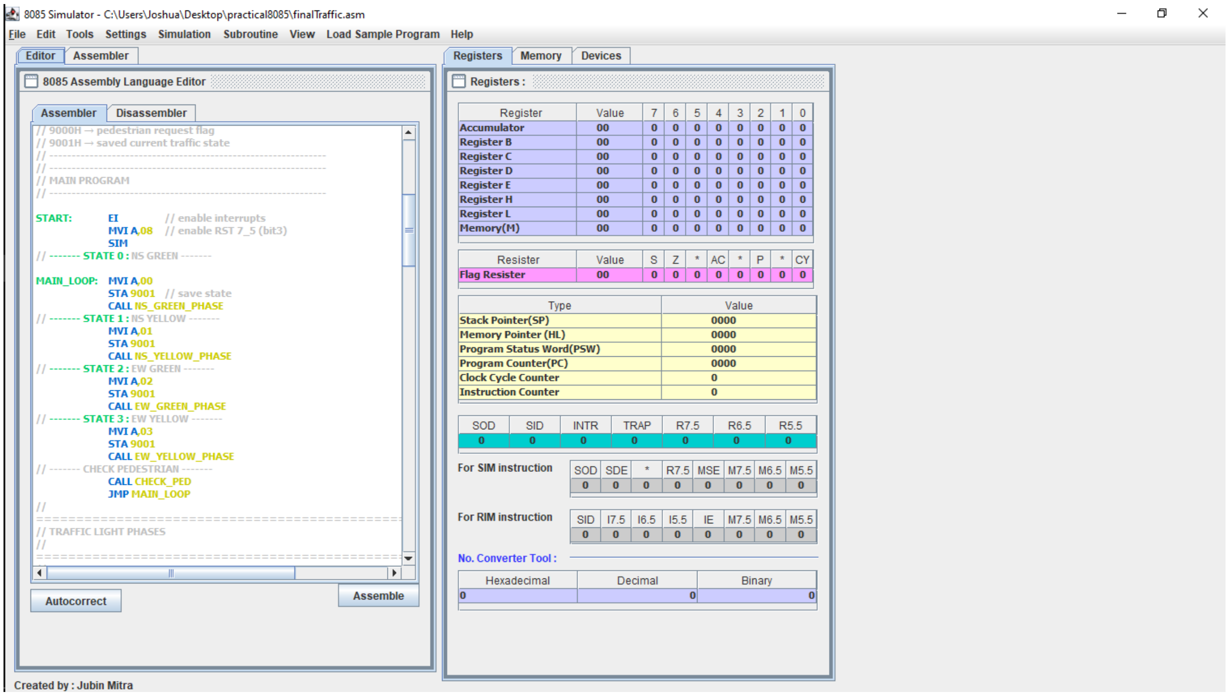
Memory: 0 | 0

```
;Author:Joshua muthenya Wambua.
;Date:10/12/2025
;Traffic control using the 8085 microprocessor.
;SIMULATOR: GNUSim8085 SIMULATOR

INIT:         JMP START
; ------------------------
; Interrupt Vector (RST 7.5)
; ------------------------
        ;Load me at 003C
        JMP PED_ISR

; ========================
; MAIN TRAFFIC CONTROLLER
; ========================
START:        EI
SIMSET:       MVI A,10H
SIMRUN:       SIM

MAIN_LOOP:    CALL GREEN_STATE
YLW_CALL:     CALL YELLOW_STATE
RED_CALL:     CALL RED_STATE
LOOP_BACK:    JMP MAIN_LOOP

; ==============================
; TRAFFIC LIGHT STATES
; ==============================
GREEN_STATE: MVI A,01H
GREEN_OUT:    OUT 01H
GREEN_DLY:    CALL DELAY_10S
GREEN_RET:    RET

```

Start 0000h

Address (Hex)	Address	Data
0000	0	0
0001	1	0
0002	2	0
0003	3	0
0004	4	0
0005	5	0
0006	6	0
0007	7	0
0008	8	0
0009	9	0
000A	10	0
000B	11	0

Line No	Assembler Message
0	Program assembled successfully



8085 Simulator - C:\Users\Joshua\Desktop\practical8085\finalTraffic.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
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Assembler
8085 Assembly Language Editor
Assembler
Disassembler
Autocorrect
Assemble
Registers
Memory
Devices
Registers :
Created by : Jubin Mitra

```
// 9000H → pedestrian request flag
// 9001H → saved current traffic state
// -----------------------------------------------------------
// -----------------------------------------------------------
// MAIN PROGRAM
// -----------------------------------------------------------

START:          EI            // enable interrupts
                MVI A,08      // enable RST 7_5 (bit3)
                SIM
// ------- STATE 0 : NS GREEN -------

MAIN_LOOP:      MVI A,00
                STA 9001     // save state
                CALL NS_GREEN_PHASE
// ------- STATE 1 : NS YELLOW -------
                MVI A,01
                STA 9001
                CALL NS_YELLOW_PHASE
// ------- STATE 2 : EW GREEN -------
                MVI A,02
                STA 9001
                CALL EW_GREEN_PHASE
// ------- STATE 3 : EW YELLOW -------
                MVI A,03
                STA 9001
                CALL EW_YELLOW_PHASE
// ------- CHECK PEDESTRIAN -------
                CALL CHECK_PED
                JMP MAIN_LOOP
//
==============================================================
// TRAFFIC LIGHT PHASES
//
==============================================================
```

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	0000
Clock Cycle Counter	0
Instruction Counter	0

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

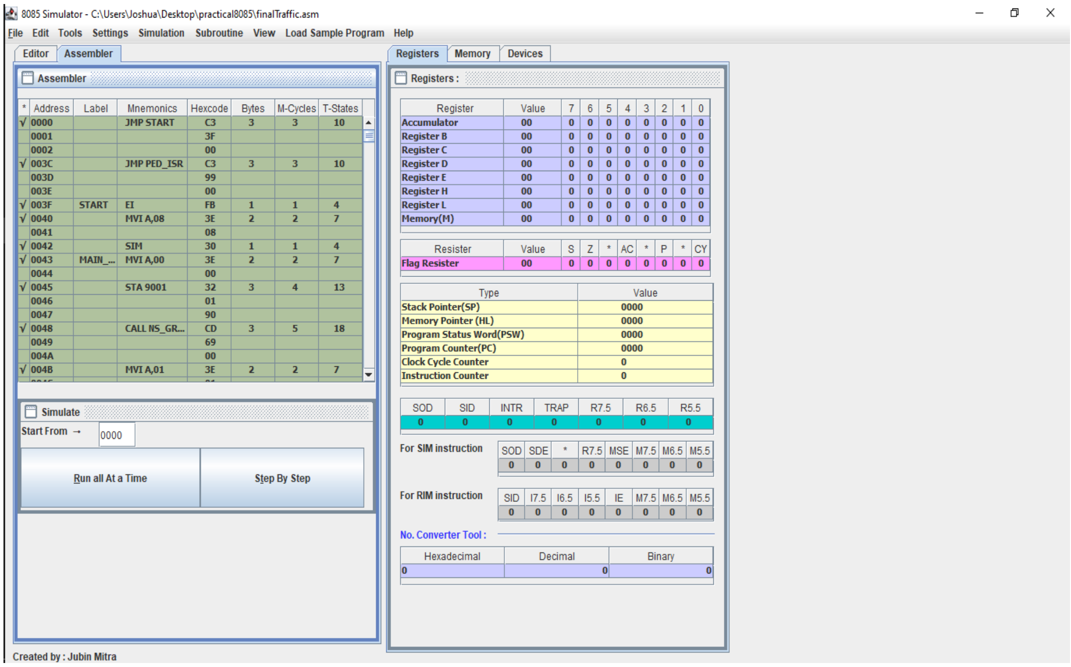
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



8085 Simulator - C:\Users\Joshua\Desktop\practical8085\finalTraffic.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
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Assembler
Simulate
Run all At a Time
Step By Step
Registers
Memory
Devices
Registers :
Created by : Jubin Mitra

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0000		JMP START	C3	3	3	10
	0001			3F			
	0002			00			
√	003C		JMP PED_ISR	C3	3	3	10
	003D			99			
	003E			00			
√	003F	START	EI	FB	1	1	4
√	0040		MVI A,08	3E	2	2	7
	0041			08			
√	0042		SIM	30	1	1	4
√	0043	MAIN_...	MVI A,00	3E	2	2	7
	0044			00			
√	0045		STA 9001	32	3	4	13
	0046			01			
	0047			90			
√	0048		CALL NS_GR...	CD	3	5	18
	0049			69			
	004A			00			
√	004B		MVI A,01	3E	2	2	7

Start From → 0000

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	0000
Clock Cycle Counter	0
Instruction Counter	0

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

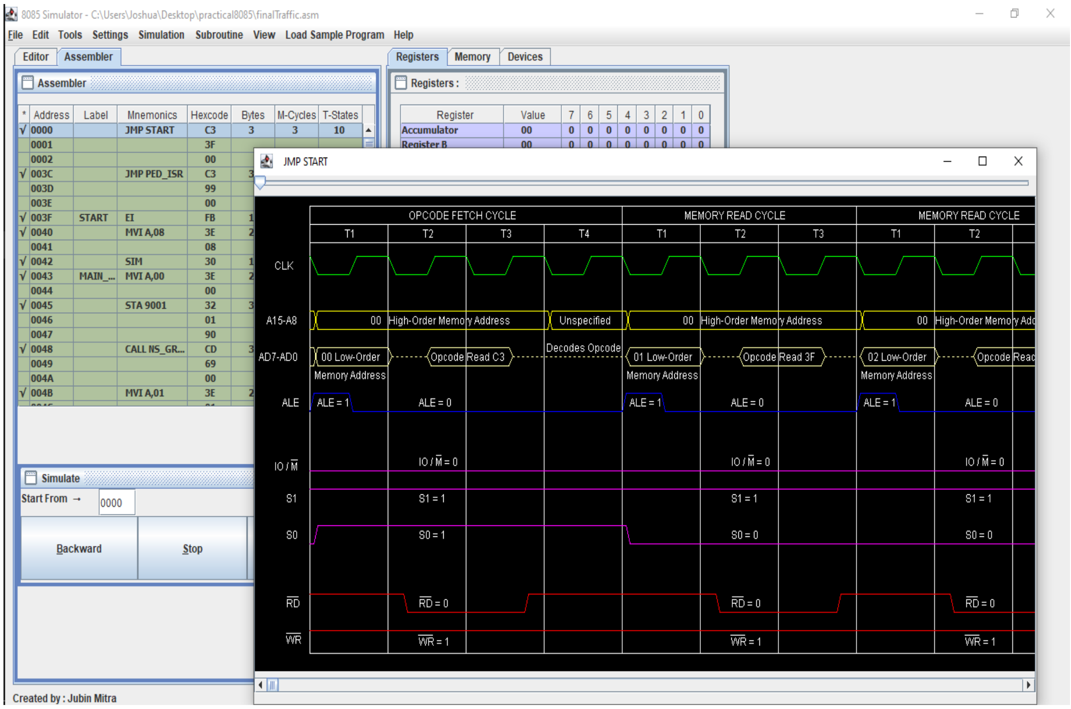
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



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Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0000		JMP START	C3	3	3	10
	0001			3F			
	0002			00			
√	003C		JMP PED_ISR	C3	3		
	003D			99			
	003E			00			
√	003F	START	EI	FB	1		
√	0040		MVI A,08	3E	2		
	0041			08			
√	0042		SIM	30	1		
√	0043	MAIN_...	MVI A,00	3E	2		
	0044			00			
√	0045		STA 9001	32	3		
	0046			01			
	0047			90			
√	0048		CALL NS_GR...	CD	3		
	0049			69			
	004A			00			
√	004B		MVI A,01	3E	2		

Registers :

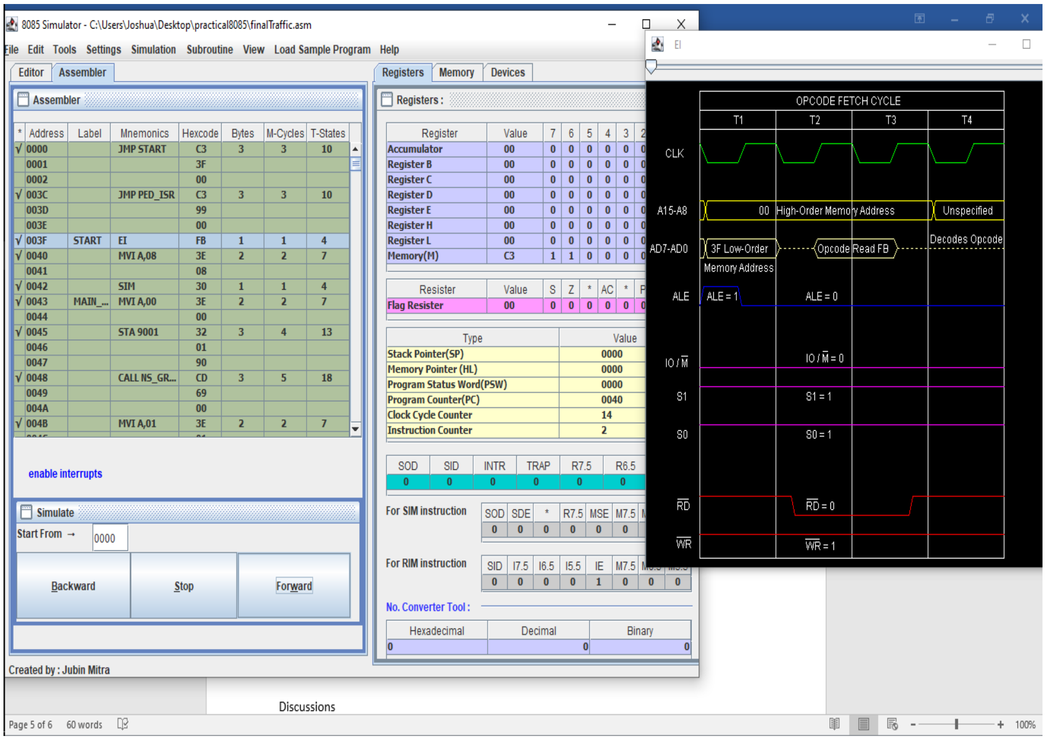
Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0

Simulate

Start From → 0000

Created by : Jubin Mitra

JMP START



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Memory
Devices

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0000		JMP START	C3	3	3	10
	0001			3F			
	0002			00			
√	003C		JMP PED_ISR	C3	3	3	10
	003D			99			
	003E			00			
√	003F	START	EI	FB	1	1	4
√	0040		MVI A,08	3E	2	2	7
	0041			08			
√	0042		SIM	30	1	1	4
√	0043	MAIN_...	MVI A,00	3E	2	2	7
	0044			00			
√	0045		STA 9001	32	3	4	13
	0046			01			
	0047			90			
√	0048		CALL NS_GR...	CD	3	5	18
	0049			69			
	004A			00			
√	004B		MVI A,01	3E	2	2	7

enable interrupts

Simulate

Start From → 0000

Created by : Jubin Mitra

Registers :

Register	Value	7	6	5	4	3	2
Accumulator	00	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0
Memory(M)	C3	1	1	0	0	0	0

Resister	Value	S	Z	*	AC	*	P
Flag Resister	00	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	0040
Clock Cycle Counter	14
Instruction Counter	2

SOD	SID	INTR	TRAP	R7.5	R6.5
0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5
0	0	0	0	0	0

For RIM instruction

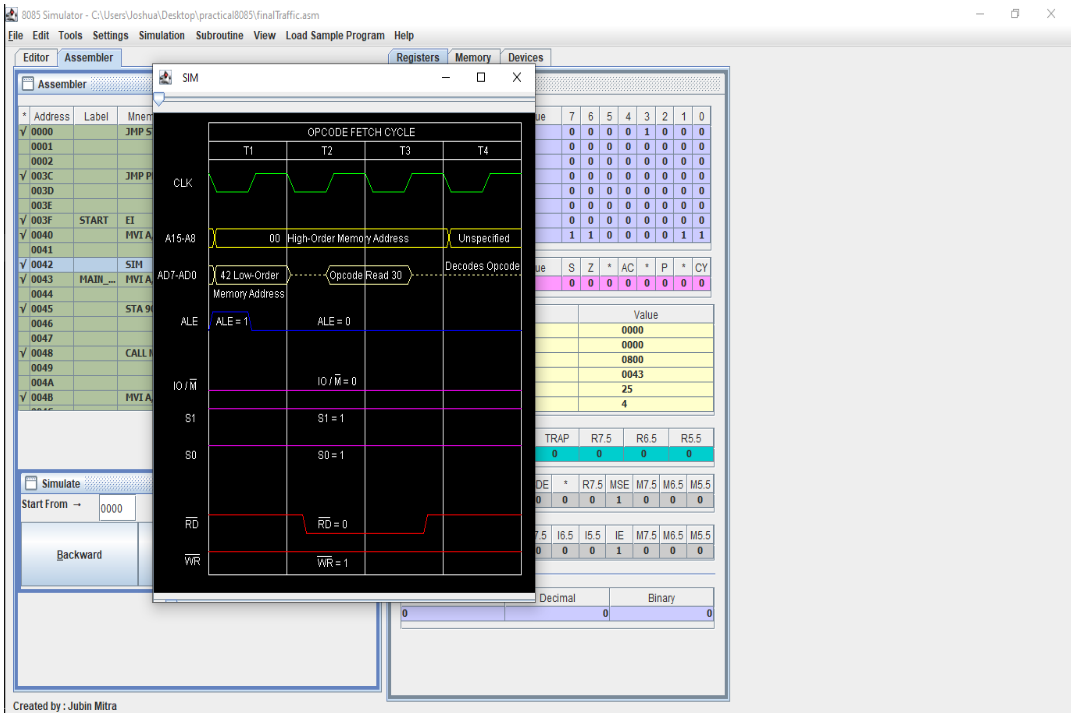
SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	1	0	0	0

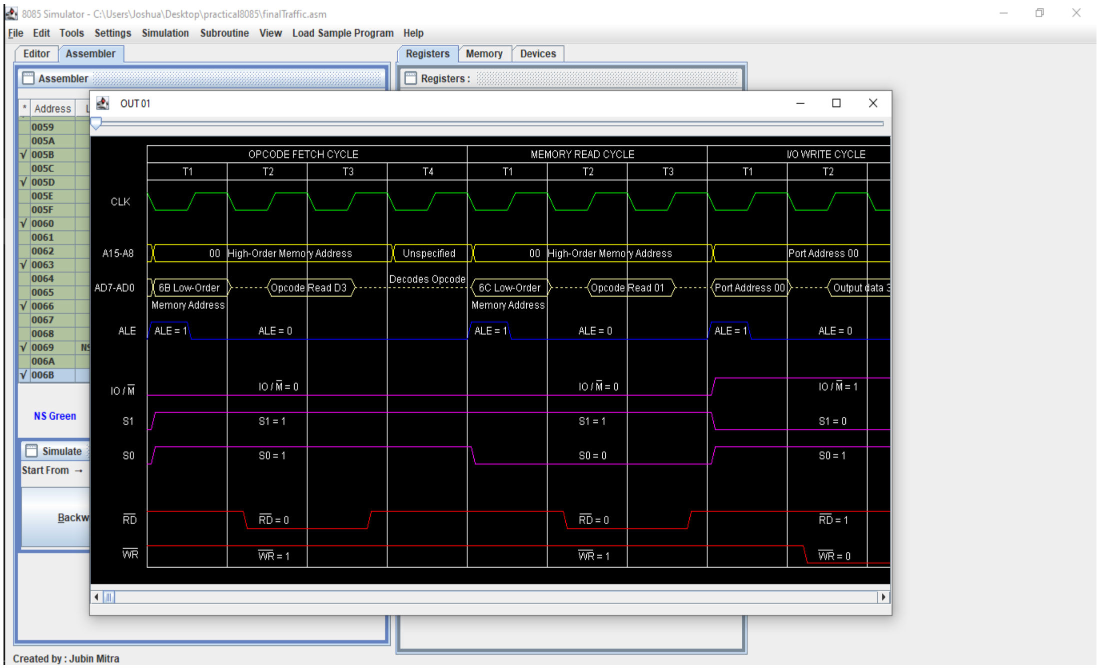
No. Converter Tool :

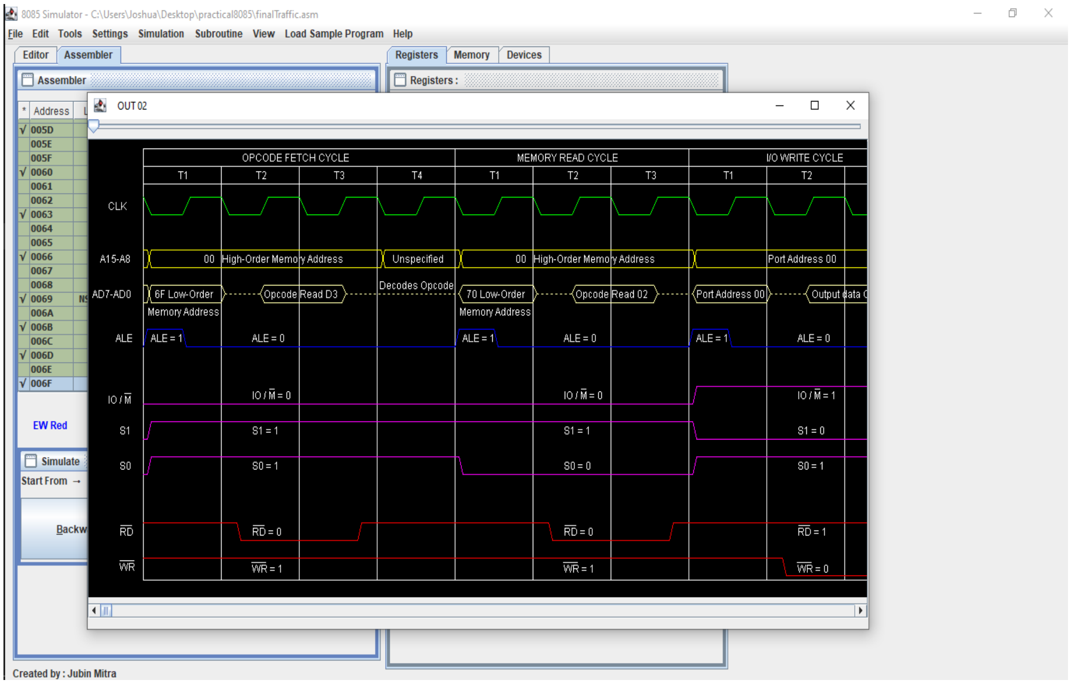
Hexadecimal	Decimal	Binary
0	0	0

EI

Discussions


8085 Simulator - C:\Users\Joshua\Desktop\practical8085\finalTraffic.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Registers Memory Devices
SIM
OPCODE FETCH CYCLE
T1 T2 T3 T4
CLK
A15-A8
00 High-Order Memory Address
Unspecified
AD7-AD0
42 Low-Order Memory Address
Opcode Read 30
Decodes Opcode
ALE
ALE = 1
ALE = 0
IO / M
IO / M = 0
S1
S1 = 1
S0
S0 = 1
RD
RD = 0
WR
WR = 1
Simulate
Start From →
0000
Backward
Created by : Jubin Mitra


8085 Simulator - C:\Users\Joshua\Desktop\practical8085\finalTraffic.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Registers Memory Devices
OUT 01
OPCODE FETCH CYCLE
MEMORY READ CYCLE
I/O WRITE CYCLE
T1 T2 T3 T4 T1 T2 T3 T1 T2
CLK
A15-A8
00 High-Order Memory Address
Unspecified
00 High-Order Memory Address
Port Address 00
AD7-AD0
6B Low-Order Memory Address
Opcode Read D3
Decodes Opcode
6C Low-Order Memory Address
Opcode Read 01
Port Address 00
Output data 3
ALE
ALE = 1
ALE = 0
ALE = 1
ALE = 0
ALE = 1
ALE = 0
IO / M
IO / M = 0
IO / M = 0
IO / M = 1
S1
S1 = 1
S1 = 1
S1 = 0
S0
S0 = 1
S0 = 0
S0 = 1
RD
RD = 0
RD = 0
RD = 1
WR
WR = 1
WR = 1
WR = 0
NS Green
Simulate
Start From →
Created by : Jubin Mitra


8085 Simulator - C:\Users\Joshua\Desktop\practical8085\finalTraffic.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
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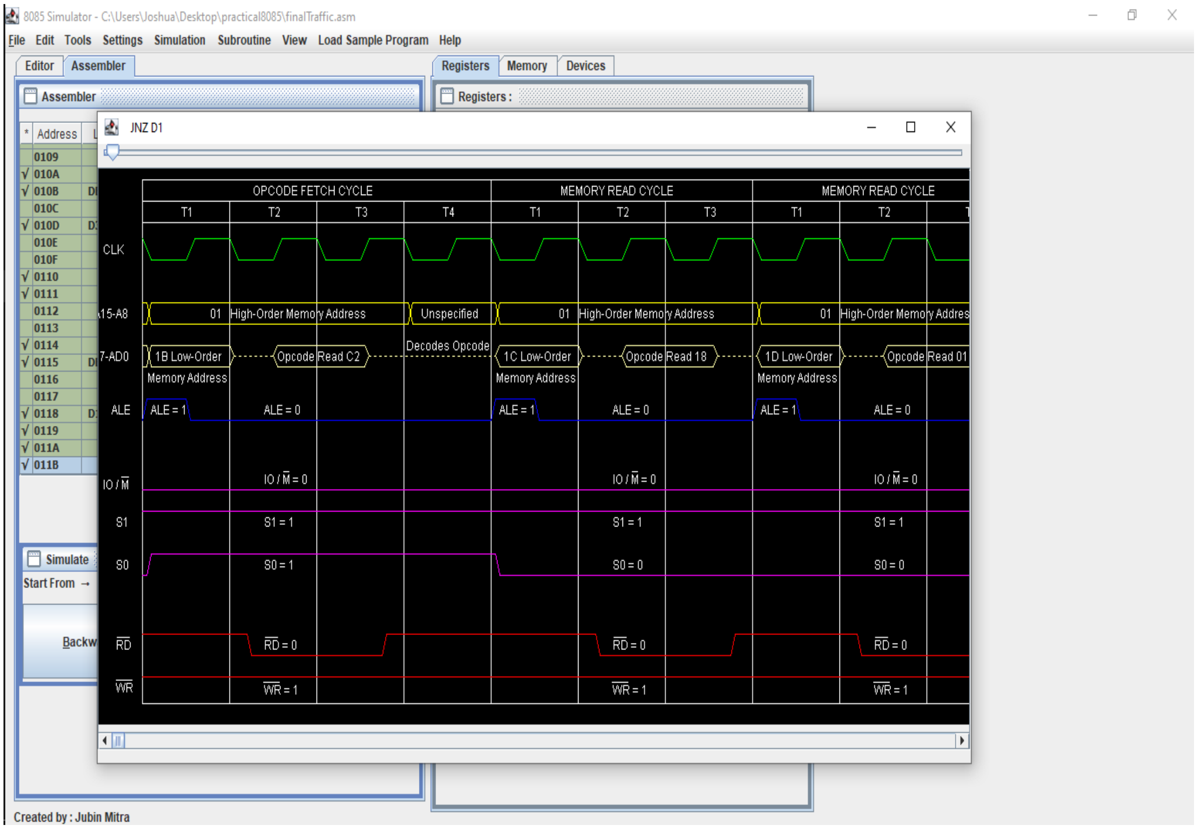
Registers :
Address
005D
005E
005F
0060
0061
0062
0063
0064
0065
0066
0067
0068
0069
006A
006B
006C
006D
006E
006F
EW Red
Simulate
Start From →
Backw
OUT 02
OPCODE FETCH CYCLE
MEMORY READ CYCLE
I/O WRITE CYCLE
T1
T2
T3
T4
T1
T2
T3
T1
T2
CLK
A15-A8
00 High-Order Memory Address
Unspecified
00 High-Order Memory Address
Port Address 00
AD7-AD0
6F Low-Order Memory Address
Opcode Read D3
Decodes Opcode
70 Low-Order Memory Address
Opcode Read 02
Port Address 00
Output data
ALE
ALE = 1
ALE = 0
ALE = 1
ALE = 0
ALE = 1
ALE = 0
IO / $\overline{M}$
IO / $\overline{M}$ = 0
IO / $\overline{M}$ = 0
IO / $\overline{M}$ = 1
S1
S1 = 1
S1 = 1
S1 = 0
S0
S0 = 1
S0 = 0
S0 = 1
$\overline{RD}$
$\overline{RD}$ = 0
$\overline{RD}$ = 0
$\overline{RD}$ = 1
$\overline{WR}$
$\overline{WR}$ = 1
$\overline{WR}$ = 1
$\overline{WR}$ = 0
Created by : Jubin Mitra


8085 Simulator - C:\Users\Joshua\Desktop\practical8085\finalTraffic.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
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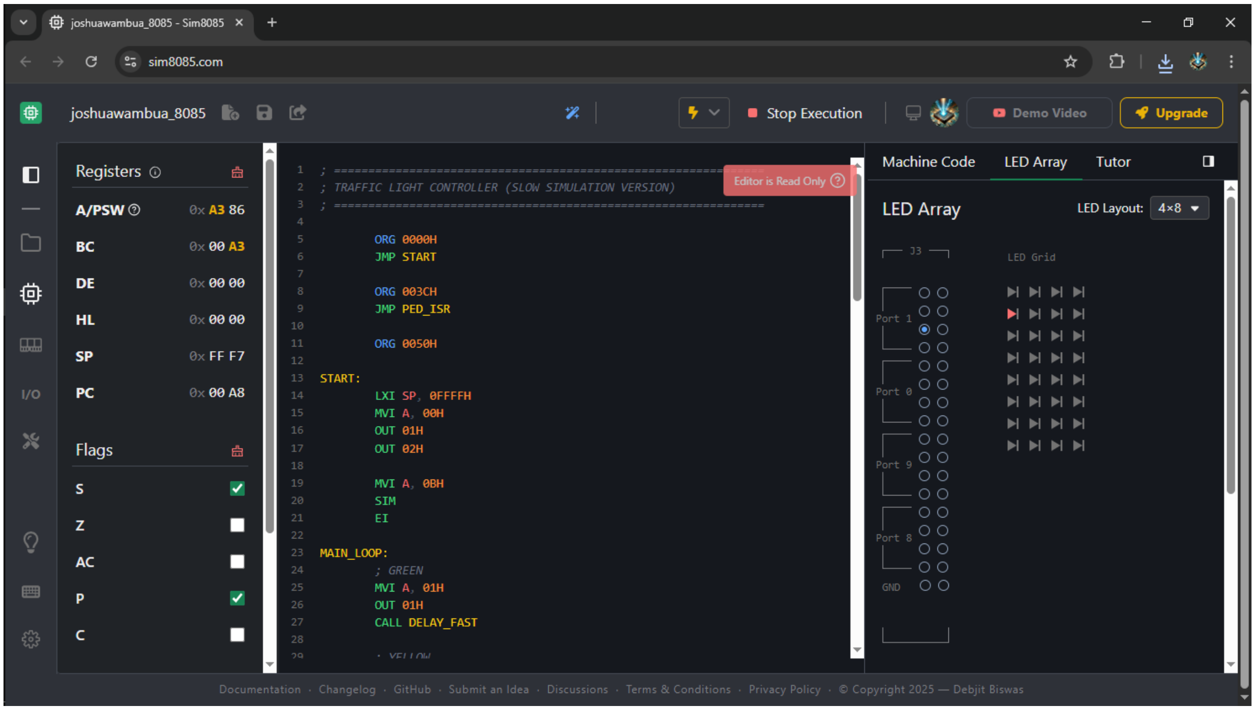
Assembler
Registers :
Address
0109
√ 010A
√ 010B
010C
√ 010D
010E
010F
√ 0110
√ 0111
0112
0113
√ 0114
√ 0115
0116
0117
√ 0118
√ 0119
√ 011A
√ 011B
Simulate
Start From →
Backw
JNZ D1
OPCODE FETCH CYCLE
MEMORY READ CYCLE
MEMORY READ CYCLE
T1 T2 T3 T4 T1 T2 T3 T1 T2
CLK
A15-A8
01 High-Order Memory Address
Unspecified
01 High-Order Memory Address
01 High-Order Memory Address
AD7-AD0
1B Low-Order Memory Address
Opcode Read C2
Decodes Opcode
1C Low-Order Memory Address
Opcode Read 18
1D Low-Order Memory Address
Opcode Read 01
ALE
ALE = 1
ALE = 0
IO / M̄
IO / M̄ = 0
S1
S1 = 1
S0
S0 = 1
S0 = 0
RD̄
RD̄ = 0
WR̄
WR̄ = 1
Created by : Jubin Mitra



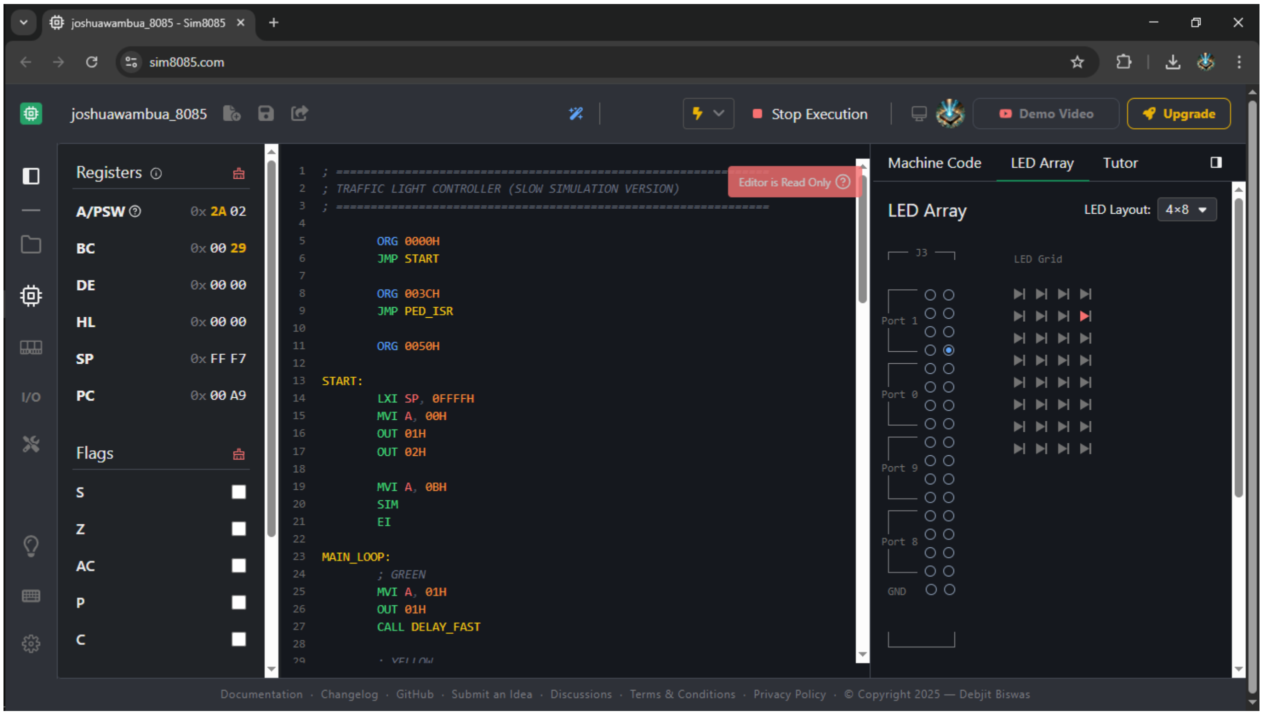
Registers

Register	Value
A/PSW	0x A3 86
BC	0x 00 A3
DE	0x 00 00
HL	0x 00 00
SP	0x FF F7
PC	0x 00 A8

Flags

Flag	
S	☑
Z	☐
AC	☐
P	☑
C	☐

```
; ================================================================
; TRAFFIC LIGHT CONTROLLER (SLOW SIMULATION VERSION)
; ================================================================

        ORG 0000H
        JMP START

        ORG 003CH
        JMP PED_ISR

        ORG 0050H

START:
        LXI SP, 0FFFFH
        MVI A, 00H
        OUT 01H
        OUT 02H

        MVI A, 0BH
        SIM
        EI

MAIN_LOOP:
        ; GREEN
        MVI A, 01H
        OUT 01H
        CALL DELAY_FAST

        ; YELLOW
```



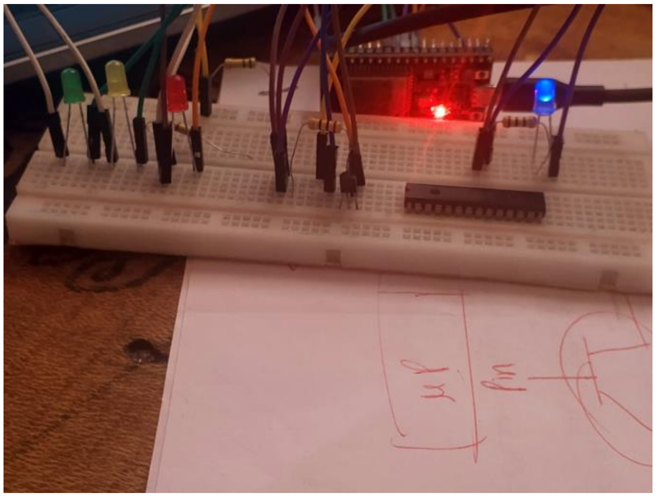
Registers

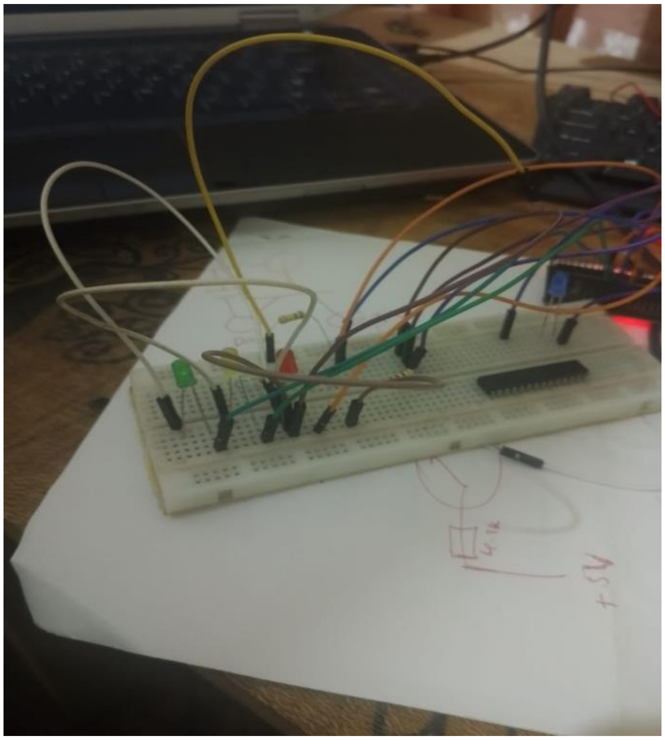
Register	Value
A/PSW	0x 2A 02
BC	0x 00 29
DE	0x 00 00
HL	0x 00 00
SP	0x FF F7
PC	0x 00 A9

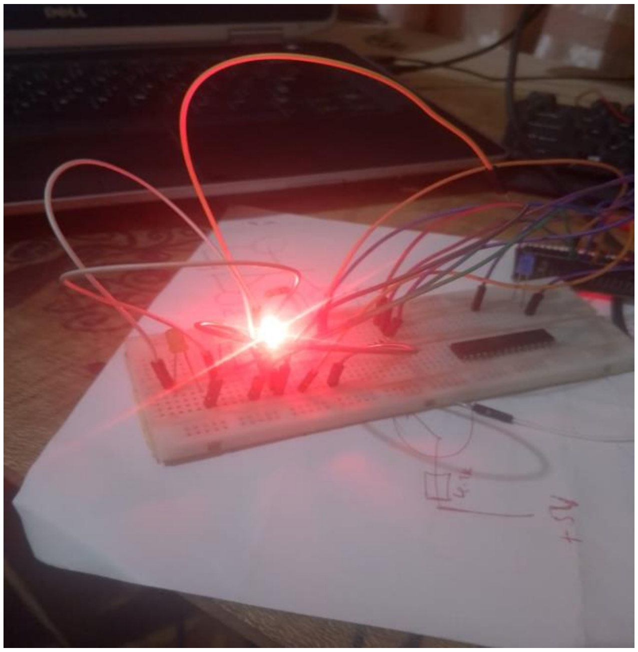
Flags

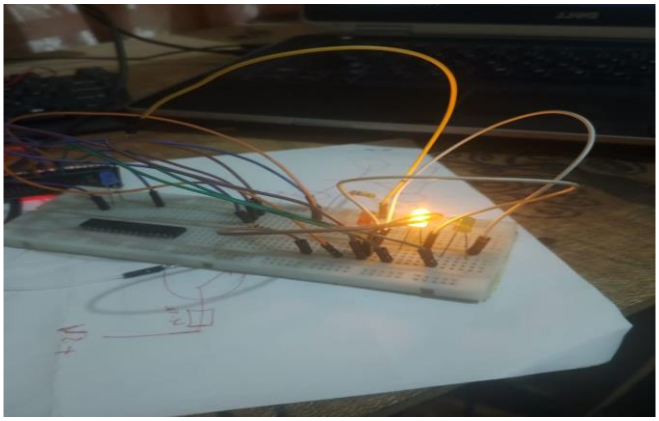
Flag	
S	☐
Z	☐
AC	☐
P	☐
C	☐

```
; ================================================================
; TRAFFIC LIGHT CONTROLLER (SLOW SIMULATION VERSION)
; ================================================================

        ORG 0000H
        JMP START

        ORG 003CH
        JMP PED_ISR

        ORG 0050H

START:
        LXI SP, 0FFFFH
        MVI A, 00H
        OUT 01H
        OUT 02H

        MVI A, 0BH
        SIM
        EI

MAIN_LOOP:
        ; GREEN
        MVI A, 01H
        OUT 01H
        CALL DELAY_FAST

        ; YELLOW
```


μP
Pin


4.7k
+5V





Discussions

Conclusion

References