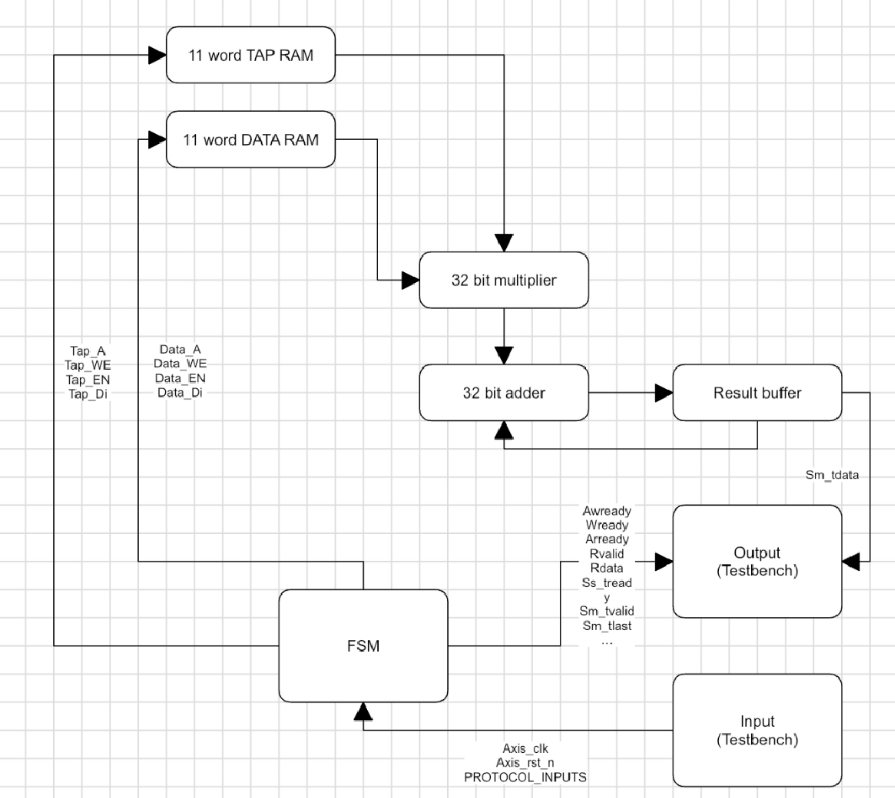
SoC Design Lab 4-2 Report

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1. Design block diagram –datapath, control-path

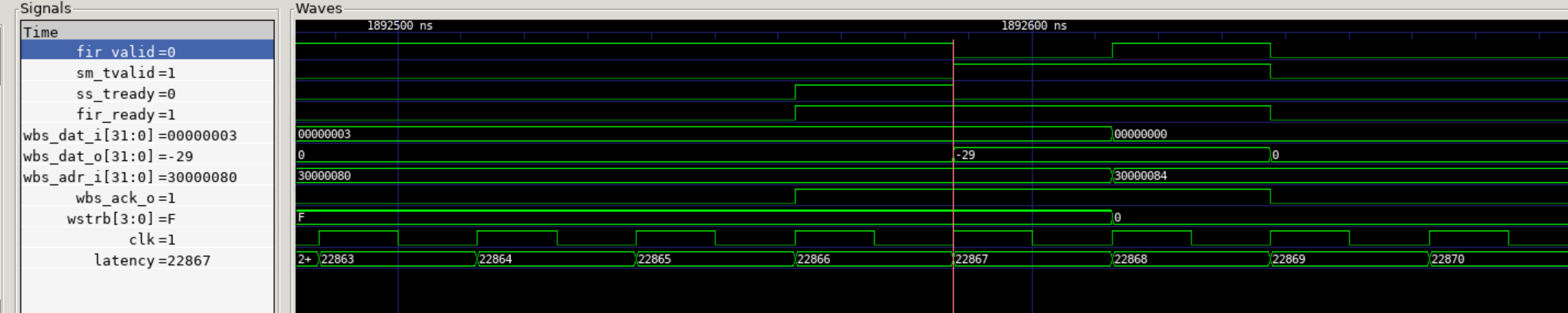
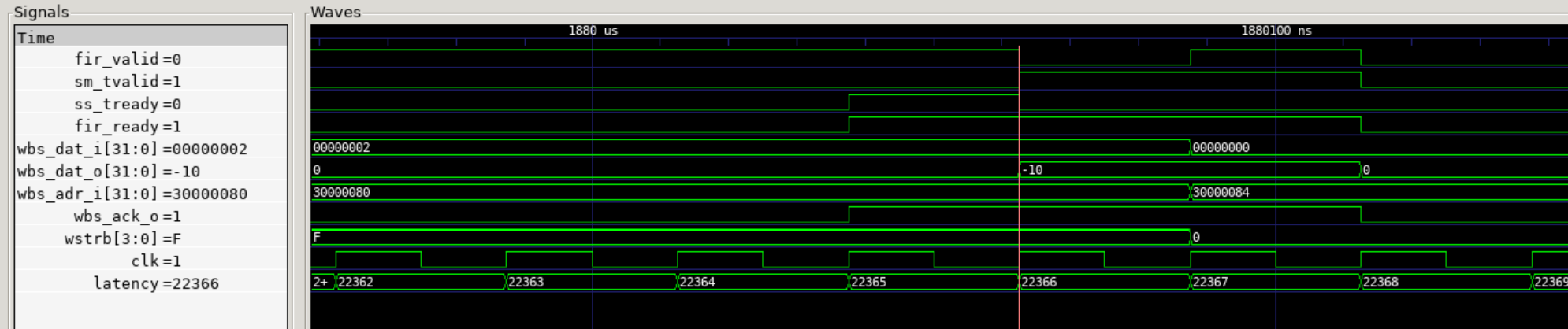


1. The interface protocol between firmware, user project and testbench

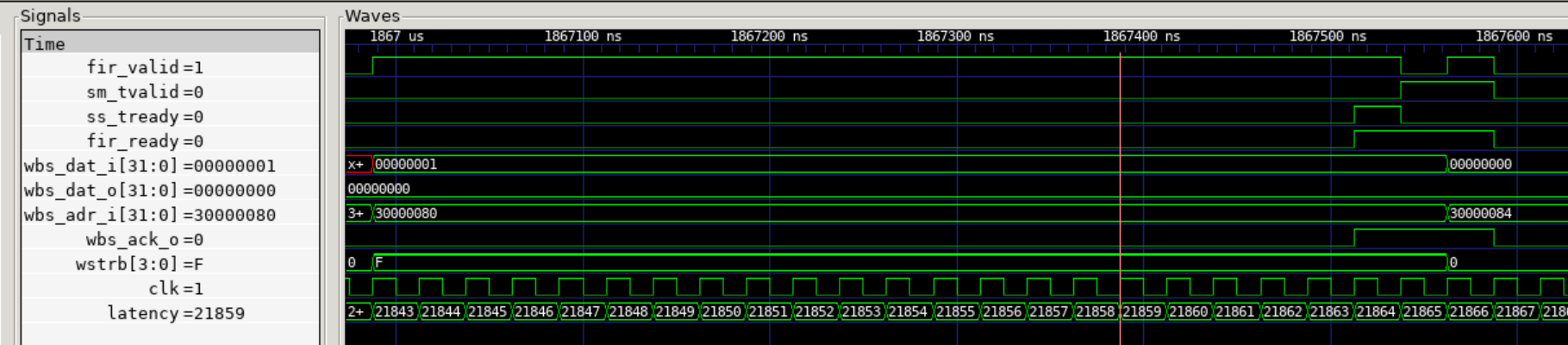
The interface protocol between firmware, user project and testbench is the Wishbone. We need to convert the WB to AXI-Lite interface to communicate with our Verilog-FIR. If wb address is in the range 3000\_0000 3000\_007F, read/write convert to Axilite. If wb address is 3000\_0080 ( send X[n]), write transaction converts to axi stream master to send data to verilog FIR. If wb address is 3000\_0084 ( read Y[n] ), Read transaction, converts to axi stream slave to read Y[n] from verilog FIR.

1. Waveform and analysis of the hardware/software behavior.

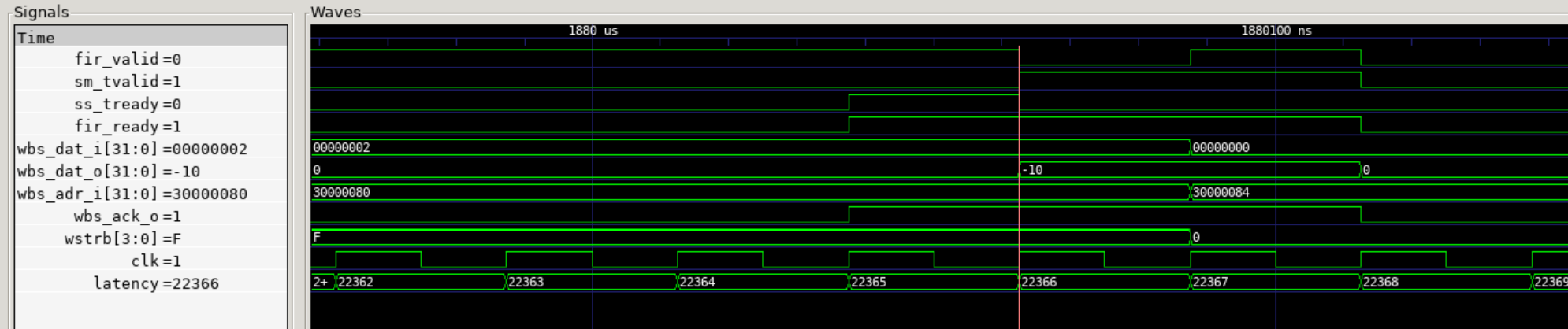
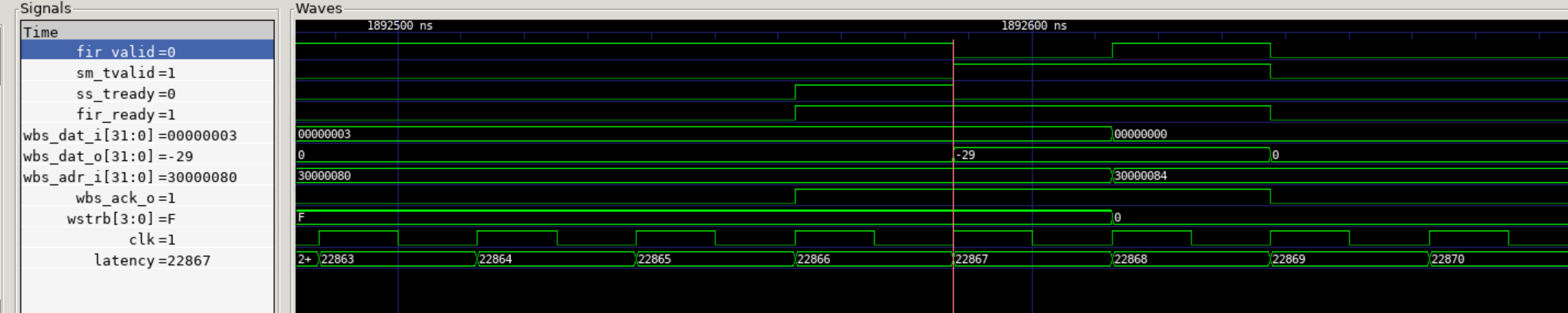
由於我們在firware中以for loop的形式將資料送給fir engine，WB接收到兩個output間的時間會因為去讀取0x3800….的地方而拉長，如下圖所示，從fir的第一個output至第二個output的間隔約為500cycle。



1. What is the FIR engine theoretical throughput, i.e. data rate? Actually measured throughput?

The theoretical throughput would 1/11\*clock frequency since the fir engine needs 11 cycle to compute one stream output. However, since we use bram to store needed data. We need to use more cycle since bram is synchronous read. As figure below, actually measured throughput in our design is 1/24\*clock frequency. (21843 cycle to 21866 cycle)

1. What is latency for firmware to feed data?

由於我們在firware中以for loop的形式將資料送給fir engine，WB接收到兩個output間的時間會因為去讀取0x3800….的地方而拉長，如下圖所示，從fir的第一個output至第二個output的間隔約為500cycle。 

1. What techniques used to improve the throughput? Does bram12 give better performance, in what way?

我們可以使用bram12來增加throughput，由於本次的fir engine最多只需要進行11次乘加運算，使用bram12可以利用到pre-fetch的方式，在前一個cycle提前準備好資料，故能將實際throughput增加。

1. Can you suggest other method to improve the performance?

在合成時，可以利用retime的技術，提升效能。