**LTSpice Analog Spike Detector: Rate-of-Change Circuit**

**1. Introduction and Purpose**

This LTSpice schematic (analog\_spike\_detector.asc) implements an analog circuit designed to detect **sudden increases in entropy**, specifically by reacting to the *rate of change* (or derivative) of an input "entropy" signal, rather than just its absolute voltage level.

**Why did we build this circuit?**

In complex systems like CPU pipelines, hazards aren't always indicated by an entropy score *crossing* a fixed high threshold (which your previous circuit handles). Sometimes, a **rapid, sudden surge** in entropy (even if the absolute value is still below a "high" threshold) can signify an impending or immediate threat. This circuit provides a **reflex path**: an immediate, analog-driven warning system that can trigger a fast, pre-emptive response in a digital control unit (like your FSM), bypassing slower, clock-dependent digital logic or ML inference. This adds an extra layer of **low-latency reactivity and robustness** to the overall hazard mitigation strategy.

**2. Circuit Description**

The circuit consists of three primary functional blocks:

1. **Input Signal (V\_entropy\_rising):**
   * This voltage source simulates an analog entropy output, specifically crafted with PWL (Piecewise Linear) segments. It features both gradual and sharp positive ramps, along with flat and falling segments, to test the rate-of-change detection.
   * Node: N\_entropy\_rising
2. **RC Differentiator:**
   * **Components:** C\_differentiator (1nF) and R\_differentiator (1kΩ).
   * **Function:** This combination forms a high-pass RC filter, which acts as an approximate differentiator. When the input voltage (N\_entropy\_rising) changes, particularly when it changes rapidly (has a steep slope), this circuit generates a voltage spike at its output. The magnitude of the output spike is proportional to the rate of change of the input. A faster rise in N\_entropy\_rising results in a higher positive spike on N\_differentiator\_out.
   * Node: N\_differentiator\_out
3. **Voltage Comparator Layer:**
   * **Component:** XU1\_comparator (using the AD711 op-amp model).
   * **Threshold:** V\_threshold (0.3V), connected to N\_threshold\_ref.
   * **Function:** This op-amp is configured as a comparator. It continuously compares the output of the differentiator (N\_differentiator\_out) with the fixed N\_threshold\_ref (0.3V).
     + If N\_differentiator\_out rises above 0.3V, the comparator's output (analog\_spike\_override) will swing high (to +5V, VDD).
     + If N\_differentiator\_out is below 0.3V, its output will swing low (to -5V, VSS).
   * **Note on AD711:** Due to library availability, we've used AD711.asy, a model for a real-world operational amplifier, instead of an ideal opamp.asy. While AD711 has practical limitations (like finite gain, slew rate, etc.) unlike an ideal op-amp, it will still effectively function as a comparator for the voltage levels in this circuit.
   * Node: analog\_spike\_override (the direct analog output)
4. **Analog-to-Digital Converter (ADC) / Level Shifter:**
   * **Component:** B1\_spike\_adc (a Behavioral Voltage Source).
   * **Function:** This crucial component takes the analog\_spike\_override signal (which swings between -5V and +5V) and converts it into a clean, digital-compatible 0V/1V signal. The expression V=F(V(analog\_spike\_override) > 2.5 ? 1 : 0) means that if analog\_spike\_override is above 2.5V (mid-point of its swing), the output N\_fsm\_spike\_in will be 1V; otherwise, it will be 0V. This output is specifically designed to be directly routed as a digital input to your FSM.
   * Node: N\_fsm\_spike\_in (the digital output for FSM)

**Power Supplies:**

* V\_VDD (+5V) and V\_VSS (-5V) provide the necessary operating voltage rails for the AD711 op-amp. All ground points are connected to a common 0V reference.

**3. Simulation Setup**

The circuit is configured for a transient simulation to observe its dynamic response to changing input.

* **Simulation Command:** .tran 0.8m (simulates for 0.8 milliseconds from 0s).
* **Library Directive:** .lib OpAmps/AD711.asy (or the full path as determined by the "Browse" function in LTSpice). This directive tells LTSpice where to find the model for the AD711 op-amp.
* **Input V\_entropy\_rising (PWL):**
  + 0 0 (0V at 0s)
  + 0.1m 0 (0V at 0.1ms)
  + 0.15m 5 (Rises sharply to 5V by 0.15ms - *Steep Slope Test*)
  + 0.2m 5 (Stays at 5V)
  + 0.25m 0 (Falls sharply to 0V)
  + 0.3m 0 (Stays at 0V)
  + 0.4m 1 (Starts rising gradually)
  + 0.45m 1.5
  + 0.5m 2
  + 0.55m 2.5
  + 0.6m 3
  + 0.65m 5 (Reaches 5V by 0.65ms - *Gradual Slope Test*)
  + 0.7m 5 (Stays at 5V)
  + 0.75m 0 (Falls sharply to 0V)

A computer screen shot of a diagram

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**4. Expected Simulation Results**

Upon running the transient simulation, we expect to see the following key waveforms:

* **N\_entropy\_rising (Input):** This trace will show the defined piecewise linear voltage. You will observe both the very sharp rise (0.1ms to 0.15ms) and the more gradual rise (0.4ms to 0.65ms), along with flat and falling segments.
* **N\_differentiator\_out (RC Differentiator Output):**
  + During the **sharp positive rise** of N\_entropy\_rising (e.g., 0.1ms to 0.15ms), this trace will exhibit a **large, distinct positive spike**.
  + During the **gradual positive rise** of N\_entropy\_rising (e.g., 0.4ms to 0.65ms), this trace will show a **smaller, lower positive bump or spike** (potentially below the 0.3V threshold, depending on the exact slope).
  + When N\_entropy\_rising is flat, N\_differentiator\_out will be near 0V.
  + During sharp falls, you will see negative spikes.
* **analog\_spike\_override (Analog Output):**
  + This signal will primarily be at −5V.
  + It will jump to +5V only when the **positive spike from N\_differentiator\_out exceeds the** 0.3V **threshold** (i.e., during the steepest positive slopes of N\_entropy\_rising).
  + It will remain at +5V for the duration that N\_differentiator\_out is above 0.3V, then fall back to −5V. This demonstrates the circuit effectively acting as a "spike detector."
* **N\_fsm\_spike\_in (Digital Output for FSM):**
  + This signal will closely mirror analog\_spike\_override, but it will be a clean 0V to 1V pulse.
  + It will transition to 1V only when analog\_spike\_override goes to +5V, and return to 0V when analog\_spike\_override returns to −5V. This is the ready-to-use digital input for your FSM.

In conclusion, this circuit successfully demonstrates a method for detecting the rate-of-change in an analog signal and converting that detection into a digital pulse, providing a rapid, hardware-accelerated hazard warning to your digital control system.