EET 3404: DIGITAL CIRCUIT DESIGN.
PARITY GENERATOR AND CHECKER.

GROUP 10 PRESENTATION.

GITHUB REPOSITORY:

https://github.com/joshuawambua/parity.git

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INTRODUCTION

In digital systems, **parity** is a method used to ensure that data remains accurate when it is transmitted or stored. It works by adding a special bit, called a **parity bit**, to a set of data bits. This bit indicates whether the total number of 1s in the data is even or odd. For example, in even parity, the parity bit is chosen so that the total number of 1s (including the parity bit) becomes even. In odd parity, it is chosen so that the total number of 1s becomes odd.

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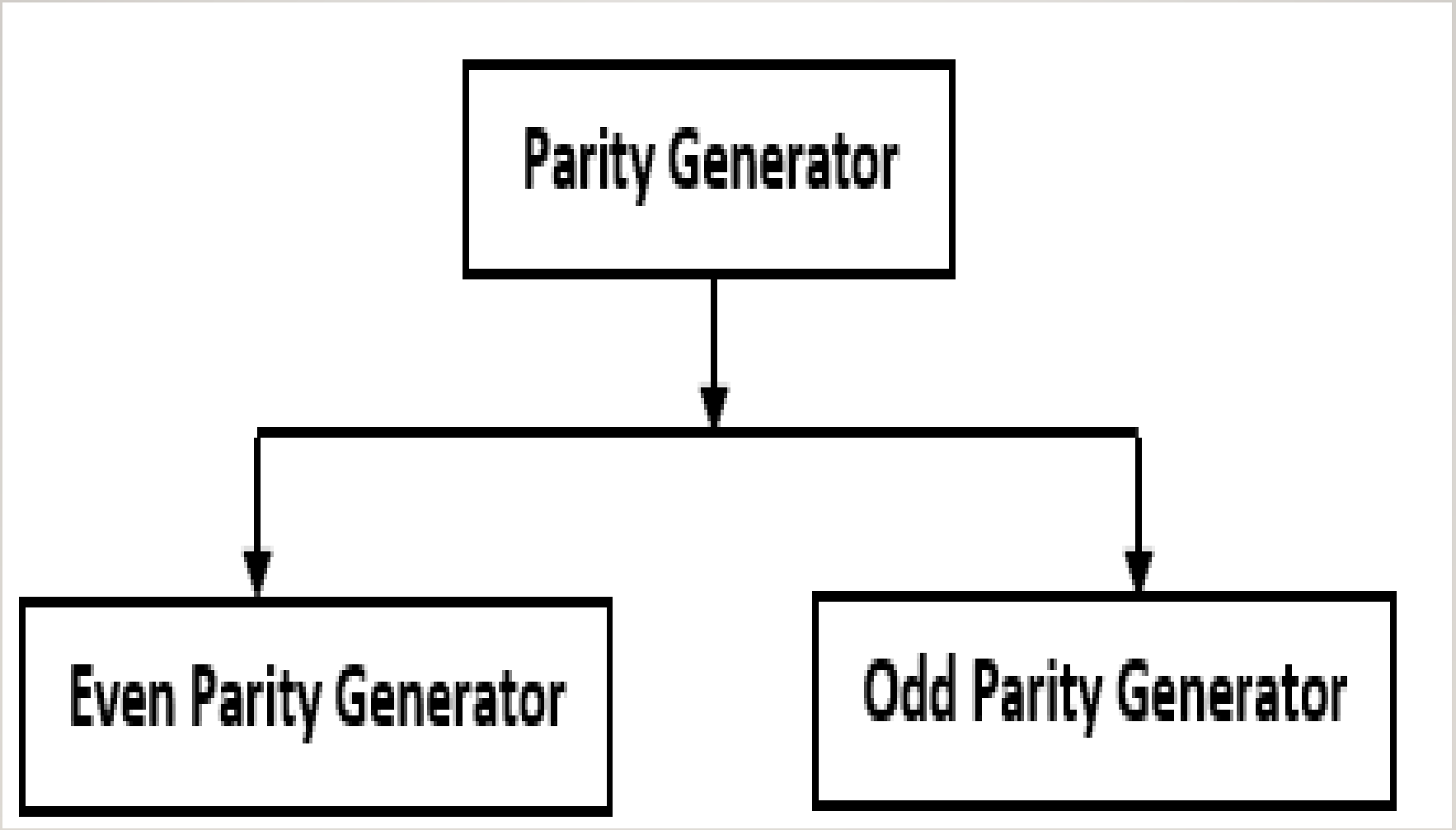
Parity checking helps detect errors that might occur when data is sent through communication channels or stored in digital memory. If a bit changes due to noise or interference, the receiver can quickly notice it by checking the parity. Although this method cannot correct the error, it provides a simple and effective way to identify when data has been altered, ensuring basic reliability in digital communication and storage systems.

EVEN PARITY.

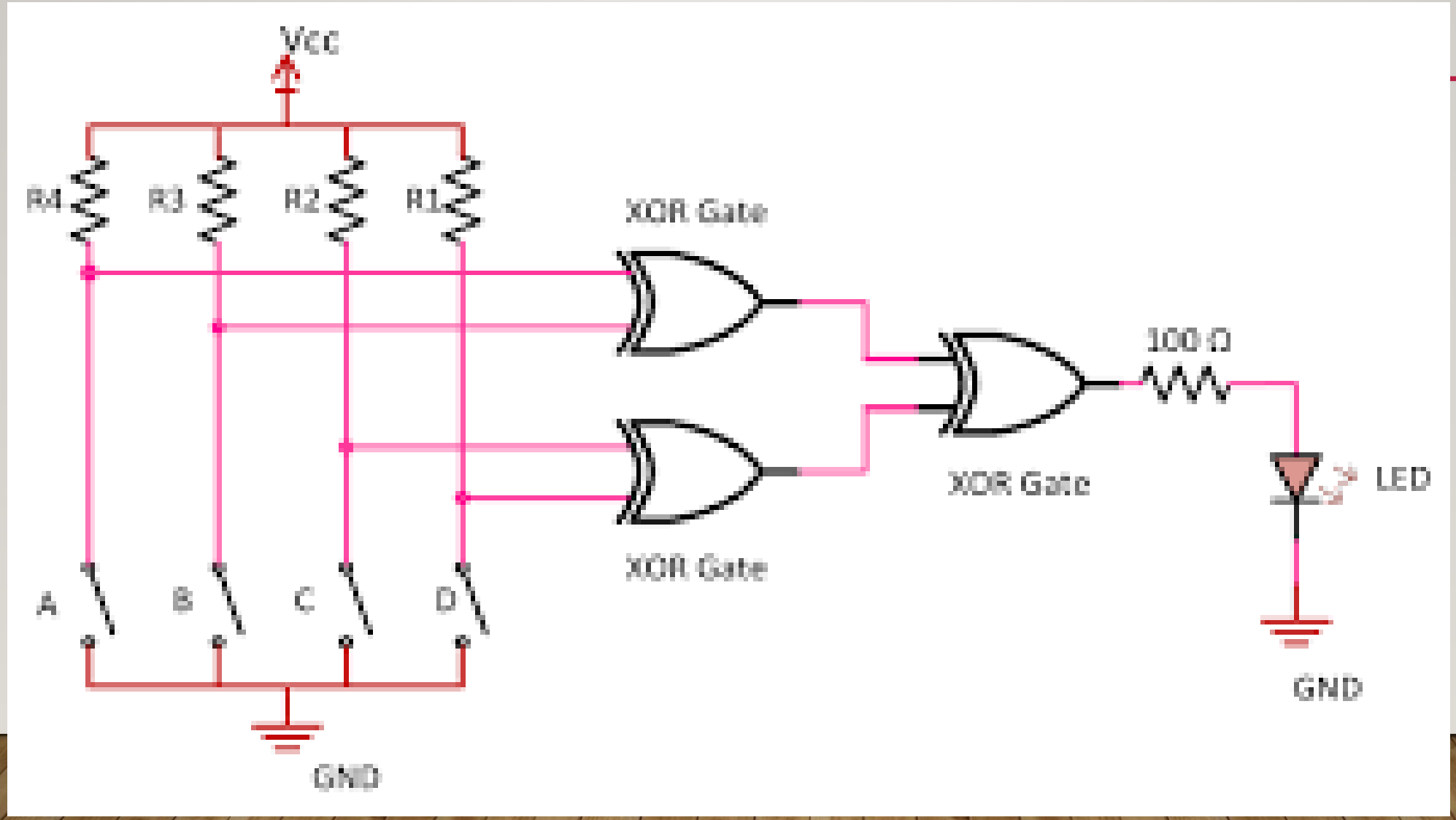
In even parity, the parity bit is chosen so that the total number of 1s in the entire data set (including the parity bit) is an even number. For instance, if a data word contains three 1s, the parity bit is set to 1 to make the total number of 1s equal to four, which is even. Even parity is one of the most common error detection methods used in communication systems and memory storage because it offers a straightforward way to check data integrity. When the receiver counts an odd number of 1s instead of even, it knows that an error has occurred during transmission.

ODD PARITY

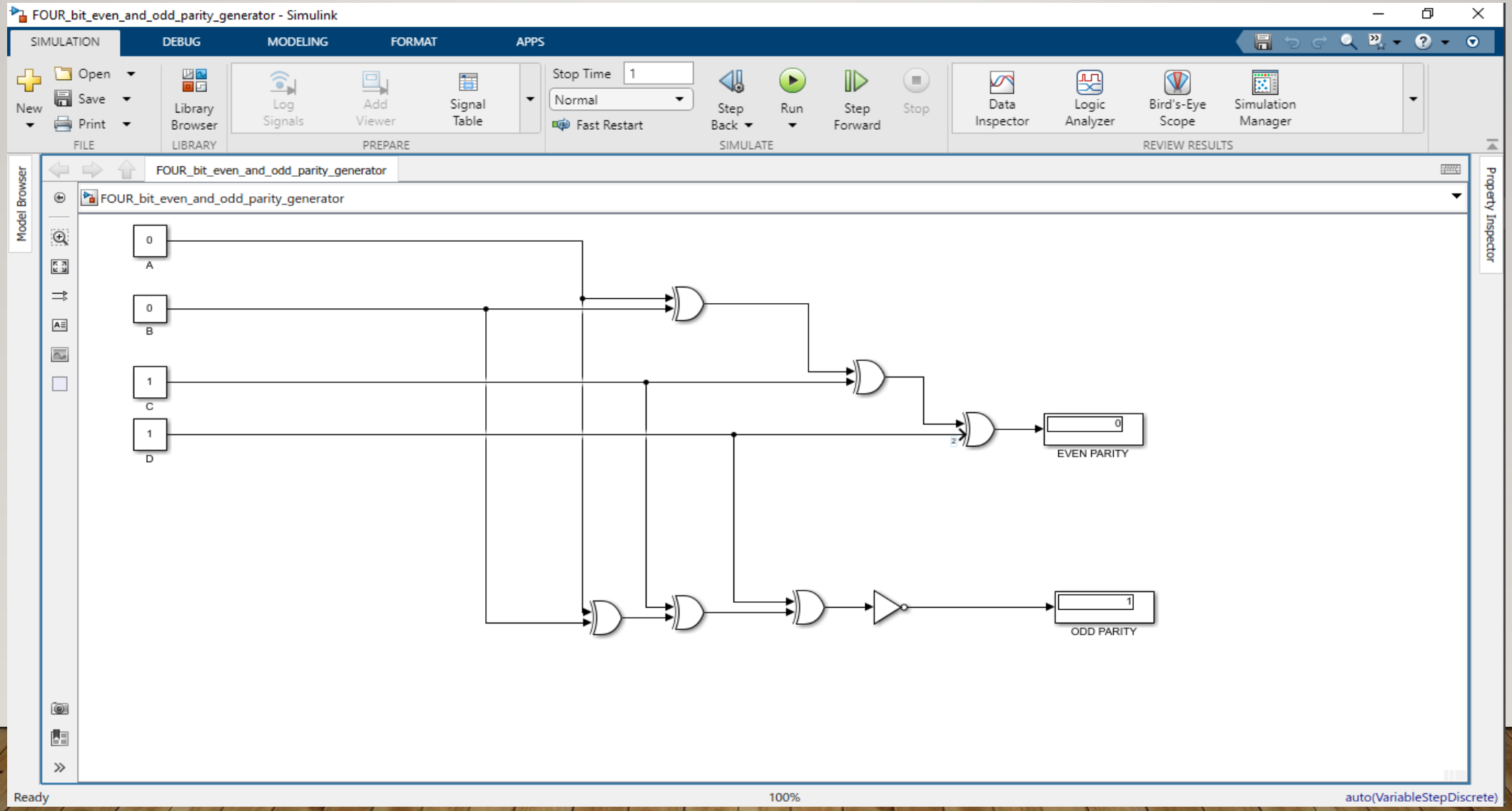
In odd parity, the parity bit is chosen so that the total number of 1s (including the parity bit) becomes an odd number. For example, if the data word already contains two 1s, the parity bit is set to 1 to make the total number of 1s three — an odd count. Odd parity works the same way as even parity but follows the opposite rule. It is used in systems or communication standards that require an odd count of 1s for consistency. Like even parity, it can detect single-bit errors efficiently, ensuring the accuracy of transmitted or stored data.


Parity Generator
Even Parity Generator
Odd Parity Generator

CIRCUIT DIAGRAM – EVEN PARITY GENERATOR.



SIMULINK CIRCUIT PARITY GENERATOR.



TRUTH TABLES
4 BIT PARITY GENERATOR.

4-bit

A	B	C	D	EVEN PARITY	ODD PARITY
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

3-bit

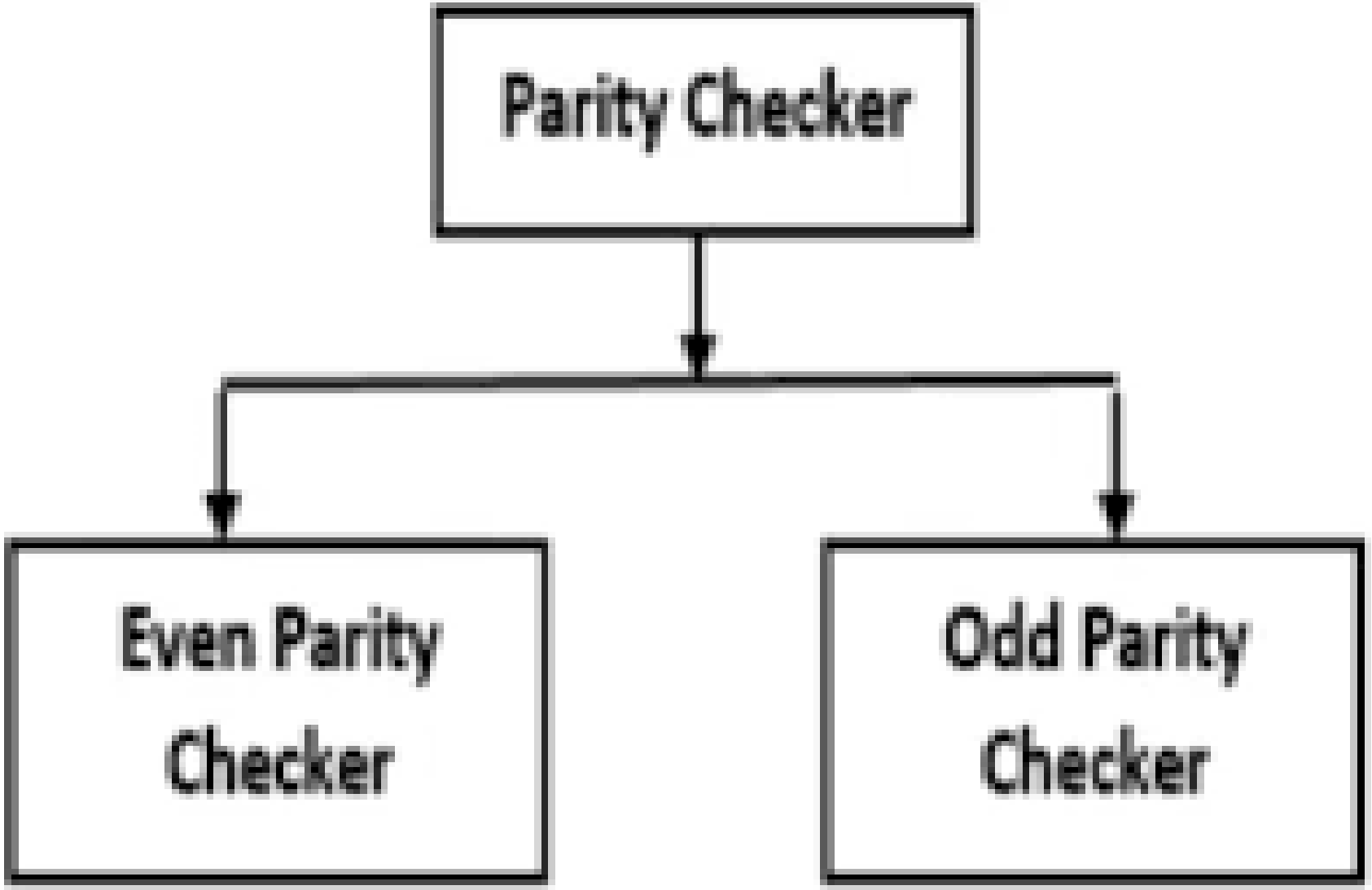
A	B	C	EVEN	ODD
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

5-BIT

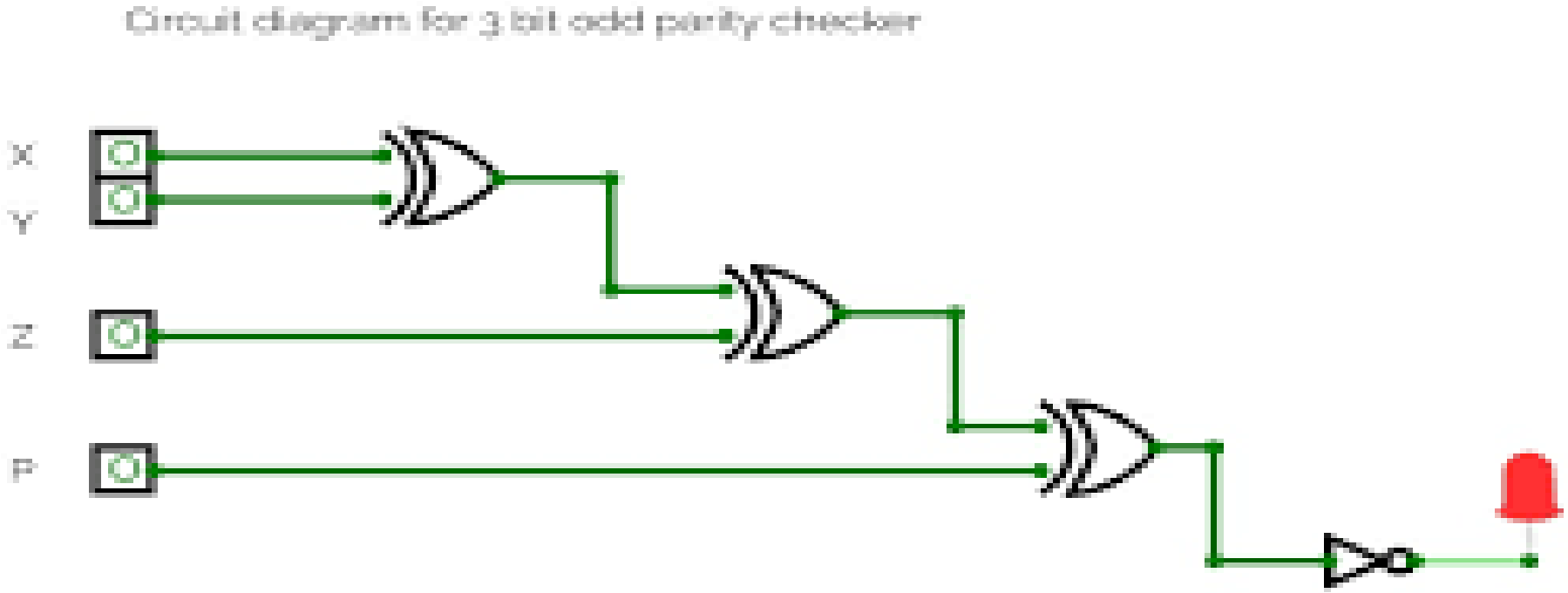
A	B	C	D	E	EVEN	ODD
0	0	0	0	0	0	1
0	0	0	0	1	1	0
0	0	0	1	0	1	0
0	0	0	1	1	0	1
0	0	1	0	0	1	0
0	0	1	0	1	0	1
0	0	1	1	0	0	1
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	0	1	0	1
0	1	0	1	0	0	1
0	1	0	1	1	1	0
0	1	1	0	0	0	1
0	1	1	0	1	1	0
0	1	1	1	0	1	0
0	1	1	1	1	0	1
1	0	0	0	0	1	0
1	0	0	0	1	0	1
1	0	0	1	0	0	1
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	0	1	0	1	1	0
1	0	1	1	0	1	0
1	0	1	1	1	0	1
1	1	0	0	0	0	1
1	1	0	0	1	1	0
1	1	0	1	0	1	0
1	1	0	1	1	0	1
1	1	1	0	0	1	0
1	1	1	0	1	0	1
1	1	1	1	0	0	1
1	1	1	1	1	1	0

PARITY CHECKER

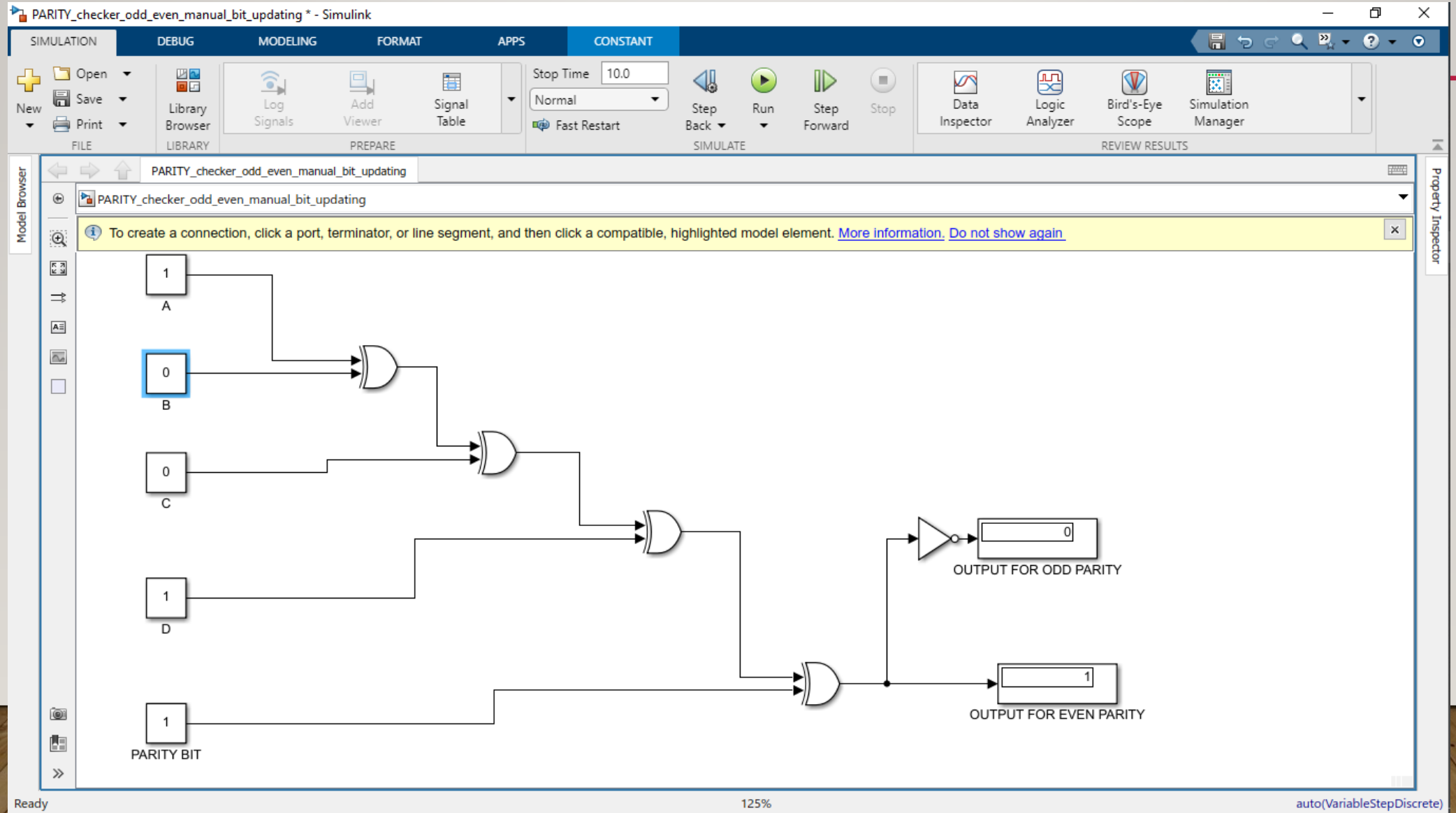
A parity checker is a digital circuit used to verify whether the received data has maintained the correct parity—either even or odd—after transmission or storage. It operates using XOR logic to compare all the data bits, including the parity bit. In the case of even parity, the total number of 1s in the data should be even; if the checker output is 0, it means the data is correct, while an output of 1 indicates an error. For odd parity, the total number of 1s should be odd; here, an output of 1 shows correct data, and an output of 0 signals an error. This method effectively detects single-bit errors and is widely used in digital communication systems, memory units, and microcontroller-based circuits to ensure data accuracy and reliability.


Parity Checker
Even Parity Checker
Odd Parity Checker

CIRCUIT DIAGRAM – ODD PARITY CHEKER.



PARITY CHECKER.



APPLICATION OF PARITY

1. Used for **error detection** in digital communication systems.

Parity bits are widely used to detect single-bit errors during digital data transmission.
When data is sent over a channel, noise or interference can flip a bit from 0 → 1 or vice versa.
A parity checker compares the received parity bit with the recalculated one – if they differ, an error is detected.
This ensures reliable communication between devices.

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APPLICATIONS OF PARITY.

2. Used in **computer memory (RAM)** to check for data corruption.

Some types of Random Access Memory (especially older systems and servers) include parity bits for every byte of data stored.

When data is read back, the memory controller checks the parity — if the parity bit doesn't match, an error is detected.

While modern systems use **ECC (Error Correction Code)** memory, parity checking laid the foundation for such technologies.

APPLICATIONS OF PARITY.

3. Storage Media (Hard Drives, CDs, DVDs)

Data stored on physical media is vulnerable to scratches, dust, and magnetic decay. Parity bits (and parity-based schemes) are used to verify that data blocks are correctly written and retrieved. If mismatched parity is detected, the system knows that data corruption occurred and may attempt recovery or request retransmission.

APPLICATIONS OF PARITY.

4.Ensures **data integrity** during transmission and storage.
5. Applied in **UART serial communication** for detecting bit errors.
6. Implemented in **network devices** like modems and routers for error checking.
7. Forms the basis of advanced error detection codes such as **Hamming Code**.
8. Utilized in **microcontrollers and embedded systems** for reliable data exchange.
9. Applied in **satellite and space communication** to detect bit flips caused by noise or radiation.


THANK
YOU!