MIPS32 Processor on DE0-Nano with Peripheral Shields

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Abstract

A Field-Programmable Gate Array (FPGA) is a prototyping device used to implement logical functions. It can be reprogrammed using Verilog or VHDL.

It can do many things a microcontroller like the Arduino can.

Table 1: Features of MIPS 32 on DE0-Nano vs. Arduino Uno

Criteria	MIPS on DE0-Nano	Arduino Uno
Clock Speed	50 MHz	16 MHz
Architecture Type	32-bit, pipelined	8-bit, single-instruction
Instruction Memory	16-32 Mb, volatile	32 kb, non-volatile flash
Dynamic Memory	16-32 Mb SDRAM	2 kb DRAM
EEPROM	2kb	1kb
# of digital pins	81 bidirectional + 7 input	14 digital pins, ICSP header
# of analog pins	8 analog inputs	6 analog inputs
I/O voltage	3.3V TTL, non-5V tolerant	5V TTL
Price	$79 ($61 academic)	$46
Power draw	~180 mA (measured)	~17 mA, can enter sleep

$79 ($59 for students)
DE0-Nano
50 MHz 32-bit soft processor
32MB SDRAM
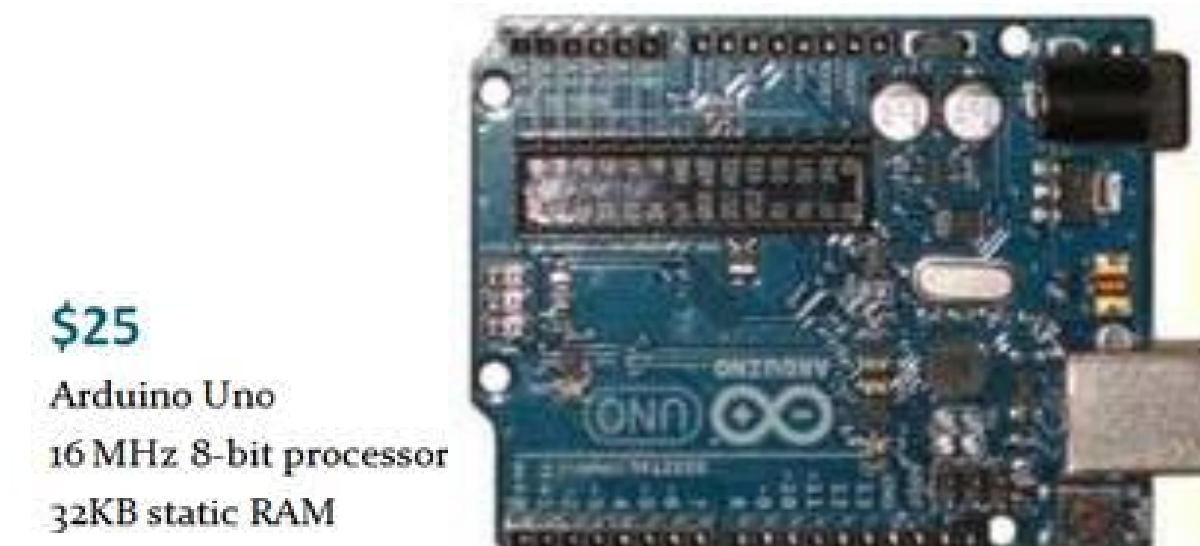
$25
Arduino Uno
16 MHz 8-bit processor
32KB static RAM

Our Objective

To create an educational platform for microprocessor design, useful for students, hobbyists, and enthusiasts

Features:
• 32 MB SDRAM chip w/ controller
• 32-bit 50 MHz RISC processor
• GCC Compiler Toolchain
• Top Debug Shield with I/O Devices:
  • Buttons
  • 7-segment Displays
  • MicroSD Socket
  • Female Pin Headers
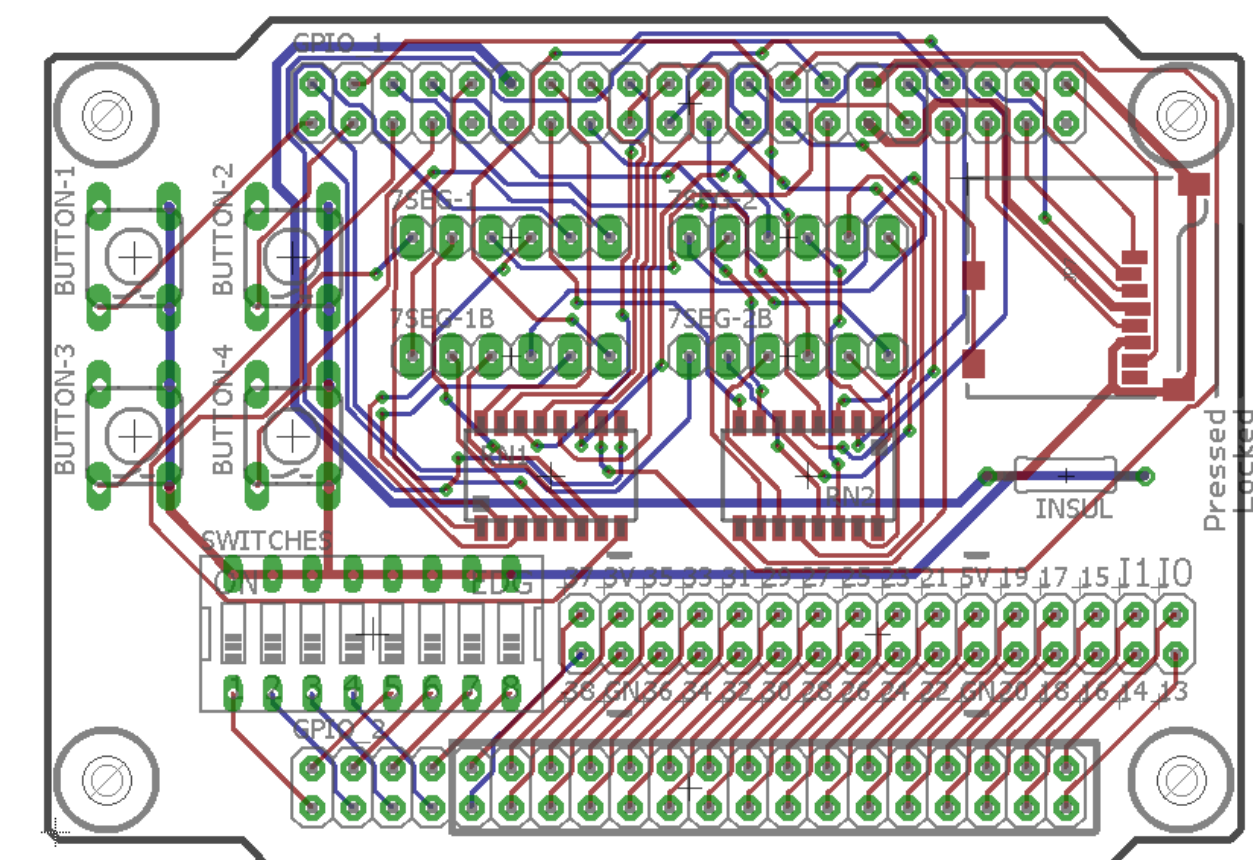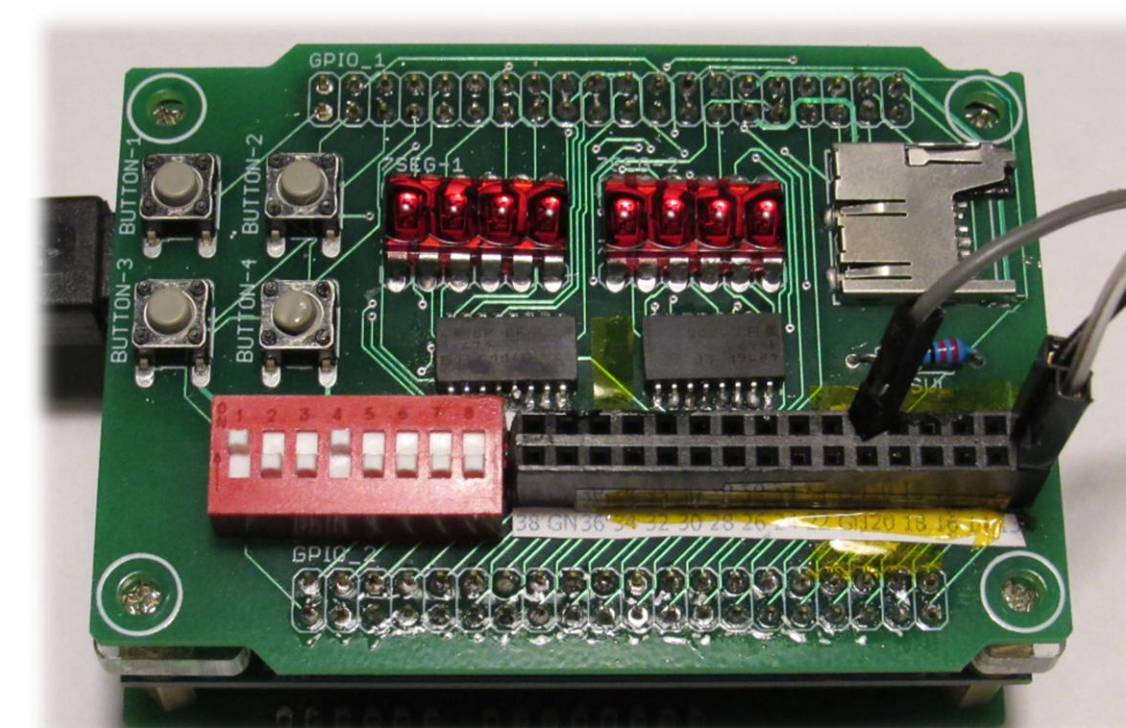• Bottom Arduino Adapter Shield
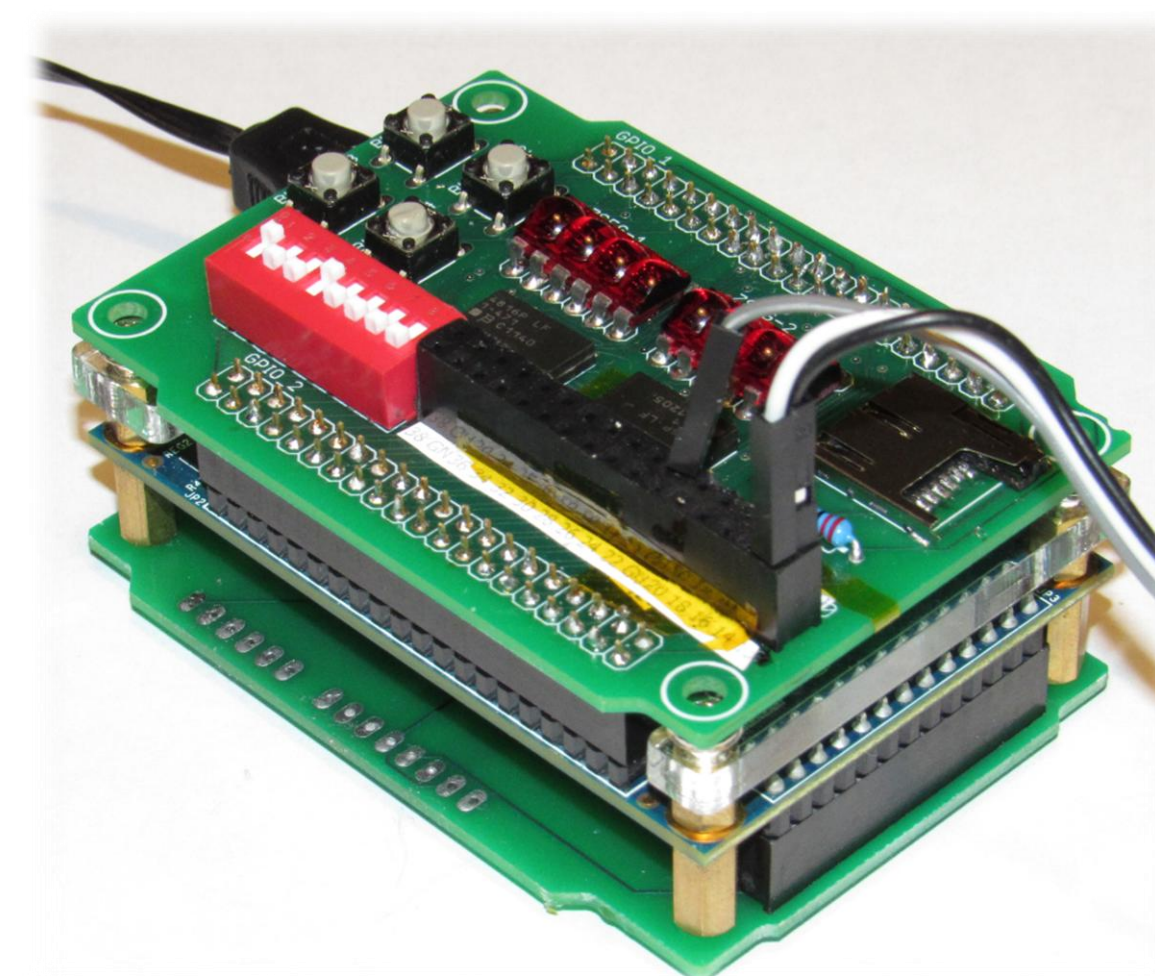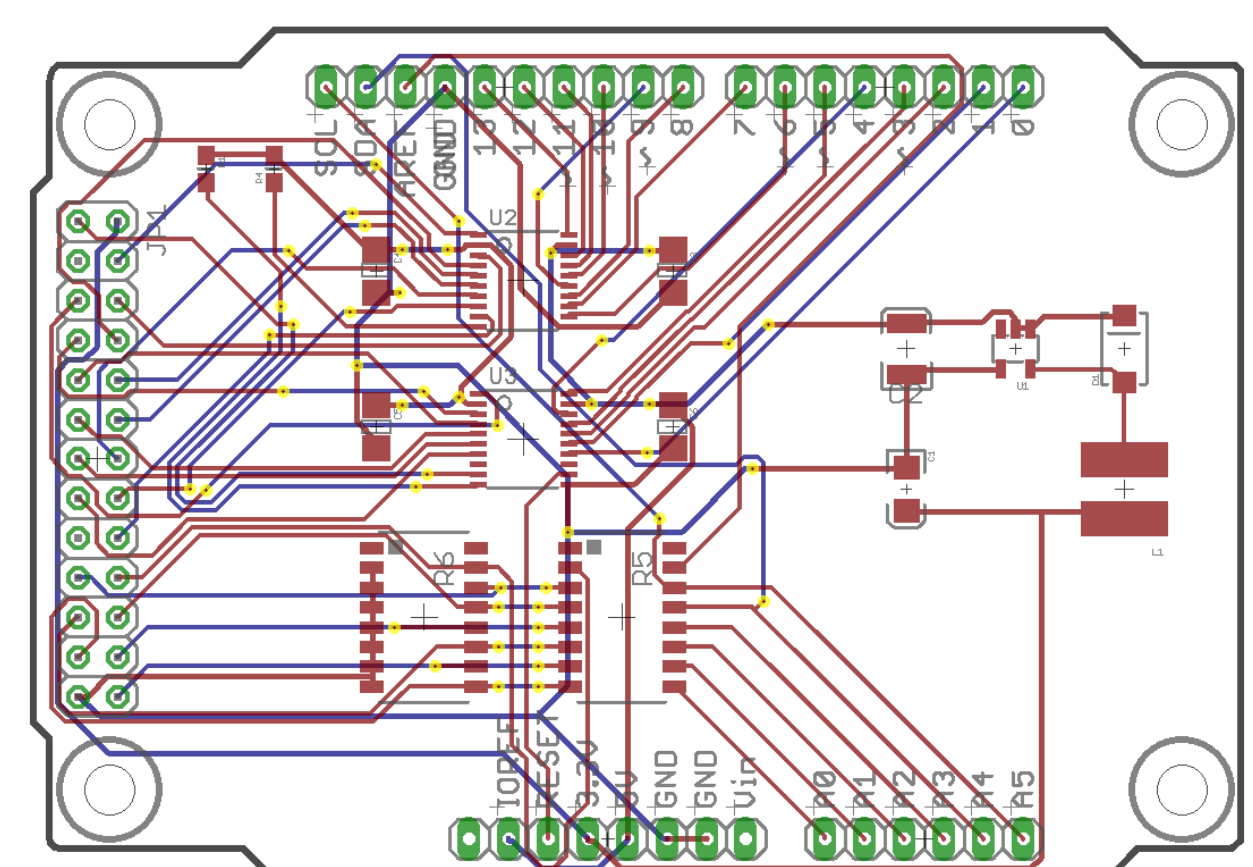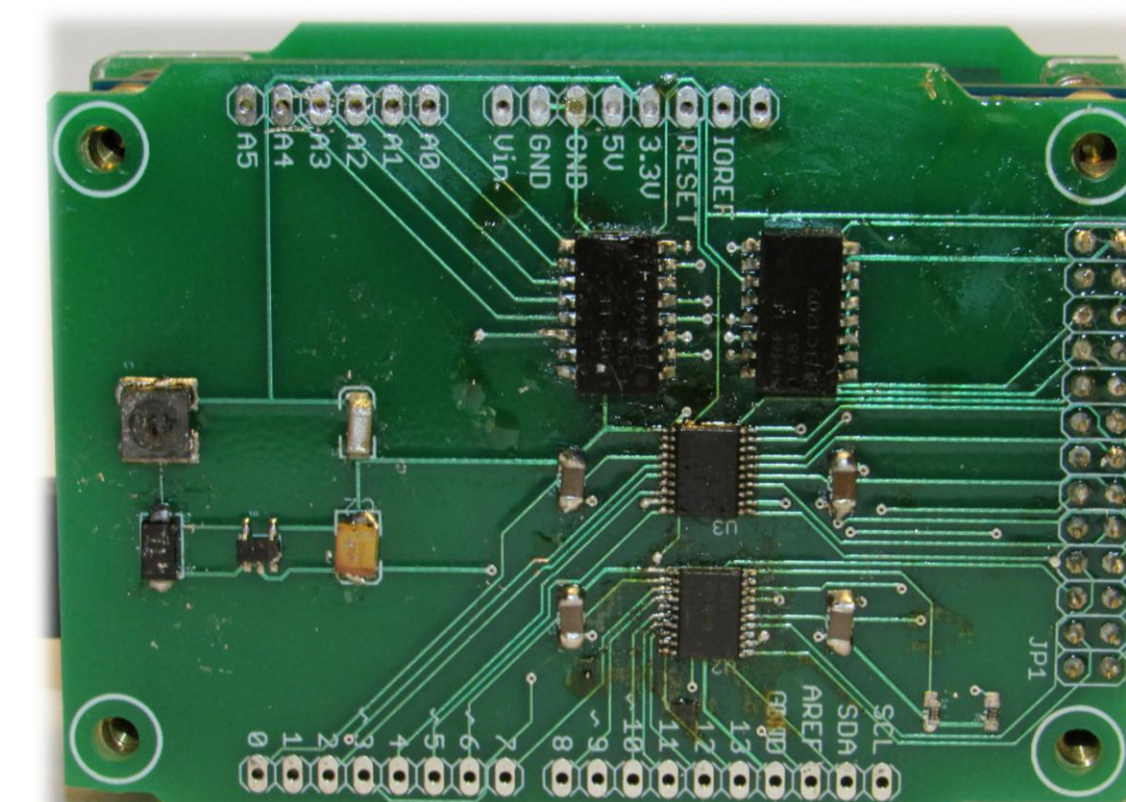
Acknowledgements

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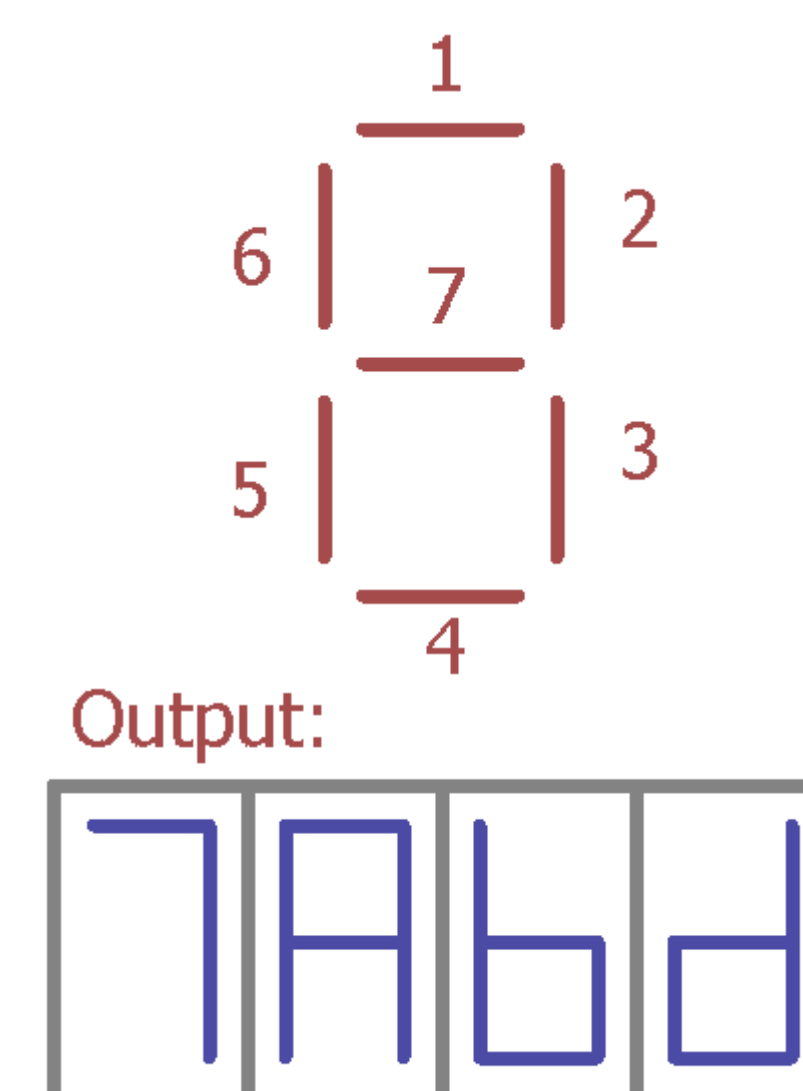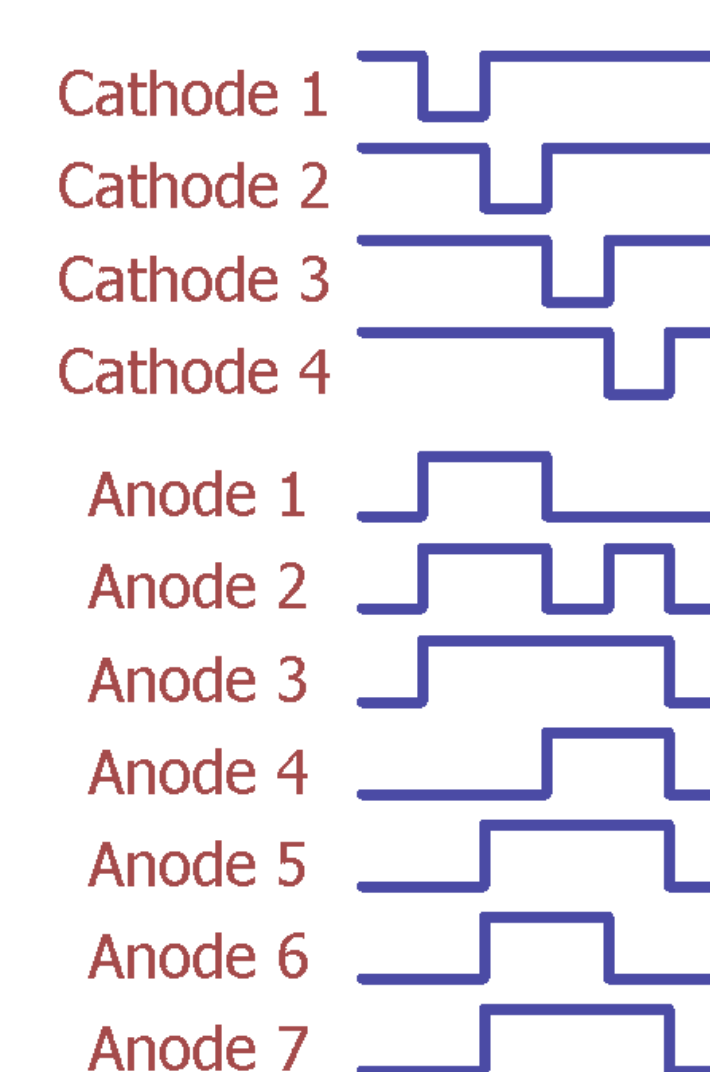
PCB Layouts

• Top Board: All-purpose debug shield

• Bottom Board: Arduino adapter

7-Segment Display Driver

• Features hardware multiplexing which can be set to any pin
• GPIO pins drive cathodes to GND to light up one number at a time
• Anodes determine the number displayed

Cathode 1
Cathode 2
Cathode 3
Cathode 4

Anode 1
Anode 2
Anode 3
Anode 4
Anode 5
Anode 6
Anode 7

Output:

I/O Memory Map

• The processor treats I/O devices such as buttons and switches as memory
• Processor gives a 32-bit address which is more than the RAM
• Therefore, we fill in empty parts of the memory space with I/O devices

GPIO[80:1]   UART connection   Instruction Memory
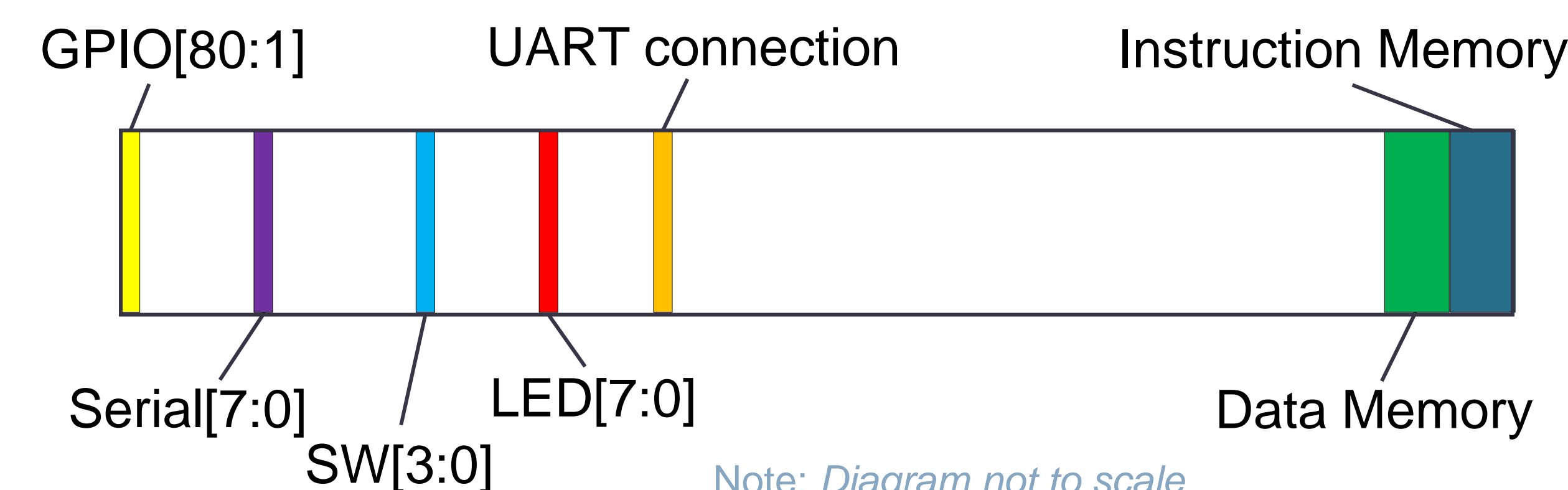
Serial[7:0]   LED[7:0]   Data Memory
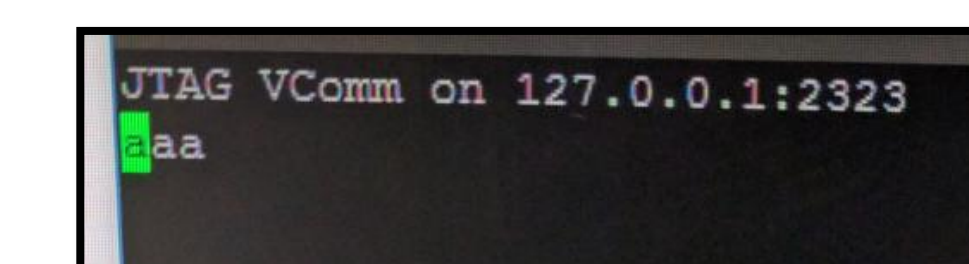SW[3:0]   Note: *Diagram not to scale*

Example Programs

• Hello World/Key test
  • Prints 'PRESS.KEY' on the 7-segments
  • Prints 'FABULOUS' when the user complies
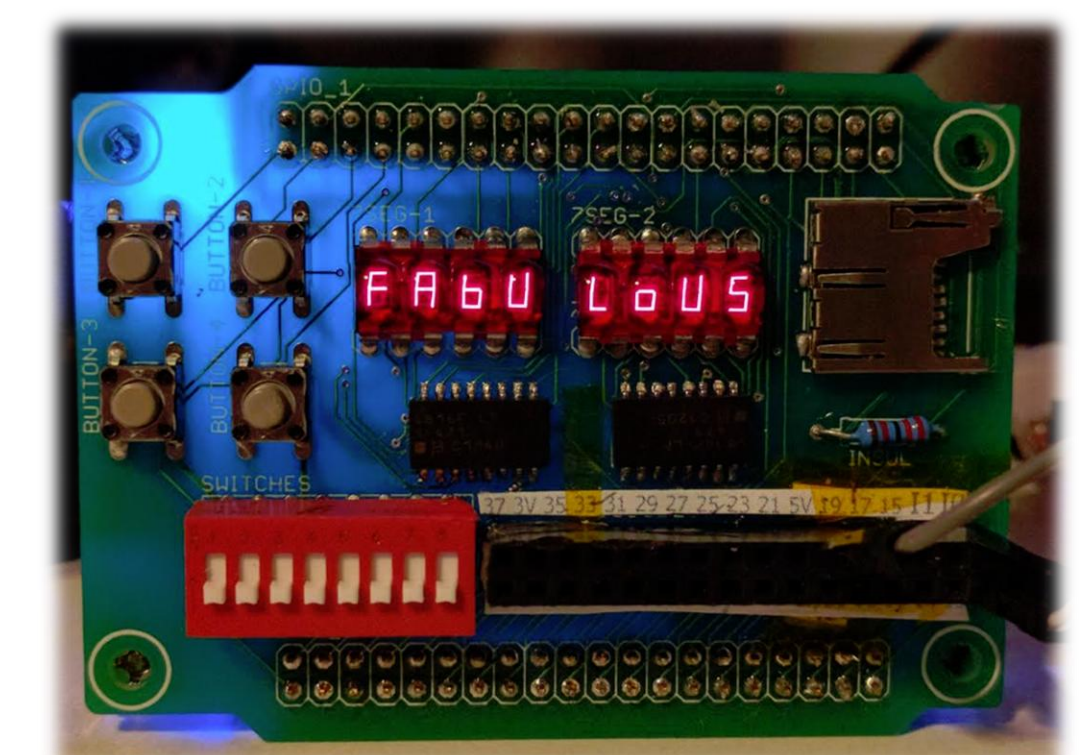
• Countdown
  • Displays a number in the 7-segment display.
  • Key 1 adds 1 to the number, Key 2 adds 10, and so on.
  • Pulling a switch makes the number count down. More switches = faster
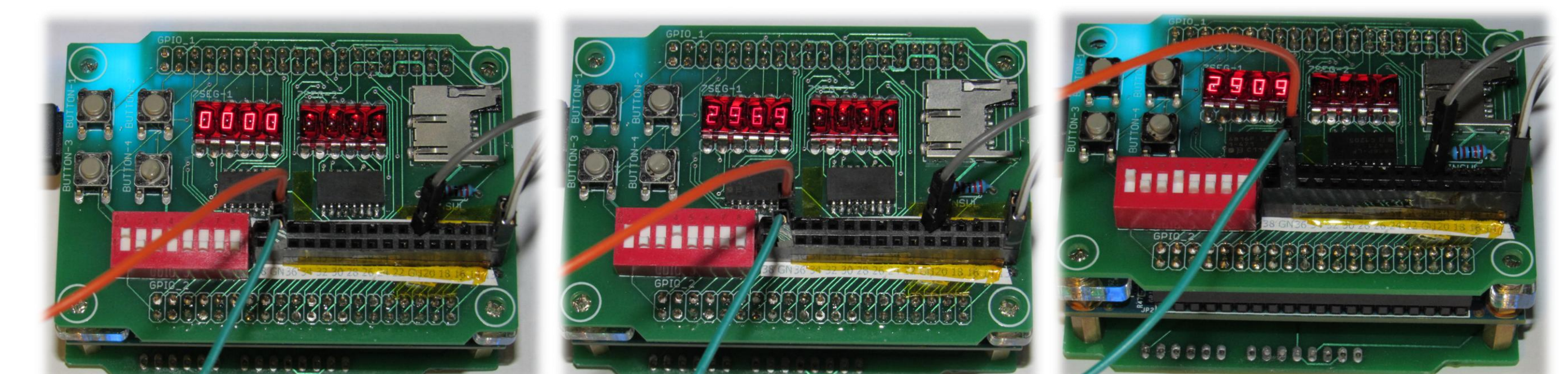
• Console
  • Receives bits written to a console in PuTTY and displays them on the 7segs
  • Sends the word "Ping" to PuTTY when a button is pressed

JTAG VComm on 127.0.0.1:2323
aa

127.0.0.1 - PuTTY
JTAG VComm on 127.0.0.1:2323
PING
        PING
                PING
                        PING

Block Diagram

A diagram of the internal architecture:

Read FIFO

Top.sv – 'Motherboard'

Virtual JTAG Module

Processor

SDRAM Control

SDRAM

GPIO

Serial

Other I/O

JTAG   De0-Nano   Pins   Hardware