Polar

Layer	Stack up	Description	Type	Base Thickness	Processed Thickness	εr	Copper Coverage	Mask Thickness	
1				0.689	2.067		100.000		
		Rogers 4835 4mil coreH/1 Low Pro	Rogers 4835	4.000	4.000	3.480			
2				1.260	1.260		73.000		
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.830	3.700			
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.830	3.700			
3				1.260	1.260		69.000		
		Iteq IT180A 28 mil core 1/1	FR4	28.000	28.000	4.280			
4				1.260	1.260		48.000		
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.691	3.700			
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.691	3.700			
5				1.260	1.260		72.000		
		Iteq IT180A 4 mil core 1/H	FR4	4.000	4.000	3.790			
6				0.689	2.067		100.000		

(Stackup diagram overall height: 56.21)

Copper Thickness = 9.173 |Dielectric Thickness = 47.041 |Solder Mask Thickness = 0.000 |Stack Up Thickness = 56.214 |Stack Up Thickness with Soldermask = 56.214 |
Stack Up Cost = 0.00 |

Impedance ID	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)	
1	Edge Coupled Surface Microstrip 1B	1	2	0	5.200	5.000	0.000	102.650	102.650	10.000	
2	Surface Coplanar Strips With Lower Ground 1B	1	2	0	7.080	0.000	8.000	51.680	51.680	10.000	
3	Surface Coplanar Strips With Lower Ground 1B	1	2	0	6.979	0.000	5.061	50.000	50.000	10.000	
4	Edge Coupled Surface Microstrip 1B	6	5	0	5.661	6.339	0.000	100.000	100.000	10.000	

Notes

StackName: tessolve-ar1243-rf-evm2-reva	Version:	Revision:	Modification:	Date of Revision:	Editor	
Date: 13/02/2k16	Associated Documents: CAM No: F13022k16-31609					Page 1/1
Author:						
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