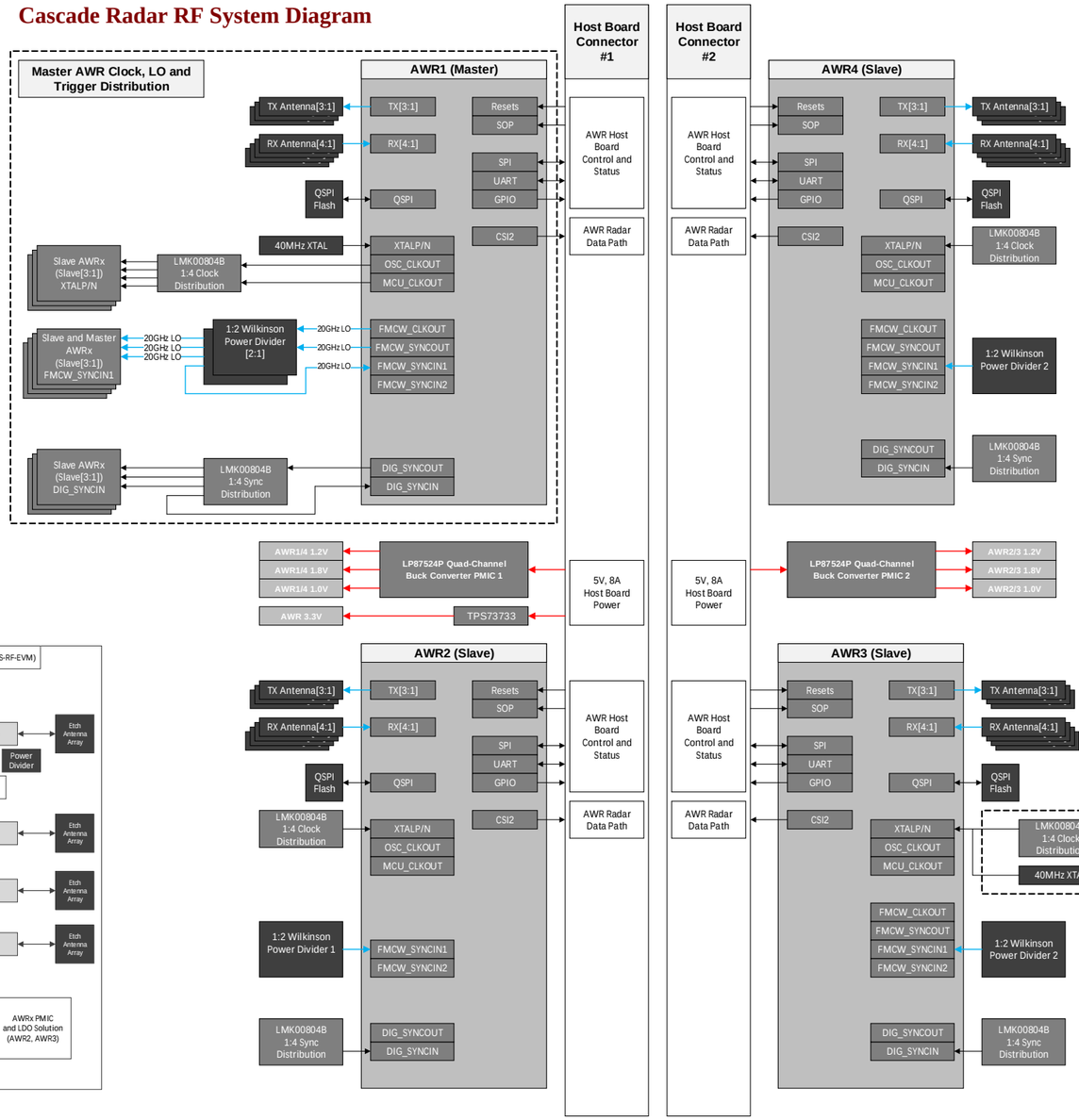
mmWave Cascade Radar RF Board (MMWCAS-RF-EVM)

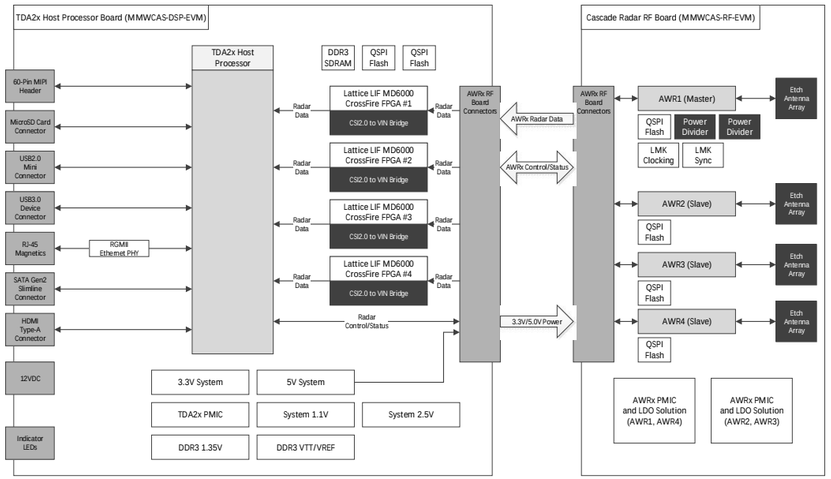
System Description

	Cascade Radar RF Board
4x AWRx 76-81GHz Radar SoC	Integrated VCO, LO distribution, PA, LNA, ADC, 3 TX and 4 RX ARM MCU R4 Controller
AWR RF Peripherals	
12x TX, 16x RX Antennas	12 total transmitters across all 4 AWRx devices 16 total receivers across all 4 AWRx devices
Embedded Antenna	4-element series-fed patch antenna
20 GHz LO Star Distribution	2x Wilkinson Power dividers fed by the Master AWRx device LO output to Slave AWRx devices
AWR Digital Peripherals	
CSI2.0 4-lane	600Mbps/Lane for 2.4Gbps ADC IF data per device
QSPI Flash	16Mbit QSPI flash for AWR firmware updates
Serial Peripherals	SPI, I2C, UART, GPIO
System Temperature	TMP112 I2C Temperature Sensors
Power	
Radar Power Management IC (PMIC) Solution	2x LP87524P Quad-Channel, Integrated FET, Buck Converters and LC filtering solution

Cascade Radar RF System Diagram



Cascade Radar Evaluation Kit Diagram



PROC054D_System_Top.SchDoc
CASCADE_RF_BOARD

PROC054D_EVM_Hardware.SchDoc
EVM_HARDWARE

PROC054D_Revision_History.SchDoc
REVISION_HISTORY

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Number: PROC054 Rev: D	Sheet Title: Coversheet	
Sync Rev: d2c440fc4a5768bc733d2b6e37e1d8b5d73	Sheet:1 of 19	
Drawn By:a0271760	File: PROC054D_Coversheet.SchDoc	Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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Cascade Radar RF Board - Top Level Schematic

AWR_1 (Master)

AWR_1
PROC054D_AWR_Interfaces.SchDoc

AWR_1
PROC054D_AWR_Pull_Resistors.SchDoc

AWR_1
PROC054D_AWR_Power_Decoupling.SchDoc

AWR_3 (Slave)

AWR_3
PROC054D_AWR_Interfaces.SchDoc

AWR_3
PROC054D_AWR_Pull_Resistors.SchDoc

AWR_3
PROC054D_AWR_Power_Decoupling.SchDoc

HOST_CONNECTORS
PROC054D_Host_Connector.SchDoc

System Power/Reset

SYSTEM_POWER
PROC054D_System_Power.SchDoc

40MHz Generation/Distribution

40MHZ_CLOCK
PROC054D_40MHZ_Clock.SchDoc

Digital Sync and 20GHZ LO

DIG_SYNC_LO_20GHZ
PROC054D_FMCW_Sync.SchDoc

AWR_2 (Slave)

AWR_2
PROC054D_AWR_Interfaces.SchDoc

AWR_2
PROC054D_AWR_Pull_Resistors.SchDoc

AWR_2
PROC054D_AWR_Power_Decoupling.SchDoc

AWR_4 (Slave)

AWR_4
PROC054D_AWR_Interfaces.SchDoc

AWR_4
PROC054D_AWR_Pull_Resistors.SchDoc

AWR_4
PROC054D_AWR_Power_Decoupling.SchDoc

System LED Indicators

SYSTEM_LED_INDICATORS
PROC054D_System_LED.SchDoc

System Temperature Sensors

SYSTEM_TEMP_SENSORS
PROC054D_Temp_Sensor.SchDoc

System Test Connectors And Termination

SYSTEM_TEST_CONN_TERMINATION
PROC054D_SMA_SMP_Connectors.SchDoc

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Number: PROC054	Rev: D	Sheet Title: System Top	
		Assembly Variant: 001	Sheet: 2 of 19
Drawn By: a0271760		File: PROC054D_System_Top.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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Cascade RF System Power

References

4-A + 2.5-A + Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

PMIC #1 - Master AWR_1 and Slave AWR_4

AWR_1_AWR_4_LP87524P
PROC054D_AWR_1_AWR_4_LP87524P.SchDoc

PMIC_NRST
PMIC1_CLKIN
PMIC_BUCK_EN
PMIC1_I2C
PMIC1_SCL
PMIC1_SDA
PMIC1_PGOOD
PMIC1_GPIO2
PMIC1_AWR_14_1V2
PMIC1_AWR_14_1V8
PMIC1_AWR_1_1V0
PMIC1_AWR_4_1V0

LC Filtering, Ferrite Filtering AWR_1 and AWR_4

AWR_1_AWR_4_LC_Filtering
PROC054D_AWR_1_AWR_4_LC_Filtering.SchDoc

AWR_1_1V2_FILT
AWR_4_1V2_FILT
AWR_1_1V8_FILT
AWR_4_1V8_FILT
AWR_1_1V0_RF1_FILT
AWR_1_1V0_RF2_FILT
AWR_4_1V0_RF1_FILT
AWR_4_1V0_RF2_FILT

SYSTEM_PGOOD
R204 0 PMIC1_PGOOD
R205 0 PMIC2_PGOOD

Note: PMIC PGOOD open-drain, active-high output.

PMIC #2 - Master AWR_2 and Slave AWR_3

AWR_2_AWR_3_LP87524P
PROC054D_AWR_2_AWR_3_LP87524P.SchDoc

PMIC2_CLKIN
PMIC_BUCK_EN
PMIC2_I2C
PMIC2_SCL
PMIC2_SDA
PMIC2_TMPSNS_SCL
PMIC2_TMPSNS_SDA
PMIC2_PGOOD
PMIC2_AWR_23_1V2
PMIC2_AWR_23_1V8
PMIC2_AWR_2_1V0
PMIC2_AWR_3_1V0

LC Filtering, Ferrite Filtering AWR_2 and AWR_3

AWR_2_AWR_3_LC_Filtering
PROC054D_AWR_2_AWR_3_LC_Filtering.SchDoc

AWR_2_1V2_FILT
AWR_3_1V2_FILT
AWR_2_1V8_FILT
AWR_3_1V8_FILT
AWR_2_1V0_RF1_FILT
AWR_2_1V0_RF2_FILT
AWR_3_1V0_RF1_FILT
AWR_3_1V0_RF2_FILT

3.3V System LDO

SYSTEM_3V3_SUPPLY
PROC054D_System_3V3_Supply.SchDoc
TLV702_EN

AWR_1 Reset Generation

Note: Allowing either host or PMIC to toggle NRST low.

SYSTEM_3V3
SYSTEM_PGOOD
AWR_1_NRST_HOST
R189 100 SYSTEM_PGOOD1_GS
R191 100 AWR_1_NRST_HOST_GS
R86 10.0k
R87 10.0k
R206 10.0k
U6A
SN74LVC1G08QDBVRQ1
R208 0 AWR_1_NRST
C205 50V 0.1uF
U6B
C162 16V 0.1uF
GND

AWR_2 Reset Generation

Note: Allowing either host or PMIC to toggle NRST low.

SYSTEM_3V3
SYSTEM_PGOOD
AWR_2_NRST_HOST
R212 100 SYSTEM_PGOOD2_GS
R190 100 AWR_2_NRST_HOST_GS
R88 10.0k
R89 10.0k
R207 10.0k
U11A
SN74LVC1G08QDBVRQ1
R209 0 AWR_2_NRST
C206 50V 0.1uF
U11B
C163 16V 0.1uF
GND

AWR_3 Reset Generation

Note: Allowing either host or PMIC to toggle NRST low.

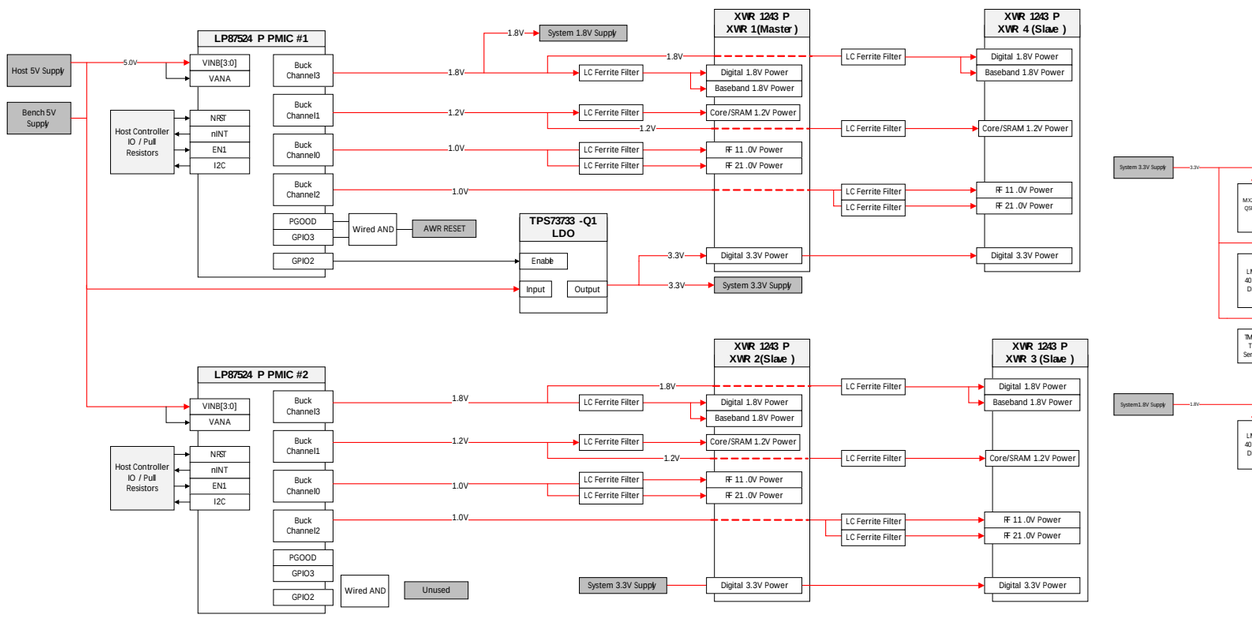
SYSTEM_3V3
SYSTEM_PGOOD
AWR_3_NRST_HOST
R38 100 SYSTEM_PGOOD3_GS
R53 100 AWR_3_NRST_HOST_GS
R90 10.0k
R91 10.0k
R37 10.0k
U12A
SN74LVC1G08QDBVRQ1
R211 0 AWR_3_NRST
C94 50V 0.1uF
U12B
C164 16V 0.1uF
GND

AWR_4 Reset Generation

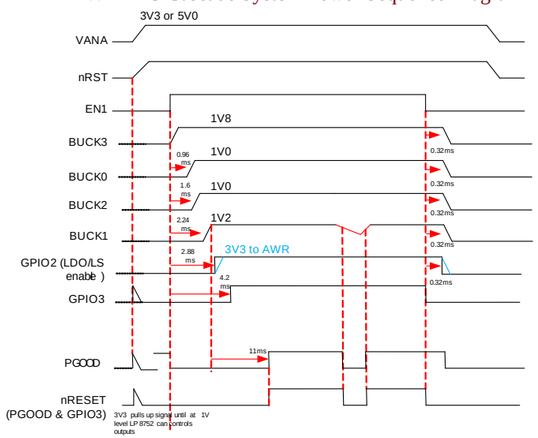
Note: Allowing either host or PMIC to toggle NRST low.

SYSTEM_3V3
SYSTEM_PGOOD
AWR_4_NRST_HOST
R62 100 SYSTEM_PGOOD4_GS
R77 100 AWR_4_NRST_HOST_GS
R92 10.0k
R93 10.0k
R61 10.0k
U13A
SN74LVC1G08QDBVRQ1
R210 0 AWR_4_NRST
C149 50V 0.1uF
U13B
C165 16V 0.1uF
GND

AWR1243 Cascade System Power Diagram



AWR1243 Cascade System Power Sequence Diagram



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TID #: N/A		Project Title:MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: System Power	
Board Rev:		Assembly VAWRiant:	Sheet:3 of 19
Drawn By:a0271760		File: PROC054D_System_Power.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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LP87524P Quad-Channel Synchronous Buck PMIC - Master AWR_1 and Slave AWR_4

References

4-A + 2.5-A + Two 1.5-A BLP875241-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

LP8752x input filtering, bulk and decoupling capacitance

SYSTEM_5V0
L9 BLM21PG300SH1D
PMIC1_VIN_B0
C39 6.8nF 100V
C40 6.3V 100uF (DNP)
C41 6.3V 100uF (DNP)
C42 16V 0.1µF
C43 10V 10µF
GND

SYSTEM_5V0
L10 BLM21PG300SH1D
PMIC1_VIN_B1
C44 6.8nF 100V
C45 6.3V 100uF (DNP)
C46 6.3V 100uF (DNP)
C47 16V 0.1µF
C48 10V 10µF
GND

SYSTEM_5V0
L11 BLM21PG300SH1D
PMIC1_VIN_B2
C51 6.8nF 100V
C52 6.3V 100uF (DNP)
C53 6.3V 100uF (DNP)
C54 16V 0.1µF
C55 10V 10µF
GND

SYSTEM_5V0
L12 BLM21PG300SH1D
PMIC1_VIN_B3
C56 6.8nF 100V
C57 6.3V 100uF (DNP)
C58 6.3V 100uF (DNP)
C59 16V 0.1µF
C60 10V 10µF
GND

LP8752x Output snubber RC filter

PMIC1_SW_B0 — C37 50V 390pF — R39 3.9 — GND
PMIC1_SW_B1 — C38 50V 390pF — R40 3.9 — GND
PMIC1_SW_B2 — C49 50V 390pF — R41 3.9 — GND
PMIC1_SW_B3 — C50 50V 390pF — R42 3.9 — GND

PMIC_NRST ↔ PMIC_NRST — TP4
PMIC1_CLKIN ↔ AWR_1_PMIC_CLKOUT — TP5
PMIC_BUCK_EN ↔ PMIC_BUCK_EN — TP6
PMIC1_GPIO2 ↔ PMIC1_GPIO2 — TP7
PMIC1_SCL ↔ PMIC1_SCL — TP9
PMIC1_SDA ↔ PMIC1_SDA — TP10
PMIC1_PGOOD — PMIC1_PGOOD — R96 0 PMIC1_PGOOD_RS — TP11
R73 0 PMIC1_GPIO3

PMIC1_AWR_1_1V0 ↔ PMIC1_AWR_1_1V0
PMIC1_AWR_14_1V2 ↔ PMIC1_AWR_14_1V2
PMIC1_AWR_4_1V0 ↔ PMIC1_AWR_4_1V0
PMIC1_AWR_14_1V8 ↔ PMIC1_AWR_14_1V8

SYSTEM_5V0 — R44 0 — PMIC1_VANA
LP87524 VANA input capacitance
C63 16V 0.1µF — GND

ClassName: SYSTEM_5V_INPUT
ClassName: PMIC_OUTPUT
U3

PMIC1_VIN_B0	9	VIN_B0	SW_B0 10 — PMIC1_SW_B0
PMIC1_VIN_B1	13	VIN_B1	FB_B0 8 — PMIC1_FB_B0
PMIC1_VIN_B2	26	VIN_B2	SW_B1 12 — PMIC1_SW_B1
PMIC1_VIN_B3	22	VIN_B3	FB_B1 14 — PMIC1_FB_B1
TP14 — PMIC1_VANA	18	VANA	SW_B2 25 — PMIC1_SW_B2
PMIC_NRST	20	RST	FB_B2 1 — PMIC1_FB_B2
AWR_1_PMIC_CLKOUT	3	CLKIN	SW_B3 23 — PMIC1_SW_B3
PMIC1_INTN	19	INT	FB_B3 21 — PMIC1_FB_B3
PMIC1_PGOOD_RS	16	PGOOD	PGND_B01 11
PMIC_BUCK_EN	7	EN1	PGND_B23 24
PMIC1_GPIO2	15	EN2	AGND 17
PMIC1_GPIO3	2	EN3	AGND 4
PMIC1_SCL	5	SCL	AGND 27
PMIC1_SDA	6	SDA	

LP87524PRNFTQ1

ClassName: PMIC_CONTROL

SYSTEM_3V3
LP87524 I2C Open-drain only 3.6V max compatible
R46 4.7k
R47 4.7k

LP87524 Buck-Converter Channels
SW0 - AWRx 1.0V RF
SW1 - AWRx/y 1.2V Core Digital
SW2 - AWRy 1.0V RF
SW3 - AWRx/y 1.8V Analog/Digital

ClassName: AWR1_POWER_RF
L13 470nH — PMIC1_SW_B0 — PMIC1_AWR_1_1V0 — R43 0 — PMIC1_FB_B0
AWR1 1.0V RF1/RF2 - 3A Max
C61 10V 22uF — C62 10V 22uF — GND

ClassName: AWR14_POWER_1V2
L14 470nH — PMIC1_SW_B1 — PMIC1_AWR_14_1V2 — R45 0 — PMIC1_FB_B1
AWR1/4 1.2V Core/SRAM - 1.5A Max
C64 10V 22uF — C65 10V 22uF — GND

ClassName: AWR4_POWER_RF
L15 470nH — PMIC1_SW_B2 — PMIC1_AWR_4_1V0 — R48 0 — PMIC1_FB_B2
AWR4 1.0V RF1/RF2 - 3A Max
C66 10V 22uF — C67 10V 22uF — GND

ClassName: AWR14_POWER_1V8
L16 470nH — PMIC1_SW_B3 — PMIC1_AWR_14_1V8 — R52 0 — PMIC1_FB_B3
AWR1/4 1.8V Baseband and Digital I/O - 2.5A Max
C68 10V 22uF — C69 10V 22uF — GND

LP87524 default pull resistors

RSTN - Pulled to 5.0V after SYSTEM_5V power on. Can be driven low by host.

CLKIN - Digital input, default pull-down. Can be driven by AWR

INTN - Open-drain, active-low interrupt output for host. De-asserted by pull-up to 3.3V after SYSTEM_3V3 power on.

PGOOD/GPIO3 - Open-drain, active-high output. Shorted together in wired AND. Pulled to PMIC_3V3 after all LP87524 rails active and additional delay.

BUCK_EN1 - Digital input, pull-ed up to 5.0V after power on to stAWRt LP87524 stAWRtup sequence. Can be driven low by host to stAWRt shutdown sequence.

GPIO2 - Digital ouput, default pull-down. Used by LP87524 to driv SYSTEM_3V3 LDO enable.

PMIC1_3V3
R94 10.0k — PMIC_NRST
R54 10.0k — AWR_1_PMIC_CLKOUT
R49 10.0k — PMIC1_INTN
R56 10.0k — PMIC1_PGOOD_RS
R50 10.0k — PMIC_BUCK_EN
R51 10.0k — PMIC1_GPIO2
R55 10.0k — PMIC1_GPIO3
R57 10.0k
R58 10.0k
GND

SYSTEM_5V0
R34 1.00
PMIC1_3V3
R36 1.96k
GND

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Scale: NONE	Rev:	Assembly VAWRiant:	Sheet: 4 of 19
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LP87524P Quad-Channel Synchronous Buck PMIC - Slave AWR_2 and Slave AWR_3

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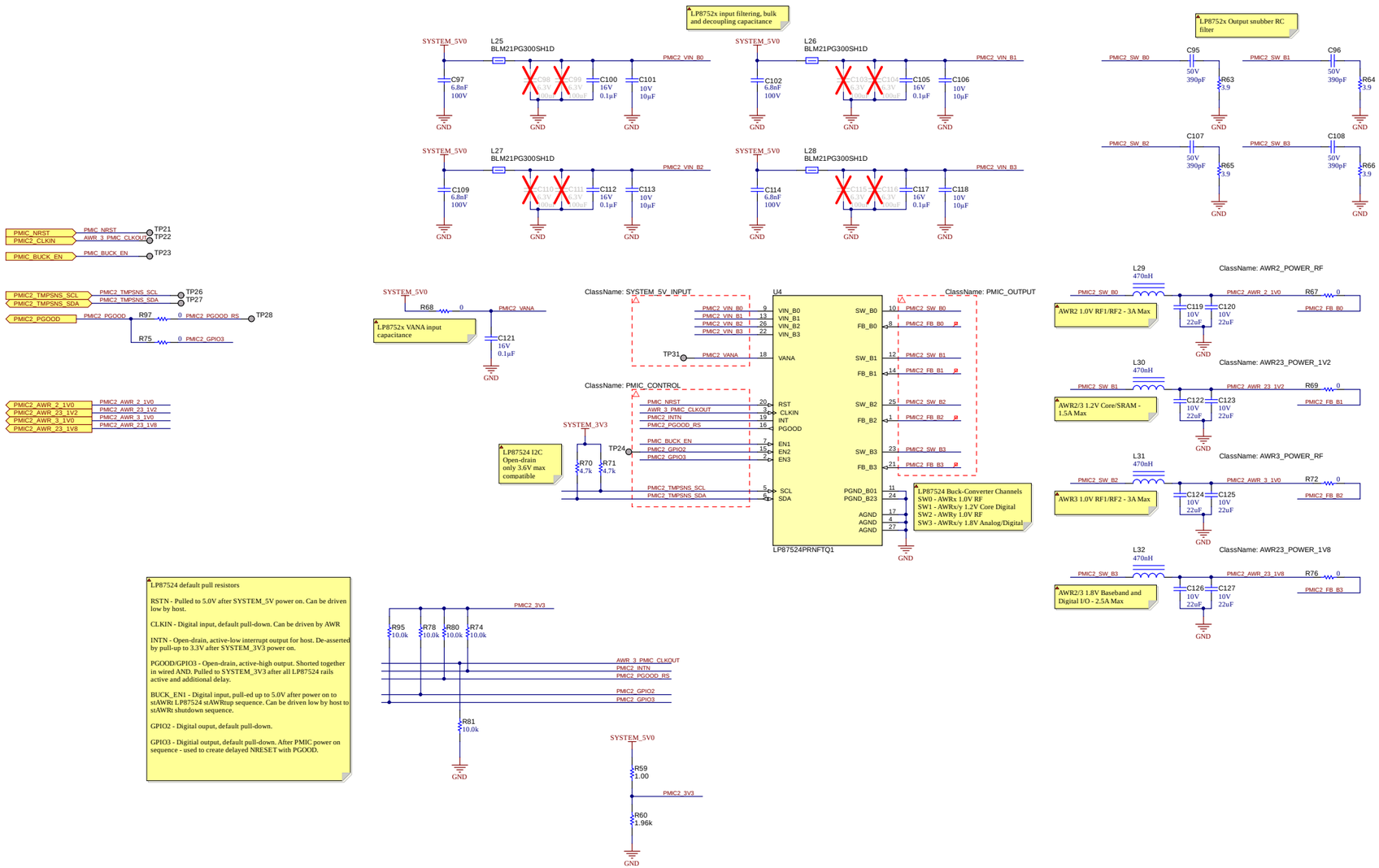

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AWR Power Filtering and Decoupling - Master AWR_1 and Slave AWR_4

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XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

PMIC1_AWR_14_1V2 → PMIC1_AWR_14_1V2
PMIC1_AWR_14_1V8 → PMIC1_AWR_14_1V8
PMIC1_AWR_1_1V0 → PMIC1_AWR_1_1V0
PMIC1_AWR_4_1V0 → PMIC1_AWR_4_1V0

AWR_1_1V2_FILT → AWR_1_1V2_FILT
AWR_4_1V2_FILT → AWR_4_1V2_FILT
AWR_1_1V8_FILT → AWR_1_1V8_FILT
AWR_4_1V8_FILT → AWR_4_1V8_FILT
AWR_1_1V0_RF1_FILT → AWR_1_1V0_RF1_FILT
AWR_1_1V0_RF2_FILT → AWR_1_1V0_RF2_FILT
AWR_4_1V0_RF1_FILT → AWR_4_1V0_RF1_FILT
AWR_4_1V0_RF2_FILT → AWR_4_1V0_RF2_FILT

LP87524P PMIC switcher LC ripple filtering and decoupling for AWR1 and AWR4

L1 NLCV32T-R10M-EFRD 100nH
PMIC1_AWR_14_1V2 → AWR_1_1V2_FILT
ClassName: AWR_1_POWER_1V2
1.2V Digital Core/SRAM AWR1/AWR4
C10 10V 10uF
C11 10V 22uF
C12 10V 10uF
C13 16V 1µF
GND

L3 NLCV32T-R10M-EFRD 100nH
PMIC1_AWR_14_1V2 → AWR_4_1V2_FILT
ClassName: AWR_4_POWER_1V2
1.2V Digital Core/SRAM AWR1/AWR4
C161 10V 10uF
C21 10V 22uF
C29 10V 10uF
C78 16V 1µF
GND

L2 NLCV32T-R10M-EFRD 100nH
PMIC1_AWR_14_1V8 → AWR_1_1V8_FILT
ClassName: AWR_1_POWER_1V8
1.8V Digitial I/O and Analog Baseband AWR1/AWR4
C14 10V 10uF
C15 10V 22uF
C16 10V 10uF
C17 16V 1µF
GND

L6 NLCV32T-R10M-EFRD 100nH
PMIC1_AWR_14_1V8 → AWR_4_1V8_FILT
ClassName: AWR_4_POWER_1V8
1.8V Digitial I/O and Analog Baseband AWR1/AWR4
C86 10V 10uF
C150 10V 22uF
C151 10V 10uF
C152 16V 1µF
GND

L4 NLCV32T-R10M-EFRD 100nH
PMIC1_AWR_1_1V0 → AWR_1_1V0_RF1_FILT
ClassName: AWR_1_POWER_1V0_RF
1.0V Analog RF AWR1
C25 10V 10uF
C22 10V 22uF
C23 10V 10uF
C26 16V 1µF
GND

L5 NLCV32T-R10M-EFRD 100nH
AWR_1_1V0_RF2_FILT
ClassName: AWR_1_POWER_1V0_RF
C27 10V 10uF
C24 10V 22uF
C32 10V 10uF
C28 16V 1µF
GND

L7 NLCV32T-R10M-EFRD 100nH
PMIC1_AWR_4_1V0 → AWR_4_1V0_RF1_FILT
ClassName: AWR_4_POWER_RF
1.0V Analog RF AWR4
C33 10V 10uF
C30 10V 22uF
C31 10V 10uF
C34 16V 1µF
GND

L8 NLCV32T-R10M-EFRD 100nH
AWR_4_1V0_RF2_FILT
ClassName: AWR_4_POWER_RF
C35 10V 10uF
C81 10V 22uF
C89 10V 10uF
C36 16V 1µF
GND

ClassName: SYSTEM_1V8
PMIC1_AWR_14_1V8 → R35 0 → SYSTEM_1V8
C18 10V 22uF
C19 10V 10uF
C20 16V 1µF
GND

AWR_1 1.8V supply also generates SYSTEM_1V8
- LMK00804B clock distribution
- LMK00804B sync distribution

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Orderable: MMW_CAS_RF_EVM		Designed for: Public Release	Mod. Date: 1/17/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: AWR_1_AWR_4_LC_Filtering	
Sys Rev:		Assembly VAWRiant:	Sheet: 6 of 19
Drawn By: a0271760		File: PROC054D_AWR_1_AWR_4_LC_Filtering.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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AWR1243 Power Filtering and Decoupling - Master AWR_2 and Slave AWR_3

References

4-A + 2.5-A + Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

PMIC2_AWR_23_1V2 → PMIC2_AWR_23_1V2
PMIC2_AWR_23_1V8 → PMIC2_AWR_23_1V8
PMIC2_AWR_2_1V0 → PMIC2_AWR_2_1V0
PMIC2_AWR_3_1V0 → PMIC2_AWR_3_1V0

AWR_2_1V2_FILT → AWR_2_1V2_FILT
AWR_3_1V2_FILT → AWR_3_1V2_FILT
AWR_2_1V8_FILT → AWR_2_1V8_FILT
AWR_3_1V8_FILT → AWR_3_1V8_FILT
AWR_2_1V0_RF1_FILT → AWR_2_1V0_RF1_FILT
AWR_2_1V0_RF2_FILT → AWR_2_1V0_RF2_FILT
AWR_3_1V0_RF1_FILT → AWR_3_1V0_RF1_FILT
AWR_3_1V0_RF2_FILT → AWR_3_1V0_RF2_FILT

LP87524P PMIC switcher LC ripple filtering and decoupling for AWR2

PMIC2_AWR_23_1V2 → L17 NLCV32T-R10M-EFRD 100nH → AWR_2_1V2_FILT
ClassName: AWR_2_POWER_1V2
1.2V Digital Core/SRAM AWR2
C70 10V 10uF → GND
C71 10V 22uF → GND
C72 10V 10uF
C73 16V 1µF

LP87524P PMIC switcher LC ripple filtering and decoupling for AWR3

PMIC2_AWR_23_1V2 → L19 NLCV32T-R10M-EFRD 100nH → AWR_3_1V2_FILT
ClassName: AWR_3_POWER_1V2
1.2V Digital Core/SRAM AWR3
C153 10V 10uF → GND
C154 10V 22uF → GND
C155 10V 10uF
C156 16V 1µF

PMIC2_AWR_23_1V8 → L18 NLCV32T-R10M-EFRD 100nH → AWR_2_1V8_FILT
ClassName: AWR_3_POWER_1V8
1.8V Digitial I/O and Analog Baseband AWR2
C74 10V 10uF → GND
C75 10V 22uF → GND
C76 10V 10uF
C77 16V 1µF

PMIC2_AWR_23_1V8 → L22 NLCV32T-R10M-EFRD 100nH → AWR_3_1V8_FILT
ClassName: AWR_3_POWER_1V8
1.8V Digitial I/O and Analog Baseband AWR3
C157 10V 10uF → GND
C158 10V 22uF → GND
C159 10V 10uF
C160 16V 1µF

PMIC2_AWR_2_1V0 → L20 NLCV32T-R10M-EFRD 100nH → AWR_2_1V0_RF1_FILT
ClassName: AWR_2_POWER_1V0_RF
1.0V Analog RF AWR2
C82 10V 10uF → GND
C79 10V 22uF → GND
C80 10V 10uF
C83 16V 1µF

L21 NLCV32T-R10M-EFRD 100nH → AWR_2_1V0_RF2_FILT
ClassName: AWR_2_POWER_1V0_RF
C84 10V 10uF → GND
C166 10V 22uF → GND
C201 10V 10uF
C85 16V 1µF

PMIC2_AWR_3_1V0 → L23 NLCV32T-R10M-EFRD 100nH → AWR_3_1V0_RF1_FILT
ClassName: AWR_3_POWER_RF
1.0V Analog RF AWR3
C90 10V 10uF → GND
C87 10V 22uF → GND
C88 10V 10uF
C91 16V 1µF

L24 NLCV32T-R10M-EFRD 100nH → AWR_3_1V0_RF2_FILT
ClassName: AWR_3_POWER_RF
C92 10V 10uF → GND
C204 10V 22uF → GND
C207 10V 10uF
C93 16V 1µF

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Orderable: MMW_CAS_RF_EVM	Designed for:Public Release — Mod. Date: 1/17/2020
TID #: N/A	Project Title: MMWCAS-RF-EVM
Number: PROC054 — Rev: D	Sheet Title: AWR_2_AWR_3_LC_Filtering
Custom Rev:	Assembly VAWRiant: — Sheet: 7 of 19
Drawn By: a0271760	File: PROC054D_AWR_2_AWR_3_LC_Filtering.SchDoc — Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave

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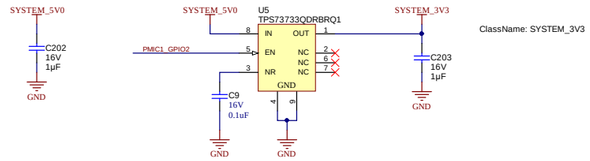
System 3.3V Supply

References

TLV70028EVM-463 Evaluation Module
TPS22965 Evaluation Module

TPS73733-Q1 5.0V to 3.3V LDO - System 3.3V Power



ClassName: SYSTEM_3V3

TLV702_EN — PMIC1_GPIO2

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 1/17/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: System_3V3_Supply	
Custom Rev:		Assembly VAWRiant:	Sheet:8 of 19
Drawn By:a0271760		File: PROC054D_System_3V3_Supply.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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Host to RF Board Connectors

ClassName: AWR_1_GENERAL

AWR_1_GPIO_0
AWR_1_GPIO_1
AWR_1_GPIO_2
AWR_1_SPI_MISO1
AWR_1_SPI_HOST_INTR1
AWR_1_SPI_CS1
AWR_1_SPI_MOSI1
AWR_1_SPI_CLK1
AWR_1_UART_RX
AWR_1_UART_TX
AWR_1_MSS_LOGGER
AWR_1_BSS_LOGGER

ClassName: AWR_1_SOP_RESET

AWR_1_SOP2_PMICCLKOUT
AWR_1_SOP1_SYNCOUT
AWR_1_SOP0_TDO
AWR_1_NRST_HOST
AWR_1_WARM_RST

ClassName: AWR_1_JTAG

AWR_1_TCK
AWR_1_TMS
AWR_1_TDO
AWR_1_TDI

ClassName: AWR_2_GENERAL

AWR_2_GPIO_0
AWR_2_GPIO_1
AWR_2_GPIO_2
AWR_2_SPI_MISO1
AWR_2_SPI_HOST_INTR1
AWR_2_SPI_CS1
AWR_2_SPI_MOSI1
AWR_2_SPI_CLK1
AWR_2_UART_RX
AWR_2_UART_TX
AWR_2_MSS_LOGGER
AWR_2_BSS_LOGGER

ClassName: AWR2_SOP_RESET

AWR_2_SOP2_PMICCLKOUT
AWR_2_SOP1_SYNCOUT
AWR_2_SOP0_TDO
AWR_2_NRST_HOST
AWR_2_WARM_RST

ClassName: AWR_2_JTAG

AWR_2_TCK
AWR_2_TMS
AWR_2_TDO
AWR_2_TDI

ClassName: AWR_SYNC

EXT_DIG_SYNC
EXT_40MHZ_CLK_1V8

ClassName: AWR_CLOCK

ClassName: PMIC_CONTROL

PMIC_NRST
PMIC1_SCL
PMIC1_SDA
PMIC2_TMPSNS_SDA
PMIC2_TMPSNS_SCL

ClassName: AWR_SAFETY

NERROR_OUT
TMPSNS_ALERT

ClassName: AWR_3_GENERAL

AWR_3_GPIO_2
AWR_3_GPIO_1
AWR_3_GPIO_0
AWR_3_SPI_CLK1
AWR_3_SPI_MOSI1
AWR_3_SPI_CS1
AWR_3_SPI_HOST_INTR1
AWR_3_SPI_MISO1
AWR_3_UART_TX
AWR_3_UART_RX
AWR_3_BSS_LOGGER
AWR_3_MSS_LOGGER

ClassName: AWR_3_SOP_RESET

AWR_3_SOP2_PMICCLKOUT
AWR_3_SOP1_SYNCOUT
AWR_3_SOP0_TDO
AWR_3_NRST_HOST
AWR_3_WARM_RST

ClassName: AWR_3_JTAG

AWR_3_TDI
AWR_3_TDO
AWR_3_TMS
AWR_3_TCK

ClassName: AWR_4_GENERAL

AWR_4_GPIO_2
AWR_4_GPIO_1
AWR_4_GPIO_0
AWR_4_SPI_CLK1
AWR_4_SPI_MOSI1
AWR_4_SPI_CS1
AWR_4_SPI_HOST_INTR1
AWR_4_SPI_MISO1
AWR_4_UART_TX
AWR_4_UART_RX
AWR_4_BSS_LOGGER
AWR_4_MSS_LOGGER

ClassName: AWR_4_SOP_RESET

AWR_4_SOP2_PMICCLKOUT
AWR_4_SOP1_SYNCOUT
AWR_4_SOP0_TDO
AWR_4_NRST_HOST
AWR_4_WARM_RST

ClassName: AWR_4_JTAG

AWR_4_TDI
AWR_4_TDO
AWR_4_TMS
AWR_4_TCK

Host Board Connector 1

ClassName: AWR_1_CSI_LVDS

AWR_1_LVDS_VALID_P
AWR_1_LVDS_VALID_N
AWR_1_LVDS_FRCLK_P
AWR_1_LVDS_FRCLK_N
AWR_1_CSI2_TX3_P
AWR_1_CSI2_TX3_N
AWR_1_CSI2_TX2_P
AWR_1_CSI2_TX2_N
AWR_1_CSI2_CLK_P
AWR_1_CSI2_CLK_N

ClassName: AWR_1_CSI_LVDS

AWR_1_CSI2_TX1_P
AWR_1_CSI2_TX1_N
AWR_1_CSI2_TX0_P
AWR_1_CSI2_TX0_N

ClassName: AWR_2_CSI_LVDS

AWR_2_LVDS_VALID_P
AWR_2_LVDS_VALID_N
AWR_2_LVDS_FRCLK_P
AWR_2_LVDS_FRCLK_N
AWR_2_CSI2_TX3_P
AWR_2_CSI2_TX3_N
AWR_2_CSI2_TX2_P
AWR_2_CSI2_TX2_N
AWR_2_CSI2_CLK_P
AWR_2_CSI2_CLK_N

ClassName: AWR_2_CSI_LVDS

AWR_2_CSI2_TX1_P
AWR_2_CSI2_TX1_N
AWR_2_CSI2_TX0_P
AWR_2_CSI2_TX0_N

TP32 CONN_MONITOR_1 — AWR_1_MCU_CLKOUT — AWR_1_MCU_CLKOUT_CONN

TP12 AWR_CONN_TP1

TP15 AWR_CONN_TP2

J4 — FX23-120P-0.5SV15

1	AWR_1_MCU_CLKOUT	61	AWR_1_GPIO_0	AWR_1_GPIO_0	
2	AWR_1_MCU_CLKOUT_CONN	62	AWR_1_GPIO_1	AWR_1_GPIO_1	
3	AWR_1_LVDS_VALID_P	63	AWR_1_GPIO_2	AWR_1_GPIO_2	
4	AWR_1_LVDS_VALID_N	64	EXT_DIG_SYNC	EXT_DIG_SYNC	
5		65			
6	AWR_1_LVDS_FRCLK_P	66	AWR_1_SPI_MISO1	AWR_1_SPI_MISO1	
7	AWR_1_LVDS_FRCLK_N	67	AWR_1_SPI_HOST_INTR1	AWR_1_SPI_HOST_INTR1	
8	AWR_1_CSI2_TX3_P	68	AWR_1_SPI_CS1	AWR_1_SPI_CS1	
9	AWR_1_CSI2_TX3_N	69	AWR_1_SPI_MOSI1	AWR_1_SPI_MOSI1	
10		70	AWR_1_SPI_CLK1	AWR_1_SPI_CLK1	
11		71			
12	AWR_1_CSI2_TX2_P	72	PMIC1_SCL	PMIC1_SCL	
13	AWR_1_CSI2_TX2_N	73	PMIC1_SDA	PMIC1_SDA	
14		74	EXT_40MHZ_CLK_1V8	EXT_40MHZ_CLK_1V8	
15		75	NERROR_OUT		
16	AWR_1_CSI2_CLK_P	76			
17	AWR_1_CSI2_CLK_N	77	AWR_1_UART_RX	AWR_1_UART_RX	
18		78	AWR_1_UART_TX	AWR_1_UART_TX	
19	AWR_1_CSI2_TX1_P	79	AWR_1_MSS_LOGGER	AWR_1_MSS_LOGGER	
20	AWR_1_CSI2_TX1_N	80	AWR_1_BSS_LOGGER	AWR_1_BSS_LOGGER	
21		81			
22		82	AWR_1_SOP2_PMICCLKOUT		
23		83	AWR_1_SOP1_SYNCOUT		
24	AWR_1_CSI2_TX0_P	84	AWR_1_SOP0_TDO		
25	AWR_1_CSI2_TX0_N	85	AWR_1_NRST_HOST	AWR_1_NRST	
26		86	AWR_1_WARM_RST	AWR_1_WARM_RST	
27		87			
28	AWR_2_LVDS_VALID_P	88	AWR_1_TCK	AWR_1_TCK	
29	AWR_2_LVDS_VALID_N	89	AWR_1_TMS	AWR_1_TMS	
30		90	AWR_1_TDO		
31	AWR_2_LVDS_FRCLK_P	91	AWR_1_TDI	AWR_1_TDI	
32	AWR_2_LVDS_FRCLK_N	92			
33	AWR_2_CSI2_TX3_P	93	AWR_2_SPI_MISO1	AWR_2_SPI_MISO1	
34	AWR_2_CSI2_TX3_N	94	AWR_2_SPI_HOST_INTR1	AWR_2_SPI_HOST_INTR1	
35		95			
36	AWR_2_CSI2_TX2_P	96	AWR_2_SPI_CS1	AWR_2_SPI_CS1	
37	AWR_2_CSI2_TX2_N	97	AWR_2_SPI_MOSI1	AWR_2_SPI_MOSI1	
38		98	AWR_2_SPI_CLK1	AWR_2_SPI_CLK1	
39	AWR_2_CSI2_CLK_P	99			
40	AWR_2_CSI2_CLK_N	100	AWR_2_UART_RX	AWR_2_UART_RX	
41		101	AWR_2_UART_TX	AWR_2_UART_TX	
42	AWR_2_CSI2_TX1_P	102	AWR_2_MSS_LOGGER	AWR_2_MSS_LOGGER	
43	AWR_2_CSI2_TX1_N	103	AWR_2_BSS_LOGGER	AWR_2_BSS_LOGGER	
44		104			
45	AWR_2_CSI2_TX0_P	105	AWR_2_GPIO_0	AWR_2_GPIO_0	
46	AWR_2_CSI2_TX0_N	106	AWR_2_GPIO_1	AWR_2_GPIO_1	
47		107	AWR_2_GPIO_2	AWR_2_GPIO_2	
48		108			
49		109	AWR_2_NRST_HOST	AWR_2_NRST	
50		110	AWR_2_WARM_RST	AWR_2_WARM_RST	
51		111			
52		112	AWR_2_SOP2_PMICCLKOUT		
53		113	AWR_2_SOP1_SYNCOUT		
54		114	AWR_2_SOP0_TDO		
55		115			
56		116	AWR_2_TCK	AWR_2_TCK	
57		117	AWR_2_TMS	AWR_2_TMS	
58		118	AWR_2_TDO		
59		119	AWR_2_TDI	AWR_2_TDI	
60		120	CONN_MONITOR_1		
P1		P3		SYSTEM_5V0	
P2		P4			
MH1		MH2			

GND GND GND GND

C190 10V 47µF
C191 10V 47µF

ClassName: SYSTEM_5V

Bench 5.0V Supply

J6 — 0039300060 Molex

GND_SENSE — SYSTEM_5V0_SENSE — SYSTEM_5V0

C194 10V 47µF

GND GND

5.0V Supply Sense

SYSTEM_5V0 — R — SYSTEM_5V0_SENSE — R — GND_SENSE

GND

GROUND TEST POINTS

TP16 5001 — TP17 5001
TP18 5001 — TP19 5001
TP20 5001 — TP25 5001
TP29 5001 — TP30 5001

GND GND

Ground test points should be distributed across board near major IC

SOP Mode / Functional Mode Signals

AWR_1_TDO	AWR_1_TDO	R147	10.0k	AWR_1_SOP0_TDO
AWR_1_DIG_SYNCOUT	AWR_1_DIG_SYNCOUT	R148	10.0k	AWR_1_SOP1_SYNCOUT
AWR_1_PMIC_CLKOUT	AWR_1_PMIC_CLKOUT	R149	10.0k	AWR_1_SOP2_PMICCLKOUT
AWR_2_TDO	AWR_2_TDO	R151	10.0k	AWR_2_SOP0_TDO
AWR_2_DIG_SYNCOUT	AWR_2_DIG_SYNCOUT	R152	10.0k	AWR_2_SOP1_SYNCOUT
AWR_2_PMIC_CLKOUT	AWR_2_PMIC_CLKOUT	R153	10.0k	AWR_2_SOP2_PMICCLKOUT
AWR_3_TDO	AWR_3_TDO	R155	10.0k	AWR_3_SOP0_TDO
AWR_3_DIG_SYNCOUT	AWR_3_DIG_SYNCOUT	R157	10.0k	AWR_3_SOP1_SYNCOUT
AWR_3_PMIC_CLKOUT	AWR_3_PMIC_CLKOUT	R159	10.0k	AWR_3_SOP2_PMICCLKOUT
AWR_4_TDO	AWR_4_TDO	R161	10.0k	AWR_4_SOP0_TDO
AWR_4_DIG_SYNCOUT	AWR_4_DIG_SYNCOUT	R162	10.0k	AWR_4_SOP1_SYNCOUT
AWR_4_PMIC_CLKOUT	AWR_4_PMIC_CLKOUT	R163	10.0k	AWR_4_SOP2_PMICCLKOUT

Note: Both functional mode and SOP modes of TDO signals are provided at the RF Host Interface connector.

Host device should not simultaneously drive the SOP mode pin and functional pin.

Host Board Connector 2

ClassName: AWR_4_CSI_LVDS

AWR_4_CSI2_TX0_N
AWR_4_CSI2_TX0_P
AWR_4_CSI2_TX1_N
AWR_4_CSI2_TX1_P

ClassName: AWR_4_CSI_LVDS

AWR_4_CSI2_CLK_N
AWR_4_CSI2_CLK_P
AWR_4_CSI2_TX2_N
AWR_4_CSI2_TX2_P
AWR_4_CSI2_TX3_N
AWR_4_CSI2_TX3_P
AWR_4_LVDS_FRCLK_N
AWR_4_LVDS_FRCLK_P
AWR_4_LVDS_VALID_N
AWR_4_LVDS_VALID_P

ClassName: AWR_3_CSI_LVDS

AWR_3_CSI2_TX0_N
AWR_3_CSI2_TX0_P
AWR_3_CSI2_TX1_N
AWR_3_CSI2_TX1_P

ClassName: AWR_3_CSI_LVDS

AWR_3_CSI2_CLK_N
AWR_3_CSI2_CLK_P
AWR_3_CSI2_TX2_N
AWR_3_CSI2_TX2_P
AWR_3_CSI2_TX3_N
AWR_3_CSI2_TX3_P
AWR_3_LVDS_FRCLK_N
AWR_3_LVDS_FRCLK_P
AWR_3_LVDS_VALID_N
AWR_3_LVDS_VALID_P

TP33 CONN_MONITOR_2 — AWR_CONN_TP3 TP8

TP13 AWR_CONN_TP4

SYSTEM_PGOOD — CONN_MONITOR_2

J5 — FX23-120P-0.5SV15

AWR_4_TDI	AWR_4_TDI	1	61		
AWR_4_TDO	AWR_4_TDO	3	63		
AWR_4_TMS	AWR_4_TMS	4	64		
AWR_4_TCK	AWR_4_TCK	5	65		
		6	66		
AWR_4_SOP0_TDO		7	67		
AWR_4_SOP1_SYNCOUT		8	68		
AWR_4_SOP2_PMICCLKOUT		9	69		
		10	70		
AWR_4_WARM_RST	AWR_4_WARM_RST	11	71		
AWR_4_NRST	AWR_4_NRST_HOST	12	72		
		13	73		
AWR_4_GPIO_2	AWR_4_GPIO_2	14	74		
AWR_4_GPIO_1	AWR_4_GPIO_1	15	75		
AWR_4_GPIO_0	AWR_4_GPIO_0	16	76		
		17	77		
AWR_4_BSS_LOGGER	AWR_4_BSS_LOGGER	18	78		
AWR_4_MSS_LOGGER	AWR_4_MSS_LOGGER	19	79		
AWR_4_UART_TX	AWR_4_UART_TX	20	80		
AWR_4_UART_RX	AWR_4_UART_RX	21	81		
		22	82		
AWR_4_SPI_CLK1	AWR_4_SPI_CLK1	23	83		
AWR_4_SPI_MOSI1	AWR_4_SPI_MOSI1	24	84		
AWR_4_SPI_CS1	AWR_4_SPI_CS1	25	85		
		26	86		
AWR_4_SPI_HOST_INTR1	AWR_4_SPI_HOST_INTR1	27	87		
AWR_4_SPI_MISO1	AWR_4_SPI_MISO1	28	88		
		29	89		
AWR_3_TDI	AWR_3_TDI	30	90		
AWR_3_TDO	AWR_3_TDO	31	91		
AWR_3_TMS	AWR_3_TMS	32	92		
AWR_3_TCK	AWR_3_TCK	33	93		
		34	94		
AWR_3_WARM_RST	AWR_3_WARM_RST	35	95		
AWR_3_NRST	AWR_3_NRST_HOST	36	96		
	AWR_3_SOP0_TDO	37	97		
	AWR_3_SOP1_SYNCOUT	38	98		
	AWR_3_SOP2_PMICCLKOUT	39	99		
		40	100		
AWR_3_BSS_LOGGER	AWR_3_BSS_LOGGER	41	101		
AWR_3_MSS_LOGGER	AWR_3_MSS_LOGGER	42	102		
AWR_3_UART_TX	AWR_3_UART_TX	43	103		
AWR_3_UART_RX	AWR_3_UART_RX	44	104		
		45	105		
PMIC_BUCKEN	PMIC_BUCK_EN	R145 0	106	PMIC_BUCKEN_CONN	
PMIC_NRST	PMIC_NRST	R146 0	107	PMIC_NRST_CONN	
PMIC2_TMPSNS_SDA	PMIC2_TMPSNS_SDA		108	PMIC2_TMPSNS_SDA	
PMIC2_TMPSNS_SCL	PMIC2_TMPSNS_SCL		109	PMIC2_TMPSNS_SCL	
			110		
AWR_3_SPI_CLK1	AWR_3_SPI_CLK1		111		
AWR_3_SPI_MOSI1	AWR_3_SPI_MOSI1		112		
AWR_3_SPI_CS1	AWR_3_SPI_CS1		113		
AWR_3_SPI_HOST_INTR1	AWR_3_SPI_HOST_INTR1		114		
AWR_3_SPI_MISO1	AWR_3_SPI_MISO1		115		
			116		
TMPSNS_ALERT	TMPSNS_ALERT		117		
AWR_3_GPIO_2	AWR_3_GPIO_2		118		
AWR_3_GPIO_1	AWR_3_GPIO_1		119	SYSTEM_PGOOD	SYSTEM_PGOOD
AWR_3_GPIO_0	AWR_3_GPIO_0		120	CONN_MONITOR_2	
SYSTEM_5V0		P1	P3		
		P2	P4		
		MH1	MH2		

C192 10V 47µF
C193 10V 47µF

GND GND GND GND

Safety Error Signals

SYSTEM_3V3 — R150 10.0k — NERROR_OUT

Note: ERROR_OUT signals are open-drain and active-low. Any one AWR device can pull the NERROR_OUT signal low in this configuration.

NERROR_OUT	NERROR_OUT	R154 0	AWR_1_NERROR_OUT	AWR_1_NERROR_OUT
		R156 0	AWR_2_NERROR_OUT	AWR_2_NERROR_OUT
		R158 0	AWR_3_NERROR_OUT	AWR_3_NERROR_OUT
		R160 0	AWR_4_NERROR_OUT	AWR_4_NERROR_OUT

AWR and PMIC I2C Signals

AWR_1_SCL	AWR_1_SCL	PMIC1_SCL	PMIC1_SCL
AWR_1_SDA	AWR_1_SDA	PMIC1_SDA	PMIC1_SDA
AWR_2_SCL	AWR_2_SCL	PMIC1_SCL	PMIC1_SCL
AWR_2_SDA	AWR_2_SDA	PMIC1_SDA	PMIC1_SDA
AWR_3_SCL	AWR_3_SCL	PMIC1_SCL	PMIC1_SCL
AWR_3_SDA	AWR_3_SDA	PMIC1_SDA	PMIC1_SDA
AWR_4_SCL	AWR_4_SCL	PMIC1_SCL	PMIC1_SCL
AWR_4_SDA	AWR_4_SDA	PMIC1_SDA	PMIC1_SDA

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 2/6/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: HOST_CONNECTOR	
Custom Rev:		Assembly VAWRiant:	Sheet:9 of 19
Drawn By:a0271760		File: PROC054D_Host_Connector.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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AWR Radar SoC - Interfaces

References

http://www.ti.com/product/AWR2243

AWR LDO and Bandgap Output Capacitors

Place output capacitors as close to power pins as possible - minimum mounting inductance.

AWR_1V4_SYNTH_1 — C1_1 16V 1uF — GND
AWR_VBGAP_1 — C2_1 16V 0.22µF — GND
AWR_1V4_APLL_1 — C3_1 16V 1uF — GND
AWR_VOUT_PA_1 — C4_1 16V 0.22µF — GND; C5_1 10V 10uF — GND

AWR Interfaces

ClassName: AWR_20GHZ_LO

FMCW_SYNCIN1_1 — AWR_1_FMCW_CLKOUT
FMCW_CLKOUT_1 — AWR_1_FMCW_CLKOUT
FMCW_SYNCOUT_1 — AWR_1_FMCW_SYNCOUT

DIG_SYNCIN_1 — AWR_1_DIG_SYNCIN
DIG_SYNCOUT_1 — AWR_1_DIG_SYNCOUT — TP1_1

OSC_CLKOUT_1 — AWR_1_OSC_CLKOUT
XTAL_CLKP_1 — AWR_1_XTAL_CLKP
XTAL_CLKM_1 — AWR_1_XTAL_CLKM

PMIC_CLKOUT_1 — AWR_1_PMIC_CLKOUT
MCU_CLKOUT_1 — AWR_1_MCU_CLKOUT — TP2_1

NRST_1 — AWR_1_NRST
WARM_RST_1 — AWR_1_WARM_RST
NERROR_IN_1 — AWR_1_NERROR_IN
NERROR_OUT_1 — AWR_1_NERROR_OUT

ClassName: AWR_SYNC

UART_RX_1 — AWR_1_UART_RX
UART_TX_1 — AWR_1_UART_TX

ClassName: AWR_CLOCK

TCK_1 — AWR_1_TCK
TMS_1 — AWR_1_TMS
TDO_1 — AWR_1_TDO — TP3_1
TDI_1 — AWR_1_TDI

SPI_HOST_INTR1_1 — AWR_1_SPI_HOST_INTR1
SPI_CLK1_1 — AWR_1_SPI_CLK1
SPI_CS1_1 — AWR_1_SPI_CS1
SPI_MISO1_1 — AWR_1_SPI_MISO1
SPI_MOSI1_1 — AWR_1_SPI_MOSI1

ClassName: AWR_GENERAL

GPIO_0_1 — AWR_1_GPIO_0
GPIO_1_1 — AWR_1_GPIO_1
GPIO_2_1 — AWR_1_GPIO_2

SCL_1 — AWR_1_SCL
SDA_1 — AWR_1_SDA
BSS_LOGGER_1 — AWR_1_BSS_LOGGER
MSS_LOGGER_1 — AWR_1_MSS_LOGGER

NOTE: UART_RX and UART_TX directions AWRe with respect to AWR

ClassName: AWR_GENERAL

CSI2_CLK_1_P — AWR_1_CSI2_CLK_P
CSI2_CLK_1_N — AWR_1_CSI2_CLK_N
CSI2_TX0_1_P — AWR_1_CSI2_TX0_P
CSI2_TX0_1_N — AWR_1_CSI2_TX0_N
CSI2_TX1_1_P — AWR_1_CSI2_TX1_P
CSI2_TX1_1_N — AWR_1_CSI2_TX1_N
CSI2_TX2_1_P — AWR_1_CSI2_TX2_P
CSI2_TX2_1_N — AWR_1_CSI2_TX2_N
CSI2_TX3_1_P — AWR_1_CSI2_TX3_P
CSI2_TX3_1_N — AWR_1_CSI2_TX3_N
LVDS_FRCLK_1_P — AWR_1_LVDS_FRCLK_P
LVDS_FRCLK_1_N — AWR_1_LVDS_FRCLK_N
LVDS_VALID_1_P — AWR_1_LVDS_VALID_P
LVDS_VALID_1_N — AWR_1_LVDS_VALID_N

AWR_1V0_RF2_1 — AWR_1_1V0_RF2_FILT

NOTE: AWR antenna routed as GCPW transmission lines to etched antenna.

ClassName: AWR_ANTENNA

NOTE: AWR FMCW_SYNCIN2 unused. Shorted to GND per datasheet requirements.

NOTE: AWR FMCW_CLKOUT/SYNCOUT unused terminated to 50-ohms per datasheet requirements.

AWR_RX1_1 — M2 RX1
AWR_RX2_1 — K2 RX2
AWR_RX3_1 — H2 RX3
AWR_RX4_1 — F2 RX4
AWR_TX1_1 — B4 TX1
AWR_TX2_1 — B6 TX2
AWR_TX3_1 — B8 TX3
AWR_1_FMCW_CLKOUT — B1 FM_CW_SYNCIN1
D15 FM_CW_SYNCIN2
AWR_1_FMCW_CLKOUT — B10 FM_CW_CLKOUT
AWR_1_FMCW_SYNCOUT — D1 FM_CW_SYNCOUT

AWR_1_DIG_SYNCIN — N10 SYNC_IN
AWR_1_DIG_SYNCOUT — R1_1 33.2 — DIG_SYNCOUT_RS_1 — P11 SYNC_OUT

AWR_1_OSC_CLKOUT — R2_1 33.2 — OSC_CLKOUT_RS_1 — A14 OSC_CLKOUT
AWR_1_XTAL_CLKP — E14 CLKP
AWR_1_XTAL_CLKM — F14 CLKM

AWR_1_PMIC_CLKOUT — R4_1 33.2 — PMIC_CLKOUT_RS_1 — P13 PMIC_CLK_OUT
AWR_1_MCU_CLKOUT — R5_1 33.2 — MCU_CLKOUT_RS_1 — N9 MCU_CLK_OUT

GPADC0_1 — C14 VSENSE
GPADC5_1 — C13 ANAMUX
GPADC1_1 — P1 ANALOGTEST1
GPADC2_1 — P2 ANALOGTEST2
GPADC3_1 — P3 ANALOGTEST3
GPADC4_1 — R2 ANALOGTEST4

AWR_1_NRST — P12 RESET
AWR_1_WARM_RST — N13 WARM_RESET
AWR_1_NERROR_IN — P7 NERROR_IN
AWR_1_NERROR_OUT — R9_1 0 — NERROR_OUT_RS_1 — N8 NERROR_OUT

AWR_1_UART_RX — N5 RS232_RX
AWR_1_UART_TX — R11_1 33.2 — UART_TX_RS_1 — N6 RS232_TX

AWR_1_SCL — P4 RESERVED
AWR_1_SDA — R13_1 33.2 — SDA_RS_1 — R3 RESERVED
AWR_1_BSS_LOGGER — R14_1 33.2 — BSS_LOGGER_RS_1 — R4 RESERVED
AWR_1_MSS_LOGGER — R15_1 33.2 — MSS_LOGGER_RS_1 — R5 RESERVED

U1_1A — XA2243PBGABL

VOUT_14SYNTH — A13 AWR_1V4_SYNTH_1
VOUT_14APLL1 — A10 AWR_1V4_APLL_1
VBGAP — B10 AWR_VBGAP_1
VOUT_PA — A2 AWR_VOUT_PA_1
VOUT_PA — B2

ClassName: AWR_POWER_ANA

Place R188 as close as possible to VOUT_PA/RF2 pins

R188_1 0 AWR_1_1V0_RF2_FILT

Note: AWR_1V0_RF2 optionally shorted to AWR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.

R188 installed - shorts AWR_VOUT_PA to AWR_1V0_RF2 (default)
R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

CSI2_TXP[0] — G15 AWR_1_CSI2_TX0_P
CSI2_TXM[0] — G14 AWR_1_CSI2_TX0_N
CSI2_TXP[1] — H15 AWR_1_CSI2_TX1_P
CSI2_TXM[1] — H14 AWR_1_CSI2_TX1_N
CSI2_CLKP — J15 AWR_1_CSI2_CLK_P
CSI2_CLKM — J14 AWR_1_CSI2_CLK_N
CSI2_TXP[2] — K15 AWR_1_CSI2_TX2_P
CSI2_TXM[2] — K14 AWR_1_CSI2_TX2_N
CSI2_TXP[3] — L15 AWR_1_CSI2_TX3_P
CSI2_TXM[3] — L14 AWR_1_CSI2_TX3_N
HS_DEBUG1_P — M15 AWR_1_LVDS_FRCLK_P
HS_DEBUG1_M — M14 AWR_1_LVDS_FRCLK_N
HS_DEBUG2_P — N15 AWR_1_LVDS_VALID_P
HS_DEBUG2_M — N14 AWR_1_LVDS_VALID_N

QSPI_FLASH_3V3_1 — R3_1 47.5k

QSPI_CS — P8 QSPI_CS_RS_1 — R6_1 0 — QSPI_CS_1
QSPI_CLK — R10 QSPI_CLK_RS_1 — R7_1 0 — QSPI_CLK_1
QSPI[0] — R11 QSPI_D0_1
QSPI[1] — P9 QSPI_D1_1
QSPI[2] — R12 QSPI_D2_1
QSPI[3] — R10 QSPI_D3_1

Place termination and pull-up resistors close to QSPI controller - minimize stubs.

ClassName: AWR_QSPI

TCK — M13 AWR_1_TCK
TMS — L13 AWR_1_TMS
TDO — TDO_RS_1 — R8_1 33.2 — AWR_1_TDO
TDI — H13 AWR_1_TDI

ClassName: AWR_JTAG

SPI_HOST_INTR_1 — P6 SPI_HOST_INTR1_RS_1 — R10_1 33.2 — AWR_1_SPI_HOST_INTR1
SPI_CLK_1 — R9 — AWR_1_SPI_CLK1
SPI_CS_1 — R7 — AWR_1_SPI_CS1
MISO_1 — P5 SPI_MISO1_RS_1 — R12_1 33.2 — AWR_1_SPI_MISO1
MOSI_1 — R8 — AWR_1_SPI_MOSI1

ClassName: AWR_GENERAL

GPIO[0] — N4 AWR_1_GPIO_0
GPIO[1] — N7 AWR_1_GPIO_1
GPIO[2] — N13 AWR_1_GPIO_2

ClassName: AWR_GENERAL

R16_1 10.0k; R17_1 10.0k; R18_1 10.0k — GND

SOP[2:0] Pins

NOTE: SOP (stAWRt on power) Pins
SOP[2]/PMIC_CLK_OUT
SOP[1]/SYNC_OUT
SOP[0]TDO

SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
SOP[2:0] = 0b001 -> SOP_MODE3 "Funcational"
SOP[2:0] = 0b101 -> SOP_MODE5 "QSPI Flashing"

NOR QSPI FLASH (For Development Purposes)

Pull-ups disable write-protect and hold functions by default.

QSPI_FLASH_3V3_1 — R27_1 10.0k; R28_1 10.0k

QSPI_D0_1 — R30_1 0 — QSPI_D0_RS_1
QSPI_D1_1 — R31_1 0 — QSPI_D1_RS_1
QSPI_D2_1 — R32_1 0 — QSPI_D2_RS_1
QSPI_D3_1 — R33_1 0 — QSPI_D3_RS_1

QSPI_FLASH_3V3_1 — 8 VCC
QSPI_CS_1 — 1 CS
QSPI_CLK_1 — 6 SCLK
5 SI/SIO0
2 SO/SIO1
3 WP/SIO2
7 HOLD/SIO3
EP 9
GND 4

U2_1 — MX25V1635FZNQ

NOR Flash 16Mb (2M x 8) 80MHz CLK

Place termination and pull-up resistors close to QSPI flash - minimize stubs.

GND

ClassName: SYSTEM_3V3

SYSTEM_3V3 — R29_1 0 — QSPI_FLASH_3V3_1

Flash 3.3V Power Disconnect - Use to disconnect power to flash.

C6_1 10V 10uF; C7_1 16V 1uF; C8_1 50V 0.1uF — GND

Debug Test Header (For Development Purposes)

GPADC1_1 — R21_1 0 — GPADC1_CONN_1
GPADC2_1 — R22_1 0 — GPADC2_CONN_1
GPADC3_1 — R23_1 0 — GPADC3_CONN_1
GPADC4_1 — R24_1 0 — GPADC4_CONN_1
GPADC5_1 — R25_1 0 — GPADC5_CONN_1
GPADC6_1 — R26_1 0 — GPADC6_CONN_1

J1_1 — TSM-106-01-L-DV — GND

ClassName: AWR_DEBUG

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 2/10/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: AWR_1	
Custom Rev:		Assembly VAWRiant:	Sheet:10 of 19
Drawn By:a0271760		File: PROC054D_AWR_Interfaces.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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AWR Radar SoC - Interfaces

References

http://www.ti.com/product/AWR2243

AWR LDO and Bandgap Output Capacitors

Place output capacitors as close to power pins as possible - minimum mounting inductance.

AWR_1V4_SYNTH_2 — C1_2 16V 1uF — GND
AWR_VBGAP_2 — C2_2 16V 0.22µF — GND
AWR_1V4_APLL_2 — C3_2 16V 1uF — GND
AWR_VOUT_PA_2 — C4_2 16V 0.22µF — GND; C5_2 10V 10uF — GND

AWR Interfaces

ClassName: AWR_20GHZ_LO

FMCW_SYNCIN1_2 — AWR_1_FMCW_CLKOUT
FMCW_CLKOUT_2 — AWR_2_FMCW_CLKOUT
FMCW_SYNCOUT_2 — AWR_2_FMCW_SYNCOUT

DIG_SYNCIN_2 — AWR_2_DIG_SYNCIN
DIG_SYNCOUT_2 — AWR_2_DIG_SYNCOUT — TP1_2
OSC_CLKOUT_2 — AWR_2_OSC_CLKOUT
XTAL_CLKP_2 — AWR_2_XTAL_CLKP
XTAL_CLKM_2 — AWR_2_XTAL_CLKM
PMIC_CLKOUT_2 — AWR_2_PMIC_CLKOUT
MCU_CLKOUT_2 — AWR_2_MCU_CLKOUT — TP2_2

NRST_2 — AWR_2_NRST
WARM_RST_2 — AWR_2_WARM_RST
NERROR_IN_2 — AWR_2_NERROR_IN
NERROR_OUT_2 — AWR_2_NERROR_OUT

ClassName: AWR_SYNC

UART_RX_2 — AWR_2_UART_RX
UART_TX_2 — AWR_2_UART_TX

ClassName: AWR_CLOCK

TCK_2 — AWR_2_TCK
TMS_2 — AWR_2_TMS
TDO_2 — AWR_2_TDO
TDI_2 — AWR_2_TDI — TP3_2

SPI_HOST_INTR1_2 — AWR_2_SPI_HOST_INTR1
SPI_CLK1_2 — AWR_2_SPI_CLK1
SPI_CS1_2 — AWR_2_SPI_CS1
SPI_MISO1_2 — AWR_2_SPI_MISO1
SPI_MOSI1_2 — AWR_2_SPI_MOSI1

ClassName: AWR_GENERAL

GPIO_0_2 — AWR_2_GPIO_0
GPIO_1_2 — AWR_2_GPIO_1
GPIO_2_2 — AWR_2_GPIO_2

SCL_2 — AWR_2_SCL
SDA_2 — AWR_2_SDA
BSS_LOGGER_2 — AWR_2_BSS_LOGGER
MSS_LOGGER_2 — AWR_2_MSS_LOGGER

NOTE: UART_RX and UART_TX directions AWRe with respect to AWR

ClassName: AWR_GENERAL

CSI2_CLK_2_P — AWR_2_CSI2_CLK_P
CSI2_CLK_2_N — AWR_2_CSI2_CLK_N
CSI2_TX0_2_P — AWR_2_CSI2_TX0_P
CSI2_TX0_2_N — AWR_2_CSI2_TX0_N
CSI2_TX1_2_P — AWR_2_CSI2_TX1_P
CSI2_TX1_2_N — AWR_2_CSI2_TX1_N
CSI2_TX2_2_P — AWR_2_CSI2_TX2_P
CSI2_TX2_2_N — AWR_2_CSI2_TX2_N
CSI2_TX3_2_P — AWR_2_CSI2_TX3_P
CSI2_TX3_2_N — AWR_2_CSI2_TX3_N
LVDS_FRCLK_2_P — AWR_2_LVDS_FRCLK_P
LVDS_FRCLK_2_N — AWR_2_LVDS_FRCLK_N
LVDS_VALID_2_P — AWR_2_LVDS_VALID_P
LVDS_VALID_2_N — AWR_2_LVDS_VALID_N

AWR_1V0_RF2_2 — AWR_2_1V0_RF2_FILT

NOTE: AWR antenna routed as GCPW transmission lines to etched antenna.

ClassName: AWR_ANTENNA

NOTE: AWR FMCW_SYNCIN2 unused. Shorted to GND per datasheet requirements.
NOTE: AWR FMCW_CLKOUT/SYNCOUT unsused terminated to 50-ohms per datasheet requirements.

AWR_RX1_2 — M2 RX1
AWR_RX2_2 — K2 RX2
AWR_RX3_2 — H2 RX3
AWR_RX4_2 — F2 RX4
AWR_TX1_2 — B4 TX1
AWR_TX2_2 — B6 TX2
AWR_TX3_2 — B8 TX3
AWR_1_FMCW_CLKOUT — B1 FM_CW_SYNCIN1
D15 FM_CW_SYNCIN2
AWR_2_FMCW_CLKOUT — B10 FM_CW_CLKOUT
AWR_2_FMCW_SYNCOUT — D1 FM_CW_SYNCOUT

AWR_2_DIG_SYNCIN — N10 SYNC_IN
AWR_2_DIG_SYNCOUT — R1_2 33.2 — DIG_SYNCOUT_RS_2 — P11 SYNC_OUT

AWR_2_OSC_CLKOUT — R2_2 33.2 — OSC_CLKOUT_RS_2 — A14 OSC_CLKOUT
AWR_2_XTAL_CLKP — E14 CLKP
AWR_2_XTAL_CLKM — F14 CLKM

AWR_2_PMIC_CLKOUT — R4_2 33.2 — PMIC_CLKOUT_RS_2 — P13 PMIC_CLK_OUT
AWR_2_MCU_CLKOUT — R5_2 33.2 — MCU_CLKOUT_RS_2 — N9 MCU_CLK_OUT

GPADC6_2 — C14 VSENSE
GPADC5_2 — C13 ANAMUX
GPADC1_2 — P1 ANALOGTEST1
GPADC2_2 — P2 ANALOGTEST2
GPADC3_2 — P3 ANALOGTEST3
GPADC4_2 — R2 ANALOGTEST4

AWR_2_NRST — P12 RESET
AWR_2_WARM_RST — N13 WARM_RESET
AWR_2_NERROR_IN — P7 NERROR_IN
AWR_2_NERROR_OUT — R9_2 0 — NERROR_OUT_RS_2 — N8 NERROR_OUT

AWR_2_UART_RX — N5 RS232_RX
AWR_2_UART_TX — R11_2 33.2 — UART_TX_RS_2 — N6 RS232_TX

AWR_2_SCL — P4 RESERVED
AWR_2_SDA — R13_2 33.2 — SDA_RS_2 — R3 RESERVED
AWR_2_BSS_LOGGER — R14_2 33.2 — BSS_LOGGER_RS_2 — R4 RESERVED
AWR_2_MSS_LOGGER — R15_2 33.2 — MSS_LOGGER_RS_2 — R5 RESERVED

U1_2A — XA2243PBGABL

VOUT_14SYNTH — A13 AWR_1V4_SYNTH_2
VOUT_14APLL1 — A10 AWR_1V4_APLL_2
VBGAP — B10 AWR_VBGAP_2
VOUT_PA — A2 AWR_VOUT_PA_2
VOUT_PA — B2

ClassName: AWR_POWER_ANA

Place R188 as close as possible to VOUT_PA/RF2 pins

R188_2 0 AWR_2_1V0_RF2_FILT

Note: AWR_1V0_RF2 optionally shorted to AWR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.

R188 installed - shorts AWR_VOUT_PA to AWR_1V0_RF2 (default)
R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

CSI2_TXP[0] — G15 AWR_2_CSI2_TX0_P
CSI2_TXM[0] — G14 AWR_2_CSI2_TX0_N
CSI2_TXP[1] — H15 AWR_2_CSI2_TX1_P
CSI2_TXM[1] — H14 AWR_2_CSI2_TX1_N
CSI2_CLKP — J15 AWR_2_CSI2_CLK_P
CSI2_CLKM — J14 AWR_2_CSI2_CLK_N
CSI2_TXP[2] — K15 AWR_2_CSI2_TX2_P
CSI2_TXM[2] — K14 AWR_2_CSI2_TX2_N
CSI2_TXP[3] — L15 AWR_2_CSI2_TX3_P
CSI2_TXM[3] — L14 AWR_2_CSI2_TX3_N
HS_DEBUG1_P — M15 AWR_2_LVDS_FRCLK_P
HS_DEBUG1_M — M14 AWR_2_LVDS_FRCLK_N
HS_DEBUG2_P — N15 AWR_2_LVDS_VALID_P
HS_DEBUG2_M — N14 AWR_2_LVDS_VALID_N

QSPI_CS — P8 QSPI_CS_RS_2 — R6_2 0 — QSPI_CS_2
QSPI_CLK — R10 QSPI_CLK_RS_2 — R7_2 0 — QSPI_CLK_2
QSPI[0] — R11 QSPI_D0_2
QSPI[1] — P9 QSPI_D1_2
QSPI[2] — R12 QSPI_D2_2
QSPI[3] — R10 QSPI_D3_2

QSPI_FLASH_3V3_2 — R3_2 47.5k

Place termination and pull-up resistors close to QSPI controller - minimize stubs.

ClassName: AWR_QSPI

TCK — M13 AWR_2_TCK
TMS — L13 AWR_2_TMS
TDO — J13 TDO_RS_2 — R8_2 33.2 — AWR_2_TDO
TDI — H13 AWR_2_TDI

ClassName: AWR_JTAG

SPI_HOST_INTR_1 — P6 SPI_HOST_INTR1_RS_2 — R10_2 33.2 — AWR_2_SPI_HOST_INTR1
SPI_CLK_1 — R9 AWR_2_SPI_CLK1
SPI_CS_1 — R7 AWR_2_SPI_CS1
MISO_1 — P5 SPI_MISO1_RS_2 — R12_2 33.2 — AWR_2_SPI_MISO1
MOSI_1 — R8 AWR_2_SPI_MOSI1

ClassName: AWR_GENERAL

GPIO[0] — N4 AWR_2_GPIO_0
GPIO[1] — N7 AWR_2_GPIO_1
GPIO[2] — N13 AWR_2_GPIO_2

ClassName: AWR_GENERAL

R16_2 10.0k R17_2 10.0k R18_2 10.0k — GND

SOP[2:0] Pins

NOTE: SOP (stAWRt on power) Pins
SOP[2]/PMIC_CLK_OUT
SOP[1]/SYNC_OUT
SOP[0]TDO

SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
SOP[2:0] = 0b001 -> SOP_MODE3 "Funcational"
SOP[2:0] = 0b101 -> SOP_MODE5 "QSPI Flashing"

NOR QSPI FLASH (For Development Purposes)

Pull-ups disable write-protect and hold functions by default.

QSPI_FLASH_3V3_2 — R27_2 10.0k — R28_2 10.0k

U2_2 — MX25V1635FZNQ

QSPI_FLASH_3V3_2 — VCC
QSPI_CS_2 — CS
QSPI_CLK_2 — SCLK
QSPI_D0_2 — R30_2 0 — QSPI_D0_RS_2 — SI/SIO0
QSPI_D1_2 — R31_2 0 — QSPI_D1_RS_2 — SO/SIO1
QSPI_D2_2 — R32_2 0 — QSPI_D2_RS_2 — WP/SIO2
QSPI_D3_2 — R33_2 0 — QSPI_D3_RS_2 — HOLD/SIO3
EP — GND

NOR Flash 16Mb (2M x 8) 80MHz CLK

Place termination and pull-up resistors close to QSPI flash - minimize stubs.

ClassName: SYSTEM_3V3

SYSTEM_3V3 — R29_2 0 — QSPI_FLASH_3V3_2

Flash 3.3V Power Disconnect - Use to disconnect power to flash.

C6_2 10V 10uF — C7_2 16V 1uF — C8_2 50V 0.1uF — GND

Debug Test Header (For Development Purposes)

GPADC1_2 — R21_2 0 — GPADC1_CONN_2
GPADC2_2 — R22_2 0 — GPADC2_CONN_2
GPADC3_2 — R23_2 0 — GPADC3_CONN_2
GPADC4_2 — R24_2 0 — GPADC4_CONN_2
GPADC5_2 — R25_2 0 — GPADC5_CONN_2
GPADC6_2 — R26_2 0 — GPADC6_CONN_2

J1_2 — TSM-106-01-L-DV — GND

ClassName: AWR_DEBUG

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 2/10/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: AWR_1	
Custom Rev:		Assembly VAWRiant:	Sheet:10 of 19
Drawn By:a0271760		File: PROC054D_AWR_Interfaces.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

TEXAS INSTRUMENTS — http://www.ti.com

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AWR Radar SoC - Interfaces

References

http://www.ti.com/product/AWR2243

AWR LDO and Bandgap Output Capacitors

Place output capacitors as close to power pins as possible - minimum mounting inductance.

AWR_1V4_SYNTH_3 — C1_3 16V 1uF — GND
AWR_VBGAP_3 — C2_3 16V 0.22µF — GND
AWR_1V4_APLL_3 — C3_3 16V 1uF — GND
AWR_VOUT_PA_3 — C4_3 16V 0.22µF — C5_3 10V 10uF — GND

AWR Interfaces

ClassName: AWR_20GHZ_LO

FMCW_SYNCIN1_3 — AWR_1_FMCW_SYNCOUT
FMCW_CLKOUT_3 — AWR_3_FMCW_CLKOUT
FMCW_SYNCOUT_3 — AWR_3_FMCW_SYNCOUT

DIG_SYNCIN_3 — AWR_3_DIG_SYNCIN
DIG_SYNCOUT_3 — AWR_3_DIG_SYNCOUT — TP1_3
OSC_CLKOUT_3 — AWR_3_OSC_CLKOUT
XTAL_CLKP_3 — AWR_3_XTAL_CLKP
XTAL_CLKM_3 — AWR_3_XTAL_CLKM
PMIC_CLKOUT_3 — AWR_3_PMIC_CLKOUT
MCU_CLKOUT_3 — AWR_3_MCU_CLKOUT — TP2_3

NRST_3 — AWR_3_NRST
WARM_RST_3 — AWR_3_WARM_RST
NERROR_IN_3 — AWR_3_NERROR_IN
NERROR_OUT_3 — AWR_3_NERROR_OUT

ClassName: AWR_SYNC

UART_RX_3 — AWR_3_UART_RX
UART_TX_3 — AWR_3_UART_TX

ClassName: AWR_CLOCK

TCK_3 — AWR_3_TCK
TMS_3 — AWR_3_TMS
TDO_3 — AWR_3_TDO
TDI_3 — AWR_3_TDI — TP3_3

SPI_HOST_INTR1_3 — AWR_3_SPI_HOST_INTR1
SPI_CLK1_3 — AWR_3_SPI_CLK1
SPI_CS1_3 — AWR_3_SPI_CS1
SPI_MISO1_3 — AWR_3_SPI_MISO1
SPI_MOSI1_3 — AWR_3_SPI_MOSI1

ClassName: AWR_GENERAL

GPIO_0_3 — AWR_3_GPIO_0
GPIO_1_3 — AWR_3_GPIO_1
GPIO_2_3 — AWR_3_GPIO_2

SCL_3 — AWR_3_SCL
SDA_3 — AWR_3_SDA
BSS_LOGGER_3 — AWR_3_BSS_LOGGER
MSS_LOGGER_3 — AWR_3_MSS_LOGGER

NOTE: UART_RX and UART_TX directions AWRe with respect to AWR

ClassName: AWR_GENERAL

CSI2_CLK_3_P — AWR_3_CSI2_CLK_P
CSI2_CLK_3_N — AWR_3_CSI2_CLK_N
CSI2_TX0_3_P — AWR_3_CSI2_TX0_P
CSI2_TX0_3_N — AWR_3_CSI2_TX0_N
CSI2_TX1_3_P — AWR_3_CSI2_TX1_P
CSI2_TX1_3_N — AWR_3_CSI2_TX1_N
CSI2_TX2_3_P — AWR_3_CSI2_TX2_P
CSI2_TX2_3_N — AWR_3_CSI2_TX2_N
CSI2_TX3_3_P — AWR_3_CSI2_TX3_P
CSI2_TX3_3_N — AWR_3_CSI2_TX3_N
LVDS_FRCLK_3_P — AWR_3_LVDS_FRCLK_P
LVDS_FRCLK_3_N — AWR_3_LVDS_FRCLK_N
LVDS_VALID_3_P — AWR_3_LVDS_VALID_P
LVDS_VALID_3_N — AWR_3_LVDS_VALID_N

AWR_1V0_RF2_3 — AWR_3_1V0_RF2_FILT

ClassName: AWR_ANTENNA

NOTE: AWR antenna routed as GCPW transmission lines to etched antenna.

NOTE: AWR FMCW_SYNCIN2 unused. Shorted to GND per datasheet requirements.

NOTE: AWR FMCW_CLKOUT/SYNCOUT unused terminated to 50-ohms per datasheet requirements.

AWR_RX1_3 — M2 RX1
AWR_RX2_3 — K2 RX2
AWR_RX3_3 — H2 RX3
AWR_RX4_3 — F2 RX4
AWR_TX1_3 — B4 TX1
AWR_TX2_3 — B6 TX2
AWR_TX3_3 — B8 TX3
AWR_1_FMCW_SYNCOUT — B1 FM_CW_SYNCIN1
D15 FM_CW_SYNCIN2
AWR_3_FMCW_CLKOUT — B15 FM_CW_CLKOUT
AWR_3_FMCW_SYNCOUT — D1 FM_CW_SYNCOUT

AWR_3_DIG_SYNCIN — N10 SYNC_IN
AWR_3_DIG_SYNCOUT — R1_3 33.2 — DIG_SYNCOUT_RS_3 — P11 SYNC_OUT

AWR_3_OSC_CLKOUT — R2_3 33.2 — OSC_CLKOUT_RS_3 — A14 OSC_CLKOUT
AWR_3_XTAL_CLKP — E14 CLKP
AWR_3_XTAL_CLKM — F14 CLKM

AWR_3_PMIC_CLKOUT — R4_3 33.2 — PMIC_CLKOUT_RS_3 — P13 PMIC_CLK_OUT
AWR_3_MCU_CLKOUT — R5_3 33.2 — MCU_CLKOUT_RS_3 — N9 MCU_CLK_OUT

GPADC6_3 — C14 VSENSE
GPADC5_3 — C13 ANAMUX
GPADC1_3 — P1 ANALOGTEST1
GPADC2_3 — P2 ANALOGTEST2
GPADC3_3 — P3 ANALOGTEST3
GPADC4_3 — R2 ANALOGTEST4

AWR_3_NRST — P12 RESET
AWR_3_WARM_RST — N12 WARM_RESET
AWR_3_NERROR_IN — P7 NERROR_IN
AWR_3_NERROR_OUT — R9_3 0 — NERROR_OUT_RS_3 — N8 NERROR_OUT

AWR_3_UART_RX — N5 RS232_RX
AWR_3_UART_TX — R11_3 33.2 — UART_TX_RS_3 — N6 RS232_TX

AWR_3_SCL — P4 RESERVED
AWR_3_SDA — R13_3 33.2 — SDA_RS_3 — R3 RESERVED
AWR_3_BSS_LOGGER — R14_3 33.2 — BSS_LOGGER_RS_3 — R4 RESERVED
AWR_3_MSS_LOGGER — R15_3 33.2 — MSS_LOGGER_RS_3 — R5 RESERVED

U1_3A — G13 RESERVED

XA2243PBGABL

ClassName: AWR_POWER_ANA

VOUT_14SYNTH — A13 AWR_1V4_SYNTH_3
VOUT_14APLL1 — A10 AWR_1V4_APLL_3
VBGAP — B10 AWR_VBGAP_3
VOUT_PA — A2 AWR_VOUT_PA_3 — R188_3 0 — AWR_3_1V0_RF2_FILT
VOUT_PA — B2

Place R188 as close as possible to VOUT_PA/RF2 pins

Note: AWR_1V0_RF2 optionally shorted to AWR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.

R188 installed - shorts AWR_VOUT_PA to AWR_1V0_RF2 (default)
R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

CSI2_TXP[0] — G15 AWR_3_CSI2_TX0_P
CSI2_TXM[0] — G14 AWR_3_CSI2_TX0_N
CSI2_TXP[1] — H15 AWR_3_CSI2_TX1_P
CSI2_TXM[1] — H14 AWR_3_CSI2_TX1_N
CSI2_CLKP — J15 AWR_3_CSI2_CLK_P
CSI2_CLKM — J14 AWR_3_CSI2_CLK_N
CSI2_TXP[2] — K15 AWR_3_CSI2_TX2_P
CSI2_TXM[2] — K14 AWR_3_CSI2_TX2_N
CSI2_TXP[3] — L15 AWR_3_CSI2_TX3_P
CSI2_TXM[3] — L14 AWR_3_CSI2_TX3_N
HS_DEBUG1_P — M15 AWR_3_LVDS_FRCLK_P
HS_DEBUG1_M — M14 AWR_3_LVDS_FRCLK_N
HS_DEBUG2_P — N15 AWR_3_LVDS_VALID_P
HS_DEBUG2_M — N14 AWR_3_LVDS_VALID_N

QSPI_CS — P8 QSPI_CS_RS_3 — R6_3 0 — QSPI_CS_3
QSPI_CLK — R10 QSPI_CLK_RS_3 — R7_3 0 — QSPI_CLK_3
QSPI[0] — R11 QSPI_D0_3
QSPI[1] — P9 QSPI_D1_3
QSPI[2] — R12 QSPI_D2_3
QSPI[3] — R10 QSPI_D3_3

QSPI_FLASH_3V3_3 — R3_3 47.5k

Place termination and pull-up resistors close to QSPI controller - minimize stubs.

ClassName: AWR_QSPI

TCK — M13 AWR_3_TCK
TMS — L13 AWR_3_TMS
TDO — J13 TDO_RS_3 — R8_3 33.2 — AWR_3_TDO
TDI — H13 AWR_3_TDI

ClassName: AWR_JTAG

SPI_HOST_INTR_1 — P6 SPI_HOST_INTR1_RS_3 — R10_3 33.2 — AWR_3_SPI_HOST_INTR1
SPI_CLK_1 — R9 — AWR_3_SPI_CLK1
SPI_CS_1 — R7 — AWR_3_SPI_CS1
MISO_1 — P5 SPI_MISO1_RS_3 — R12_3 33.2 — AWR_3_SPI_MISO1
MOSI_1 — R8 — AWR_3_SPI_MOSI1

ClassName: AWR_GENERAL

GPIO[0] — N4 AWR_3_GPIO_0
GPIO[1] — N7 AWR_3_GPIO_1
GPIO[2] — N13 AWR_3_GPIO_2

ClassName: AWR_GENERAL

R16_3 10.0k — R17_3 10.0k — R18_3 10.0k — GND

SOP[2:0] Pins

NOTE: SOP (staWRt on power) Pins
SOP[2]/PMIC_CLK_OUT
SOP[1]/SYNC_OUT
SOP[0]TDO

SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
SOP[2:0] = 0b001 -> SOP_MODE3 "Funcational"
SOP[2:0] = 0b101 -> SOP_MODE5 "QSPI Flashing"

NOR QSPI FLASH (For Development Purposes)

Pull-ups disable write-protect and hold functions by default.

QSPI_FLASH_3V3_3 — R27_3 10.0k — R28_3 10.0k

QSPI_D0_3 — R30_3 0 — QSPI_D0_RS_3
QSPI_D1_3 — R31_3 0 — QSPI_D1_RS_3
QSPI_D2_3 — R32_3 0 — QSPI_D2_RS_3
QSPI_D3_3 — R33_3 0 — QSPI_D3_RS_3

QSPI_FLASH_3V3_3 — 8 VCC
QSPI_CS_3 — 1 CS
QSPI_CLK_3 — 6 SCLK
QSPI_D0_RS_3 — 5 SI/SIO0
QSPI_D1_RS_3 — 2 SO/SIO1
QSPI_D2_RS_3 — 3 WP/SIO2
QSPI_D3_RS_3 — 7 HOLD/SIO3
EP — 9
GND — 4 — GND

U2_3 — MX25V1635FZNQ

NOR Flash 16Mb (2M x 8) 80MHz CLK

Place termination and pull-up resistors close to QSPI flash - minimize stubs.

ClassName: SYSTEM_3V3

SYSTEM_3V3 — R29_3 0 — QSPI_FLASH_3V3_3

Flash 3.3V Power Disconnect - Use to disconnect power to flash.

C6_3 10V 10uF — C7_3 16V 1uF — C8_3 50V 0.1uF — GND

Debug Test Header (For Development Purposes)

GPADC1_3 — R21_3 0 — GPADC1_CONN_3
GPADC2_3 — R22_3 0 — GPADC2_CONN_3
GPADC3_3 — R23_3 0 — GPADC3_CONN_3
GPADC4_3 — R24_3 0 — GPADC4_CONN_3
GPADC5_3 — R25_3 0 — GPADC5_CONN_3
GPADC6_3 — R26_3 0 — GPADC6_CONN_3

J1_3 — TSM-106-01-L-DV — GND

ClassName: AWR_DEBUG

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 2/10/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: AWR_1	
Cust Rev:		Assembly VAWRiant:	Sheet:10of 19
Drawn By:a0271760		File: PROC054D_AWR_Interfaces.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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AWR Radar SoC - Interfaces

References

http://www.ti.com/product/AWR2243

AWR LDO and Bandgap Output Capacitors

Place output capacitors as close to power pins as possible - minimum mounting inductance.

AWR_1V4_SYNTH_4 — C1_4 16V 1uF — GND
AWR_VBGAP_4 — C2_4 16V 0.22uF — GND
AWR_1V4_APLL_4 — C3_4 16V 1uF — GND
AWR_VOUT_PA_4 — C4_4 16V 0.22uF — GND; C5_4 10V 10uF — GND

AWR Interfaces

ClassName: AWR_20GHZ_LO

FMCW_SYNCIN1_4 — AWR_1_FMCW_SYNCOUT
FMCW_CLKOUT_4 — AWR_4_FMCW_CLKOUT
FMCW_SYNCOUT_4 — AWR_4_FMCW_SYNCOUT

DIG_SYNCIN_4 — AWR_4_DIG_SYNCIN
DIG_SYNCOUT_4 — AWR_4_DIG_SYNCOUT — TP1_4
OSC_CLKOUT_4 — AWR_4_OSC_CLKOUT
XTAL_CLKP_4 — AWR_4_XTAL_CLKP
XTAL_CLKM_4 — AWR_4_XTAL_CLKM
PMIC_CLKOUT_4 — AWR_4_PMIC_CLKOUT
MCU_CLKOUT_4 — AWR_4_MCU_CLKOUT — TP2_4

NRST_4 — AWR_4_NRST
WARM_RST_4 — AWR_4_WARM_RST
NERROR_IN_4 — AWR_4_NERROR_IN
NERROR_OUT_4 — AWR_4_NERROR_OUT

ClassName: AWR_SYNC

UART_RX_4 — AWR_4_UART_RX
UART_TX_4 — AWR_4_UART_TX

ClassName: AWR_CLOCK

TCK_4 — AWR_4_TCK
TMS_4 — AWR_4_TMS
TDO_4 — AWR_4_TDO
TDI_4 — AWR_4_TDI — TP3_4

SPI_HOST_INTR1_4 — AWR_4_SPI_HOST_INTR1
SPI_CLK1_4 — AWR_4_SPI_CLK1
SPI_CS1_4 — AWR_4_SPI_CS1
SPI_MISO1_4 — AWR_4_SPI_MISO1
SPI_MOSI1_4 — AWR_4_SPI_MOSI1

ClassName: AWR_GENERAL

GPIO_0_4 — AWR_4_GPIO_0
GPIO_1_4 — AWR_4_GPIO_1
GPIO_2_4 — AWR_4_GPIO_2
SCL_4 — AWR_4_SCL
SDA_4 — AWR_4_SDA
BSS_LOGGER_4 — AWR_4_BSS_LOGGER
MSS_LOGGER_4 — AWR_4_MSS_LOGGER

NOTE: UART_RX and UART_TX directions AWRe with respect to AWR

ClassName: AWR_GENERAL

CSI2_CLK_4_P — AWR_4_CSI2_CLK_P
CSI2_CLK_4_N — AWR_4_CSI2_CLK_N
CSI2_TX0_4_P — AWR_4_CSI2_TX0_P
CSI2_TX0_4_N — AWR_4_CSI2_TX0_N
CSI2_TX1_4_P — AWR_4_CSI2_TX1_P
CSI2_TX1_4_N — AWR_4_CSI2_TX1_N
CSI2_TX2_4_P — AWR_4_CSI2_TX2_P
CSI2_TX2_4_N — AWR_4_CSI2_TX2_N
CSI2_TX3_4_P — AWR_4_CSI2_TX3_P
CSI2_TX3_4_N — AWR_4_CSI2_TX3_N
LVDS_FRCLK_4_P — AWR_4_LVDS_FRCLK_P
LVDS_FRCLK_4_N — AWR_4_LVDS_FRCLK_N
LVDS_VALID_4_P — AWR_4_LVDS_VALID_P
LVDS_VALID_4_N — AWR_4_LVDS_VALID_N

AWR_1V0_RF2_4 — AWR_4_1V0_RF2_FILT

ClassName: AWR_ANTENNA

NOTE: AWR antenna routed as GCPW transmission lines to etched antenna.

NOTE: AWR FMCW_SYNCIN2 unused. Shorted to GND per datasheet requirements.

NOTE: AWR FMCW_CLKOUT/SYNCOUT unused terminated to 50-ohms per datasheet requirements.

AWR_RX1_4 — M2 RX1
AWR_RX2_4 — K2 RX2
AWR_RX3_4 — H2 RX3
AWR_RX4_4 — F2 RX4
AWR_TX1_4 — B4 TX1
AWR_TX2_4 — B6 TX2
AWR_TX3_4 — B8 TX3
AWR_1_FMCW_SYNCOUT — B1 FM_CW_SYNCIN1
D15 FM_CW_SYNCIN2
AWR_4_FMCW_CLKOUT — B15 FM_CW_CLKOUT
AWR_4_FMCW_SYNCOUT — D1 FM_CW_SYNCOUT

AWR_4_DIG_SYNCIN — N10 SYNC_IN
AWR_4_DIG_SYNCOUT — R1_4 33.2 DIG_SYNCOUT_RS_4 — P11 SYNC_OUT

AWR_4_OSC_CLKOUT — R2_4 33.2 OSC_CLKOUT_RS_4 — A14 OSC_CLKOUT
AWR_4_XTAL_CLKP — E14 CLKP
AWR_4_XTAL_CLKM — F14 CLKM

AWR_4_PMIC_CLKOUT — R4_4 33.2 PMIC_CLKOUT_RS_4 — P13 PMIC_CLK_OUT
AWR_4_MCU_CLKOUT — R5_4 33.2 MCU_CLKOUT_RS_4 — N9 MCU_CLK_OUT

GPADC6_4 — C14 VSENSE
GPADC5_4 — C13 ANAMUX
GPADC1_4 — P1 ANALOGTEST1
GPADC2_4 — P2 ANALOGTEST2
GPADC3_4 — P3 ANALOGTEST3
GPADC4_4 — R2 ANALOGTEST4

AWR_4_NRST — P12 RESET
AWR_4_WARM_RST — N13 WARM_RESET
AWR_4_NERROR_IN — P7 NERROR_IN
AWR_4_NERROR_OUT — R9_4 0 NERROR_OUT_RS_4 — N8 NERROR_OUT

AWR_4_UART_RX — N5 RS232_RX
AWR_4_UART_TX — R11_4 33.2 UART_TX_RS_4 — N6 RS232_TX

AWR_4_SCL — P4 RESERVED
AWR_4_SDA — R13_4 33.2 SDA_RS_4 — R3 RESERVED
AWR_4_BSS_LOGGER — R14_4 33.2 BSS_LOGGER_RS_4 — R4 RESERVED
AWR_4_MSS_LOGGER — R15_4 33.2 MSS_LOGGER_RS_4 — R5 RESERVED

U1_4A — XA2243PBGABL

ClassName: AWR_POWER_ANA

VOUT_14SYNTH — A13 AWR_1V4_SYNTH_4
VOUT_14APLL1 — A10 AWR_1V4_APLL_4
VBGAP — B10 AWR_VBGAP_4
VOUT_PA — A2 AWR_VOUT_PA_4
VOUT_PA — B2

Place R188 as close as possible to VOUT_PA/RF2 pins

R188_4 0 AWR_4_1V0_RF2_FILT

Note: AWR_1V0_RF2 optionally shorted to AWR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.

R188 installed - shorts AWR_VOUT_PA to AWR_1V0_RF2 (default)
R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

CSI2_TXP[0] — G15 AWR_4_CSI2_TX0_P
CSI2_TXM[0] — G14 AWR_4_CSI2_TX0_N
CSI2_TXP[1] — H15 AWR_4_CSI2_TX1_P
CSI2_TXM[1] — H14 AWR_4_CSI2_TX1_N
CSI2_CLKP — J15 AWR_4_CSI2_CLK_P
CSI2_CLKM — J14 AWR_4_CSI2_CLK_N
CSI2_TXP[2] — K15 AWR_4_CSI2_TX2_P
CSI2_TXM[2] — K14 AWR_4_CSI2_TX2_N
CSI2_TXP[3] — L15 AWR_4_CSI2_TX3_P
CSI2_TXM[3] — L14 AWR_4_CSI2_TX3_N
HS_DEBUG1_P — M15 AWR_4_LVDS_FRCLK_P
HS_DEBUG1_M — M14 AWR_4_LVDS_FRCLK_N
HS_DEBUG2_P — N15 AWR_4_LVDS_VALID_P
HS_DEBUG2_M — N14 AWR_4_LVDS_VALID_N

QSPI_FLASH_3V3_4 — R3_4 47.5k

QSPI_CS — P8 QSPI_CS_RS_4 — R6_4 0 QSPI_CS_4
QSPI_CLK — R10 QSPI_CLK_RS_4 — R7_4 0 QSPI_CLK_4
QSPI[0] — R11 QSPI_D0_4
QSPI[1] — P9 QSPI_D1_4
QSPI[2] — P12 QSPI_D2_4
QSPI[3] — R10 QSPI_D3_4

Place termination and pull-up resistors close to QSPI controller - minimize stubs.

ClassName: AWR_QSPI

TCK — M13 AWR_4_TCK
TMS — L13 AWR_4_TMS
TDO — L13 TDO_RS_4 — R8_4 33.2 AWR_4_TDO
TDI — H13 AWR_4_TDI

ClassName: AWR_JTAG

SPI_HOST_INTR_1 — P6 SPI_HOST_INTR1_RS_4 — R10_4 33.2 AWR_4_SPI_HOST_INTR1
SPI_CLK_1 — R9 AWR_4_SPI_CLK1
SPI_CS_1 — R7 AWR_4_SPI_CS1
MISO_1 — P5 SPI_MISO1_RS_4 — R12_4 33.2 AWR_4_SPI_MISO1
MOSI_1 — R8 AWR_4_SPI_MOSI1

ClassName: AWR_GENERAL

GPIO[0] — N4 AWR_4_GPIO_0
GPIO[1] — N7 AWR_4_GPIO_1
GPIO[2] — N13 AWR_4_GPIO_2

ClassName: AWR_GENERAL

R16_4 10.0k R17_4 10.0k R18_4 10.0k — GND

SOP[2:0] Pins

NOTE: SOP (stAWRt on power) Pins
SOP[2]/PMIC_CLK_OUT
SOP[1]/SYNC_OUT
SOP[0]TDO

SOP[2:0] = 0b011 -> SOP_MODE2 "Development"
SOP[2:0] = 0b001 -> SOP_MODE3 "Funcational"
SOP[2:0] = 0b101 -> SOP_MODE5 "QSPI Flashing"

NOR QSPI FLASH (For Development Purposes)

Pull-ups disable write-protect and hold functions by default.

QSPI_FLASH_3V3_4 — R27_4 10.0k — R28_4 10.0k

QSPI_D0_4 — R30_4 0 — QSPI_D0_RS_4
QSPI_D1_4 — R31_4 0 — QSPI_D1_RS_4
QSPI_D2_4 — R32_4 0 — QSPI_D2_RS_4
QSPI_D3_4 — R33_4 0 — QSPI_D3_RS_4

QSPI_FLASH_3V3_4 — 8 VCC
QSPI_CS_4 — 1 CS
QSPI_CLK_4 — 6 SCLK
5 SI/SIO0
2 SO/SIO1
3 WP/SIO2
7 HOLD/SIO3
EP 9
GND 4

U2_4 — MX25V1635FZNQ

NOR Flash 16Mb (2M x 8) 80MHz CLK

Place termination and pull-up resistors close to QSPI flash - minimize stubs.

ClassName: SYSTEM_3V3

SYSTEM_3V3 — R29_4 0 — QSPI_FLASH_3V3_4

Flash 3.3V Power Disconnect - Use to disconnect power to flash.

C6_4 10V 10uF
C7_4 16V 1uF
C8_4 50V 0.1uF
— GND

Debug Test Header (For Development Purposes)

GPADC1_4 — R21_4 0 — GPADC1_CONN_4
GPADC2_4 — R22_4 0 — GPADC2_CONN_4
GPADC3_4 — R23_4 0 — GPADC3_CONN_4
GPADC4_4 — R24_4 0 — GPADC4_CONN_4
GPADC5_4 — R25_4 0 — GPADC5_CONN_4
GPADC6_4 — R26_4 0 — GPADC6_CONN_4

J1_4 — TSM-106-01-L-DV — GND

ClassName: AWR_DEBUG

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TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: AWR_1	
Custom Rev:		Assembly VAWRiant:	Sheet:10of 19
Drawn By:a0271760		File: PROC054D_AWR_Interfaces.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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References
http://www.ti.com/product/AWR2243

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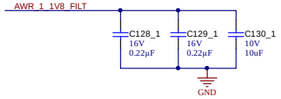
AWR Power - BGA Decoupling

VIN_18BB SUPPLY



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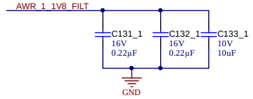

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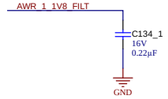

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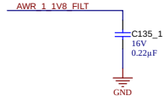

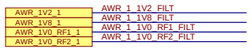

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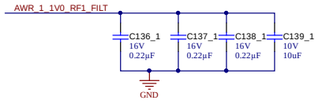

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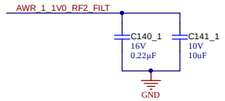

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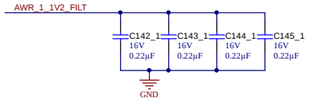

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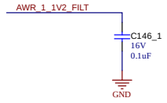

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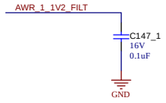

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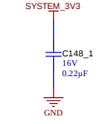
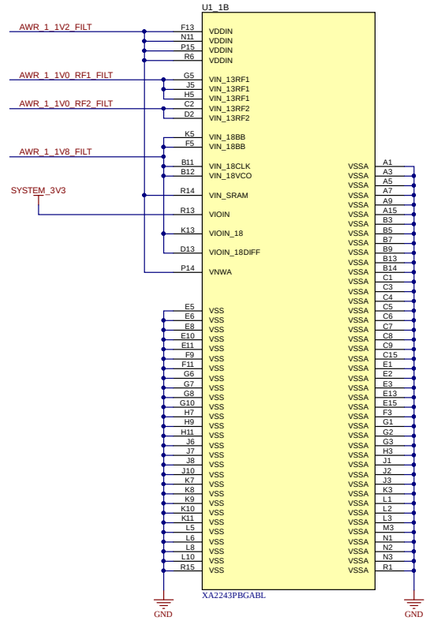


AWR Power



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TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: DECOUPLING_CAPS_1	
Custom Rev:		Assembly VAWRiant:	Sheet: 11 of 19
Drawn By: a0271760		File: PROC054D_AWR_Power_Decoupling.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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References
http://www.ti.com/product/AWR2243

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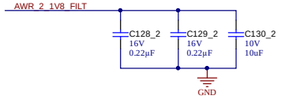
VIN_18BB SUPPLY



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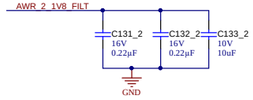

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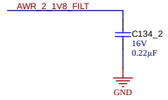

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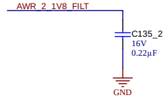

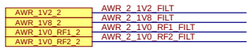

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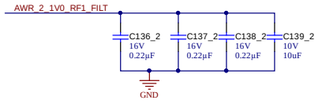

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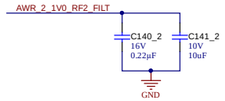

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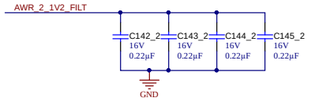

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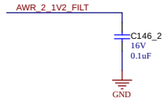

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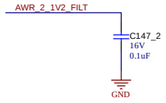

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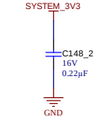
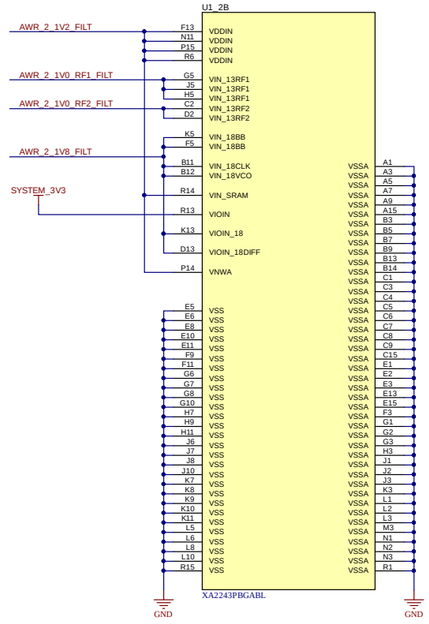


AWR Power



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Number: PROC054	Rev: D	Sheet Title: DECOUPLING_CAPS_1	
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Drawn By:a0271760		File: PROC054D_AWR_Power_Decoupling.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

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References
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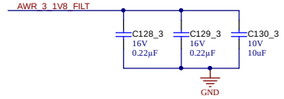
VIN_18BB SUPPLY



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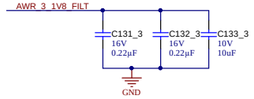

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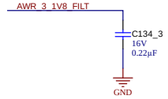

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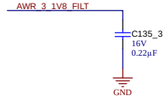

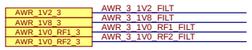

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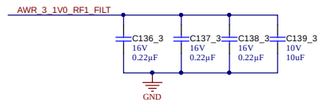

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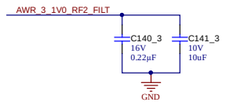

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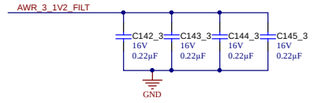

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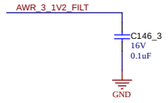

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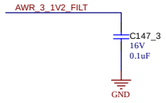

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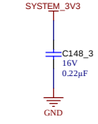
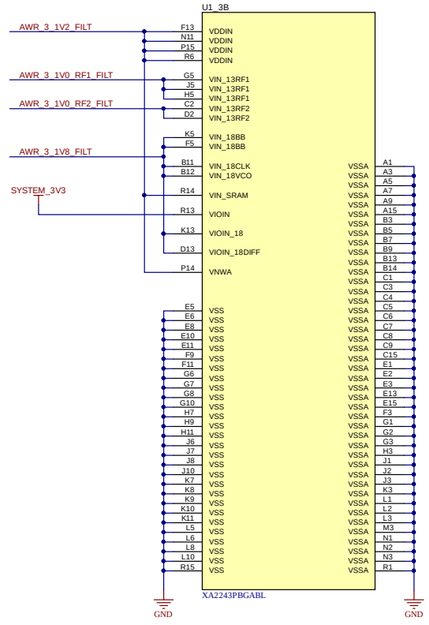


AWR Power



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Drawn By:a0271760		File: PROC054D_AWR_Power_Decoupling.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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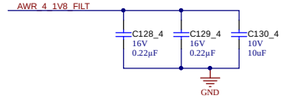
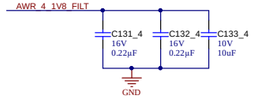
VIN_18BB SUPPLY



VIN_18VCO, VIN_18CLK SUPPLY



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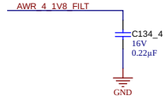

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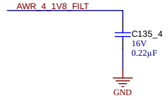

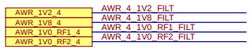

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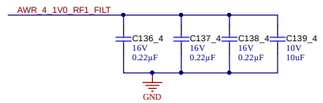

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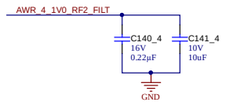

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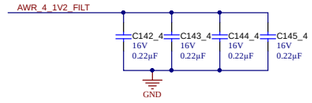

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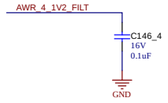

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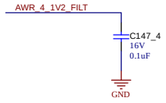

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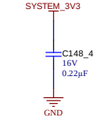

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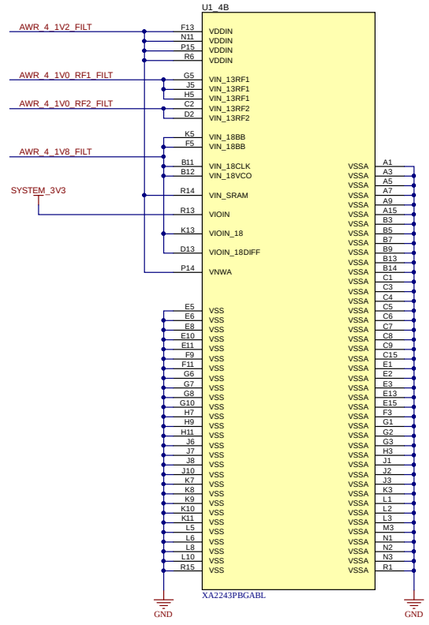

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 1/20/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: DECOUPLING_CAPS_1	
Custom Rev:		Assembly VAWRiant:	Sheet:11 of 19
Drawn By:a0271760		File: PROC054D_AWR_Power_Decoupling.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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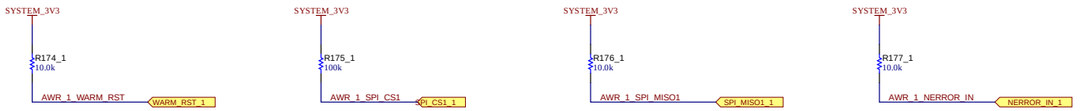
References
http://www.ti.com/product/AWR2243

AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



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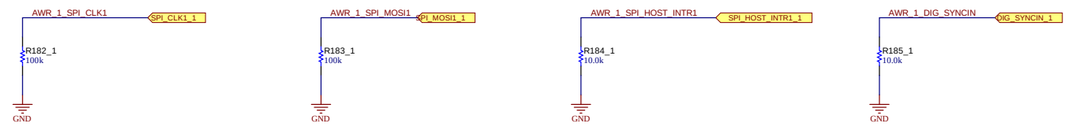

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Drawn By:a0271760	File: PROC054D_AWR_Pull_Resistors.SchDoc	Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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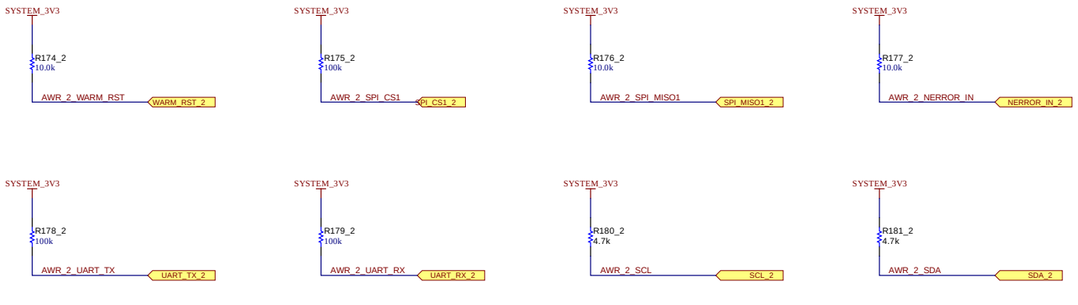
AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



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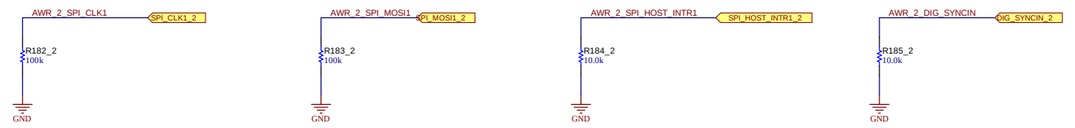

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Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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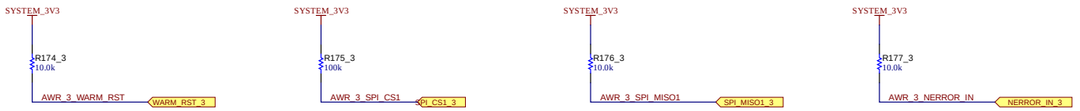
AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



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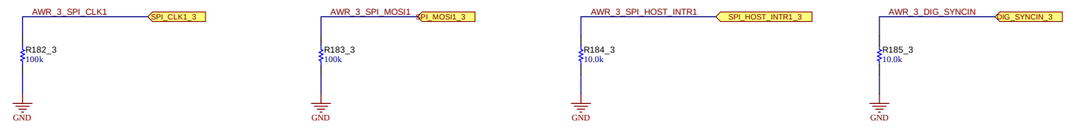

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Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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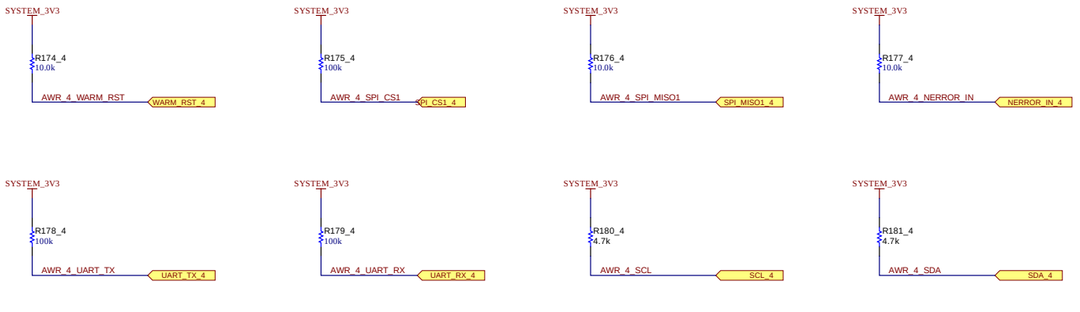
AWR Radar SoC - Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



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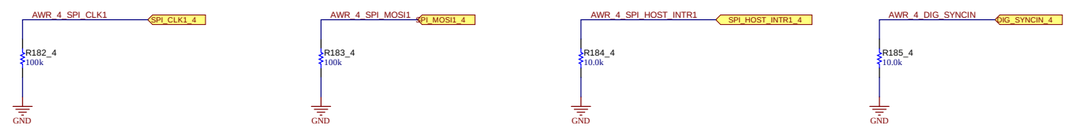

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Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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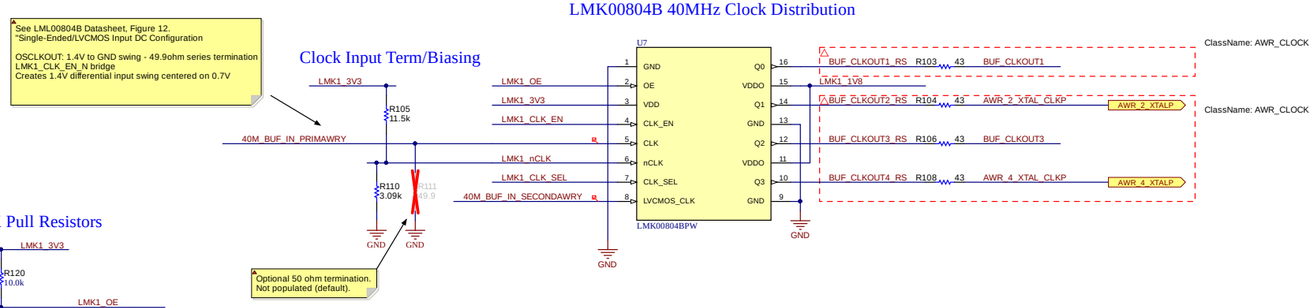
40 MHz Clock Generation and Distribution

References

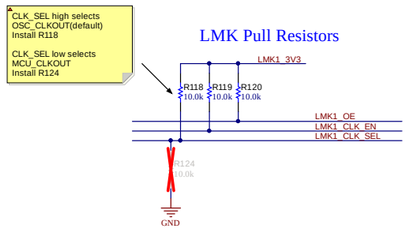
LMK00804BEVM User's Guide

LMK00804B 40MHz Clock Distribution

Clock Input Term/Biasing



LMK Pull Resistors



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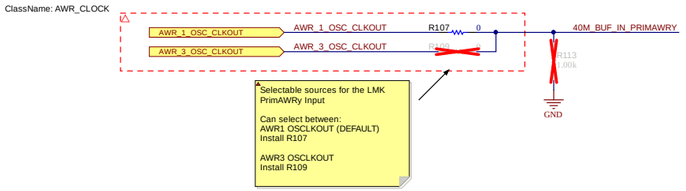

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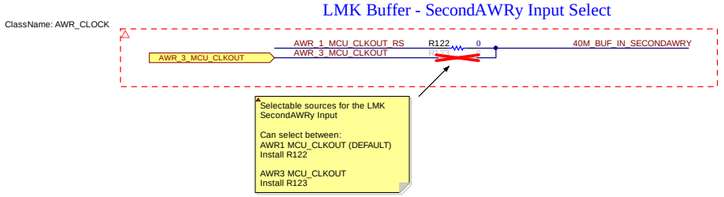

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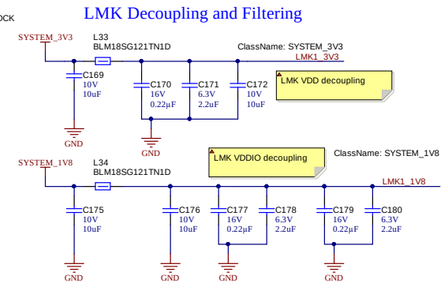

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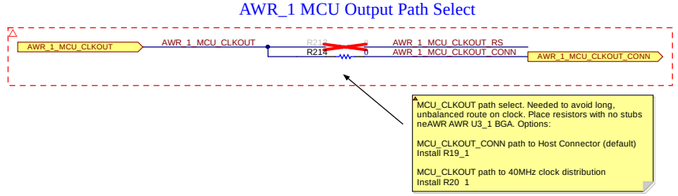

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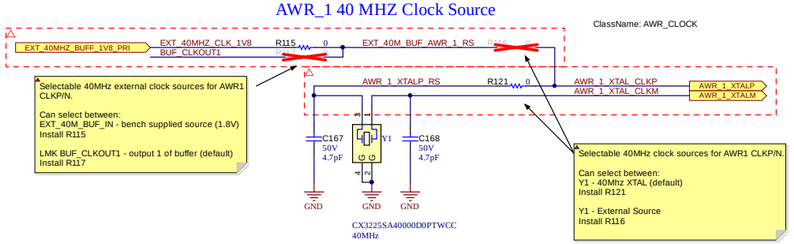
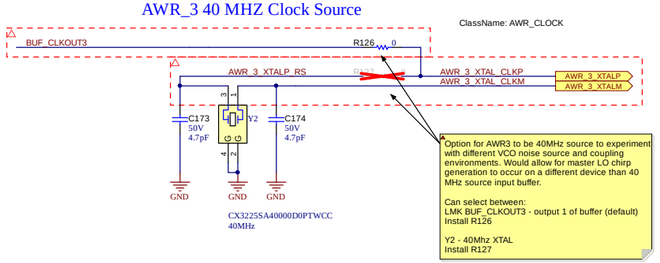
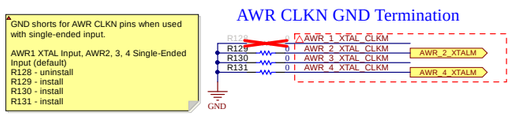


AWR_3 40 MHZ Clock Source



AWR CLKN GND Termination



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Orderable: MMW_CAS_RF_EVM		Designed for: Public Release	Mod. Date: 1/17/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: 40MHZ_CLOCK_1	
Drawn By: a0271760		Assembly VariAWRant:	Sheet: 13 of 19
Engineer: a0271760		File: PROC054D_40MHZ_Clock.SchDoc	Size: C
		Contact: http://www.ti.com/mmwave	http://www.ti.com

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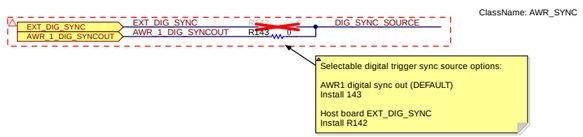
References

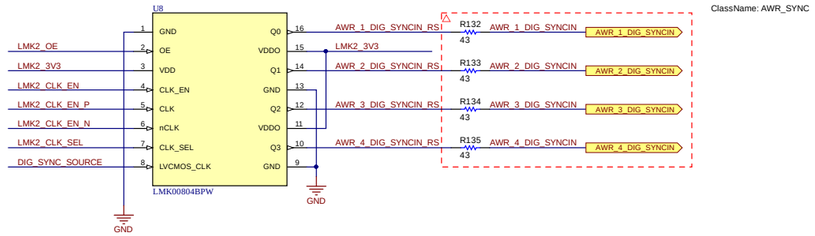
LMK00804BEVM User's Guide

Digital Sync Trigger and 20GHz LO Distribution

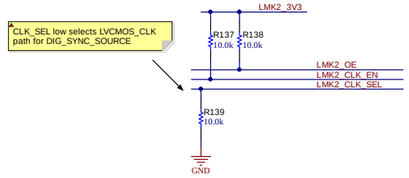
Digital Sync Source Select



LMK00804B Digital Sync Distribution



LMK Pull Resistors



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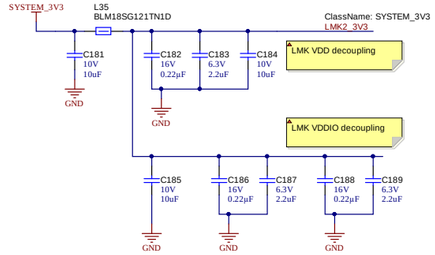

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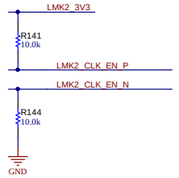

FMCW 20GHz LO SYNC

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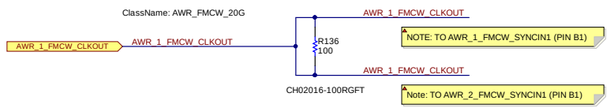

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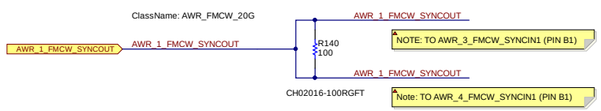

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TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: FMCW_SYNC	
		Assembly VAWRiant:	Sheet:14of 19
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Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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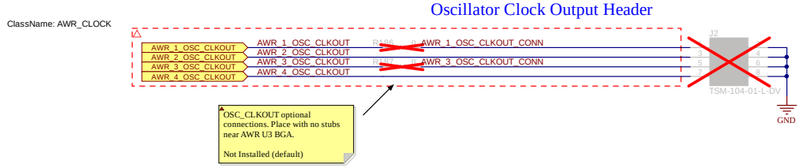
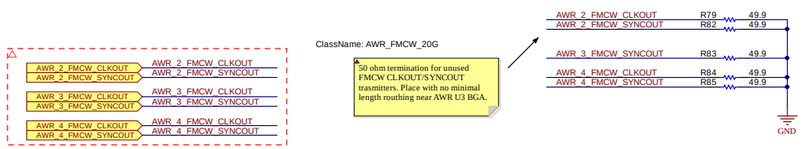
Test Headers, Connectors and Terminations

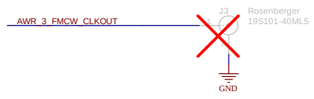
Oscillator Clock Output Header



Unused 20GHz LO Output Termination



20GHz LO Test Output



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Number: PROC054 Rev: D	Sheet Title: SMA_SMP_CONNECTORS	
Variant: Rev:	Assembly VAWRiant:	Sheet 15of 19
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Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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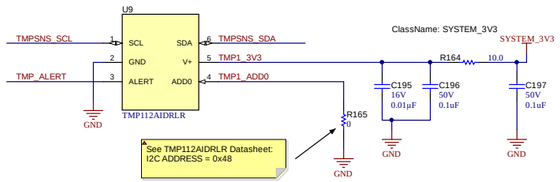
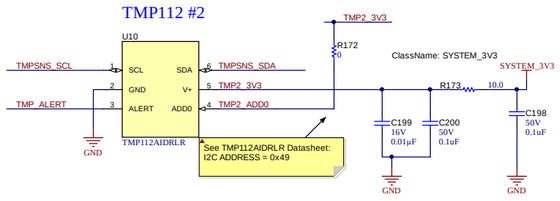
System Temperature Sensors

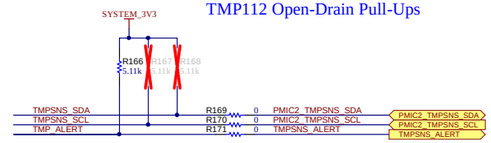
TMP112 #1



TMP112 #2



TMP112 Open-Drain Pull-Ups



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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 1/17/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: ON_BRD_TEMP_SENSOR	
Custom Rev:		Assembly VAWRiant:	Sheet: 16 of 19
Drawn By: a0271760		File: PROC054D_Temp_Sensor.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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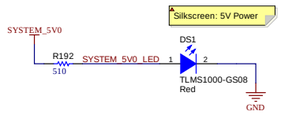
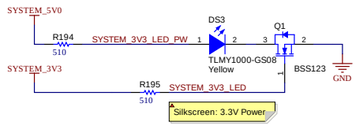
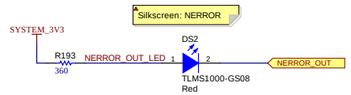
System Indicator LED

POWER LEDS

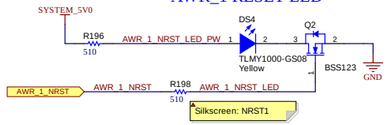




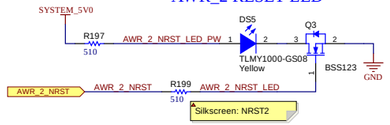
ERROR LEDS



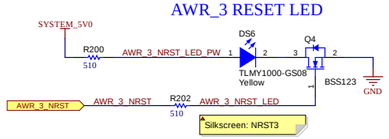
AWR_1 RESET LED



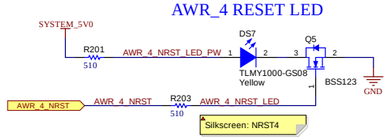
AWR_2 RESET LED



AWR_3 RESET LED



AWR_4 RESET LED



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Orderable: MMW_CAS_RF_EVM	Designed for: Public Release	Mod. Date: 2/6/2020
TID #: N/A	Project Title: MMWCAS-RF-EVM	
Number: PROC054 Rev: D	Sheet Title: SYSTEM_LED	
Customer Rev:	Assembly VAWRiant:	Sheet: 17 of 19
Drawn By: a0271760	File: PROC054D_System_LED.SchDoc	Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave	

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Hardware, Mounting Holes and Logos

FID1 FID2 FID3 FID4 FID5 FID6

PCB Number: PROC054
PCB Rev: D

PCB LOGO
Texas Instruments

CE MAWRk

PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

PCB LOGO
ESD Susceptible

CAUTION HOT SURFACE

ZZ1
Assembly Note
These assemblies AWRe ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standAWRds IPC-A-610 Class 2, unless otherwise specified.

ZZ4
Assembly Note
R136/R140 require special attention due to no solder-mask RF construction. For any questions, please contact TI design team.

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 2/10/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: HAWRdwAWRe	
Sub Rev: 1df32a29e7cc7fa2fde6928ae0b7d4ff7e37		Assembly Variant: Area [Locally Modified]	Sheet:18 of 19
Drawn By:a0271760		File: PROC054D_EVM_Hardware.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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Cascade Radar RF Board - Revision History

Revision History			
Rev	**Date**	**Released By**	**Notes**
1	2018/07/09	Randy Rosales <rosales.r@ti.com>	Initial release for layout cleanup and internal review.
2	2018/07/17	Randy Rosales <rosales.r@ti.com>	Updating based on 2018/07/09 comments. Combined PMIC_BUCK_EN and PMIC_NRST Combined PMIC1_PGOOD and PMIC2_PGOOD into single SYSTEM_PGOOD Updating NRST generation scheme from LP87524P PMIC Created sepAWRate AWR_X reset generation paths Combined GPIO2 and PGOOD into PGOOD net Removing leftover resistor selection options from the previous LDO and PMIC power paths. Removing first level LC filtering options from the previous LDO and PMIC power paths. Removed: L3, L6, L19, L22 Removed: C21, C29, C78, C86 Removed: C21, C29, C78, C86 This also removed a few power net segments which will now be fed directly from PMIC output Combined AWR_1_1V8_FILT and AWR_4_1V8_FILT into AWR_14_1V8_FILT Combined AWR_2_1V8_FILT and AWR_3_1V8_FILT into AWR_23_1V8_FILT Changing XWR LC filter to use TDK NLCV32T-R10M-EFRD identified by power team analysis PMIC1_AWR_14_1V8 now directly feeds into SYSTEM_1V8 supply - there was no reason to run this through XWR 1.8V LC filter. Added SYSTEM_5V0 to 3.3V resistor divider for LP87524 PMIC pull-up resistors Updated U2 to the Macronix MX25V1635FZNQ - aligning with other XWR EVM kits Removed R125 - Optional resistor remaining from previously removed option for alternative XTAL input Changed NERROR_OUT LED bias to SYSTEM_3V3 Updated coversheet block diagram Updated power distribution block diagram
2	2018/07/17	Randy Rosales <rosales.r@ti.com>	Added variant information for do not populate stuffing options.
3	2018/07/18	Randy Rosales <rosales.r@ti.com>	Removed 50 ohm terminations to ground at the J2 OSCCLK_OUT test header Removed test headers on PMIC output rails Added zero-ohm resistor between PMIC GPIO3 and PGOOD Replaced all note, class and netname instances of AWR with XWR for industrial/automotive alignment of schematics Replaced all series termination on LMK00804B output with 43 ohm resistors per LMK00804B datasheet Replaced XWR reset generation circuit with discrete AND gate Required for achieving clean reset of XWR devices across all device mAWRgins Netname error on XWR SPI interface - MISO netname change R112 and EXT_40MHZ_CLK_1V8 removed - this was an alternative clock path that is no longer supported Eliminated RF1/2 channel naming error in PROC054_System_Power.SchDoc and PROC054_System_Top.SchDoc
4	2018/07/21	Randy Rosales <rosales.r@ti.com>	Changed R54 to pull-up resistor. LP87524P GPIO2 and GPIO3 both configured as open-drain output.
5	2018/07/21	Randy Rosales <rosales.r@ti.com>	Added 10kohm pull-up to LP87524P GPIO3 - required after change separating out GPIO3 and PGOOD nets Aligned PMIC1 and PMIC2 RF1 and RF2 LC filter components with 1.2V and 1.8V filter Previous RF1 and RF2 LC values were still not merged from removal of LDO option separation of RF1 and RF2 supplies
6	2018/07/28	Randy Rosales <rosales.r@ti.com>	Changing all layout critical resistors and capacitors to small-outline version in Altium Vault libraryy Required to allow Tessolve to implement original decoupling and series resistor layout near the AWR BGA Will allow for more compact routing throughout the design as well Changed R136, R140 FMCW LO power divider resistor to RF resistor CH02016-100RJFT Changed U3 and U4 PMIC to reference proper P-version in Altium vault. Adding zero-ohm resistors to AWR_1/2/3/4 I2C interfaces, optionally shorting those interfaces to the PMIC1_I2C Changed NERROR_OUT LED to sourced from shorted NERROR_OUT Originally being fed AWR_1_ERROR_OUT
7	2018/08/08	Randy Rosales <rosales.r@ti.com>	Added R188 which shorts AWR_VOUT_PA to AWR_1V0_RF2 supply nets. Recommended for supporting increased current into the RF2 supplies in 1.0V mode supporting simultaneous 3 TX operation
8	2018/08/09	Randy Rosales <rosales.r@ti.com>	Added burn danger logo Added ESD danger logo Consolidated FMCW 20G LO, digital sync and clock net classes. Created the following net classes: AWR_FMCW_20G AWR_CLOCK AWR_SYNC Removed extraneous MCU_CLKOUT_CONN path from XWR2, XWR3 and XWR4 Consolidated XWR1 MCU_CLKOUT path output options on PROC054_40MHZ_CLK1 schematic sheet Renamed schematic PROC054_40MHZ_FMCW_SYNC to PROC054_FMCW_SYNC Aligned antennas with AWR prefix naming convention Added all nets on 40MHZ_CLOCK_1 schematic sheet to netclass XWR_CLOCK
9	2018/08/10	Randy Rosales <rosales.r@ti.com>	Added additional nets to the AWR_SYNC net class Added additional nets to the AWR_FMCW_20G net class Replaced J3 with correct Rosenberger 19S101 part from TI Altium Vault.
10	2018/08/16	Randy Rosales <rosales.r@ti.com>	Added additional R19 and R20 0-ohm resistors to create optional feedback path for bench supply connector P3
11	2020/01/16	Randy Rosales <rosales.r@ti.com>	Revision D updates Changing primary IC (U1_1, U1_2, U1_3 and U1_4) to AWR2243P Cleaning up net names, ports, net classes, and notes to reference AWR vs. AWR12 specificially

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Orderable: MMW_CAS_RF_EVM		Designed for:Public Release	Mod. Date: 2/6/2020
TID #: N/A		Project Title: MMWCAS-RF-EVM	
Number: PROC054	Rev: D	Sheet Title: Revision History	
Cust Rev:		Assembly VAWRiant:	Sheet:19 of 19
Drawn By:a0271760		File: PROC054D_Revision_History.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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