STACKUP TABLE:

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.80mil	3.5	
1	L1 TOP	Copper	1.60mil		
	Dielectric 1	RO3003	5.00mil	3	
2	L2 GND	Copper	0.80mil		
	Dielectric2	RO4450F	5.00mil	4.2	
3	L3 SIGNAL 1	Copper	0.60mil		
	Dielectric3	RO4835 LOPRO	10.70mil	3.66	
4	L4 GND	Copper	0.60mil		
	Dielectric4	370HR	5.00mil	4.2	
5	L5 SIGNAL 2	Copper	1.20mil		
	Dielectric5	370HR	10.00mil	4.34	
6	L6 SIGNAL 3	Copper	0.60mil		
	Dielectric6	370HR	5.00mil	4.2	
7	L7 GND	Copper	0.80mil		
	Dielectric7	370HR	5.00mil	4.34	
8	L8 BOTTOM	Copper	1.60mil		
	Bottom Solder	Solder Resist	0.80mil	3.5	
	Bottom Overlay				

THIS IS AN IMPEDANCE CONTROLLED BOARD

NOTE:
1. EXTERNAL LAYER CU THICKNESS ARE FINISHED THICKNESS AFTER PLATING.

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.

2. THE SOLDER MASK IMAGES THAT ARE THE SAME SIZE AS THE COMPONENT PADS MAY BE ENLARGED AS
   PER THE MANUFACTURING CAPABILITIES BUT NOT BEYOND 0.08MM PER SIDE OR 0.15MM OVERALL.
   ALL OTHER SOLDER MASK IMAGES SHALL NOT BE MODIFIED.

3. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL
   FOR ETCHING ACCURACY NEAR THE ANTENNA REFER "ANTENNA_ETCHING_REQUIREMENTS" DOCUMENT

4. 5.9MIL VIA ONLY ON PAD SHOULD BE FILLED WITH CONDUCTIVE COPPER AND SURFACE SHOULD BE FLAT.
   FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON TOP SIDE.

5. BACKDRILLING INFO: 12 MIL DRILL AND 24 MIL PAD NEED TO BE REMOVED FROM THE BOTTOM TO LAYER 4
   USE 24MIL DRILL BIT FOR BACKDRILLING ABOVE MENTIONED DRILLS. VENDOR MUST CUT L4 AND MUST NOT CUT L3.

6. PRINTED WIRING BOARD SHALL COMPLY WITH REQUIREMENTS OF ANSI/J-STD-003.

7. BOW AND TWIST SHALL NOT EXCEED 0.7% OF LONGEST SIDE

8. R136/R140 REQUIRE SPECIAL ASSEMBLY ATTENTION DUE TO THEIR NO SOLDER-MASK, RF CONSTRUCTION.

9. FOR ANY ASSEMBLY OR FABRICATION QUESTIONS PLEASE CONTACT THE RESPONSIBLE TI PCB DESIGN TEAM.

IMPEDANCE TABLE

LAYER	TRACE WIDTH (mil)	TRACE SPACING (mil)	IMPEDANCE
1	10.5	–	50 OHM +/-10%
1	6.5	5.5	100 OHM +/-10%
3	5.1	–	50 OHM +/-10%
5	12	–	50 OHM +/-10%
6	6.9	–	50 OHM +/-10%
6	6.9	7	100 OHM +/-10%
8	7.75	–	50 OHM +/-10%
8	5.25	6.75	100 OHM +/-10%

DRILL TABLE: (L1-L8)

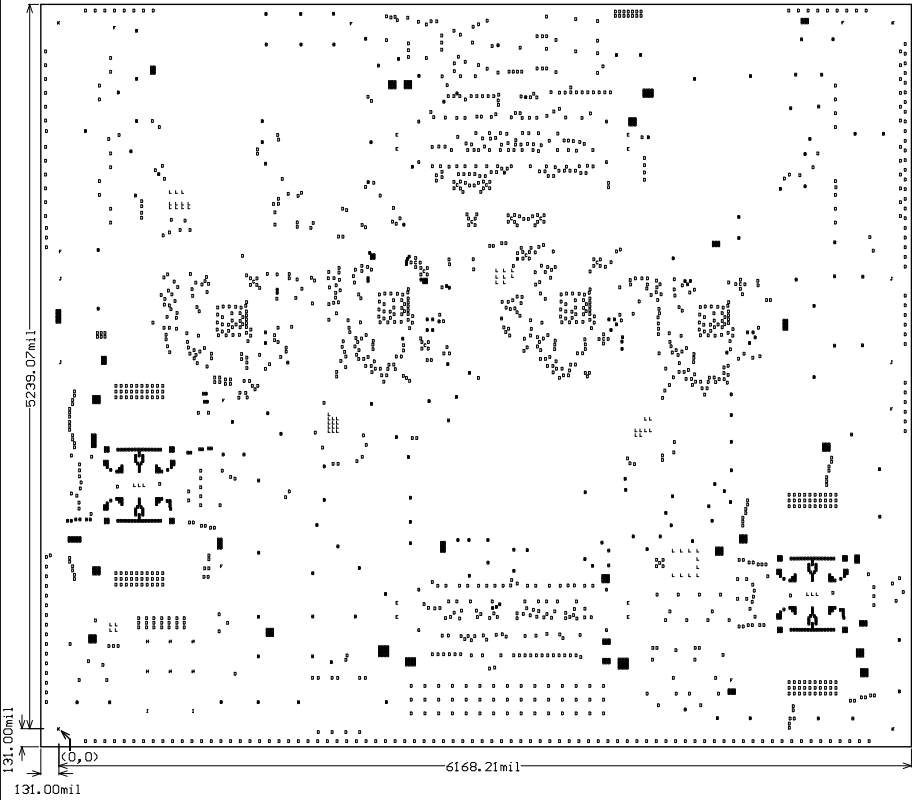| Symbol	Count	Hole Size	Drill Layer Pair	Plated	Hole Tolerance(mil)
L	60	7.87mil (0.200mm)	L1 TOP - L8 BOTTOM	PTH	+0/-7.87
B	727	8.00mil (0.203mm)	L1 TOP - L8 BOTTOM	PTH	+0/-8
C	13	12.00mil (0.305mm)	L1 TOP - L8 BOTTOM	PTH	+0/-12
D	1522	12.20mil (0.310mm)	L1 TOP - L8 BOTTOM	PTH	+0/-12.2
E	8	39.37mil (1.000mm)	L1 TOP - L8 BOTTOM	PTH	+4/-0
F	8	40.00mil (1.016mm)	L1 TOP - L8 BOTTOM	PTH	+/-3
G	8	47.24mil (1.200mm)	L1 TOP - L8 BOTTOM	PTH	+4/-0
H	6	70.87mil (1.800mm)	L1 TOP - L8 BOTTOM	PTH	+/-2
I	2	118.11mil (3.000mm)	L1 TOP - L8 BOTTOM	NPTH	+/-2
J	4	118.11mil (3.000mm)	L1 TOP - L8 BOTTOM	PTH	+/-3
K	4	160.00mil (4.064mm)	L1 TOP - L8 BOTTOM	PTH	+/-3
	2362 Total				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4 MIL
MIN. VIA PAD SIZE: 13.77 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 2 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER REFER STACKUP
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER 55MIL +/-10%
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [ ] ANSI IPC-6012 TYPE 3 CLASS 2
[X] OTHER +/- REFER NOTE 7

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER RED
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
[X] MM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS
TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE:
MMWCAS-RF-EVM
DESIGNED FOR:
Public Release
FILE NAME:
PROCO54D_MMWCAS_RF_EVM.PcbDoc

ENGINEER: a0271760	LAYOUT BY: Tessolve/TI
SCALE: 0.54	ALTIUM DESIGNER VERSION: 19.1.6.110

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = Board Dimensions
BOARD #: PROCO54   REV: D
SVN REV: 1df32a29e7cc7fa2fde6928ffd21bd41b67e37ea [Locally Modified]
GENERATED : 2/10/2020 6:05:52 PM
TEXAS INSTRUMENTS

WO#307308-7306-D

SHEET 1/2

5239.07mil
131.00mil
(0,0)
6168.21mil
131.00mil

Symbol	Count	Hole Size	Drill Layer Pair	Plated	Hole Tolerance(mil)
A	5523	5.90mil (0.150mm)	L1 TOP - L2 GND	PTH	+0/-5.9
	5523 Total				

DRILL TABLE: (L1-L2)

TEXAS INSTRUMENTS

PROJECT TITLE:
MMWCAS-RF-EVM

DESIGNED FOR:
Public Release

FILE NAME:
PROC054D_MMWCAS_RF_EVM.PcbDoc

ENGINEER: a0271760	LAYOUT BY: Tessolve/TI
SCALE: 0.54	ALTIUM DESIGNER VERSION: 19.1.6.110

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = ABP Board Dimensions

BOARD #: PROC054   REV: D

SVN REV: 1df32a29e7cc7fa2fde6928lfd21bd41b67e37ea [Locally Modified]

GENERATED   : 2/10/2020   6:05:59 PM

TEXAS INSTRUMENTS

WO#307308-7306-D

SHEET 2/2

5239.07mil
6168.21mil
131.00mil
131.00mil
(0,0)