

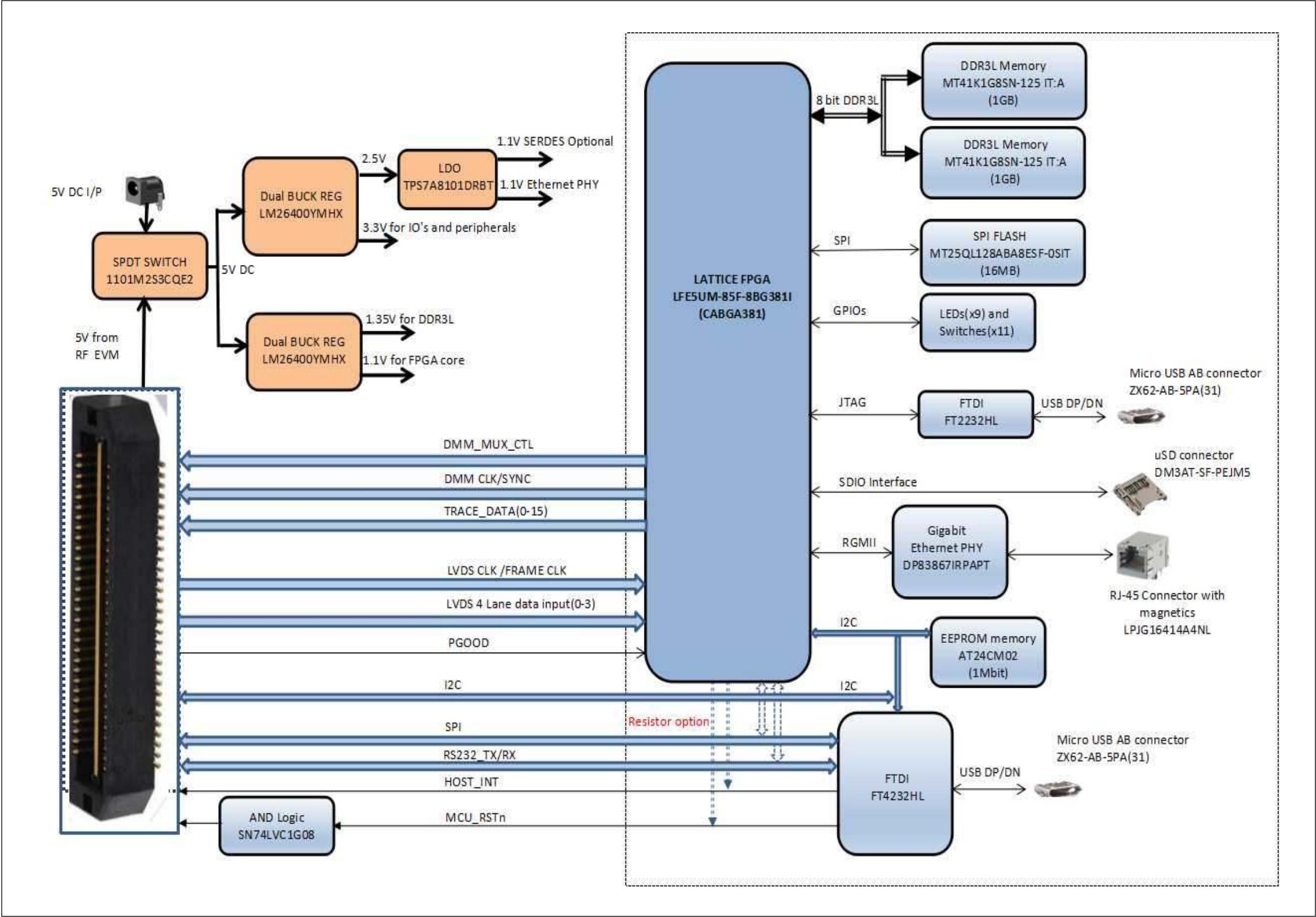
DCA1000EVM

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REV.	A
VERSION	1.00

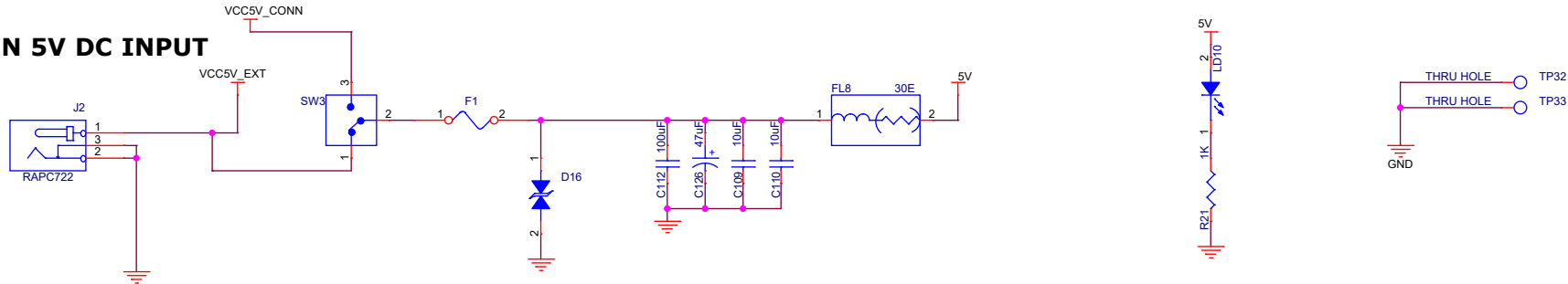
VERSION HISTORY					
VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.10	06 DEC 2017	MODIFICATION DONE TO REV-E1 SCHEMATICS AS PER BELOW CHANGES, 1. VCC_CORE SUPPLY FEEDBACK RESISTOR VALUES CHANGED IN PAGE 4. 2. AUTO NEGOTIATION RESISTORS ADDED IN PAGE 08. 3. SPI MISO & MOSI SIGNALS SWAPPED IN PAGE 12. 4. UART TX & RX SIGNALS SWAPPED IN PAGE 12.	BALA	ALAGAPPAN	ALAGAPPAN
1.00	26 DEC 2017	REVIEWED & BASELINED	BALA	ALAGAPPAN	ALAGAPPAN

BLOCK DIAGRAM

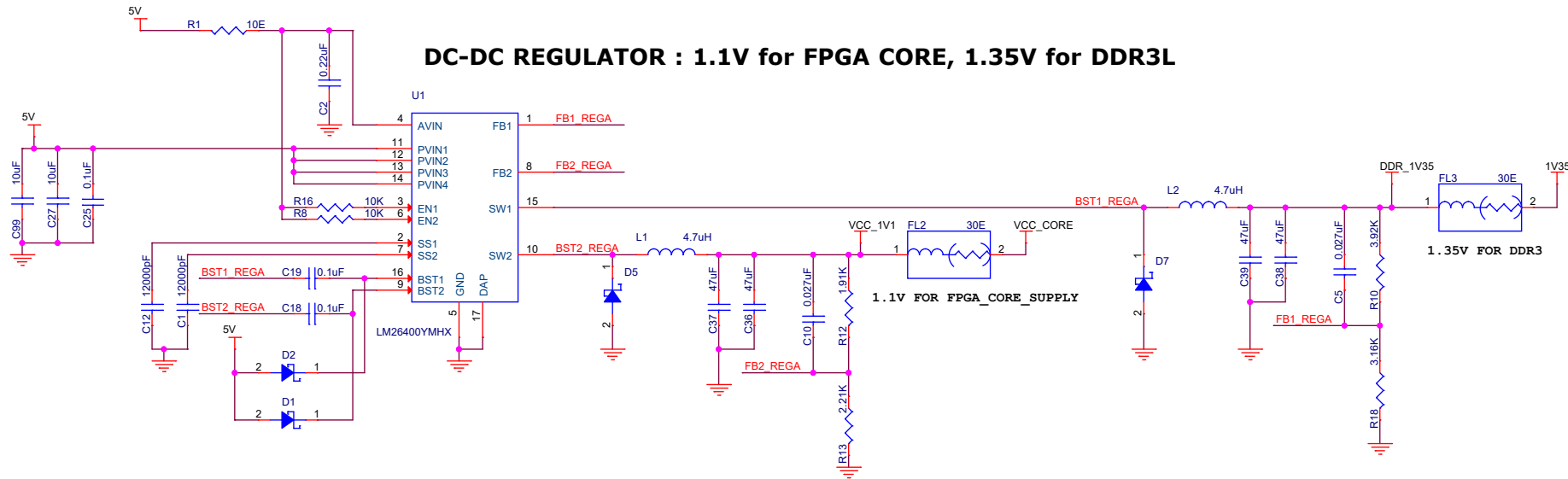


POWER_SECTION

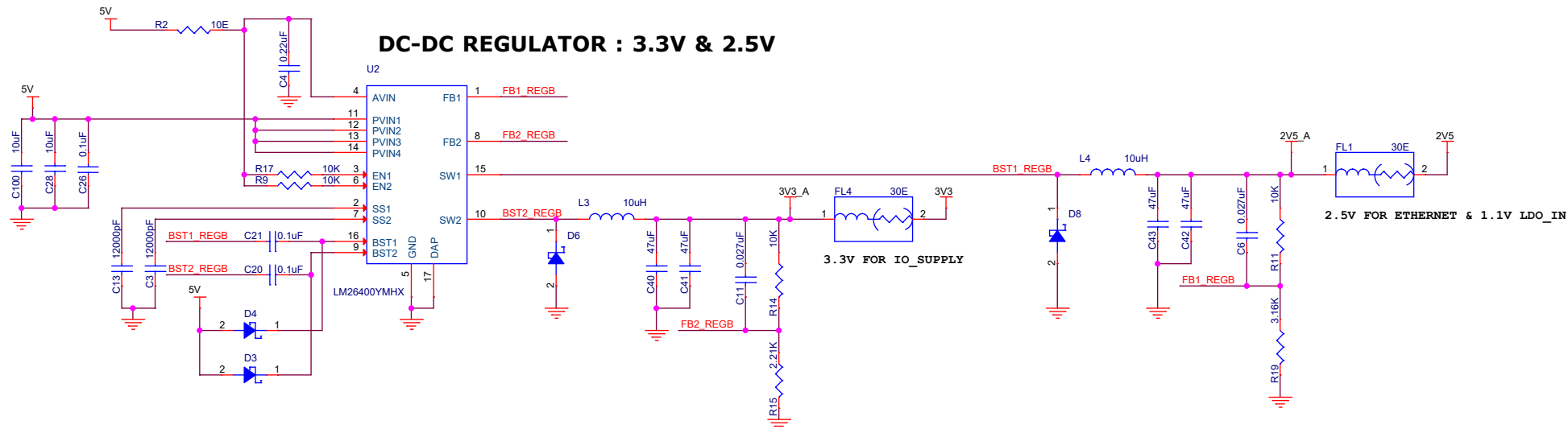
MAIN 5V DC INPUT



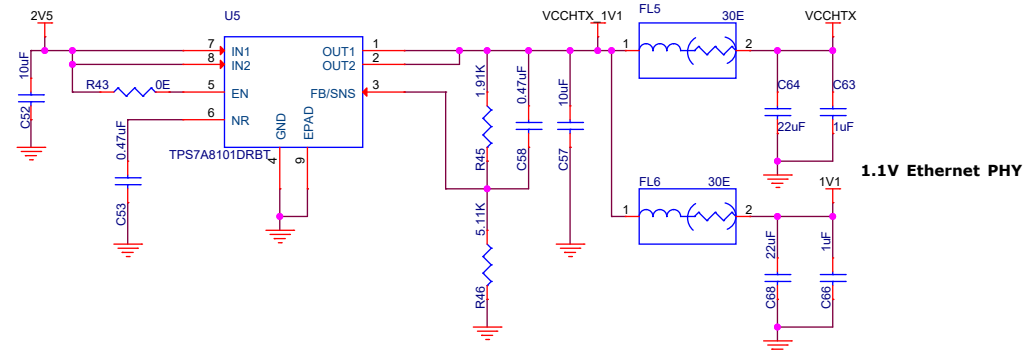
DC-DC REGULATOR : 1.1V for FPGA CORE, 1.35V for DDR3L



DC-DC REGULATOR : 3.3V & 2.5V

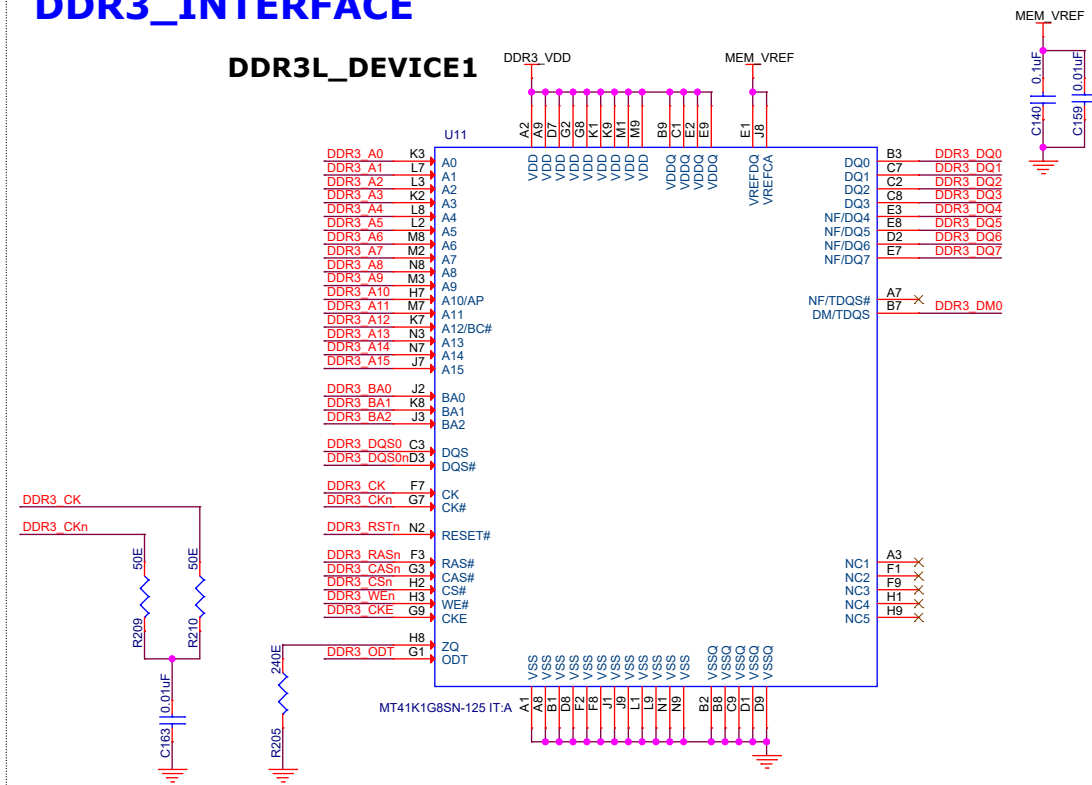


LDO REGULATOR : 1.1V

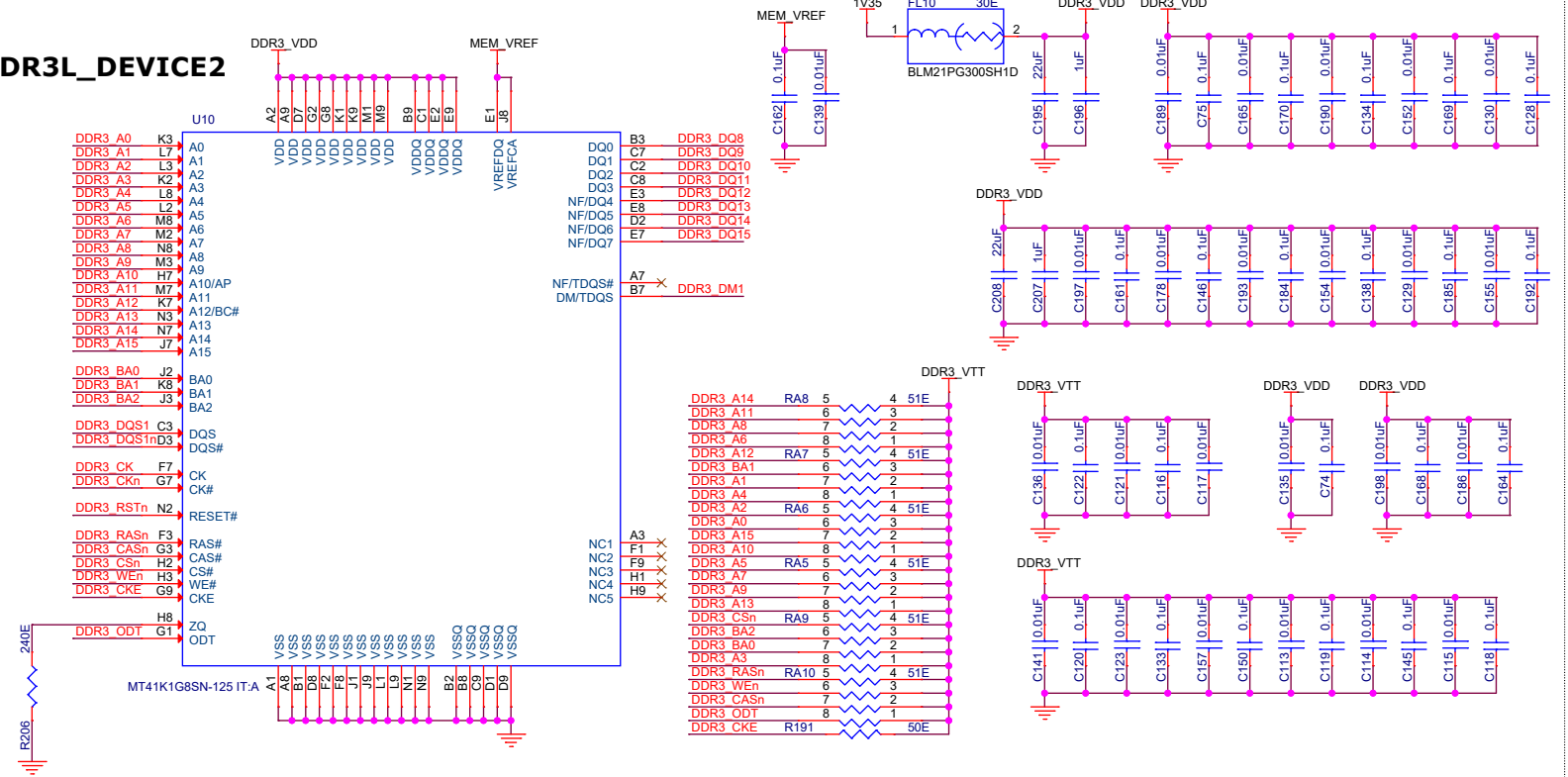


DDR3_INTERFACE

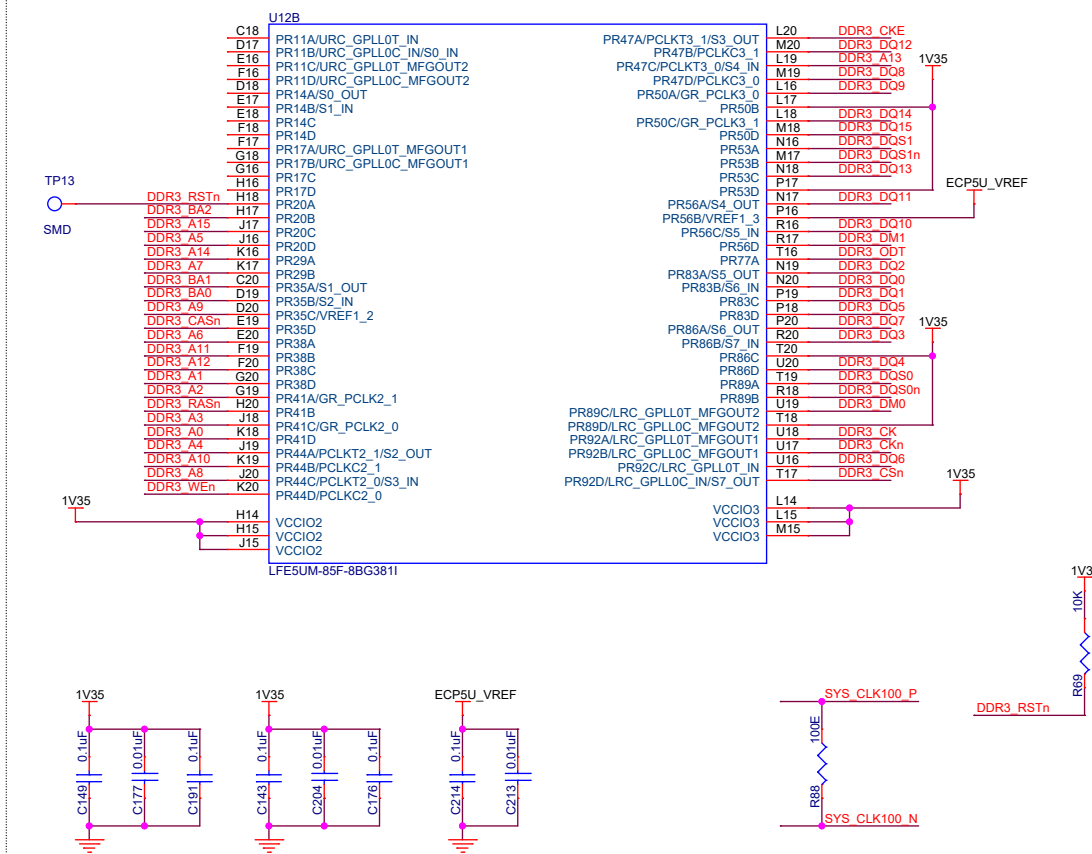
DDR3L_DEVICE1



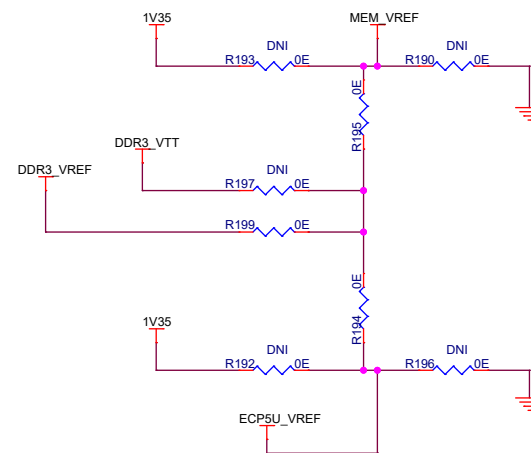
DDR3L_DEVICE2



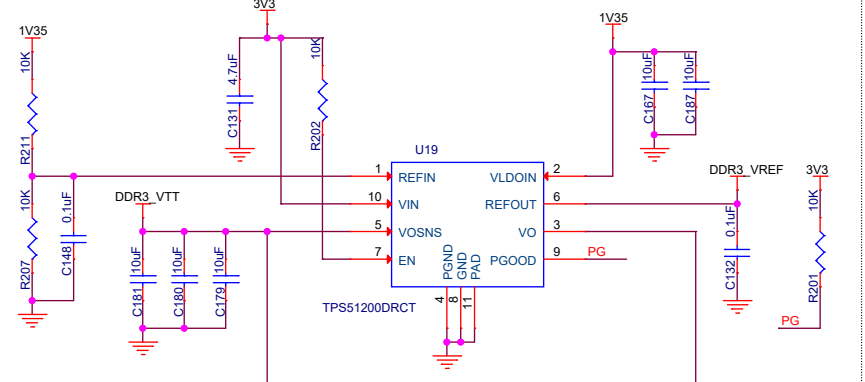
FPGA_DDR3_BANK_2&3



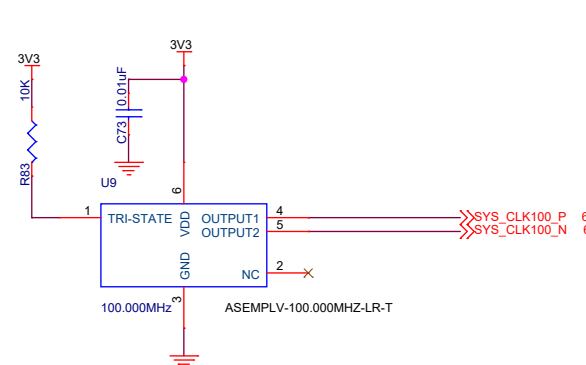
DDR3_VREF_SUPPLY_SEL



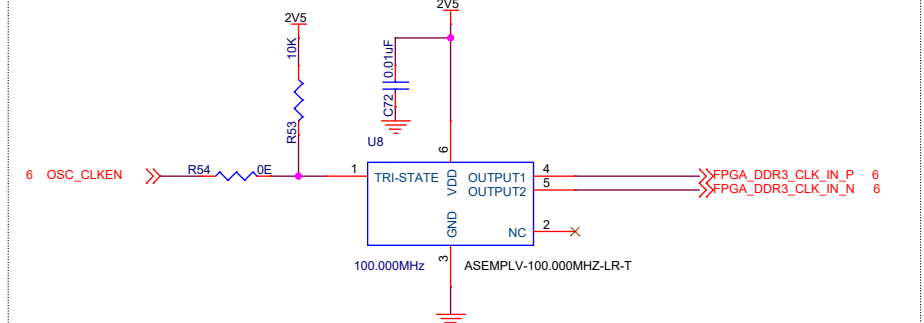
DDR3_VREF&VTT_REGULATOR



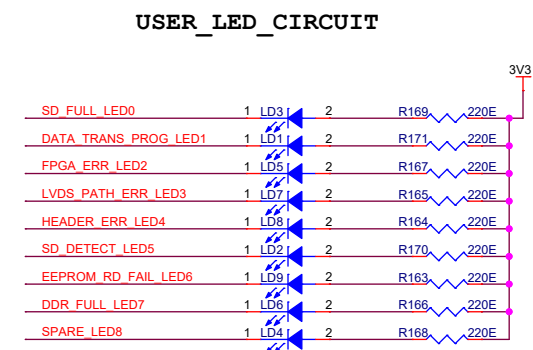
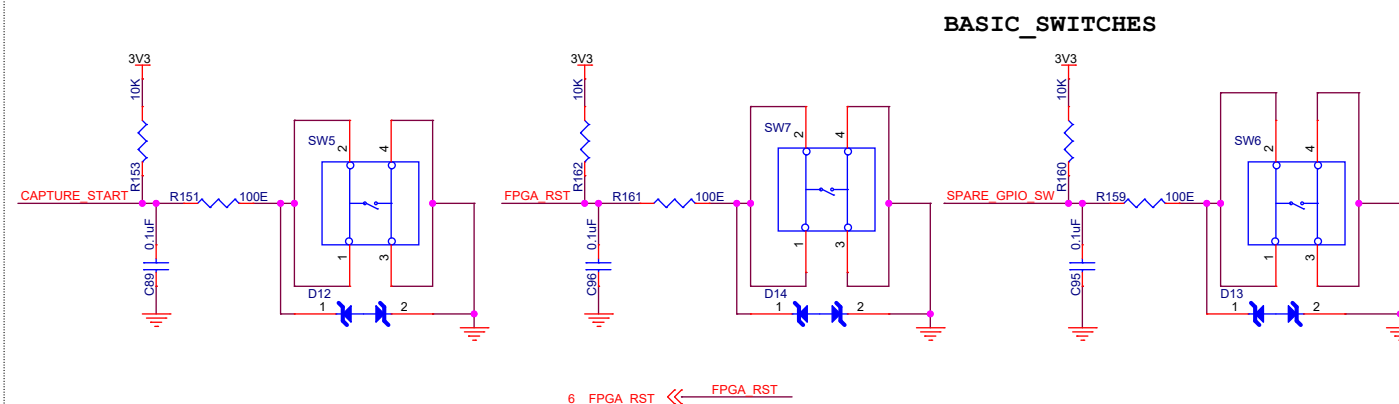
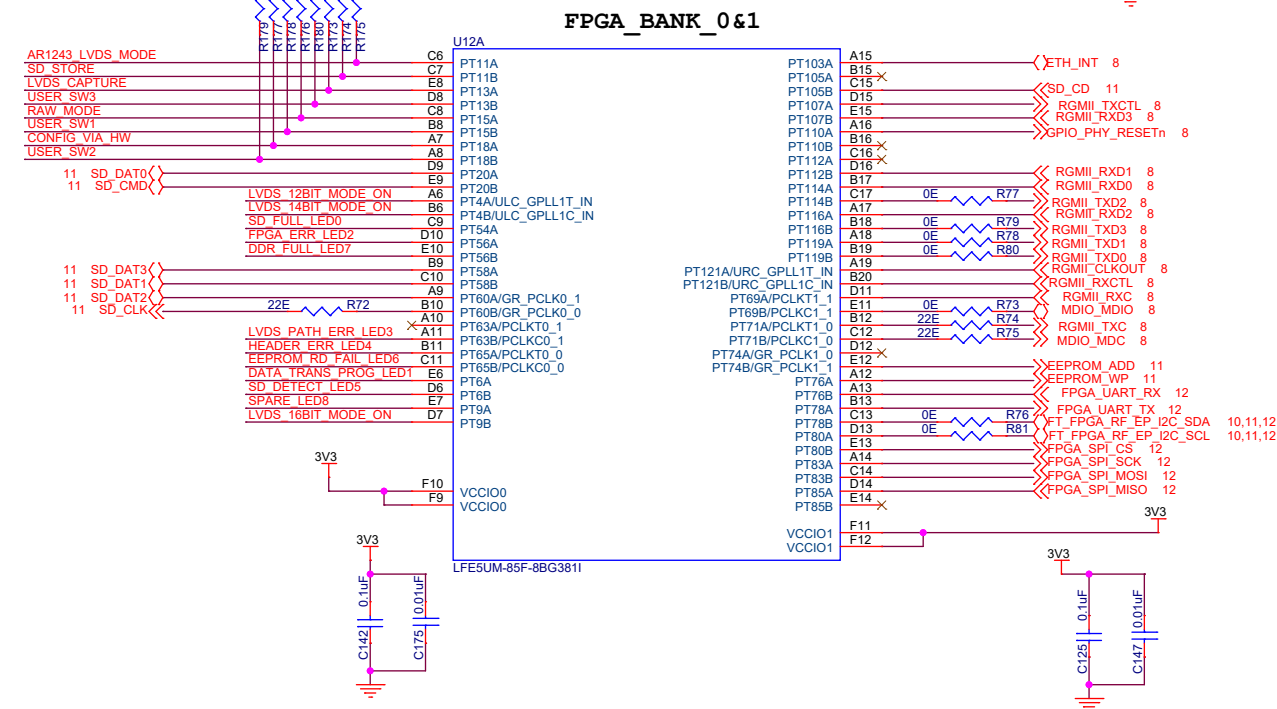
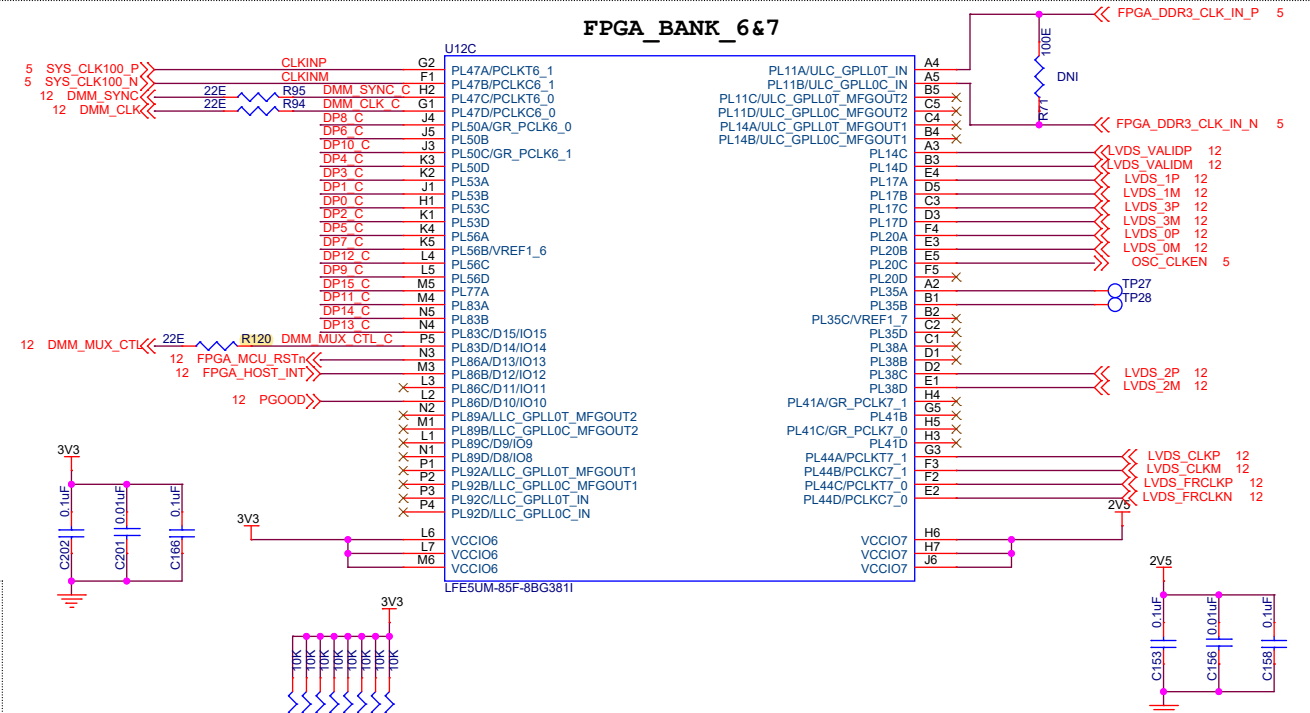
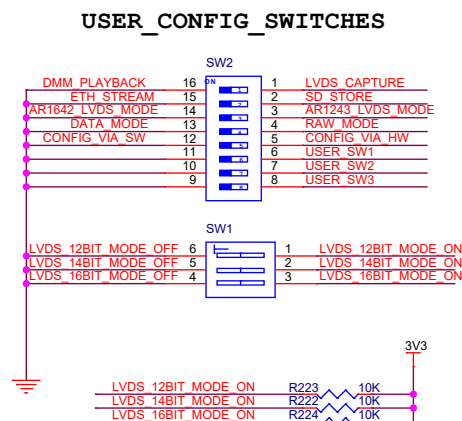
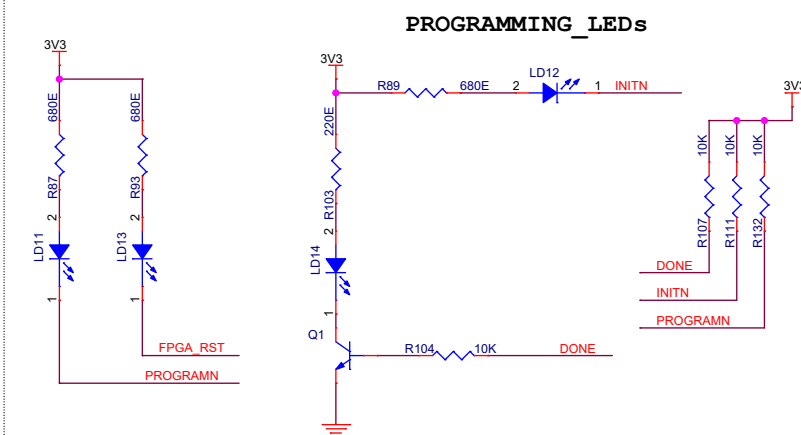
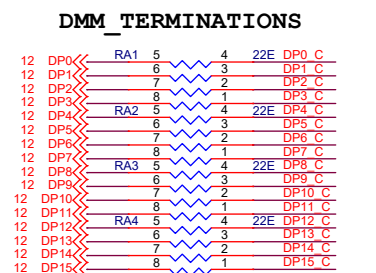
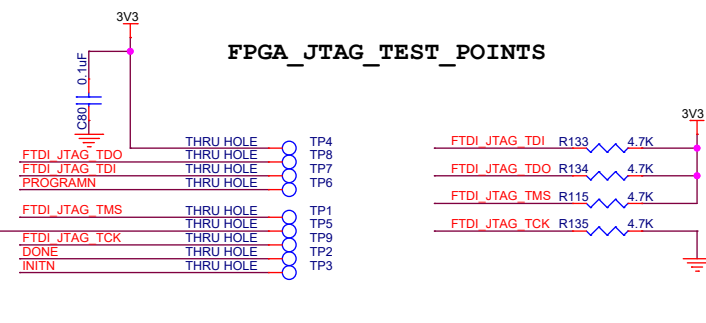
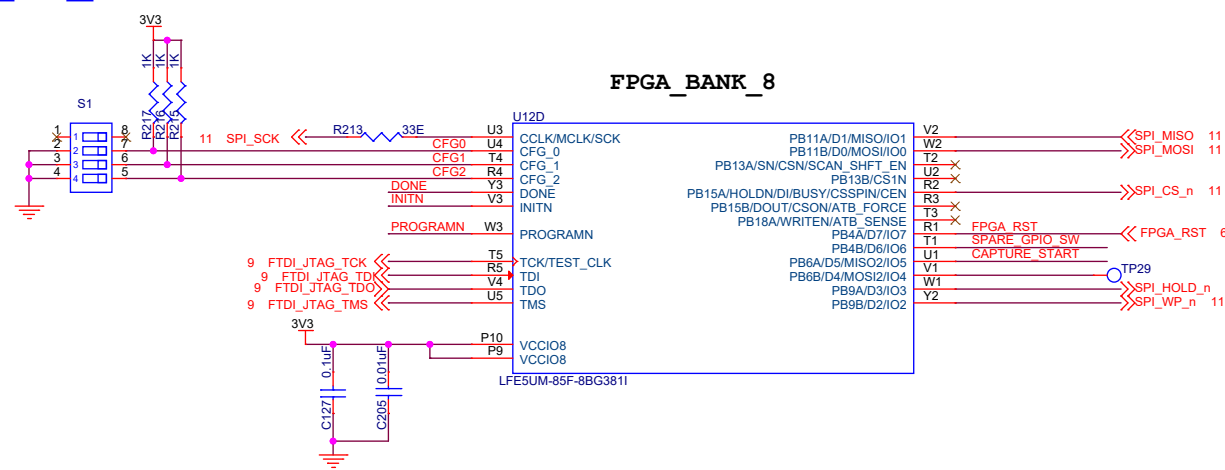
FPGA_SYS_CLK_100MHz_GENERATOR



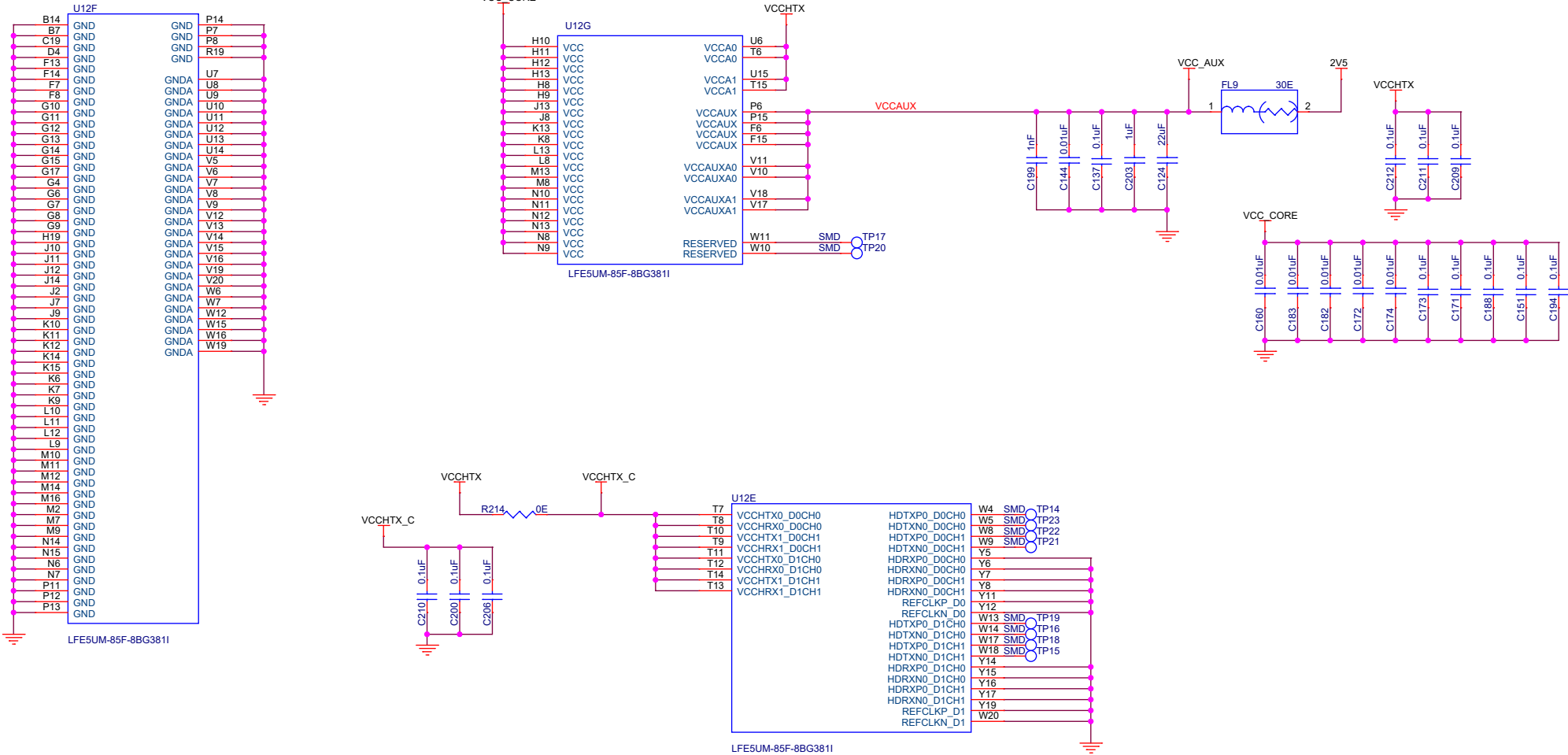
FPGA_DDR3_100MHz_CLK_GENERATOR



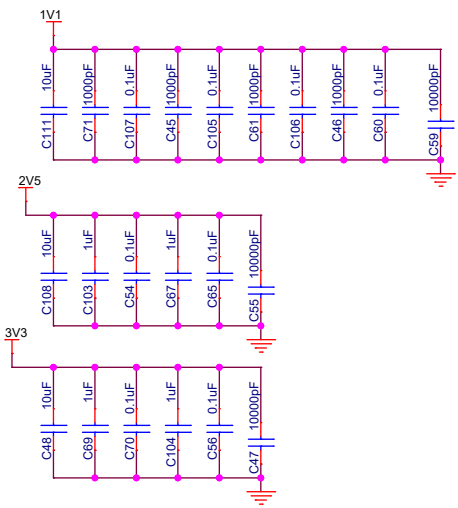
FPGA_IO_SECTION



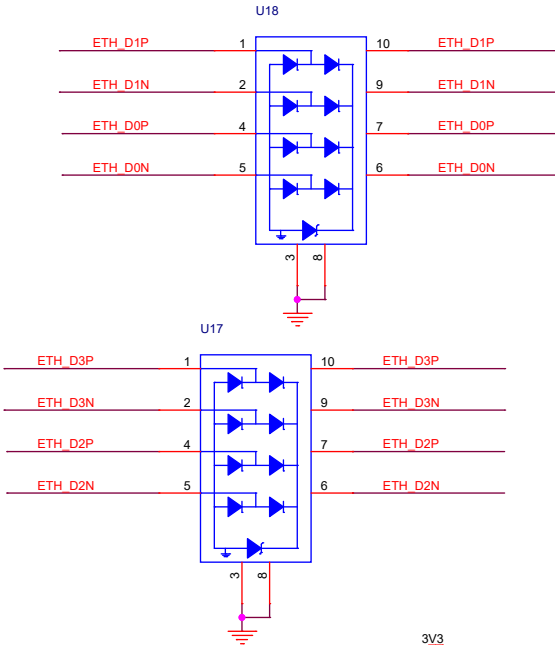
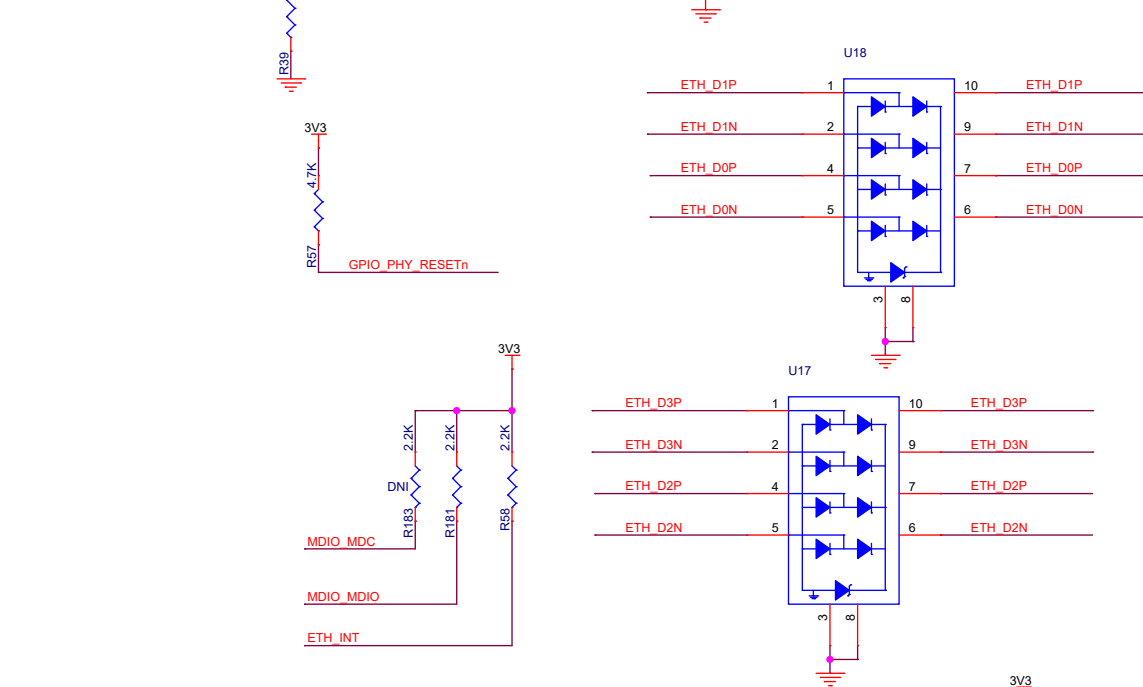
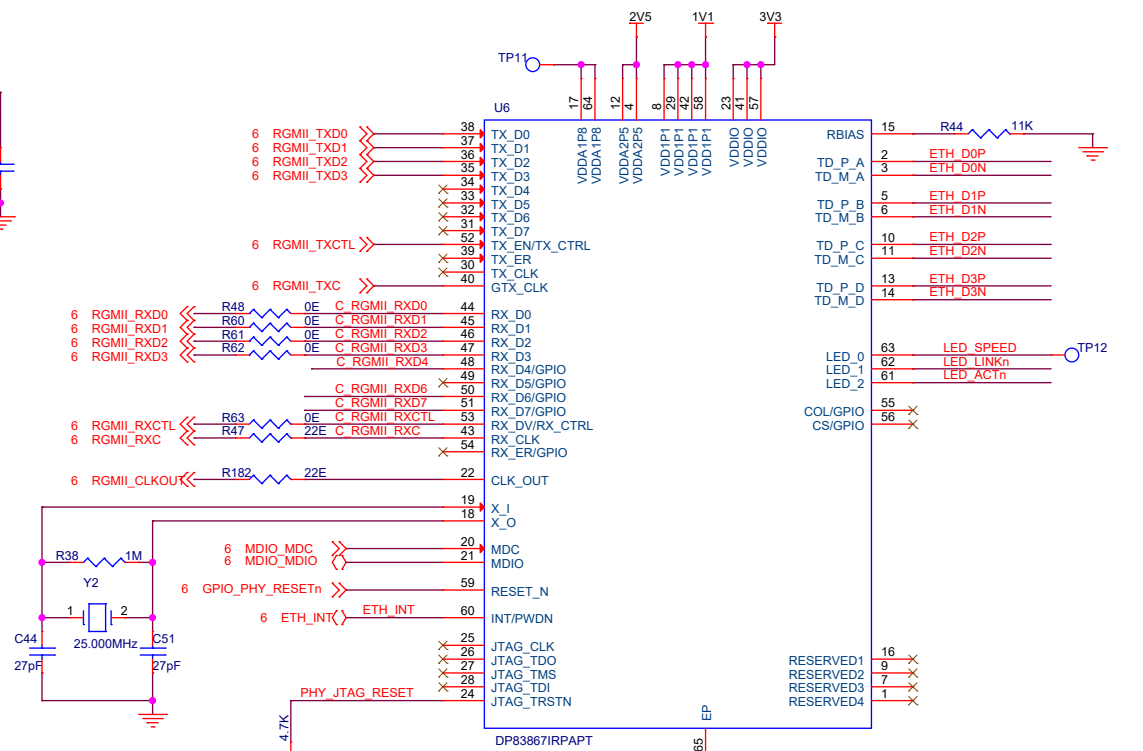
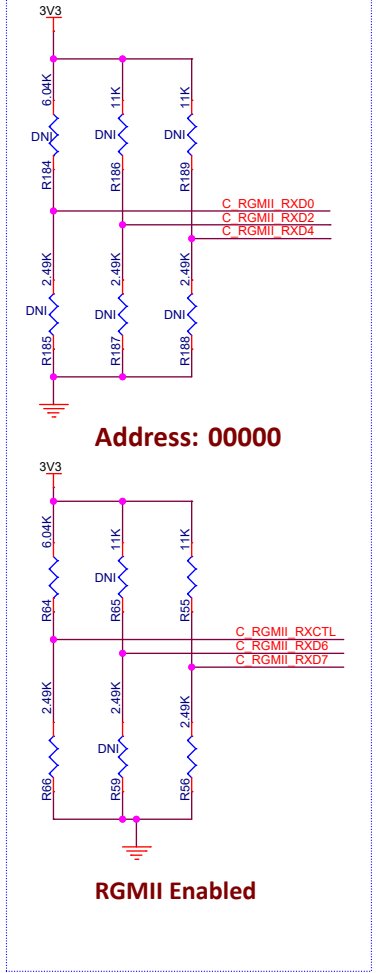
FPGA_POWER



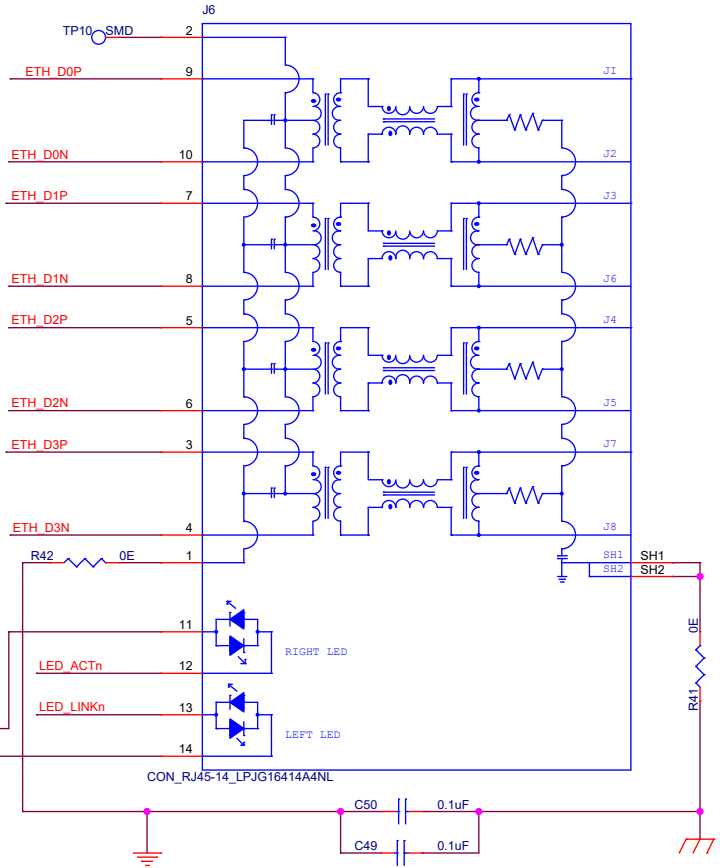
ETHERNET_PHY



STRAP_SETTINGS

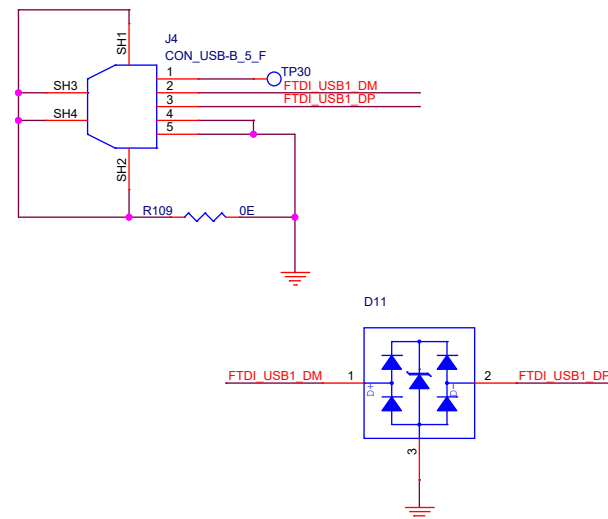


RJ45_MACJACK_CONNECTOR

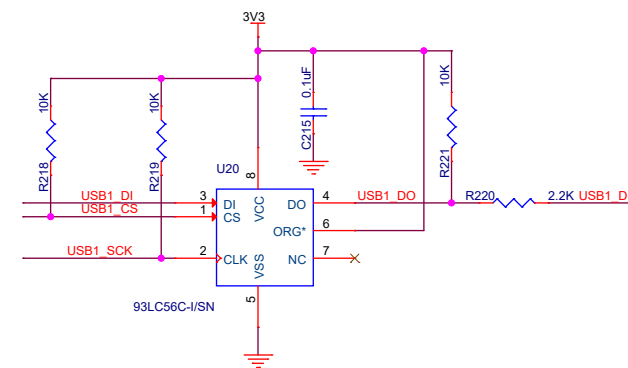


FPGA_FTDI_JTAG

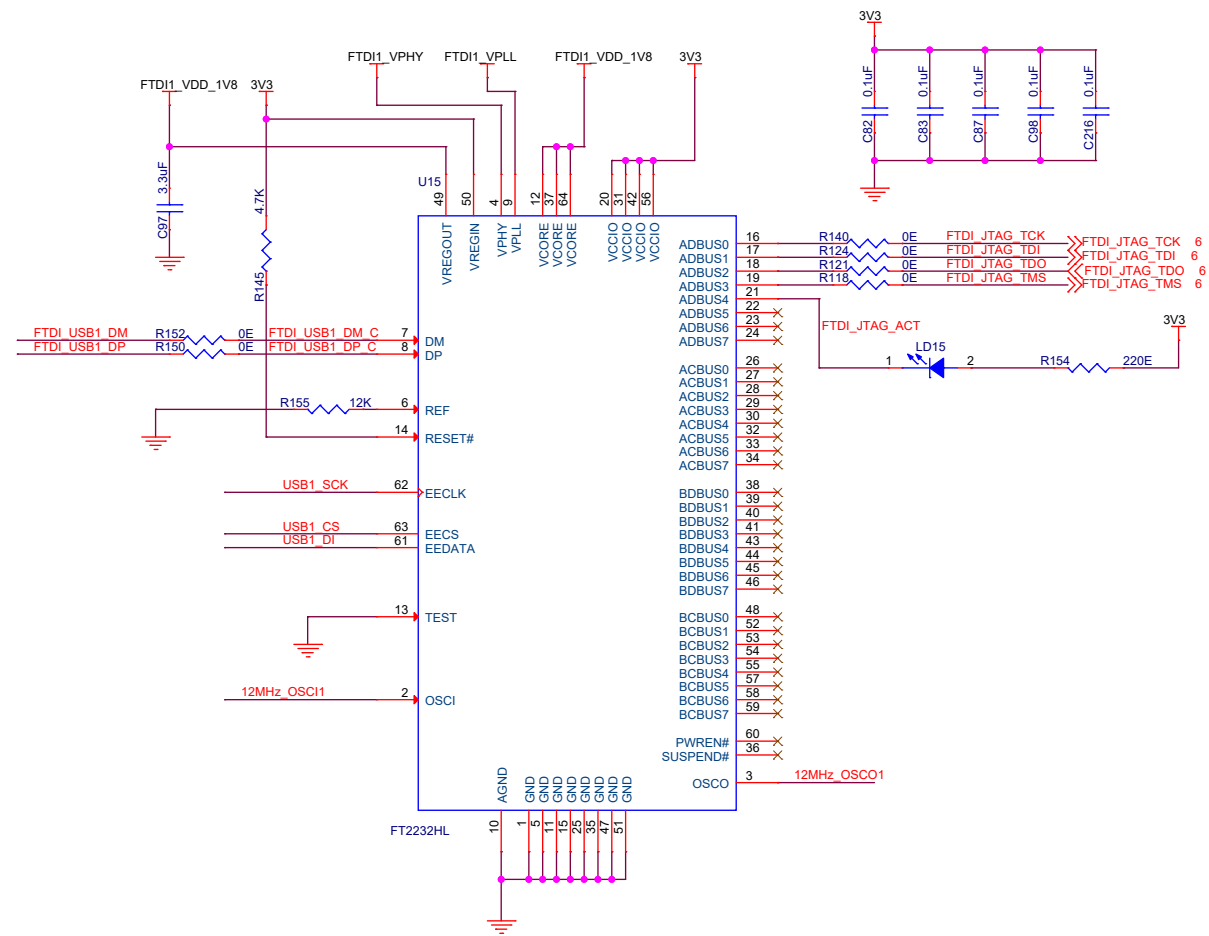
USB_CONN1_FOR_FPGA_PROGRAMMING



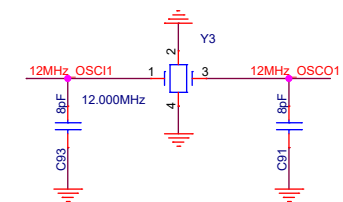
FTDI1_EEPROM



FTDI_CHIP1

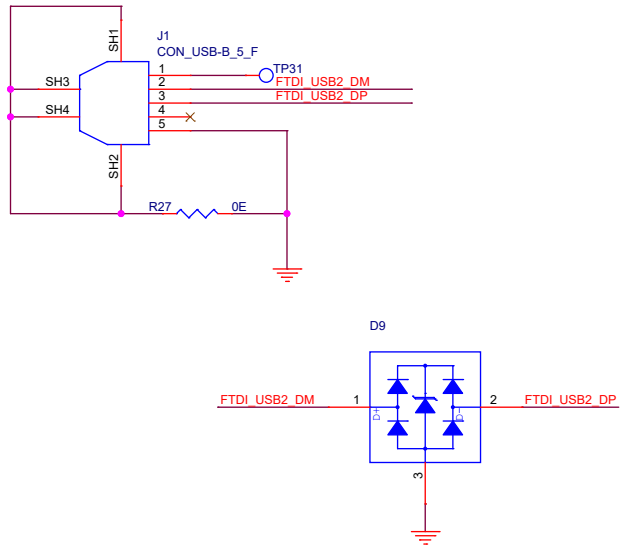


FTDI1_12MHz_CRYSTAL

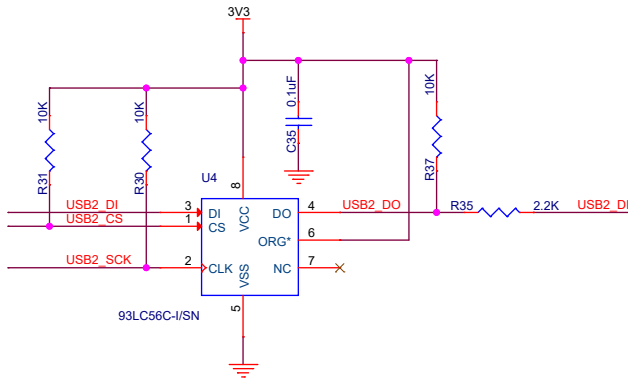


FTDI_UART_SPI_I2C

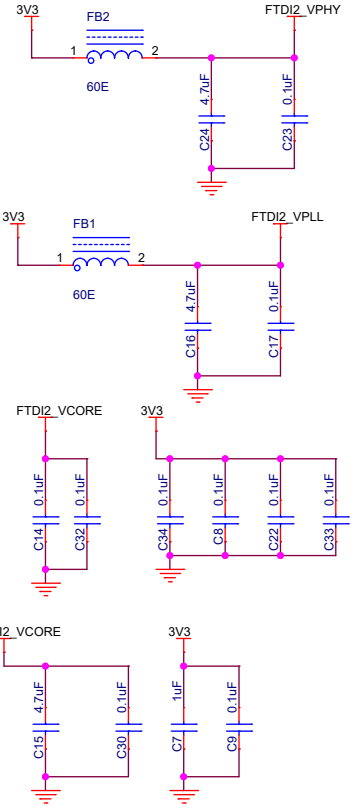
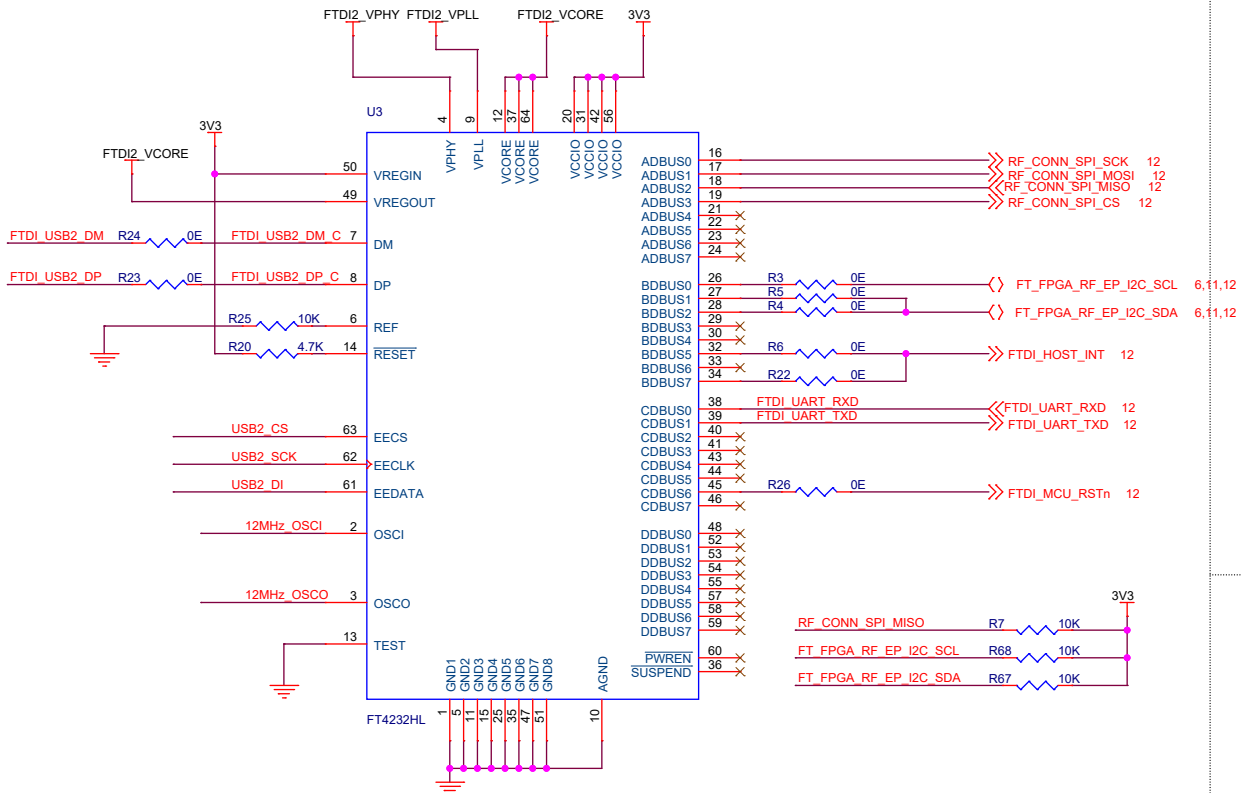
USB_CONN2_FOR_HOST



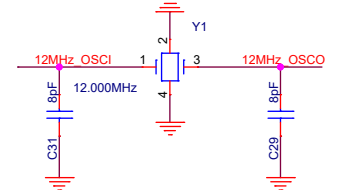
FTDI2_EEPROM



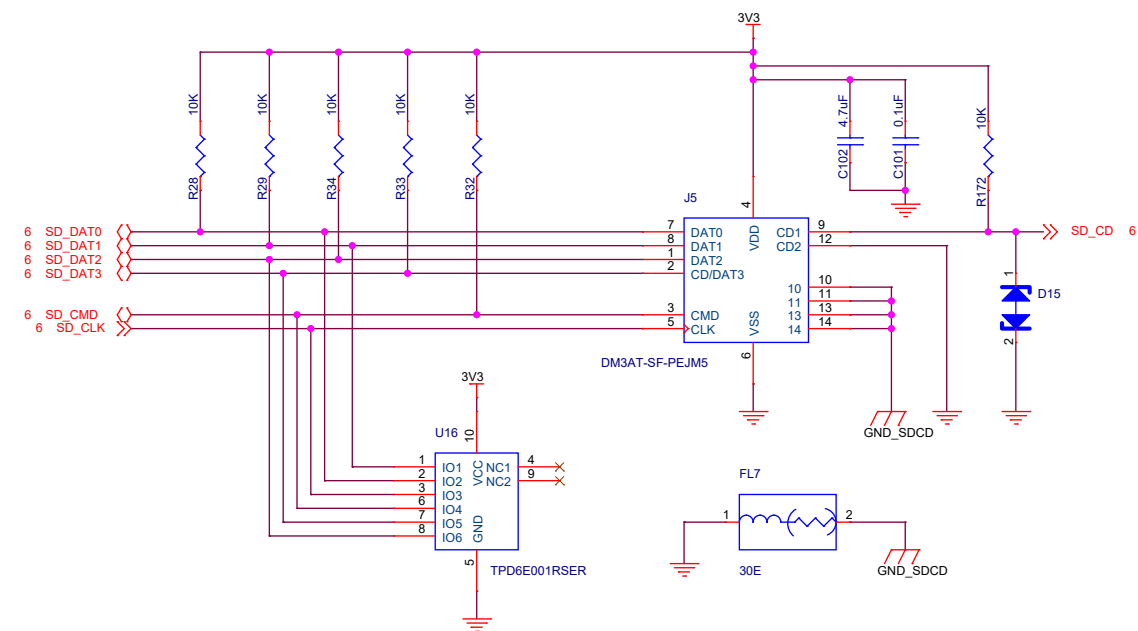
FTDI_CHIP2



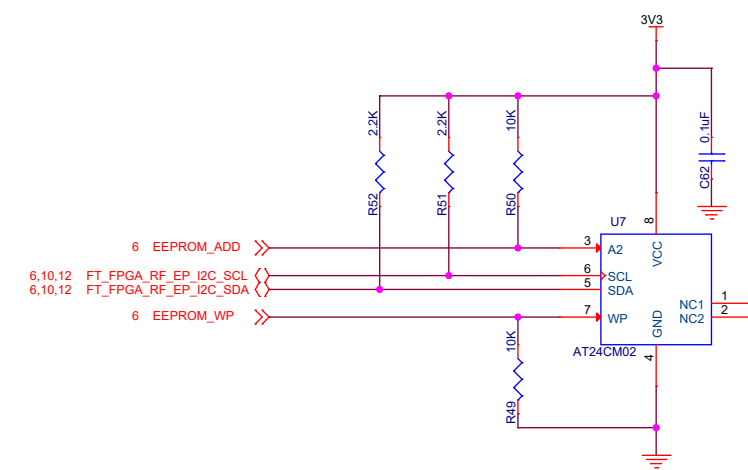
FTDI2_12MHz_CRYSTAL



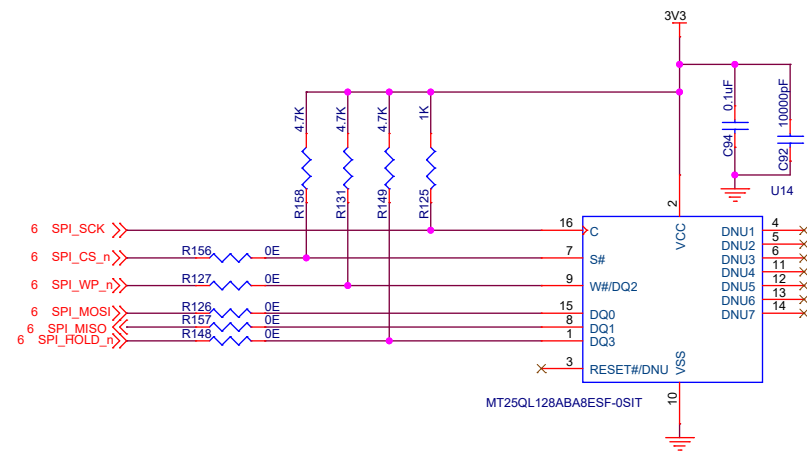
microSD_Card



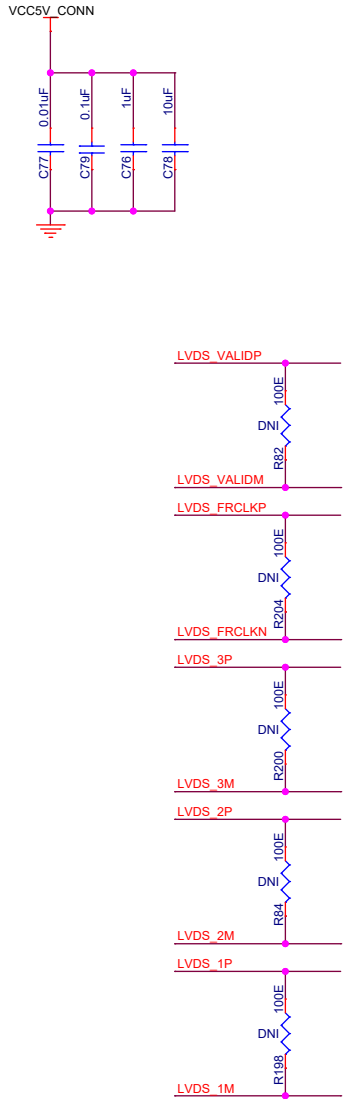
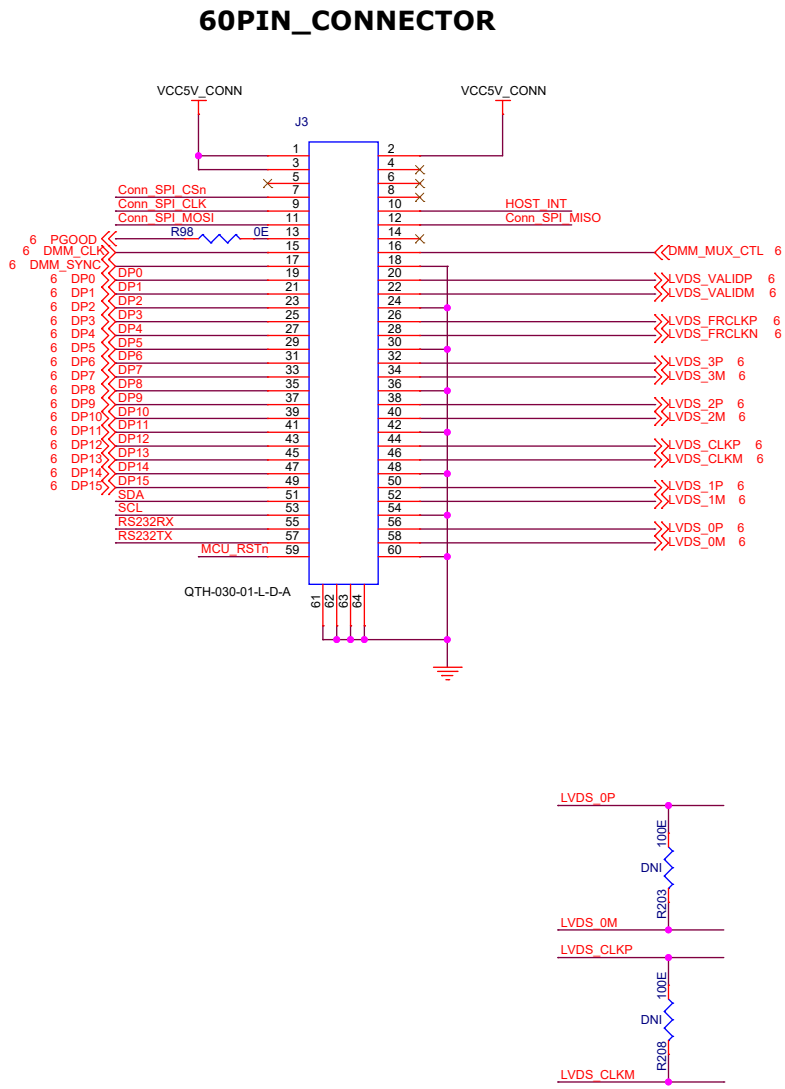
EEPROM



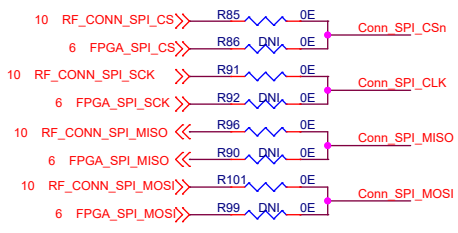
SPI_FLASH



RADAR_EVM_CONNECTOR



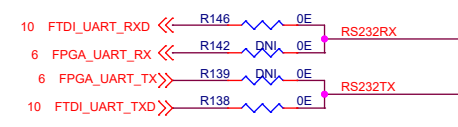
SPI_SELECTION_PATH



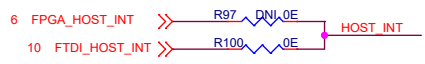
I2C_SELECTION_PATH



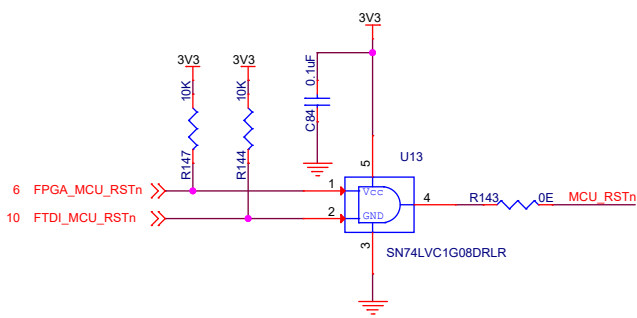
UART_SELECTION_PATH



HOST_INT_SELECTION_PATH

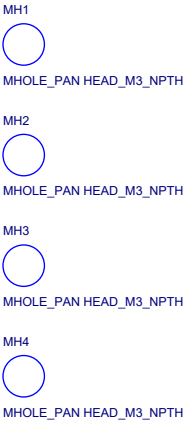


MCU_RSTn_AND_GATE

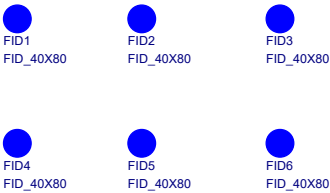


HARDWARE

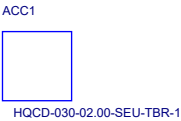
Mounting Holes



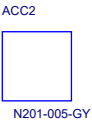
FIDUCIALS



Samtec 60 pin Cable



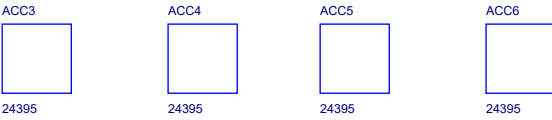
Ethernet Cable



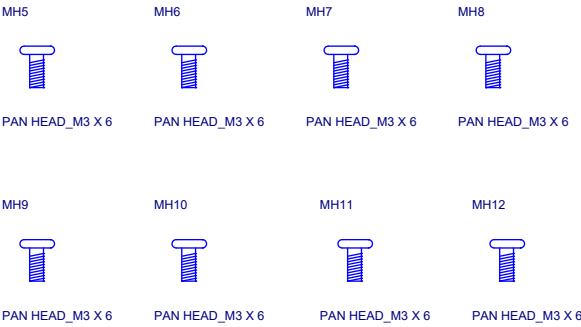
uSD CARD



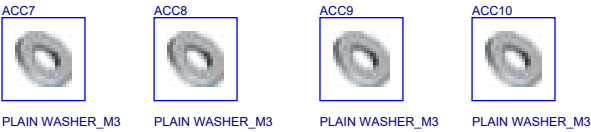
Spacers - M3 X 15MM



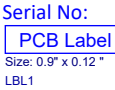
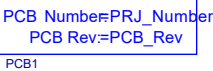
Screws - M3 X 6MM



WASHERS - M3 X 0.5MM



LOGOs & LABELS



Label Assembly Note
ZZ1
The boards and components must be baked before assembly

Label Assembly Note
ZZ2
Provide serial numbers to the assembled boards for identification

Label Assembly Note
ZZ3
Please carry out the cold points check verification and provide the report for each assembled board

Label Assembly Note
ZZ4
The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

Label Assembly Note
ZZ5
All MSL components should be baked as per JEDEC standard

Label Assembly Note
ZZ6
PCB should be baked at 120 degree for 8 hours

Label Assembly Note
ZZ7
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Label Assembly Note
ZZ8
These assemblies are ESD sensitive, ESD precautions shall be observed.

Label Assembly Note
ZZ9
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Project : DCA1000EVM	Designed for TI by Mistral Solutions Pvt Ltd  	Title HARDWARE			
		Size Document Number		Rev	
		C PROC048A_SCH		A	
		Date: Tuesday, January 23, 2018		Sheet 13 of 13	