Class Report 2: Reaction Timer Circuit

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1 Introduction

This report describes the design and implementation of a reaction timer circuit on a Nexys4 DDR FPGA board using SystemVerilog. The circuit measures human eye–hand coordination by displaying reaction times in milliseconds after a visual stimulus (an LED) is presented. The project required deriving an ASMD chart, writing HDL code, and verifying the design through simulation and hardware prototyping.

GitHub repo: `https://github.com/josietwirls/SoC/tree/main/CR2`
Oral presentation: `https://youtube.com/shorts/PibpZeL8q88?si=aLplmGuOLTR2bVH4`

2 Background

Eye–hand coordination is commonly studied by measuring reaction times to stimuli. In digital design, this can be modeled using a finite-state machine (FSM) with precise

timing control. The seven-segment LED display provides user feedback, while counters track time in milliseconds.

The problem statement (Textbook Problem 6.5.6) requires:

1. Initial "HI" welcome message with LED off.
2. A random waiting interval of 2–15 seconds before the LED stimulus.
3. A millisecond counter once the LED turns on, displayed on the seven-segment display.
4. User input to stop the counter, or automatic timeout at 1000 ms.
5. Penalty condition when the stop button is pressed early, displaying "9999."

The ASMD approach provides a structured way to implement this behavior by combining state transitions, outputs, and decision logic.

3 Problem Statement

The goal is to design a reaction timer circuit that measures and displays a user's reaction time in milliseconds. The design requires three pushbutton inputs (`clear`, `start`, `stop`), one stimulus LED, and a four-digit seven-segment display. The display cycles through welcome, blank, live timing, timeout, and penalty modes depending on user actions and state machine transitions.

4 Solution Methodology

4.1 ASMD Chart

The ASMD chart was derived to model the sequence of states:

- **IDLE:** LED off, display "HI."
- **START:** Waiting interval loaded from pseudo-random generator.
- **REACTION:** LED on, counter enabled.
- **WIN:** Display frozen reaction time.
- **LATE:** Display "1000."
- **EARLY:** Display "9999" if stop pressed early.

The ASMD chart is included in Figure 1.

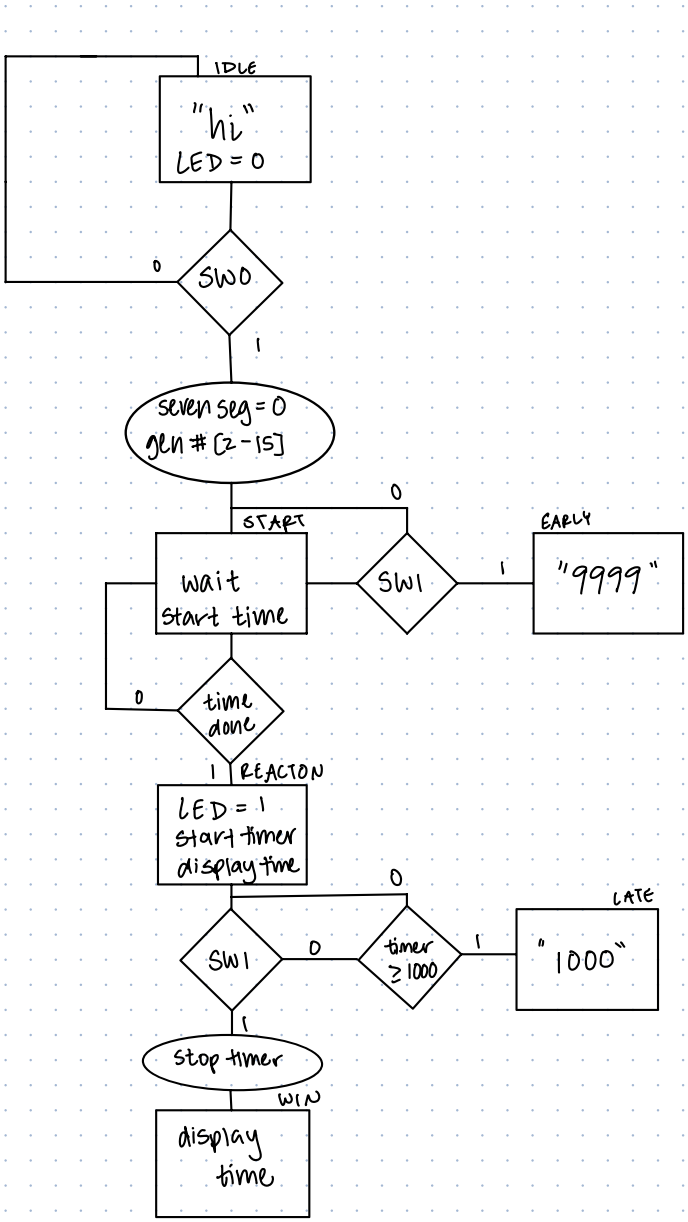

Figure 1: ASMD chart for Reaction Timer.

4.2 HDL Design

The design was implemented in SystemVerilog across multiple modules:

- `prbs.sv` — pseudo-random bit sequence generator for timing delay.
- `timer.sv` — millisecond counter with enable, clear, and timeout outputs.
- `sseg.sv` — seven-segment driver for four-digit display.

- `reaction_timer_top.sv` — top-level FSM integrating inputs, outputs, and submodules.

Testbenches (`prbs_tb.sv`, `sseg_tb.sv`) were developed to validate functionality prior to synthesis.

4.3 Synthesis and Verification

The design was synthesized in Vivado and programmed onto the Nexys4 DDR FPGA. Simulation confirmed correct state sequencing, while hardware tests verified the LED stimulus, proper display output, and accurate millisecond timing.

5 Experimental Results

Simulation waveforms demonstrated that:

- The pseudo-random generator produced varying wait times in the required range.
- The counter incremented every millisecond and halted at stop or timeout.
- The display correctly rendered "HI," live timing, and special outputs (1000 and 9999).

On the FPGA board, the circuit performed as expected. Typical reaction times measured ranged between 150–300 ms, consistent with human response. The early-stop penalty and timeout were also verified.

6 Discussion

This project illustrated how FSM design, counters, and random delay generation can be combined to implement a real-world application. The ASMD chart provided a clear blueprint for coding the HDL. Testbenches reduced debugging effort, and FPGA implementation confirmed functional correctness. Overall, the design demonstrates practical integration of control logic, randomization, and user interaction in FPGA systems.

7 Conclusion

The reaction timer circuit successfully measured user response times with accurate millisecond precision and displayed results via the seven-segment display. The combination of ASMD-based FSM design and modular SystemVerilog coding yielded a reliable implementation. This project deepened understanding of FSM design, timing control, and FPGA-based prototyping.