1.8V to 5.5V, 80μA, 8-, 10-, and 12-Bit, Low-Power, Single-Channel, DIGITAL-TO-ANALOG CONVERTERS in SC70 Package

Check for Samples: DAC5311, DAC6311, DAC7311

FEATURES

- **Relative Accuracy:**
  - **0.25 LSB INL (DAC5311: 8-bit)**
  - **0.5 LSB INL (DAC6311: 10-bit)**
  - **1 LSB INL (DAC7311: 12-bit)**
- ***micro*Power Operation: 80μA at 1.8V**
- **Power-Down: 0.5μA at 5V, 0.1μA at 1.8V**
- **Wide Power Supply: +1.8V to +5.5V**
- **Power-On Reset to Zero Scale**
- **Straight Binary Data Format**
- **Low Power Serial Interface with Schmitt-Triggered Inputs: Up to 50MHz**
- **On-Chip Output Buffer Amplifier, Rail-to-Rail Operation**
- **$\overline{\text{SYNC}}$ Interrupt Facility**
- **Extended Temperature Range –40°C to +125°C**
- **Pin-Compatible Family in a Tiny, 6-Pin SC70 Package**

APPLICATIONS

- **Portable, Battery-Powered instruments**
- **Process Control**
- **Digital Gain and Offset Adjustment**
- **Programmable Voltage and Current Sources**

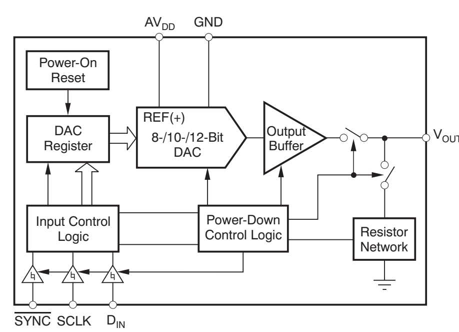
RELATED DEVICES	16-BIT	14-BIT	12-BIT	10-BIT	8-BIT
Pin and Function Compatible	DAC8411	DAC8311	DAC7311	DAC6311	DAC5311

DESCRIPTION

The DAC5311 (8-bit), DAC6311 (10-bit), and DAC7311 (12-bit) are low-power, single-channel, voltage output digital-to-analog converters (DAC). They are monotonic by design and provide excellent linearity and minimize undesired code-to-code transient voltages while offering an easy upgrade path within a pin-compatible family. All devices use a versatile, 3-wire serial interface that operates at clock rates of up to 50MHz and is compatible with standard SPI™, QSPI™, MICROWIRE™, and digital signal processor (DSP) interfaces.

All devices use an external power supply as a reference voltage to set the output range. The devices incorporate a power-on reset (POR) circuit that ensures the DAC output powers up at 0V and remains there until a valid write to the device occurs. The DAC5311, DAC6311, and DAC7311 contain a power-down feature, accessed over the serial interface, that reduces current consumption of the device to 0.1μA at 1.8V in power down mode. The low power consumption of this part in normal operation makes it ideally suited for portable, battery-operated equipment. The power consumption is 0.55mW at 5V, reducing to 2.5μW in power-down mode.

These devices are pin-compatible with the DAC8311 and DAC8411, offering an easy upgrade path from 8-, 10-, and 12-bit resolution to 14- and 16-bit. All devices are available in a small, 6-pin, SC70 package. This package offers a flexible, pin-compatible, and functionally-compatible drop-in solution within the family over an extended temperature range of –40°C to +125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI, QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corporation.
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC5311	±0.25	±0.25	SC70-6	DCK	–40°C to 125°C	D53
DAC6311	±0.5	±0.5	SC70-6	DCK	–40°C to 125°C	D63
DAC7311	±1	±1	SC70-6	DCK	–40°C to 125°C	D73

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	VALUE	UNIT
AV_{DD} to GND	–0.3 to +6	V
Digital input voltage to GND	–0.3 to $+AV_{DD}$ +0.3	V
AV_{OUT} to GND	–0.3 to $+AV_{DD}$ +0.3	V
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature (T_J max)	+150	°C
Power dissipation	$(T_J \text{ max} – T_A)/\theta_{JA}$	W
θ_{JA} thermal impedance	250	°C/W

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At AV_{DD} = +1.8V to +5.5V, R_L = 2kΩ to GND, and C_L = 200 pF to GND, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DAC5311, DAC6311, DAC7311 MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
DAC5311	Resolution		8			Bits
	Relative accuracy	Measured by the line passing through codes 3 and 252		±0.01	±0.25	LSB
	Differential nonlinearity			±0.01	±0.25	LSB
DAC6311	Resolution		10			Bits
	Relative accuracy	Measured by the line passing through codes 12 and 1012		±0.06	±0.5	LSB
	Differential nonlinearity			±0.03	±0.5	LSB
DAC7311	Resolution		12			Bits
	Relative accuracy	Measured by the line passing through codes 30 and 4050		±0.3	±1	LSB
	Differential nonlinearity			±0.2	±1	LSB
Offset error		Measured by the line passing through two codes(2)		±0.05	±4	mV
Offset error drift				3		μV/°C
Zero code error		All zeros loaded to the DAC register		0.2		mV
Full-scale error		All ones loaded to DAC register		0.04	0.2	% of FSR
Gain error				0.05	±0.15	% of FSR
Gain temperature coefficient		AV_{DD} = +5V		±0.5		ppm of FSR/°C
		AV_{DD} = +1.8V		±1.5		
OUTPUT CHARACTERISTICS(3)						
Output voltage range			0		AV_{DD}	V
Output voltage settling time		R_L = 2kΩ, C_L = 200 pF, AV_{DD} = 5V, 1/4 scale to 3/4 scale		6	10	μs
		R_L = 2MΩ, C_L = 470pF		12		μs
Slew rate				0.7		V/μs
Capacitive load stability		R_L = ∞		470		pF
		R_L = 2kΩ		1000		pF
Code change glitch impulse		1LSB change around major carry		0.5		nV-s
Digital feedthrough				0.5		nV-s
Power-on glitch impulse		R_L = 2kΩ, C_L = 200pF, AV_{DD} = 5V		17		mV
DC output impedance				0.5		Ω
Short-circuit current		AV_{DD} = +5V		50		mA
		AV_{DD} = +3V		20		mA
Power-up time		Coming out of power-down mode		50		μs
AC PERFORMANCE						
SNR		T_A= +25°C, BW = 20kHz, 12-bit level, AV_{DD} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		81		dB
THD				–65		dB
SFDR				65		dB
SINAD				65		dB
DAC output noise density(4)		T_A= +25°C, at zero-scale input, f_{OUT} = 1kHz, AV_{DD} = 5V		17		nV/√Hz
		T_A= +25°C, at mid-code input, f_{OUT} = 1kHz, AV_{DD} = 5V		110		nV/√Hz
DAC output noise(5)		T_A= +25°C, at mid-code input, 0.1Hz to 10Hz, AV_{DD} = 5V		3		$μV_{PP}$

(1) Linearity calculated using a reduced code range of 3 to 252 for 8-bit, 12 to 1012 for 10bit, and 30 to 4050 for 12-bit, output unloaded.
(2) Straight line passing through codes 3 and 252 for 8-bit, 12 and 1012 for 10bit, and 30 and 4050 for 12-bit, output unloaded.
(3) Specified by design and characterization, not production tested.
(4) For more details, see Figure 22.
(5) For more details, see Figure 23.

ELECTRICAL CHARACTERISTICS (continued)

At AV_{DD} = +1.8V to +5.5V, R_L = 2kΩ to GND, and C_L = 200 pF to GND, unless otherwise noted.

PARAMETER		TEST CONDITIONS		DAC5311, DAC6311, DAC7311 MIN	TYP	MAX	UNIT
LOGIC INPUTS(6)							
Input current						±1	µA
$V_{IN}L$, input low voltage		AV_{DD} = 2.7V to 5.5V				$0.3AV_{DD}$	V
		AV_{DD} = 1.8V to 2.7V				$0.1AV_{DD}$	V
$V_{IN}H$, input high voltage		AV_{DD} = 2.7V to 5.5V		$0.7AV_{DD}$			V
		AV_{DD} = 1.8V to 2.7V		$0.9AV_{DD}$			V
Pin capacitance					1.5	3	pF
POWER REQUIREMENTS							
AV_{DD}				1.8		5.5	V
I_{DD}	Normal mode	$V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND, at midscale code(7)	AV_{DD} = 3.6V to 5.5V		110	160	µA
			AV_{DD} = 2.7V to 3.6V		95	150	
			AV_{DD} = 1.8V to 2.7V		80	140	
	All power-down mode	$V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND, at midscale code	AV_{DD} = 3.6V to 5.5V		0.5	3.5	µA
			AV_{DD} = 2.7V to 3.6V		0.4	3.0	
			AV_{DD} = 1.8V to 2.7V		0.1	2.0	
Power dissipation	Normal mode	$V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND, at midscale code	AV_{DD} = 3.6V to 5.5V		0.55	0.88	mW
			AV_{DD} = 2.7V to 3.6V		0.25	0.54	
			AV_{DD} = 1.8V to 2.7V		0.14	0.38	
	All power-down mode	$V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND, at midscale code	AV_{DD} = 3.6V to 5.5V		2.50	19.2	µW
			AV_{DD} = 2.7V to 3.6V		1.08	10.8	
			AV_{DD} = 1.8V to 2.7V		0.72	8.1	
TEMPERATURE RANGE							
Specified performance range				–40		+125	°C

(6) Specified by design and characterization, not production tested.
(7) For more details, see Figure 15, Figure 58, and Figure 91.

PIN CONFIGURATION

DCK PACKAGE
SC70-6
(TOP VIEW)

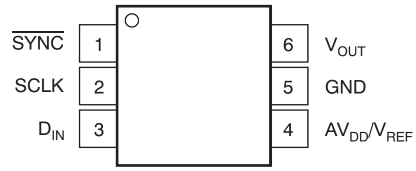
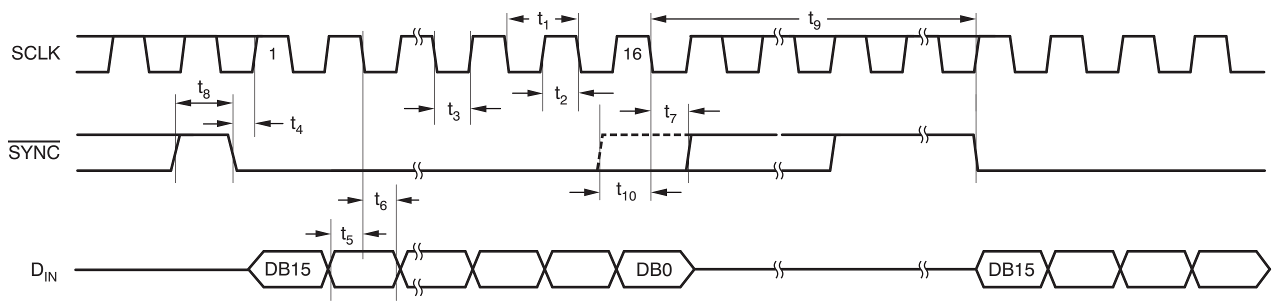


Table 1. PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	$\overline{\text{SYNC}}$	Level-triggered control input (active low). This is the frame sychronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register and data are transferred in on the falling edges of the following clocks. The DAC is updated following 16th clock cycle, unless $\overline{\text{SYNC}}$ is taken high before this edge, in which case the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the DACx311. Refer to the *$\overline{\text{SYNC}}$ Interrupt* section for more details.
2	SCLK	Serial Clock Input. Data can be transferred at rates up to 50MHz.
3	D_{IN}	Serial Data Input. Data is clocked into the 16-bit input shift register on the falling edge of the serial clock input.
4	AV_{DD}/V_{REF}	Power Supply Input, +1.8V to 5.5V.
5	GND	Ground reference point for all circuitry on the part.
6	V_{OUT}	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.

SERIAL WRITE OPERATION



TIMING REQUIREMENTS(1)

All specifications at –40°C to +125°C, and AV_{DD} = +1.8V to +5.5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1 (2)	SCLK cycle time	AV_{DD} = 1.8V to 3.6V	50			ns
		AV_{DD} = 3.6V to 5.5V	20			
t_2	SCLK high time	AV_{DD} = 1.8V to 3.6V	25			ns
		AV_{DD} = 3.6V to 5.5V	10			
t_3	SCLK low time	AV_{DD} = 1.8V to 3.6V	25			ns
		AV_{DD} = 3.6V to 5.5V	10			
t_4	$\overline{\text{SYNC}}$ to SCLK rising edge setup time	AV_{DD} = 1.8V to 3.6V	0			ns
		AV_{DD} = 3.6V to 5.5V	0			
t_5	Data setup time	AV_{DD} = 1.8V to 3.6V	5			ns
		AV_{DD} = 3.6V to 5.5V	5			
t_6	Data hold time	AV_{DD} = 1.8V to 3.6V	4.5			ns
		AV_{DD} = 3.6V to 5.5V	4.5			
t_7	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	AV_{DD} = 1.8V to 3.6V	0			ns
		AV_{DD} = 3.6V to 5.5V	0			
t_8	Minimum $\overline{\text{SYNC}}$ high time	AV_{DD} = 1.8V to 3.6V	50			ns
		AV_{DD} = 3.6V to 5.5V	20			
t_9	16th SCLK falling edge to $\overline{\text{SYNC}}$ falling edge	AV_{DD} = 1.8V to 3.6V	100			ns
		AV_{DD} = 3.6V to 5.5V	100			
t_{10}	$\overline{\text{SYNC}}$ rising edge to 16th SCLK falling edge (for successful $\overline{\text{SYNC}}$ interrupt)	AV_{DD} = 1.8V to 3.6V	15			ns
		AV_{DD} = 3.6V to 5.5V	15			

(1) All input signals are specified with $t_R = t_F$ = 3ns (10% to 90% of AV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) Maximum SCLK frequency is 50MHz at AV_{DD} = 3.6V to 5.5V and 20MHz at AV_{DD} = 1.8V to 3.6V.

TYPICAL CHARACTERISTICS: AV_{DD} = +5V

At T_A = +25°C, AV_{DD} = +5V, and DAC loaded with midscale code, unless otherwise noted.

DAC7311 12-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (–40°C)

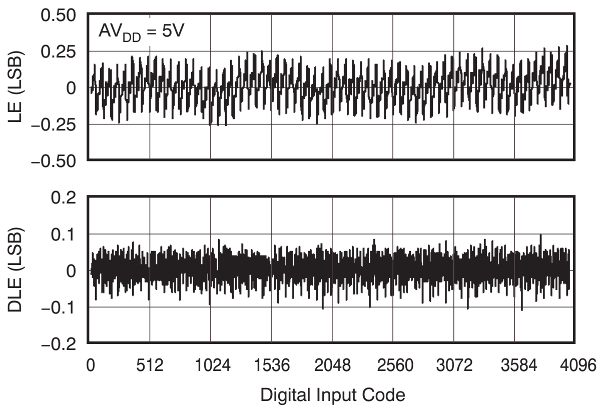


Figure 1.

DAC6311 10-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (–40°C)

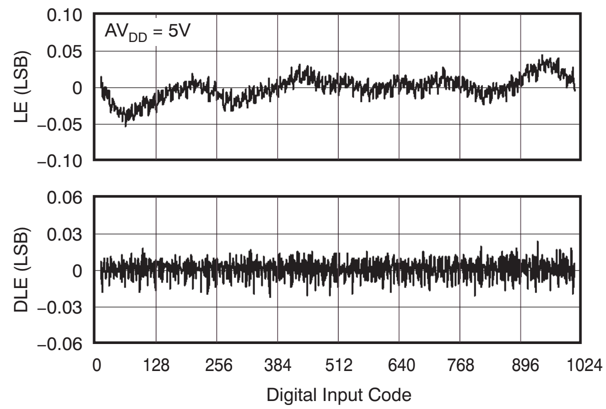


Figure 2.

DAC7311 12-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+25°C)

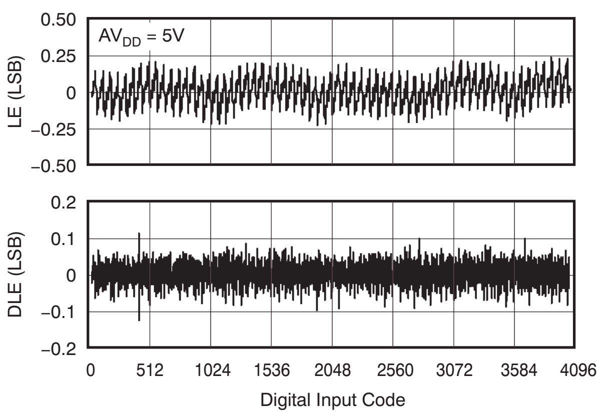


Figure 3.

DAC6311 10-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+25°C)

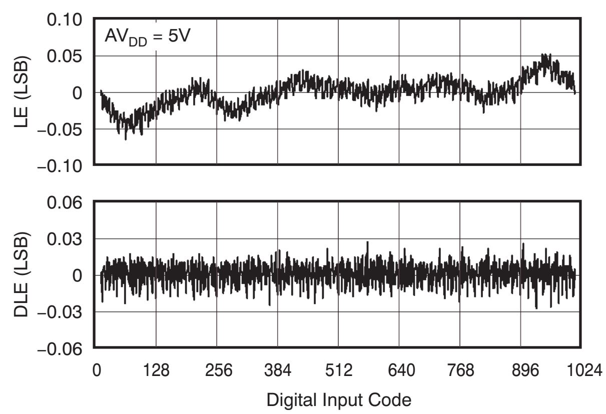


Figure 4.

DAC7311 12-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+125°C)

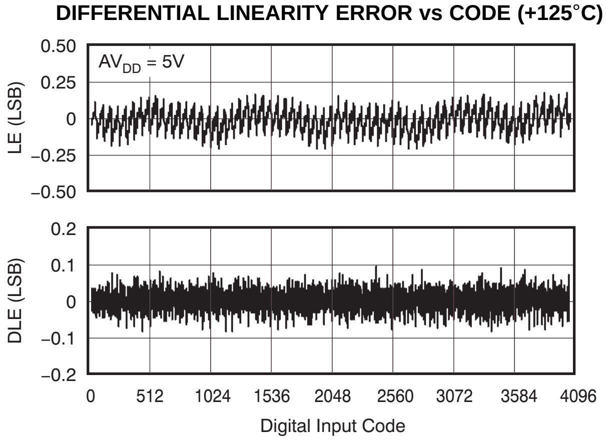


Figure 5.

DAC6311 10-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+125°C)

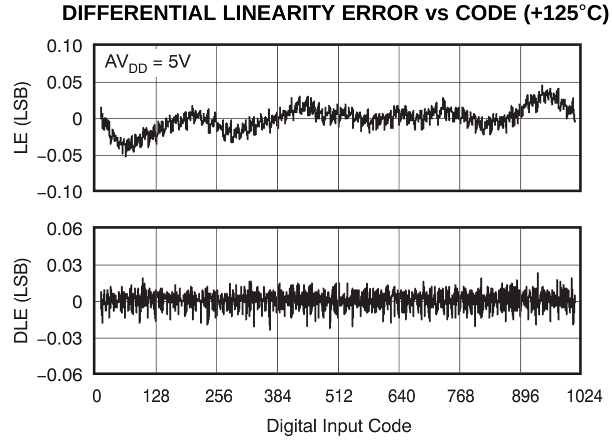


Figure 6.

TYPICAL CHARACTERISTICS: AV_{DD} = +5V (continued)

At T_A = +25°C, AV_{DD} = +5V, and DAC loaded with midscale code, unless otherwise noted.

DAC5311 8-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (–40°C)

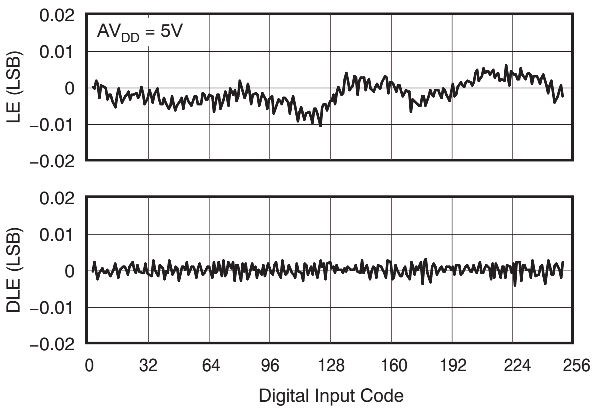


Figure 7.

ZERO-CODE ERROR vs TEMPERATURE

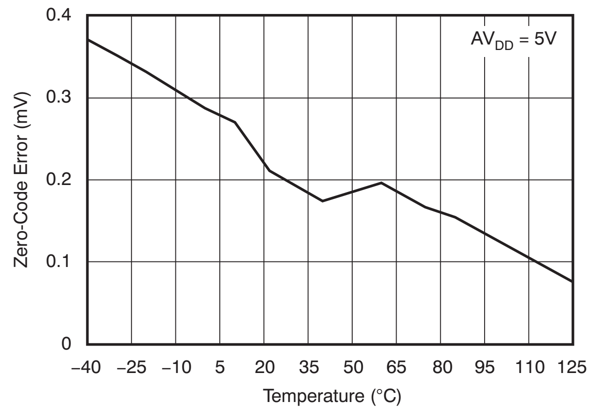


Figure 8.

DAC5311 8-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+25°C)

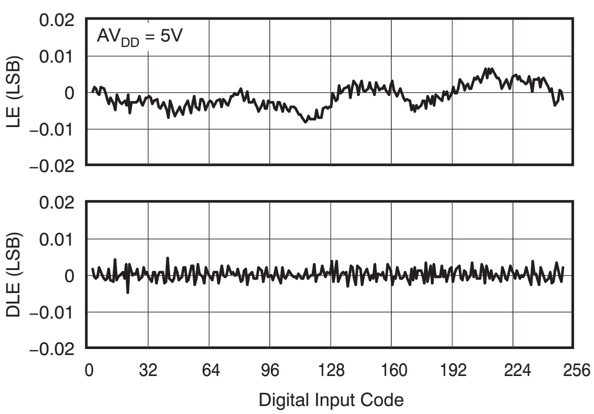


Figure 9.

OFFSET ERROR vs TEMPERATURE

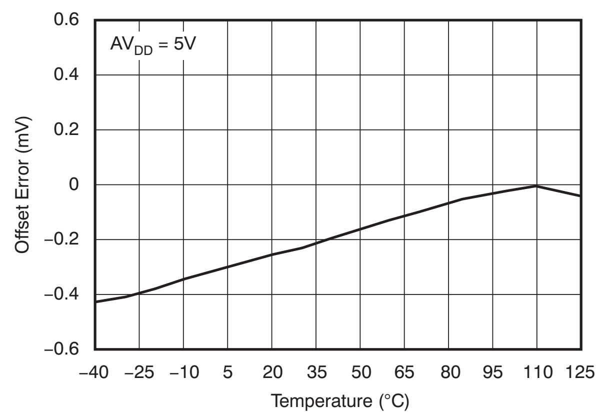


Figure 10.

DAC5311 8-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+125°C)

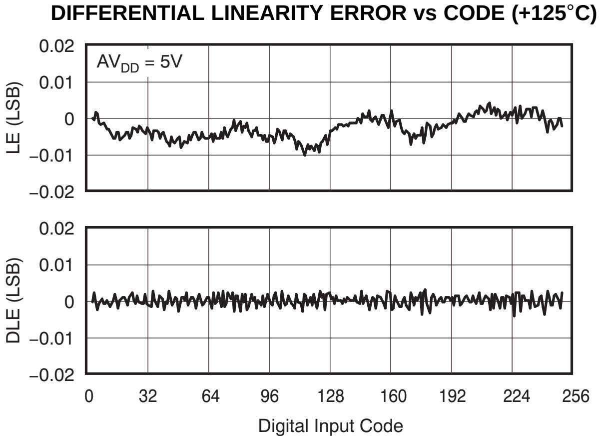


Figure 11.

FULL-SCALE ERROR vs TEMPERATURE

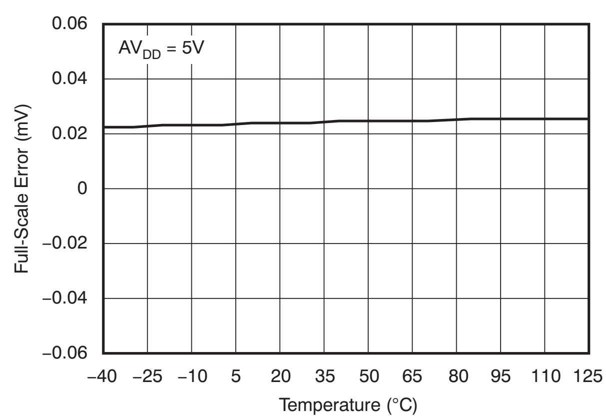


Figure 12.

TYPICAL CHARACTERISTICS: AV_{DD} = +5V (continued)

At T_A = +25°C, AV_{DD} = +5V, and DAC loaded with midscale code, unless otherwise noted.

SOURCE CURRENT AT POSITIVE RAIL

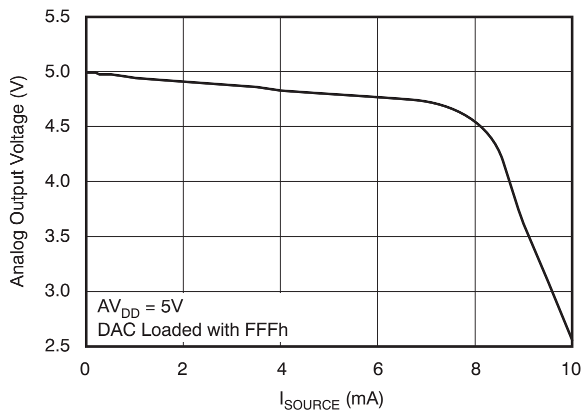


Figure 13.

SINK CURRENT AT NEGATIVE RAIL

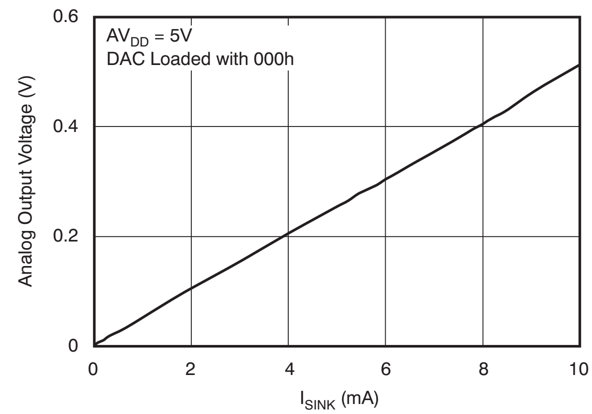


Figure 14.

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

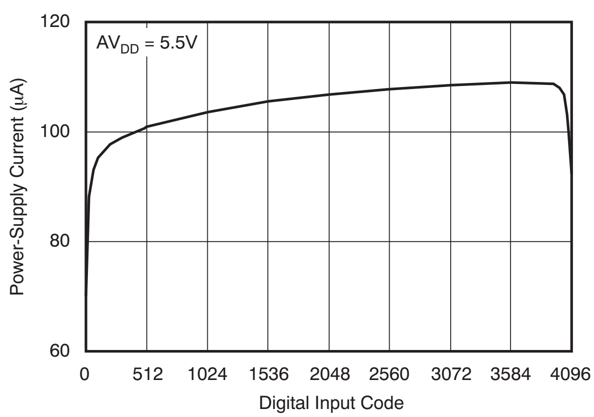


Figure 15.

POWER-SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

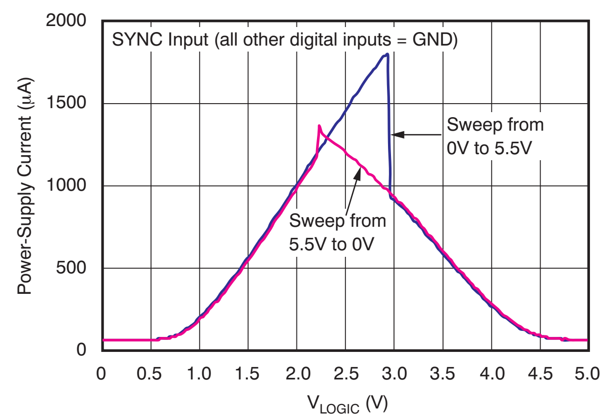


Figure 16.

POWER-SUPPLY CURRENT vs TEMPERATURE

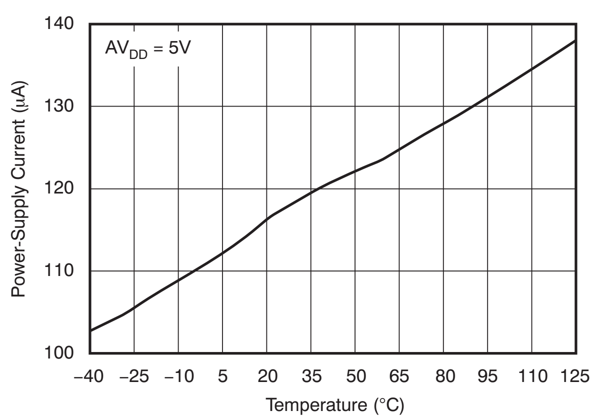


Figure 17.

POWER-DOWN CURRENT vs TEMPERATURE

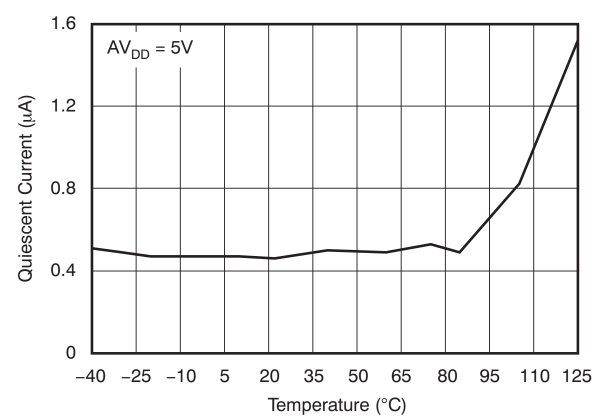


Figure 18.

TYPICAL CHARACTERISTICS: AV_{DD} = +5V (continued)

At T_A = +25°C, AV_{DD} = +5V, and DAC loaded with midscale code, unless otherwise noted.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

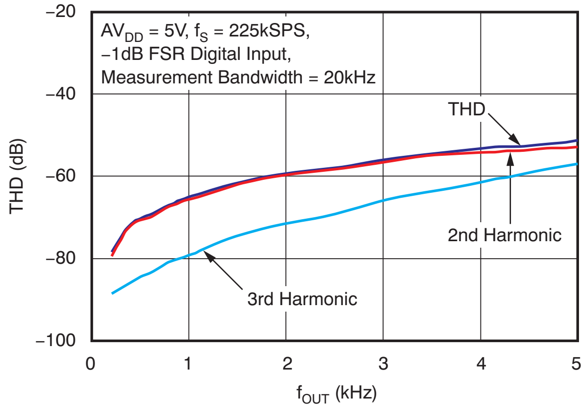


Figure 19.

SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY

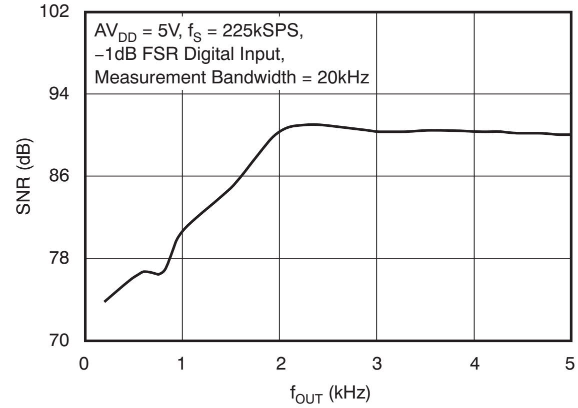


Figure 20.

POWER SPECTRAL DENSITY

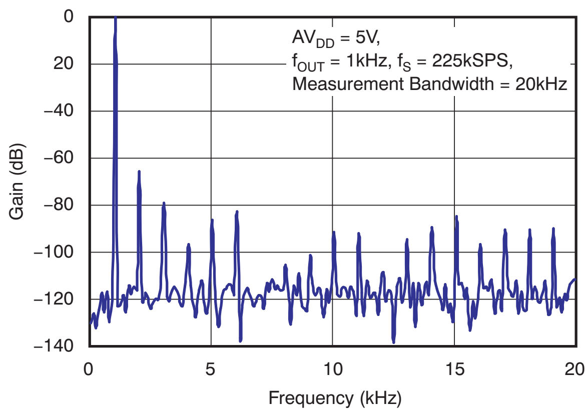


Figure 21.

DAC OUTPUT NOISE DENSITY vs FREQUENCY

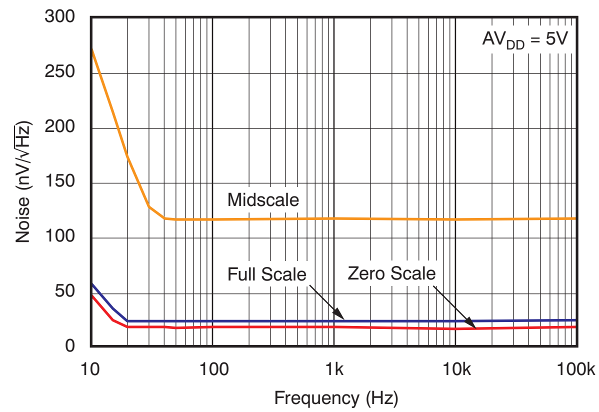
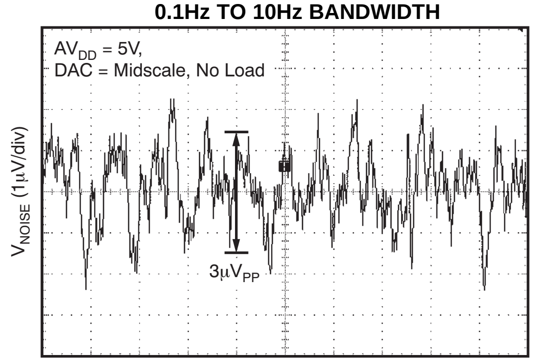


Figure 22.

DAC OUTPUT NOISE 0.1Hz TO 10Hz BANDWIDTH



Time (2s/div)

Figure 23.

TYPICAL CHARACTERISTICS: AV_{DD} = +5V (continued)

At T_A = +25°C, AV_{DD} = +5V, and DAC loaded with midscale code, unless otherwise noted.

CLOCK FEEDTHROUGH
5V, 2MHz, MIDSCALE

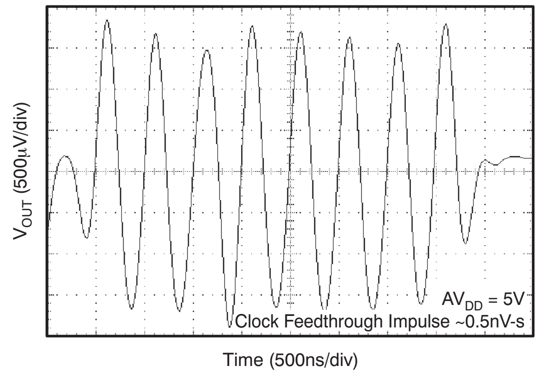


Figure 24.

GLITCH ENERGY
5V, 12-BIT, 1LSB STEP, RISING EDGE

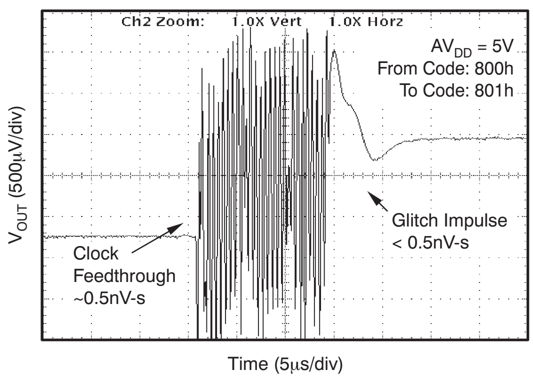


Figure 25.

GLITCH ENERGY
5V, 12-BIT, 1LSB STEP, FALLING EDGE

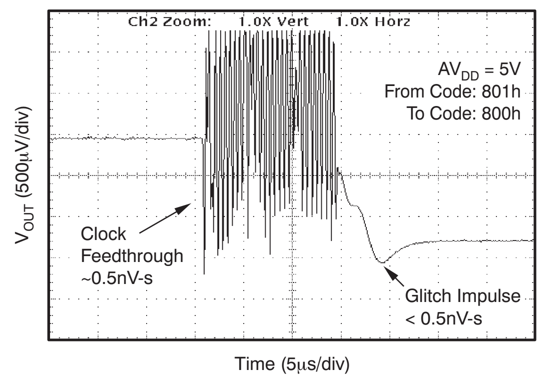


Figure 26.

GLITCH ENERGY
5V, 8-BIT, 1LSB STEP, RISING EDGE

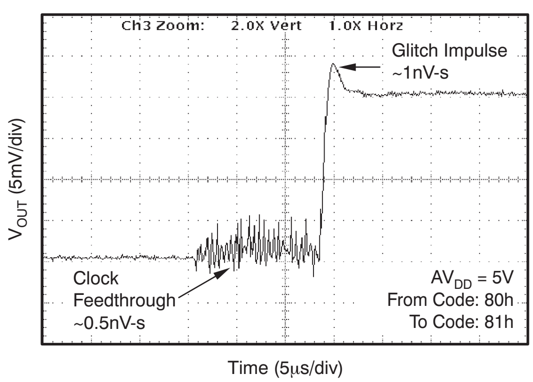


Figure 27.

GLITCH ENERGY
5V, 8-BIT, 1LSB STEP, FALLING EDGE

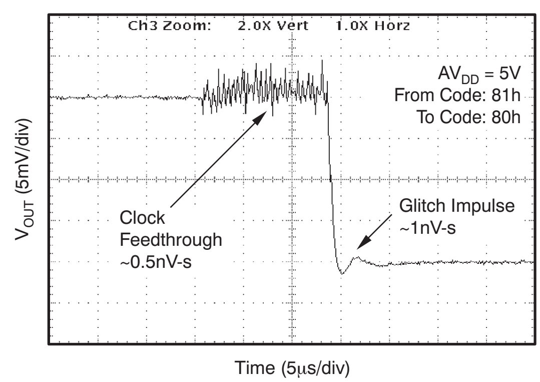


Figure 28.

TYPICAL CHARACTERISTICS: AV_{DD} = +5V (continued)

At T_A = +25°C, AV_{DD} = +5V, and DAC loaded with midscale code, unless otherwise noted.

FULL-SCALE SETTLING TIME 5V RISING EDGE

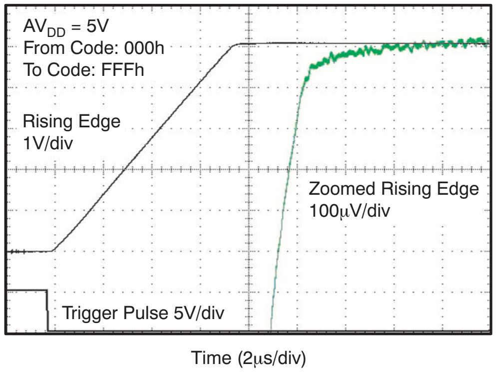


Figure 29.

FULL-SCALE SETTLING TIME 5V FALLING EDGE

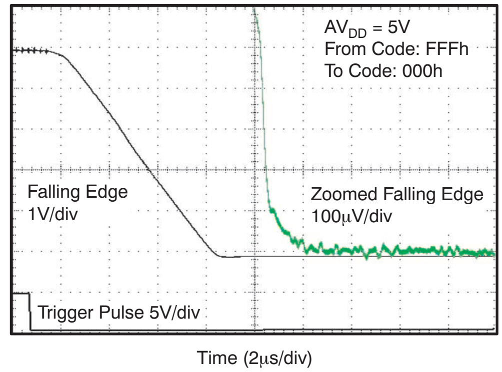


Figure 30.

HALF-SCALE SETTLING TIME 5V RISING EDGE

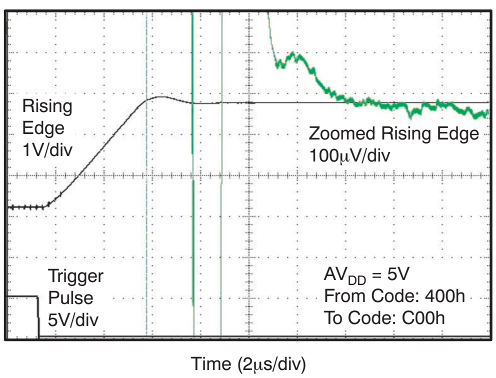


Figure 31.

HALF-SCALE SETTLING TIME 5V FALLING EDGE

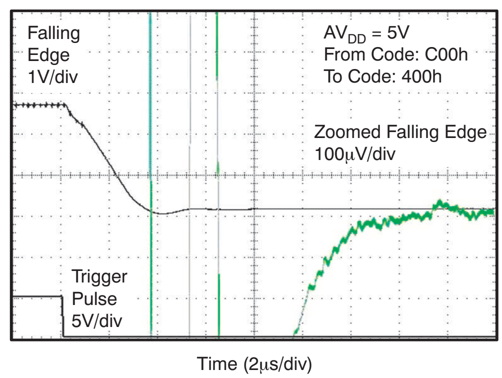


Figure 32.

POWER-ON RESET TO 0V POWER-ON GLITCH

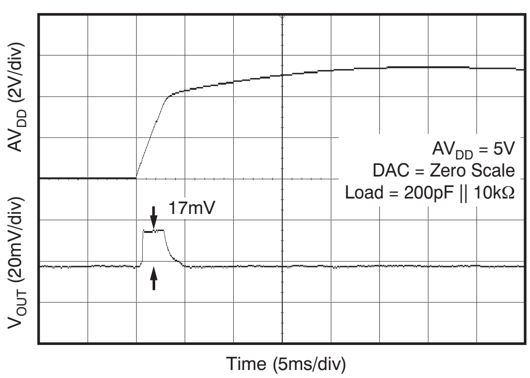


Figure 33.

POWER-OFF GLITCH

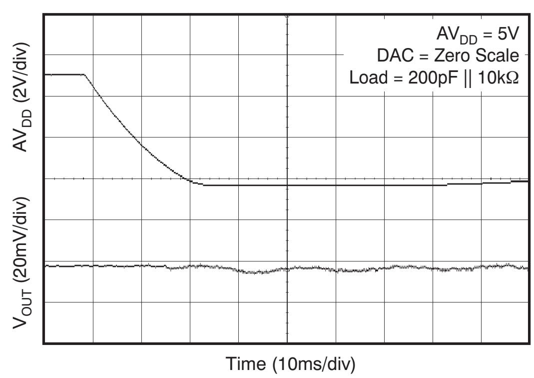


Figure 34.

TYPICAL CHARACTERISTICS: AV_{DD} = +5V (continued)

At T_A = +25°C, AV_{DD} = +5V, and DAC loaded with midscale code, unless otherwise noted.

POWER-SUPPLY CURRENT vs POWER-SUPPLY VOLTAGE

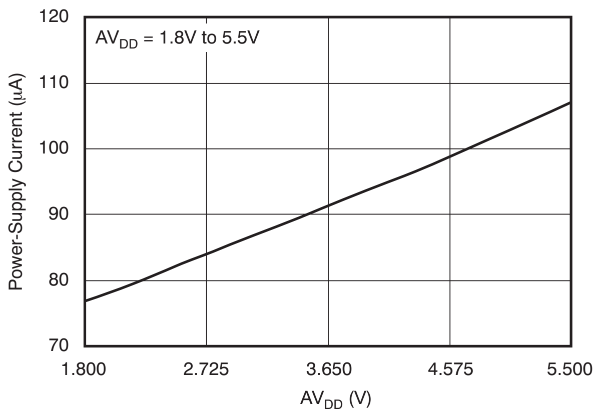


Figure 35.

POWER-DOWN CURRENT vs POWER-SUPPLY VOLTAGE

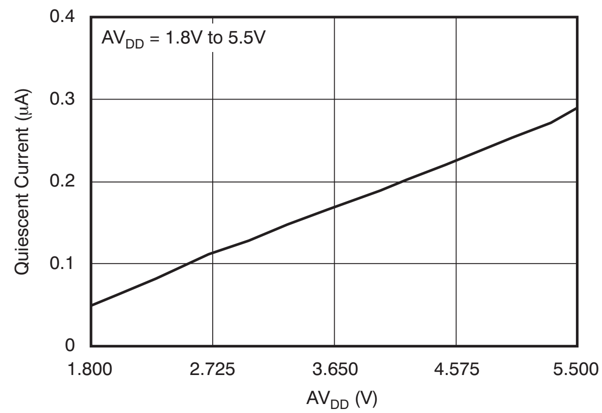


Figure 36.

POWER-SUPPLY CURRENT HISTOGRAM

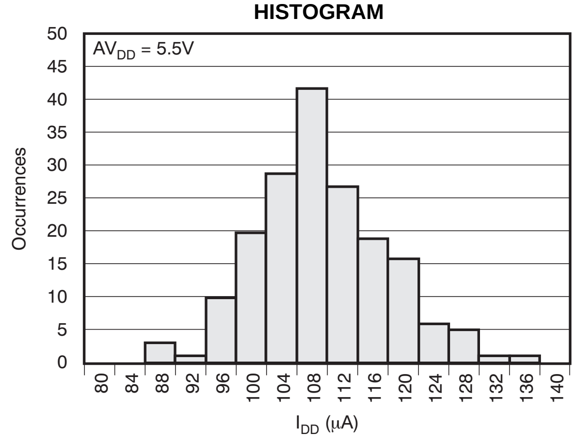


Figure 37.

TYPICAL CHARACTERISTICS: AV_{DD} = +3.6V

At T_A = 25°C, AV_{DD} = +3.6V, and DAC loaded with midscale code, unless otherwise noted.

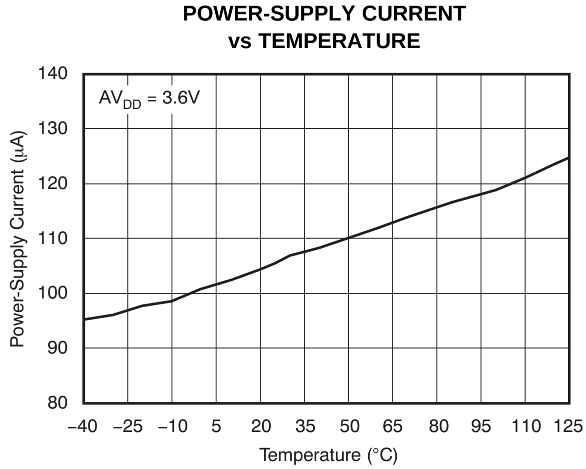


Figure 38.

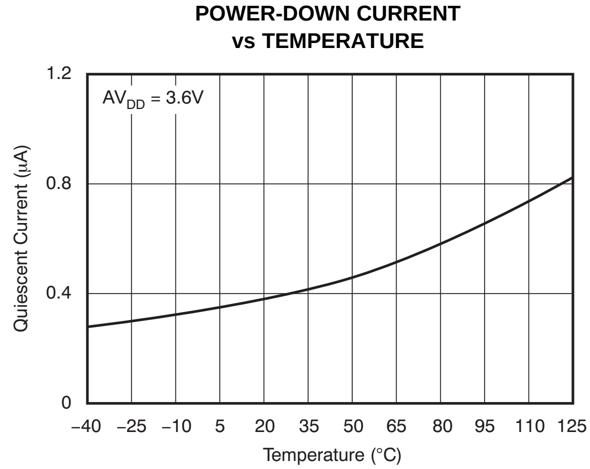


Figure 39.

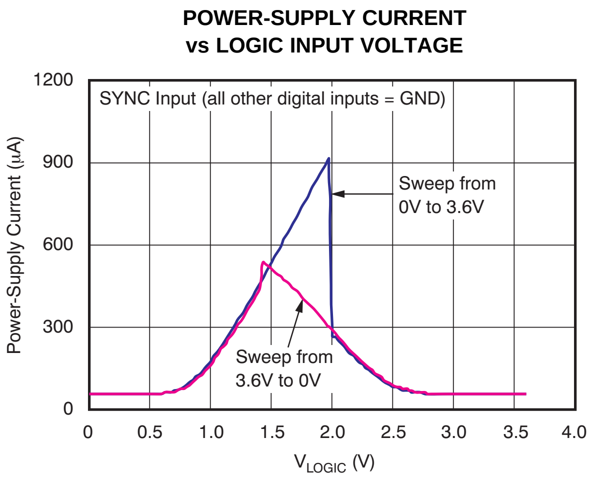


Figure 40.

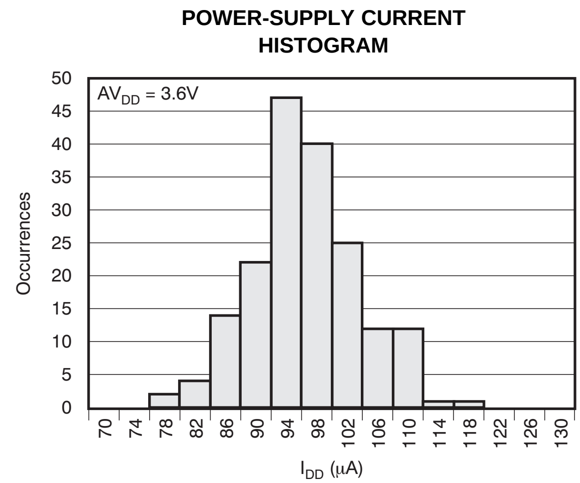


Figure 41.

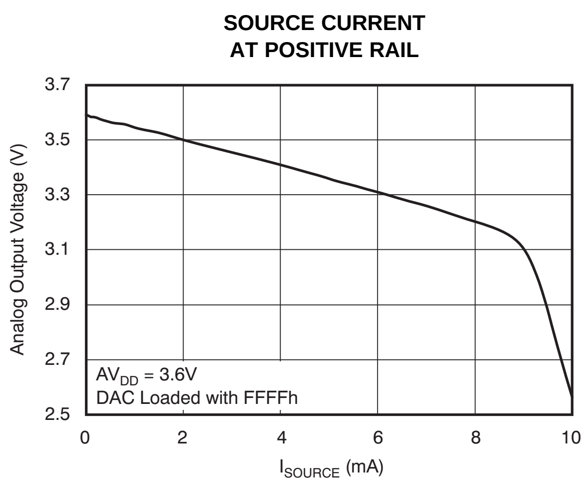


Figure 42.

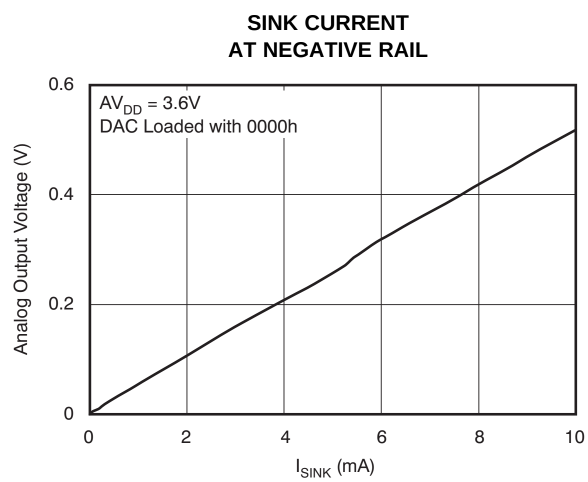


Figure 43.

TYPICAL CHARACTERISTICS: AV_{DD} = +2.7V

At T_A = 25°C, AV_{DD} = +2.7V, and DAC loaded with midscale code, unless otherwise noted.

DAC7311 12-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (–40°C)

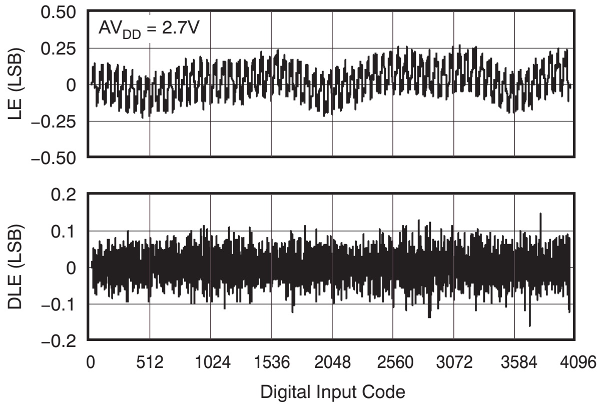


Figure 44.

DAC6311 10-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (–40°C)

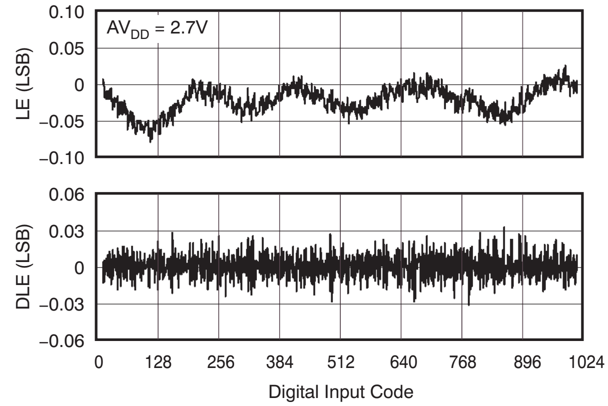


Figure 45.

DAC7311 12-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+25°C)

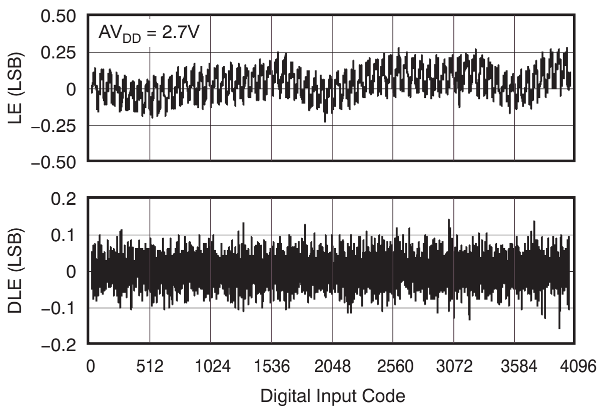


Figure 46.

DAC6311 10-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+25°C)

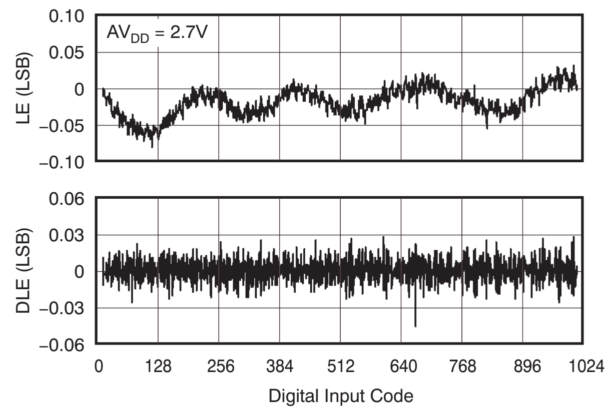


Figure 47.

DAC7311 12-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+125°C)

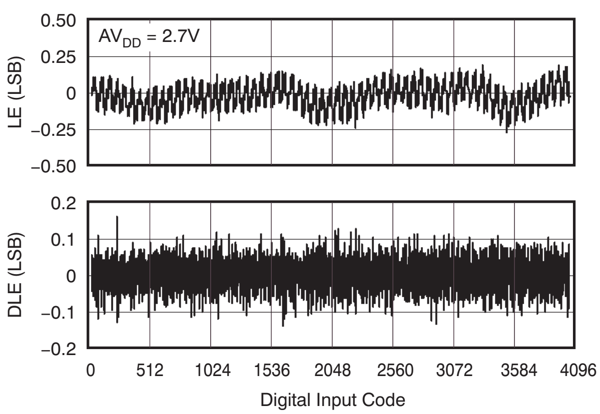


Figure 48.

DAC6311 10-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+125°C)

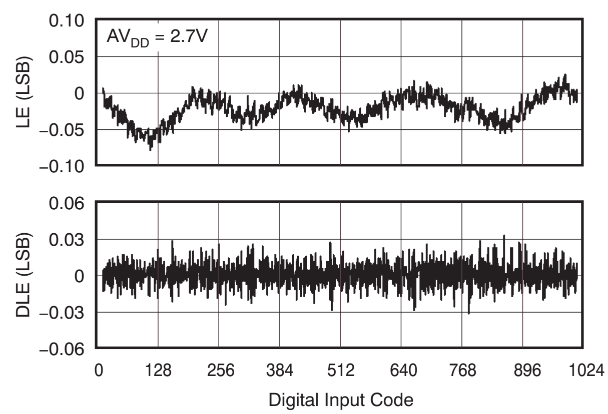


Figure 49.

TYPICAL CHARACTERISTICS: AV_{DD} = +2.7V (continued)

At T_A = 25°C, AV_{DD} = +2.7V, and DAC loaded with midscale code, unless otherwise noted.

DAC5311 8-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (–40°C)

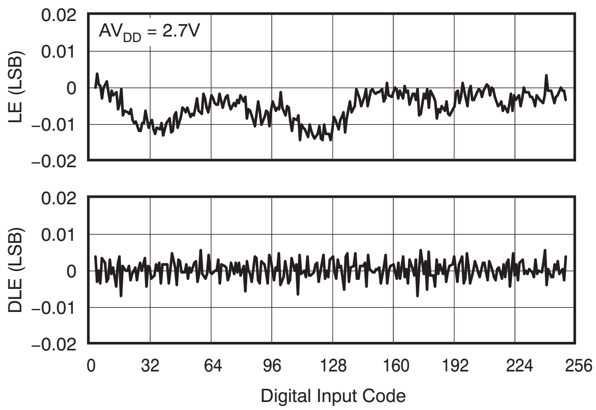


Figure 50.

ZERO-CODE ERROR vs TEMPERATURE

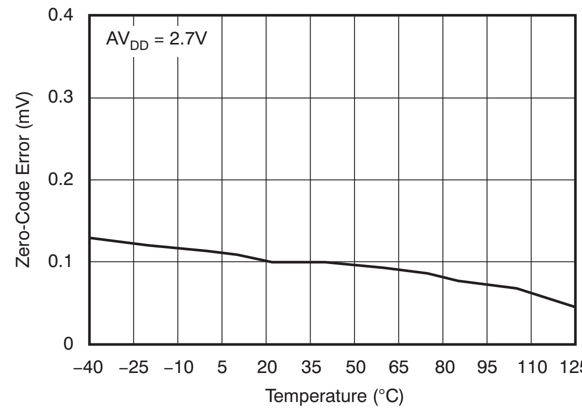


Figure 51.

DAC5311 8-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+25°C)

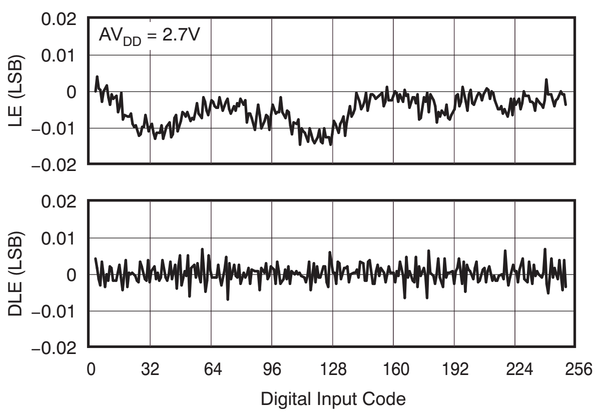


Figure 52.

OFFSET ERROR vs TEMPERATURE

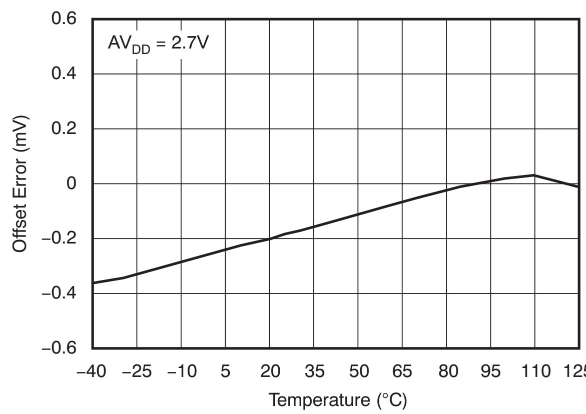


Figure 53.

DAC5311 8-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+125°C)

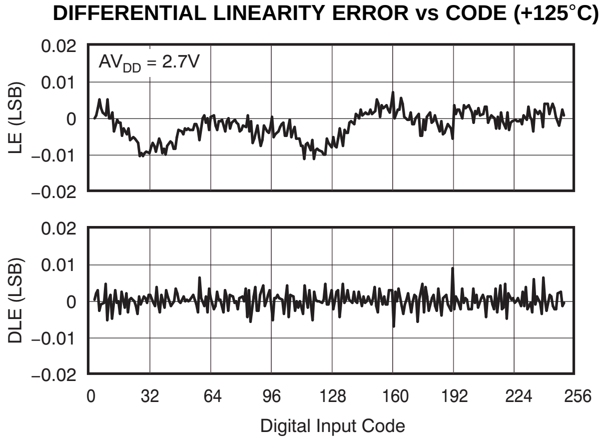


Figure 54.

FULL-SCALE ERROR vs TEMPERATURE

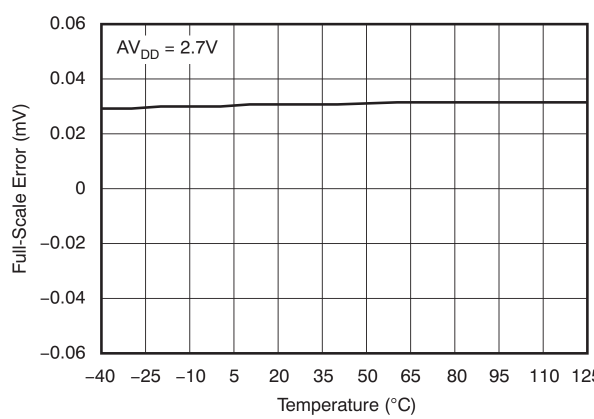


Figure 55.

TYPICAL CHARACTERISTICS: AV_{DD} = +2.7V (continued)

At T_A = 25°C, AV_{DD} = +2.7V, and DAC loaded with midscale code, unless otherwise noted.

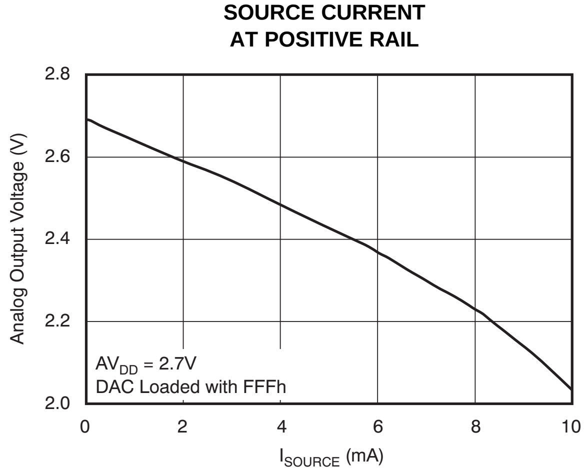


Figure 56.

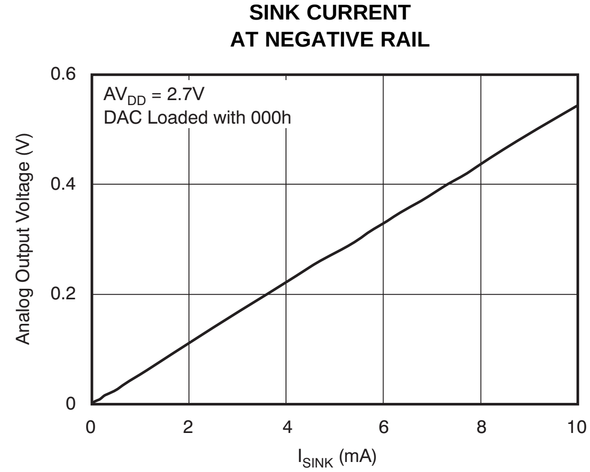


Figure 57.

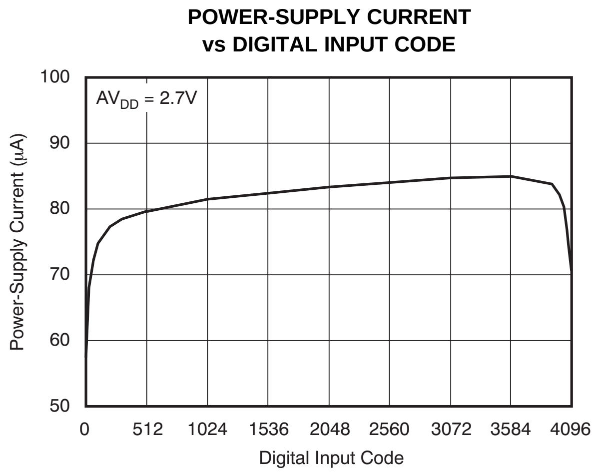


Figure 58.

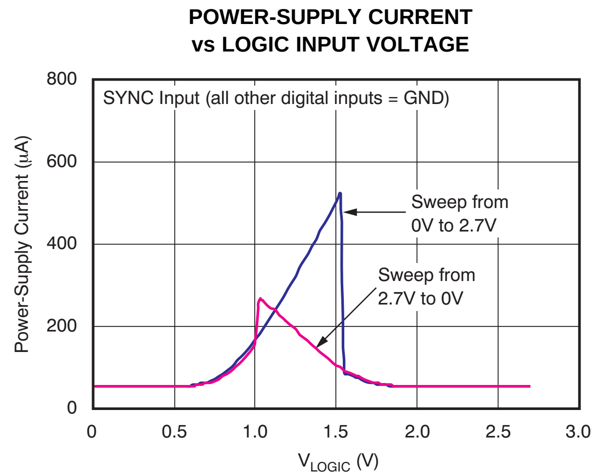


Figure 59.

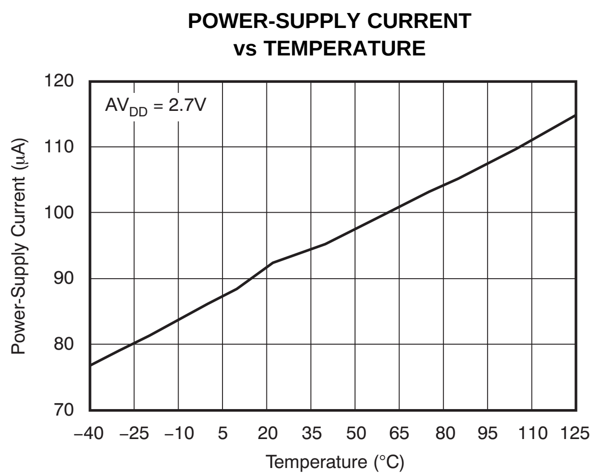


Figure 60.

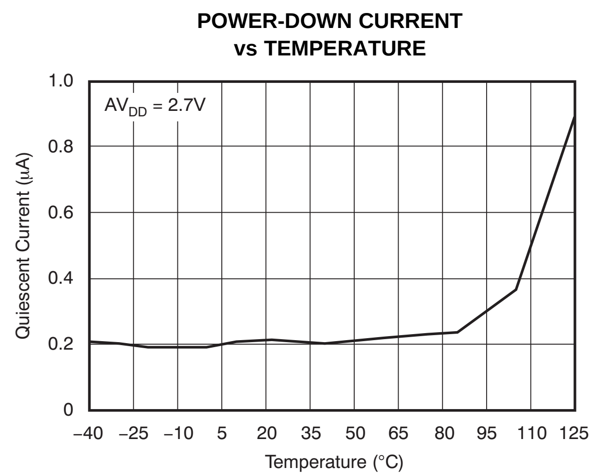


Figure 61.

TYPICAL CHARACTERISTICS: AV_{DD} = +2.7V (continued)

At T_A = 25°C, AV_{DD} = +2.7V, and DAC loaded with midscale code, unless otherwise noted.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

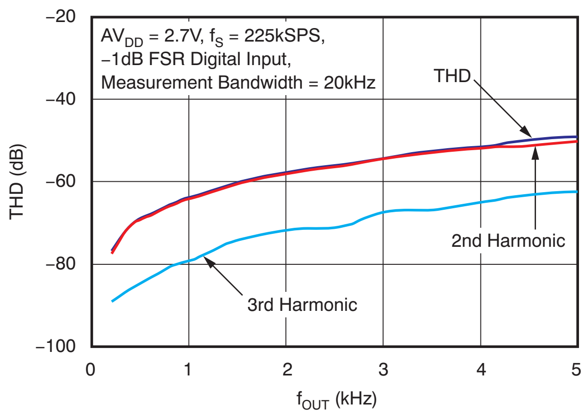


Figure 62.

SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY

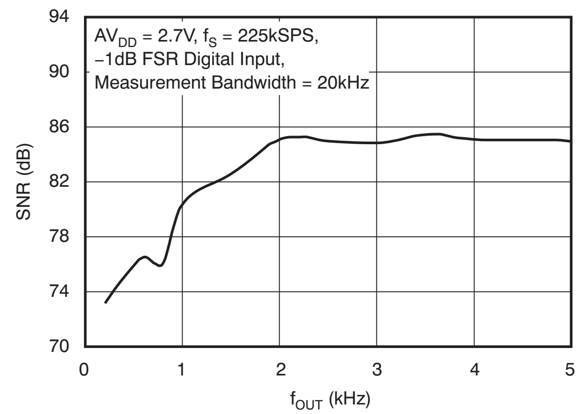


Figure 63.

POWER SPECTRAL DENSITY

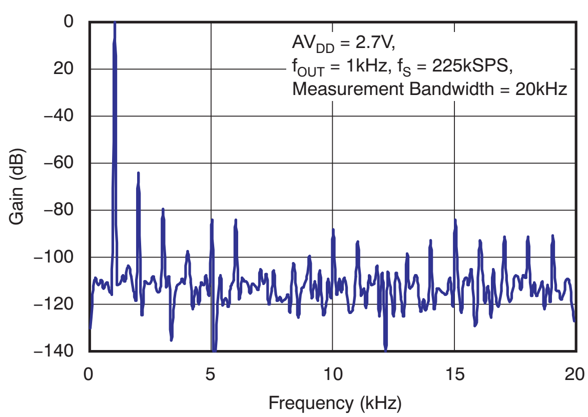


Figure 64.

POWER-SUPPLY CURRENT HISTOGRAM

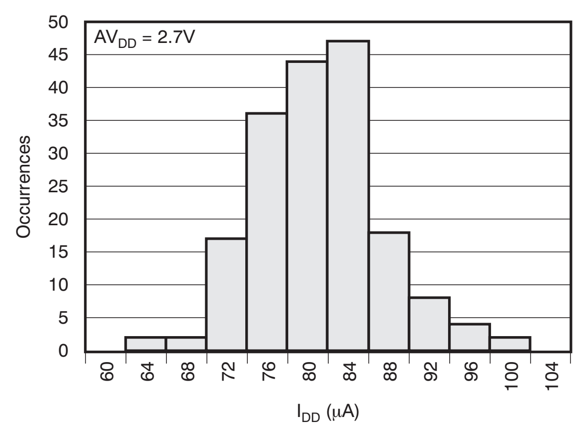


Figure 65.

TYPICAL CHARACTERISTICS: AV_{DD} = +2.7V (continued)

At T_A = 25°C, AV_{DD} = +2.7V, and DAC loaded with midscale code, unless otherwise noted.

CLOCK FEEDTHROUGH
2.7V, 20MHz, MIDSCALE

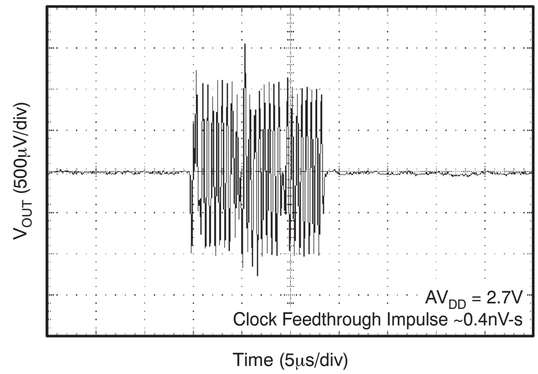


Figure 66.

GLITCH ENERGY
2.7V, 12-BIT, 1LSB STEP, RISING EDGE

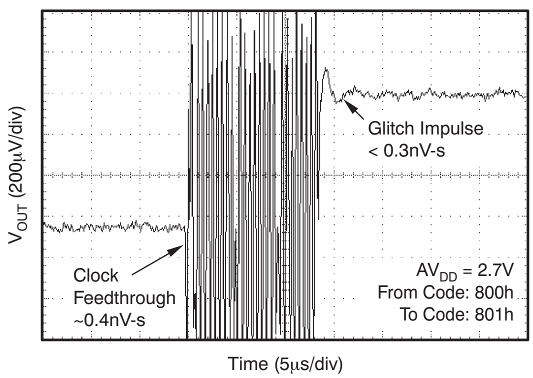


Figure 67.

GLITCH ENERGY
2.7V, 12-BIT, 1LSB STEP, FALLING EDGE

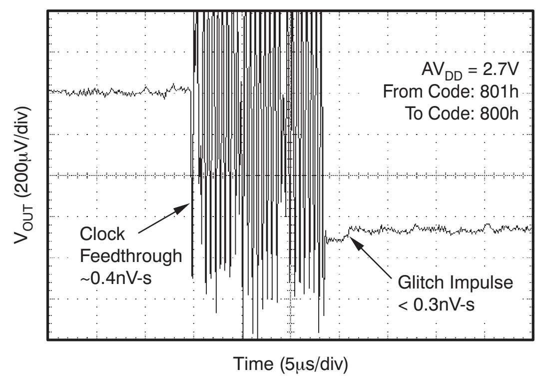


Figure 68.

GLITCH ENERGY
2.7V, 8-BIT, 1LSB STEP, RISING EDGE

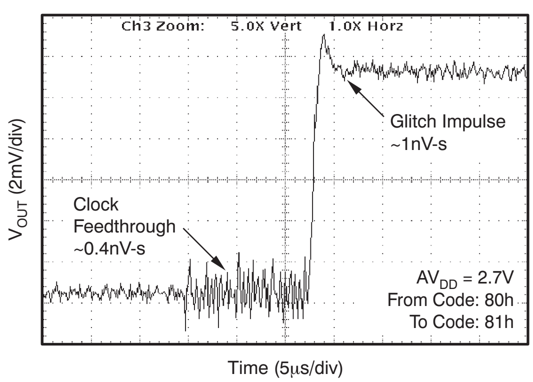


Figure 69.

GLITCH ENERGY
2.7V, 8-BIT, 1LSB STEP, FALLING EDGE

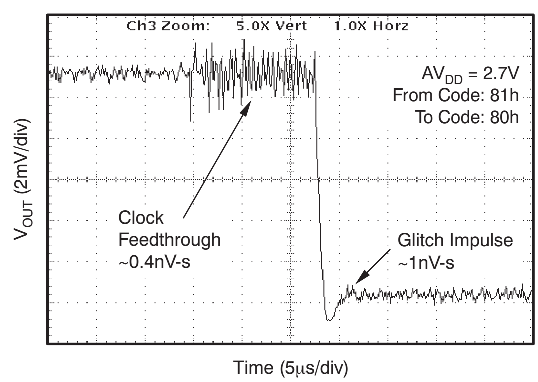


Figure 70.

TYPICAL CHARACTERISTICS: AV_{DD} = +2.7V (continued)

At T_A = 25°C, AV_{DD} = +2.7V, and DAC loaded with midscale code, unless otherwise noted.

**FULL-SCALE SETTLING TIME
2.7V RISING EDGE**

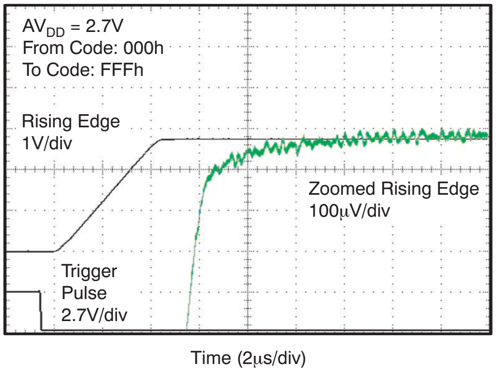


Figure 71.

**FULL-SCALE SETTLING TIME
2.7V FALLING EDGE**

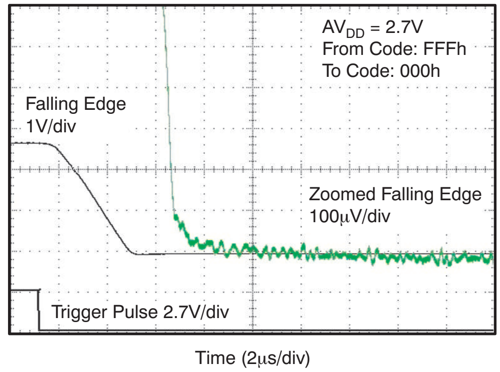


Figure 72.

**HALF-SCALE SETTLING TIME
2.7V RISING EDGE**

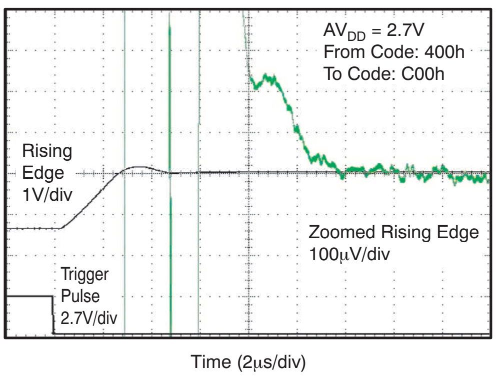


Figure 73.

**HALF-SCALE SETTLING TIME
2.7V FALLING EDGE**

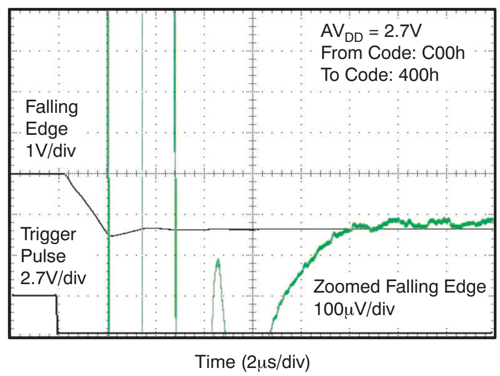


Figure 74.

**POWER-ON RESET TO 0V
POWER-ON GLITCH**

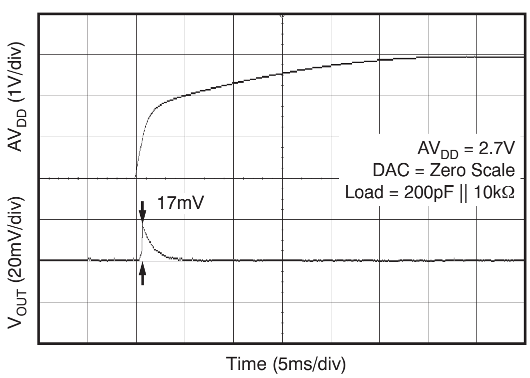


Figure 75.

POWER-OFF GLITCH

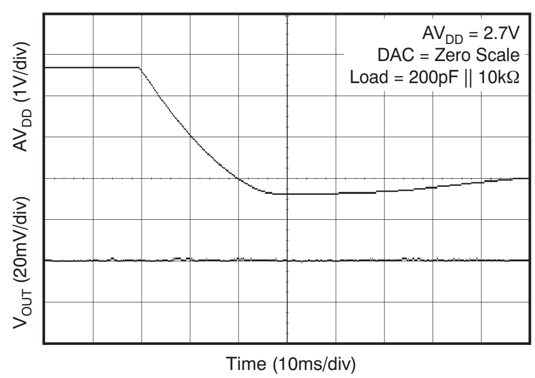


Figure 76.

TYPICAL CHARACTERISTICS: AV_{DD} = +1.8V

At T_A = 25°C, AV_{DD} = +1.8V, and DAC loaded with midscale code, unless otherwise noted.

DAC7311 12-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (–40°C)

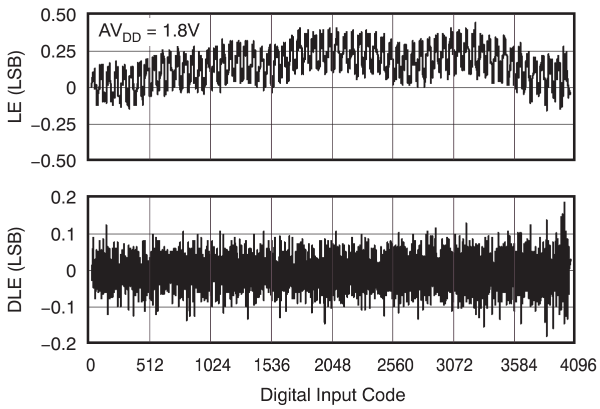


Figure 77.

DAC6311 10-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (–40°C)

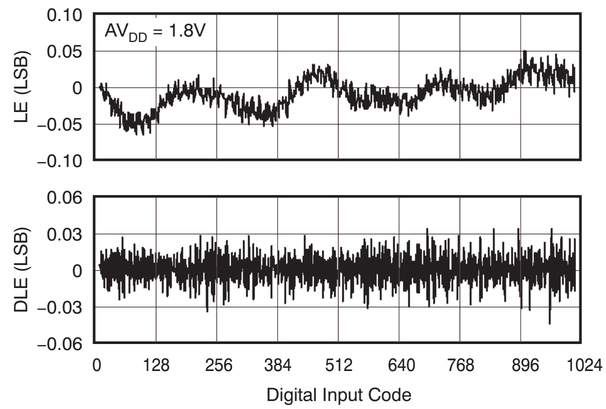


Figure 78.

DAC7311 12-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+25°C)

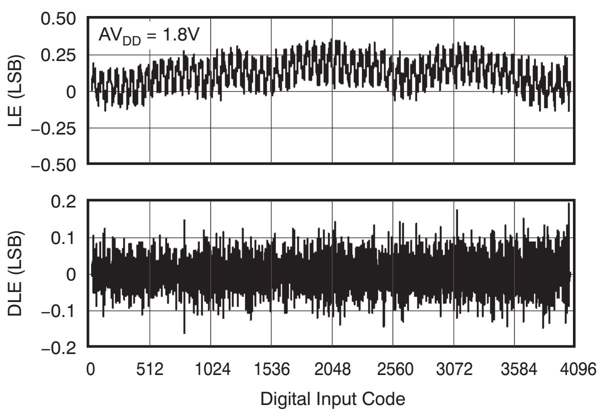


Figure 79.

DAC6311 10-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+25°C)

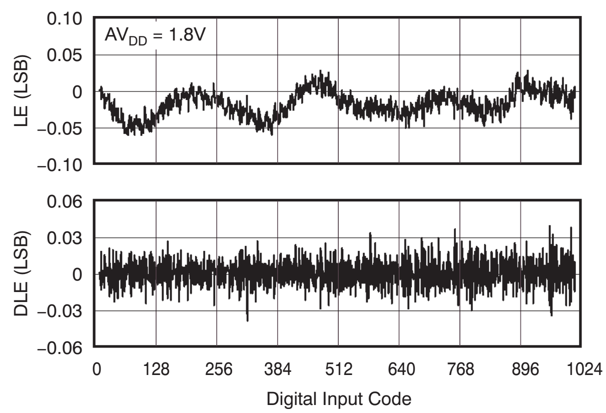


Figure 80.

DAC7311 12-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+125°C)

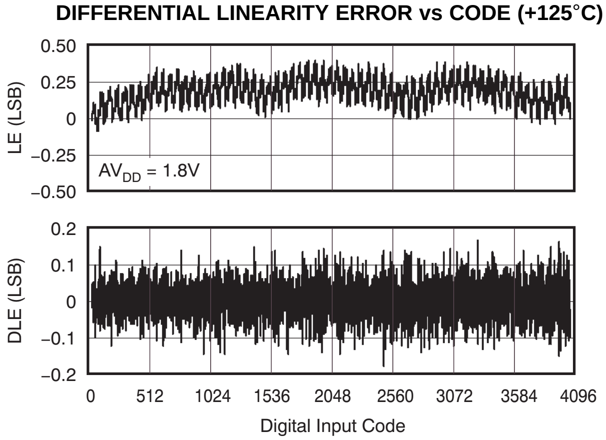


Figure 81.

DAC6311 10-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+125°C)

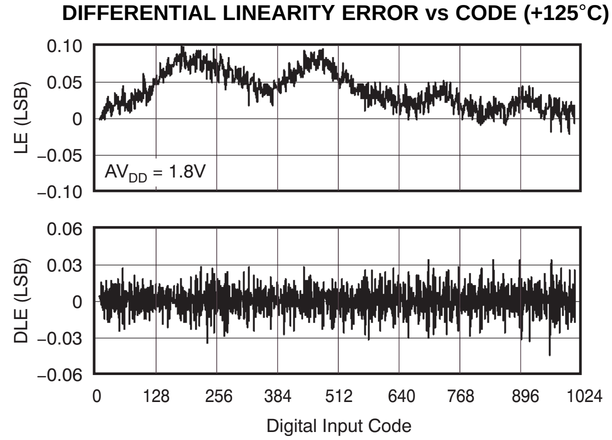


Figure 82.

TYPICAL CHARACTERISTICS: AV_{DD} = +1.8V (continued)

At T_A = 25°C, AV_{DD} = +1.8V, and DAC loaded with midscale code, unless otherwise noted.

DAC5311 8-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (–40°C)

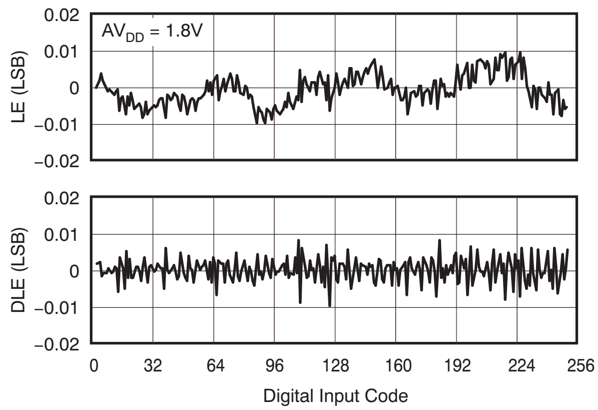


Figure 83.

ZERO-CODE ERROR vs TEMPERATURE

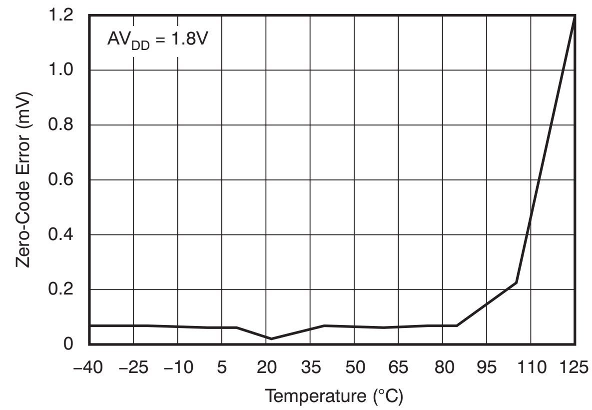


Figure 84.

DAC5311 8-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+25°C)

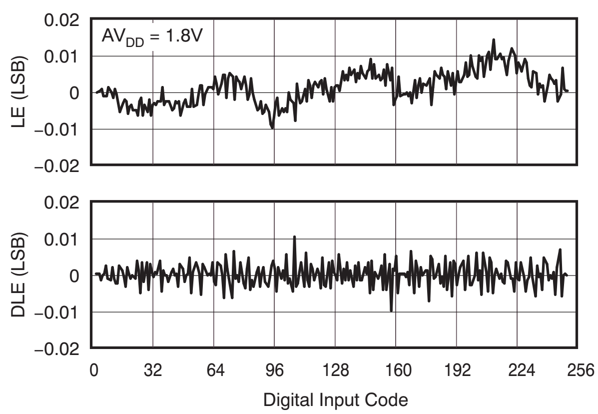


Figure 85.

OFFSET ERROR vs TEMPERATURE

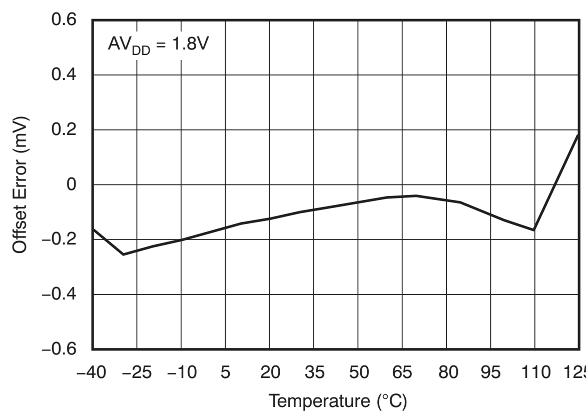


Figure 86.

DAC5311 8-BIT LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (+125°C)

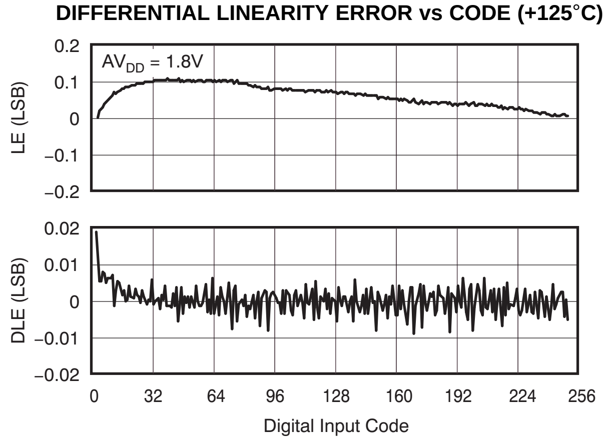


Figure 87.

FULL-SCALE ERROR vs TEMPERATURE

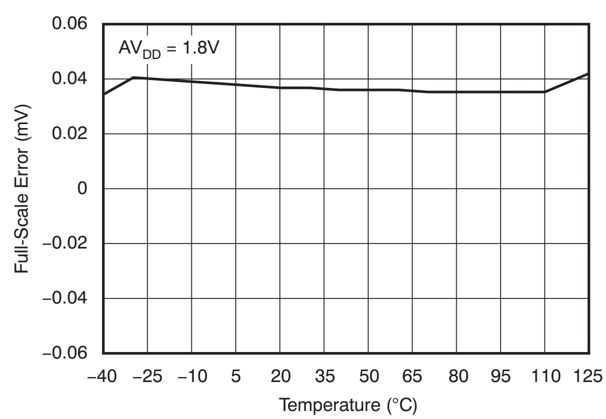


Figure 88.

TYPICAL CHARACTERISTICS: AV_{DD} = +1.8V (continued)

At T_A = 25°C, AV_{DD} = +1.8V, and DAC loaded with midscale code, unless otherwise noted.

SOURCE CURRENT AT POSITIVE RAIL

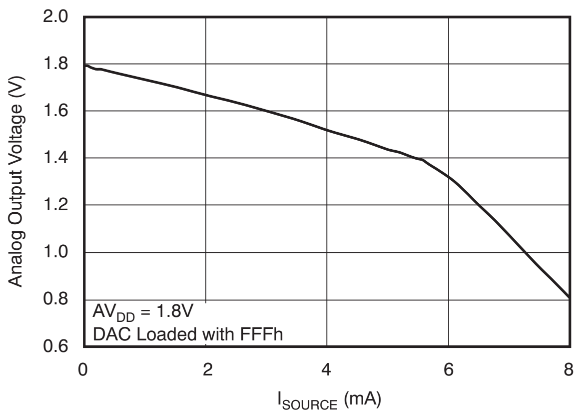


Figure 89.

SINK CURRENT AT NEGATIVE RAIL

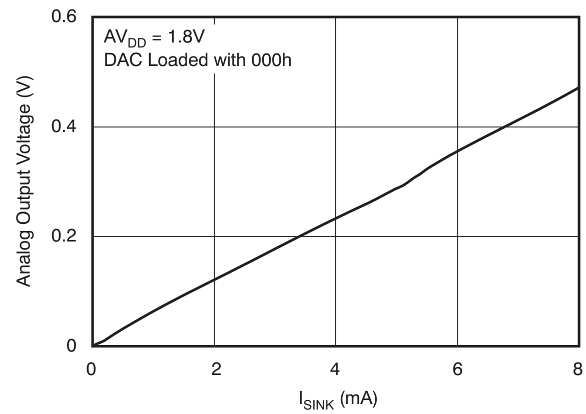


Figure 90.

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

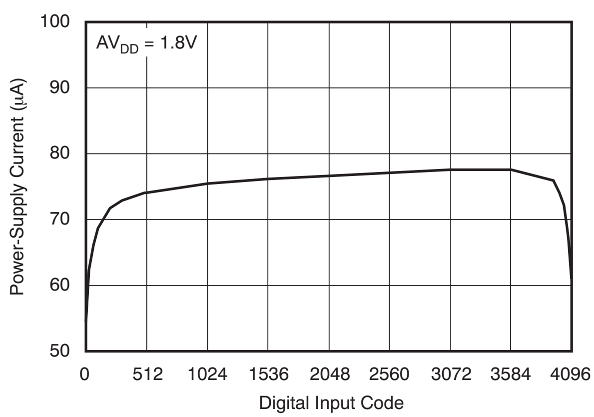


Figure 91.

POWER-SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

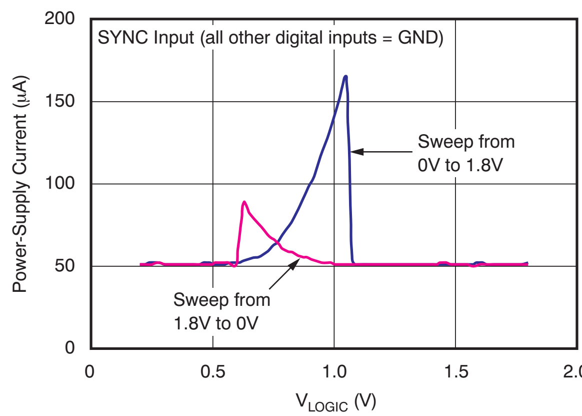


Figure 92.

POWER-SUPPLY CURRENT vs TEMPERATURE

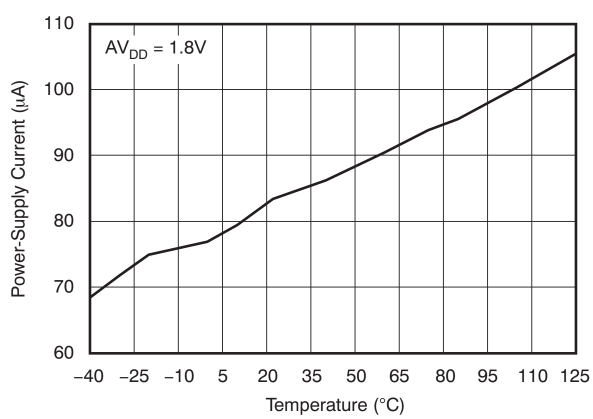


Figure 93.

POWER-DOWN CURRENT vs TEMPERATURE

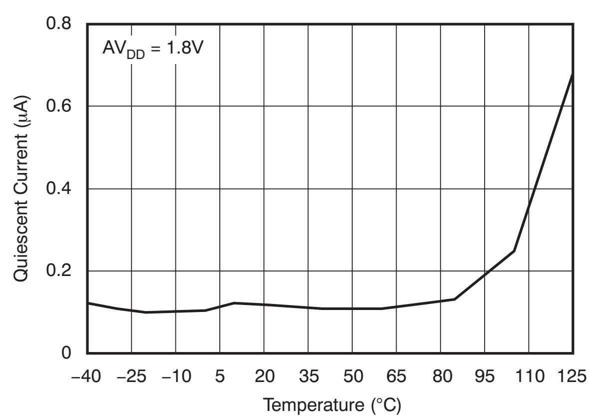


Figure 94.

TYPICAL CHARACTERISTICS: AV_{DD} = +1.8V (continued)

At T_A = 25°C, AV_{DD} = +1.8V, and DAC loaded with midscale code, unless otherwise noted.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

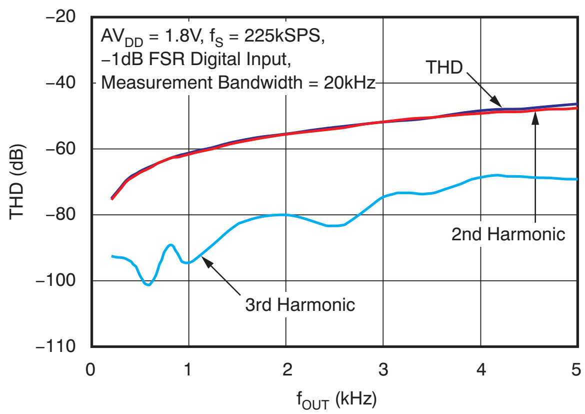


Figure 95.

SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY

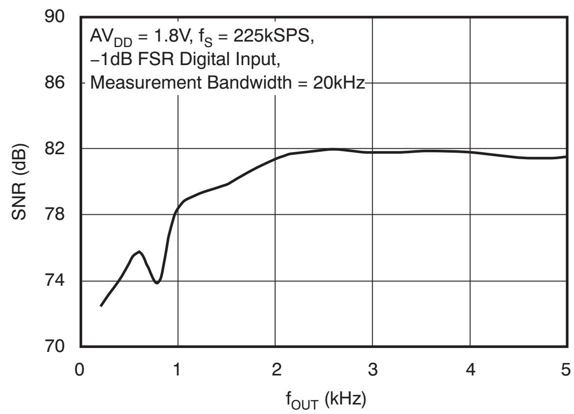


Figure 96.

POWER SPECTRAL DENSITY

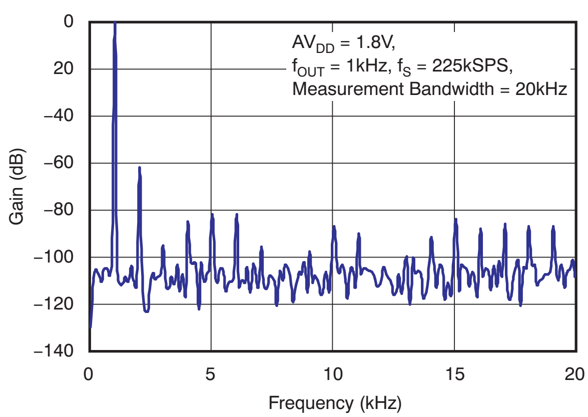


Figure 97.

POWER-SUPPLY CURRENT HISTOGRAM

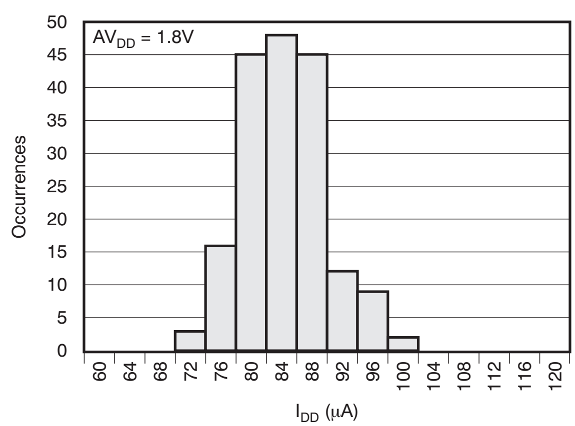


Figure 98.

TYPICAL CHARACTERISTICS: AV_{DD} = +1.8V (continued)

At T_A = 25°C, AV_{DD} = +1.8V, and DAC loaded with midscale code, unless otherwise noted.

CLOCK FEEDTHROUGH
1.8V, 20MHz, MIDSCALE

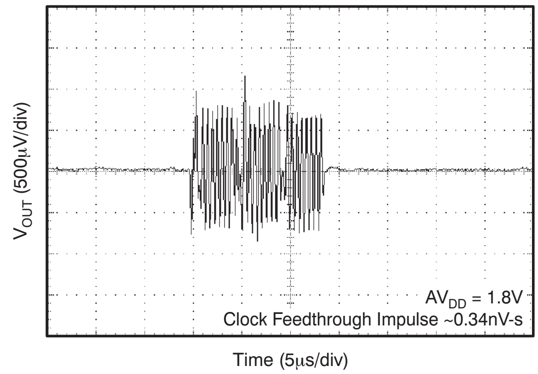


Figure 99.

GLITCH ENERGY
1.8V, 12-BIT, 1LSB STEP, RISING EDGE

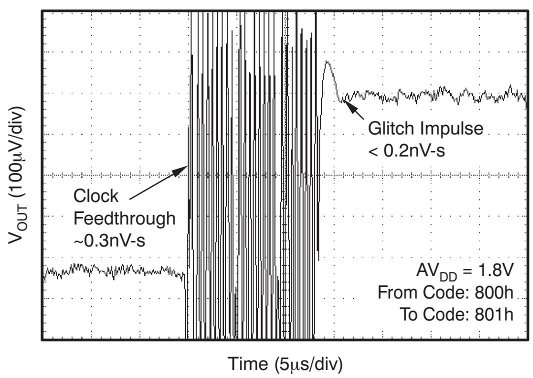


Figure 100.

GLITCH ENERGY
1.8V, 12-BIT, 1LSB STEP, FALLING EDGE

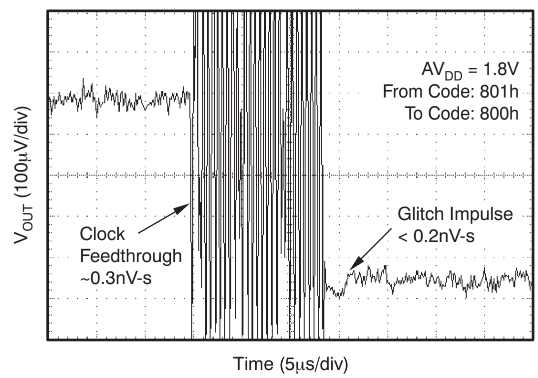


Figure 101.

GLITCH ENERGY
1.8V, 8-BIT, 1LSB STEP, RISING EDGE

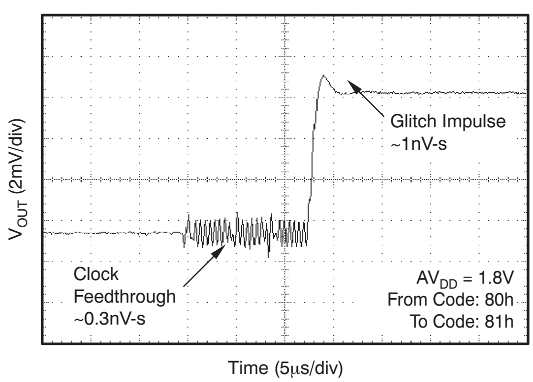


Figure 102.

GLITCH ENERGY
1.8V, 8-BIT, 1LSB STEP, FALLING EDGE

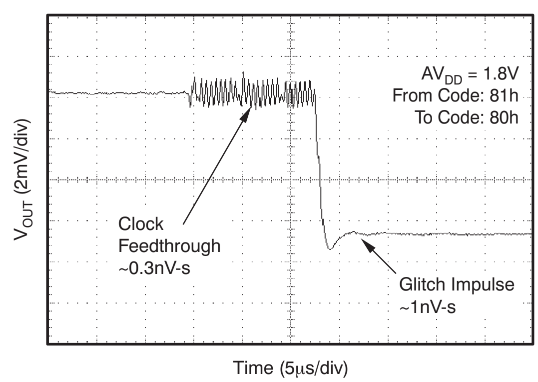


Figure 103.

TYPICAL CHARACTERISTICS: AV_{DD} = +1.8V (continued)

At T_A = 25°C, AV_{DD} = +1.8V, and DAC loaded with midscale code, unless otherwise noted.

FULL-SCALE SETTLING TIME 1.8V RISING EDGE

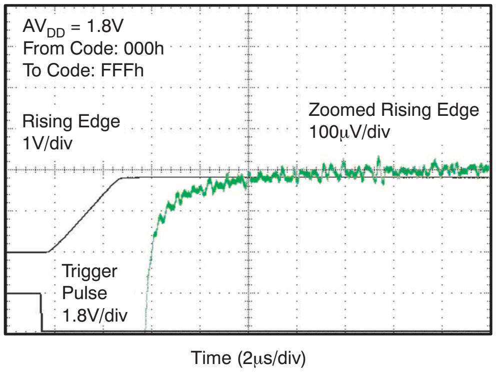


Figure 104.

FULL-SCALE SETTLING TIME 1.8V FALLING EDGE

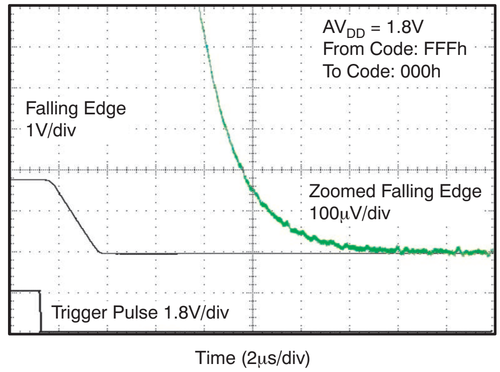


Figure 105.

HALF-SCALE SETTLING TIME 1.8V RISING EDGE

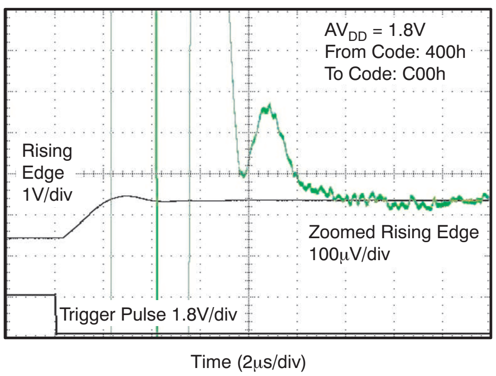


Figure 106.

HALF-SCALE SETTLING TIME 1.8V FALLING EDGE

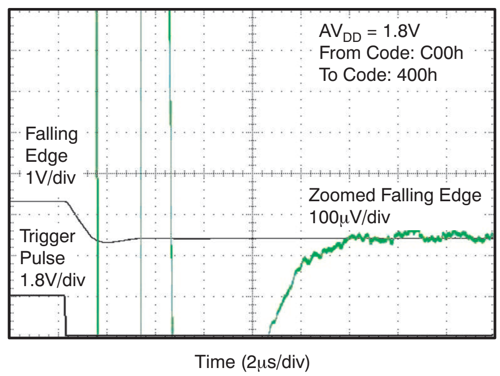


Figure 107.

POWER-ON RESET TO 0V POWER-ON GLITCH

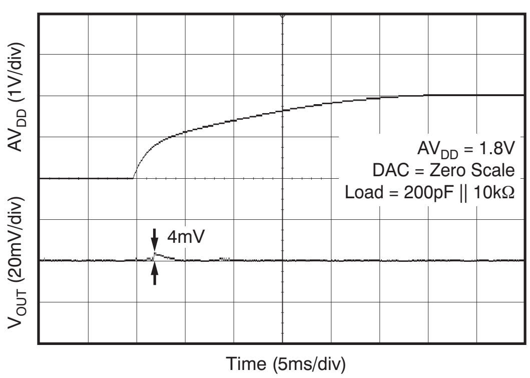


Figure 108.

POWER-OFF GLITCH

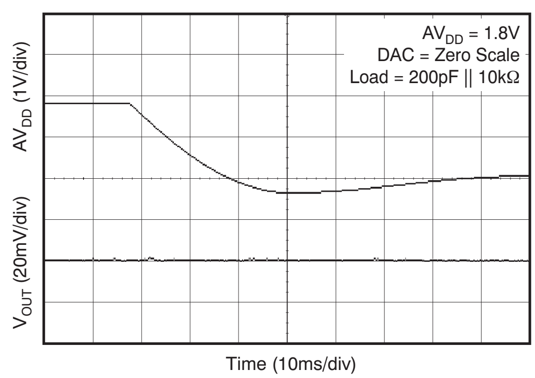


Figure 109.

THEORY OF OPERATION

DAC SECTION

The DAC5311, DAC6311, and DAC7311 are fabricated using TI's proprietary HPA07 process technology. The architecture consists of a string DAC followed by an output buffer amplifier. Because there is no reference input pin, the power supply (AV_{DD}) acts as the reference. Figure 110 shows a block diagram of the DAC architecture.

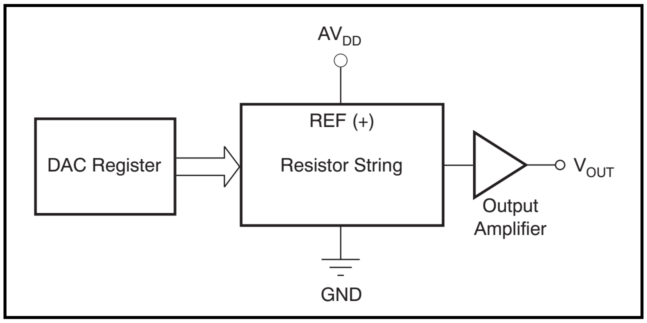


Figure 110. DACx311 Architecture

The input coding to the DACx311 is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = AV_{DD} \times \frac{D}{2^n}$$

Where:

n = resolution in bits; either 8 (DAC5311), 10 (DAC6311), or 12 (DAC7311).

D = decimal equivalent of the binary code that is loaded to the DAC register. It ranges from 0 to 255 for 8-bit DAC5311; from 0 to 1023 for the 10-bit DAC6311; and 0 to 4095 for the 12-bit DAC7311.

RESISTOR STRING

The resistor string section is shown in Figure 111. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is tested monotonic because it is a string of resistors.

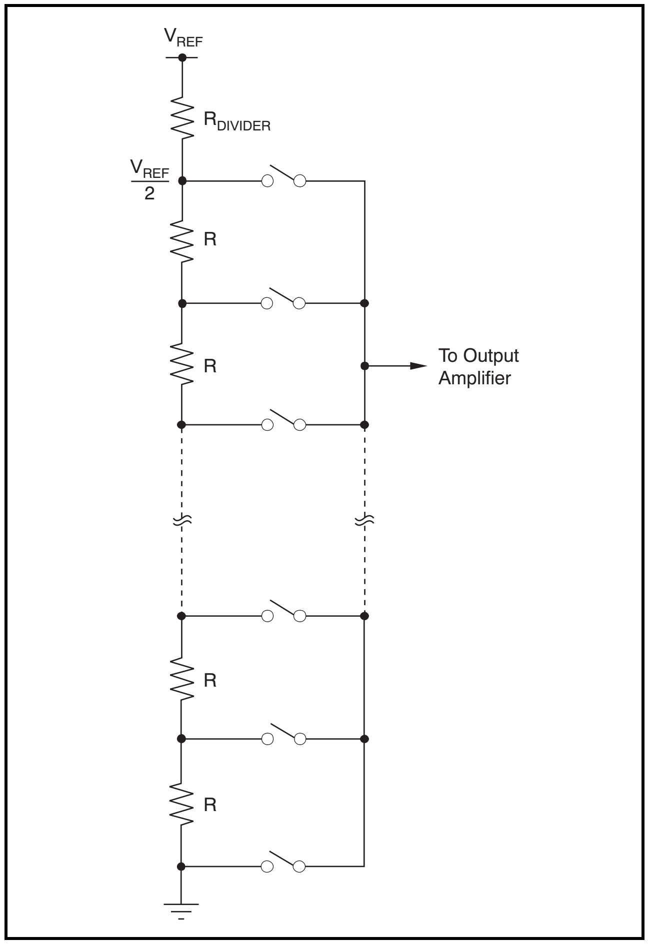


Figure 111. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0V to AV_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics section for the given voltage input. The slew rate is 0.7V/μs with a half-scale settling time of typically 6μs with the output unloaded.

SERIAL INTERFACE

The DACx311 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

DACx311 Input Shift Register

The input shift register is 16 bits wide, as shown in Table 2. The first two bits (PD0 and PD1) are reserved control bits that set the desired mode of operation (normal mode or any one of three power-down modes) as indicated in Table 5.

The remaining data bits are either 12 (DAC7311), 10 (DAC6311), or 8 (DAC5311) data bits, followed by *don't care* bits, as shown in Table 2, Table 3, and Table 4, respectively.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line are clocked into the 16-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50MHz, making the DACx311 compatible with high-speed DSPs. On the 16th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed.

At this point, the $\overline{\text{SYNC}}$ line may be kept low or brought high. In either case, it must be brought high for a minimum of 20ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. As previously mentioned, it must be brought high again before the next write sequence.

DACx311 $\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, bringing $\overline{\text{SYNC}}$ high before the 16th falling edge acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in Figure 112.

Table 2. DAC5311 8-Bit Data Input Register

DB15	DB14								DB6	DB5					DB0
PD1	PD0	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X

Table 3. DAC6311 10-Bit Data Input Register

DB15	DB14										DB4	DB3			DB0
PD1	PD0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

Table 4. DAC7311 12-Bit Data Input Register

DB15	DB14												DB2	DB1	DB0
PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X

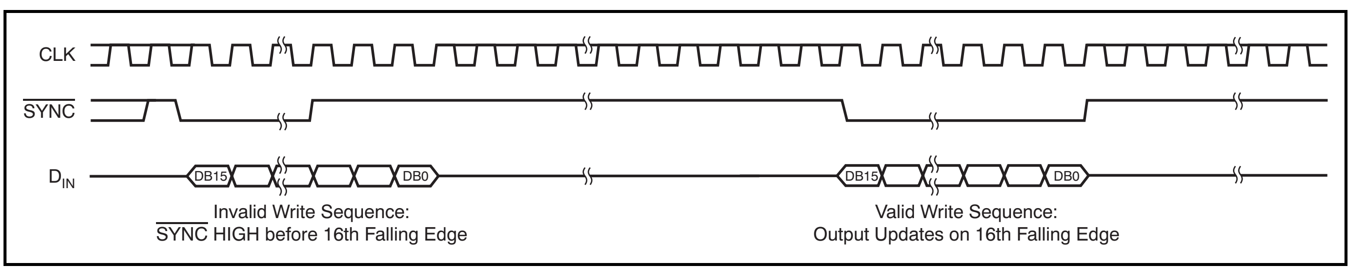


Figure 112. DACx311 $\overline{\text{SYNC}}$ Interrupt Facility

POWER-ON RESET TO ZERO-SCALE

The DACx311 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC register is filled with zeros and the output voltage is 0V. The DAC register remains that way until a valid write sequence is made to the DAC. This design is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

The occurring power-on glitch impulse is only a few millivolts (typically, 17mV; see Figure 33).

POWER-DOWN MODES

The DACx311 contains four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 5 shows how the state of the bits corresponds to the mode of operation of the device.

Table 5. Modes of Operation for the DACx311

PD1	PD0	OPERATING MODE
Normal Mode		
0	0	Normal Operation
Power-Down Modes		
0	1	Output 1kΩ to GND
1	0	Output 100kΩ to GND
1	1	High-Z

When both bits are set to '0', the device works normally with a standard power consumption of typically 80µA at 1.8V. However, for the three power-down modes, the typical supply current falls to 0.5µA at 5V, 0.4µA at 3V, and 0.1µA at 1.8V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. The advantage of this architecture is that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND either through a 1kΩ resistor or a 100kΩ resistor, or is left open-circuited (High-Z). Figure 113 illustrates the output stage.

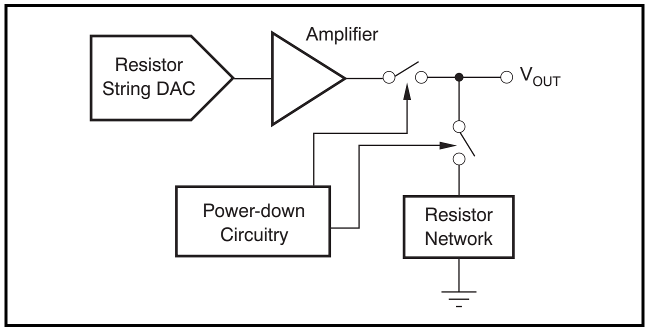


Figure 113. Output Stage During Power-Down

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 50µs for AV_{DD} = 5V and AV_{DD} = 3V.

DAC NOISE PERFORMANCE

Typical noise performance for the DACx311 is shown in Figure 34 and 35. Output noise spectral density at the V_{OUT} pin versus frequency is depicted in Figure 34 for full-scale, midscale, and zero-scale input codes. The typical noise density for midscale code is 110nV/$\sqrt{Hz}$ at 1kHz and at 1MHz.

APPLICATION INFORMATION

USING THE REF5050 AS A POWER SUPPLY FOR THE DACx311

As a result of the extremely low supply current required by the DACx311, an alternative option is to use a REF5050 +5V precision voltage reference to supply the required voltage to the part, as shown in Figure 114. This option is especially useful if the power supply is too noisy or if the system supply voltages are at some value other than 5V. The REF5050 outputs a steady supply voltage for the DACx311. If the REF5050 is used, the current needed to supply DACx311 is typically 110µA at 5V, with no load on the output of the DAC. When the DAC output is loaded, the REF5050 also needs to supply the current to the load. The total current required (with a 5kΩ load on the DAC output) is:

110µA + (5V/5kΩ) = 1.11mA

The load regulation of the REF5050 is typically 0.002%/mA, which results in an error of 90µV for the 1.1mA current drawn from it. This value corresponds to a 0.07LSB error at 12 bits (DAC7311).

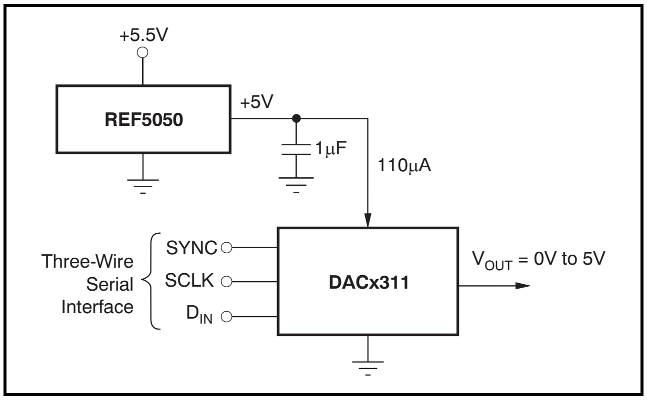


Figure 114. REF5050 as Power Supply to DACx311

For other power-supply voltages, alternative references such as the REF3030 (3V), REF3033 (3.3V), or REF3220 (2.048V) are recommended. For a full list of available voltage references from TI, see the TI web site at www.ti.com.

BIPOLAR OPERATION USING THE DACx311

The DACx311 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 115. The circuit shown gives an output voltage range of ±5V. Rail-to-rail operation at the amplifier output is achievable using an OPA211, OPA340, or OPA703 as the output amplifier. For a full list of available operational amplifiers from TI, see the TI web site at www.ti.com

The output voltage for any input code can be calculated as follows:

$$V_O = \left[AV_{DD} \times \left(\frac{D}{2^n}\right) \times \left(\frac{R_1 + R_2}{R_1}\right) - AV_{DD} \times \left(\frac{R_2}{R_1}\right)\right] \quad (1)$$

Where:

n = resolution in bits; either 8 (DAC5311), 10 (DAC6311), or 12 (DAC7311).

D = decimal equivalent of the binary code that is loaded to the DAC register. It ranges from 0 to 255 for 8-bit DAC5311; from 0 to 1023 for the 10-bit DAC6311; and 0 to 4095 for the 12-bit DAC7311.

With AV_{DD} = 5V, $R_1 = R_2$ = 10kΩ:

$$V_O = \left(\frac{10 \times D}{2^n}\right) - 5V \quad (2)$$

This is an output voltage range of ±5V with 000h (12-bit level) corresponding to a –5V output and FFFh (12-bit level) corresponding to a +5V output.

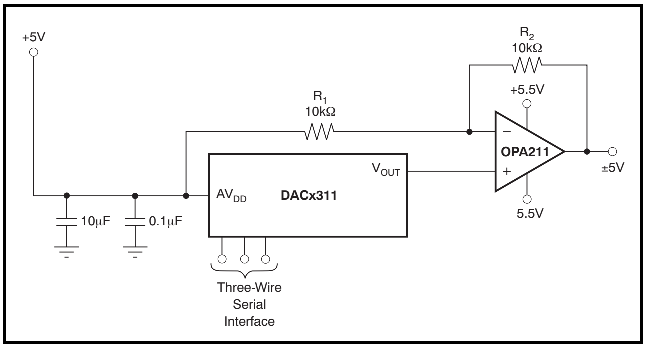
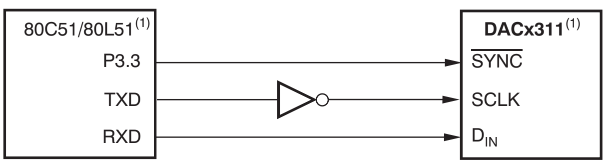


Figure 115. Bipolar Operation with the DACx311

MICROPROCESSOR INTERFACING

DACx311 to 8051 Interface

Figure 116 shows a serial interface between the DACx311 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DACx311, while RXD drives the serial data line of the part. The SYNC signal is derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data are to be transmitted to the DACx311, P3.3 is taken low. The 8051 transmits data only in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 remains low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 8051 outputs the serial data in a format which has the LSB first. The DACx311 requires its data with the MSB as the first bit received. Therefore, the 8051 transmit routine must take this requirement into account, and *mirror* the data as needed.

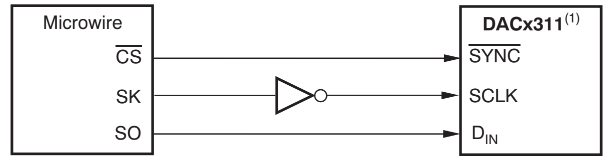


NOTE: (1) Additional pins omitted for clarity.

Figure 116. DACx311 to 80C51/80L51 Interfaces

DACx311 to Microwire Interface

Figure 117 shows an interface between the DACx311 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and are clocked into the DACx311 on the rising edge of the SK signal.

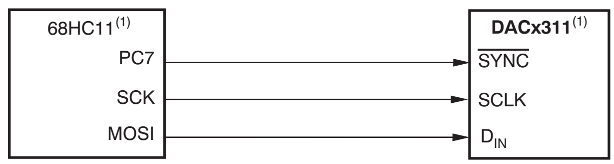


NOTE: (1) Additional pins omitted for clarity.

Figure 117. DACx311 to Microwire Interface

DACx311 to 68HC11 Interface

Figure 118 shows a serial interface between the DACx311 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DACx311, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7), similar to what was done for the 8051.



NOTE: (1) Additional pins omitted for clarity.

Figure 118. DACx311 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is a '0' and its CPHA bit is a '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the SYNC line is taken low (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data are transmitted MSB first. In order to load data to the DACx311, PC7 is held low after the first eight bits are transferred, and a second serial write operation is performed to the DAC; PC7 is taken high at the end of this procedure.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DACx311 offers single-supply operation; it is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

Because of the single ground pin of the DACx311, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND is connected directly to an analog ground plane. This plane should be separate from the ground connection for the digital components until they are connected at the power entry point of the system.

The power applied to AV_{DD} should be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as the internal logic switches state. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. This condition is particularly true for the DACx311, as the power supply is also the reference voltage for the DAC.

As with the GND connection, AV_{DD} should be connected to a +5V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1μF to 10μF and 0.1μF bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a 100μF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the +5V supply, removing the high-frequency noise.

PARAMETER DEFINITIONS

With the increased complexity of many different specifications listed in product data sheets, this section summarizes selected specifications related to digital-to-analog converters.

STATIC PERFORMANCE

Static performance parameters are specifications such as differential nonlinearity (DNL) or integral nonlinearity (INL). These are dc specifications and provide information on the accuracy of the DAC. They are most important in applications where the signal changes slowly and accuracy is required.

Resolution

Generally, the DAC resolution can be expressed in different forms. Specifications such as IEC 60748-4 recognize the numerical, analog, and relative resolution. The numerical resolution is defined as the number of digits in the chosen numbering system necessary to express the total number of steps of the transfer characteristic, where a step represents both a digital input code and the corresponding discrete analogue output value. The most commonly-used definition of resolution provided in data sheets is the numerical resolution expressed in bits.

Least Significant Bit (LSB)

The least significant bit (LSB) is defined as the smallest value in a binary coded system. The value of the LSB can be calculated by dividing the full-scale output voltage by 2^n, where *n* is the resolution of the converter.

Most Significant Bit (MSB)

The most significant bit (MSB) is defined as the largest value in a binary coded system. The value of the MSB can be calculated by dividing the full-scale output voltage by 2. Its value is one-half of full-scale.

Relative Accuracy or Integral Nonlinearity (INL)

Relative accuracy or integral nonlinearity (INL) is defined as the maximum deviation between the real transfer function and a straight line passing through the endpoints of the ideal DAC transfer function. INL is measured in LSBs.

Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is defined as the maximum deviation of the real LSB step from the ideal 1LSB step. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. If the DNL is within ±1LSB, the DAC is said to be monotonic.

Full-Scale Error

Full-scale error is defined as the deviation of the real full-scale output voltage from the ideal output voltage while the DAC register is loaded with the full-scale code (0xFFFF). Ideally, the output should be V_{DD} – 1LSB. The full-scale error is expressed in percent of full-scale range (%FSR).

Offset Error

Offset error is defined as the difference between actual output voltage and the ideal output voltage in the linear region of the transfer function. This difference is calculated by using a straight line defined by two codes (for example, for 16-bit resolution, codes 485 and 64714). Since the offset error is defined by a straight line, it can have a negative or positve value. Offset error is measured in mV.

Zero-Code Error

Zero-code error is defined as the DAC output voltage, when all '0's are loaded into the DAC register. Zero-scale error is a measure of the difference between actual output voltage and ideal output voltage (0V). It is expressed in mV. It is primarily caused by offsets in the output amplifier.

Gain Error

Gain error is defined as the deviation in the slope of the real DAC transfer characteristic from the ideal transfer function. Gain error is expressed as a percentage of full-scale range (%FSR).

Full-Scale Error Drift

Full-scale error drift is defined as the change in full-scale error with a change in temperature. Full-scale error drift is expressed in units of %FSR/°C.

Offset Error Drift

Offset error drift is defined as the change in offset error with a change in temperature. Offset error drift is expressed in μV/°C.

Zero-Code Error Drift

Zero-code error drift is defined as the change in zero-code error with a change in temperature. Zero-code error drift is expressed in μV/°C.

Gain Temperature Coefficient

The gain temperature coefficient is defined as the change in gain error with changes in temperature. The gain temperature coefficient is expressed in ppm of FSR/°C.

Power-Supply Rejection Ratio (PSRR)

Power-supply rejection ratio (PSRR) is defined as the ratio of change in output voltage to a change in supply voltage for a full-scale output of the DAC. The PSRR of a device indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is measured in decibels (dB).

Monotonicity

Monotonicity is defined as a slope whose sign does not change. If a DAC is monotonic, the output changes in the same direction or remains at least constant for each step increase (or decrease) in the input code.

DYNAMIC PERFORMANCE

Dynamic performance parameters are specifications such as settling time or slew rate, which are important in applications where the signal rapidly changes and/or high frequency signals are present.

Slew Rate

The output slew rate (SR) of an amplifier or other electronic circuit is defined as the maximum rate of change of the output voltage for all possible input signals.

$$SR = \max\left(\left|\frac{\Delta V_{OUT}(t)}{\Delta t}\right|\right) \quad (3)$$

Where $\Delta V_{OUT}(t)$ is the output produced by the amplifier as a function of time *t*.

Output Voltage Settling Time

Settling time is the total time (including slew time) for the DAC output to settle within an error band around its final value after a change in input. Settling times are specified to within ±0.003% (or whatever value is specified) of full-scale range (FSR).

Code Change/Digital-to-Analog Glitch Energy

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanovolts-second (nV-s), and is measured when the digital input code is changed by 1LSB at the major carry transition.

Digital Feedthrough

Digital feedthrough is defined as impulse seen at the output of the DAC from the digital inputs of the DAC. It is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus; that is, from all '0's to all '1's and vice versa.

Channel-to-Channel DC Crosstalk

Channel-to-channel dc crosstalk is defined as the dc change in the output level of one DAC channel in response to a change in the output of another DAC channel. It is measured with a full-scale output change on one DAC channel while monitoring another DAC channel remains at midscale. It is expressed in LSB.

Channel-to-Channel AC Crosstalk

AC crosstalk in a multi-channel DAC is defined as the amount of ac interference experienced on the output of a channel at a frequency (f) (and its harmonics), when the output of an adjacent channel changes its value at the rate of frequency (f). It is measured with one channel output oscillating with a sine wave of 1kHz frequency, while monitoring the amplitude of 1kHz harmonics on an adjacent DAC channel output (kept at zero scale). It is expressed in dB.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) is defined as the ratio of the root mean-squared (RMS) value of the output signal divided by the RMS values of the sum of all other spectral components below one-half the output frequency, not including harmonics or dc. SNR is measured in dB.

Total Harmonic Distortion (THD)

Total harmonic distortion + noise is defined as the ratio of the RMS values of the harmonics and noise to the value of the fundamental frequency. It is expressed in a percentage of the fundamental frequency amplitude at sampling rate f_S.

Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range (SFDR) is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of the difference in amplitude between the fundamental and the largest harmonically or non-harmonically related spur from dc to the full Nyquist bandwidth (half the DAC sampling rate, or $f_S/2$). A spur is any frequency bin on a spectrum analyzer, or from a Fourier transform, of the analog output of the DAC. SFDR is specified in decibels relative to the carrier (dBc).

Signal-to-Noise plus Distortion (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing any internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DAC Output Noise Density

Output noise density is defined as internally-generated random noise. Random noise is characterized as a spectral density ($nV/\sqrt{Hz}$). It is measured by loading the DAC to midscale and measuring noise at the output.

DAC Output Noise

DAC output noise is defined as any voltage deviation of DAC output from the desired value (within a particular frequency band). It is measured with a DAC channel kept at midscale while filtering the output voltage within a band of 0.1Hz to 10Hz and measuring its amplitude peaks. It is expressed in terms of peak-to-peak voltage (V_{pp}).

Full-Scale Range (FSR)

Full-scale range (FSR) is the difference between the maximum and minimum analog output values that the DAC is specified to provide; typically, the maximum and minimum values are also specified. For an *n*-bit DAC, these values are usually given as the values matching with code 0 and $2^n – 1$.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August, 2008) to Revision A **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DAC5311IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC5311IDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC5311IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC5311IDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC6311IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC6311IDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC6311IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC6311IDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC7311IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC7311IDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC7311IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
DAC7311IDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF DAC5311 :

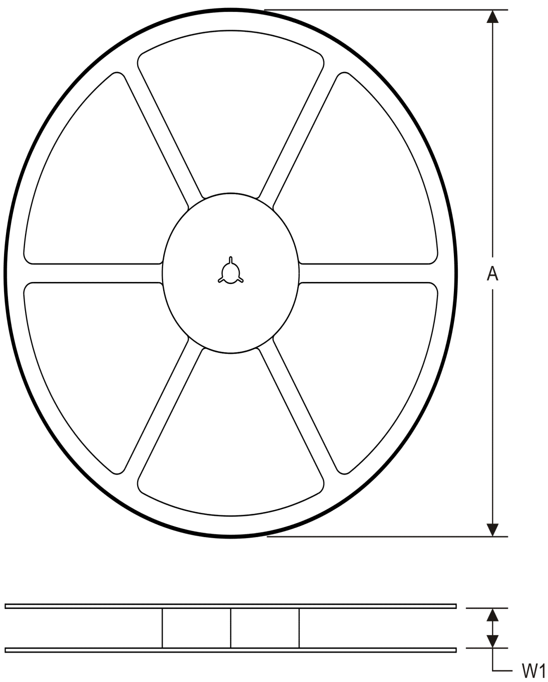
- Automotive: DAC5311-Q1

NOTE: Qualified Version Definitions:

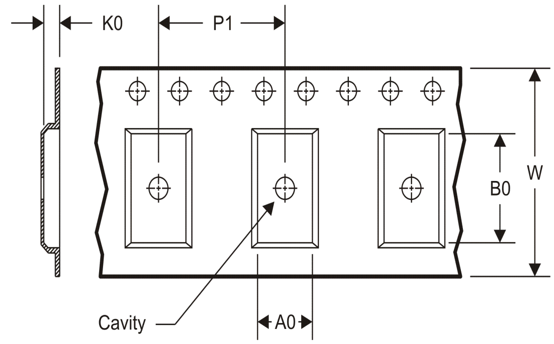
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



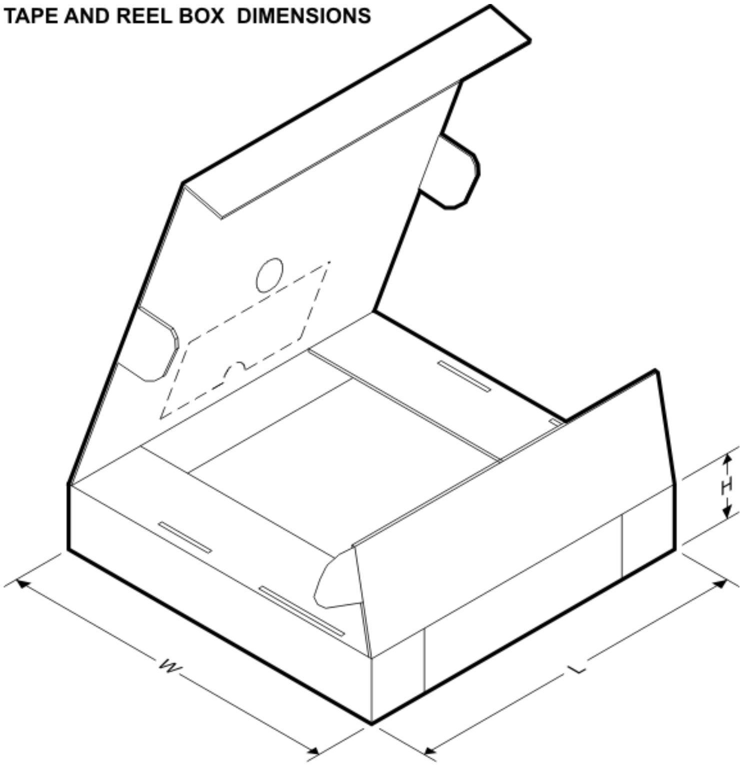
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5311IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC5311IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC6311IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC6311IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC7311IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC7311IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

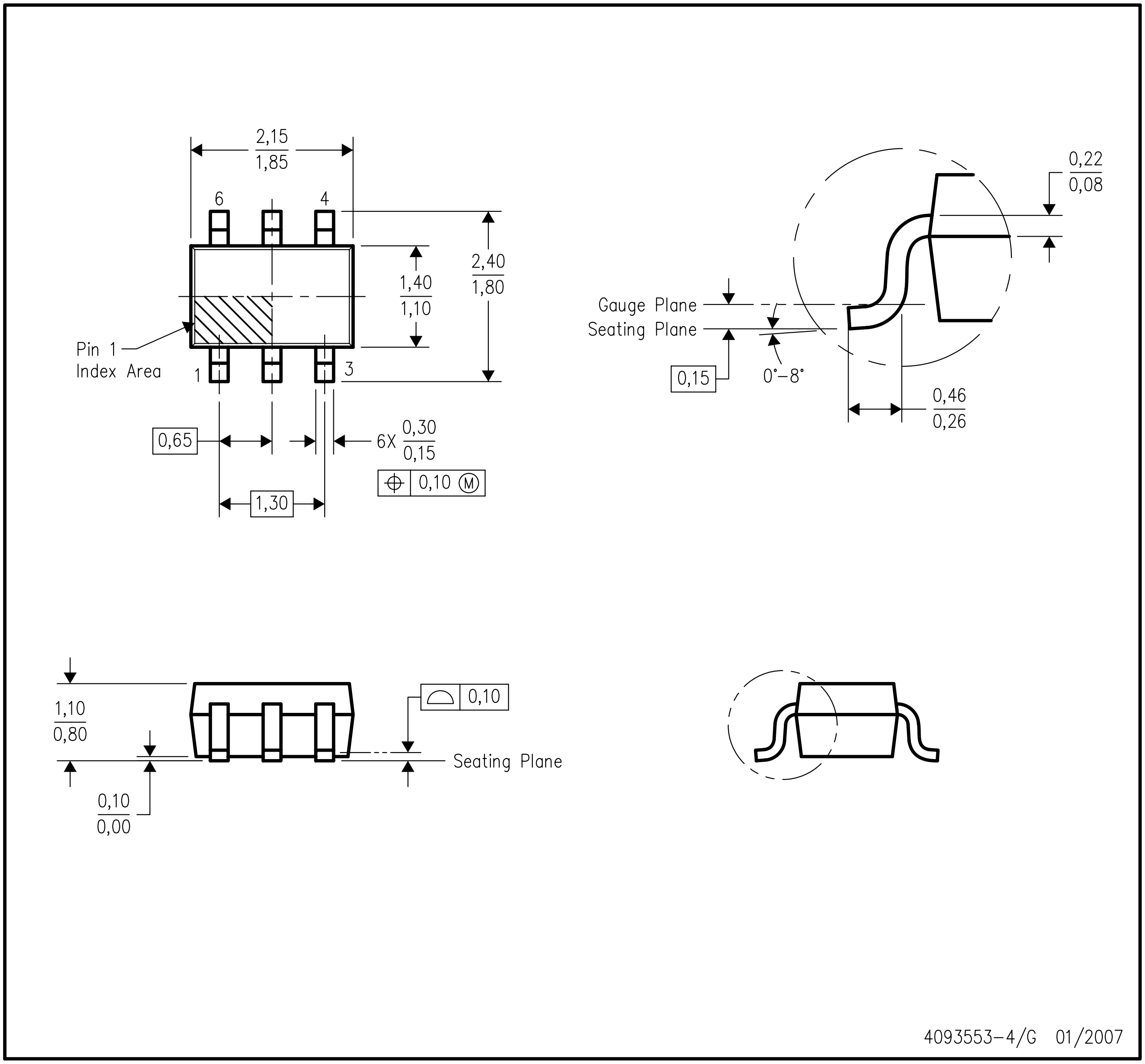
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

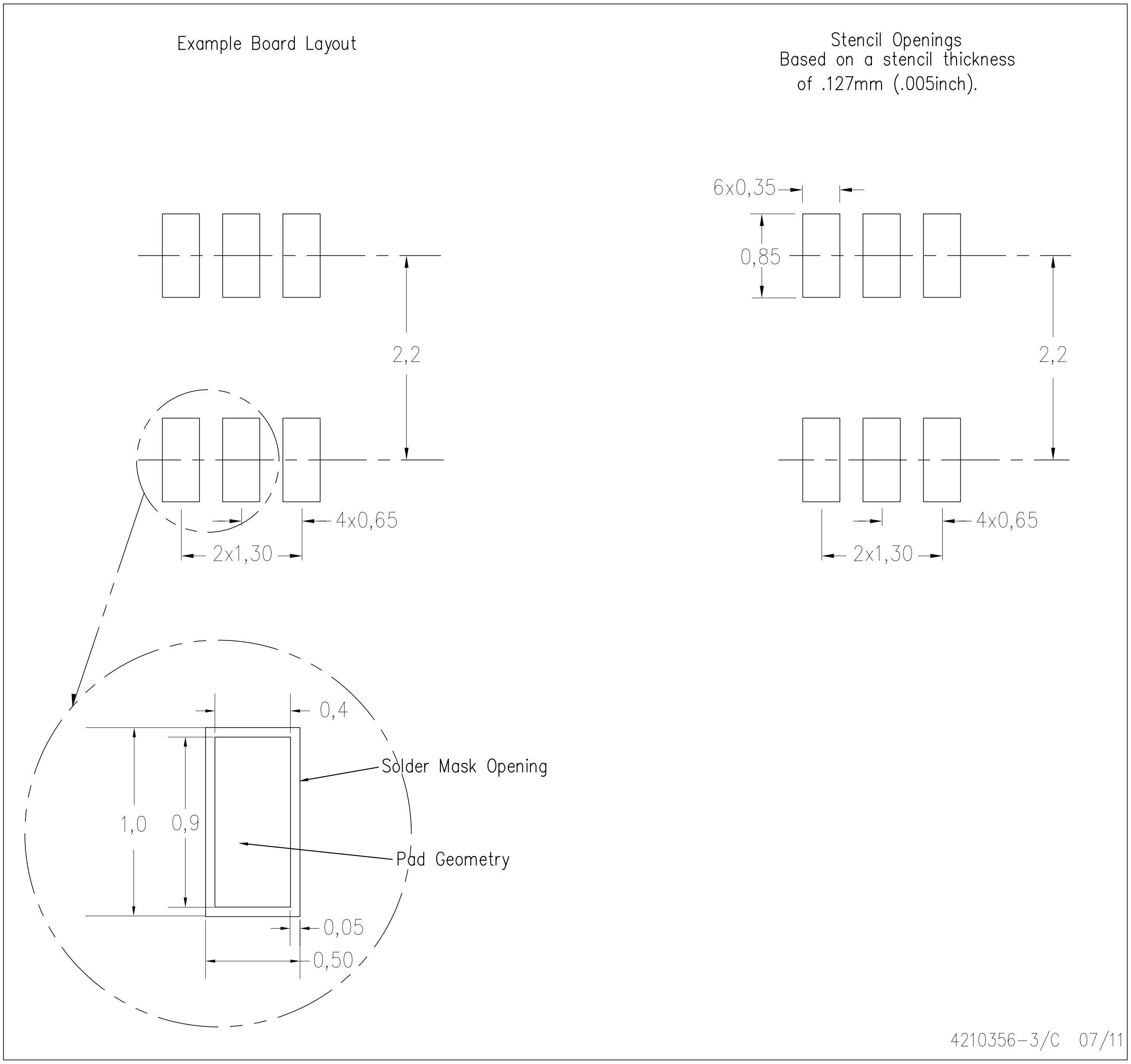
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5311IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
DAC5311IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
DAC6311IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
DAC6311IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
DAC7311IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
DAC7311IDCKT	SC70	DCK	6	250	180.0	180.0	18.0

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.