DAVICOM Semiconductor, Inc.

DM9051A-E1

SPI Fast Ethernet Controller

Proposal

Preliminary
Version: DM9051A_pro_1

February 1, 2024

Modification records:

11/29/2023: first release

12/18/2023: update 3.1a QFN-32 pin-out

02/01/2024: add 4.1.2b MAC register 46H for test chip version ID

1. Features

Based on DM9051, add

- **Bulid-in E-fuse for MAC address**
- **Build-in Bandgap 6.8K ohm resistor**
- **Fiber SD configurable source**
- **Support MAC data encrypt/decrypt mode**
- **Support TX packet buffer continued mode**
- **Bulid-in PTP clocks**
- **Support TimeStamp capture for TX/RX packets**
- **2 GPIO pins for PTP triggers or events**
- **Support TX one-step TimeStamp replacement**

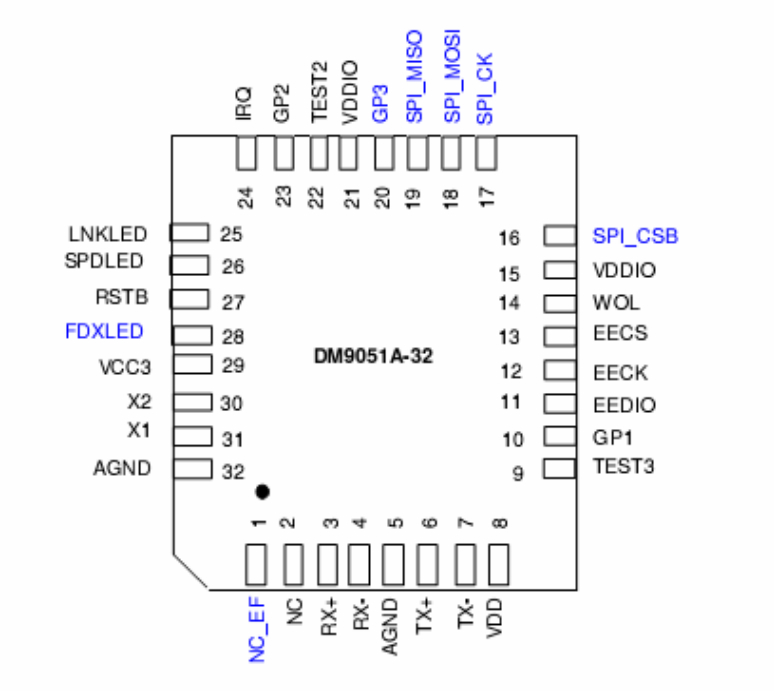
Note:
Process: UMC 0.11um AL
Use DM9111B-E2 analog PHY

2. Block Diagram

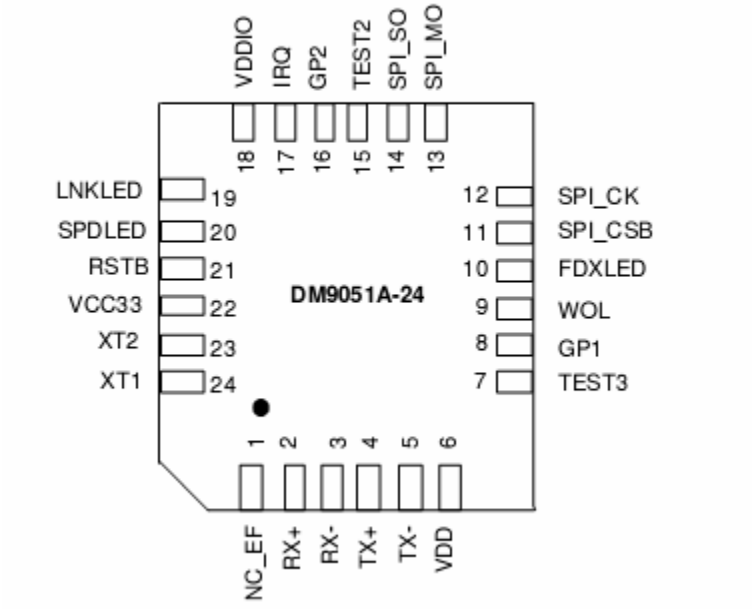
(TBD)

3. Pin Configuration

3.1a QFN-32 pin-out



3.1b QFN-24 pin-out



3.2 Pin Description

Same as DM9051 except:

operation test mode in QFN-32/24:

mode	Pin 9/7 TEST3	Pin 22/15 TEST2
Normal SPI	1 (default)	0 (default)
PHY test mode	0	0
uP-32 test mode	0	1
ATPG test	1	1

4. Control and Status Register Set

Same as DM9051 except following registers

MAC new Register table

Register name	MAC address	Default Value
TX Control Register	02H	00H
Auto-Transmit Control Register	30H	00H
TX Free Space Status Register	3BH	30H
Fiber SD Source Control Register	3CH	00H
Test chip version ID	46H	0CH
E-fuse control Register	58H	00H
PTP Status and GPIO Page Register	60H	00H
PTP Clock Control Registers	61H	00H
PTP GPIO and TX/RX Control Register	62H	00H
PTP One Step Checksum ControlRegister	63H	00H
PTP Receive Configuration 1 Register	64H	00H
PTP One Step Address Offset	65H	4EH
PTP One Step checksum Address Offset	66H	3CH
PTP Clock Period Register	67H	28H
PTP Timestamp Registers	68H	00H
PTP Monitor Register	69H	00H
GPIO Configuration Register	6AH	00H
GPIO Trigger/Event Configuration Register	6BH	00H
GPIO Trigger Asserted Pulse Low Register	6CH	00H
GPIO Trigger Asserted Pulse High Register	6DH	00H
GPIO Trigger Periodic De-asserted Pulse Low Register	6EH	00H
GPIO Trigger Periodic De-asserted Pulse High Register	6FH	00H

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type>
Where:
<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
?H	Bits set to hex. value
X	No default value

P = default value from power on reset
S = default value from software reset
E = default value from EEPROM setting
T = default value from strap pin
<Access Type>:
RO = Read only
RW = Read/Write
R/C = Read and Clear
RW/C1=Read/Write and Cleared by write 1
WO = Write only
R/WC = Read/Write and auto-cleared
Reserved bits should be written with 0.
Reserved bits are undefined on read access.

4.0 Old MAC Registers

4.0.1 TX Control Register (02H)

Bit	Bit Name	Default	Description
7	TX_TS_EN	0,RW	**Transmit TimeStamp Capture when REG_61H PTP_EN=1** 0: disable 1: enable
6	TJDIS	PS0,RW	**Transmit Jabber Timer (2048 bytes) Control or Transmit One Step Enable when REG_61H PTP_EN=1** 1 = Disabled. 0 = Enable
5	EXCECM	PS0,RW	**Excessive Collision Mode Control** 1 = Still tries to transmit this packet 0 = Aborts this packet when excessive collision counts more than 15
4	PAD_DIS2	PS0,RW	**PAD Appends for Packet Index 2** 1 = Disable 0 = Enable
3	CRC_DIS2	PS0,RW	**CRC Appends for Packet Index 2** 1 = Disable 0 = Enable
2	PAD_DIS1	PS0,RW	**PAD Appends for Packet Index 1** 1 = Disable 0 = Enable
1	CRC_DIS1	PS0,RW	**CRC Appends for Packet Index 1** 1 = Disable 0 = Enable
0	TXREQ	PS0,RW	**TX Request. Auto-Clear after Sending Completely** 1 = Transmit in progress 0 = No transmit in progress

4.02 Auto-Transmit Control Register (30H)

Bit	Bit Name	Default	Description
7	AUTO_TX	PS0,RW	**Auto-Transmit Control** 1 = Auto-Transmit enabled. Packet transmitted automatically when end of write TX buffer 0 = Auto-Transmit disabled. When transmit packet, need to set register 2 bit 0 to "1"
6:5	RESERVED	P0,RO	Reserved
4	TX_MODE2	PS0.RW	Transmit Buffer Continued mode Control 1: enable 0: disable
3:2	RESERVED	P0,RO	Reserved
1:0	RESERVED	PS0,RW	Reserved

Note: When in TX_MODE2 enabled, the transmit buffer data address in dword boundary and in sequence write.

TX packet format:

Byte 0/1: TX size low/high byte

Byte 2: TX control: bit 7= TX TimeStamp Capture enable

Bit 6= TX One-Step enable

Bit 5~0=0 reserved

Byte 3: TX Buffer control: 80H= TX buffer data available

Byte 4~TX_END_BYTE: packet payload

4.0.2 RX Status Byte in RX header

Bit	Bit Name	Description
7	RF	**Runt Frame** It is set to indicate that the size of the received frame is smaller than 64 bytes. 1 = Affirmative 0 = Negative
6	MF	**Multicast Frame** It is set to indicate that the received frame has a multicast address. 1 = Affirmative 0 = Negative
5	RXTS_EN	**RX Time Stamp available** 1 = RX timestamp data in RX header begin from byte 4 0 = no RX timestamp available
4	RWTO	**Receive Watchdog Time-Out** It is set to indicate that it receives more than 2048 bytes. 1 = Affirmative 0 = Negative
3	RXTS_PARITY	**RX Time Stamp Odd Parity value**
2	RXTS_LEN	**RX Time Stamp byte length** 1 = 8-byte (4-byte sec + 4-byte nano-sec) 0 = 4-byte (2-bit sec + 4-byte nano-sec)
1	CE	**CRC Error** It is set to indicate that the received frame ends with a CRC error. 1 = Affirmative 0 = Negative
0	FOE	**RX Memory Overflow Error** It is set to indicate that a RX memory overflow error happens during the frame reception. 1 = Affirmative 0 = Negative

Note: RX packet data format in RX memory (0xc00~0x3fff)

RX_header (RX_flag + RX_status + RX_size_low + RX_size_high) 4-byte

RX_timestamp (8-byte if RX_status bit 5 is ‘1’ & bit 2 is ‘1’)

(4-byte if RX_status bit 5 is ‘1’ & bit 2 is ‘0’)

(none if RX_status bit 5 is ‘0’)

RX_data with RX size

4.1 new MAC Registers (besides dm9051)

4.1.1 TX Free Space Status Register (3BH)

Bit	Bit Name	Default	Description
7:0	TX_FREE	PS0,R30H	**TX Free Space in 64-byte unit**

4.1.2 Fiber SD Source Control Register (3CH)

Bit	Name	Default	Description
7:5	RESERVED	P0,RO	reserved
4	GP1_TXC	P0,RW	GP1 pin act as TXC for IEEE 802.3 test reference clock. 0: as normal GP1 , 1: as TXC out
3	SD_POL	P0,RW	Fiber SD Active Low Control 0: active high, 1: active low
2:0	SD_SRC	P0,RW	Fiber SD Source Index 000: from Fiber RX+/- activity 001: from GP1 010: from GP2 011: from GP3 100: from LNKLED 101: from SPDLED 110: from FDXLED 111: reserved

4.1.2b Test Chip Version ID Register (46H)

Bit	Name	Default	Description
7:5	RESERVED	P0,RO	reserved
4:2	VER_ID	PX,RO	Test Chip Version 111: test chip v0 011: test chip v1 110: test chip v2 010: test chip v3.
1:0	RESERVED	P0,RO	reserved

4.1.3 E-fuse Control Register (58H)

Bit	Name	Default	Description
7	EF_EN	P0,RW	E-fuse read/write function enable 1: to enable read or write function from register 0BH command
6:4	RESERVED	P0,RO	reserved
3	EF_WREN	P0,RW	E-fuse write function enable 0: disable, 1: enable
2	RESERVED	P0,RW	reserved
1:0	RESERVED	P0,RO	reserved

Note 1: when write E-fuse command, the REG_1FH bit 0 must be set to "1" (i.e. PHY power-down)

Note2 : MAC ID (in REG_10H~15H) init. Flow:

1. after power-on reset, MAC_ID have random value, except REG_10H=0x00.
2. detect external EEPROM exist or not:
3. If EEPROM present: load EEPROM byte 0~5 to MAC_ID
4. if EEPROM absent: read E-fuse

4.1 if E-fuse byte 0 not equal to 0xff, load bytes 0~5 to MAC_ID

4.2 Else if E-fuse byte 6 not equal to 0xff, load bytes 6~11 to MAC_ID

4.3 Else if E-fuse byte 12 not equal to 0xff and byte 22 bits [1:0] or [3:2] or [5:4] are not equal to "01", load bytes 12~17 to MAC_ID

4.1.4 PTP Status Register (60H)

Bit	Name	Default	Description
7	GP2_ST	P0,RWC 1	GP2 trigger/event status 0: disable or trigger completed 1: trigger active or event ready Write “1” to clear this bit
6	GP2_TYPE	P0,RO	GP2 event type status 0: event 1 is falling edge 1: event 1 is rising edge
5	GP1_ST	P0,RWC 1	GP1 trigger/event status 0: disable or trigger completed 1: trigger active or event ready Write “1” to clear this bit
4	GP1_TYPE	P0,RO	GP1 event type 0: event 0 is falling edge 1: event 0 is rising edge
3:2	RESERVED	P0,RO	reserved
1	GP_PAGE	P0,RW	GPIO Registers in 6AH ~ 6FH 0: for GP1 1: for GP2
0	PTP_RST	P0,RW	PTP Function 0: enable 1: disable

4.1.5 PTP Clock Control Register (61H)

Bit	Name	Default	Description
7	IDX_RST	PS0,RWC	Reset Register 68H Index Write “1” to clear register 68H index. This bit is self-cleared after write
6	RATE_CTL	PS0,RW	PTP Rate Control 0: add 1: subtract
5	PTP_RATE	PS0,RWC	Write PTP Rate Clock The continued value of register 68H will be added/subtract to PTP clock in 2^{-32}ns unit at every system clock This bit is self-cleared after write
4	PTP_ADD	PS0,RWC	Add PTP Clock The continued value of register 68H will be added to PTP clock This bit is self-cleared after write
3	PTP_WRITE	PS0,RWC	Write PTP Clock The continued value of register 68H will be written to PTP clock This bit is self-cleared after write
2	PTP_READ	PS0,RWC	Read PTP Clock The PTP clock will read-out from The continued value of register 68H This bit is self-cleared after write
1	PTP_DIS	PS0,RW	PTP Clock Disable Write “1” to disable PTP clock. Write bit 0 to “1” will clear this bit.
0	PTP_EN	PS0,RW	PTP Clock Enable Write “1” to enable PTP clock. Write bit 1 to “1” will clear this bit.

4.1.6 PTP GPIO and TX/RX Control Register (62H)

Bit	Name	Default	Description
7	INT_MASK	P0,RW	PTP Interrupt Mask 0: Interrupt disabled 1: Interrupt enabled
6	RESERVED	P0,RO	Reserved
5	GP2_TE	P0,RWC	GP2 Trigger Load or Event Read this bit will be cleared automatically after the loading completed For trigger: After set this bit, the TIMER in register 68H will be loaded into trigger timer register. For event: After set this bit, the event timestamp will be loaded into register 68H.
4	GP1_TE	P0,RWC	GP1 Trigger Load or Event Read this bit will be cleared automatically after the loading completed For trigger: After set this bit, the TIMER in register 68H will be loaded into trigger timer register. For event: After set this bit, the event timestamp will be loaded into register 68H.
3:1	RESERVED	P0,RO	Reserved
0	RD_TS	P0,RWC	Read TX Time Stamp Clock The TX timestamp will read-out to register 68H This bit is self-cleared after write

4.1.7 PTP One Step Check Sum Control Register (63H)

Bit	Name	Default	Description
7	CKSM_DIS	P0,RW	TX One Step Check Sum disabled 0: enable to update one step check sum 1: disable
6	RD68_DIS	P0,RW	Read REG_68H in One SPI cycle disabled 0: enable continued read in one SPI cycle 1: disable
5:0	RESERVED	P0,RO	Reserved

4.1.8 PTP Receive Control 1 Register (64H)

Bit	Name	Default	Description
7	RESERVED	P0,RW	Reserved
6:5	RESERVED	P0,RO	Reserved
4	RXTS_EN	PS0,RW	Capture RX Timestamp to RX memory. The 8-byte RX timestamp is saved between RX header and first RX data. 0: disable 1: enable
3:2	RESERVED	P0,RO	Reserved
1:0	RXTS_FLTR	PS0,RW	RX Timestamp Control for DA Filter 00=all packets 01=multicast packets 10=DA byte 0 is 0x01 11=specified DA packets (see note)

Note: specified DA packets are 01:80:C2:00:00:0E, or 01:1B:19:00:00:00, or 01:00:5E:00:01:81

4.1.9 PTP One Step Address Offset (65H)

Bit	Name	Default	Description
7:0	ADR_1STEP	PS4EH, RW	Address offset for TX One-Step When TX one-step option enable, the 8-byte TX TimeStamp will be transmitted start from packet data address of this register

4.1.10 PTP One Step Check Sum Address Offset (66H)

Bit	Name	Default	Description
7:0	ADR_1CKSM	PS3CH, RW	Address offset for TX One-Step Check Sum When TX one-step check sum option not disabled, the 2-byte TX TimeStamp check sum will be transmitted start from packet data address of this register

4.1.11 PTP Clock Period (67H)

Bit	Name	Default	Description
7:0	CLK_WIDTH	PS28H, RW	PTP Clock Period The PTP clock is same as system clock.

4.1.12 PTP Timestamp Registers (68H)

The index number will be increased after write or read this register.
The all PTP Timestamp can be read in one SPI cycle.

4.1.12.1 PTP Timestamp Nanosecond 0 Registers (68H)- index 0

Bit	Name	Default	Description
7:0	TNS_0	PS0,RW	Timestamp nanosecond[07:00]

4.1.12.2 PTP Timestamp Nanosecond 1 Registers (68H)- index 1

Bit	Name	Default	Description
7:0	TNS_1	PS0,RW	Timestamp nanosecond[15:08]

4.1.12.3 PTP Timestamp Nanosecond 2 Registers (68H)- index 2

Bit	Name	Default	Description
7:0	TNS_2	PS0,RW	Timestamp nanosecond[23:16]

4.1.12.4 PTP Timestamp Nanosecond 3 Registers (68H)- index 3

Bit	Name	Default	Description
7:0	TNS_3	PS0,RW	Timestamp nanosecond[31:24]

4.1.12.5 PTP Timestamp Second 0 Registers (68H)- index 4

Bit	Name	Default	Description
7:0	TS_0	PS0,RW	Timestamp second[07:00]

4.1.12.6 PTP Timestamp Second 1 Registers (68H)- index 5

Bit	Name	Default	Description
7:0	TS_1	PS0,RW	Timestamp second[15:08]

4.1.12.7 PTP Timestamp Second 2 Registers (68H)- index 6

Bit	Name	Default	Description
7:0	TS_2	PS0,RW	Timestamp second[23:16]

4.1.12.8 PTP Timestamp Second 3 Registers (68H)- index 7

Bit	Name	Default	Description
15:0	TS_3	PS0,RW	Timestamp second[31:24]

4.1.12b PTP Monitor Register (69H)

Bit	Name	Default	Description
7:4	IDX_68H	P0,RO	Index of REG_68H
3:1	RESERVED	P0,RO	Reserved
0	RD_RATE	P0,RW	Read Clock Rate Value The PTP clock rate will read-out from the continued 5 bytes value of register 68H Byte 1~4 are the clock rate value Byte 5: 0=positive rate, 1=negative rate

4.1.13 GPIO Control Register (6AH)

Bit	Name	Default	Description
7	GP_ST	P0,RWC 1	GP2 trigger/event status 0: disable or trigger completed 1: trigger active or event ready Write "1" to clear this bit
6	GP_TYPE	P0,RO	GP2 event type status 0: event 1 is falling edge 1: event 1 is rising edge
5:3	RESERVED	P0,RO	Reserved
2	GP_INTEN	P0,RW	GPIO Interrupt Control 0: GPIO interrupt disable 1: GPIO interrupt enable
1	TRIG_EN	P0,RW	GPIO Trigger/Event Enable Control 0: trigger and event disabled 1: trigger or event enabled
0	GP_TYPE	P0,RW	GPIO type 0: trigger output mode 1: event input mode

4.1.14 GPIO Trigger/Event Control Register (6BH)

Bit	Name	Default	Description
7	RESERVED	P0,RO	Reserved
6	EVENT_LCK	P0,RW	GPIO Event Timestamp Lock Disable 0: lock first event, 1: can overwrite,
5	GP_R_EVT	P0,RW	GPIO Event Rise Detect 0: no detect rising edge event 1: detect rising edge event
4	GP_F_EVT	P0,RW	GPIO Event Fall Detect 0: no detect falling edge event 1: detect falling edge event
3:2	TRIG_TYPE	P0,RW	Trigger Output Type 00: edge output, 01: edge toggle 10: single pulse, 11: periodic pulse

1	TRIG_POR	P0,RW	GPIO Trigger Polarity Control 0: GPIO trigger output active low 1: GPIO trigger output active high
0	RESERVED	P0,RO	Reserved

4.1.15 GPIO Trigger Asserted Pulse Low Register (6CH)

Bit	Name	Default	Description
7:0	PULSE1_LO	P0,RW	Pulse Width or Periodic Pulse Asserted Period [7:0]

4.1.16 GPIO Trigger Asserted Pulse High Register (6DH)

Bit	Name	Default	Description
7:6	PULSE1_U	P0,RW	Pulse Width or Periodic Pulse Asserted Period Unit 00: 120ns 01: 1us 10: 1ms 11: 1us
5:0	PULSE1_HI	P0,RW	Pulse Width or Periodic Pulse Asserted Period [13:8]

4.1.17 GPIO Trigger Periodic De-asserted Pulse Low Register (6EH)

Bit	Name	Default	Description
7:0	PULSE2_LO	P0,RW	Periodic Pulse Deasserted Period [7:0]

4.1.18 GPIO Trigger Periodic De-asserted Pulse High Register (6FH)

Bit	Name	Default	Description
7:6	PULSE2_U	P0,RW	Periodic Pulse De-asserted Period Unit 00: 120ns 01: 1us 10: 1ms 11: 1us
5:0	PULSE2_HI	P0,RW	Periodic Pulse De-asserted Period [13:8]

4.2 PHY register

4.2.1 DSP Control Register (DSPCR) – 27 (1BH)

Bit	Bit Name	Default	Description
15:12	FIL_CTL	0,RW	FILTER Write Control The FILTER can be written only when these three bits equal to 1111.
11	RESERVED	0,RW	reserved
10	CABLE_LEN	0,RW	Cable length control/status 0: short cable (< 50m) 1: long cable (> 50m)
9:8	FILTER	00.RW	Equalizer Filter Control parameter
7:0	RESERVED	0,RW	reserved

4.2.2 Regulator Control Register (RGCR) – 28 (1CH)

Bit	Bit Name	Default	Description
15:4	RESERVED	0,RW	reserved
3:2	REG_CTL	0.RW	1.2V Regulator Control 00: 1.2V (default) 01: 1.15V 10: 1.1V 11: 1.05V
1:0	RESERVED	0,RW	reserved

4.3 E-fuse Format

Name	Byte	Description
MAC ID SET 1	0~5	6 Byte Ethernet Address Set 1
MAC ID SET 2	6~11	6 Byte Ethernet Address Set 2
MAC ID SET 3	12~17	6 Byte Ethernet Address Set 3 Valid if byte 22[5:4] and [3:2] and [1:0] are all not equal to “01”
Vendor ID_LO	12	vendor ID low byte
Vendor ID_HI	13	vendor ID high byte
Product ID_LO	14	product ID low byte
Product ID_HI	15	product ID high byte
SPI Pin control	16	When byte 22 bit [3:2]=01, these bits can be controlled. Bit 4~0: Reserved, set to 0 in application Bit 5: Eliminate SPI_CSB high spike control This bit will be load into register 38H bit 2 Bit 7~6: SPI_MISO driving capability This bit will be load into register 38H bit [6:5]
Wake-up mode control	17	When byte 22 bit [5:4]=01, these bits can be controlled. Bit 0: The WOL pin is active low when set Bit 1: The WOL pin is in pulse mode when set Bit 2: Magic wakeup event is enabled when set. Bit 3: Link change wakeup event is enabled when set Bit 6~4: Reserved; set to 0 in application Bit 7 = LED mode 0, 1=LED mode 1
TRIM_RES	18	Trim Value of internal 50Ohm Resistor Bit 7~6 = 01: Accept setting of byte 18 [5:0] as trim data PHY 50Ohm
CODE1	19	Encryption/decryption code 1 Valid if not equal to 0xFF
CODE2	20	Encryption/decryption code 2 Valid if not equal to 0xFF and CODE1 is not valid.
CODE3	21	Encryption/decryption code 3 Valid if not equal to 0xFF and CODE1/2 are not valid.
Auto Load Control	22	When EEPROM is not exist, Bit 1:0 = 01: Update vendor ID and product ID from byte 12~15. Bit 3:2 = 01: Accept setting of byte 16 [7:5] Bit 5:4 = 01: Accept setting of byte 17 [7,3:0] Bit 7:6 = 01: Accept setting of byte 23 [4:0]
PHY/IRQ Control	23	When byte 22 bit [7:6]=01, these bits can be controlled. Bit 0: 1 = Internal PHY is enabled after power-on Bit 1: PHY Fiber Mode Control; 1= Fiber mode, 0: TP mode Bit 2: PHY enable 802.3az, to register 3FH bit [7] Bit 3: IRQ pin is active low when set Bit 4: IRQ pin is open-collected

Note: byte 0~17, and 22~23 valid only if no EEPROM exist.