DAVICOM Semiconductor, Inc.

DM9051A(I)N

SPI Fast Ethernet Controller

DATA SHEET

Version: DM9051A(I)N-11-MCO-DS-P01

January 8, 2025

Content

1 General Description

The DM9051A(I)N is a fully integrated and cost-effective low pin count single chip Fast Ethernet controller with SPI, a 10/100M PHY and 4K Dword SRAM. It is designed for low power consumption and high performance, featuring the SPI with 1.8~3.3V I/O.

The DM9051A(I)N supports SPI to internal memory accesses for various processors. The PHY of the DM9051A(I)N can interface to the UTP3, 4, 5 in 10Base-T and UTP5 in 100Base-TX with HP Auto-MDIX. It is fully compliant with the IEEE 802.3u Spec. Its auto-negotiation function will automatically configure the DM9051A(I)N to take advantage of its capabilities. The DM9051A(I)N also supports IEEE 802.3x full-duplex flow control.

The DM9051A(I)N supports IEEE 802.3az in PHY and MAC to save power consumption when Ethernet is idle. The IEEE 802.3x Full-Duplex flow control and Half-Duplex back-pressure function also supported to avoid Ethernet packet loss with link partner.

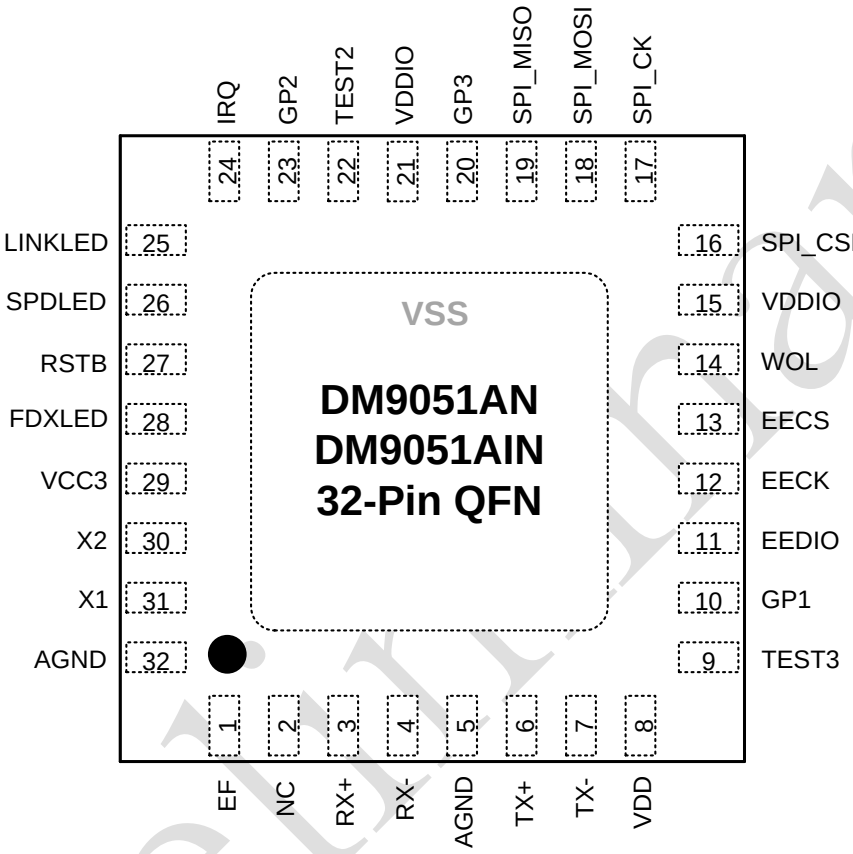
The slave SPI interface is designed to support SPI clock mode 0 and 3 that compatible with the all master SPI interface of CPU. The clock speed can up to 50Mhz to co-work with most high throughput master SPI. The SPI burst command format is code-effective to minimize the command overhead in access DM9051A(I)N internal registers and packet data in memory.

2 Features

- Slave SPI with clock speeds up to 50MHz for high throughput applications
- Supports SPI clock mode 0 and 3
- Supports 10BASE-T and 100BASE-TX
- Supports 100M Fiber interface and multiple Fiber mode signal detection
- Supports HP Auto-MDIX crossover function in 10BASE-T and 100BASE-TX
- Supports IEEE 802.3az Energy Efficient Ethernet (EEE)
- Supports back pressure flow control for Half-Duplex mode
- Supports IEEE802.3x flow control for Full-Duplex mode
- Supports wake up frame, link status change and magic packet events to generate remote wake on LAN (WOL) signal
- Supports IPv4 IP/TCP/UDP checksum generation and checking
- Supports application for IPv6 IP/TCP/UDP protocol stack
- Configurable of internal transmit/receive buffers within 16K-Byte memory
- Built-in OTP memory suitable for MAC address
- Eliminates the need of bandgap resistor
- Supports printed circuit board level of data security
- Built-in integrated regulator for internal core use
- Reaches Class B EMI standard
- Industrial Temperature Range: －40℃ to +85℃
- Multi-Voltage I/O VDDIO Supply (1.8V, 2.5V, 3.3V)

3 Pin Configuration

3.1 32-Pin QFN



Note: The DM9051A(I)N IC employs a QFN package, which means the absence of a pin dedicated to ground (GND). In the QFN package, the GND is located at the bottom of the IC directly in the middle. Exposed pad (VSS) on bottom of package must be connected to ground.

4 Pin Description

Buffer Type			
I = Input	O = Output	I/O = Input/Output	P = Power
O/D = Open Drain		PD = Internal Pull-low about 60K	PU = Internal Pull-high about 60K

4.1 SPI Processor Interface

Pin No.	Pin Name	Type	Description
16	SPI_CSB	I,PU	**SPI Chip Select** The low active chip select pin from master SPI.
17	SPI_CK	I,PD	**SPI Clock** The SPI clock mode 0 or 3 from master SPI.
18	SPI_MOSI	I	**SPI Data In** The data pin from master SPI.
19	SPI_MISO	O,PD	**SPI Data Out** The data pin to master SPI.
24	IRQ	O,PD	**Interrupt Request** This pin is high active at default.

4.2 Clock Interface

Pin No.	Pin Name	Type	Description
30	X2	O	Crystal 25MHz Out
31	X1	I	Crystal 25MHz In

4.3 LED Interface

Pin No.	Pin Name	Type	Description
28	FDXLED	O/D	**Full-Duplex LED** In LED mode 1, its low output indicates that the internal PHY is operated in Full-Duplex mode, or it is floating for the Half-Duplex mode of the internal PHY. In LED mode 0, its low output indicates that the internal PHY is operated in 10M mode, or it is floating for the 100M mode of the internal PHY. More LED modes are controlled by MAC register 57H
25	LINKLED	O/D	**Link / Active LED** In LED mode 1, it is the combined LED of link and carrier sense signal of the internal PHY. In LED mode 0, it is the LED of the carrier sense signal of the internal PHY only. More LED modes are controlled by MAC register 57H.
26	SPDLED	O/D	**Speed LED** Its low output indicates that the internal PHY is operated in 100M/S, or it is floating for the 10M mode of the internal PHY. More LED modes are controlled by MAC register 57H.

Note: LED mode 0 or 1 is defined in MAC register 2DH.

4.4 10/100 PHY/Fiber

Pin No.	Pin Name	Type	Description
1	EF	I/O	Reserved Connection, Leave it open
8	VDD	P	Internal Voltage, Connect to 0.1uF Cap.
3,4	RX+/ RX-	I/O	**RX+/-** The RX input in 10BASE-T/100BASE-TX MDI mode or TX output in 10BASE-T/100BASE-TX MDIX mode. In 100M Fiber mode, these pins are for RX input only.
6,7	TX+/ TX-	I/O	**TX+/-** The TX output in 10BASE-T/100BASE-TX MDI mode or RX input in 10BASE-T/100BASE-TX MDIX mode. In 100M Fiber mode, these pins are for TX output only.

4.5 Miscellaneous

Pin No.	Pin Name	Type	Description
9	TEST3	I,PD	**Operation Mode** Force to high in normal application
10	GP1	I/O	**General Purpose Pin 1** This is a general purpose pin controlled by bit 1 of MAC register 1EH/1FH.
14	WOL	O,PD	**Wake On LAN** This is a control signal when wake up event occurred.
20	GP3	I/O,PD	**General Purpose Pin 3** This is a general purpose pin controlled by bit 3 of MAC register 1EH/1FH.
22	TEST2	I,PD	**Operation Mode** Force to ground in normal application
23	GP2	I/O	**General Purpose Pin 2** This is a general purpose pin controlled by bit 2 of MAC register 1EH/1FH.
27	RSTB	I	**Power on Reset** Active low signal to initiate the DM9051A(I)N. The DM9051A(I)N is ready after 5us when this pin disserted.
2	NC	-	Not Connected

4.6 Power Pins

Pin No.	Pin Name	Type	Description
15,21	VDDIO	P	**Voltage Source for IO pins** 3.3V,2.5V,1.8V power input
29	VCC3	P	**VCC** 3.3V power input
5,32	AGND	P	Analog Ground
33	VSS	P	The QFN package ground

4.7 EEPROM Interface

Pin No.	Pin Name	Type	Description
11	EEDIO	I/O,PD	**EEPROM IO Data** The IO data pin to or from EEPROM.
12	EECK	O,PD	**EEPROM Clock** The clock pin to EEPROM. This pin is also used as the strap pin of the polarity of the IRQ pin. When this pin is pulled-high, the IRQ pin is low active; otherwise the IRQ pin is high active.
13	EECS	O,PD	**EEPROM Chip Select** The high active chip select to EEPROM.

4.8 Strap Pins

Pin No.	Pin Name	Description
12	EECK	**Polarity of IRQ** 1 = IRQ pin low active 0 = IRQ pin high active
13	EECS	**BIST Control** 1 = Enable BIST 0 = Disable BIST
14	WOL	**IRQ Output Type** 1 = Open-Drain 0 = Push-pull mode

5 Functional Description

5.1 SPI Processor Interface

The DM9051A(I)N supports a slave mode SPI interface. In this mode, an external SPI master device (from micro-controller or CPU) supplies the operating serial clock (SPI_CK), chip select (SPI_CSN), and serial input data (SPI_MOSI). A Serial output data (SPI_MISO) is driven from DM9051A(I)N. SPI_MOSI is the output on SPI_CK falling edge of SPI master device, sampled by DM9051A(I)N on SPI_CK rising edge. SPI_MISO is driven from DM9051A(I)N on SPI_CK falling edge and sampled on SPI_CK rising edge by SPI master device. The falling edge of SPI_CSN starts the SPI burst operation and the rising edge of SPI_CSN stops the SPI burst operation. The SPI_CK stays in low state at SPI mode 0 or stays in high state at SPI mode 3 when SPI burst operation is idle (the SPI_CSN in high state).

5.2 Direct Memory Access Control

The DM9051A(I)N provides DMA capability to simplify the access of the internal memory. After the programming of the starting address of the internal memory and then issuing a dummy read/write command to load the current data to internal data buffer, the desired location of the internal memory can be accessed by the read/write command registers. The memory's address will be increased with one byte and the data of the next location will be loaded into internal data buffer automatically. It is noted that the data of the first access (the dummy read/write command) in a sequential burst should be ignored because that the data was the contents of the last read/write command.

The internal memory size is 16K bytes. The first location of 3K bytes is used for the data buffer of the packet transmission. The other 13K bytes are used for the buffer of the receiving packets. So in the write memory operation, when the bit 7 of IMR is set, the memory address increment will wrap to location 0 if the end of address (i.e. 3K) is reached. In a similar way, in the read memory operation, when the bit 7 of IMR is set, the memory address increment will wrap to location 0C00H if the end of address (i.e. 16K) is reached.

5.3 Packet Transmission

There are two packets, sequentially named as index I and index II, can be stored in the TX SRAM at the same time. The index MAC register 02H controls the insertion of CRC and pads. Their statuses are recorded at index MAC registers 03H and 04H respectively.

The start address of transmission is 00h and the current packet is index I after software or power-on reset. Firstly write data to the TX memory using the DMA port MAC register 78H and then write the byte count to TX packet length register at MAC register 7CH and 7DH. Set the bit 1 of transmit control register MAC 02H or by Auto-Transmit command burst, the DM9051A(I)N starts to transmit the index I packet. Before the transmission of the index I packet ends, the data of the next (index II) packet can be write into TX memory and transmit it. After the index I/II packet ends the transmission, the status MAC register 01H bit 3 and 4 will be set to indicate the next index I or II packet can be transmitted.

5.4 Packet Reception

The RX memory is a ring data structure. The start address of RX memory is default 0C00H after software or power-on reset or by set MAC register 55H bit 0. Each packet content format is a 4-byte status header followed with the data of the reception packet which CRC field is included. The format of the 4-byte status header is flag byte, RX status, low byte of RX size, and high byte of RX size respectively. The flag byte is 01h or is RX checksum status if register 32H bit 1 is set.

5.5 100Base –TX Operation

The transmitter section contains the following functional blocks:
- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Encoder
- NRZI to MLT-3
- MLT-3 Driver

5.5.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC reconciliation layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC reconciliation layer, the 4B5B encoder injects the T/R code group pair (01101 00111) indicating end-of-frame. After the T/R code group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

The DM9051A(I)N includes a Bypass 4B5B conversion option within the 100Base-TX Transmitter for support of applications like 100 Mbps repeaters, which do not require 4B5B conversion.

5.5.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to repeated 5B sequences like continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

5.5.3 Parallel to Serial Converter

The parallel to serial converter receives parallel 5B scrambled data from the scrambler and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block.

5.5.4 NRZ to NRZI Encoder

Since the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable.

5.5.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output from the NRZI encoder into two binary data streams with alternately phased logic one event.

5.5.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

5.5.7 4B5B Code Group

Table 1

Symbol	Meaning	4B Code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	Undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	Undefined	01101
R	ESD (2)	Undefined	00111
H	Error	Undefined	00100
V	Invalid	Undefined	00000
V	Invalid	Undefined	00001
V	Invalid	Undefined	00010
V	Invalid	Undefined	00011
V	Invalid	Undefined	00101
V	Invalid	Undefined	00110
V	Invalid	Undefined	01000
V	Invalid	Undefined	01100
V	Invalid	Undefined	10000
V	Invalid	Undefined	11001

5.6 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.

The receive section contains the following functional blocks:
- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

5.6.1 Signal Detect

The signal detects function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

5.6.2 Adaptive Equalization

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

5.6.3 MLT-3 to NRZI Decoder

The DM9051A(I)N decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

5.6.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the
NRZI to NRZ decoder.

5.6.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to parallel conversion block.

5.6.6 Serial to Parallel

The serial to parallel converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

5.6.7 Descrambler

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the serial to parallel converter, and it descrambles the data streams, and presents the data streams to the code GGoup alignment block.

5.6.8 Code Group Alignment

The code group alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code group alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

5.6.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols).

The T/R symbol pair is also stripped from the nibble, presented to the reconciliation layer.

5.7 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM9051A(I)N is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

5.8 Collision Detection

For Half-Duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in Full-Duplex operation.

5.9 Carrier Sense

Carrier Sense (CRS) in internal MII is asserted in Half-Duplex operation during transmission or reception of data. During Full-Duplex mode, CRS is asserted only during receive operations.

5.10 Auto-Negotiation

The objective of Auto-Negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-Negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Auto-Negotiation also provides a parallel detection function for devices that do not support the Auto-Negotiation feature. During parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-Negotiation but support a common mode of operation to establish a link.

5.11 Power Reduced Mode

The signal detect circuit is always turned to monitor whether there is any signal on the media (cable disconnected).

The DM9051A(I)N automatically turns off the power and enters the Power Reduced mode, whether its operation mode is N-way or force mode. When enters the Power Reduced mode, the transmit circuit still sends out fast link pulse with minimum power consumption. If a valid signal is detected from the media, which might be N-ways fast link pulse, 10Base-T normal link pulse, or 100Base-TX MLT3 signals, the device will wake up and resume a normal operation mode.

That can be writing zero to PHY register 16 bit 4 to disable Power Reduced mode.

5.11.1 Power Down Mode

The PHY register 0 bit 11 can be set high to enter the power down mode, which disables all transmit and receive functions, except the access of PHY registers

6 DC Characteristics

6.1 Absolute Maximum Ratings (25°C) (DM9051AI support -40°C~+85°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VCC3	Supply Voltage	-0.3	3.6	V	Power pin
VIN	DC Input Voltage (VIN)	-0.5	3.6	V	IO pin
VOUT	DC Output Voltage(VOUT)	-0.3	3.6	V	IO pin
Tstg	Storage Temperature Range	-65	+150	℃	
TA	Ambient Temperature	0	+70	℃	DM9051AN
TA	Ambient Temperature	-40	+85	℃	DM9051AIN
LT	Lead Temperature (TL,soldering,10 sec.).	—	+260	℃	

6.1.1 Operating Conditions(VDDIO = 3.3V, ±5%)

Symbol	Parameter	Min.	Typ. VCC3/VDDIO	Max.	Unit	Conditions
PD (Power Dissipation)	100BASE-TX		50 / 1.2		mA	3.3V / 3.3V
	100BASE-TX (802.3az)		45.4 / 1.2		mA	3.3V / 3.3V
	10BASE-T TX		32.5 / 1.0		mA	3.3V / 3.3V
	Auto-Negotiation		22 / 0.6		mA	3.3V / 3.3V
	Power Down Mode		4.6 / 0.6		mA	3.3V / 3.3V

6.1.2 Operating Conditions(VDDIO = 2.5V, ±5%)

Symbol	Parameter	Min.	Typ. VCC3/VDDIO	Max.	Unit	Conditions
PD (Power Dissipation)	100BASE-TX		50 / 0.6		mA	3.3V / 2.5V
	100BASE-TX (802.3az)		45.4 / 0.6		mA	3.3V / 2.5V
	10BASE-T TX		32.5 / 0.4		mA	3.3V / 2.5V
	Auto-Negotiation		22 / 0.37		mA	3.3V / 2.5V
	Power Down Mode		4.3 / 0.3		mA	3.3V / 2.5V

6.1.3 Operating Conditions(VDDIO = 1.8V, ±5%)

Symbol	Parameter	Min.	Typ. VCC3/VDDIO	Max.	Unit	Conditions
PD (Power Dissipation)	100BASE-TX		50 / 0.1		mA	3.3V / 1.8V
	100BASE-TX (802.3az)		45.4 / 0.1		mA	3.3V / 1.8V
	10BASE-T TX		32.5 / 0.2		mA	3.3V / 1.8V
	Auto-Negotiation		22 / 0.1		mA	3.3V / 1.8V
	Power Down Mode		4.3 / 0.1		mA	3.3V / 1.8V

6.2 DC Electrical Characteristics

6.2.1 DC Electrical Characteristics (VDDIO = 3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
V_{IL}	Input Low Voltage	-	-	0.8	V	
V_{IH}	Input High Voltage	2.0	-	-	V	
I_{IL}	Input Low Leakage Current	-10	-	10	uA	Input Voltage = 0.0V
I_{IH}	Input High Leakage Current	-10	-	10	uA	Input Voltage = 3.3V
Outputs						
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -4mA

6.2.2 DC Electrical Characteristics (VDDIO = 2.5V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
V_{IL}	Input Low Voltage	-	-	0.7	V	
V_{IH}	Input High Voltage	1.7	-	-	V	
I_{IL}	Input Low Leakage Current	-10	-	10	uA	Input Voltage = 0.0V
I_{IH}	Input High Leakage Current	-10	-	10	uA	Input Voltage = 2.5V
Outputs						
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	1.85	-	-	V	I_{OH} = 4mA

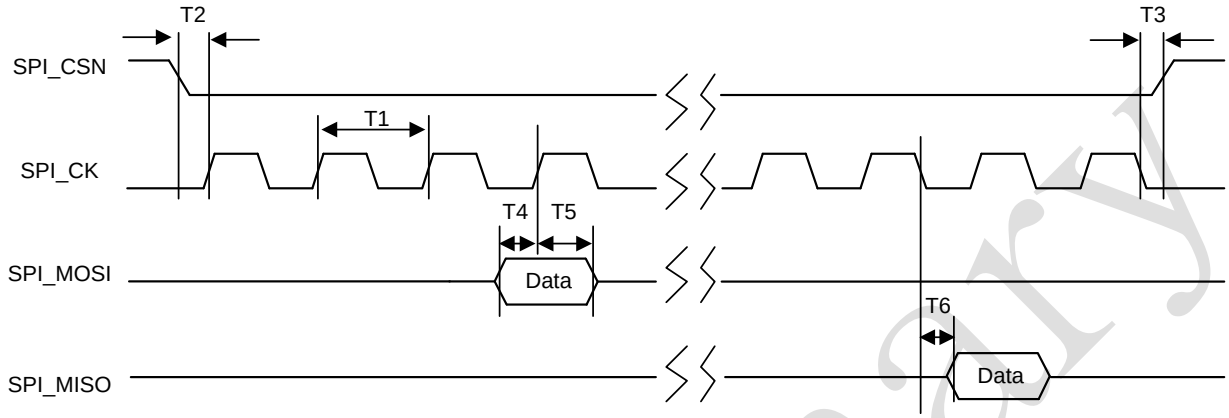
6.2.3 DC Electrical Characteristics (VDDIO = 1.8V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
V_{IL}	Input Low Voltage	-	-	0.6	V	
V_{IH}	Input High Voltage	1.2	-	-	V	
I_{IL}	Input Low Leakage Current	-10	-	10	uA	Input Voltage = 0.0V
I_{IH}	Input High Leakage Current	-10	-	10	uA	Input Voltage = 1.8V
Outputs						
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	1.42	-	-	V	I_{OH} = 4mA

7 AC Electrical Characteristics & Timing Waveforms

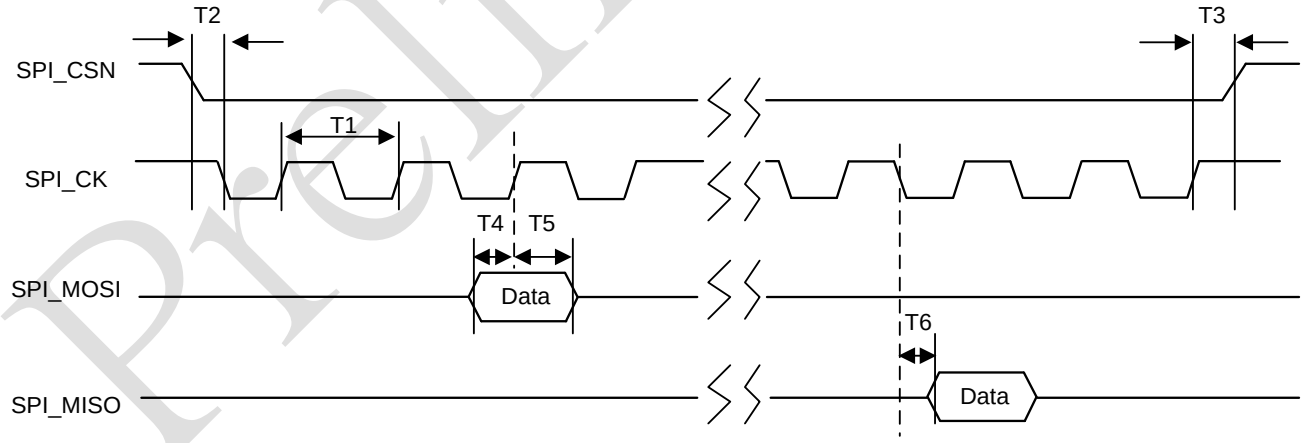
7.1 SPI Timing

M0 Mode



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	SPI_CK Frequency	-	40	50	MHz
T2	SPI_CSN go low to SPI_CK go high	10	-	-	ns
T3	SPI_CK go low to SPI_CSN go high	10	-	-	ns
T4	SPI_MOSI setup time from SPI_CK go high	3	-	-	ns
T5	SPI_MOSI hold time after SPI_CK go high	3	-	-	ns
T6	SPI_MISO Output Delay after SPI_CK go low	5	6	7	ns

M3 Mode



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	SPI_CK Frequency	-	40	50	MHz
T2	SPI_CSN go low to SPI_CK go low	0	-	-	ns
T3	SPI_CK go high to SPI_CSN go high	0	-	-	ns
T4	SPI_MOSI setup time from SPI_CK go high	3	-	-	ns
T5	SPI_MOSI hold time after SPI_CK go high	3	-	-	ns
T6	SPI_MISO output delay after SPI_CK go low	5	6	7	ns

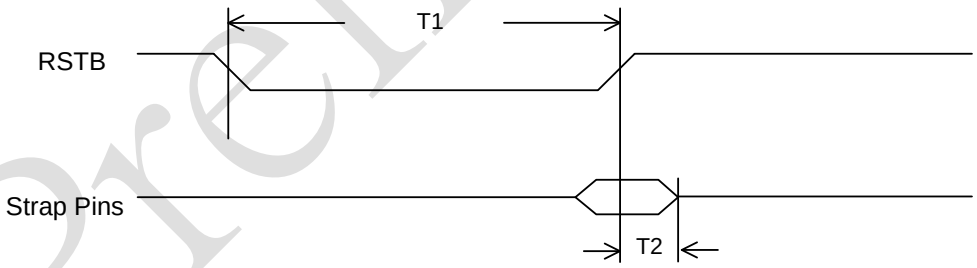
7.2 TP Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{TR/F}$	100TX+/- Differential Rise/Fall Time	3.0	-	5.0	ns	-
t_{TM}	100TX+/- Differential Rise/Fall Time Mismatch	0	-	0.5	ns	-
t_{TDC}	100TX+/- Differential Output Duty Cycle Distortion	0	-	0.5	ns	-
$T_{t/T}$	100TX+/- Differential Output Peak-to-Peak Jitter	0	-	1.4	ns	-
X_{OST}	100TX+/- Differential Voltage Overshoot	0	-	5	%	-
Receiver						
V_{ICM}	RX+/RX- Common Mode Input Voltage	-	TBD	-	V	100 Ω Termination Across
Transmitter						
V_{TD100}	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
V_{TD10}	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak

7.3 Oscillator/Crystal Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T_{CKC}	OSC Clock Cycle	39.9988	40	40.0012	ns	30ppm
T_{PWH}	OSC Pulse Width High	16	20	24	ns	-
T_{PWL}	OSC Pulse Width Low	16	20	24	ns	-

7.4 Power On Reset Timing



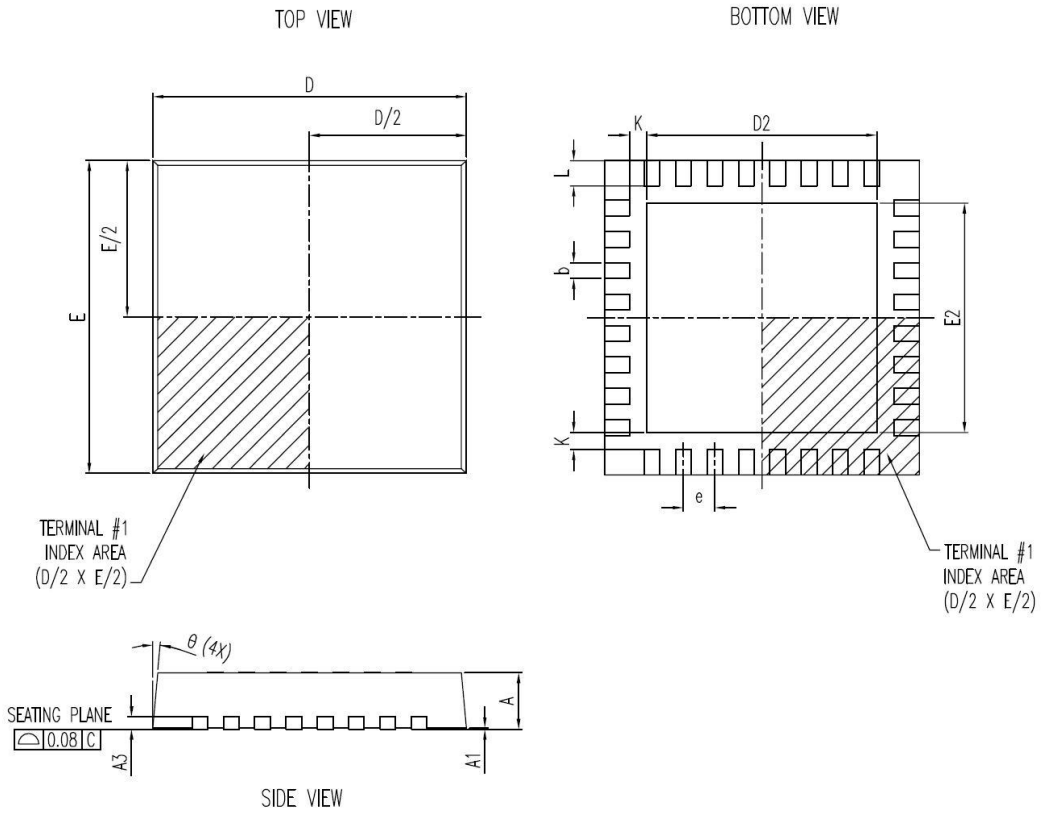
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	RSTB Low Period	1	-	-	ms	-
T2	Strap Pins hold time with RSTB	40	-		ns	-

7.5 LED (traffic ON/OFF timing) any LED as Traffic

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	LED Traffic ON Time	-	16	-	ms
T2	LED Traffic OFF Time	64	-	-	ms

8 Package Information

8.1 32-Pin QFN



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF.	
D		5.00 BASIC	
D2	3.50	3.65	3.80
E		5.00 BASIC	
E2	3.50	3.65	3.80
e		0.50 BASIC	
b	0.18	0.25	0.30
L	0.35	0.40	0.45
K	0.20		
θ	0°		14°
JEDEC	MO-220 (Variation VHHD-4)		

9 Ordering Information

Part Number	Description
DM9051AIN	32 PIN, QFN Package (Pb-Free), Industrial grade -40℃ to +85℃
DM9051AN	32 PIN, QFN Package (Pb-Free), Commercial grade 0℃ to +70℃

Disclaimer

The information appearing in this publication is believed to be accurate. Integrated circuits sold by DAVICOM Semiconductor are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. DAVICOM makes no warranty, express, statutory, implied or by description regarding the information in this publication or regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, DAVICOM MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. DAVICOM reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by DAVICOM for such applications.

Please note that application circuits illustrated in this document are for reference purposes only.

DAVICOM's terms and conditions printed on the order acknowledgment govern all sales by DAVICOM. DAVICOM will not be bound by any terms inconsistent with these unless DAVICOM agrees otherwise in writing. Acceptance of the buyer's orders shall be based on these terms.

Company Overview

DAVICOM Semiconductor Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

Contact Windows

For additional information about DAVICOM products, contact the Sales department at:

Headquarters

Hsin-chu Office:
No.6, Li-Hsin 6th Rd.,
Hsinchu Science Park,
Hsin-chu City 300, Taiwan, R.O.C.
TEL: +886-3-5798797
FAX: +886-3-5646929
MAIL: sales@davicom.com.tw
HTTP: http://www.davicom.com.tw

WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.