English Language Test Description

Contract Number: N00244-09-C-0054

For

Unit Under Test

UUT Nomenclature: CVSD Encoder/Decoder CCA
UUT Part Number: 2618553-1
UUT Reference Designator: ICS A1

From

Assault Amphibious Vehicle
AN/PSM-115

ATE (Automated Test Equipment) SYSTEM

AN/USM-657B(V)2 Third Echelon Test System (TETS)
AN/USM-717(V)2 Virtual Instrument Portable Equipment Repair / Tester (VIPER/T)

Developed by

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Prepared By	Signature	Date Prepared	Date Submitted
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Approved By	Signature	Date Received	Date Approved

ELTD REVISION SUMMARY

Revision Number	Date	Reason	Approved By – Date Approved
-	05/18/2010	ORIGINAL ISSUE	

1. Introduction

The Unit Under Test (UUT) for this English Language Test Description (ELTD) is the CVSD Encoder/Decoder Circuit Card Assembly (CCA), Part Number 2618553-1. The CCA is reference designator A1 in all versions of the Intercommunication Set (ICS) Line Replaceable Unit (LRU) part number AN/MIQ-1(V)3. It may also be found in slots A2 and A3, depending on the LRU version. The LRU resides in the Assault Amphibious Vehicle (AAV) Weapon System.

1.1. Scope

An ELTD is a detailed supplementary document consisting of textual test descriptions with graphical representation of signal interconnectivity and a functional flow chart.

1.2. Purpose

The purpose of this document is to provide English language test descriptions for the TP_AAV_ICS_A1 test program, to a level of detail used for maintenance purposes. The TP_AAV_ICS_A1 test program makes up part of the AN/PSM-115 Application Program Set (APS).

1.3. Content Arrangement

The document is laid out in the sequence the Test Program Set (TPS) would be executed when a 95 “Run All Mods” is entered in the main menu. A paragraph at the beginning of each module will describe the test description for that module. Each step will contain a description for that particular test followed by a graphical representation of the connections made from the receiver, through the Interface Test Adapter (ITA) and cable W10 to the CVSD Encoder/Decoder CCA. A Functional Flow Chart resides at the end of the document.

2. English Language Test Description (ELTD)

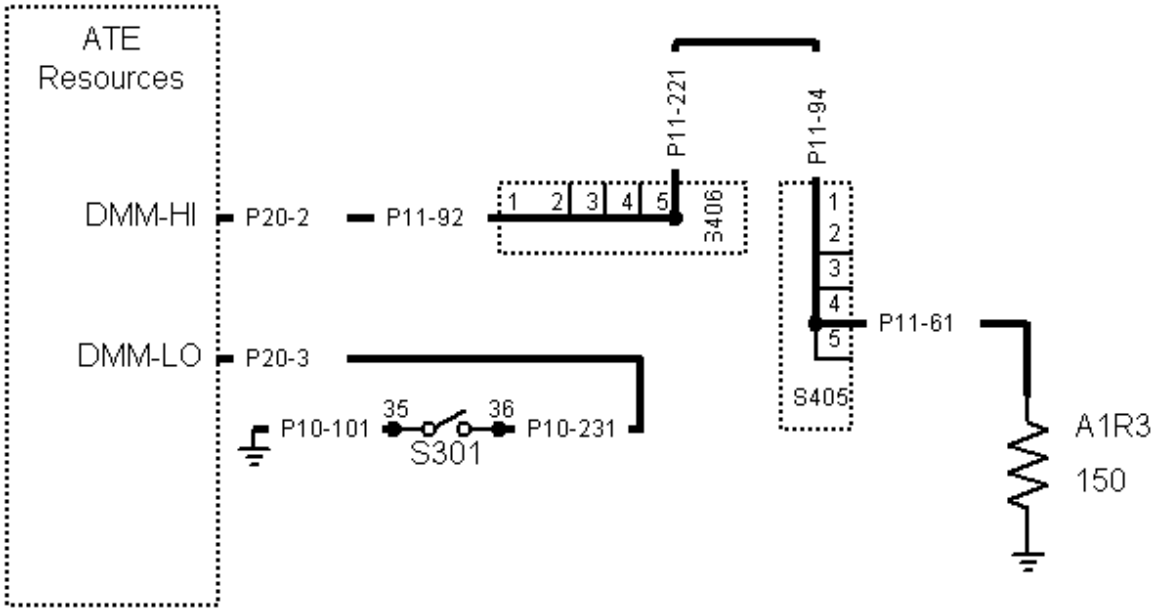
WEAPON SYSTEM: Assault Amphibious Vehicle (AAV)
UNIT UNDER TEST: 2618553-1
TEST PROGRAM SET: TP_AAV_ICS_A1

SAFE TO TURN ON TESTS

Step 1 ITA Identification

Test step 1 verifies the correct ITA is installed by using the DMM to measure the resistance of ITA A1R3. The resistance should be from 149 ohms to 155 ohms.

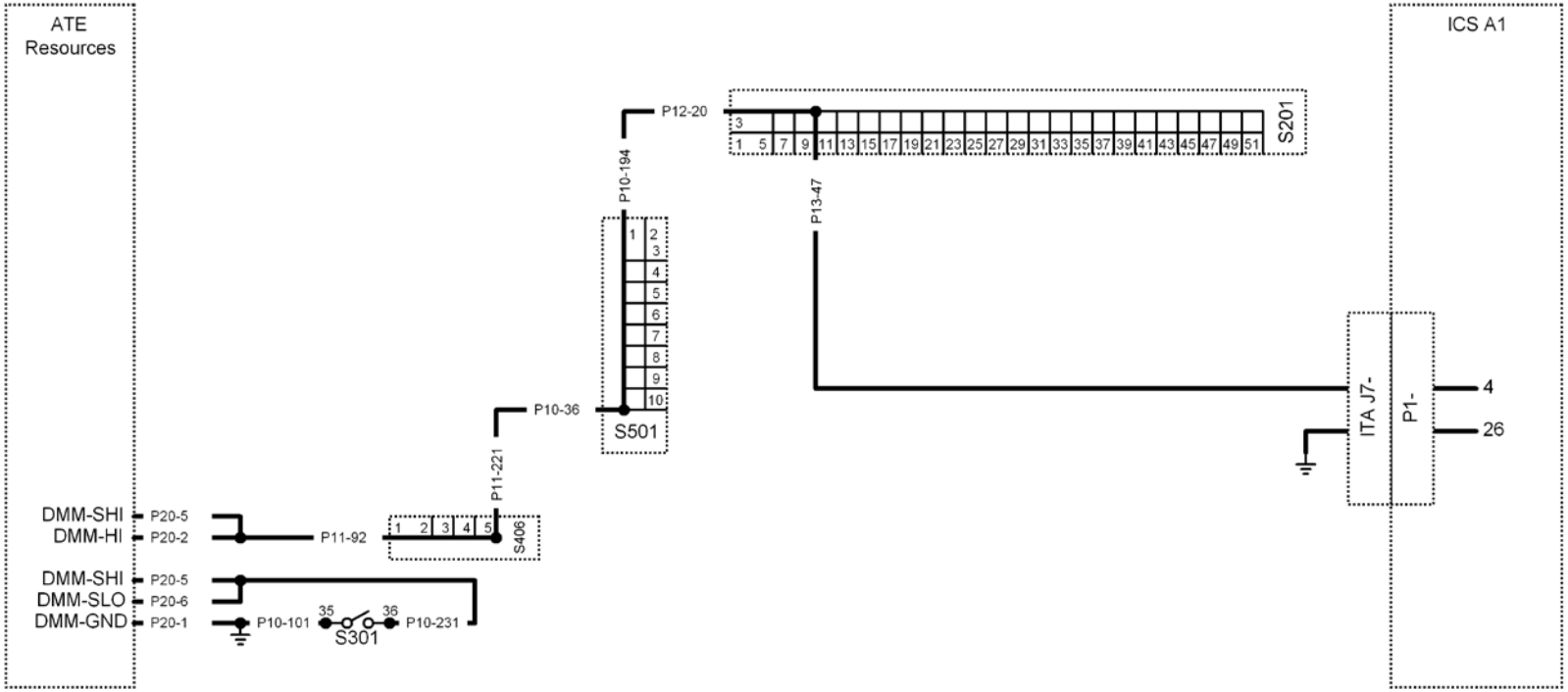
Connection Path as follows:



Step 2 UUT Identification (P1-4/GND)

This step (in conjunction with Step 3) identifies the UUT as a CVSD Encoder/Decoder CCA. The DMM is used to verify less than 10 ohms from P1-4 to GND.

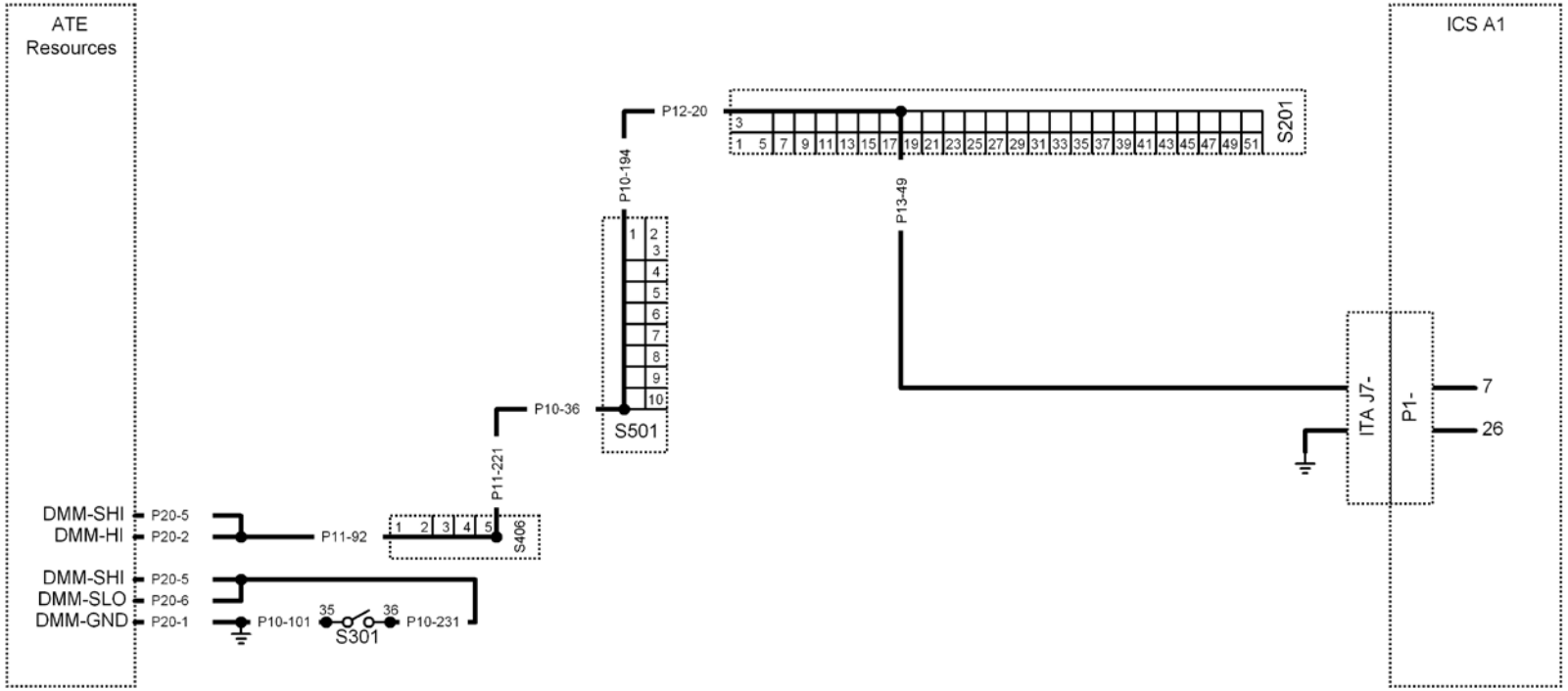
Connection Path as follows:


ATE
Resources
ICS A1
P12-20
S201
P10-194
P13-47
S501
P10-36
P11-221
S406
P11-92
DMM-SHI
DMM-HI
DMM-SHI
DMM-SLO
DMM-GND
P20-5
P20-2
P20-5
P20-6
P20-1
P10-101
S301
P10-231
ITA J7-
P1-
4
26

Step 3 UUT Identification (P1-7/GND)

This step (in conjunction with Step 2) identifies the UUT as a CVSD Encoder/Decoder CCA. The DMM is used to verify less than 10 ohms from P1-7 to GND.

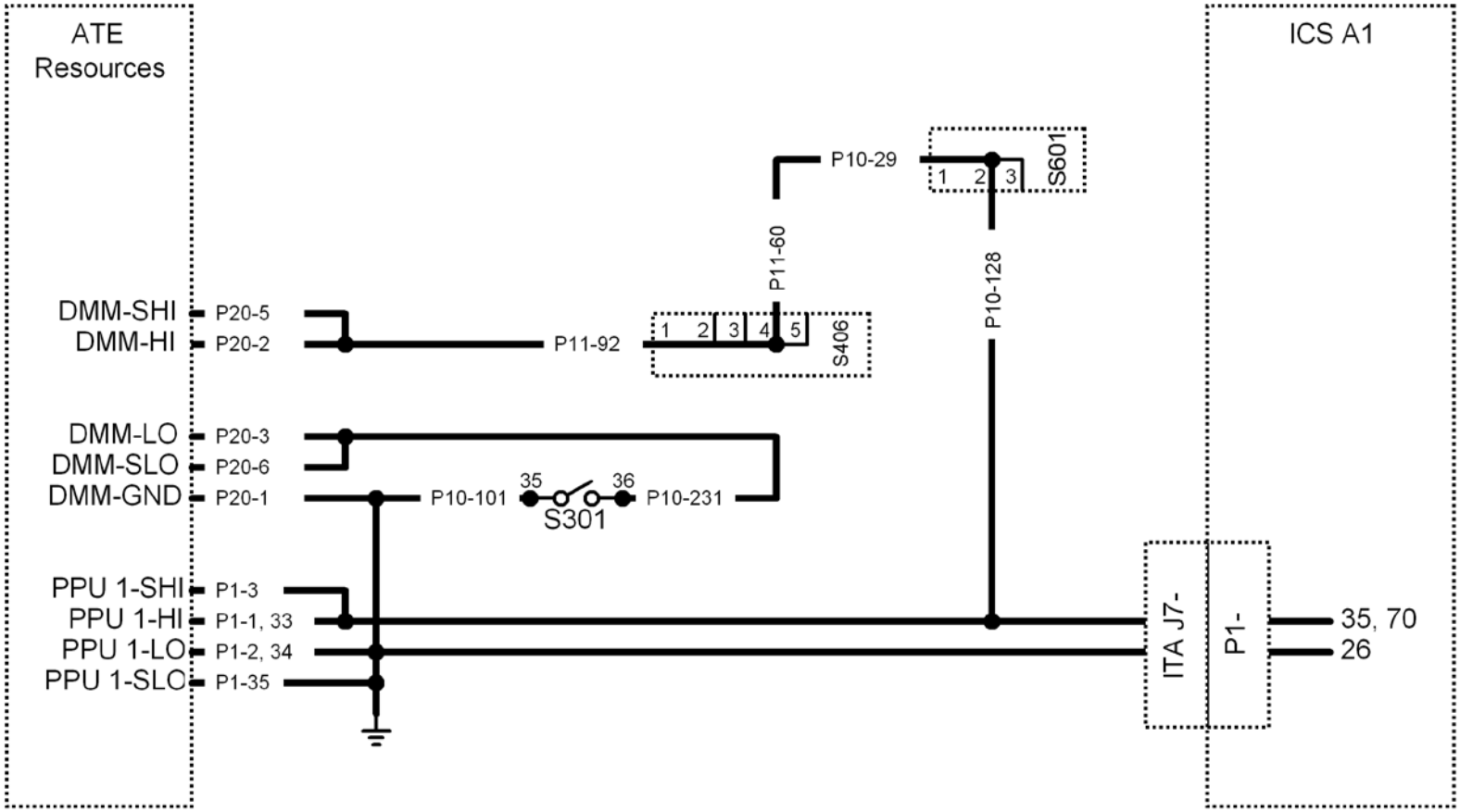
Connection Path as follows:


ATE
Resources
ICS A1
P12-20
S201
P10-194
P13-49
P10-36
S501
P11-221
ITA J7-
P1-
7
26
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
S406
DMM-SHI
DMM-SLO
DMM-GND
P20-5
P20-6
P20-1
P10-101
S301
P10-231

Step 4 +15 VDC Input Power STTO Test

This step verifies the UUT +15V power input circuitry is free of shorts that would constitute an Unsafe-to-Turn-On condition. DCPS (PPU) #1 is applied at P1-35/GND at a low voltage of 2V at 0.2 amps. The DMM is used to verify that the PPU did not sense an over-current condition by verifying nominally greater than 1.5VDC at P1-70/GND.

Connection Path as follows:


ATE
Resources
ICS A1
P10-29
S601
1 2 3
P11-60
P10-128
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
1 2 3 4 5
S406
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-101
35
36
P10-231
S301
PPU 1-SHI
PPU 1-HI
PPU 1-LO
PPU 1-SLO
P1-3
P1-1, 33
P1-2, 34
P1-35
ITA J7-
P1-
35, 70
26

UUT POWER UP

The UUT requires the following input power which remains applied for the duration of the test program:

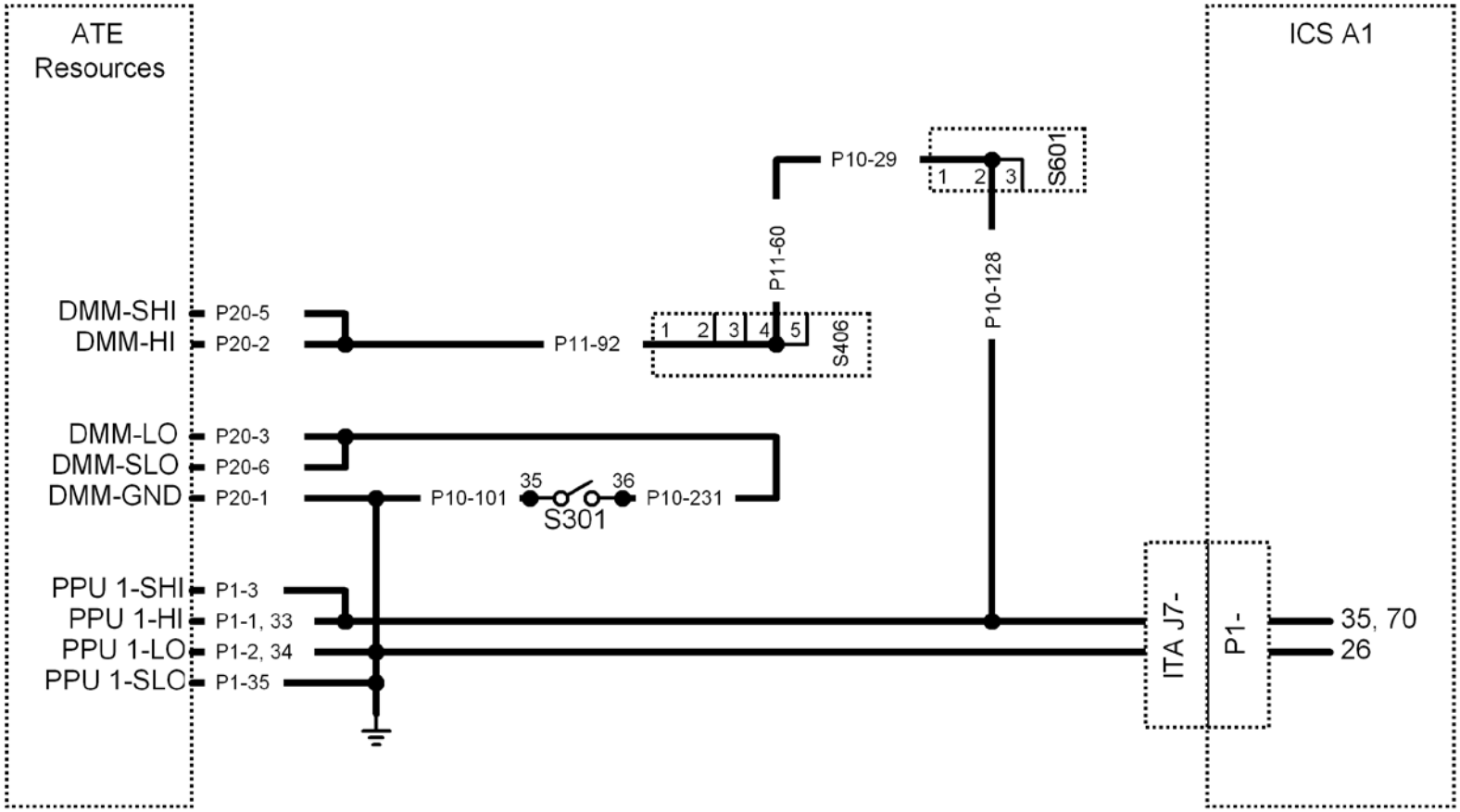
UUT PINS	VOLTAGE	CURRENT	PPU USED
P1-35,70(+)/P1-26(-)	+15.0VDC +/-0.25VDC	1.0 A	DCPS 1

UUT POWER UP TESTS

Step 5 +15 VDC Power Up Test

This step applies UUT +15V power and verifies the UUT +15V power input circuit is free of shorts that were not detected by the Safe-to-Turn-On Test. The DMM is used to verify 15 +/-0.25 VDC at P1-70/GND.

Connection Path as follows:


ATE
Resources
ICS A1
P10-29
S601
1 2 3
P11-60
P10-128
DMM-SHI P20-5
DMM-HI P20-2
P11-92
1 2 3 4 5
S406
DMM-LO P20-3
DMM-SLO P20-6
DMM-GND P20-1
P10-101
35
36
P10-231
S301
PPU 1-SHI P1-3
PPU 1-HI P1-1, 33
PPU 1-LO P1-2, 34
PPU 1-SLO P1-35
ITA J7-
P1-
35, 70
26

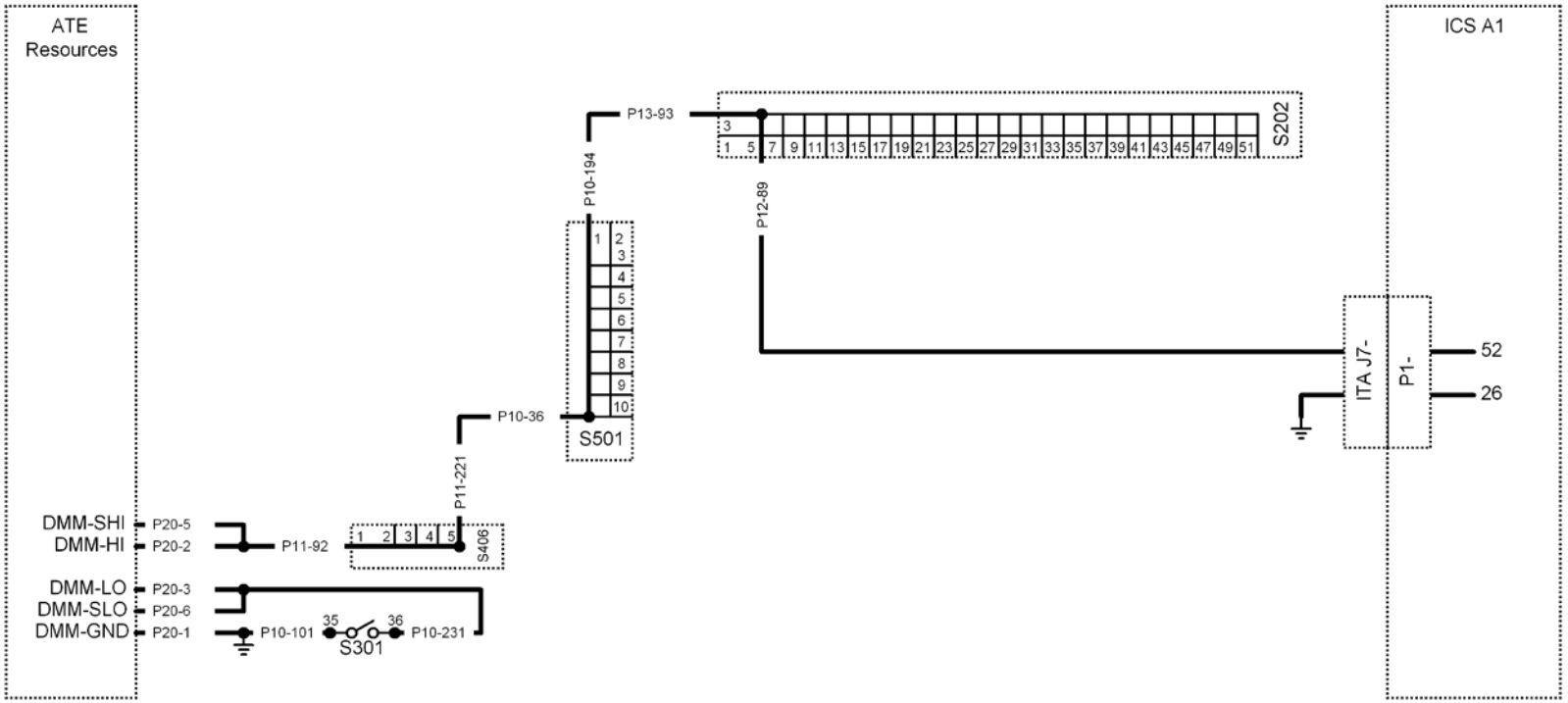
MODULE 1 STATIC TESTS

Module 1 performs static voltage measurements on various UUT I/O pins with no input signals applied. This also verifies the +6 VDC and +12 VDC voltage regulators are functional.

Step 101 Regulated +12V Output/R80 Pullup Test

This step verifies the +12 VDC pullup on P1-52 via R80. By doing so, it also verifies functionality of the +12 VDC regulator circuit. The DMM is used to verify 12.0 +/- 2VDC at P1-52/GND.

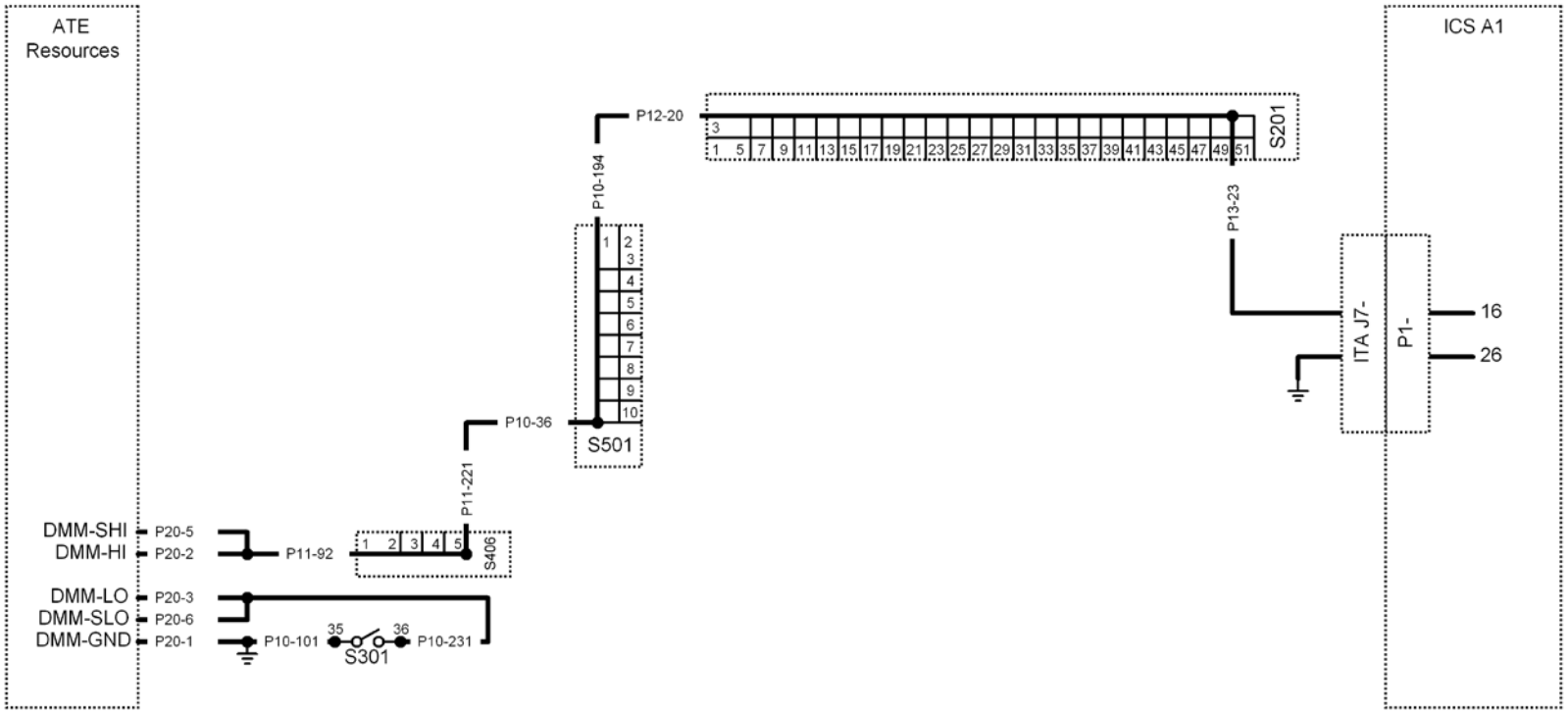
Connection Path as follows:


ATE
Resources
ICS A1
P13-93
S202
P10-194
P12-89
S501
P10-36
P11-221
ITA J7-
P1-
52
26
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
S406
P10-101
S301
P10-231

Step 102 R78 Pullup (+12V) Test

This step verifies the +12 VDC pullup on P1-16 via R78. The DMM is used to verify 12.0 +/-2VDC at P1-16/GND.

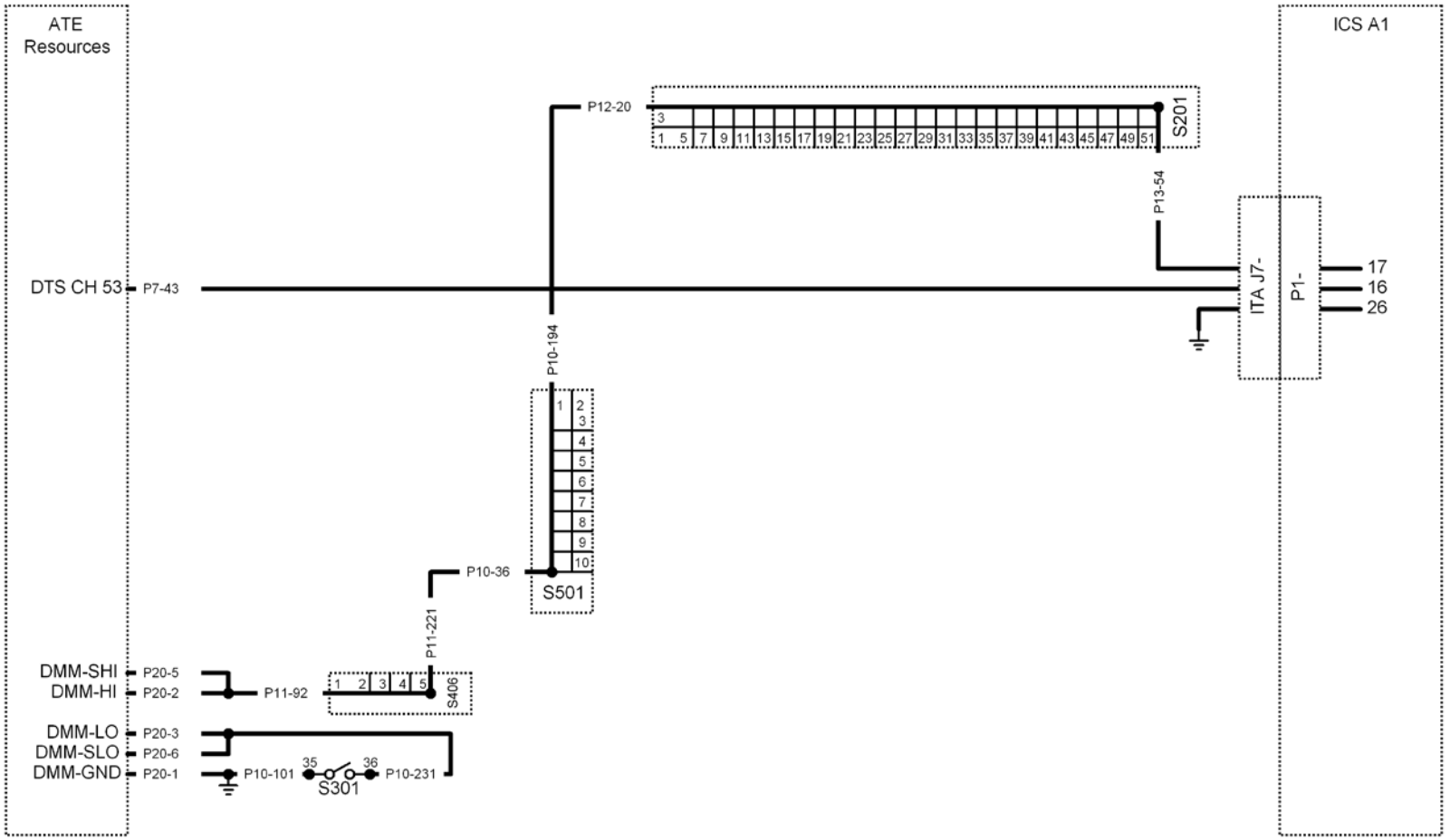
Connection Path as follows:


ATE
Resources
ICS A1
P12-20
S201
P10-194
P13-23
P10-36
S501
P11-221
ITA J7-
P1-
16
26
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
S406
P10-101
S301
P10-231

Step 103 R79 Pullup (+12V) Test

This step verifies the +12 VDC pullup on P1-17 via R79. A logic LO is applied to P1-16 to open switch contacts on U5-10 using the DTS. The DMM is then used to verify 12.0 +/-2VDC at P1-17/GND.

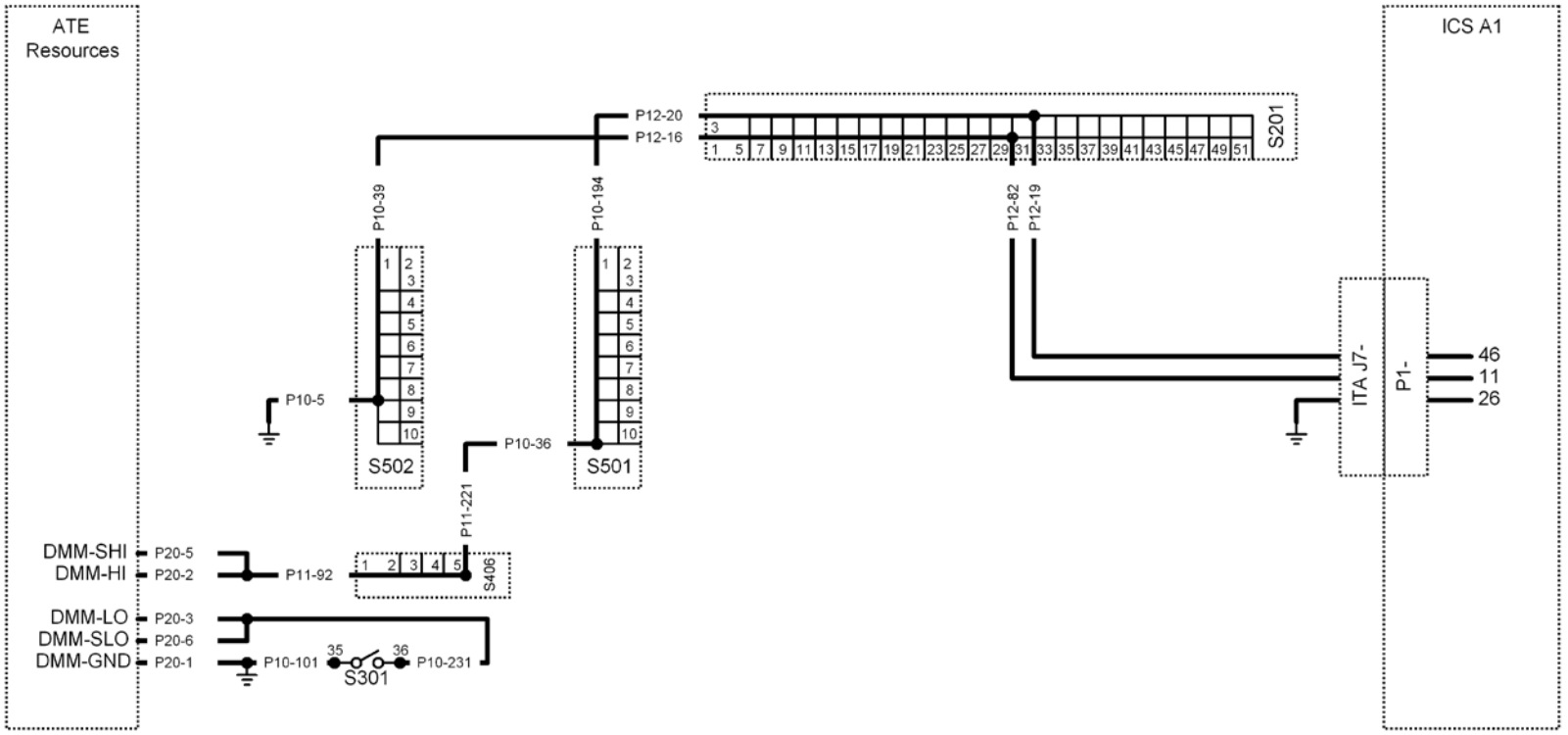
Connection Path as follows:


ATE
Resources
ICS A1
P12-20
S201
P13-54
ITA J7-
P1-
17
16
26
DTS CH 53
P7-43
P10-194
P10-36
S501
P11-221
DMM-SHI
P20-5
DMM-HI
P20-2
P11-92
S406
DMM-LO
P20-3
DMM-SLO
P20-6
DMM-GND
P20-1
P10-101
S301
P10-231

Step 104 R71 Pullup (+12V) Test

This step verifies the +12 VDC pullup on P1-46 via R71. P1-11 is connected to GND to test for a U8-1 to U8-2 (B-C) short. The DMM is used to verify 12.0 +/-2VDC at P1-46/GND.

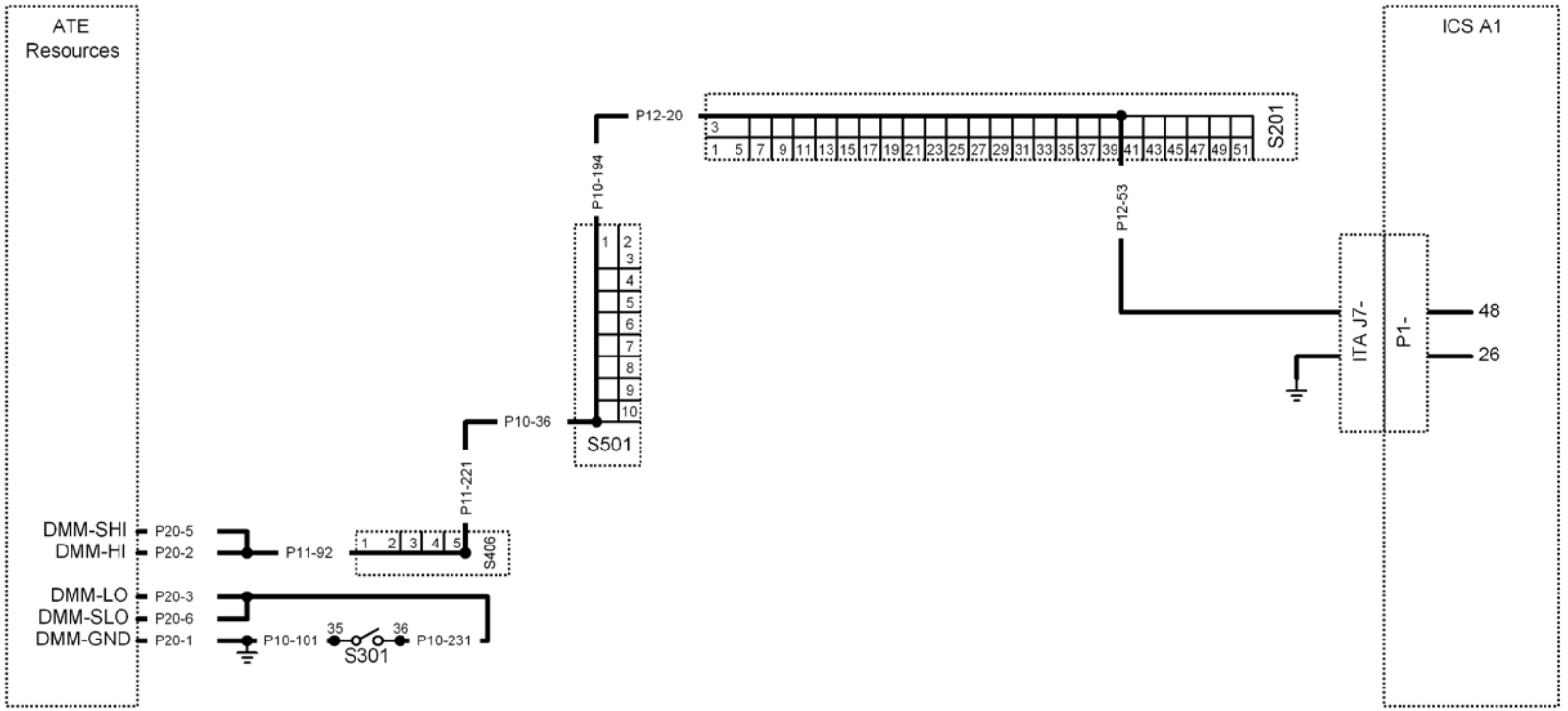
Connection Path as follows:


ATE
Resources
ICS A1
P12-20
P12-16
S201
P10-39
P10-194
P12-82
P12-19
P10-5
P10-36
S502
S501
ITA J7-
P1-
46
11
26
P11-221
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
S406
P10-101
P10-231
S301

Step 105 R72 Pullup (+12V) Test

This step verifies the +12 VDC pullup on P1-48 via R72. The DMM is then used to verify 12.0 +/-2VDC at P1-48/GND.

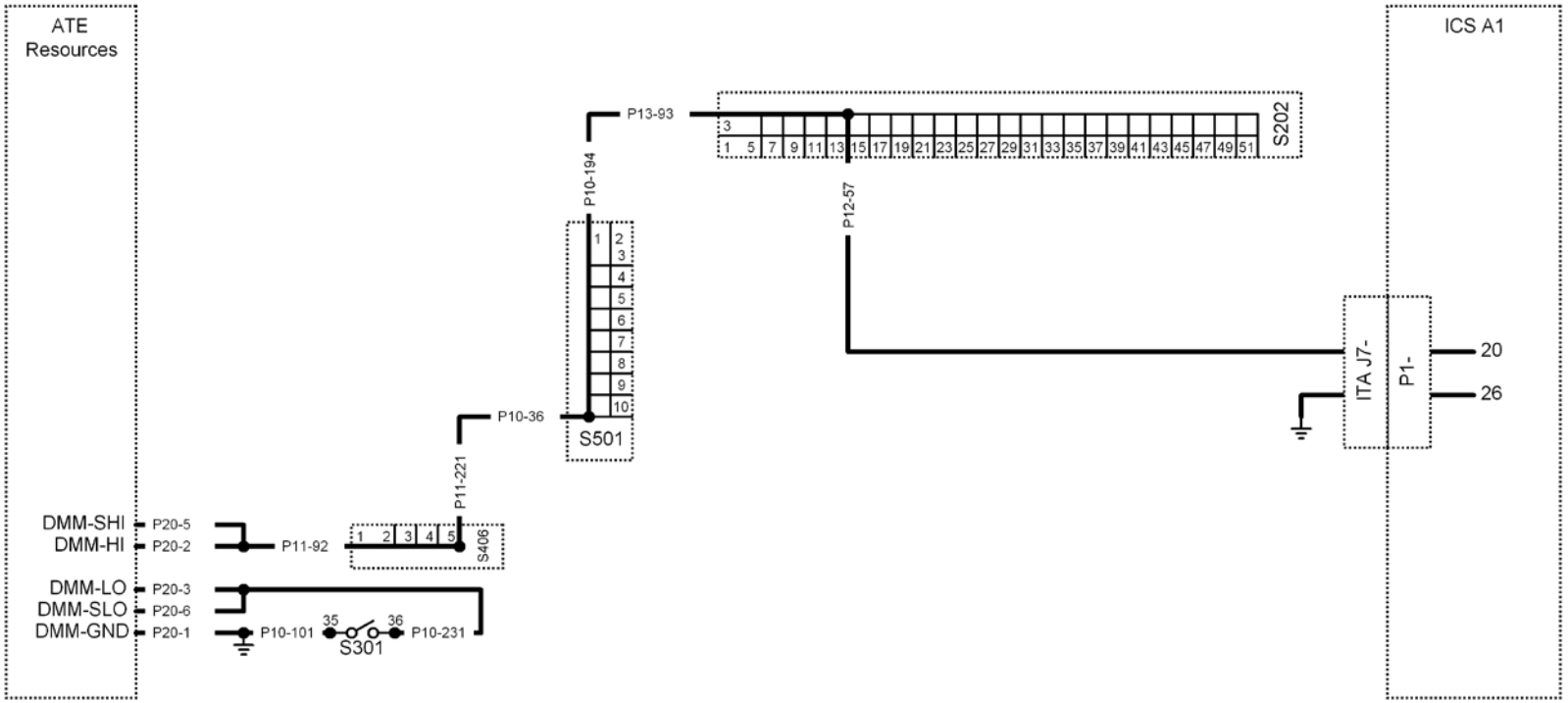
Connection Path as follows:


ATE
Resources
ICS A1
P12-20
S201
P10-194
P12-53
P10-36
S501
P11-221
ITA J7-
P1-
48
26
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
S406
P10-101
P10-231
S301
35
36

Step 106 Regulated +6V Output/R85 Pullup Test

This step verifies the +6 VDC pullup on P1-20 via R85. By doing so, it also verifies functionality of the +6 VDC regulator circuit. The DMM is used to verify 6.0 +/-1VDC at P1-20/GND.

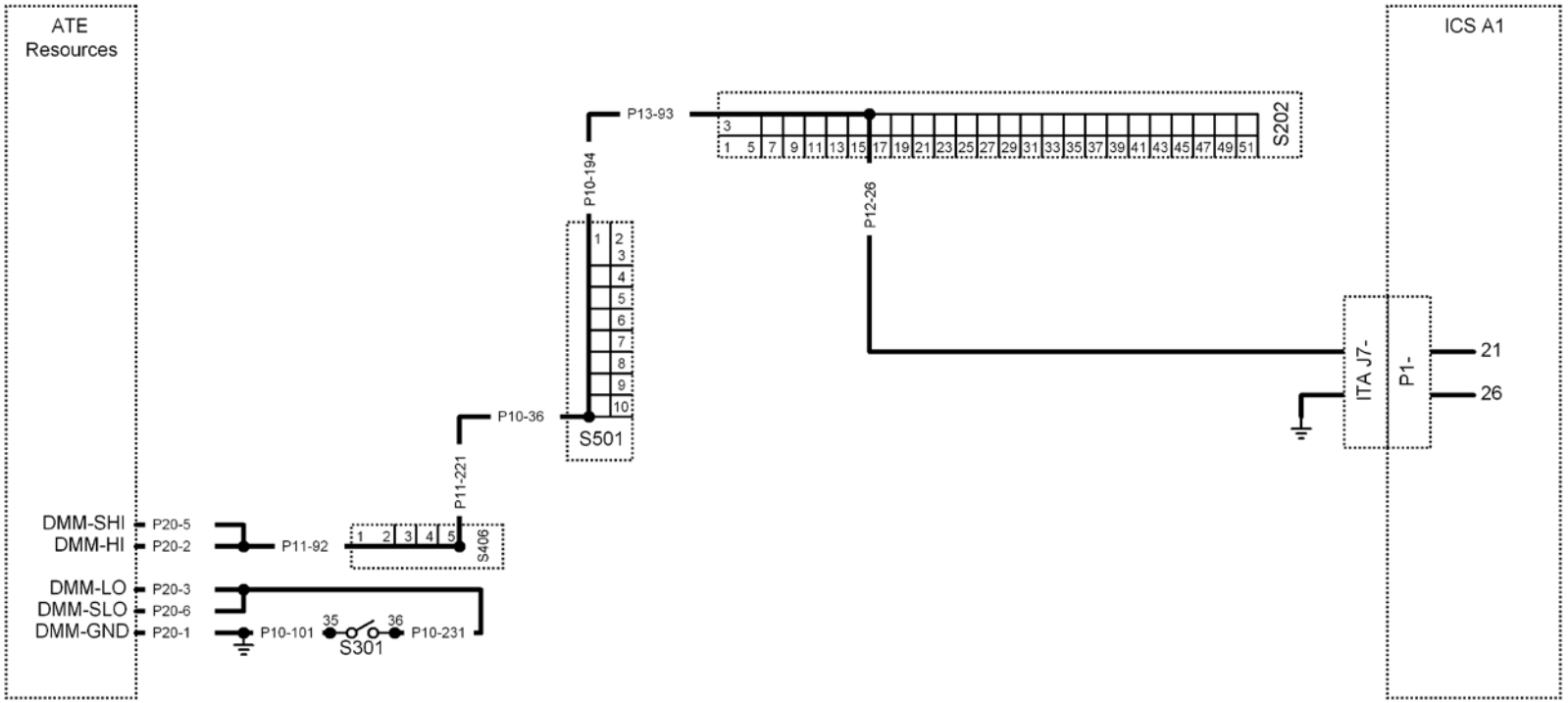
Connection Path as follows:


ATE
Resources
ICS A1
P13-93
S202
P10-194
P12-57
S501
P10-36
P11-221
ITA J7-
P1-
20
26
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
S406
P10-101
S301
P10-231

Step 107 R84 Pullup (+6V) Test

This step verifies the +6 VDC pullup on P1-21 via R84. The DMM is used to verify 6.0 +/-1VDC at P1-21/GND.

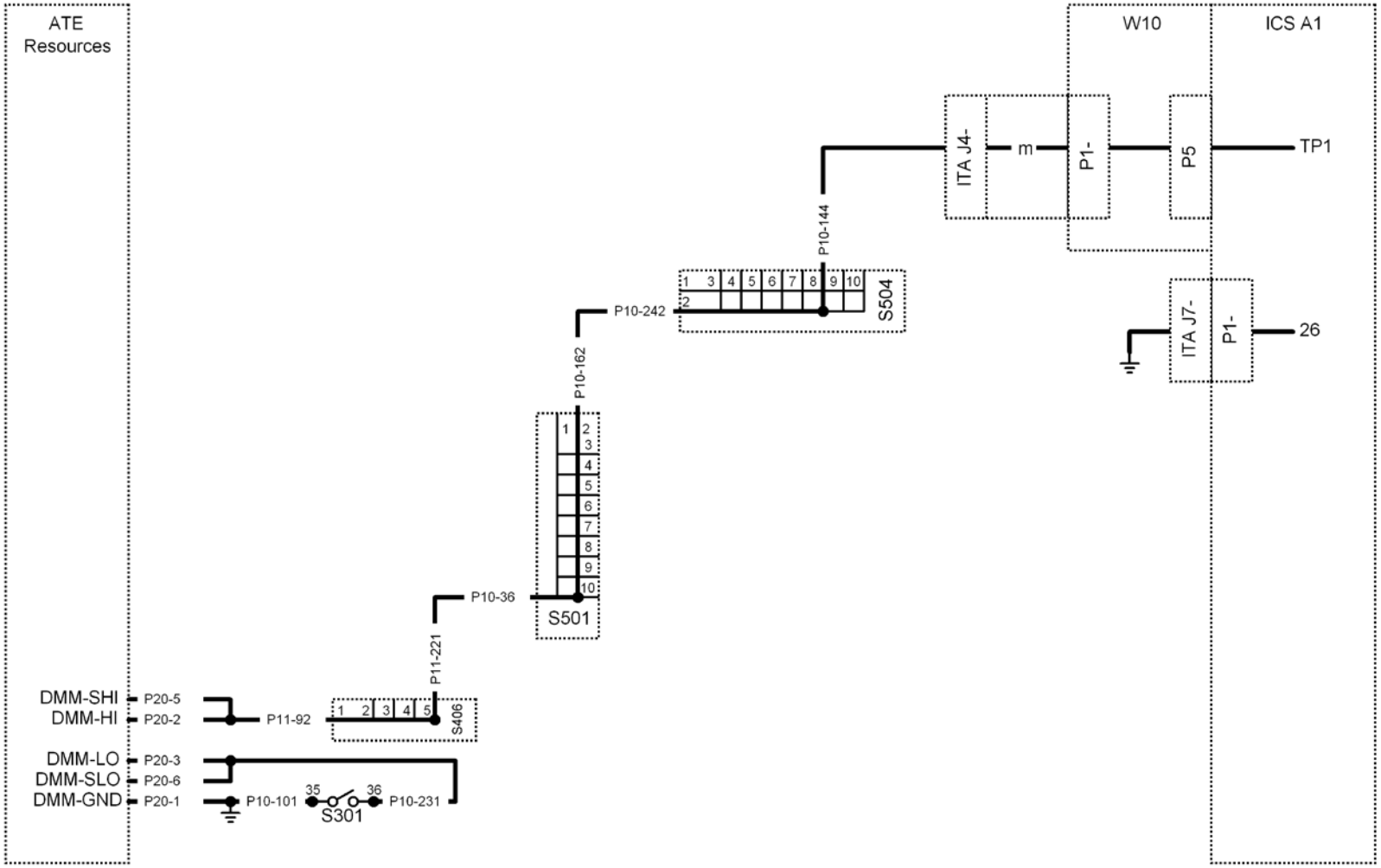
Connection Path as follows:


ATE
Resources
ICS A1
P13-93
S202
P10-194
P12-26
P10-36
S501
P11-221
ITA J7-
P1-
21
26
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
S406
P10-101
S301
P10-231

Step 108 R12 Pullup (+6V) Test

This step verifies the +6 VDC pullup on the input to U1-A at TP1. The DMM is used to verify 6.0 +/-1VDC at TP1/GND.

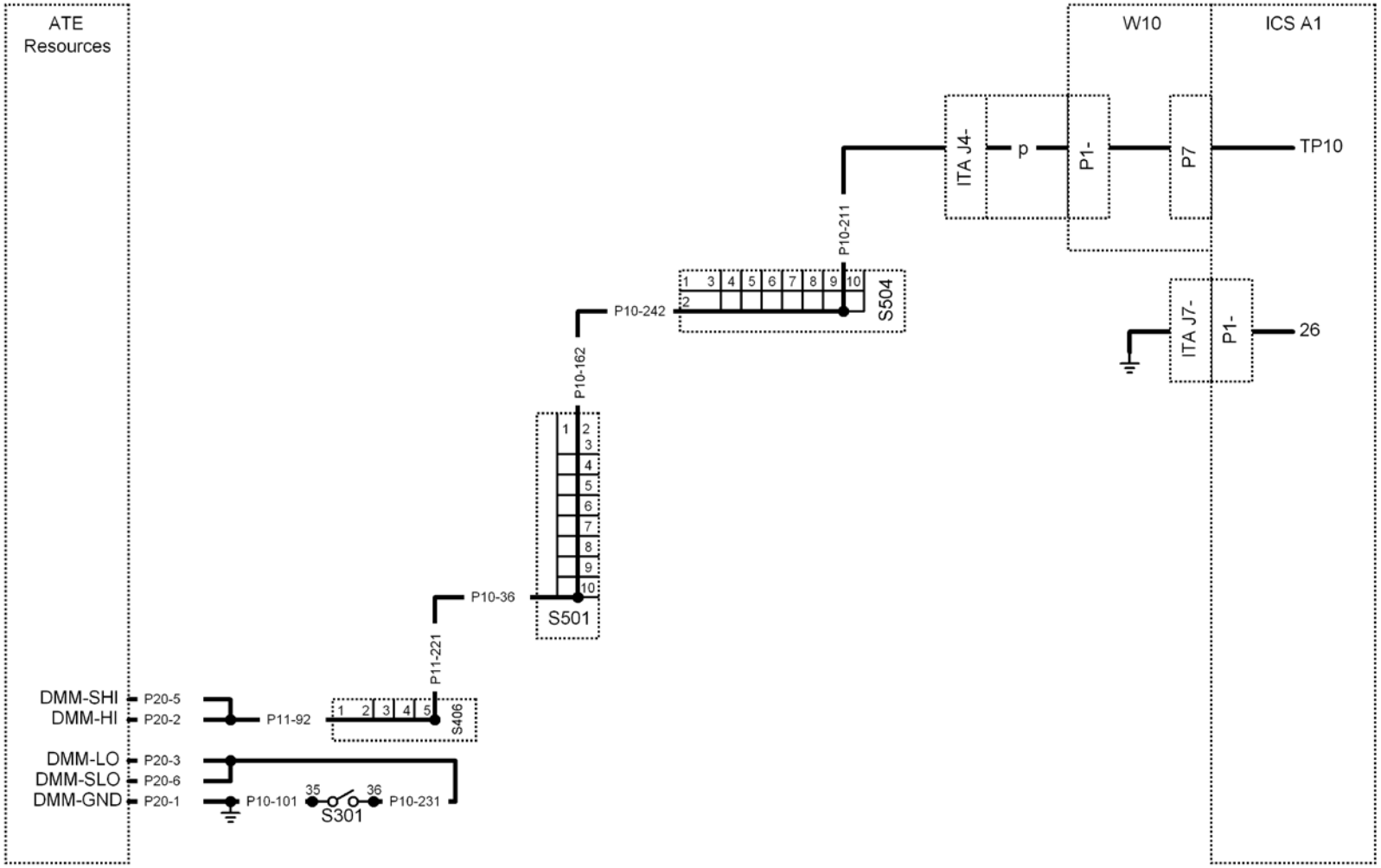
Connection Path as follows:


ATE
Resources
W10
ICS A1
ITA J4-
m
P1-
P5
TP1
P10-144
S504
P10-242
P10-162
ITA J7-
P1-
26
P10-36
S501
P11-221
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
S406
P10-101
S301
P10-231

Step 109 R41 Pullup (+6V) Test

This step verifies the +6 VDC pullup on the input to U7-A at TP10. The DMM is used to verify 6.0 +/-1VDC at TP10/GND.

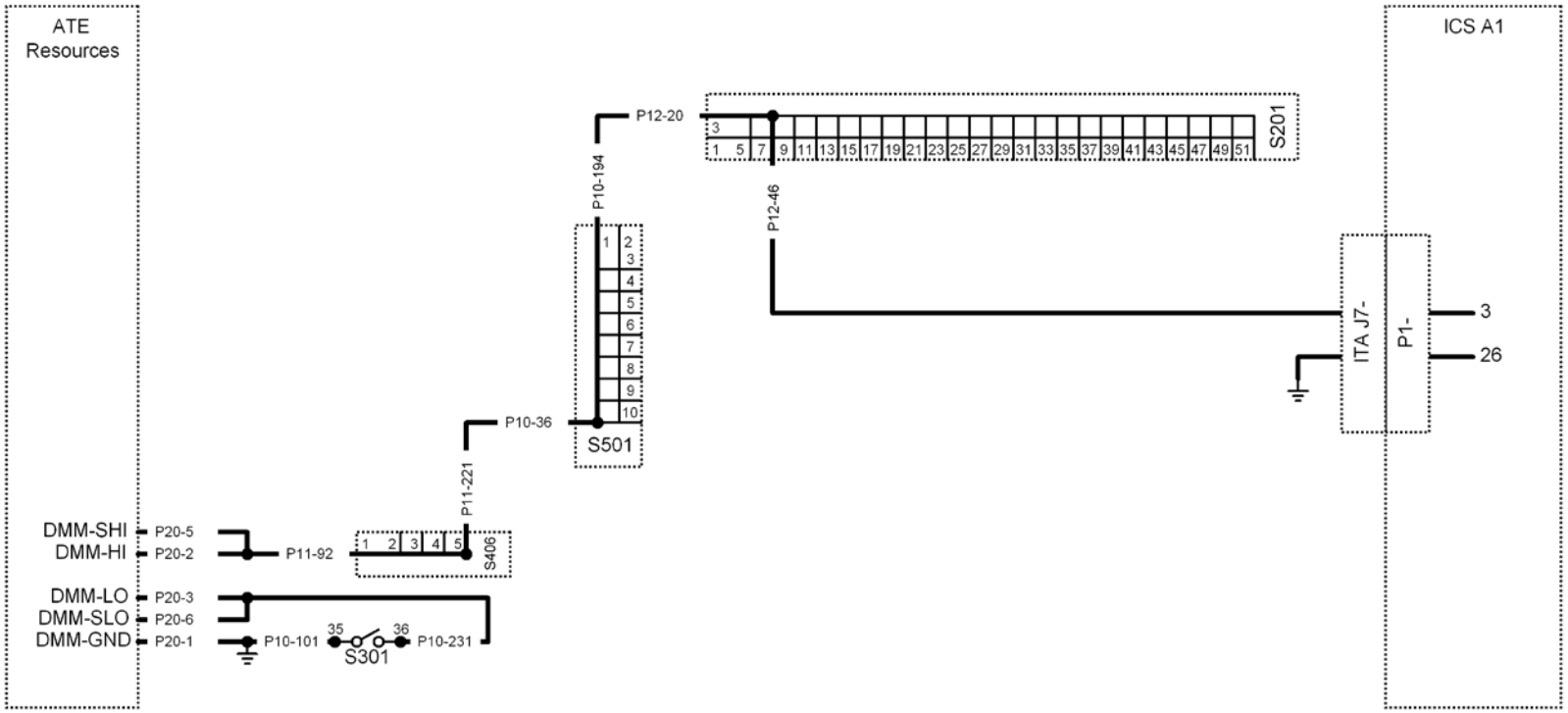
Connection Path as follows:


ATE
Resources
W10
ICS A1
ITA J4-
p
P1-
P7
TP10
P10-211
S504
P10-242
P10-162
ITA J7-
P1-
26
P10-36
S501
P11-221
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
S406
P10-101
S301
P10-231

Step 110 C47 Short Test

This step verifies that C47 is not shorted. The DMM is used to verify less than 0.1 VDC is present on P1-3.

Connection Path as follows:


ATE
Resources
ICS A1
P12-20
S201
P10-194
P12-46
P10-36
S501
P11-221
ITA J7-
P1-
3
26
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
S406
P10-101
P10-231
S301

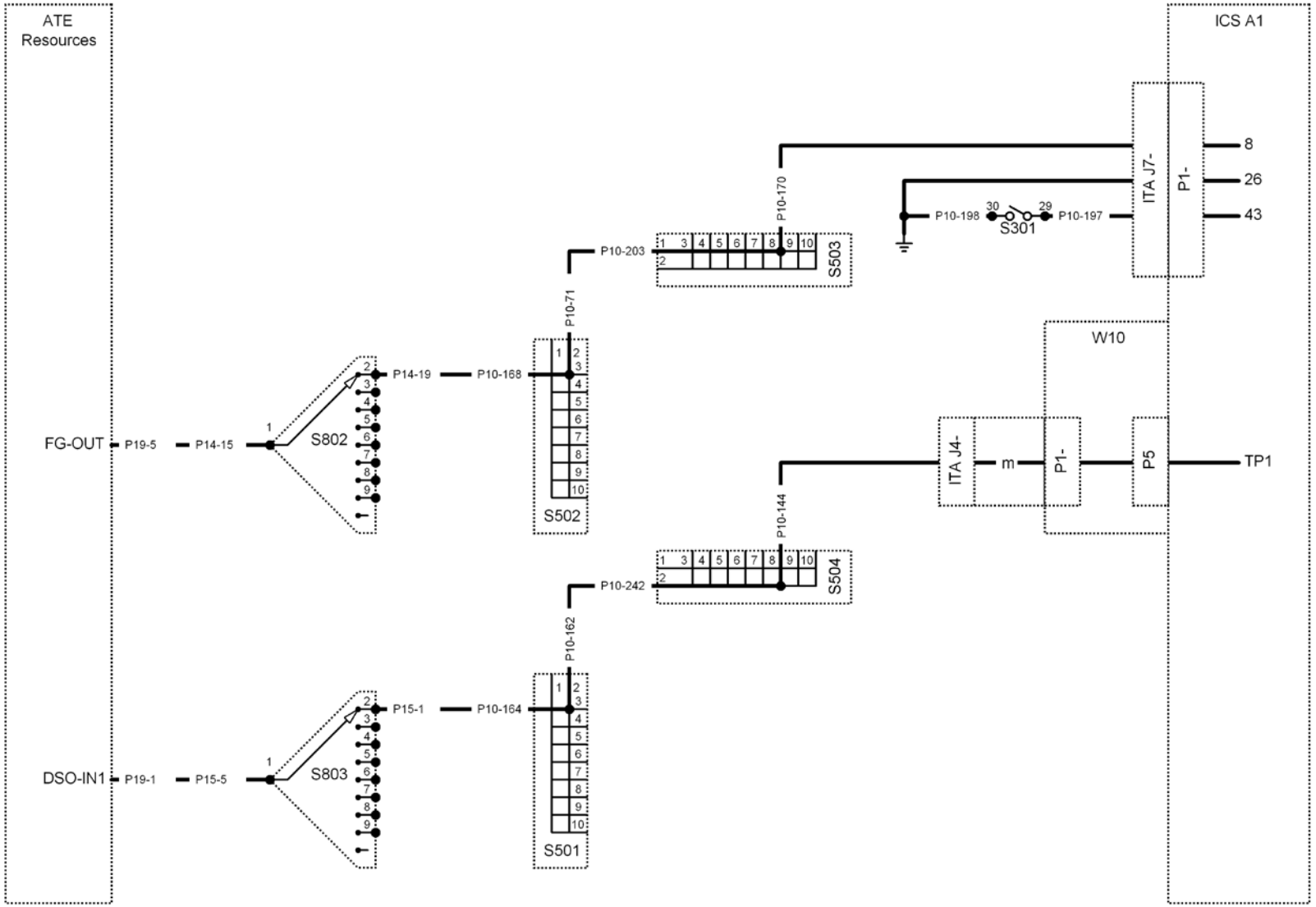
MODULE 2 COMPRESSOR OPERATION TESTS

Module 2 verifies the performance of the input compressor circuit by applying a test audio signal at T1 primary input and verifying the specified amplitude at TP1.

Step 201 Compressor Amplifier Amplitude via “Radio” Input Test

This step verifies the functionality of the Compressor Amplifier circuitry. A high-level 1.0 KHz sine wave audio input of 10.28 Vpp is applied to the RADIO INPUT at P1-8/43 using the Function Generator. Because of the 50-ohm input impedance of the Function Generator and a voltage divider at the input of the circuit 5.6 Vpp is programmed, but during execution this voltage is doubled to 11.2 Vpp, then divided back down to 10.2 Vpp before the signal reaches any active circuitry. The amplitude at TP1 is verified using the Digitizing Oscilloscope to be 1.0 to 1.6 Vpp. The measured value is saved and used by step 202 to determine measurement tolerances for that step.

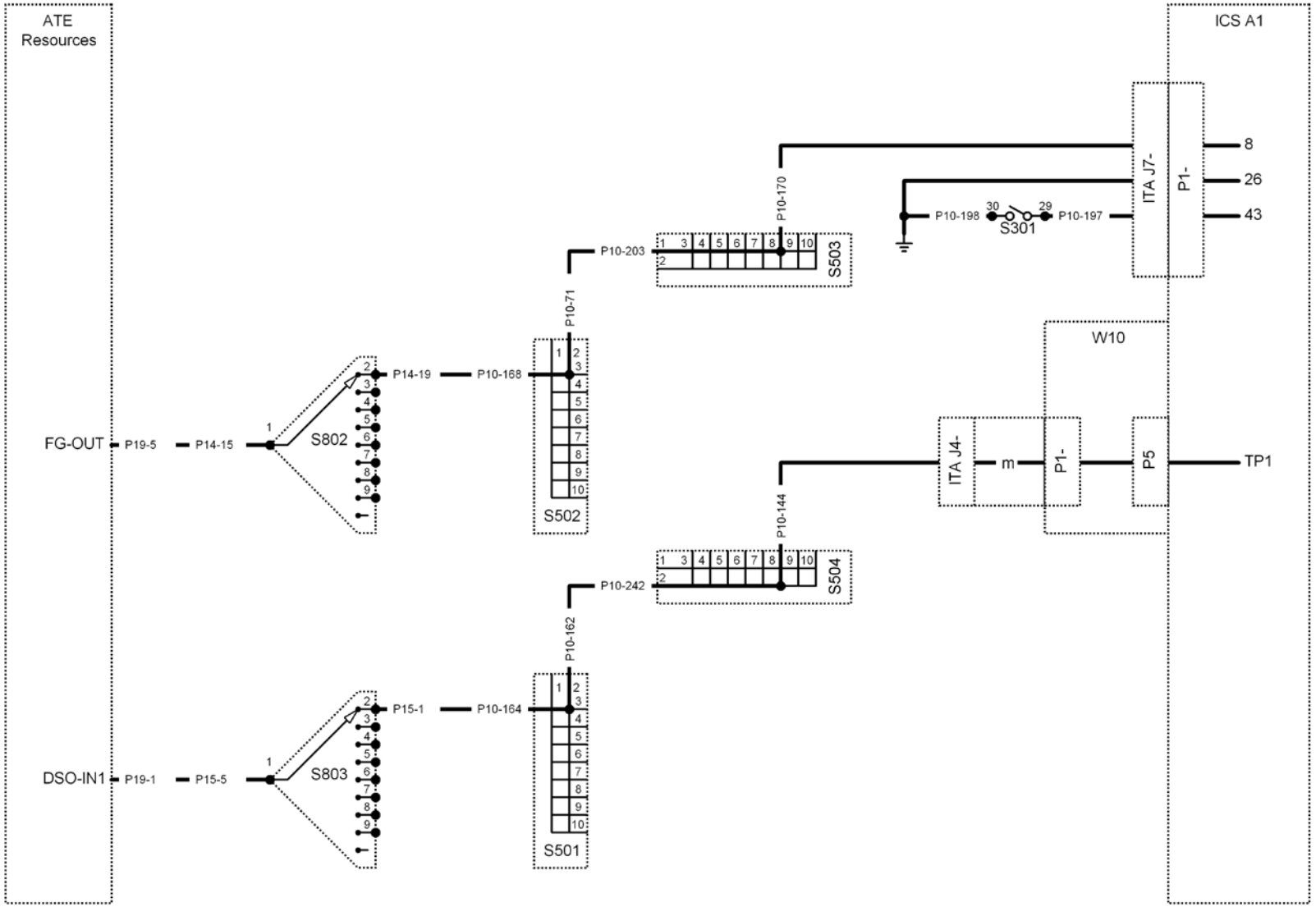
Connection Path as follows:


ATE Resources
ICS A1
FG-OUT
P19-5
P14-15
S802
P14-19
P10-168
S502
P10-71
P10-203
S503
P10-170
P10-198
S301
P10-197
ITA J7-
P1-
8
26
43
W10
ITA J4-
m
P1-
P5
TP1
P10-144
S504
P10-242
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
S501
P10-162

Step 202 Compressor Amplifier Distortion Test

This step verifies that no distortion is present on Compressor Amplifier output at TP1. A sine wave audio input of 10.0 Vpp is applied to the RADIO INPUT at P1-8/43 using the Function Generator. Because of the 50-ohm input impedance of the Function Generator and a voltage divider at the input of the circuit 5.6 Vpp is programmed, but during execution this voltage is doubled to 11.2 Vpp, then divided back down to 10.0 Vpp before the signal reaches any active circuitry. The True-RMS voltage TP1 is verified using the DMM to show a power difference of no greater than 10% when compared to the Vpp measured by Step 201.

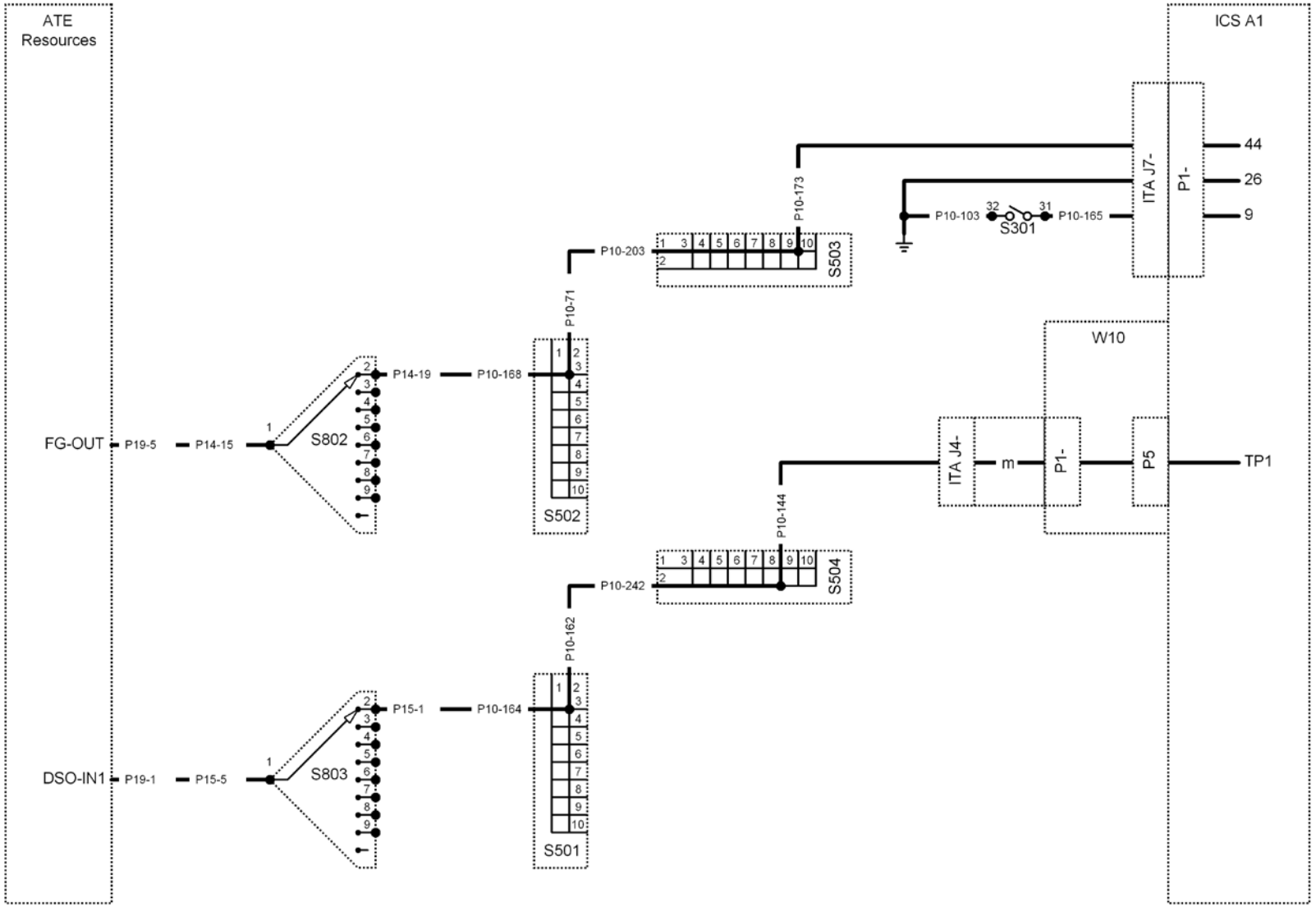
Connection Path as follows:


ATE
Resources
ICS A1
FG-OUT
P19-5
P14-15
S802
P14-19
P10-168
S502
P10-71
P10-203
S503
P10-170
P10-198
S301
P10-197
ITA J7-
P1-
8
26
43
W10
ITA J4-
m
P1-
P5
TP1
P10-144
S504
P10-242
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
S501
P10-162

Step 203 Compressor Amplifier Amplitude via “Crew” Input Test

This step verifies the functionality of the Compressor Amplifier circuitry with a sine wave audio input of 15.0 Vpp is applied to the CREW INPUT at P1-44/9 using the Function Generator. Because of the 50-ohm input impedance of the Function Generator only 7.5 Vpp is programmed, but during execution this voltage is doubled before it is applied. The amplitude at TP1 is verified using the Digitizing Oscilloscope to be 0.5 to 1.6 Vpp.

Connection Path as follows:


ATE Resources
ICS A1
FG-OUT
P19-5
P14-15
S802
P14-19
P10-168
P10-71
S502
P10-203
P10-173
S503
P10-103
S301
P10-165
ITA J7-
P1-
44
26
9
W10
ITA J4-
m
P1-
P5
TP1
P10-144
S504
P10-242
P10-162
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
S501

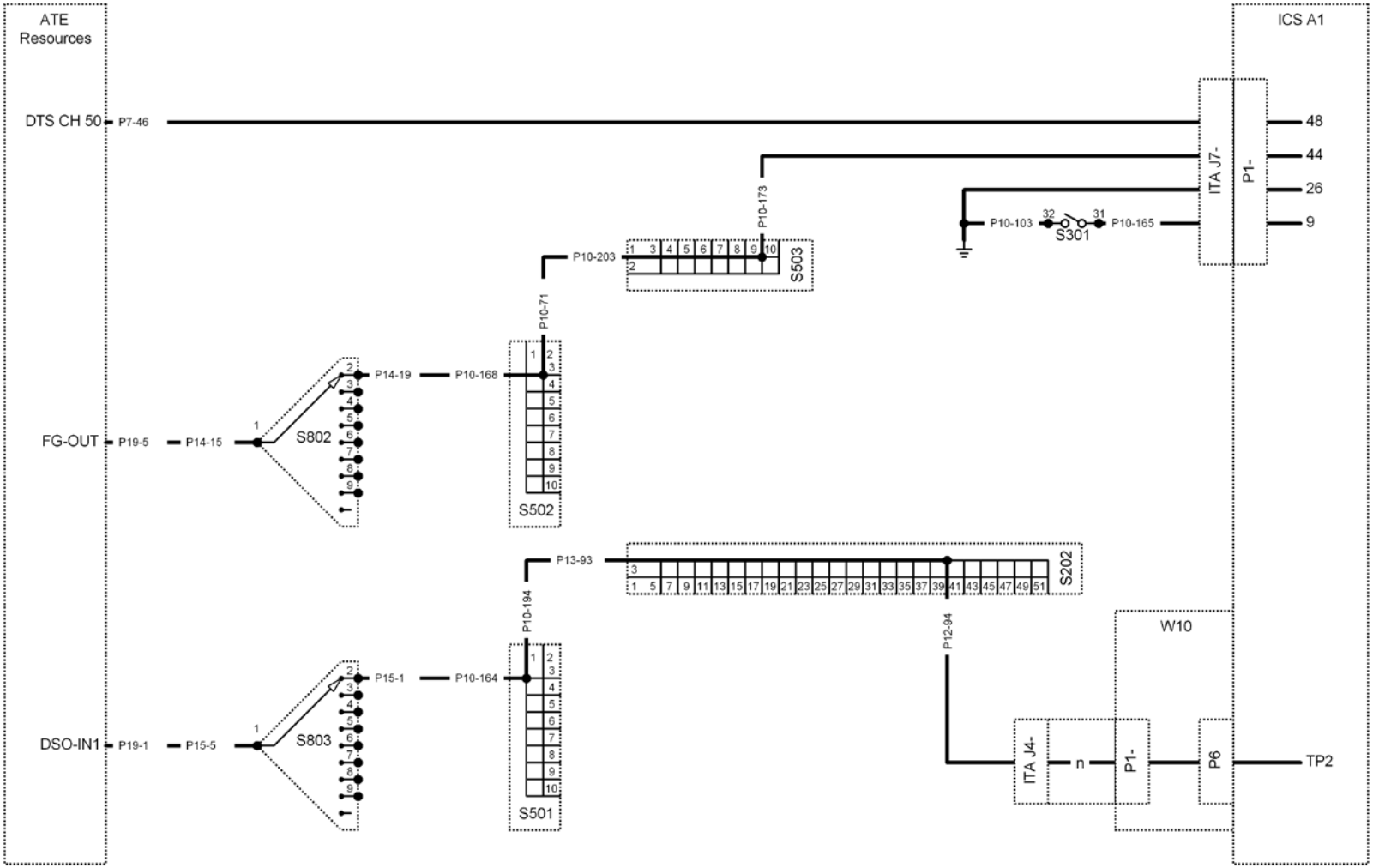
MODULE 3 PREAMPLIFIER AND ENCODER FILTER TESTS

Module 3 verifies the functionality of the preamp/encoder filter circuit built around U1, by applying a test audio signal at T1 primary input and verifying the specified amplitude at TP2.

Step 301 Preamplifier Amplitude Test.

This step verifies the gain through the Preamplifier/Encoder Filter circuit built around U1. Preamplifier gain select pin P1-46 is left open (HI) and the DTS is used to apply a logic LO to P1-48. A 1.0 KHz sine wave audio input of 15.0 Vpp is applied to the CREW INPUT at P1-44/9 using the Function Generator. Because of the 50-ohm input impedance of the Function Generator only 7.5 Vpp is programmed, but during execution this voltage is doubled before it is applied. The amplitude at TP2 is verified using the Digitizing Oscilloscope to be 1.0 to 3.0 Vpp. The measured value is saved and used by step 302 to determine measurement tolerances for that step.

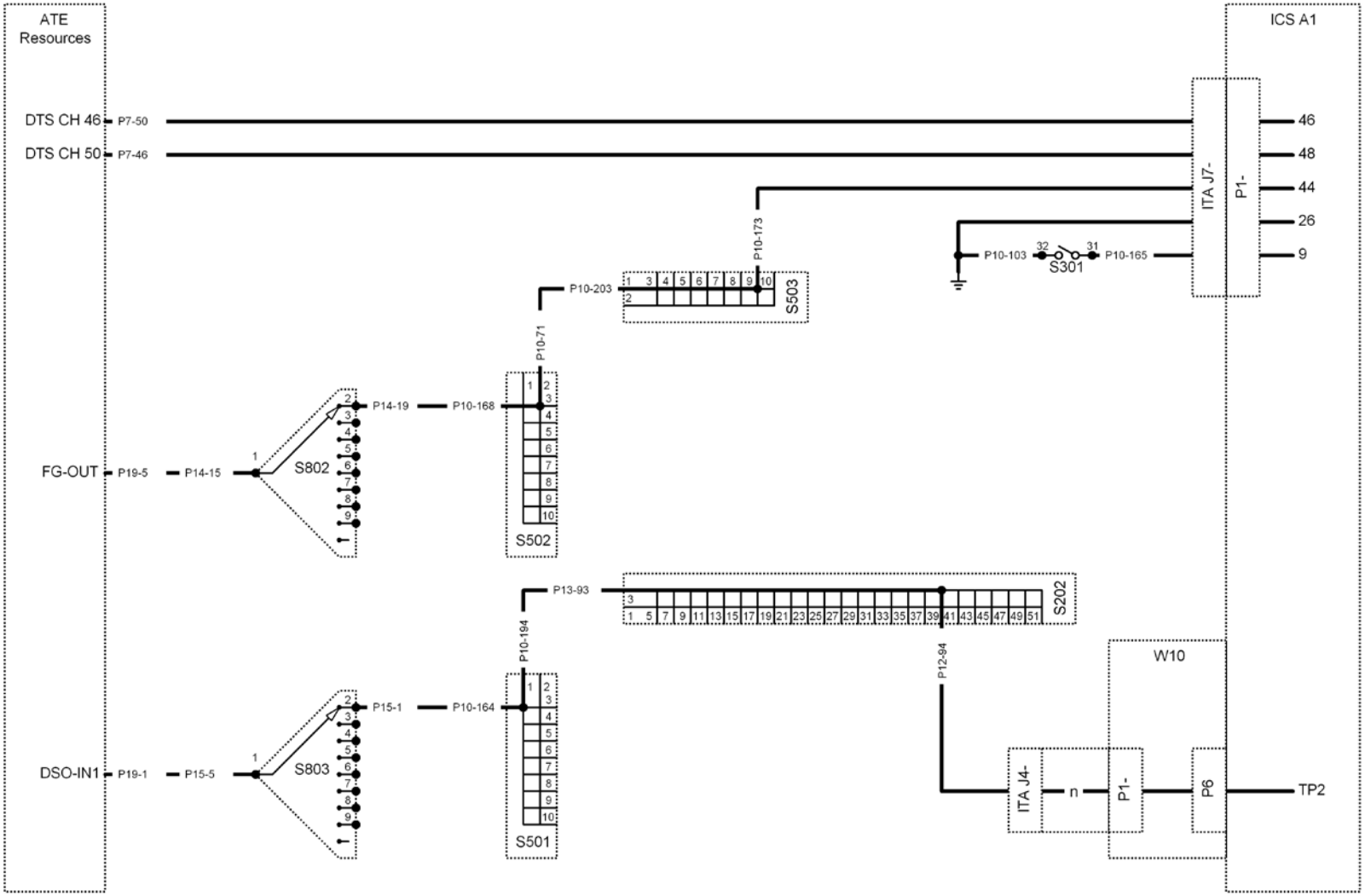
Connection Path as follows:


ATE Resources
ICS A1
DTS CH 50
P7-46
FG-OUT
P19-5
P14-15
S802
P14-19
P10-168
P10-71
S502
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
P10-194
S501
P10-203
P10-173
S503
P10-103
S301
P10-165
ITA J7-
P1-
48
44
26
9
P13-93
S202
P12-94
W10
ITA J4-
n
P1-
P6
TP2

Step 302 U1-A Low-Gain Test

This step verifies functionality of the preamplifier gain select input at P1-46. A sine wave audio input of 15.0 Vpp applied to the CREW INPUT at P1-44/9 using the Function Generator. Because of the 50-ohm input impedance of the Function Generator only 7.5 Vpp is programmed, but during execution this voltage is doubled before it is applied. The DTS is used to apply a logic LO to gain select inputs P1-46 and P1-48. The amplitude at TP2 is verified using the Digitizing Oscilloscope to be between 80% and 95% of the amplitude measured in Step 301.

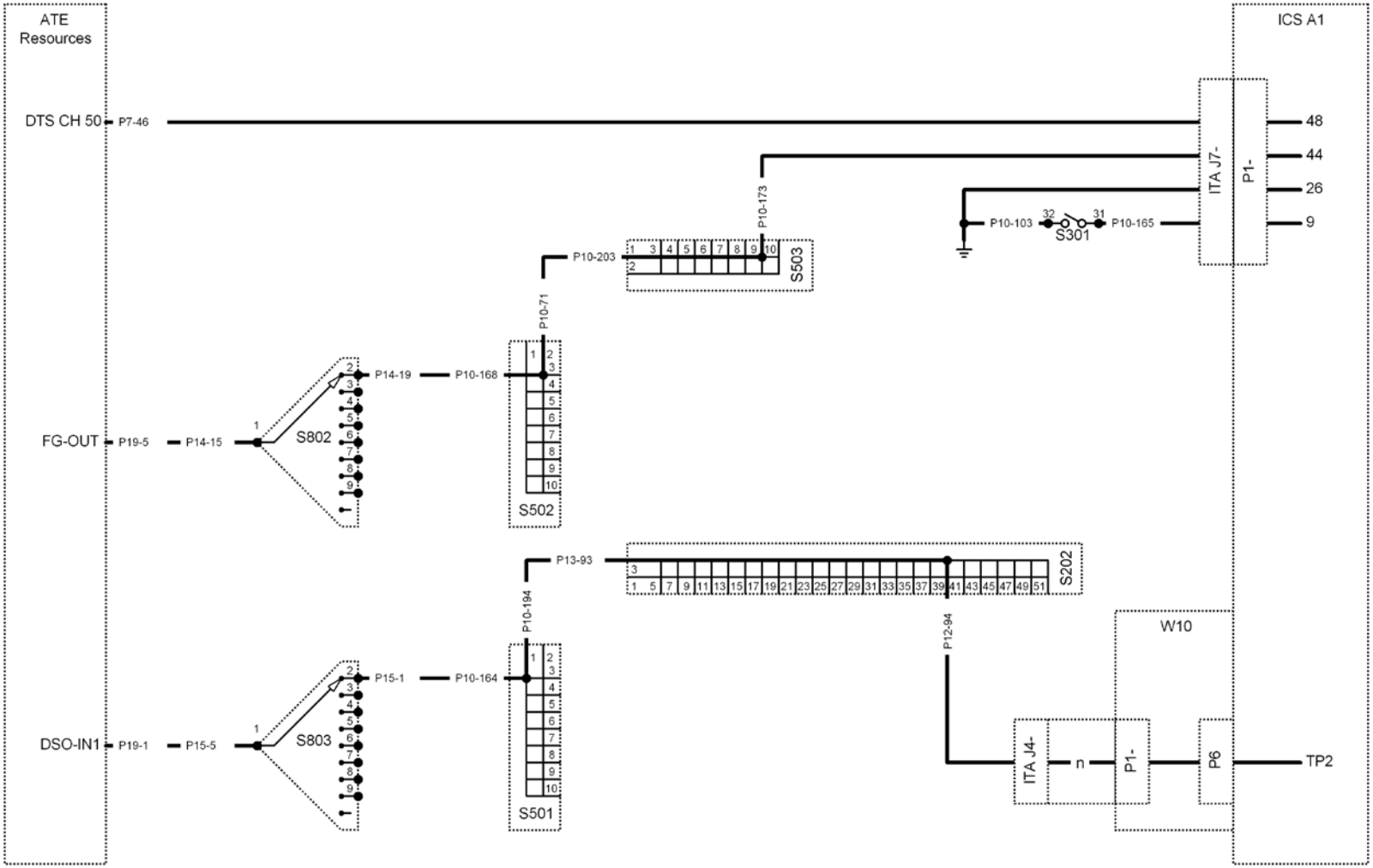
Connection Path as follows:


ATE Resources
ICS A1
DTS CH 46
P7-50
DTS CH 50
P7-46
ITA J7-
P1-
46
48
44
26
9
P10-173
P10-103
32
31
P10-165
S301
P10-203
S503
P10-71
FG-OUT
P19-5
P14-15
S802
P14-19
P10-168
S502
P13-93
S202
P10-194
P12-94
W10
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
S501
ITA J4-
n
P1-
P6
TP2

Step 303 High-Pass Filter -3dB Roll-off Point Test

This step verifies that the 3dB roll-off (1/2 power) point of the High-Pass filter circuit is within the specified range of 150 to 400 Hz. To perform the test, the output frequency of the Function Generator (applied at P1-44/9 at 15.0 Vpp) is adjusted to 450 Hz and a reference output reading (Vpp) is made and stored using the Digitizing Oscilloscope at TP2. The DTS is used to apply a logic LO to gain select input P1-48. Then, the frequency is swept down from 425 KHz to a minimum of 125 Hz (in 25 Hz increments), until the 3dB roll-off point is detected. This is defined as the input frequency at which the amplitude is less than 0.707 times that of the reference reading at 450 Hz.

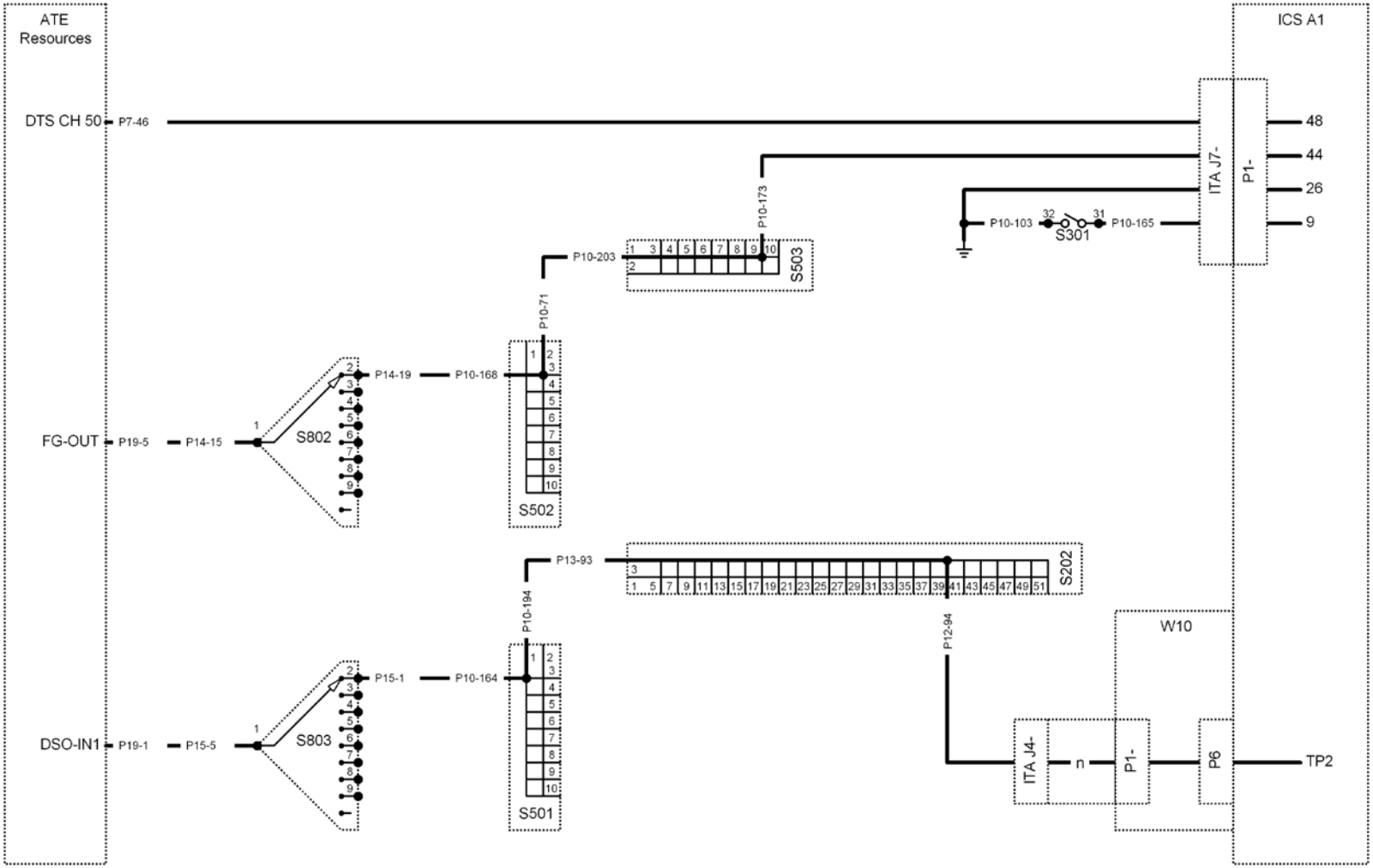
Connection Path as follows:


ATE Resources
ICS A1
DTS CH 50
P7-46
FG-OUT
P19-5
P14-15
S802
P14-19
P10-168
P10-71
S502
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
P10-194
S501
P10-203
P10-173
S503
P10-103
S301
P10-165
ITA J7-
P1-
48
44
26
9
P13-93
S202
P12-94
W10
ITA J4-
n
P1-
P6
TP2

Step 304 Low-Pass Filter -3dB Roll-off Point Test

This step verifies that the 3dB roll-off (1/2 power) point of the Low-Pass filter circuit is within the specified range of 3.0 to 4.2 KHz. To perform the test, the output frequency of the Function Generator (applied at P1-44/9 at 15.0 Vpp) is adjusted to 2.8 KHz and a reference output reading (Vpp) is made and stored using the Digitizing Oscilloscope at TP2. The DTS is used to apply a logic LO to gain select input P1-48. Then, the frequency is swept down from 2.9 KHz to a maximum of 4.3 KHz (in 100 Hz increments), until the 3dB roll-off point is detected. This is defined as the input frequency at which the amplitude is less than 0.707 times that of the reference reading at 2.8 KHz.

Connection Path as follows:


ATE Resources
ICS A1
DTS CH 50
P7-46
FG-OUT
P19-5
P14-15
S802
P14-19
P10-168
P10-71
S502
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
P10-194
S501
P10-203
P10-173
S503
P10-103
S301
P10-165
ITA J7-
P1-
48
44
26
9
P13-93
S202
P12-94
W10
ITA J4-
n
P1-
P6
TP2

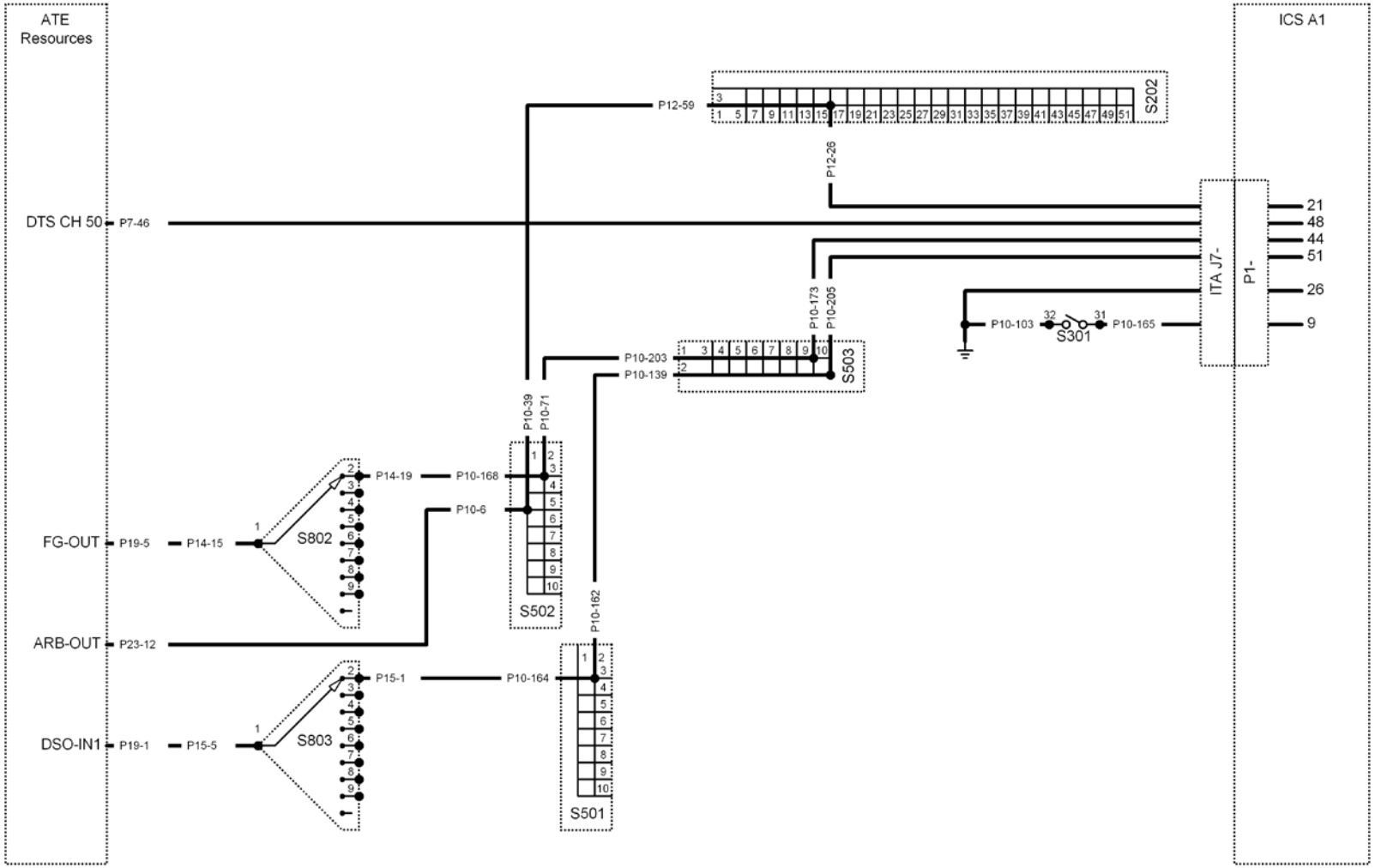
MODULE 4 CVSD ENCODER TESTS

Module 4 verifies the functionality of the CVSD Encoder U4, by applying a test audio signal at T1 primary input and verifying the specified single-ended amplitude at P1-51.

Step 401 CVSD Encoder Amplitude Test

This step verifies the amplitude at the CVSD Encoder output at test access pin P1-51. Preamplifier gain select pin P1-46 is left open (HI) and the DTS is used to apply a logic LO to P1-48. A 1.0 KHz sine wave audio input of 15.0 Vpp is applied to the CREW INPUT at P1-44/9 using the Function Generator and a single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21 using the ARB. Because of the 50-ohm input impedance of the Function Generator only 7.5 Vpp is programmed, but during execution this voltage is doubled before it is applied. The amplitude at P1-51 is verified using the Digitizing Oscilloscope to be 4.0 and 7.0 Vpp.

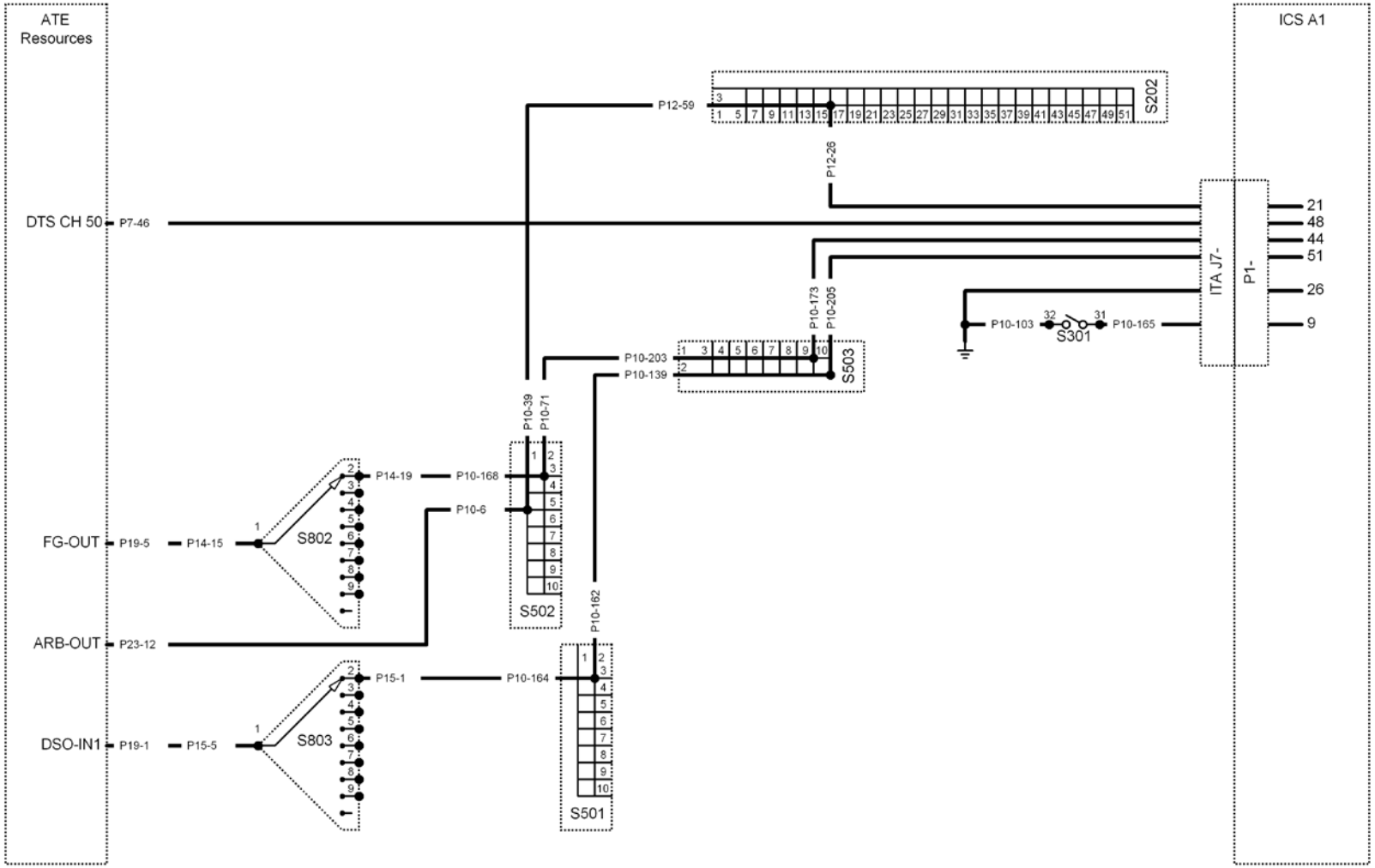
Connection Path as follows:


ATE Resources
ICS A1
DTS CH 50
P7-46
FG-OUT
P19-5
P14-15
ARB-OUT
P23-12
DSO-IN1
P19-1
P15-5
S802
S803
P14-19
P10-168
P10-6
P15-1
P10-164
P12-59
P12-26
S202
P10-203
P10-139
P10-173
P10-205
S503
P10-103
S301
P10-165
ITA J7-
P1-
21
48
44
51
26
9
P10-39
P10-71
S502
P10-162
S501

Step 402 CVSD Encoder Duty Cycle Test

This step verifies the DUTY-CYCLE of the CVSD Encoder output at test access pin P1-51 is varying (not equal to 50%, which indicates a fault condition). Preamplifier gain select pin P1-46 is left open (HI) and the DTS is used to apply a logic LO to P1-48. A sine wave audio input of 15.0 Vpp is applied to the CREW INPUT at P1-44/9 using the Function Generator and a single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21 using the ARB. Because of the 50-ohm input impedance of the Function Generator only 7.5 Vpp is programmed, but during execution this voltage is doubled before it is applied. The DUTY-CYCLE at P1-51 is verified using the Digitizing Oscilloscope to not be 50% +/- 2%. Multiple readings are taken if required since occasionally the reading will be 50%.

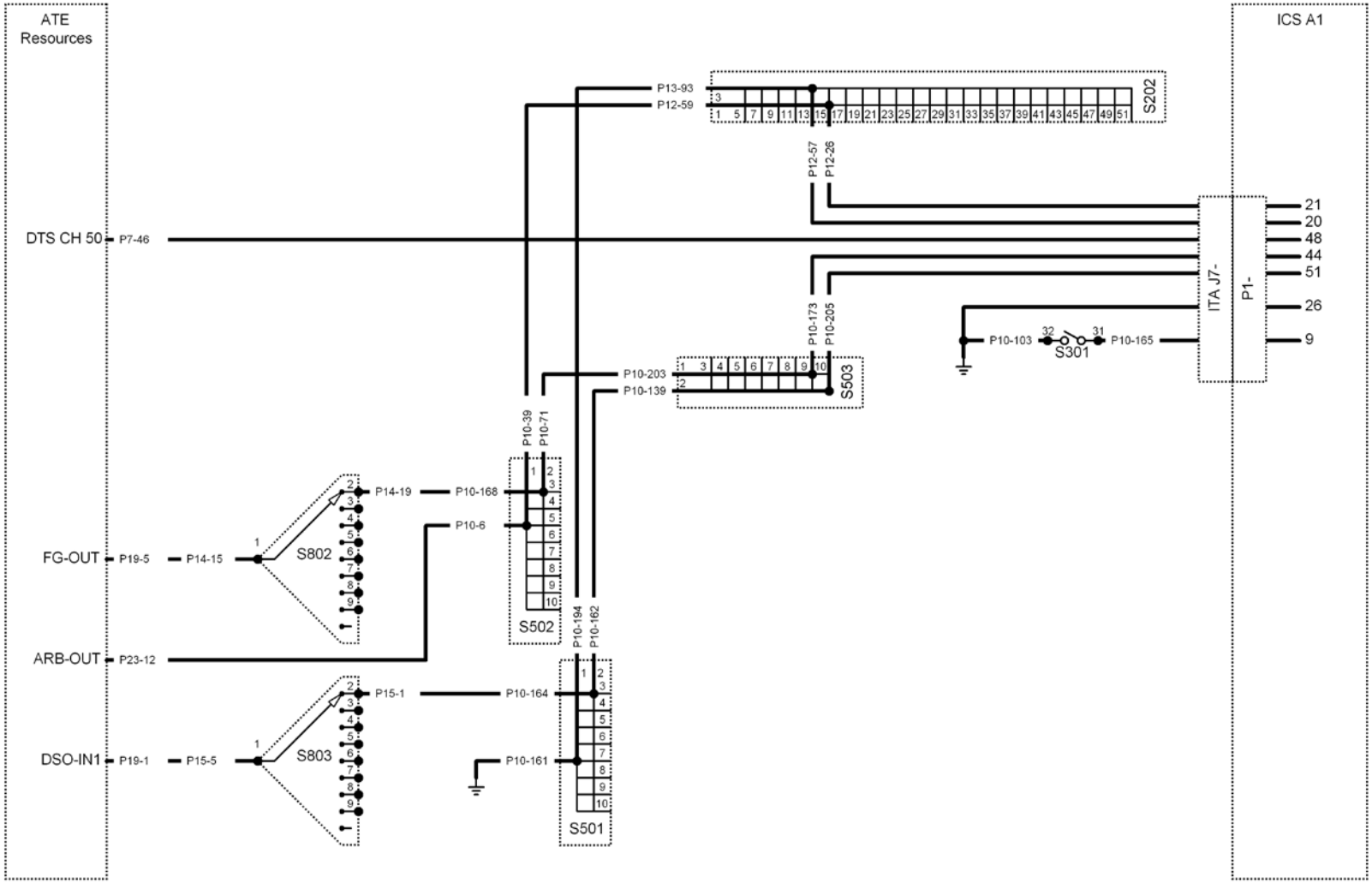
Connection Path as follows:


ATE Resources
ICS A1
DTS CH 50
P7-46
FG-OUT
P19-5
P14-15
S802
ARB-OUT
P23-12
DSO-IN1
P19-1
P15-5
S803
P14-19
P10-168
P10-6
P15-1
P10-164
P12-59
S202
P12-26
P10-39
P10-71
S502
P10-162
S501
P10-203
P10-139
P10-173
P10-205
S503
P10-103
S301
P10-165
ITA J7-
P1-
21
48
44
51
26
9

Step 403 CVSD Encoder Force-Zero Operation (PTT Disabled) Test

This step disables the PTT ENABLE input at P1-20 and verifies the DUTY-CYCLE of the CVSD Encoder output at test access pin P1-51 is 50%. Preamplifier gain select pin P1-46 is left open (HI) and the DTS is used to apply a logic LO to P1-48. A sine wave audio input of 15.0 Vpp is applied to the CREW INPUT at P1-44/9 using the Function Generator and a single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21 using the ARB. Because of the 50-ohm input impedance of the Function Generator only 7.5 Vpp is programmed, but during execution this voltage is doubled before it is applied. A GND is connected to P1-20 and the DUTY-CYCLE at P1-51 is verified using the Digitizing Oscilloscope to be 50% +/- 2%. Ten readings are taken and all are verified to be nominally 50%.

Connection Path as follows:


ATE Resources
ICS A1
DTS CH 50
P7-46
FG-OUT
P19-5
P14-15
S802
P14-19
P10-168
P10-6
ARB-OUT
P23-12
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
P10-161
S501
P10-194
P10-162
S502
P10-39
P10-71
S503
P10-173
P10-205
P10-203
P10-139
S202
P13-93
P12-59
P12-57
P12-26
P10-103
S301
P10-165
ITA J7-
P1-
21
20
48
44
51
26
9

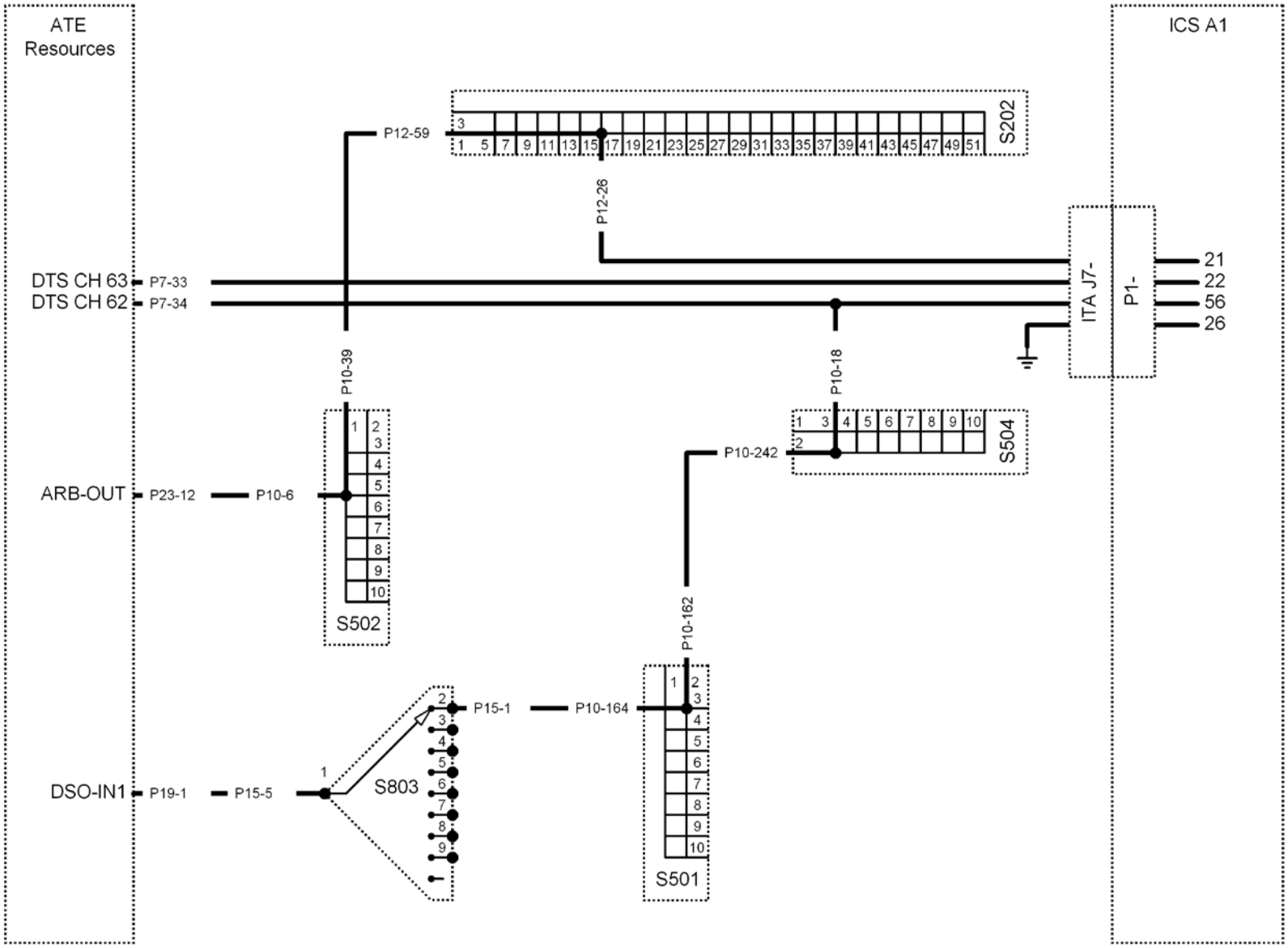
MODULE 5 CVSD LINE DRIVER TESTS

Module 5 verifies the functionality of the CVSD line driver U10 and associated circuitry at differential outputs P1-56(+)/P1-22(-).

Step 501 CVSD Digital(+) Out Amplitude Test

This step verifies the amplitude of the CVSD (+) digital output of line driver U10. A single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21 using the ARB. No audio is applied in order to generate a stable 50% Duty-Cycle output from CVSD Encoder U4. A DTS active load of 2.0V, 10mA is used to apply a nominal 170 ohm load across P1-56/P1-22. The amplitude at P1-56 is verified using the Digitizing Oscilloscope to be 2.0 to 5.0 Vpp.

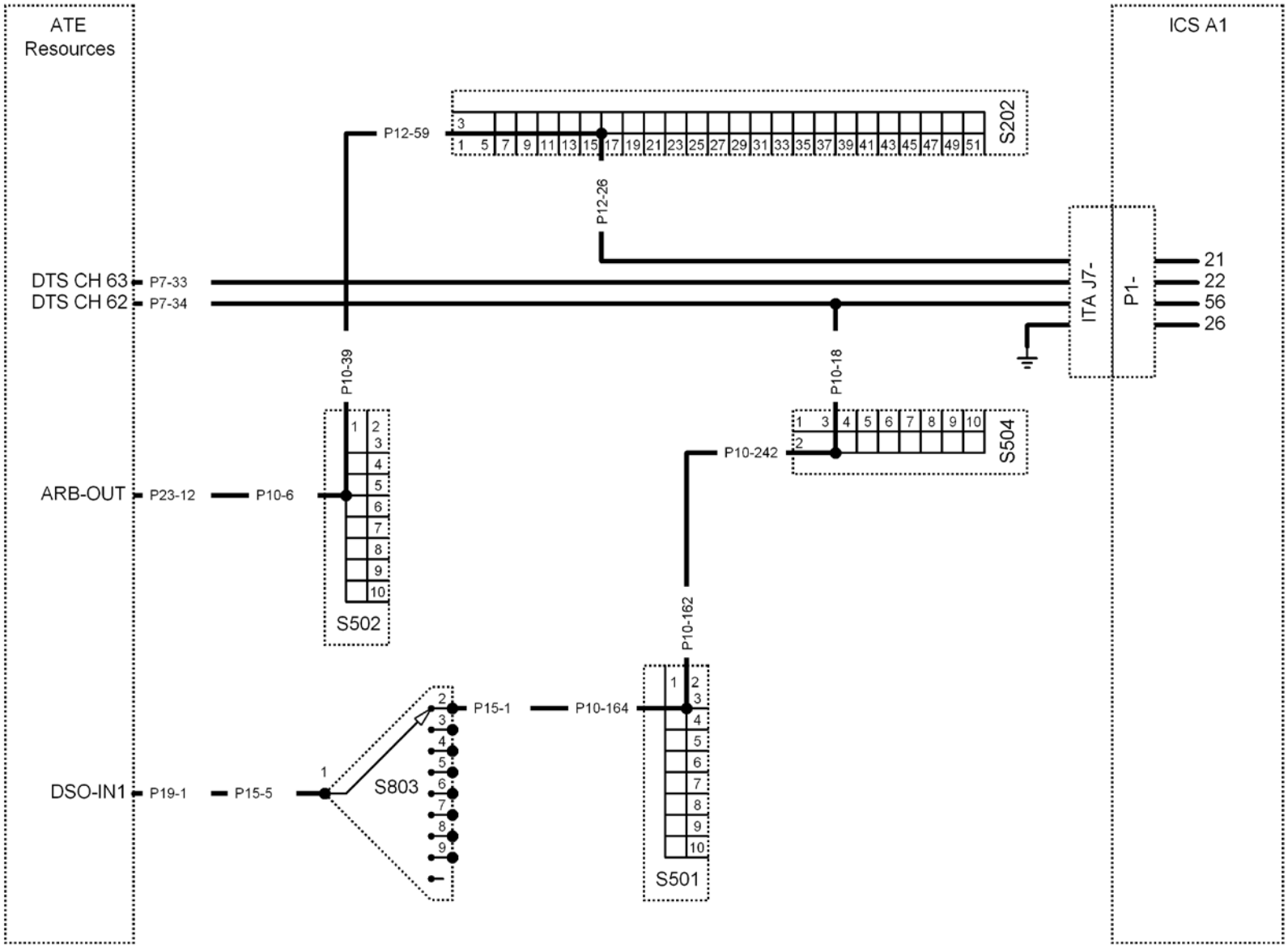
Connection Path as follows:


ATE
Resources
ICS A1
S202
P12-59
P12-26
DTS CH 63
DTS CH 62
P7-33
P7-34
ITA J7-
P1-
21
22
56
26
P10-39
P10-18
S504
P10-242
ARB-OUT
P23-12
P10-6
S502
P10-162
P15-1
P10-164
DSO-IN1
P19-1
P15-5
S803
S501

Step 502 CVSD Digital(+) Out Rise-Time Test

This step verifies the RISE-TIME of the CVSD (+) digital output of line driver U10. A single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21 using the ARB. No audio is applied in order to generate a stable 50% Duty-Cycle output from CVSD Encoder U4. A DTS active load of 2.0V, 10mA is used to apply a nominal 170 ohm load across P1-56/P1-22. The Rise-Time at P1-56 is verified using the Digitizing Oscilloscope to be > 200 nSec, which verifies C24 is not open.

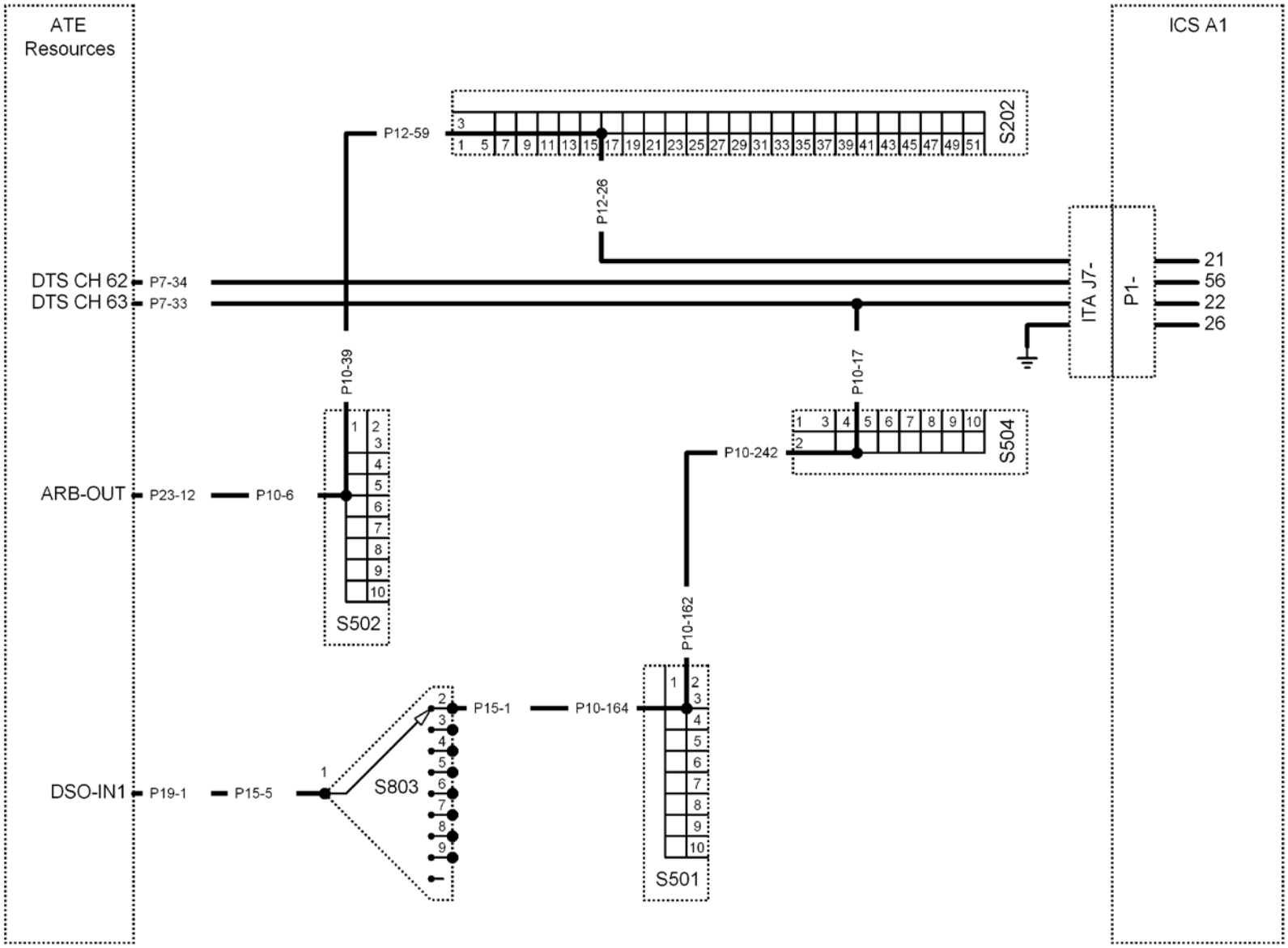
Connection Path as follows:


ATE
Resources
ICS A1
S202
P12-59
P12-26
DTS CH 63
DTS CH 62
P7-33
P7-34
ITA J7-
P1-
21
22
56
26
P10-39
P10-18
S504
P10-242
ARB-OUT
P23-12
P10-6
S502
P10-162
P15-1
P10-164
DSO-IN1
P19-1
P15-5
S803
S501

Step 503 CVSD Digital(-) Out Amplitude Test

This step verifies the amplitude of the CVSD (-) digital output of line driver U10. A single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21 using the ARB. No audio is applied in order to generate a stable 50% Duty-Cycle output from CVSD Encoder U4. A DTS active load of 2.0V, 10mA is used to apply a nominal 170 ohm load across P1-56/P1-22. The amplitude at P1-22 is verified using the Digitizing Oscilloscope to be 2.0 to 5.0 Vpp.

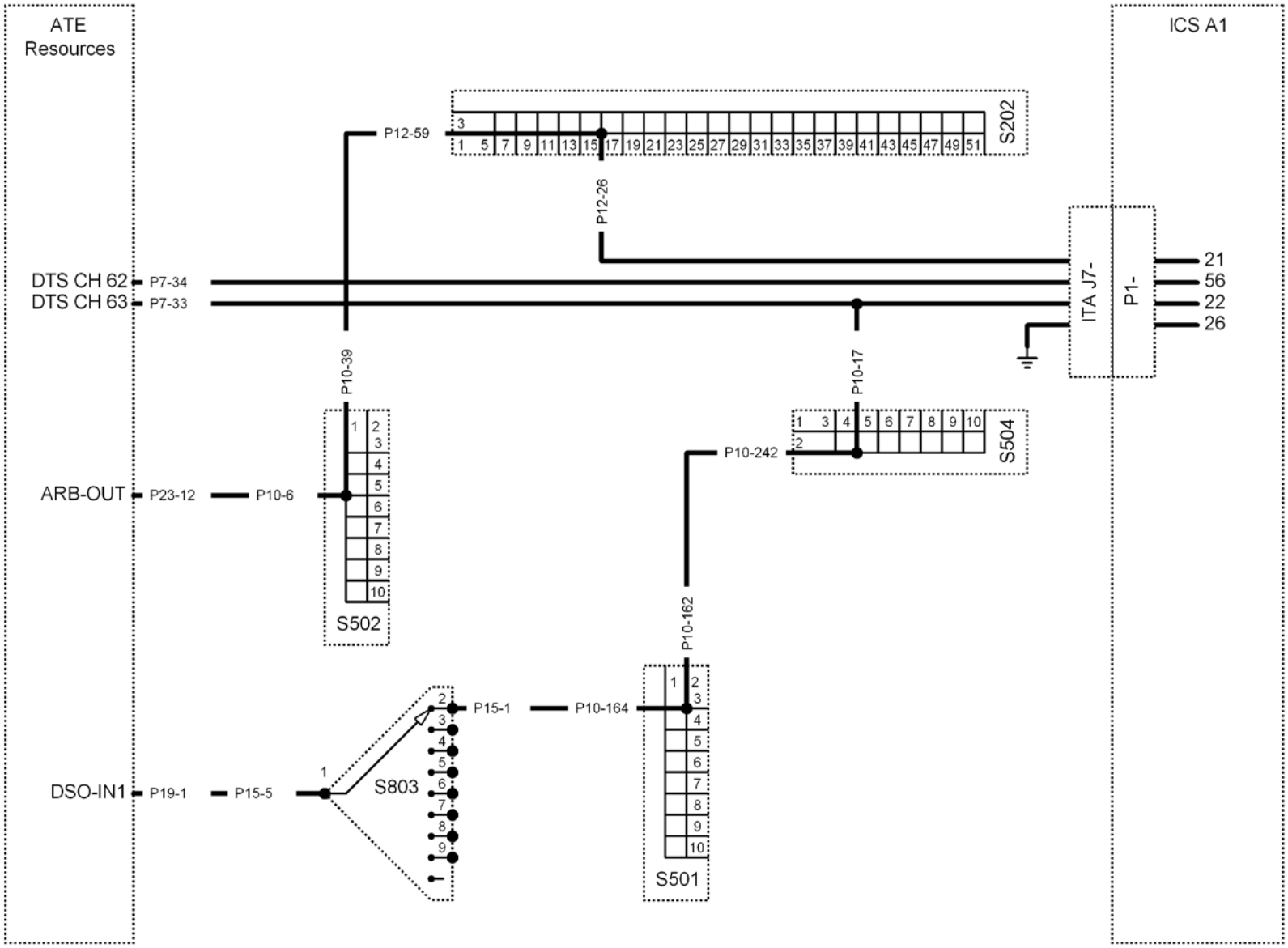
Connection Path as follows:


ATE
Resources
ICS A1
S202
P12-59
P12-26
DTS CH 62
DTS CH 63
P7-34
P7-33
ITA J7-
P1-
21
56
22
26
P10-39
P10-17
S504
P10-242
ARB-OUT
P23-12
P10-6
S502
P10-162
P15-1
P10-164
DSO-IN1
P19-1
P15-5
S803
S501

Step 504 CVSD Digital(-) Out Rise-Time Test

This step verifies the RISE-TIME of the CVSD (-) digital output of line driver U10. A single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21 using the ARB. No audio is applied in order to generate a stable 50% Duty-Cycle output from CVSD Encoder U4. A DTS active load of 2.0V, 10mA is used to apply a nominal 170 ohm load across P1-56/P1-22. The Rise-Time at P1-22 is verified using the Digitizing Oscilloscope to be > 200 nSec, which verifies C23 is not open.

Connection Path as follows:


ATE
Resources
ICS A1
S202
P12-59
P12-26
DTS CH 62
DTS CH 63
P7-34
P7-33
ITA J7-
P1-
21
56
22
26
P10-39
P10-17
S504
P10-242
ARB-OUT
P23-12
P10-6
S502
P10-162
P15-1
P10-164
DSO-IN1
P19-1
P15-5
S803
S501

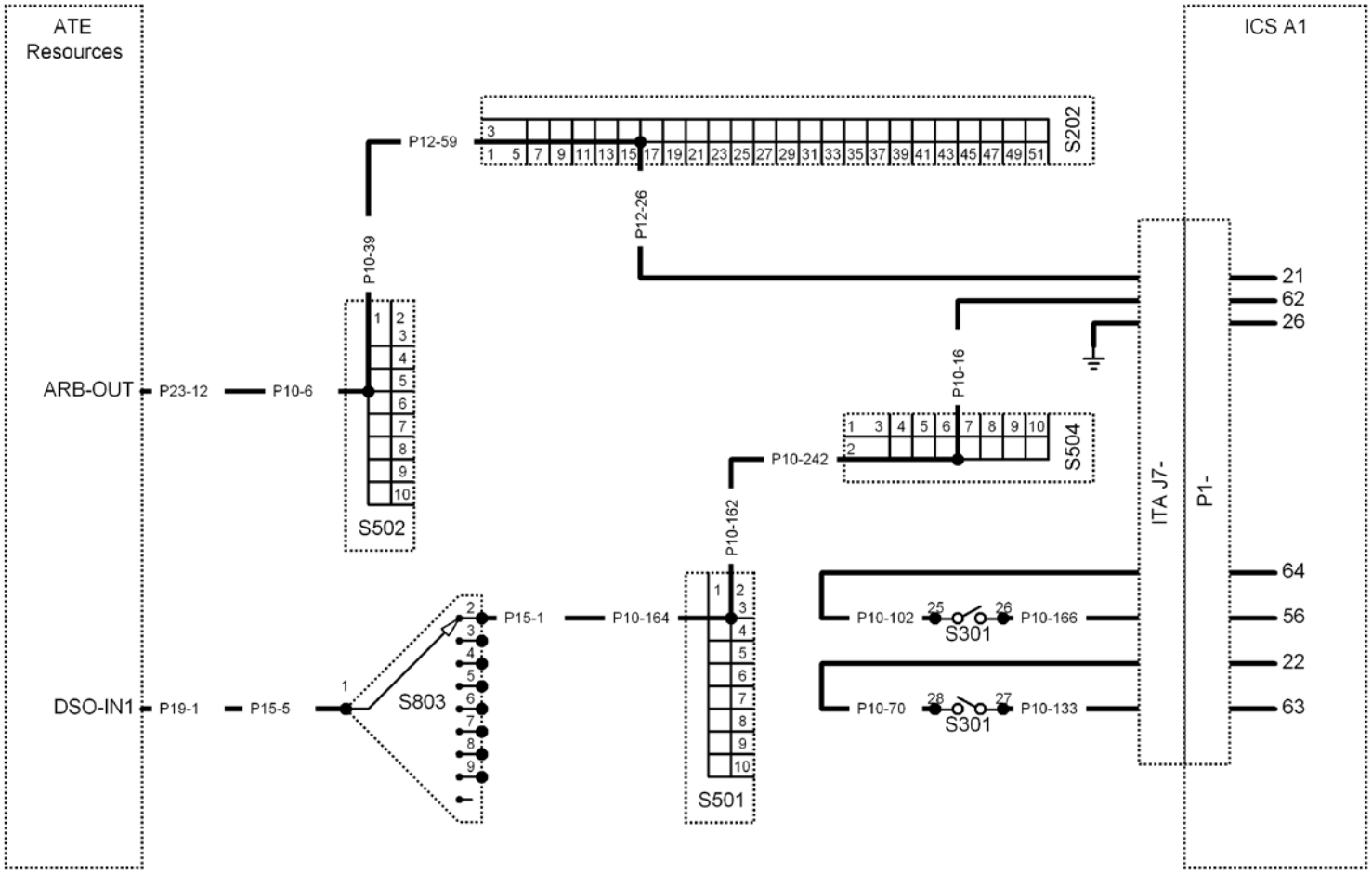
MODULE 6 CVSD LINE RECEIVER TESTS

Module 6 verifies the functionality of the CVSD line receiver U12 and associated circuitry at single-ended output P1-62.

Step 601 CVSD Line Receiver Amplitude Test

This step verifies the amplitude of the output of CVSD line receiver U12. A single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21 using the ARB. No audio is applied in order to generate a stable 50% Duty-Cycle output from CVSD Encoder U4. The CVSD differential output at P1-56/P1-22 is connected to the differential input at P1-64/P1-63. The amplitude at P1-62 is verified using the Digitizing Oscilloscope to be 4.0 to 7.0 Vpp.

Connection Path as follows:


ATE
Resources
ICS A1
ARB-OUT
P23-12
P10-6
DSO-IN1
P19-1
P15-5
P12-59
P12-26
P10-39
P10-16
P10-242
P10-162
P15-1
P10-164
P10-102
P10-166
P10-70
P10-133
S202
S502
S504
S501
S803
S301
S301
ITA J7-
P1-
21
62
26
64
56
22
63

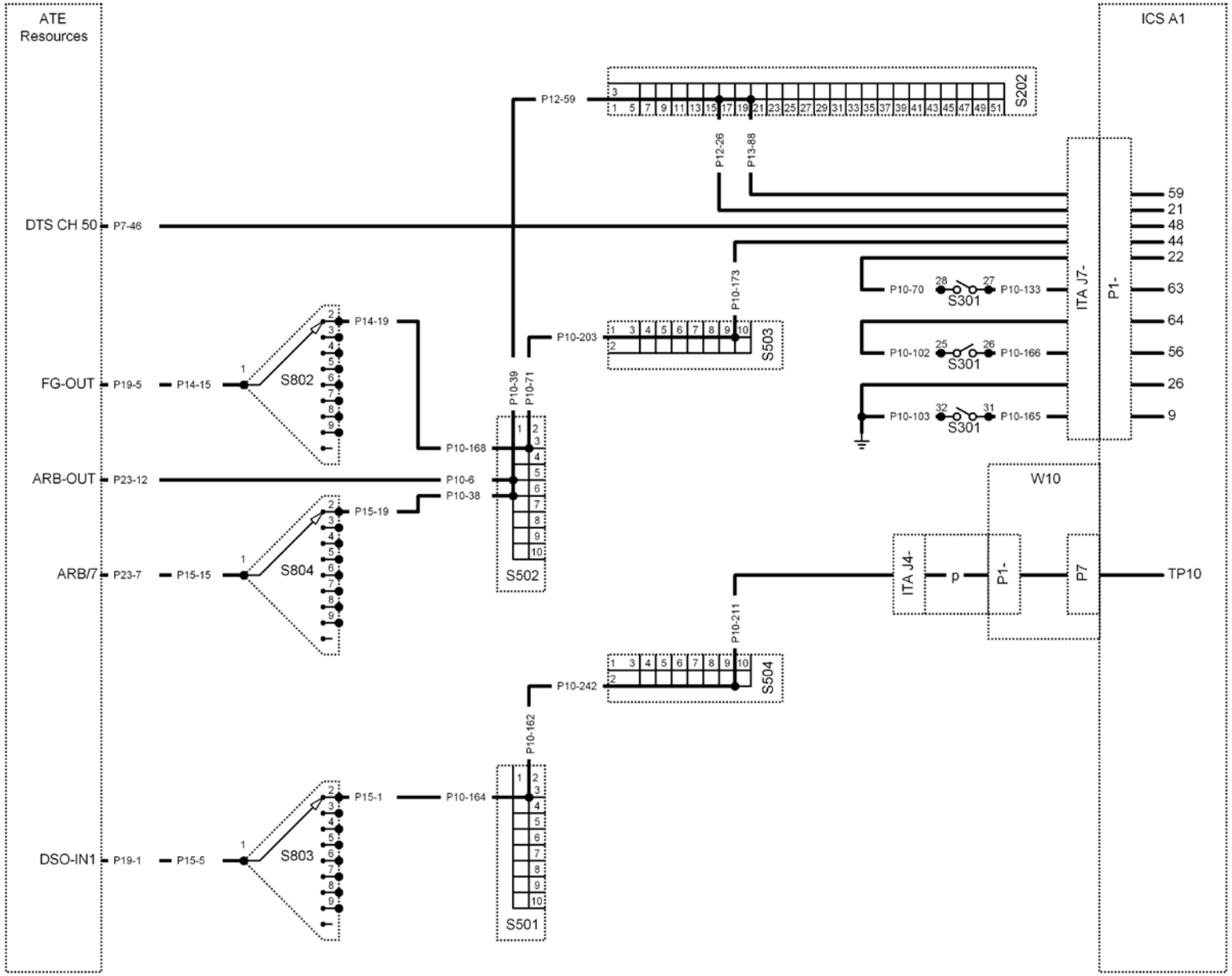
MODULE 7 CVSD DECODER TESTS

Module 7 verifies the functionality of the CVSD Decoder U6, by applying a test audio signal at T1 primary input and verifying the specified amplitude at TP10.

Step 701 CVSD Decoder Amplitude Test

This step verifies the amplitude of the output of CVSD Decoder U6. A sine wave audio input of 15.0 Vpp is applied to the CREW INPUT at P1-44/9 using the Function Generator and a single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21/P1-59 using the ARB and ARB/7 output. Because of the 50-ohm input impedance of the Function Generator only 7.5 Vpp is programmed, but during execution this voltage is doubled before it is applied. Preamplifier gain select pin P1-46 is left open (HI) and the DTS is used to apply a logic LO to P1-48. The CVSD differential output at P1-56/P1-22 is connected to the differential input at P1-64/P1-63. The amplitude at TP10 is verified using the Digitizing Oscilloscope to be 0.5 to 2.0 Vpp. The measured value is stored and used to calculate test tolerances for step 801.

Connection Path as follows:


ATE Resources
ICS A1
DTS CH 50
P7-46
FG-OUT
P19-5
P14-15
S802
P14-19
ARB-OUT
P23-12
ARB/7
P23-7
P15-15
S804
P15-19
DSO-IN1
P19-1
P15-5
S803
P15-1
P12-59
S202
P12-26
P13-88
P10-173
P10-203
S503
P10-70
P10-133
P10-102
P10-166
P10-103
P10-165
S301
ITA J7-
P1-
59
21
48
44
22
63
64
56
26
9
P10-39
P10-71
P10-168
P10-6
P10-38
S502
P10-211
P10-242
S504
P10-162
P10-164
S501
W10
ITA J4-
p
P1-
P7
TP10

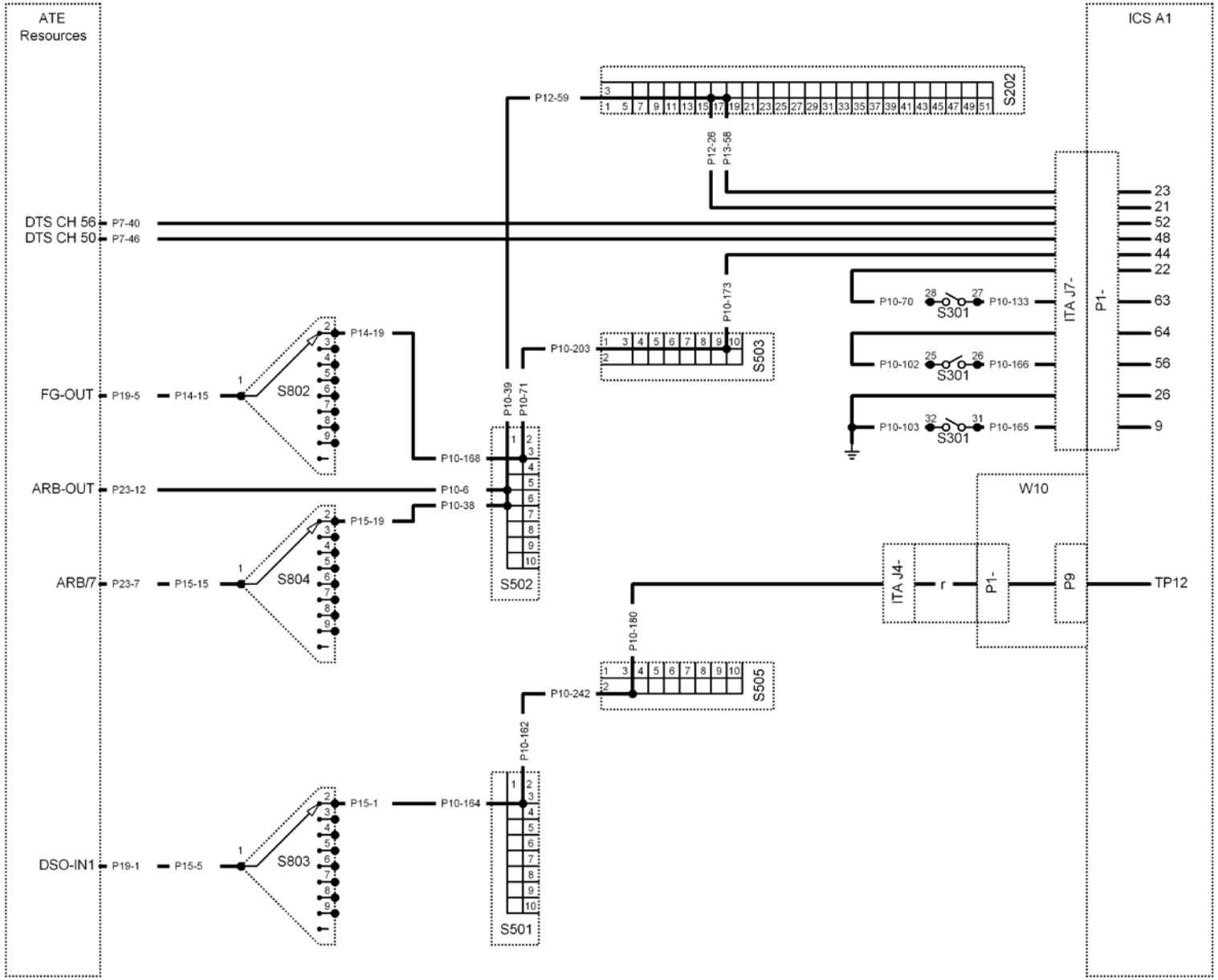
MODULE 8 DECODER FILTER TESTS

Module 8 verifies the functionality of the Decoder filter circuit built around U7, by applying a test audio signal at T1 primary input and verifying the specified amplitude at TP12 and P1-3.

Step 801 CVSD Decoder Filter/Amplifier Amplitude Test

This step verifies the amplitude of the output of the CVSD Decoder Filter circuit built around U7. A sine wave audio input of 15.0 Vpp is applied to the CREW INPUT at P1-44/9 using the Function Generator and a single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21/P1-23 using the ARB and ARB/7 output. Because of the 50-ohm input impedance of the Function Generator only 7.5 Vpp is programmed, but during execution this voltage is doubled before it is applied. Preamplifier gain select pin P1-46 is left open (HI) and the DTS is used to apply a logic LO to P1-48. The Decoder Amplifier gain is set to low by applying a logic LO at P1-52. The CVSD differential output at P1-56/P1-22 is connected to the differential input at P1-64/P1-63. The amplitude at TP12 is verified using the Digitizing Oscilloscope to be nominally 3.1, +/- 25% (the gain of U7-A with P1-52 open) times the measured amplitude at TP10 (see Step 701).

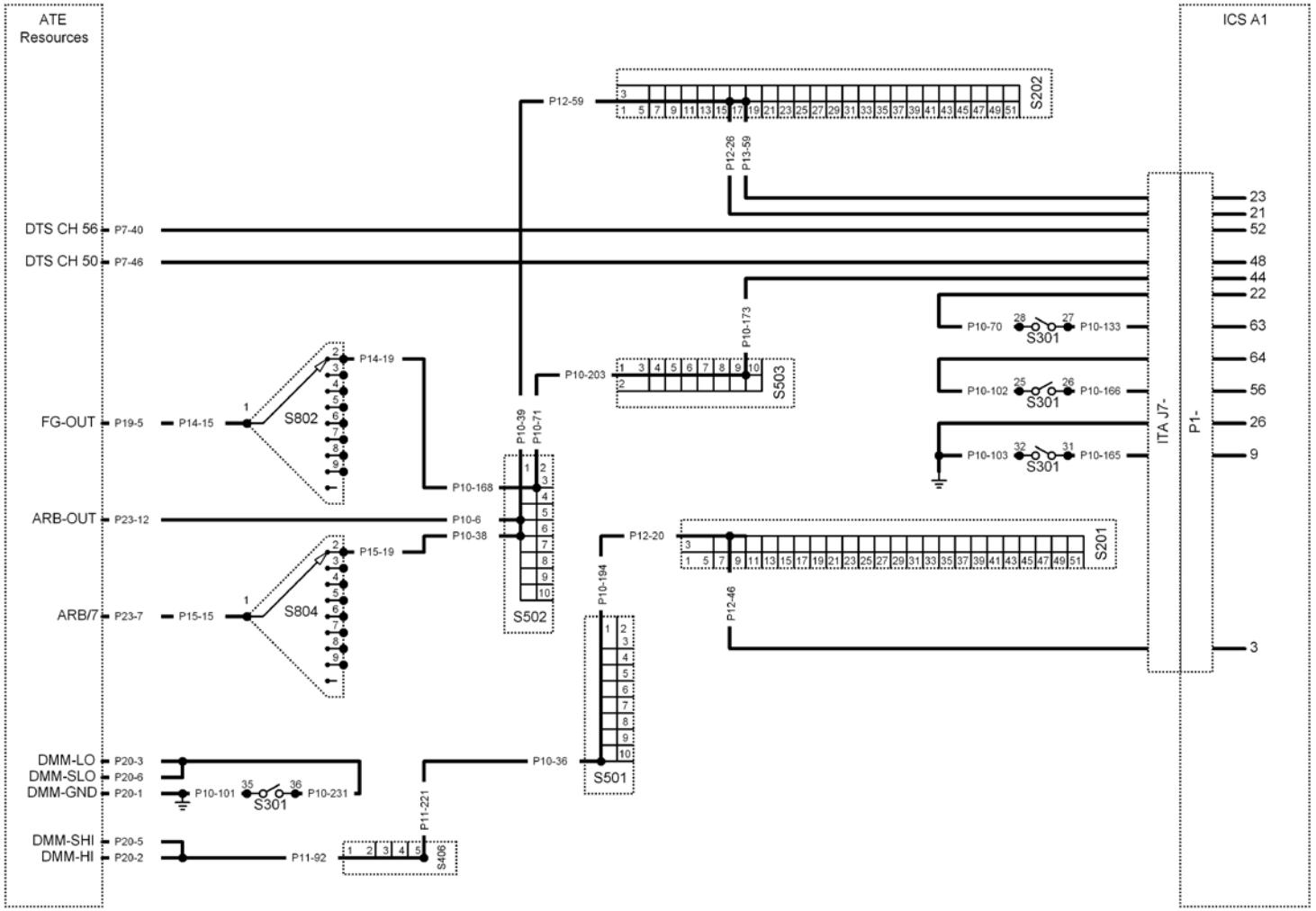
Connection Path as follows:


ATE Resources
ICS A1
DTS CH 56
DTS CH 50
P7-40
P7-46
FG-OUT
P19-5
P14-15
S802
P14-19
P10-168
ARB-OUT
P23-12
P10-6
P10-38
ARB/7
P23-7
P15-15
S804
P15-19
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
P12-59
S202
P12-26
P13-58
P10-203
S503
P10-173
P10-39
P10-71
S502
P10-242
S505
P10-180
P10-162
S501
P10-70
P10-133
S301
P10-102
P10-166
P10-103
P10-165
ITA J7-
P1-
23
21
52
48
44
22
63
64
56
26
9
W10
ITA J4-
P1-
P9
TP12

Step 802 Audio Output Amplitude Test

This step verifies that coupling capacitor C47 is not open. With the same stimulus and gain settings as applied in Step 801, the DMM is used to verify that the output level at P1-3 is nominally equal (no less 15%) to that at TP12. The lower limit is calculated in Vrms as: (('STEP_801_MEASURED-VALUE'/2) * 1/SQRT(2)) * 0.85.

Connection Path as follows:


ATE Resources
ICS A1
DTS CH 56 P7-40
DTS CH 50 P7-46
FG-OUT P19-5
ARB-OUT P23-12
ARB/7 P23-7
DMM-LO P20-3
DMM-SLO P20-6
DMM-GND P20-1
DMM-SHI P20-5
DMM-HI P20-2
P14-15
P15-15
P10-101
P10-231
P11-92
S802
S804
S301
S406
P14-19
P15-19
P10-168
P10-6
P10-38
P10-39
P10-71
S502
P10-203
S503
P10-173
P12-59
S202
P12-26
P13-59
P10-70
P10-133
P10-102
P10-166
P10-103
P10-165
P12-20
S201
P12-46
P10-194
S501
P10-36
P11-221
ITA J7-
P1-
23
21
52
48
44
22
63
64
56
26
9
3

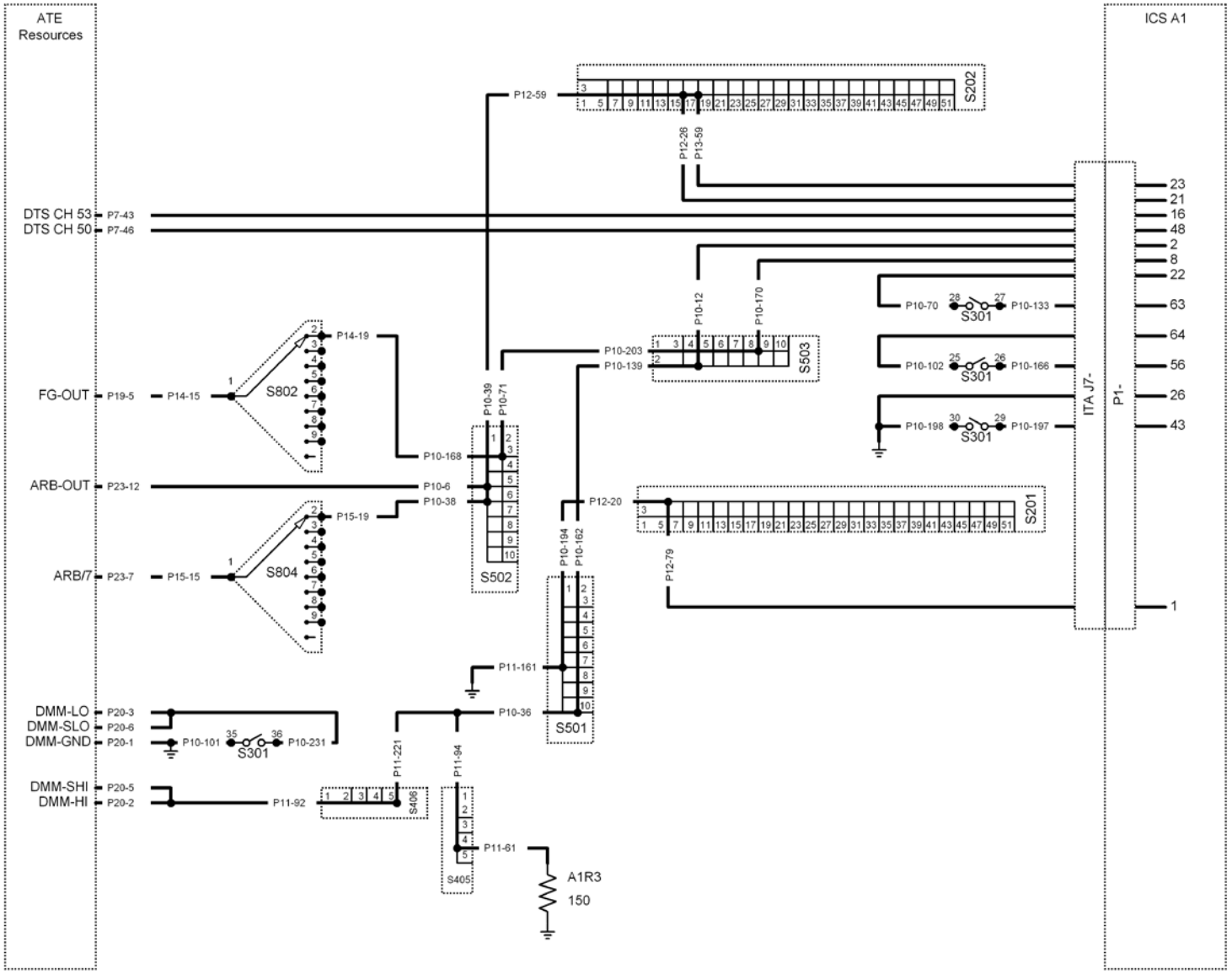
MODULE 9 RADIO OUTPUT TESTS

Module 9 verifies the correct amplitude at balanced audio output of T2, by applying a test audio signal at T1 primary input and verifying the specified amplitude across T2 secondary output.

Step 901 Balanced Output Amplitude Test

This step verifies the amplitude of the balanced output of transformer T2. A sine wave audio input of 10.0 Vpp is applied to the RADIO INPUT at P1-8/43 using the Function Generator and a single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21/P1-23 using the ARB and ARB/7 output. Because of the 50-ohm input impedance of the Function Generator only 5.0 Vpp is programmed, but during execution this voltage is doubled before it is applied. Preamplifier gain select pin P1-46 is left open (HI) and the DTS is used to apply a logic LO to P1-48 and MIC OUT LEVEL control, P1-16 to select HI-Level audio out. The CVSD differential output at P1-56/P1-22 is connected to the differential input at P1-64/P1-63. The amplitude at P1-2 with a 150 ohm load connected across T2 secondary is verified using the DMM to be at least 5.6 mVAC. The measured value is stored and used to calculate test tolerances for step 902.

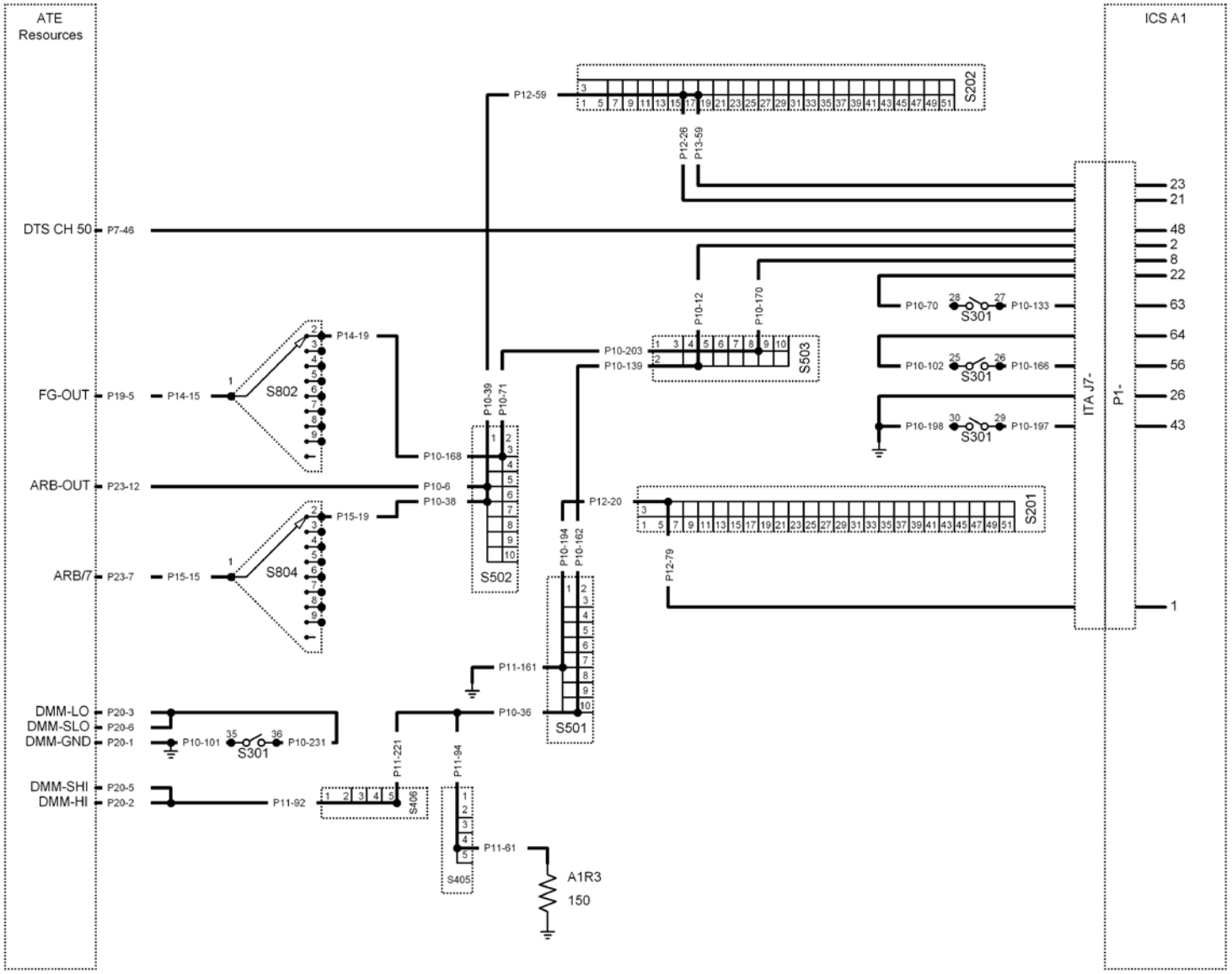
Connection Path as follows:


ATE Resources
ICS A1
DTS CH 53 P7-43
DTS CH 50 P7-46
FG-OUT P19-5
ARB-OUT P23-12
ARB/7 P23-7
DMM-LO P20-3
DMM-SLO P20-6
DMM-GND P20-1
DMM-SHI P20-5
DMM-HI P20-2
S802
S804
S202
S201
S503
S502
S501
S301
S406
S405
P12-59
P12-26
P13-59
P14-19
P14-15
P15-19
P15-19
P10-6
P10-38
P10-168
P10-39
P10-71
P10-203
P10-139
P10-12
P10-170
P10-70
P10-133
P10-102
P10-166
P10-198
P10-197
P12-20
P12-79
P10-194
P10-162
P11-161
P10-36
P10-101
P10-231
P11-221
P11-94
P11-92
P11-61
A1R3
150
ITA J7-
P1-
23
21
16
48
2
8
22
63
64
56
26
43
1

Step 902 Microphone Level Control Test

This step verifies the MIC OUT LEVEL control is functional. The same test stimulus is applied as in Step 901. MIC OUT LEVEL control, P1-16 is left open to select LO-Level audio out. The CVSD differential output at P1-56/P1-22 is connect to the differential input at P1-64/P1-63. The amplitude at P1-2 with a 150 ohm load connected across T2 secondary is verified using the DMM to be less than 50% of that measured previously in step 901 with P1-16 set to LO.

Connection Path as follows:


ATE Resources
ICS A1
DTS CH 50
P7-46
FG-OUT
P19-5
P14-15
S802
P14-19
ARB-OUT
P23-12
P10-6
P10-38
ARB/7
P23-7
P15-15
S804
P10-168
S502
P10-39
P10-71
P12-59
S202
P12-26
P13-59
P10-12
P10-170
P10-203
P10-139
S503
P10-70
P10-133
P10-102
P10-166
P10-198
P10-197
S301
ITA J7-
P1-
23
21
48
2
8
22
63
64
56
26
43
1
P12-20
S201
P12-79
P10-194
P10-162
S501
P11-161
P10-36
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-101
P10-231
P11-221
P11-94
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
S406
S405
P11-61
A1R3
150

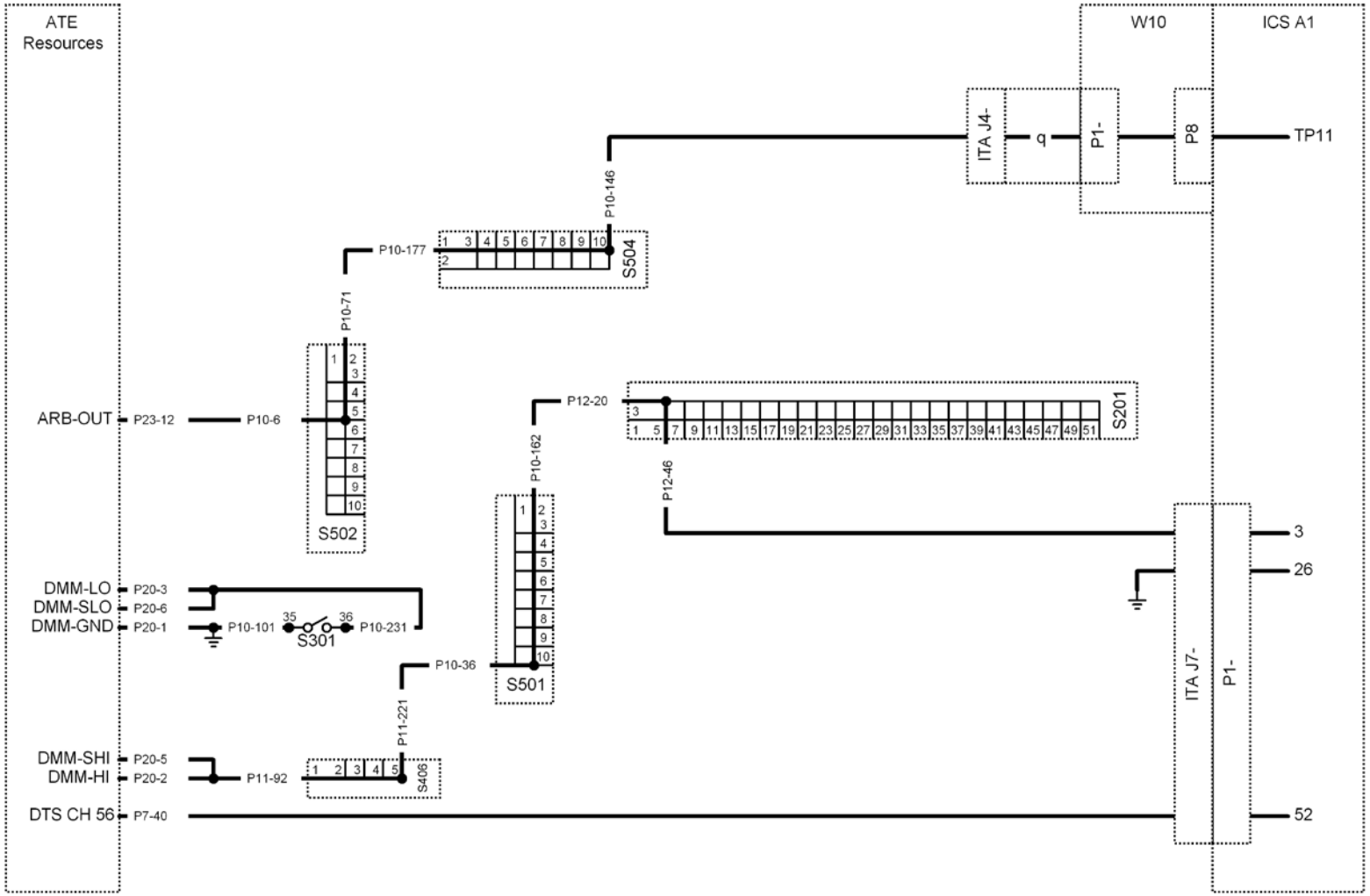
MODULE 10 DECODER FILTER RESPONSE AND LOOPBACK TESTS

Module 10 verifies the frequency response of the Decoder filter circuit built around U7. A test audio signal is applied at TP11 at the required test frequencies for the test being performed and the resultant output is measured at P1-3.

Step 1001 Filter Bandpass at 3 KHz Test

This step verifies the low-pass filter circuit frequency response at the upper end of the band at 3.0 KHz. The ARB, using the ARBNAM running file 'SineOffs-1KHz.Arb', is used to apply a 1.0 KHz sine wave, offset to +6VDC using ARB segment file 'SineOffs.Seg' (required due to the effect of R41) at TP11 and a reference reading is taken at P1-3. Then the ARB frequency is changed to 3.0 KHz using ARBNAM file SineOffs-3KHz.Arb and the output voltage at P1-3 is verified to be no less than 0.707 times the 1 KHz reference value (no more than 1/2 power, or 3dB down). The DTS is used to apply a logic LO at P1-52 to select maximum decoder amplifier gain. The DMM is used for both measurements.

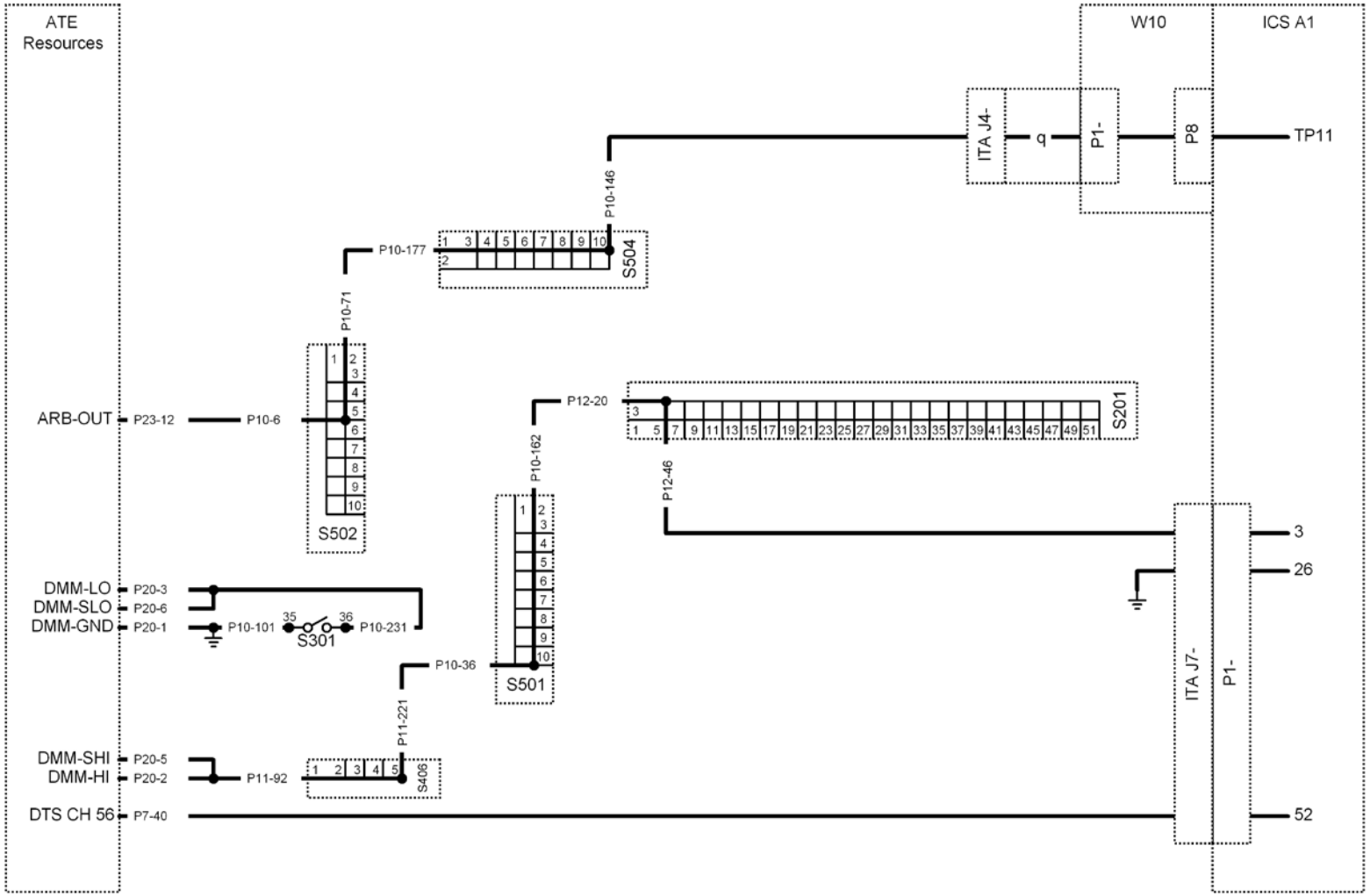
Connection Path as follows:


ATE Resources
W10
ICS A1
ITA J4-
q
P1-
P8
TP11
P10-146
P10-177
S504
P10-71
S502
ARB-OUT
P23-12
P10-6
P12-20
S201
P10-162
P12-46
S501
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-101
S301
P10-231
P10-36
P11-221
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
S406
DTS CH 56
P7-40
ITA J7-
P1-
3
26
52

Step 1002 Filter Bandpass at 4 KHz Test

This step verifies the low-pass filter circuit frequency response at 4.0 KHz. The ARB, using the ARBNAM running file 'SineOffs-1KHz.Arb', is used to apply a 1.0 KHz sine wave, offset to +6VDC using ARB segment file ‘SineOffs.Seg’ (required due to the effect of R41) at TP11 and a reference reading is taken at P1-3. Then the ARB frequency is changed to 4.0 KHz using ARBNAM file SineOffs-4KHz.Arb and the output voltage at P1-3 is verified to be no greater than 0.707 times the 1 KHz reference value (at least 1/2 power, or 3dB down). The DTS is used to apply a logic LO at P1-52 to select maximum decoder amplifier gain. The DMM is used for both measurements.

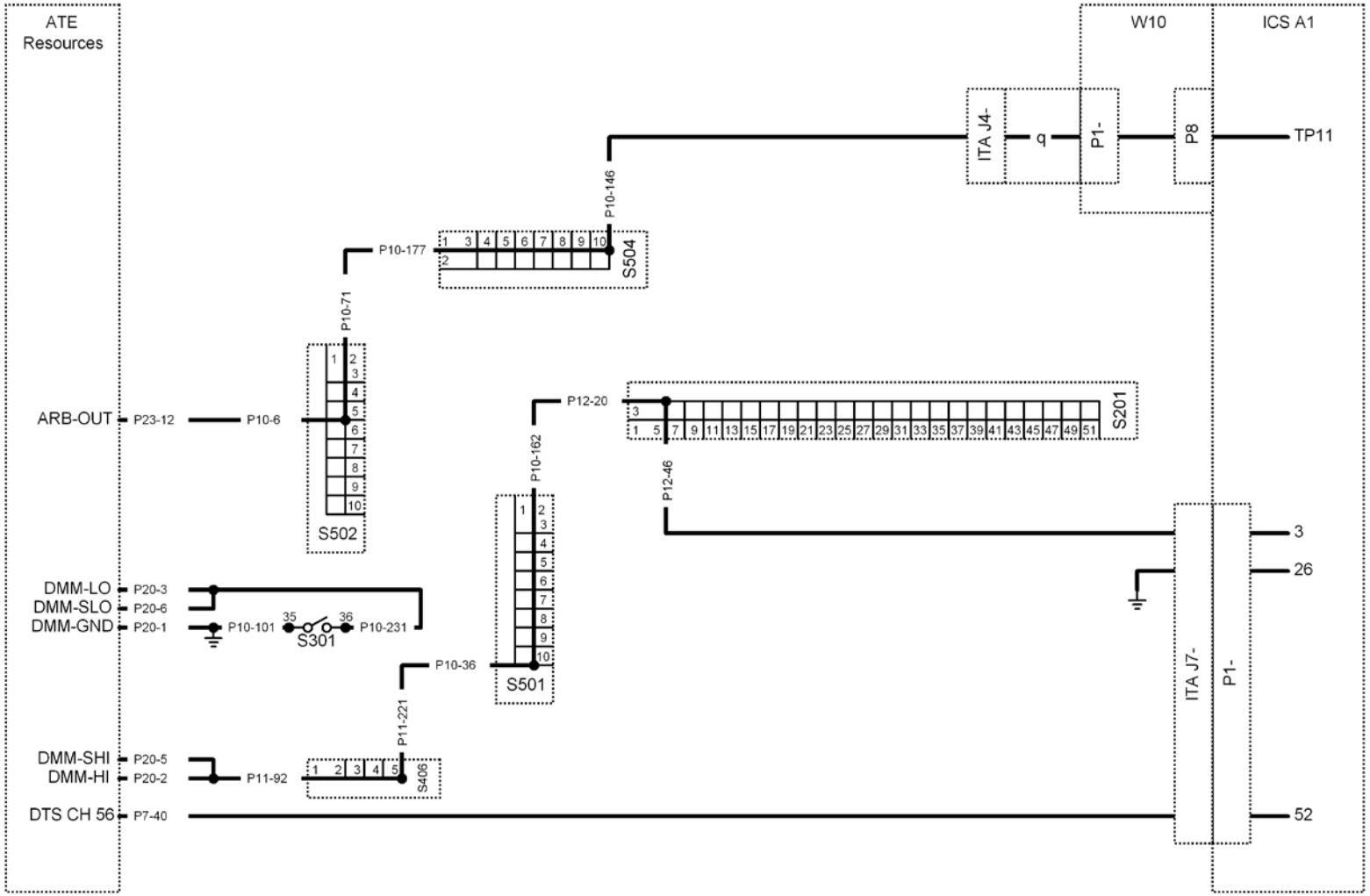
Connection Path as follows:


ATE Resources
W10
ICS A1
ITA J4-
q
P1-
P8
TP11
P10-146
P10-177
S504
P10-71
S502
ARB-OUT
P23-12
P10-6
P12-20
S201
P10-162
P12-46
S501
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-101
S301
P10-231
P10-36
P11-221
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
S406
DTS CH 56
P7-40
ITA J7-
P1-
3
26
52

Step 1003 Flatness at 150 Hz Test

This step verifies the high-pass filter circuit frequency response at 150 Hz. The ARB, using the ARBNAM running file 'SineOffs-1KHz.Arb', is used to apply a 1.0 KHz sine wave, offset to +6VDC using ARB segment file ‘SineOffs.Seg’ (required due to the effect of R41) at TP11 and a reference reading is taken at P1-3. Then the ARB frequency is changed to 150 Hz using ARBNAM file SineOffs-150Hz.Arb and the output voltage at P1-3 is verified to be no less than 0.707 times the 1 KHz reference value (no more than 1/2 power, or 3dB down). The DTS is used to apply a logic LO at P1-52 to select maximum decoder amplifier gain. The DMM is used for both measurements.

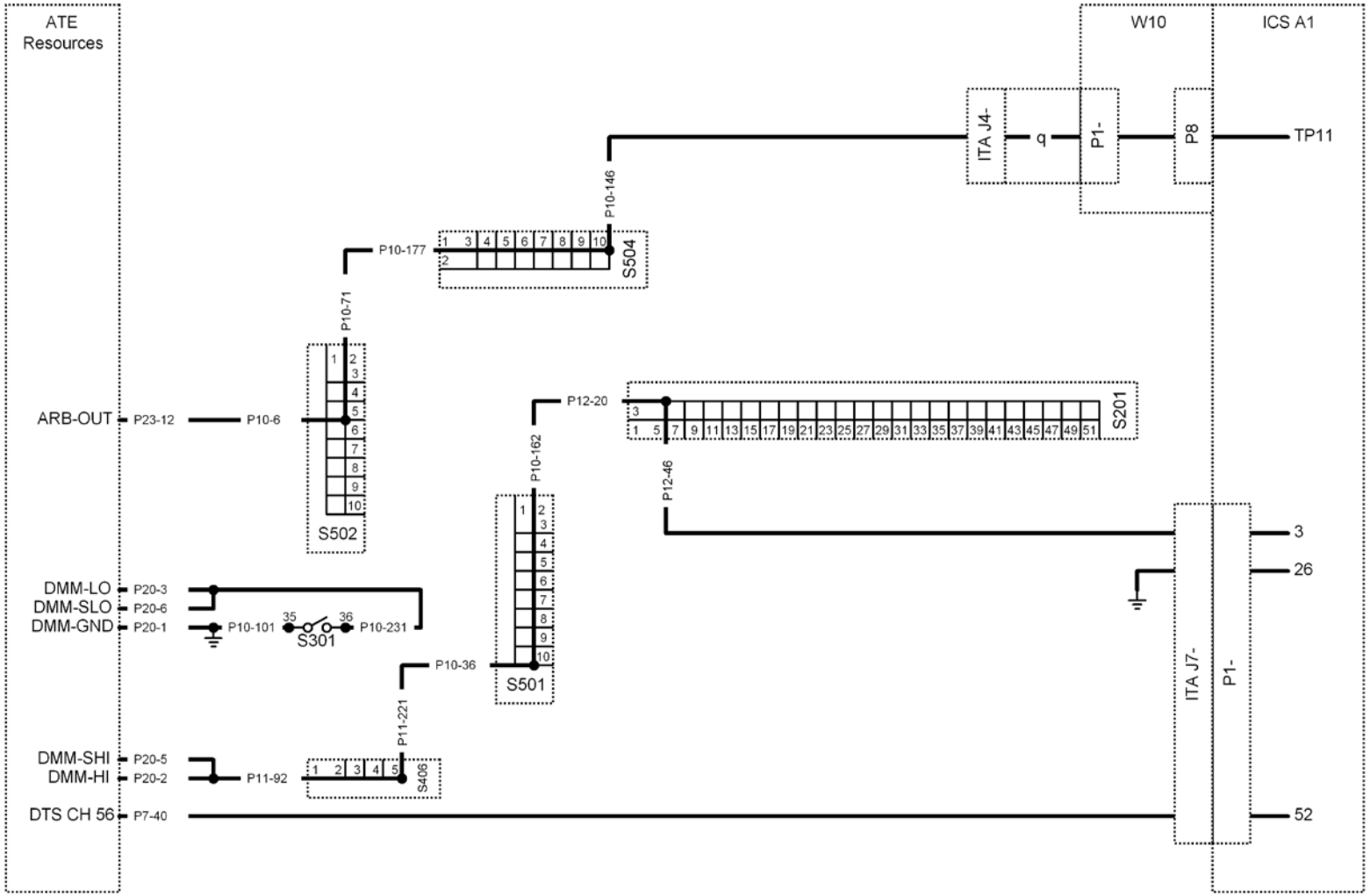
Connection Path as follows:


ATE Resources
W10
ICS A1
ITA J4-
q
P1-
P8
TP11
P10-146
P10-177
S504
P10-71
S502
ARB-OUT
P23-12
P10-6
P12-20
S201
P10-162
P12-46
S501
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-101
S301
P10-231
P10-36
P11-221
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
S406
DTS CH 56
P7-40
ITA J7-
P1-
3
26
52

Step 1004 Flatness at 3 KHz Test

This step verifies the high-pass filter circuit frequency response at 3kHz. The ARB, using the ARBNAM running file 'SineOffs-1KHz.Arb', is used to apply a 1.0 KHz sine wave, offset to +6VDC using ARB segment file ‘SineOffs.Seg’ (required due to the effect of R41) at TP11 and a reference reading is taken at P1-3. Then the ARB frequency is changed to 3.0 kHz using ARBNAM file SineOffs-3KHz.Arb and the output voltage at P1-3 is verified to be no less than 0.707 times the 1 KHz reference value (no more than 1/2 power, or 3dB down). The DTS is used to apply a logic LO at P1-52 to select maximum decoder amplifier gain. The DMM is used for both measurements.

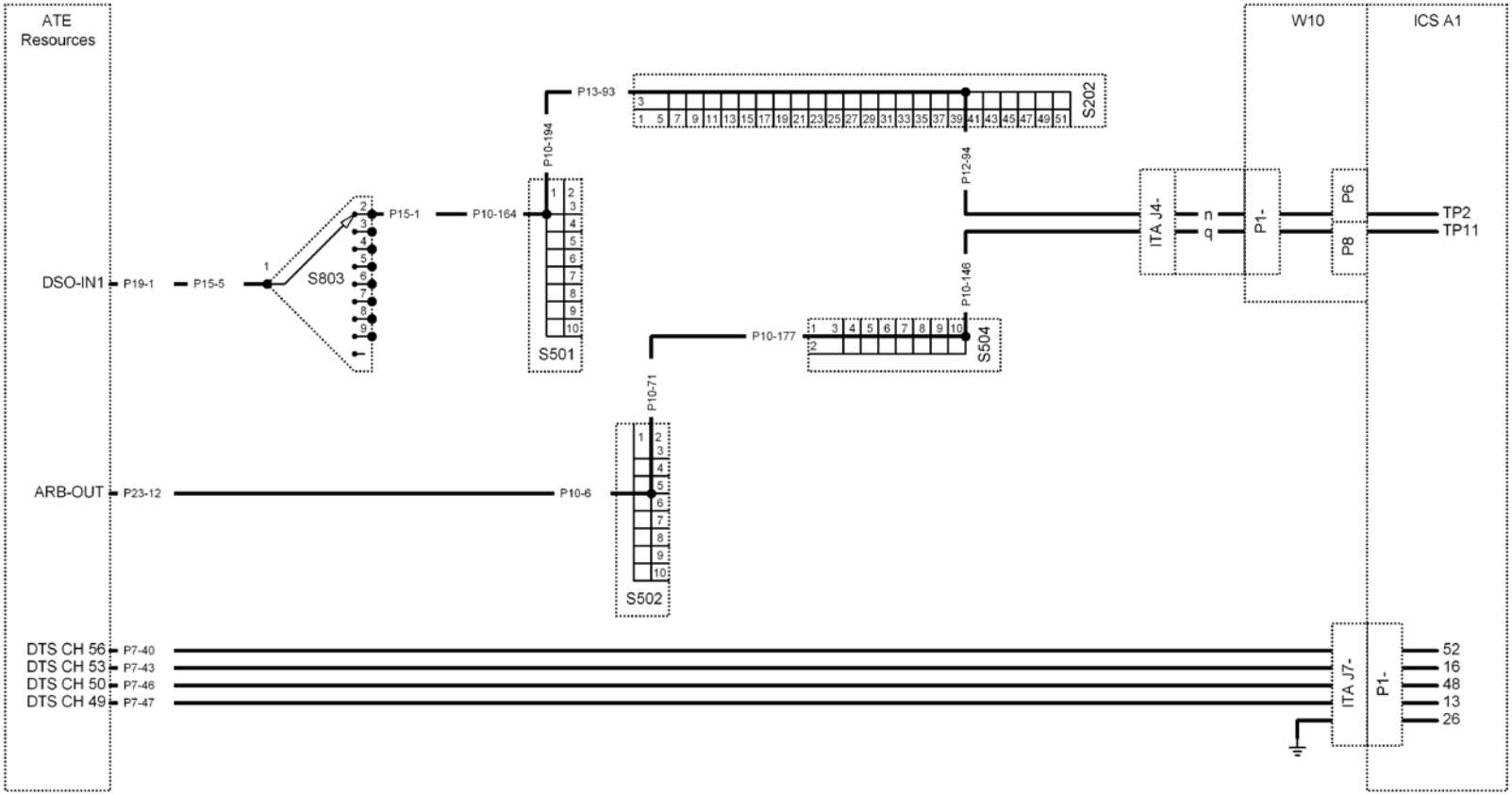
Connection Path as follows:


ATE Resources
W10
ICS A1
ITA J4-
q
P1-
P8
TP11
P10-146
P10-177
S504
P10-71
S502
ARB-OUT
P23-12
P10-6
P12-20
S201
P10-162
P12-46
S501
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-101
S301
P10-231
P10-36
P11-221
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
S406
DTS CH 56
P7-40
ITA J7-
P1-
3
26
52

Step 1005 Loopback ON Test

This step verifies the functionality of the CVSD Loopback switch (U5-1/2) and control (U8). The ARB, using the ARBNAM running file 'SineOffs-1KHz.Arb', is used to apply a 1.0 KHz sine wave, offset to +6VDC using ARB segment file ‘SineOffs.Seg’ (required due to the effect of R41) at TP11. The DTS is used to put the UUT in loopback mode by applying a logic HI at P1-13. Pre-amplifier and Decoder-Amplifier gain is set by applying a logic LO at P1-48 and P1-16/P1-52, respectively. The Digitizing Oscilloscope is used to verify greater than 0.05 Vpp at TP2, indicating the decoder output has been looped back to the pre-amplifier input. The measured value is stored and used to calculate test tolerances for step 1006.

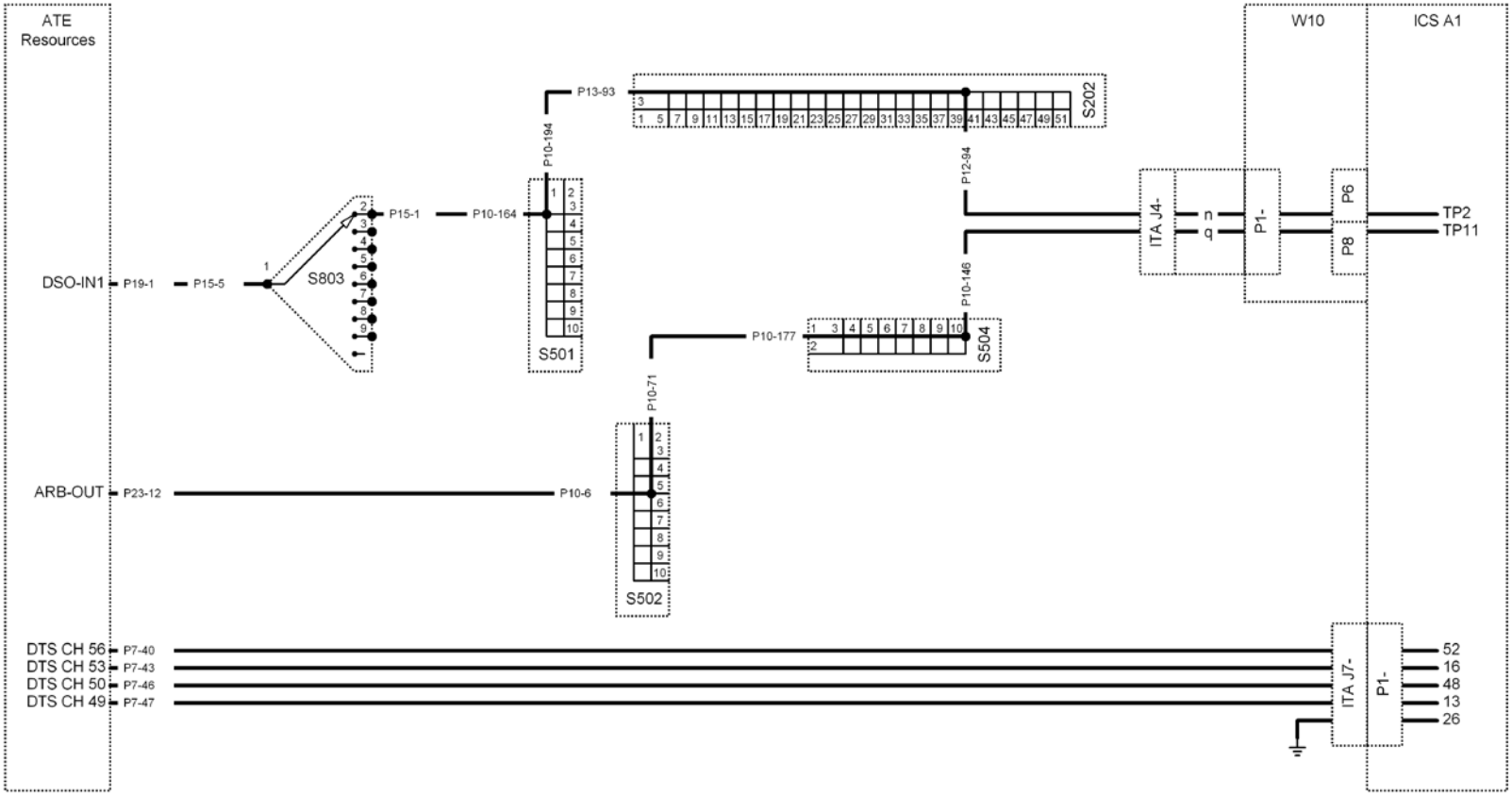
Connection Path as follows:


ATE
Resources
W10
ICS A1
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
S501
P10-194
P13-93
S202
P12-94
P10-146
S504
P10-177
ITA J4-
n
q
P1-
P6
P8
TP2
TP11
P10-71
S502
ARB-OUT
P23-12
P10-6
DTS CH 56
DTS CH 53
DTS CH 50
DTS CH 49
P7-40
P7-43
P7-46
P7-47
ITA J7-
P1-
52
16
48
13
26

Step 1006 Loopback OFF Test

This step verifies the CVSD Loopback switch (U5-1/2) is not stuck in the closed (loopback) position. The ARB, using the ARBNAM running file 'SineOffs-1KHz.Arb', is used to apply a 1.0 KHz sine wave, offset to +6VDC using ARB segment file 'SineOffs.Seg' (required due to the effect of R41) at TP11. Pre-amplifier and Decoder-Amplifier gain is set by applying a logic LO at P1-48 and P1-16/P1-52, respectively. With no CVSD LOOPBACK input (logic HI) applied at P1-13, the Digitizing Oscilloscope is used to verify the amplitude at TP2 to be no greater than 30% of the value measured in Step 1005.

Connection Path as follows:


ATE
Resources
W10
ICS A1
DSO-IN1
P19-1
P15-5
S803
P15-1
P10-164
P10-194
S501
P13-93
S202
P12-94
P10-146
P10-177
S504
P10-71
S502
ARB-OUT
P23-12
P10-6
ITA J4-
n
q
P1-
P6
P8
TP2
TP11
DTS CH 56
DTS CH 53
DTS CH 50
DTS CH 49
P7-40
P7-43
P7-46
P7-47
ITA J7-
P1-
52
16
48
13
26

MODULE 11 OVERALL ENCODER/DECODER PERFORMANCE TESTS

Module 11 verifies the overall gain flatness (frequency response) of the UUT with a test audio signal applied at T1 primary swept across the UUT frequency band of 400 Hz to 2.5 KHz.

Step 1101 Flatness (400 Hz to 2.5 KHz) Test

This step verifies that the gain of the complete audio path is flat (within 3 dB) across the specified band of 400 Hz to 2.5 KHz. A sine wave audio input of 10.0 Vpp is applied to the RADIO INPUT at P1-8/43 using the Function Generator and a single-ended TTL level 32 KHz square wave CLOCK signal is applied at P1-21/P1-23 using the ARB and ARB/7 output. Because of the 50-ohm input impedance of the Function Generator only 5.0 Vpp is programmed, but during execution this voltage is doubled before it is applied. Amplifier gain is set to maximum by using the DTS to apply a logic LO at P1-16, P1-48, and P1-52. The CVSD differential output at P1-56/P1-22 is connected to the differential input at P1-64/P1-63. The audio input signal frequency is swept from 400 Hz to 2.5 KHz in 100 Hz increments. The DMM is used to measure the audio amplitude output at TP12. The amplitude at each frequency is stored. The procedure then locates the highest amplitude (Vmax) point and the lowest amplitude (Vmin) point. Overall flatness (in decibels) is calculated by the formula: 20*Log(Vmax/Vmin) and verified to be less than 3.5 dB.

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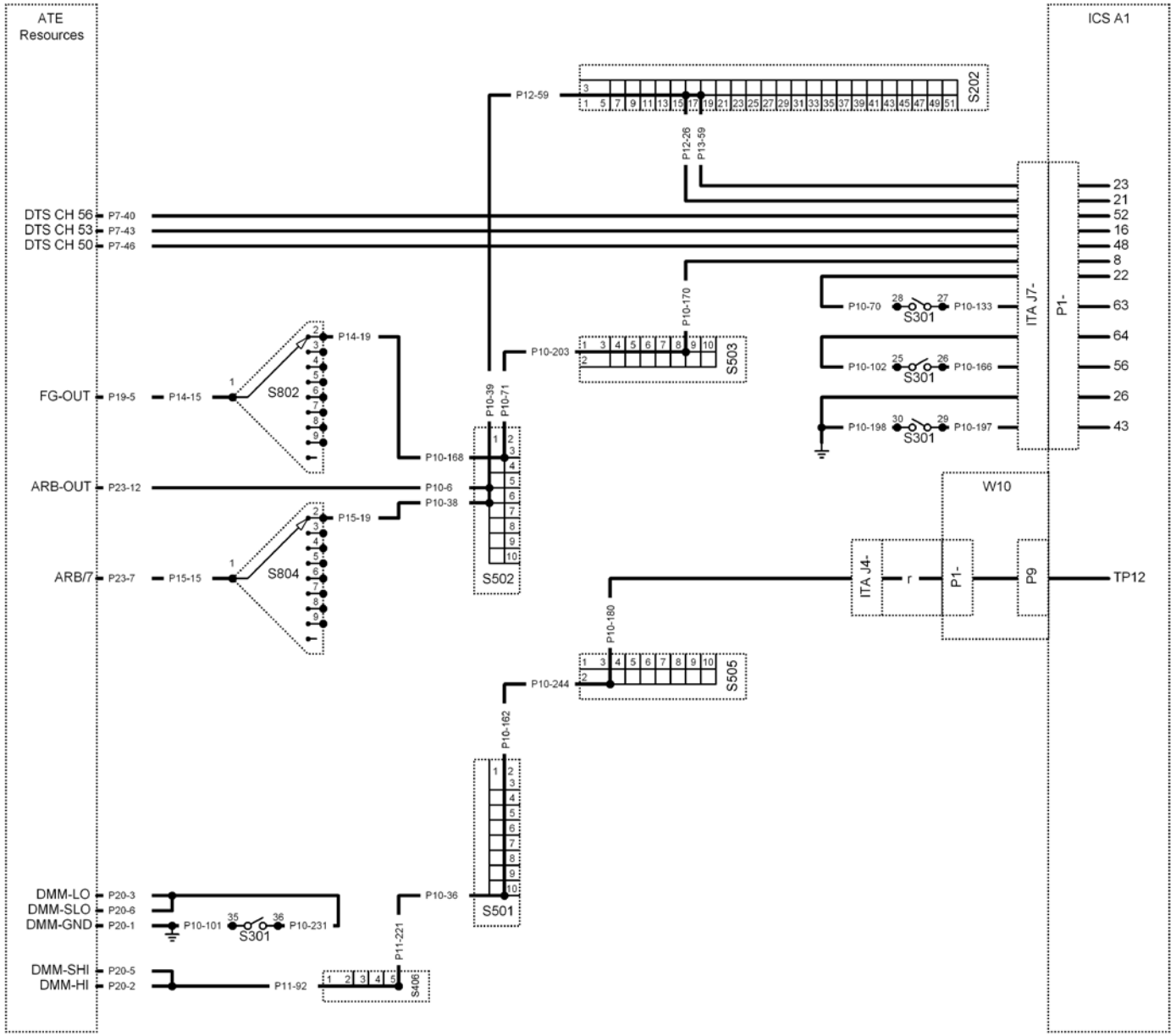
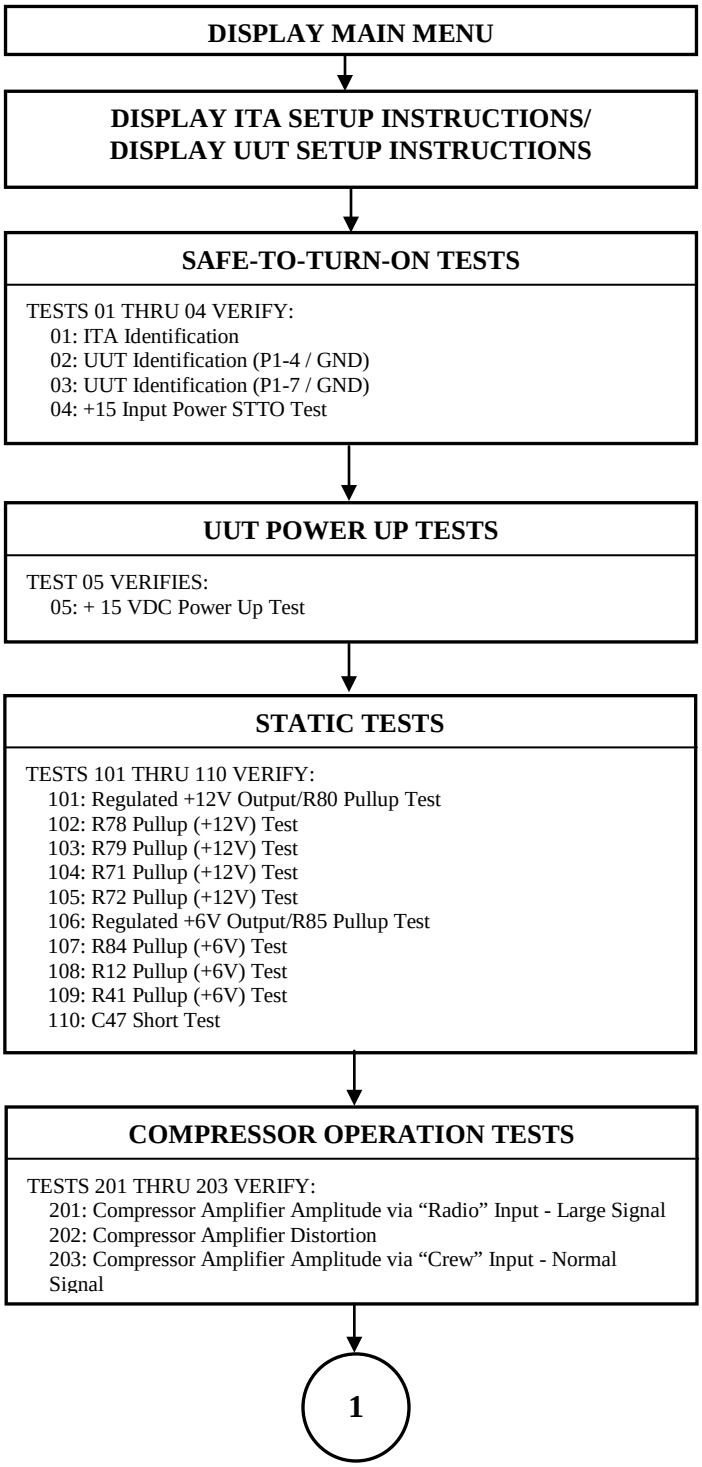
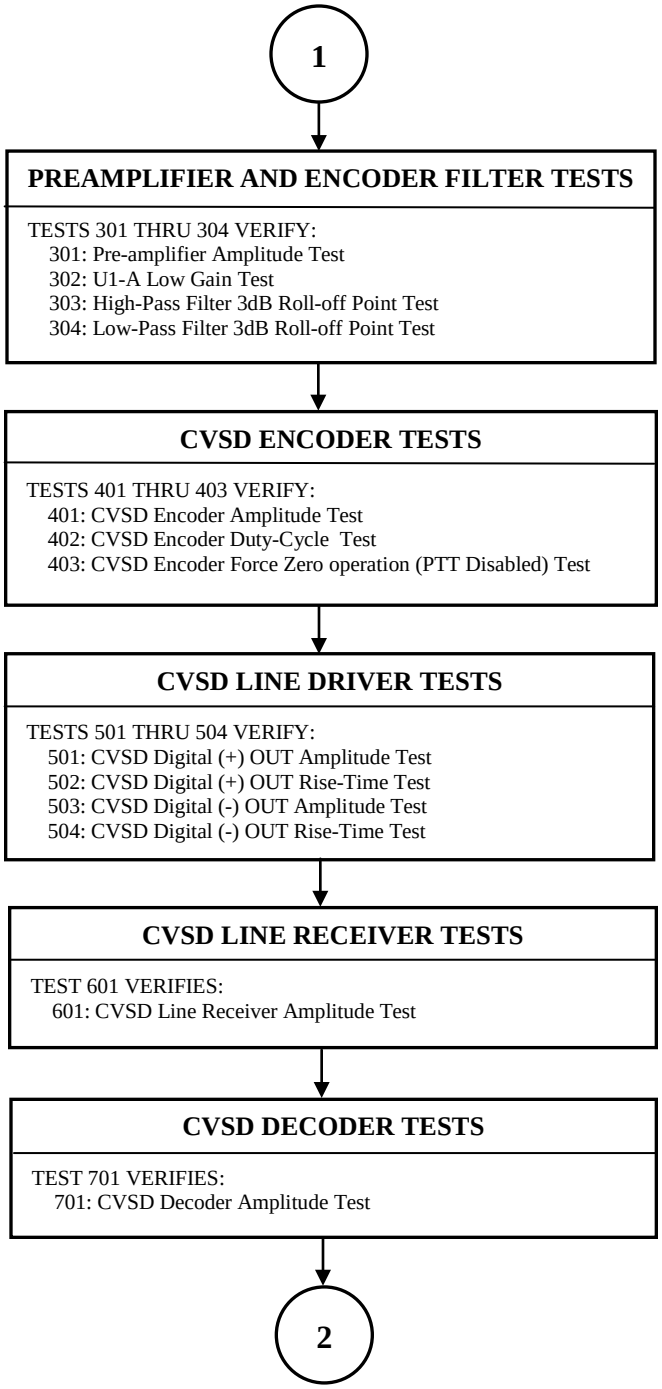
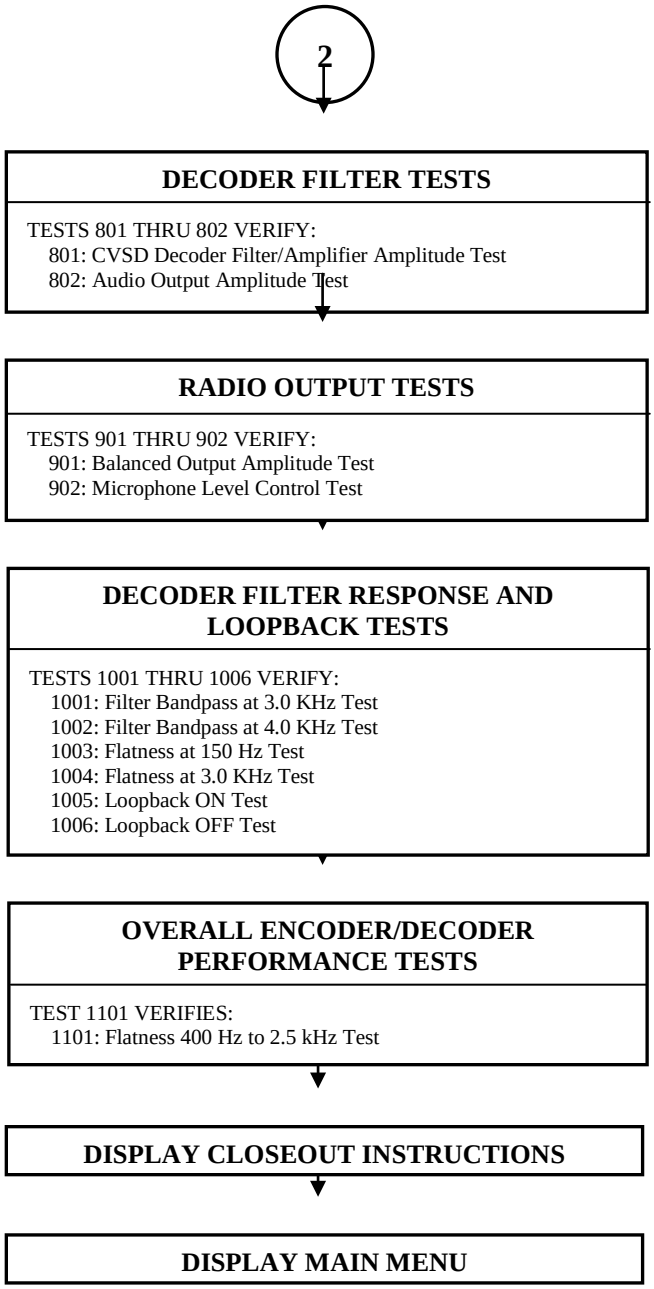
Connection Path as follows:


ATE Resources
ICS A1
DTS CH 56 P7-40
DTS CH 53 P7-43
DTS CH 50 P7-46
FG-OUT P19-5
ARB-OUT P23-12
ARB/7 P23-7
DMM-LO P20-3
DMM-SLO P20-6
DMM-GND P20-1
DMM-SHI P20-5
DMM-HI P20-2
P12-59
P12-26
P13-59
S202
P14-19
P14-15
S802
P15-19
P15-15
S804
P10-203
P10-170
S503
P10-168
P10-6
P10-38
P10-39
P10-71
S502
P10-244
P10-180
S505
P10-162
P10-36
S501
P10-101
P10-231
S301
P11-221
P11-92
S406
P10-70
P10-133
P10-102
P10-166
P10-198
P10-197
ITA J7-
P1-
23
21
52
16
48
8
22
63
64
56
26
43
W10
ITA J4-
P1-
P9
TP12

FUNCTIONAL FLOW CHART (FFC)




1
PREAMPLIFIER AND ENCODER FILTER TESTS
TESTS 301 THRU 304 VERIFY:
301: Pre-amplifier Amplitude Test
302: U1-A Low Gain Test
303: High-Pass Filter 3dB Roll-off Point Test
304: Low-Pass Filter 3dB Roll-off Point Test
CVSD ENCODER TESTS
TESTS 401 THRU 403 VERIFY:
401: CVSD Encoder Amplitude Test
402: CVSD Encoder Duty-Cycle Test
403: CVSD Encoder Force Zero operation (PTT Disabled) Test
CVSD LINE DRIVER TESTS
TESTS 501 THRU 504 VERIFY:
501: CVSD Digital (+) OUT Amplitude Test
502: CVSD Digital (+) OUT Rise-Time Test
503: CVSD Digital (-) OUT Amplitude Test
504: CVSD Digital (-) OUT Rise-Time Test
CVSD LINE RECEIVER TESTS
TEST 601 VERIFIES:
601: CVSD Line Receiver Amplitude Test
CVSD DECODER TESTS
TEST 701 VERIFIES:
701: CVSD Decoder Amplitude Test
2


2
DECODER FILTER TESTS
TESTS 801 THRU 802 VERIFY:
801: CVSD Decoder Filter/Amplifier Amplitude Test
802: Audio Output Amplitude Test
RADIO OUTPUT TESTS
TESTS 901 THRU 902 VERIFY:
901: Balanced Output Amplitude Test
902: Microphone Level Control Test
DECODER FILTER RESPONSE AND LOOPBACK TESTS
TESTS 1001 THRU 1006 VERIFY:
1001: Filter Bandpass at 3.0 KHz Test
1002: Filter Bandpass at 4.0 KHz Test
1003: Flatness at 150 Hz Test
1004: Flatness at 3.0 KHz Test
1005: Loopback ON Test
1006: Loopback OFF Test
OVERALL ENCODER/DECODER PERFORMANCE TESTS
TEST 1101 VERIFIES:
1101: Flatness 400 Hz to 2.5 kHz Test
DISPLAY CLOSEOUT INSTRUCTIONS
DISPLAY MAIN MENU