English Language Test Description

Contract Number: N00244-09-C-0054

For

Unit Under Test

UUT Nomenclature: 6802 Computer CCA
UUT Part Number: 2618567-2
UUT Reference Designator: CON A4

From

Assault Amphibious Vehicle
AN/PSM-115

ATE (Automated Test Equipment) SYSTEM

AN/USM-657B(V)2 Third Echelon Test System (TETS)
AN/USM-717(V)2 Virtual Instrument Portable Equipment Repair / Tester (VIPER/T)

Developed by

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Prepared By	Signature	Date Prepared	Date Submitted
Tom Biggs		05/19/2010	

Approved By	Signature	Date Received	Date Approved

ELTD REVISION SUMMARY

Revision Number	Date	Reason	Approved By – Date Approved
-	05/19/2010	ORIGINAL ISSUE	

1. Introduction

The Unit Under Test (UUT) for this English Language Test Description (ELTD) is the 6802 Computer Circuit Card Assembly (CCA), Part Number 2618567-2. The CCA is reference designator A4 of the Controller, C10879/MSQ-115 Line Replaceable Unit (LRU) part number 2618506-1. The LRU resides in the Assault Amphibious Vehicle (AAV) Weapon System.

1.1. Scope

An ELTD is a detailed supplementary document consisting of textual test descriptions with graphical representation of signal interconnectivity and a functional flow chart.

1.2. Purpose

The purpose of this document is to provide English language test descriptions for the TP_AAV_CON_A4 test program, to a level of detail used for maintenance purposes. The TP_AAV_CON_A4 test program makes up part of the AN/PSM-115 Application Program Set (APS).

1.3. Content Arrangement

The document is laid out in the sequence the Test Program Set (TPS) would be executed when a 95 “Run All Mods” is entered in the main menu. A paragraph at the beginning of each module will describe the test description for that module. Each step will contain a description for that particular test followed by a graphical representation of the connections made from the receiver, through the Interface Test Adapter (ITA) and cable W10 to the 6802 Computer CCA. A Functional Flow Chart resides at the end of the document.

2. English Language Test Description (ELTD)

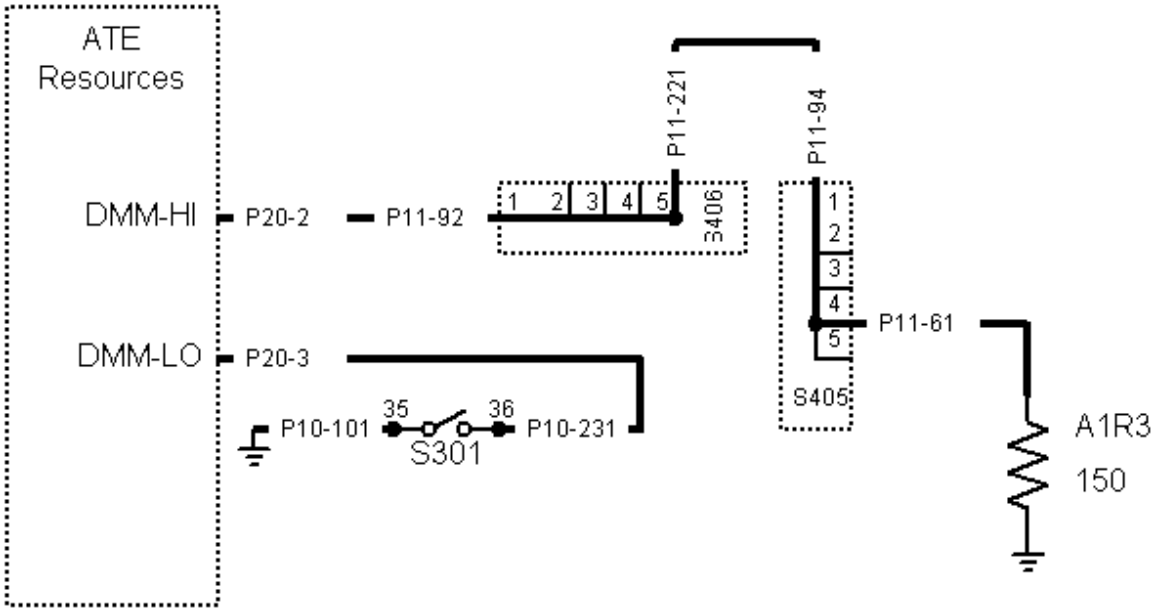
WEAPON SYSTEM: Assault Amphibious Vehicle (AAV)
UNIT UNDER TEST: 2618567-2
TEST PROGRAM SET: TP_AAV_CON_A4

SAFE TO TURN ON TESTS

Step 1 ITA Identification

Test step 1 verifies the correct ITA is installed by using the DMM to measure the resistance of ITA A1R3. The resistance should be from 149 ohms to 155 ohms.

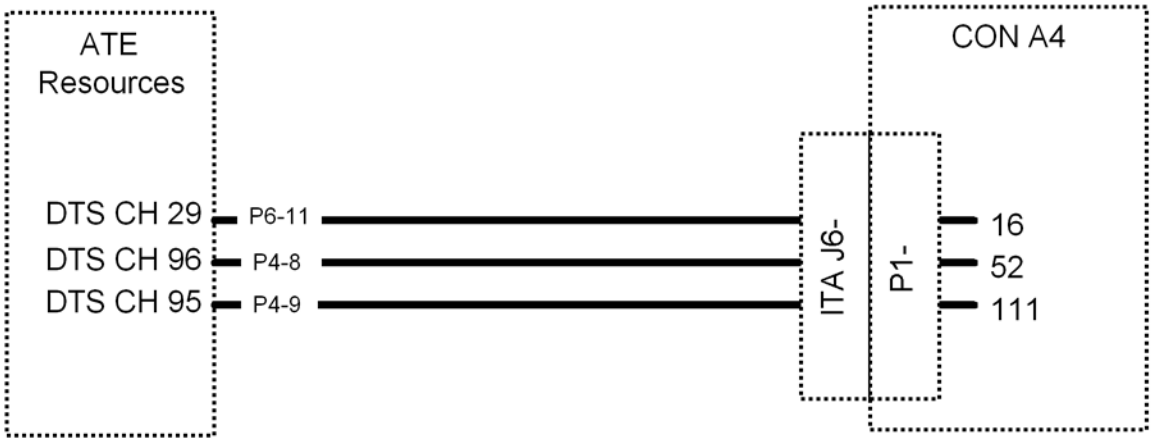
Connection Path as follows:



Step 2 UUT Identification

This step verifies continuity between UUT P1-16 and P1-52 as well as verifies a weak connection from P1-111 to UUT digital ground in order to ensure that the correct UUT is installed. It does this by applying a 1500 uA pullup toward 5.0 V on P1-52 and P1-111. A logic low is applied on P1-16 and the test verifies a binary B'00' on P1-52 and P1-111. The entire test is performed using the DTS.

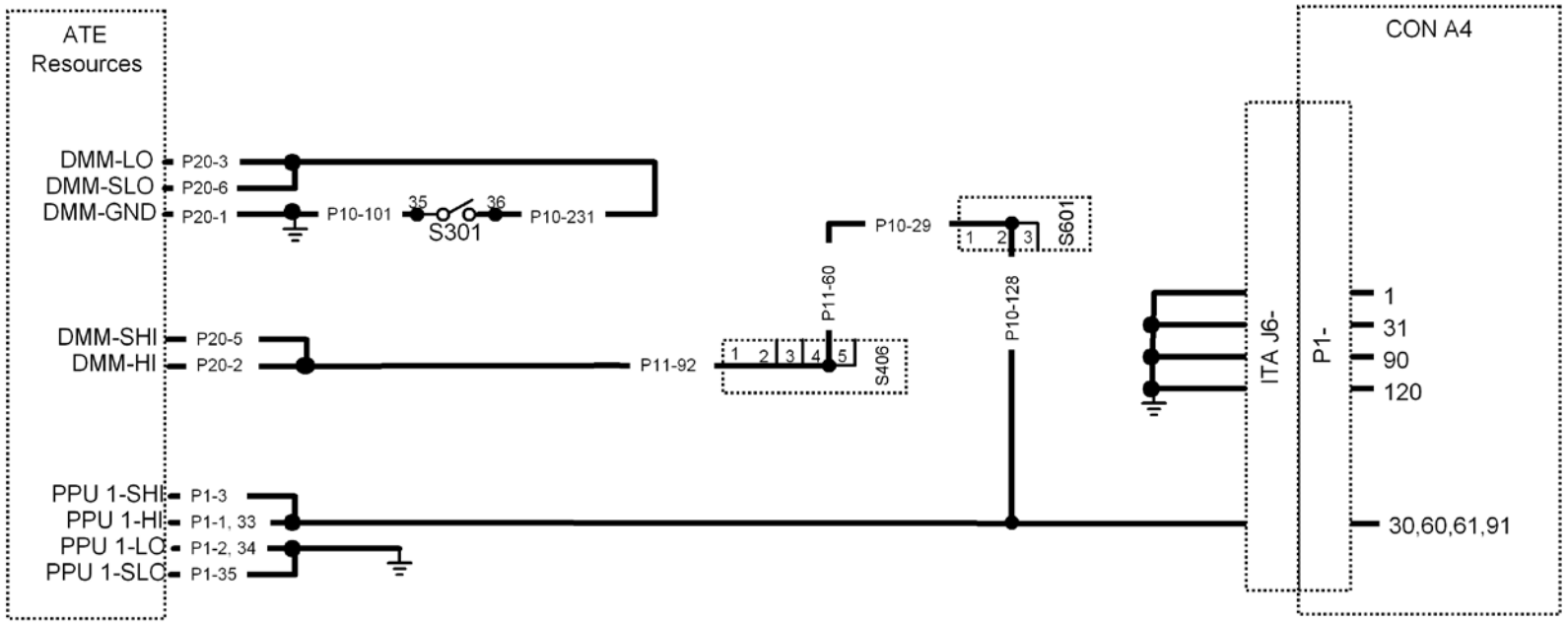
Connection Path as follows:



Step 3 +5VDC Power STTO

This step detects the presence of a +5 volt power supply overload condition prior to fully powering up the UUT. It does this by apply 750 mVDC using DC1 with a current limit setting of 150 mA. Then the DMM is used to verify that between 562.5 mV and 1.000 V is present on the UUT power pins. If an overload is present DC1 will exceed its current limit and turn off before the measurement causing the test to fail.

Connection Path as follows:


ATE
Resources
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-101
35
36
S301
P10-231
P10-29
S601
1 2 3
P11-60
P10-128
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
1 2 3 4 5
S406
PPU 1-SHI
PPU 1-HI
PPU 1-LO
PPU 1-SLO
P1-3
P1-1, 33
P1-2, 34
P1-35
CON A4
ITA J6-
P1-
1
31
90
120
30,60,61,91

UUT POWER UP

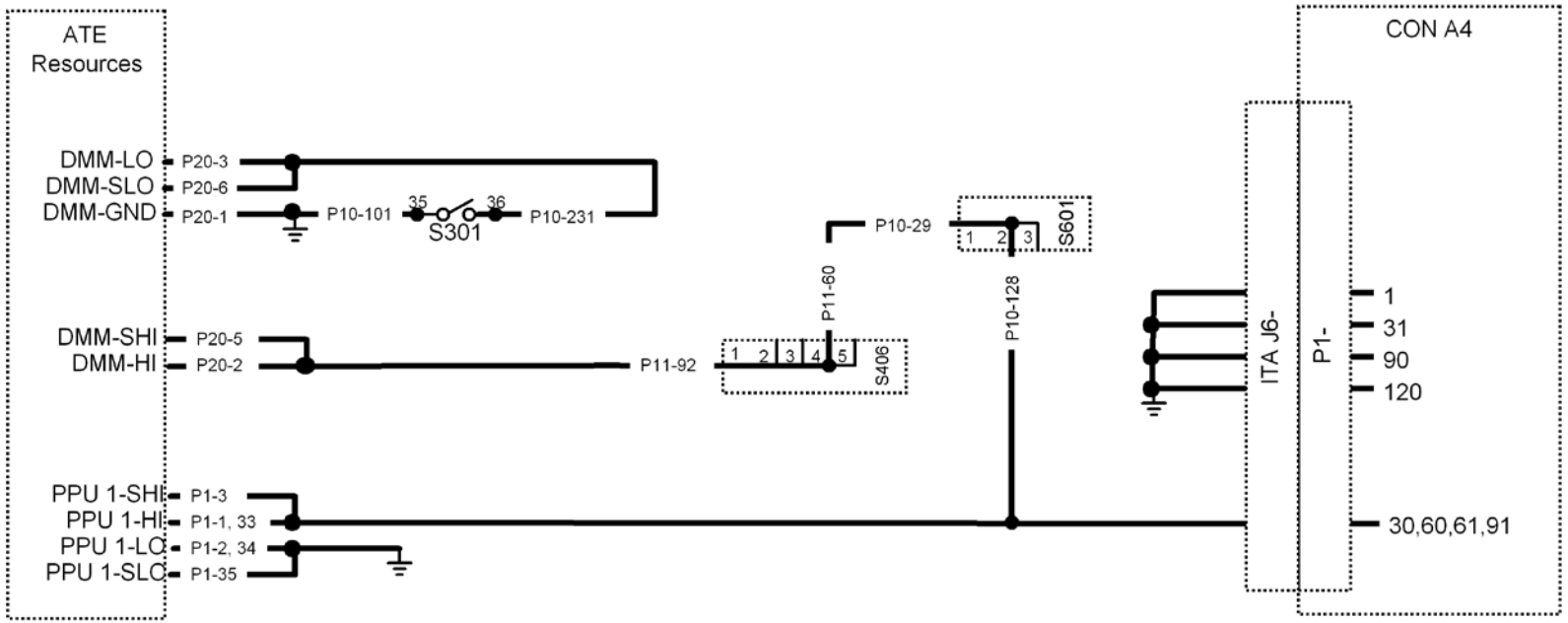
+5 Vdc at 1.5 A with a tolerance of ±0.8 Vdc is required to power the UUT.

UUT POWER UP TESTS

Step 4 +5VDC Power Up Test

This step applies UUT +5V power and verifies the UUT +5V power input voltage is within tolerance following application. Power is applied at a voltage of 5.1 VDC using DC1 at 1.5 Amps across UUT power pins P1-30, 60, 61, and 91 to GND (P1-1, 31, 90, and 120). The DMM is then used to verify input power is between 4.2 and 5.8 VDC at P1-30/GND.

Connection Path as follows:


ATE
Resources
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-101
35
36
S301
P10-231
P10-29
S601
1 2 3
P11-60
P10-128
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
1 2 3 4 5
S406
PPU 1-SHI
PPU 1-HI
PPU 1-LO
PPU 1-SLO
P1-3
P1-1, 33
P1-2, 34
P1-35
CON A4
ITA J6-
P1-
1
31
90
120
30,60,61,91

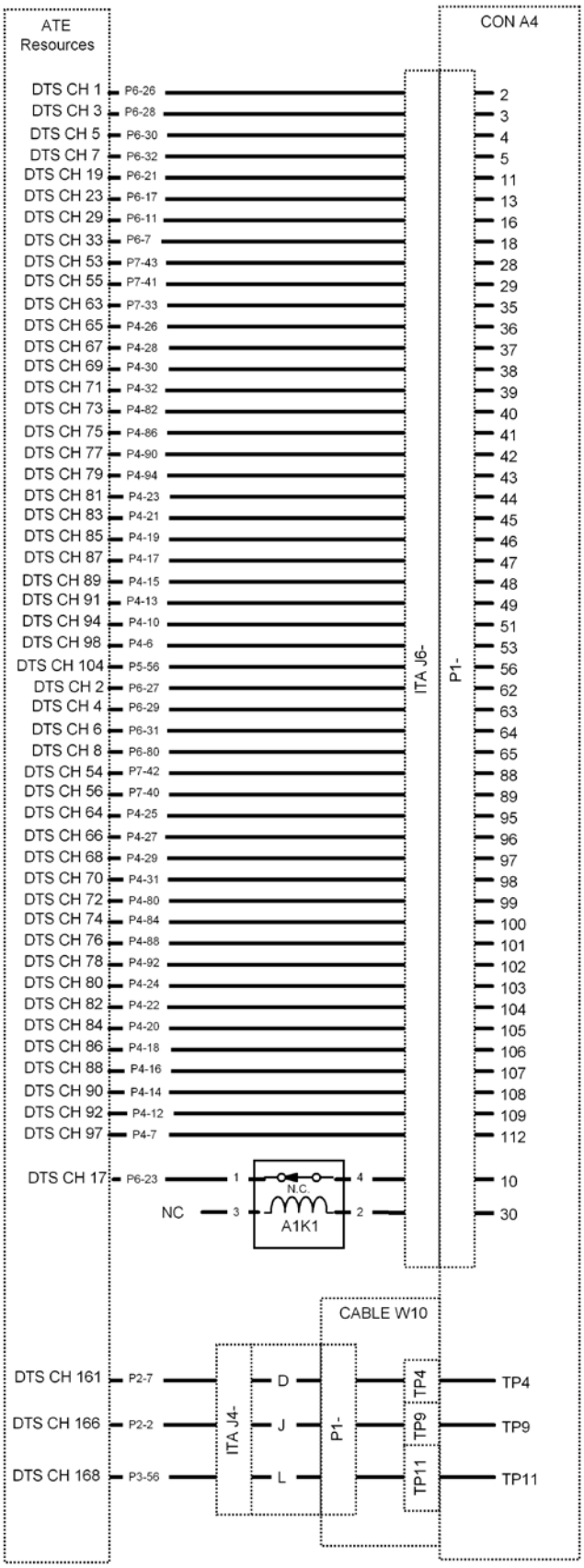
MODULE 1 LASAR DIGITAL TEST

Module 1 consists of one LASAR generated test step which performs a majority of the testing on this primarily digital UUT.

Step 101 LASAR Digital Test

This test step tests a majority of the digital components of the UUT using a LASAR generated digital test binary file '6802.DTB', which is executed using the M910NAM non ATLAS module. The 6802 microprocessor, U65, is held permanently in a bus-acknowledged state throughout this test. In this state the CPU will not assert any signals on the address or data busses. This is done because there was not a model available to completely represent the 6802 for the simulation. Instead a simplified model was created that accurately replicates the behavior of the 6802 CPU only while it is in the bus-acknowledged state. For all other digital components which were included in the simulation, the models are fully accurate. In the event of a failure, automatic guided probe diagnostics will be employed to isolate the failure. Almost all digital edge pins are used in this test and also some test points. One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. Pin 3 of A1K1 is connected to a switch that is left open for this test, effectively leaving Pin 3 Not Connected (NC). The test should pass without any errors.

Connection Path as follows:


ATE Resources
CON A4
ITA J6-
P1-
DTS CH 1 P6-26 2
DTS CH 3 P6-28 3
DTS CH 5 P6-30 4
DTS CH 7 P6-32 5
DTS CH 19 P6-21 11
DTS CH 23 P6-17 13
DTS CH 29 P6-11 16
DTS CH 33 P6-7 18
DTS CH 53 P7-43 28
DTS CH 55 P7-41 29
DTS CH 63 P7-33 35
DTS CH 65 P4-26 36
DTS CH 67 P4-28 37
DTS CH 69 P4-30 38
DTS CH 71 P4-32 39
DTS CH 73 P4-82 40
DTS CH 75 P4-86 41
DTS CH 77 P4-90 42
DTS CH 79 P4-94 43
DTS CH 81 P4-23 44
DTS CH 83 P4-21 45
DTS CH 85 P4-19 46
DTS CH 87 P4-17 47
DTS CH 89 P4-15 48
DTS CH 91 P4-13 49
DTS CH 94 P4-10 51
DTS CH 98 P4-6 53
DTS CH 104 P5-56 56
DTS CH 2 P6-27 62
DTS CH 4 P6-29 63
DTS CH 6 P6-31 64
DTS CH 8 P6-80 65
DTS CH 54 P7-42 88
DTS CH 56 P7-40 89
DTS CH 64 P4-25 95
DTS CH 66 P4-27 96
DTS CH 68 P4-29 97
DTS CH 70 P4-31 98
DTS CH 72 P4-80 99
DTS CH 74 P4-84 100
DTS CH 76 P4-88 101
DTS CH 78 P4-92 102
DTS CH 80 P4-24 103
DTS CH 82 P4-22 104
DTS CH 84 P4-20 105
DTS CH 86 P4-18 106
DTS CH 88 P4-16 107
DTS CH 90 P4-14 108
DTS CH 92 P4-12 109
DTS CH 97 P4-7 112
DTS CH 17 P6-23 1 N.C. 4 10
NC 3 A1K1 2 30
CABLE W10
DTS CH 161 P2-7 D TP4 TP4
DTS CH 166 P2-2 J TP9 TP9
DTS CH 168 P3-56 L TP11 TP11
ITA J4-
P1-

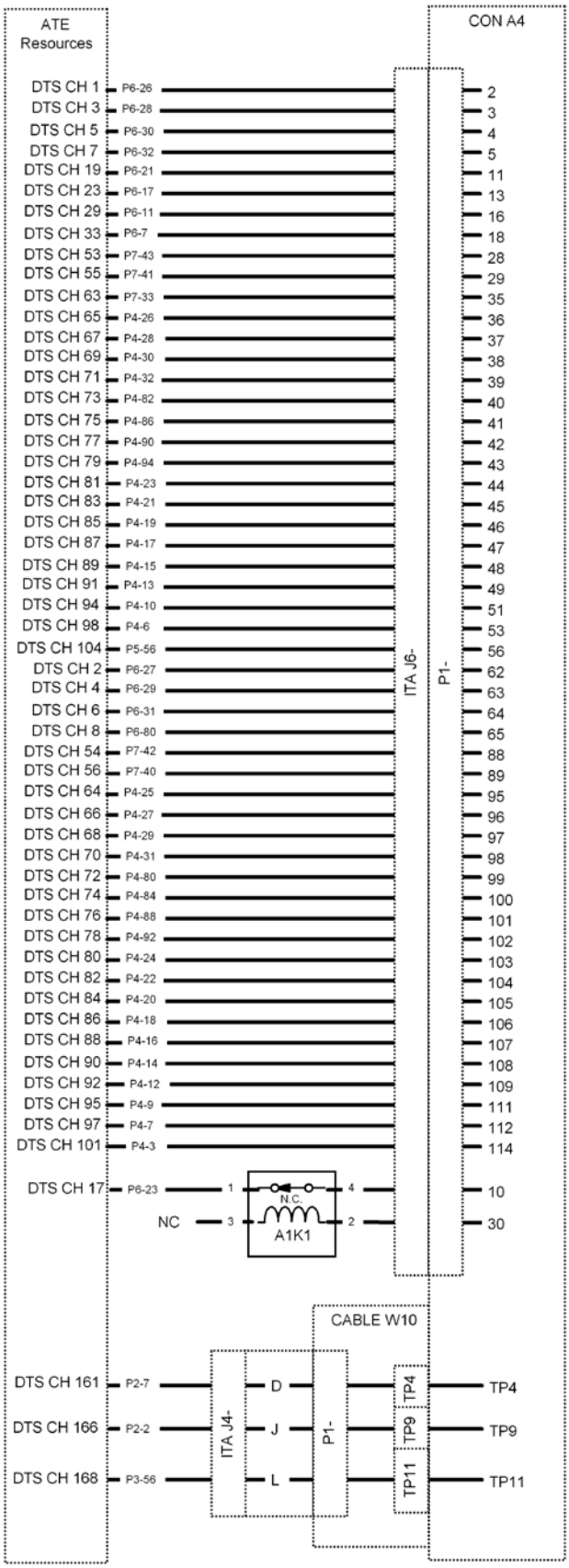
MODULE 2 MICROPROCESSOR TEST

Module 2 performs testing which focuses on the 6802 CPU (U65) and supporting components which could not be tested in Module 1 due to a lack of a LASAR model for U65.

Step 201 Microprocessor Test

This test consists of a manually generated digital test binary file, '6802CPU.DTB', executed using the M910NAM non ATLAS module. LASAR was not used to test the CPU because a complete model of the 6802 CPU was not available. This test verifies the following: All edge pins of the CPU (U65), all internal RAM cells of the CPU, all internal registers of the CPU and all edge pins of CPU supporting components that could not be tested in LASAR due to their close connection to the operation of the CPU, which include all or part of U45, R13, U14, U15, U35, U44, U45, U54, and U64. Also more thorough detections for R6 and R7 are placed in this test since there were not sufficient level set resources remaining in the LASAR test. This major part of this test is accomplished by supplying a synthesized micro-program to the CPU starting with the first program byte read following a CPU reset. This is accomplished by disabling the data outputs of the EPROMs by placing a logic '1' on edge pins P1-28, P1-88, P1-89 and P1-29. By doing this the data bus becomes free whenever the CPU attempts to address and read a program instruction. At this time a generated program instruction can be placed on the data bus for the CPU to read. In this way, the state of the CPU can be controlled by issuing machine language commands from the instruction set of the 6802. All registers, RAM, and edge pins are fully exercised by this synthetic micro-program. The micro-program also causes the CPU to receive and transmit the necessary logic data on its address, data and control line edge pins to test the CPU supporting components that are covered by this test. However, the entire instruction set is not verified. One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. Pin 3 of A1K1 is connected to a switch that is left open for this test, effectively leaving Pin 3 Not Connected (NC). The test should pass without any errors.

Connection Path as follows:


ATE Resources
CON A4
DTS CH 1 P6-26
DTS CH 3 P6-28
DTS CH 5 P6-30
DTS CH 7 P6-32
DTS CH 19 P6-21
DTS CH 23 P6-17
DTS CH 29 P6-11
DTS CH 33 P6-7
DTS CH 53 P7-43
DTS CH 55 P7-41
DTS CH 63 P7-33
DTS CH 65 P4-26
DTS CH 67 P4-28
DTS CH 69 P4-30
DTS CH 71 P4-32
DTS CH 73 P4-82
DTS CH 75 P4-86
DTS CH 77 P4-90
DTS CH 79 P4-94
DTS CH 81 P4-23
DTS CH 83 P4-21
DTS CH 85 P4-19
DTS CH 87 P4-17
DTS CH 89 P4-15
DTS CH 91 P4-13
DTS CH 94 P4-10
DTS CH 98 P4-6
DTS CH 104 P5-56
DTS CH 2 P6-27
DTS CH 4 P6-29
DTS CH 6 P6-31
DTS CH 8 P6-80
DTS CH 54 P7-42
DTS CH 56 P7-40
DTS CH 64 P4-25
DTS CH 66 P4-27
DTS CH 68 P4-29
DTS CH 70 P4-31
DTS CH 72 P4-80
DTS CH 74 P4-84
DTS CH 76 P4-88
DTS CH 78 P4-92
DTS CH 80 P4-24
DTS CH 82 P4-22
DTS CH 84 P4-20
DTS CH 86 P4-18
DTS CH 88 P4-16
DTS CH 90 P4-14
DTS CH 92 P4-12
DTS CH 95 P4-9
DTS CH 97 P4-7
DTS CH 101 P4-3
ITA J6-
P1-
2
3
4
5
11
13
16
18
28
29
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
51
53
56
62
63
64
65
88
89
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
111
112
114
DTS CH 17 P6-23
NC
N.C.
A1K1
1
4
3
2
10
30
CABLE W10
DTS CH 161 P2-7
DTS CH 166 P2-2
DTS CH 168 P3-56
ITA J4-
D
J
L
P1-
TP4
TP9
TP11
TP4
TP9
TP11

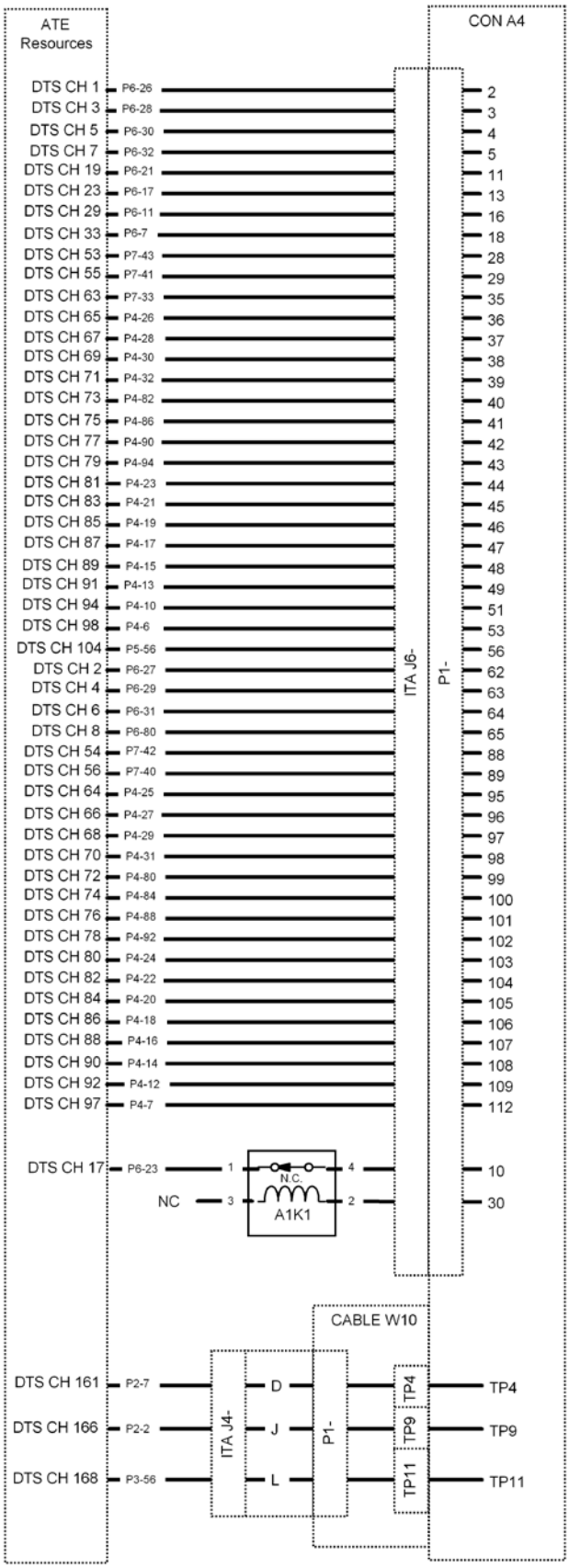
MODULE 3 ROM DATA TEST

Module performs a complete readback of all ROM data contents for ROM components U11, U21, U31, and U41.

Step 301 ROM Bank 0 Data Test

This test consists of a manually generated digital test binary file, '6802.DTB', executed using the M910NAM non ATLAS module. This test verifies all data content of the first EPROM bank which consists of U11. This is accomplished by first placing a logic low on P1-28, P1-88, P1-89 and P1-29 which enables the data outputs of all EPROMS. Then the 6802 CPU (U65) is reset by momentarily back-driving a logic low on TP11. Then the CPU is placed in the HALT condition by placing a logic low on P1-18. This causes the CPU BA output (U65-7) to go to logic high which in turn disables the CPU address buffer (U35 and U45) and CPU data buffer (U64) and in effect causes the CPU to surrender control of the address and data buses. Also while in the HALT state the CPU R/W line (U65-34) remains in the logic high (read) state. In order to cause the data direction of the outer data buffer (U24) to be outwards toward the bidirectional data edge pins D7-D0 (P1-46, 45, 44, 43, 103, 104, 105, and 106) where EPROM data will be read, the static R_W signal is overridden by back-driving a logic low on P1-51 (TP5). The EPROMS are still read because they are read-only and do not respond to the R_W signal even though it has been placed in the (write) state. For this reason they are the only devices on the CCA from which data can be read directly onto the CCA data edge pins. Then the outer data buffer (U24) must be enabled by back-driving a logic low on P1-53 (TP1), since this buffer will not normally be decoded by the address decoder (U15) when an EPROM address is present because I/O from the EPROM is normally only to the CPU which does not require the use of this buffer. At this point any EPROM address placed directly on the address edge pins A15-A0 (P1-42, 41, 38, 40, 37, 39, 36, 35, 95, 96, 97, 98, 99, 100, 101, and 102) will cause the EPROM to read and the data to propagate immediately to the data edge pins via data buffer U24. The addresses in the range 0xC000 thru 0xCFFF, which corresponds to this EPROM bank U11, are then placed on the address bus one at a time, while each data byte is tested at the data edge pins D7-D0. One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. Pin 3 of A1K1 is connected to a switch that is left open for this test, effectively leaving Pin 3 Not Connected (NC). The test should pass without any errors.

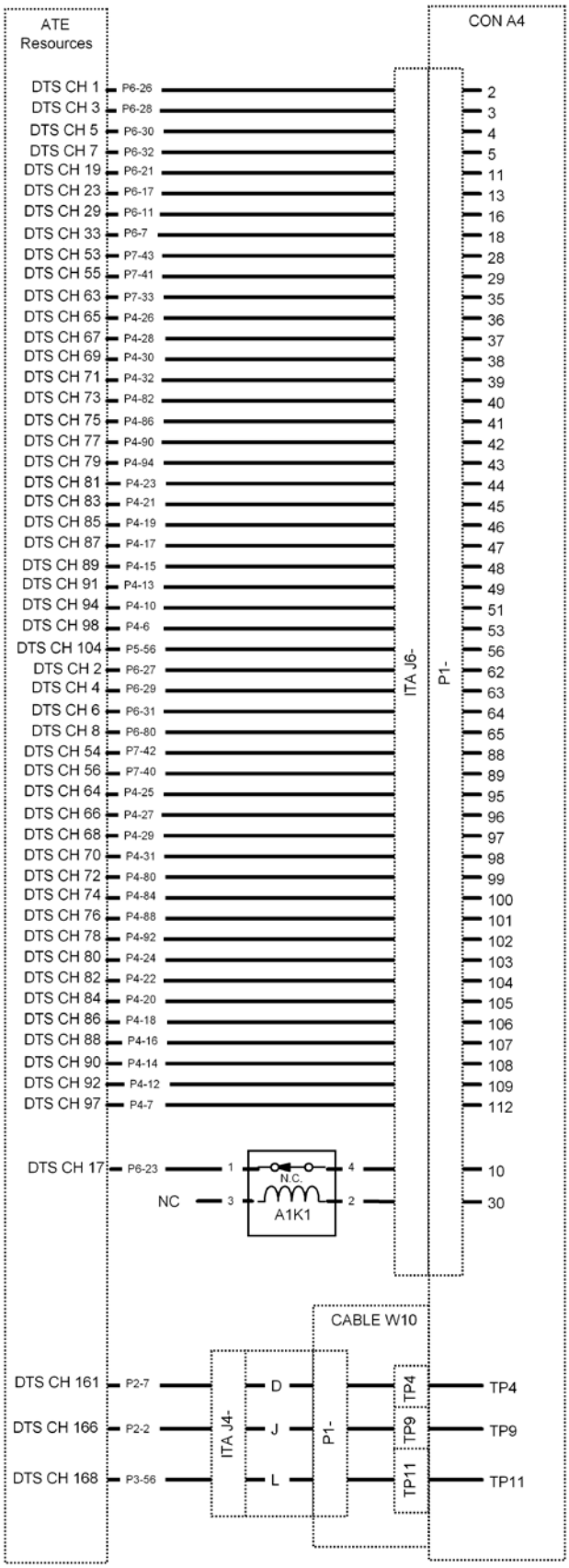
Connection Path as follows:


ATE Resources
CON A4
DTS CH 1 P6-26
DTS CH 3 P6-28
DTS CH 5 P6-30
DTS CH 7 P6-32
DTS CH 19 P6-21
DTS CH 23 P6-17
DTS CH 29 P6-11
DTS CH 33 P6-7
DTS CH 53 P7-43
DTS CH 55 P7-41
DTS CH 63 P7-33
DTS CH 65 P4-26
DTS CH 67 P4-28
DTS CH 69 P4-30
DTS CH 71 P4-32
DTS CH 73 P4-82
DTS CH 75 P4-86
DTS CH 77 P4-90
DTS CH 79 P4-94
DTS CH 81 P4-23
DTS CH 83 P4-21
DTS CH 85 P4-19
DTS CH 87 P4-17
DTS CH 89 P4-15
DTS CH 91 P4-13
DTS CH 94 P4-10
DTS CH 98 P4-6
DTS CH 104 P5-56
DTS CH 2 P6-27
DTS CH 4 P6-29
DTS CH 6 P6-31
DTS CH 8 P6-80
DTS CH 54 P7-42
DTS CH 56 P7-40
DTS CH 64 P4-25
DTS CH 66 P4-27
DTS CH 68 P4-29
DTS CH 70 P4-31
DTS CH 72 P4-80
DTS CH 74 P4-84
DTS CH 76 P4-88
DTS CH 78 P4-92
DTS CH 80 P4-24
DTS CH 82 P4-22
DTS CH 84 P4-20
DTS CH 86 P4-18
DTS CH 88 P4-16
DTS CH 90 P4-14
DTS CH 92 P4-12
DTS CH 97 P4-7
ITA J6-
P1-
2
3
4
5
11
13
16
18
28
29
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
51
53
56
62
63
64
65
88
89
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
112
DTS CH 17 P6-23
NC
N.C.
A1K1
1
3
4
2
10
30
CABLE W10
DTS CH 161 P2-7
DTS CH 166 P2-2
DTS CH 168 P3-56
ITA J4-
D
J
L
P1-
TP4
TP9
TP11
TP4
TP9
TP11

Step 302 ROM Bank 1 Data Test

This test consists of a manually generated digital test binary file, '6802.DTB', executed using the M910NAM non ATLAS module. This test verifies all data content of the 2nd EPROM bank which consists of U21. This is accomplished by first placing a logic low on P1-28, P1-88, P1-89 and P1-29 which enables the data outputs of all EPROMS. Then the 6802 CPU (U65) is reset by momentarily back-driving a logic low on TP11. Then the CPU is placed in the HALT condition by placing a logic low on P1-18. This causes the CPU BA output (U65-7) to go to logic high which in turn disables the CPU address buffer (U35 and U45) and CPU data buffer (U64) and in effect causes the CPU to surrender control of the address and data buses. Also while in the HALT state the CPU R/W line (U65-34) remains in the logic high (read) state. In order to cause the data direction of the outer data buffer (U24) to be outwards toward the bidirectional data edge pins D7-D0 (P1-46, 45, 44, 43, 103, 104, 105, and 106) where EPROM data will be read, the static R_W signal is overridden by back-driving a logic low on P1-51 (TP5). The EPROMS are still read because they are read-only and do not respond to the R_W signal even though it has been placed in the (write) state. For this reason they are the only devices on the CCA from which data can be read directly onto the CCA data edge pins. Then the outer data buffer (U24) must be enabled by back-driving a logic low on P1-53 (TP1), since this buffer will not normally be decoded by the address decoder (U15) when an EPROM address is present because I/O from the EPROM is normally only to the CPU which does not require the use of this buffer. At this point any EPROM address placed directly on the address edge pins A15-A0 (P1-42, 41, 38, 40, 37, 39, 36, 35, 95, 96, 97, 98, 99, 100, 101, and 102) will cause the EPROM to read and the data to propagate immediately to the data edge pins via data buffer U24. The addresses in the range 0xD000 thru 0xDFFF, which corresponds to this EPROM bank U21, are then placed on the address bus one at a time, while each data byte is tested at the data edge pins D7-D0. One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. Pin 3 of A1K1 is connected to a switch that is left open for this test, effectively leaving Pin 3 Not Connected (NC). The test should pass without any errors.

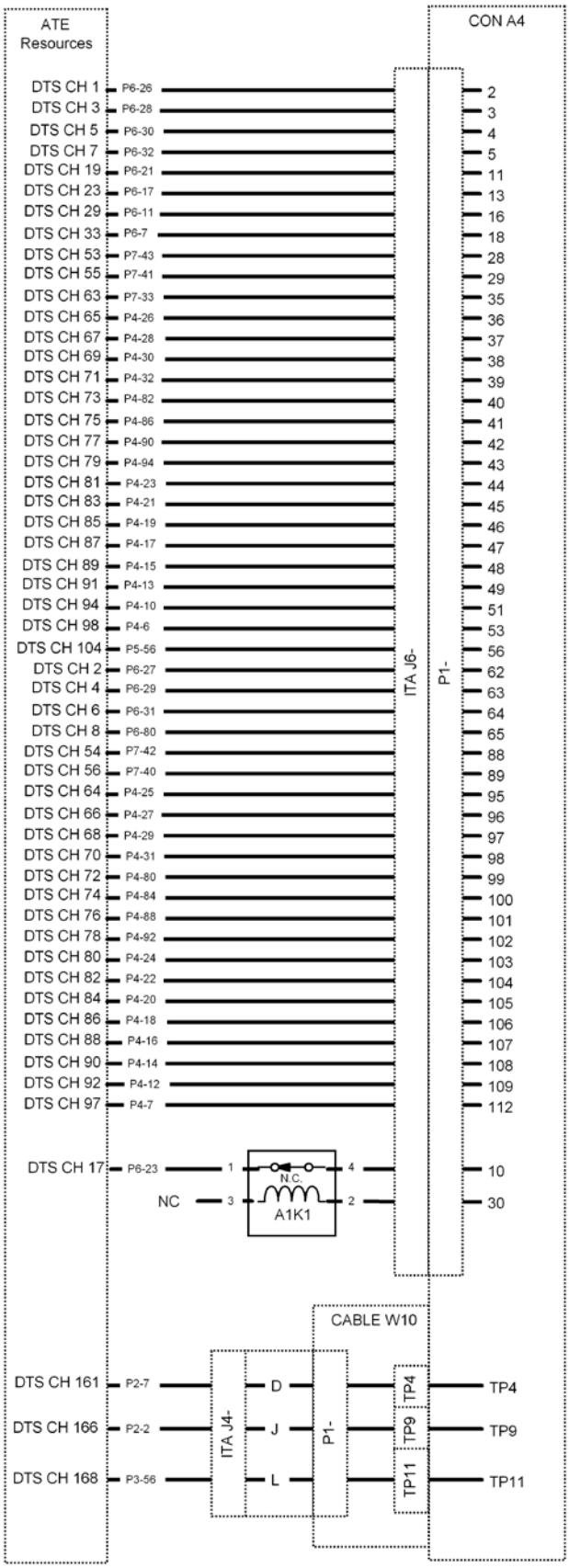
Connection Path as follows:


ATE Resources
CON A4
DTS CH 1 P6-26
DTS CH 3 P6-28
DTS CH 5 P6-30
DTS CH 7 P6-32
DTS CH 19 P6-21
DTS CH 23 P6-17
DTS CH 29 P6-11
DTS CH 33 P6-7
DTS CH 53 P7-43
DTS CH 55 P7-41
DTS CH 63 P7-33
DTS CH 65 P4-26
DTS CH 67 P4-28
DTS CH 69 P4-30
DTS CH 71 P4-32
DTS CH 73 P4-82
DTS CH 75 P4-86
DTS CH 77 P4-90
DTS CH 79 P4-94
DTS CH 81 P4-23
DTS CH 83 P4-21
DTS CH 85 P4-19
DTS CH 87 P4-17
DTS CH 89 P4-15
DTS CH 91 P4-13
DTS CH 94 P4-10
DTS CH 98 P4-6
DTS CH 104 P5-56
DTS CH 2 P6-27
DTS CH 4 P6-29
DTS CH 6 P6-31
DTS CH 8 P6-80
DTS CH 54 P7-42
DTS CH 56 P7-40
DTS CH 64 P4-25
DTS CH 66 P4-27
DTS CH 68 P4-29
DTS CH 70 P4-31
DTS CH 72 P4-80
DTS CH 74 P4-84
DTS CH 76 P4-88
DTS CH 78 P4-92
DTS CH 80 P4-24
DTS CH 82 P4-22
DTS CH 84 P4-20
DTS CH 86 P4-18
DTS CH 88 P4-16
DTS CH 90 P4-14
DTS CH 92 P4-12
DTS CH 97 P4-7
ITA J6-
P1-
2
3
4
5
11
13
16
18
28
29
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
51
53
56
62
63
64
65
88
89
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
112
DTS CH 17 P6-23
NC
1
2
3
4
N.C.
A1K1
10
30
CABLE W10
DTS CH 161 P2-7
DTS CH 166 P2-2
DTS CH 168 P3-56
ITA J4-
D
J
L
P1-
TP4
TP9
TP11
TP4
TP9
TP11

Step 303 ROM Bank 2 Data Test

This test consists of a manually generated digital test binary file, '6802.DTB', executed using the M910NAM non ATLAS module. This test verifies all data content of the third EPROM bank which consists of U31. This is accomplished by first placing a logic low on P1-28, P1-88, P1-89 and P1-29 which enables the data outputs of all EPROMS. Then the 6802 CPU (U65) is reset by momentarily back-driving a logic low on TP11. Then the CPU is placed in the HALT condition by placing a logic low on P1-18. This causes the CPU BA output (U65-7) to go to logic high which in turn disables the CPU address buffer (U35 and U45) and CPU data buffer (U64) and in effect causes the CPU to surrender control of the address and data buses. Also while in the HALT state the CPU R/W line (U65-34) remains in the logic high (read) state. In order to cause the data direction of the outer data buffer (U24) to be outwards toward the bidirectional data edge pins D7-D0 (P1-46, 45, 44, 43, 103, 104, 105, 106) where EPROM data will be read, the static R_W signal is overridden by back-driving a logic low on P1-51(TP5). The EPROMS are still read because they are read-only and do not respond to the R_W signal even though it has been placed in the (write) state. For this reason they are the only devices on the CCA from which data can be read directly onto the CCA data edge pins. Then the outer data buffer (U24) must be enabled by back-driving a logic low on P1-53 (TP1), since this buffer will not normally be decoded by the address decoder (U15) when an EPROM address is present because I/O from the EPROM is normally only to the CPU which does not require the use of this buffer. At this point any EPROM address placed directly on the address edge pins A15-A0 (P1-42, 41, 38, 40, 37, 39, 36, 35, 95, 96, 97, 98, 99, 100, 101, and 102) will cause the EPROM to read and the data to propagate immediately to the data edge pins via data buffer U24. The addresses in the range 0xE000 thru 0xEFFF, which corresponds to this EPROM bank U31, are then placed on the address bus one at a time, while each data byte is tested at the data edge pins D7-D0. One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. Pin 3 of A1K1 is connected to a switch that is left open for this test, effectively leaving Pin 3 Not Connected (NC). The test should pass without any errors.

Connection Path as follows:


ATE Resources
CON A4
DTS CH 1 P6-26
DTS CH 3 P6-28
DTS CH 5 P6-30
DTS CH 7 P6-32
DTS CH 19 P6-21
DTS CH 23 P6-17
DTS CH 29 P6-11
DTS CH 33 P6-7
DTS CH 53 P7-43
DTS CH 55 P7-41
DTS CH 63 P7-33
DTS CH 65 P4-26
DTS CH 67 P4-28
DTS CH 69 P4-30
DTS CH 71 P4-32
DTS CH 73 P4-82
DTS CH 75 P4-86
DTS CH 77 P4-90
DTS CH 79 P4-94
DTS CH 81 P4-23
DTS CH 83 P4-21
DTS CH 85 P4-19
DTS CH 87 P4-17
DTS CH 89 P4-15
DTS CH 91 P4-13
DTS CH 94 P4-10
DTS CH 98 P4-6
DTS CH 104 P5-56
DTS CH 2 P6-27
DTS CH 4 P6-29
DTS CH 6 P6-31
DTS CH 8 P6-80
DTS CH 54 P7-42
DTS CH 56 P7-40
DTS CH 64 P4-25
DTS CH 66 P4-27
DTS CH 68 P4-29
DTS CH 70 P4-31
DTS CH 72 P4-80
DTS CH 74 P4-84
DTS CH 76 P4-88
DTS CH 78 P4-92
DTS CH 80 P4-24
DTS CH 82 P4-22
DTS CH 84 P4-20
DTS CH 86 P4-18
DTS CH 88 P4-16
DTS CH 90 P4-14
DTS CH 92 P4-12
DTS CH 97 P4-7
ITA J6-
P1-
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63
64
65
88
89
95
96
97
98
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112
DTS CH 17 P6-23
NC
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3
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N.C.
A1K1
10
30
CABLE W10
DTS CH 161 P2-7
DTS CH 166 P2-2
DTS CH 168 P3-56
ITA J4-
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P1-
TP4
TP9
TP11
TP4
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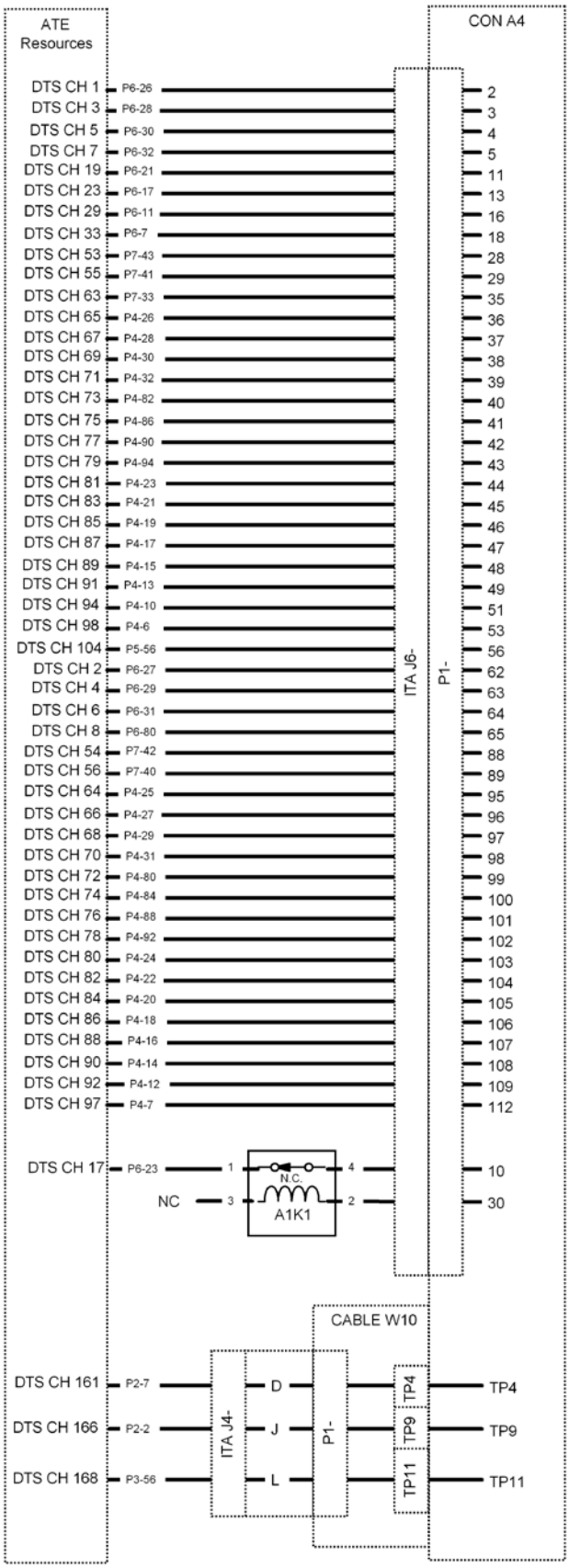
TP11

Step 304 ROM Bank 3 Data Test

This test consists of a manually generated digital test binary file, '6802.DTB', executed using the M910NAM non ATLAS module. This test verifies all data content of the fourth EPROM bank which consists of U41. This is accomplished by first placing a logic low on P1-28, P1-88, P1-89 and P1-29 which enables the data outputs of all EPROMS. Then the 6802 CPU (U65) is reset by momentarily back-driving a logic low on TP11. Then the CPU is placed in the HALT condition by placing a logic low on P1-18. This causes the CPU BA output (U65-7) to go to logic high which in turn disables the CPU address buffer (U35 and U45) and CPU data buffer (U64) and in effect causes the CPU to surrender control of the address and data buses. Also while in the HALT state the CPU R/W line (U65-34) remains in the logic high (read) state. In order to cause the data direction of the outer data buffer (U24) to be outwards toward the bidirectional data edge pins D7-D0 (P1-46, 45, 44, 43, 103, 104, 105, and 106) where EPROM data will be read, the static R_W signal is overridden by back-driving a logic low on P1-51 (TP5). The EPROMS are still read because they are read-only and do not respond to the R_W signal even though it has been placed in the (write) state. For this reason they are the only devices on the CCA from which data can be read directly onto the CCA data edge pins. Then the outer data buffer (U24) must be enabled by back-driving a logic low on P1-53(TP1), since this buffer will not normally be decoded by the address decoder (U15) when an EPROM address is present because I/O from the EPROM is normally only to the CPU which does not require the use of this buffer. At this point any EPROM address placed directly on the address edge pins A15-A0 (P1-42, 41, 38, 40, 37, 39, 36, 35, 95, 96, 97, 98, 99, 100, 101, and 102) will cause the EPROM to read and the data to propagate immediately to the data edge pins via data buffer U24. The addresses in the range 0xF000 thru 0xFFFF, which corresponds to this EPROM bank U41, are then placed on the address bus one at a time, while each data byte is tested at the data edge pins D7-D0. One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. Pin 3 of A1K1 is connected to a switch that is left open for this test, effectively leaving Pin 3 Not Connected (NC). The test should pass without any errors.

Connection Path as follows:


ATE Resources
CON A4
DTS CH 1 P6-26
DTS CH 3 P6-28
DTS CH 5 P6-30
DTS CH 7 P6-32
DTS CH 19 P6-21
DTS CH 23 P6-17
DTS CH 29 P6-11
DTS CH 33 P6-7
DTS CH 53 P7-43
DTS CH 55 P7-41
DTS CH 63 P7-33
DTS CH 65 P4-26
DTS CH 67 P4-28
DTS CH 69 P4-30
DTS CH 71 P4-32
DTS CH 73 P4-82
DTS CH 75 P4-86
DTS CH 77 P4-90
DTS CH 79 P4-94
DTS CH 81 P4-23
DTS CH 83 P4-21
DTS CH 85 P4-19
DTS CH 87 P4-17
DTS CH 89 P4-15
DTS CH 91 P4-13
DTS CH 94 P4-10
DTS CH 98 P4-6
DTS CH 104 P5-56
DTS CH 2 P6-27
DTS CH 4 P6-29
DTS CH 6 P6-31
DTS CH 8 P6-80
DTS CH 54 P7-42
DTS CH 56 P7-40
DTS CH 64 P4-25
DTS CH 66 P4-27
DTS CH 68 P4-29
DTS CH 70 P4-31
DTS CH 72 P4-80
DTS CH 74 P4-84
DTS CH 76 P4-88
DTS CH 78 P4-92
DTS CH 80 P4-24
DTS CH 82 P4-22
DTS CH 84 P4-20
DTS CH 86 P4-18
DTS CH 88 P4-16
DTS CH 90 P4-14
DTS CH 92 P4-12
DTS CH 97 P4-7
ITA J6-
P1-
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99
100
101
102
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112
DTS CH 17 P6-23
NC
N.C.
A1K1
1
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CABLE W10
DTS CH 161 P2-7
DTS CH 166 P2-2
DTS CH 168 P3-56
ITA J4-
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TP4
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TP11
TP4
TP9
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MODULE 4 RAM CELL TEST

Module 4 performs all internal testing of RAM components U13, U22, U23, U32, U33, U42, U43, and U53. This includes full cell testing and address testing, meaning that all internal cells of the RAM are verified to be able to independently store a binary piece of information and that this data can be recovered by reading. Edge pin testing of these components has already been performed in Module 1.

Step 401 RAM Bank 0 Data Test

This test consists of a manually generated digital test binary file, '6802.DTB', executed using the M910NAM non ATLAS module. This test completely tests the RAM chips of the first RAM bank (U13, U53). This includes full cell testing and full address testing. This is accomplished by first resetting the 6802 CPU (U65) by momentarily back-driving a logic low on TP11. Then the CPU is placed in the HALT condition by placing a logic low on P1-18. This causes the CPU BA output (U65-7) to go to logic high which in turn disables the CPU address buffer (U35 and U45) and CPU data buffer (U64) and in effect causes the CPU to surrender control of the address and data buses. Also while in the HALT state the CPU R/W line (U65-34) remains in the logic high (read) state.

Each write to the RAM is accomplished within a single pattern. The outer data buffer (U24) is placed in the inward data direction by back-driving a logic low on P1-16 (TP7). This causes no change at the moment but prevents the data direction of the outer data buffer from changing when the write pulse is applied later. Then P1-53 is back-driven to logic low to enable the outer data buffer (U24) since this buffer will not normally be decoded by the address decoder (U15) when a RAM address is present because I/O from the RAM is normally only to the CPU which does not require the use of this buffer. P1-51 (TP5) has a return to off (ROFF) format for this test. In addition, the timing of this pin is set such that it will assert a logic level starting at 900 nS into each pattern and return to the off 'Hi-Z' state at 1800 nS into each pattern. Since the quiescent state of P1-51 is logic high when it isn't being back-driven, back-driving a logic low on P1-51 causes a low pulse from 900 nS to 1800 nS in the pattern. This pulse enables the write circuit in the currently addressed RAM and effectively strobes one byte of data to be written. In each write pattern the address edge pins A15-A0 (P1-42, 41, 38, 40, 37, 39, 36, 35, 95, 96, 97, 98, 99, 100, 101, and 102) and data edge pins D7-D0 (P1-46, 45, 44, 43, 103, 104, 105, and 106) are setup with the write data and write destination. Logic changes on the address edge pins A15-A0 and data edge pins D7-D0 occur at 0 nS into each pattern. This timing ensures data and address setup and hold times are met relative to the write pulse on P1-51.

Each read is also accomplished within a single pattern, however the propagation of the data to the edge pin extends into the next pattern so that each data byte is actually tested in the pattern following the read pattern. In other words the data is tested while the next byte of RAM is being read. This is due to the propagation delay of the lamp drivers (U61, U62, U71, and U72). The outer data buffer (U24) is not used in the read so it is left in the

disabled state and thus the directional setting is also irrelevant. The outer data buffer can not be used to read the RAM because it is impossible to place it in the correct direction while the RAM is in the read state. Read data is delivered to the tester via the lamp state latch (U52) and the lamp drivers and associated edge pins DD7-DD0 (P1-62, 3, 64, 5, 2, 63, 4, and 65). RAM data is transferred the data bus simply by placing the RAM source address on the address edge pins A15-A0, since the normal condition of the R_W signal is "read" while the CPU is halted. P1-51 (TP5) has a return to off (ROFF) format for this test. In addition, the timing of this pin is set such that it will assert a logic level starting at 1600 nS into each pattern and return to the off 'Hi-Z' state at 1800 nS into each pattern. Since the quiescent state of TP4 is logic high when it isn't being back-driven, back-driving a logic low on TP4 causes a low pulse from 1600 nS to 1800 nS in the pattern. TP4 is given a logic low state causing this low pulse to occur in every read pattern. Each pulse latches the RAM data from the data bus. The data then propagates from the output of the lamp latch to the lamp drive edge pins DD7-DD0 via the lamp drivers to be tested during the following pattern.

To accomplish the RAM cell testing, this test writes each address within the 10-bit address space of this RAM bank with the 8 least significant bits of the address. The addresses are written in sequence 0x000 thru 0x3FF. Note that this address range notation represents the offset within this bank of RAM. The full 16-bit system address range for this bank is 0x1000 thru 0x13FF which are the actual logic words placed on the address edge pins A15 thru A0. The resulting data set consists of the data values 0x00 thru 0xFF repeated four times. Then each of these RAM locations in this range is read and tested in the same order, 0x000 thru 0x3FF.

Then the same process of writing to the address range 0x000 thru 0x3FF is repeated identically, except that the 1's compliments of the 8 least significant bits of the address are written at each location. The resulting data set consists of the data values 0xFF thru 0x00 repeated four times. Then each of the RAM locations in this range is read and tested in the same order, 0x000 thru 0x3FF. At this point all RAM data cells have been tested for both the SA0 and SA1 state. However the upper two address edge pins of the RAM chips in this bank (U13 and U53) have not been tested.

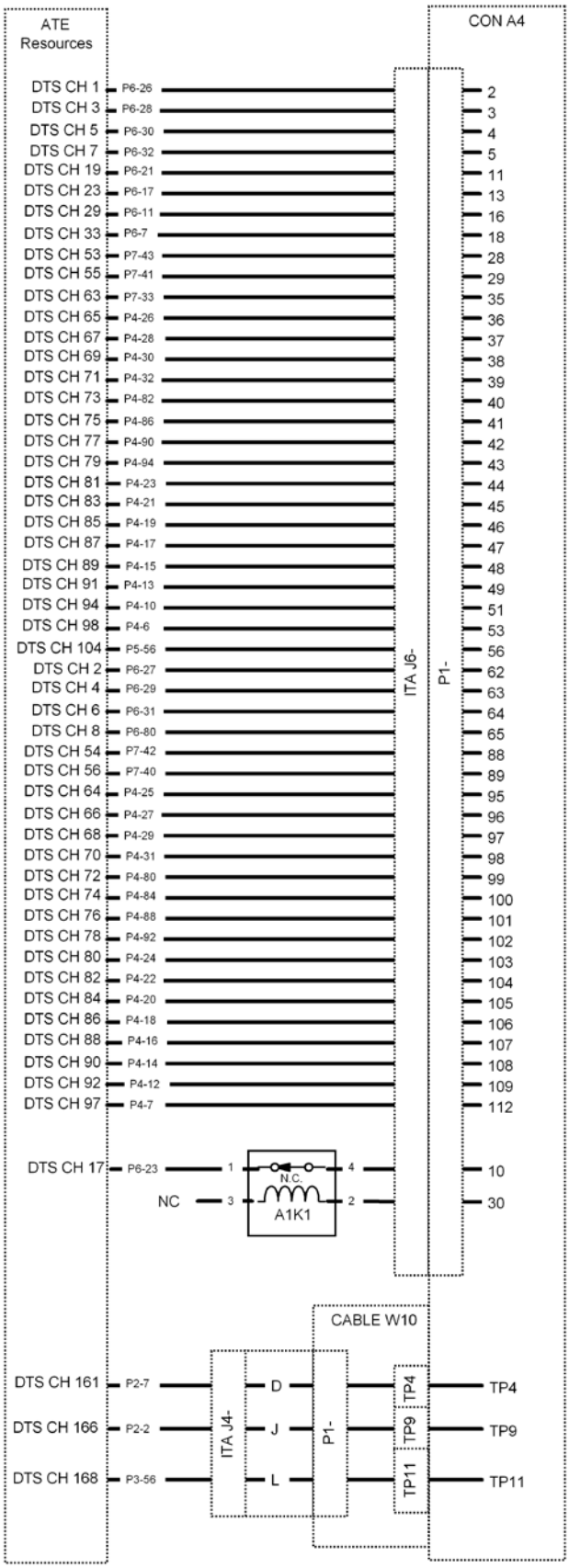
At this point a very efficient and very thorough RAM address logic test will be used to detect any remaining failures of the address logic including failures of all address signals that could affect as few as one bit of data only. This test method goes beyond simply testing for OT1 on each address edge pins and covers the possibility that a failure may exist between any address line and any one data bit. To test one of these fundamental RAM address logic faults, a unique bit value must be written to a pair of address locations for the tested data bit. These data values stored in the tested bit must of course be 0 and 1 in order to be unique. The two locations must be the same address with only the state of the tested address line different between the two. Then, each of the two locations must be read and the data from the tested bit must be recovered intact. At this point the address line / data bit pair have been fully tested. In other words it has been proven that the tested data bit responds to address changes on the tested address line. This test must be performed for all address line / data bit combinations. This would be a

number of tests equaling the number of address lines multiplied by the number of data lines. In this test this theory is highly compressed by two methods so that the all address logic of the 10 address line by 8 data line RAM bank can be tested by writing only 11 locations and then reading those 11 locations back. This is partly because 8 data bits can be written to and read at once which represents 8 tests at a time. Then it is more compressed because a single location can serve as the first address in all of the necessary pairs of address locations.

The first location written is 0x000 which is written with the data value 0xFF. Then each of the 10 address lines is complimented one at a time by writing to addresses 0x001, 0x002, 0x004, 0x008, 0x010, 0x020, 0x040, 0x080, 0x100, 0x200. These 11 locations represent 10 pairs of address locations with location 0x000 being the shared first location in each pair. Note that these address notations represent the offset within this bank of RAM. To all ten of these locations the data value 0x00 is written. Note that this represents the compliment of all eight data bits. Finally these 11 locations are read back. At this point all address logic of the current RAM bank has been tested.

One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. Pin 3 of A1K1 is connected to a switch that is left open for this test, effectively leaving Pin 3 Not Connected (NC). The test should pass without any errors.

Connection Path as follows:


ATE Resources
CON A4
DTS CH 1 P6-26
DTS CH 3 P6-28
DTS CH 5 P6-30
DTS CH 7 P6-32
DTS CH 19 P6-21
DTS CH 23 P6-17
DTS CH 29 P6-11
DTS CH 33 P6-7
DTS CH 53 P7-43
DTS CH 55 P7-41
DTS CH 63 P7-33
DTS CH 65 P4-26
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DTS CH 17 P6-23
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CABLE W10
DTS CH 161 P2-7
DTS CH 166 P2-2
DTS CH 168 P3-56
ITA J4-
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Step 402 RAM Bank 1 Data Test

This test consists of a manually generated digital test binary file, '6802.DTB', executed using the M910NAM non ATLAS module. This test completely tests the RAM chips of the second RAM bank (U22 and U23). This includes full cell testing and full address testing. This is accomplished by first resetting the 6802 CPU (U65) by momentarily back-driving a logic low on TP11. Then the CPU is placed in the HALT condition by placing a logic low on P1-18. This causes the CPU BA output (U65-7) to go to logic high which in turn disables the CPU address buffer (U35 and U45) and CPU data buffer (U64) and in effect causes the CPU to surrender control of the address and data buses. Also while in the HALT state the CPU R/W line (U65-34) remains in the logic high (read) state.

Each write to the RAM is accomplished within a single pattern. The outer data buffer (U24) is placed in the inward data direction by back-driving a logic low on P1-16 (TP7). This causes no change at the moment but prevents the data direction of the outer data buffer from changing when the write pulse is applied later. Then P1-53 is back-driven to logic low to enable the outer data buffer (U24) since this buffer will not normally be decoded by the address decoder (U15) when a RAM address is present because I/O from the RAM is normally only to the CPU which does not require the use of this buffer. P1-51 (TP5) has a return to off (ROFF) format for this test. In addition, the timing of this pin is set such that it will assert a logic level starting at 900 nS into each pattern and return to the off 'Hi-Z' state at 1800 nS into each pattern. Since the quiescent state of P1-51 is logic high when it isn't being back-driven, back-driving a logic low on P1-51 causes a low pulse from 900 nS to 1800 nS in the pattern. This pulse enables the write circuit in the currently addressed RAM and effectively strobes one byte of data to be written. In each write pattern the address edge pins A15-A0 (P1-42, 41, 38, 40, 37, 39, 36, 35, 95, 96, 97, 98, 99, 100, 101, and 102) and data edge pins D7-D0 (P1-46, 45, 44, 43, 103, 104, 105, and 106) are setup with the write data and write destination. Logic changes on the address edge pins A15-A0 and data edge pins D7-D0 occur at 0 nS into each pattern. This timing ensures data and address setup and hold times are met relative to the write pulse on P1-51.

Each read is also accomplished within a single pattern, however the propagation of the data to the edge pin extends into the next pattern so that each data byte is actually tested in the pattern following the read pattern. In other words the data is tested while the next byte of RAM is being read. This is due to the propagation delay of the lamp drivers (U61, U62, U71, and U72). The outer data buffer (U24) is not used in the read so it is left in the disabled state and thus the directional setting is also irrelevant. The outer data buffer can not be used to read the RAM because it is impossible to place it in the correct direction while the RAM is in the read state. Read data is delivered to the tester via the lamp state latch (U52) and the lamp drivers and associated edge pins DD7-DD0 (P1-62, 3, 64, 5, 2, 63, 4, and 65). RAM data is transferred the data bus simply by placing the RAM source address on the address edge pins A15-A0, since the normal condition of the R_W signal is "read" while the CPU is halted. P1-51(TP5) has a return to off (ROFF) format for this

test. In addition, the timing of this pin is set such that it will assert a logic level starting at 1600 nS into each pattern and return to the off 'Hi-Z' state at 1800 nS into each pattern. Since the quiescent state of TP4 is logic high when it isn't being back-driven, back-driving a logic low on TP4 causes a low pulse from 1600 nS to 1800 nS in the pattern. TP4 is given a logic low state causing this low pulse to occur in every read pattern. Each pulse latches the RAM data from the data bus. The data then propagates from the output of the lamp latch to the lamp drive edge pins DD7-DD0 via the lamp drivers to be tested during the following pattern.

To accomplish the RAM cell testing, this test writes each address within the 10-bit address space of this RAM bank with the 8 least significant bits of the address. The addresses are written in sequence 0x000 thru 0x3FF. Note that this address range notation represents the offset within this bank of RAM. The full 16-bit system address range for this bank is 0x1400 thru 0x17FF which are the actual logic words placed on the address edge pins A15 thru A0. The resulting data set consists of the data values 0x00 thru 0xFF repeated four times. Then each of these RAM locations in this range is read and tested in the same order, 0x000 thru 0x3FF.

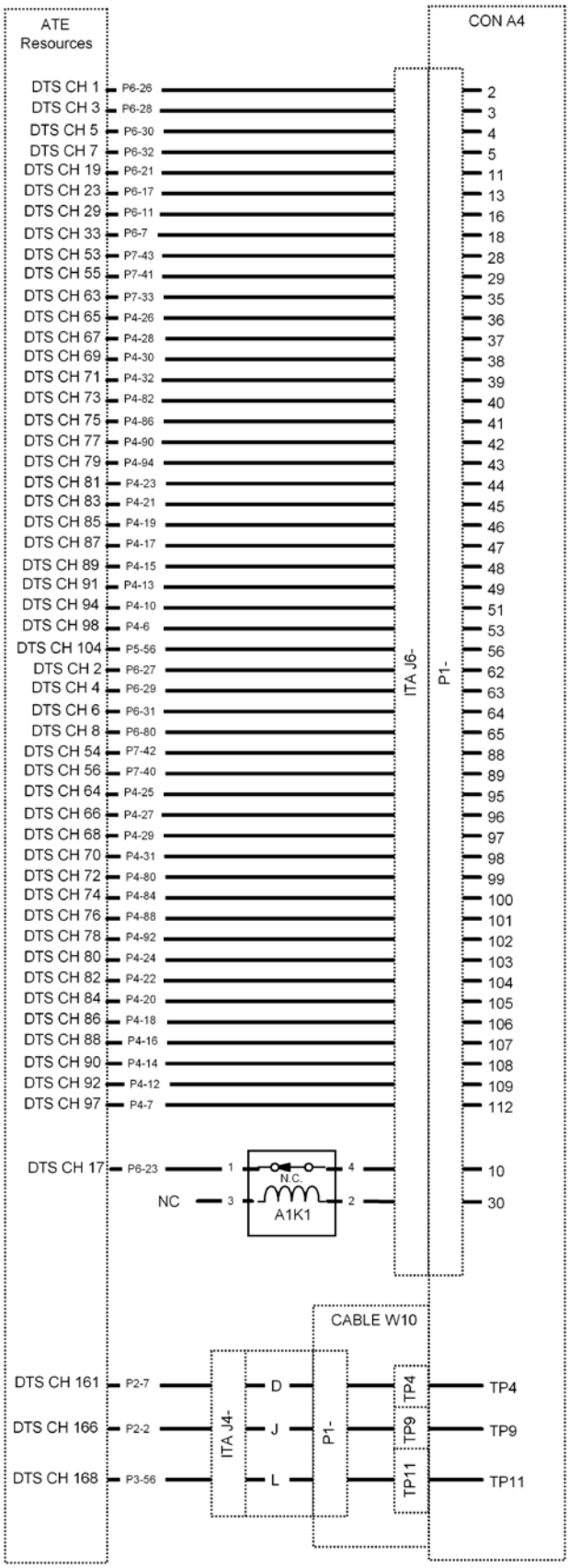
Then the same process of writing to the address range 0x000 thru 0x3FF is repeated identically, except that the 1's compliments of the 8 least significant bits of the address are written at each location. The resulting data set consists of the data values 0xFF thru 0x00 repeated four times. Then each of the RAM locations in this range is read and tested in the same order, 0x000 thru 0x3FF. At this point all RAM data cells have been tested for both the SA0 and SA1 state. However the upper two address edge pins of the RAM chips in this bank (U22 and U23) have not been tested.

At this point a very efficient and very thorough RAM address logic test will be used to detect any remaining failures of the address logic including failures of all address signals that could affect as few as one bit of data only. This test method goes beyond simply testing for OT1 on each address edge pins and covers the possibility that a failure may exist between any address line and any one data bit. To test one of these fundamental RAM address logic faults, a unique bit value must be written to a pair of address locations for the tested data bit. These data values stored in the tested bit must of course be 0 and 1 in order to be unique. The two locations must be the same address with only the state of the tested address line different between the two. Then, each of the two locations must be read and the data from the tested bit must be recovered intact. At this point the address line / data bit pair have been fully tested. In other words it has been proven that the tested data bit responds to address changes on the tested address line. This test must be performed for all address line / data bit combinations. This would be a number of tests equaling the number of address lines multiplied by the number of data lines. In this test this theory is highly compressed by two methods so that the all address logic of the 10 address line by 8 data line RAM bank can be tested by writing only 11 locations and then reading those 11 locations back. This is partly because 8 data bits can be written to and read at once which represents 8 tests at a time. Then it is more compressed because a single location can serve as the first address in all of the necessary pairs of address locations.

The first location written is 0x000 which is written with the data value 0xFF. Then each of the 10 address lines is complimented one at a time by writing to addresses 0x001, 0x002, 0x004, 0x008, 0x010, 0x020, 0x040, 0x080, 0x100, 0x200. These 11 locations represent 10 pairs of address locations with location 0x000 being the shared first location in each pair. Note that these address notations represent the offset within this bank of RAM. To all ten of these locations the data value 0x00 is written. Note that this represents the compliment of all eight data bits. Finally these 11 locations are read back. At this point all address logic of the current RAM bank has been tested.

One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. Pin 3 of A1K1 is connected to a switch that is left open for this test, effectively leaving Pin 3 Not Connected (NC). The test should pass without any errors.

Connection Path as follows:


ATE Resources
CON A4
DTS CH 1 P6-26
DTS CH 3 P6-28
DTS CH 5 P6-30
DTS CH 7 P6-32
DTS CH 19 P6-21
DTS CH 23 P6-17
DTS CH 29 P6-11
DTS CH 33 P6-7
DTS CH 53 P7-43
DTS CH 55 P7-41
DTS CH 63 P7-33
DTS CH 65 P4-26
DTS CH 67 P4-28
DTS CH 69 P4-30
DTS CH 71 P4-32
DTS CH 73 P4-82
DTS CH 75 P4-86
DTS CH 77 P4-90
DTS CH 79 P4-94
DTS CH 81 P4-23
DTS CH 83 P4-21
DTS CH 85 P4-19
DTS CH 87 P4-17
DTS CH 89 P4-15
DTS CH 91 P4-13
DTS CH 94 P4-10
DTS CH 98 P4-6
DTS CH 104 P5-56
DTS CH 2 P6-27
DTS CH 4 P6-29
DTS CH 6 P6-31
DTS CH 8 P6-80
DTS CH 54 P7-42
DTS CH 56 P7-40
DTS CH 64 P4-25
DTS CH 66 P4-27
DTS CH 68 P4-29
DTS CH 70 P4-31
DTS CH 72 P4-80
DTS CH 74 P4-84
DTS CH 76 P4-88
DTS CH 78 P4-92
DTS CH 80 P4-24
DTS CH 82 P4-22
DTS CH 84 P4-20
DTS CH 86 P4-18
DTS CH 88 P4-16
DTS CH 90 P4-14
DTS CH 92 P4-12
DTS CH 97 P4-7
ITA J6-
P1-
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108
109
112
DTS CH 17 P6-23
NC
N.C.
A1K1
1
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4
10
30
CABLE W10
DTS CH 161 P2-7
DTS CH 166 P2-2
DTS CH 168 P3-56
ITA J4-
D
J
L
P1-
TP4
TP9
TP11
TP4
TP9
TP11

Step 403 RAM Bank 2 Data Test

This test consists of a manually generated digital test binary file, '6802.DTB', executed using the M910NAM non ATLAS module. This test completely tests the RAM chips of the third RAM bank (U32 and U33). This includes full cell testing and full address testing. This is accomplished by first resetting the 6802 CPU (U65) by momentarily back-driving a logic low on TP11. Then the CPU is placed in the HALT condition by placing a logic low on P1-18. This causes the CPU BA output (U65-7) to go to logic high which in turn disables the CPU address buffer (U35 and U45) and CPU data buffer (U64) and in effect causes the CPU to surrender control of the address and data buses. Also while in the HALT state the CPU R/W line (U65-34) remains in the logic high (read) state.

Each write to the RAM is accomplished within a single pattern. The outer data buffer (U24) is placed in the inward data direction by back-driving a logic low on P1-16 (TP7). This causes no change at the moment but prevents the data direction of the outer data buffer from changing when the write pulse is applied later. Then P1-53 is back-driven to logic low to enable the outer data buffer (U24) since this buffer will not normally be decoded by the address decoder (U15) when a RAM address is present because I/O from the RAM is normally only to the CPU which does not require the use of this buffer. P1-51 (TP5) has a return to off (ROFF) format for this test. In addition, the timing of this pin is set such that it will assert a logic level starting at 900 nS into each pattern and return to the off 'Hi-Z' state at 1800 nS into each pattern. Since the quiescent state of P1-51 is logic high when it isn't being back-driven, back-driving a logic low on P1-51 causes a low pulse from 900 nS to 1800 nS in the pattern. This pulse enables the write circuit in the currently addressed RAM and effectively strobes one byte of data to be written. In each write pattern the address edge pins A15-A0 (P1-42, 41, 38, 40, 37, 39, 36, 35, 95, 96, 97, 98, 99, 100, 101, and 102) and data edge pins D7-D0 (P1-46, 45, 44, 43, 103, 104, 105, and 106) are setup with the write data and write destination. Logic changes on the address edge pins A15-A0 and data edge pins D7-D0 occur at 0 nS into each pattern. This timing ensures data and address setup and hold times are met relative to the write pulse on P1-51.

Each read is also accomplished within a single pattern, however the propagation of the data to the edge pin extends into the next pattern so that each data byte is actually tested in the pattern following the read pattern. In other words the data is tested while the next byte of RAM is being read. This is due to the propagation delay of the lamp drivers (U61, U62, U71, and U72). The outer data buffer (U24) is not used in the read so it is left in the disabled state and thus the directional setting is also irrelevant. The outer data buffer can not be used to read the RAM because it is impossible to place it in the correct direction while the RAM is in the read state. Read data is delivered to the tester via the lamp state latch (U52) and the lamp drivers and associated edge pins DD7-DD0(P1-62, 3, 64, 5, 2, 63, 4, 65). RAM data is transferred the data bus simply by placing the RAM source address on the address edge pins A15-A0, since the normal condition of the R_W signal is "read" while the CPU is halted. P1-51(TP5) has a return to off (ROFF) format for this

test. In addition, the timing of this pin is set such that it will assert a logic level starting at 1600 nS into each pattern and return to the off 'Hi-Z' state at 1800 nS into each pattern. Since the quiescent state of TP4 is logic high when it isn't being back-driven, back-driving a logic low on TP4 causes a low pulse from 1600 nS to 1800 nS in the pattern. TP4 is given a logic low state causing this low pulse to occur in every read pattern. Each pulse latches the RAM data from the data bus. The data then propagates from the output of the lamp latch to the lamp drive edge pins DD7-DD0 via the lamp drivers to be tested during the following pattern.

To accomplish the RAM cell testing, this test writes each address within the 10-bit address space of this RAM bank with the 8 least significant bits of the address. The addresses are written in sequence 0x000 thru 0x3FF. Note that this address range notation represents the offset within this bank of RAM. The full 16-bit system address range for this bank is 0x1800 thru 0x1BFF which are the actual logic words placed on the address edge pins A15 thru A0. The resulting data set consists of the data values 0x00 thru 0xFF repeated four times. Then each of these RAM locations in this range is read and tested in the same order, 0x000 thru 0x3FF.

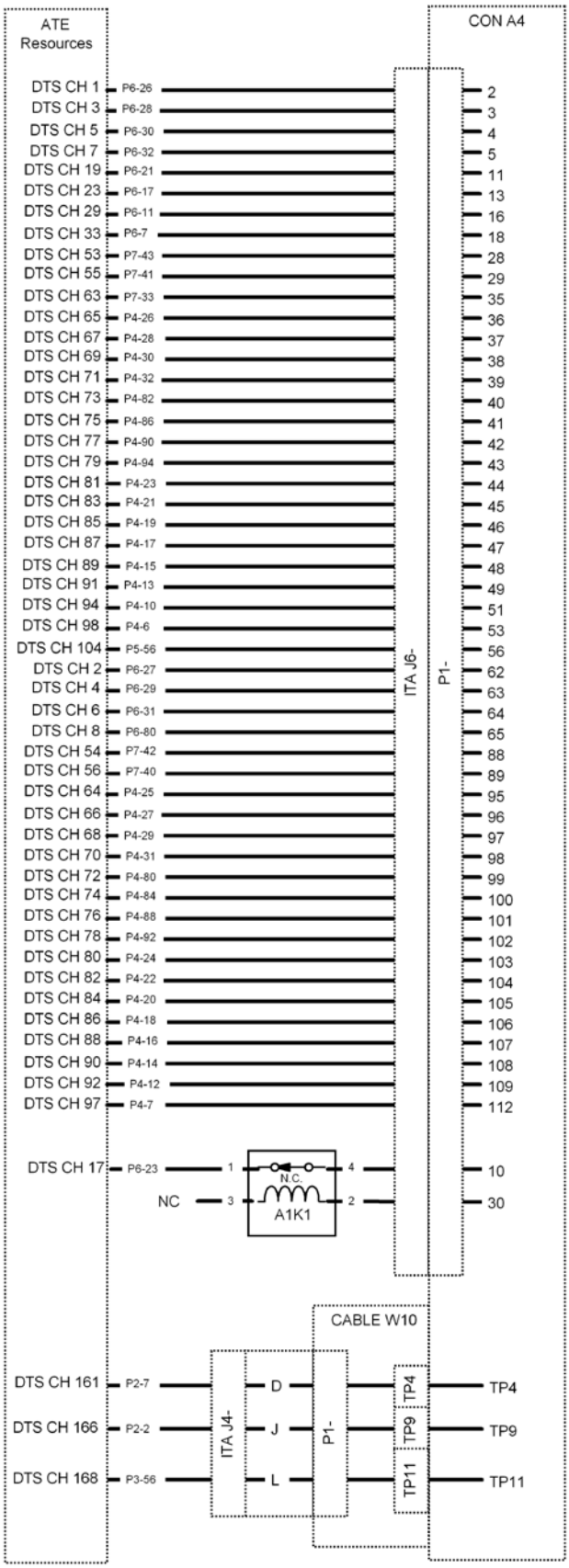
Then the same process of writing to the address range 0x000 thru 0x3FF is repeated identically, except that the 1's compliments of the 8 least significant bits of the address are written at each location. The resulting data set consists of the data values 0xFF thru 0x00 repeated four times. Then each of the RAM locations in this range is read and tested in the same order, 0x000 thru 0x3FF. At this point all RAM data cells have been tested for both the SA0 and SA1 state. However the upper two address edge pins of the RAM chips in this bank (U32 and U33) have not been tested.

At this point a very efficient and very thorough RAM address logic test will be used to detect any remaining failures of the address logic including failures of all address signals that could affect as few as one bit of data only. This test method goes beyond simply testing for OT1 on each address edge pins and covers the possibility that a failure may exist between any address line and any one data bit. To test one of these fundamental RAM address logic faults, a unique bit value must be written to a pair of address locations for the tested data bit. These data values stored in the tested bit must of course be 0 and 1 in order to be unique. The two locations must be the same address with only the state of the tested address line different between the two. Then, each of the two locations must be read and the data from the tested bit must be recovered intact. At this point the address line / data bit pair have been fully tested. In other words it has been proven that the tested data bit responds to address changes on the tested address line. This test must be performed for all address line / data bit combinations. This would be a number of tests equaling the number of address lines multiplied by the number of data lines. In this test this theory is highly compressed by two methods so that the all address logic of the 10 address line by 8 data line RAM bank can be tested by writing only 11 locations and then reading those 11 locations back. This is partly because 8 data bits can be written to and read at once which represents 8 tests at a time. Then it is more compressed because a single location can serve as the first address in all of the necessary pairs of address locations.

The first location written is 0x000 which is written with the data value 0xFF. Then each of the 10 address lines is complimented one at a time by writing to addresses 0x001, 0x002, 0x004, 0x008, 0x010, 0x020, 0x040, 0x080, 0x100, 0x200. These 11 locations represent 10 pairs of address locations with location 0x000 being the shared first location in each pair. Note that these address notations represent the offset within this bank of RAM. To all ten of these locations the data value 0x00 is written. Note that this represents the compliment of all eight data bits. Finally these 11 locations are read back. At this point all address logic of the current RAM bank has been tested.

One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. Pin 3 of A1K1 is connected to a switch that is left open for this test, effectively leaving Pin 3 Not Connected (NC). The test should pass without any errors.

Connection Path as follows:


ATE Resources
CON A4
DTS CH 1 P6-26
DTS CH 3 P6-28
DTS CH 5 P6-30
DTS CH 7 P6-32
DTS CH 19 P6-21
DTS CH 23 P6-17
DTS CH 29 P6-11
DTS CH 33 P6-7
DTS CH 53 P7-43
DTS CH 55 P7-41
DTS CH 63 P7-33
DTS CH 65 P4-26
DTS CH 67 P4-28
DTS CH 69 P4-30
DTS CH 71 P4-32
DTS CH 73 P4-82
DTS CH 75 P4-86
DTS CH 77 P4-90
DTS CH 79 P4-94
DTS CH 81 P4-23
DTS CH 83 P4-21
DTS CH 85 P4-19
DTS CH 87 P4-17
DTS CH 89 P4-15
DTS CH 91 P4-13
DTS CH 94 P4-10
DTS CH 98 P4-6
DTS CH 104 P5-56
DTS CH 2 P6-27
DTS CH 4 P6-29
DTS CH 6 P6-31
DTS CH 8 P6-80
DTS CH 54 P7-42
DTS CH 56 P7-40
DTS CH 64 P4-25
DTS CH 66 P4-27
DTS CH 68 P4-29
DTS CH 70 P4-31
DTS CH 72 P4-80
DTS CH 74 P4-84
DTS CH 76 P4-88
DTS CH 78 P4-92
DTS CH 80 P4-24
DTS CH 82 P4-22
DTS CH 84 P4-20
DTS CH 86 P4-18
DTS CH 88 P4-16
DTS CH 90 P4-14
DTS CH 92 P4-12
DTS CH 97 P4-7
ITA J6-
P1-
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88
89
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107
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109
112
DTS CH 17 P6-23
NC
N.C.
A1K1
1
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CABLE W10
DTS CH 161 P2-7
DTS CH 166 P2-2
DTS CH 168 P3-56
ITA J4-
D
J
L
P1-
TP4
TP9
TP11
TP4
TP9
TP11

Step 404 RAM Bank 3 Data Test

This test consists of a manually generated digital test binary file, '6802.DTB', executed using the M910NAM non ATLAS module. This test completely tests the RAM chips of the fourth RAM bank (U43, U42). This includes full cell testing and full address testing. This is accomplished by first resetting the 6802 CPU (U65) by momentarily back-driving a logic low on TP11. Then the CPU is placed in the HALT condition by placing a logic low on P1-18. This causes the CPU BA output (U65-7) to go to logic high which in turn disables the CPU address buffer (U35 and U45) and CPU data buffer (U64) and in effect causes the CPU to surrender control of the address and data buses. Also while in the HALT state the CPU R/W line (U65-34) remains in the logic high (read) state.

Each write to the RAM is accomplished within a single pattern. The outer data buffer (U24) is placed in the inward data direction by back-driving a logic low on P1-16 (TP7). This causes no change at the moment but prevents the data direction of the outer data buffer from changing when the write pulse is applied later. Then P1-53 is back-driven to logic low to enable the outer data buffer (U24) since this buffer will not normally be decoded by the address decoder (U15) when a RAM address is present because I/O from the RAM is normally only to the CPU which does not require the use of this buffer. P1-51 (TP5) has a return to off (ROFF) format for this test. In addition, the timing of this pin is set such that it will assert a logic level starting at 900 nS into each pattern and return to the off 'Hi-Z' state at 1800 nS into each pattern. Since the quiescent state of P1-51 is logic high when it isn't being back-driven, back-driving a logic low on P1-51 causes a low pulse from 900 nS to 1800 nS in the pattern. This pulse enables the write circuit in the currently addressed RAM and effectively strobes one byte of data to be written. In each write pattern the address edge pins A15-A0 (P1-42, 41, 38, 40, 37, 39, 36, 35, 95, 96, 97, 98, 99, 100, 101, and 102) and data edge pins D7-D0 (P1-46, 45, 44, 43, 103, 104, 105, and 106) are setup with the write data and write destination. Logic changes on the address edge pins A15-A0 and data edge pins D7-D0 occur at 0 nS into each pattern. This timing ensures data and address setup and hold times are met relative to the write pulse on P1-51.

Each read is also accomplished within a single pattern, however the propagation of the data to the edge pin extends into the next pattern so that each data byte is actually tested in the pattern following the read pattern. In other words the data is tested while the next byte of RAM is being read. This is due to the propagation delay of the lamp drivers (U61, U62, U71, and U72). The outer data buffer (U24) is not used in the read so it is left in the disabled state and thus the directional setting is also irrelevant. The outer data buffer can not be used to read the RAM because it is impossible to place it in the correct direction while the RAM is in the read state. Read data is delivered to the tester via the lamp state latch (U52) and the lamp drivers and associated edge pins DD7-DD0 (P1-62, 3, 64, 5, 2, 63, 4, 65). RAM data is transferred the data bus simply by placing the RAM source address on the address edge pins A15-A0, since the normal condition of the R_W signal is "read" while the CPU is halted. P1-51 (TP5) has a return to off (ROFF) format for this test. In addition, the timing of this pin is set such that it will assert a logic level starting at

1600 nS into each pattern and return to the off 'Hi-Z' state at 1800 nS into each pattern. Since the quiescent state of TP4 is logic high when it isn't being back-driven, back-driving a logic low on TP4 causes a low pulse from 1600 nS to 1800 nS in the pattern. TP4 is given a logic low state causing this low pulse to occur in every read pattern. Each pulse latches the RAM data from the data bus. The data then propagates from the output of the lamp latch to the lamp drive edge pins DD7-DD0 via the lamp drivers to be tested during the following pattern.

To accomplish the RAM cell testing, this test writes each address within the 10-bit address space of this RAM bank with the 8 least significant bits of the address. The addresses are written in sequence 0x000 thru 0x3FF. Note that this address range notation represents the offset within this bank of RAM. The full 16-bit system address range for this bank is 0x1C00 thru 0x1FFF which are the actual logic words placed on the address edge pins A15 thru A0. The resulting data set consists of the data values 0x00 thru 0xFF repeated four times. Then each of these RAM locations in this range is read and tested in the same order, 0x000 thru 0x3FF.

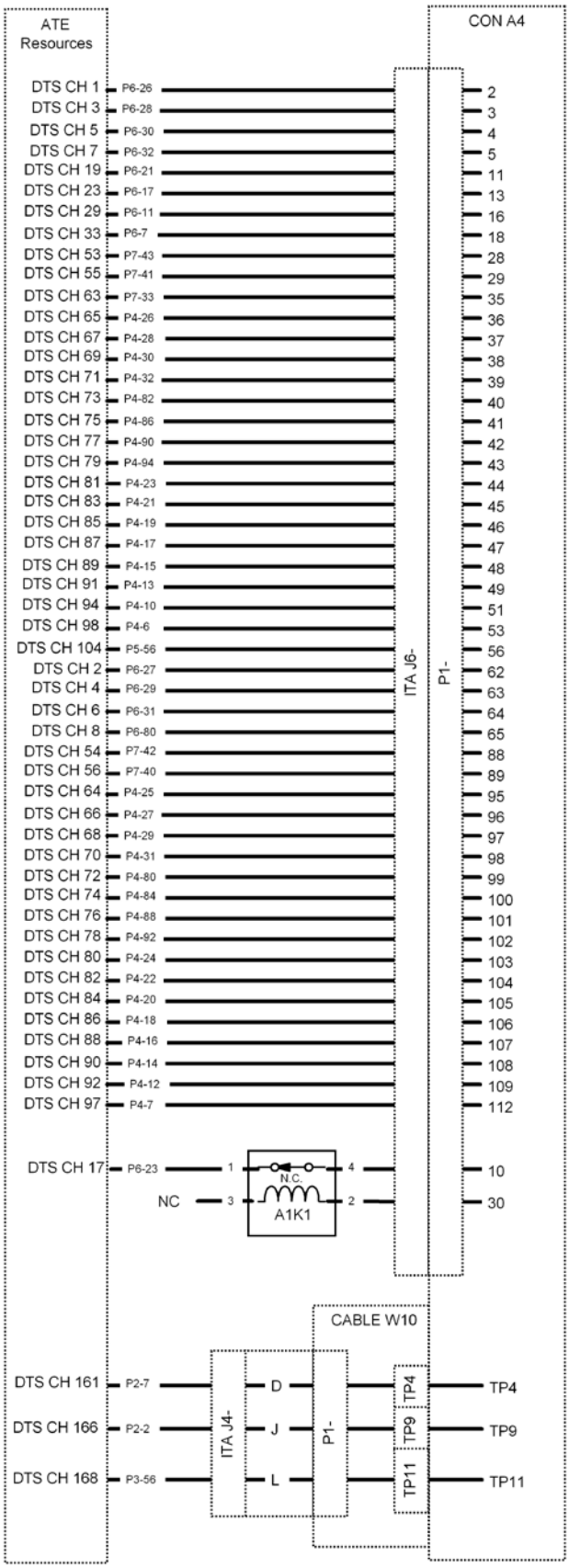
Then the same process of writing to the address range 0x000 thru 0x3FF is repeated identically, except that the 1's compliments of the 8 least significant bits of the address are written at each location. The resulting data set consists of the data values 0xFF thru 0x00 repeated four times. Then each of the RAM locations in this range is read and tested in the same order, 0x000 thru 0x3FF. At this point all RAM data cells have been tested for both the SA0 and SA1 state. However the upper two address edge pins of the RAM chips in this bank (U35 and U45) have not been tested.

At this point a very efficient and very thorough RAM address logic test will be used to detect any remaining failures of the address logic including failures of all address signals that could affect as few as one bit of data only. This test method goes beyond simply testing for OT1 on each address edge pins and covers the possibility that a failure may exist between any address line and any one data bit. To test one of these fundamental RAM address logic faults, a unique bit value must be written to a pair of address locations for the tested data bit. These data values stored in the tested bit must of course be 0 and 1 in order to be unique. The two locations must be the same address with only the state of the tested address line different between the two. Then, each of the two locations must be read and the data from the tested bit must be recovered intact. At this point the address line / data bit pair have been fully tested. In other words it has been proven that the tested data bit responds to address changes on the tested address line. This test must be performed for all address line / data bit combinations. This would be a number of tests equaling the number of address lines multiplied by the number of data lines. In this test this theory is highly compressed by two methods so that the all address logic of the 10 address line by 8 data line RAM bank can be tested by writing only 11 locations and then reading those 11 locations back. This is partly because 8 data bits can be written to and read at once which represents 8 tests at a time. Then it is more compressed because a single location can serve as the first address in all of the necessary pairs of address locations.

The first location written is 0x000 which is written with the data value 0xFF. Then each of the 10 address lines is complimented one at a time by writing to addresses 0x001, 0x002, 0x004, 0x008, 0x010, 0x020, 0x040, 0x080, 0x100, 0x200. These 11 locations represent 10 pairs of address locations with location 0x000 being the shared first location in each pair. Note that these address notations represent the offset within this bank of RAM. To all ten of these locations the data value 0x00 is written. Note that this represents the compliment of all eight data bits. Finally these 11 locations are read back. At this point all address logic of the current RAM bank has been tested.

One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. Pin 3 of A1K1 is connected to a switch that is left open for this test, effectively leaving Pin 3 Not Connected (NC). The test should pass without any errors.

Connection Path as follows:


ATE Resources
CON A4
DTS CH 1 P6-26
DTS CH 3 P6-28
DTS CH 5 P6-30
DTS CH 7 P6-32
DTS CH 19 P6-21
DTS CH 23 P6-17
DTS CH 29 P6-11
DTS CH 33 P6-7
DTS CH 53 P7-43
DTS CH 55 P7-41
DTS CH 63 P7-33
DTS CH 65 P4-26
DTS CH 67 P4-28
DTS CH 69 P4-30
DTS CH 71 P4-32
DTS CH 73 P4-82
DTS CH 75 P4-86
DTS CH 77 P4-90
DTS CH 79 P4-94
DTS CH 81 P4-23
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DTS CH 87 P4-17
DTS CH 89 P4-15
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DTS CH 94 P4-10
DTS CH 98 P4-6
DTS CH 104 P5-56
DTS CH 2 P6-27
DTS CH 4 P6-29
DTS CH 6 P6-31
DTS CH 8 P6-80
DTS CH 54 P7-42
DTS CH 56 P7-40
DTS CH 64 P4-25
DTS CH 66 P4-27
DTS CH 68 P4-29
DTS CH 70 P4-31
DTS CH 72 P4-80
DTS CH 74 P4-84
DTS CH 76 P4-88
DTS CH 78 P4-92
DTS CH 80 P4-24
DTS CH 82 P4-22
DTS CH 84 P4-20
DTS CH 86 P4-18
DTS CH 88 P4-16
DTS CH 90 P4-14
DTS CH 92 P4-12
DTS CH 97 P4-7
ITA J6-
P1-
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64
65
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89
95
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107
108
109
112
DTS CH 17 P6-23
NC
N.C.
A1K1
1
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30
CABLE W10
DTS CH 161 P2-7
DTS CH 166 P2-2
DTS CH 168 P3-56
ITA J4-
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J
L
P1-
TP4
TP9
TP11
TP4
TP9
TP11

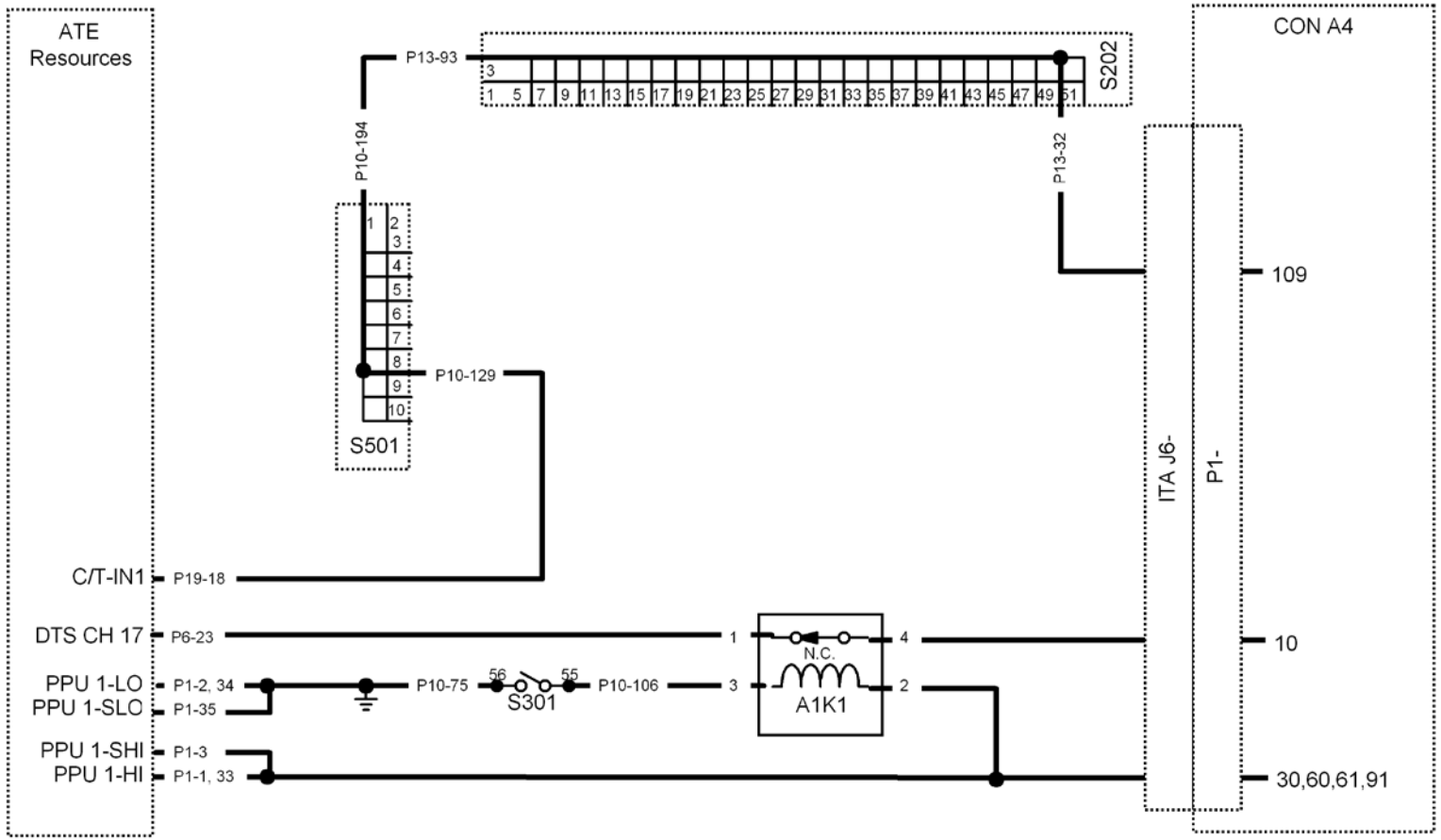
MODULE 5 CLOCK OSCILLATOR TEST

Module 5 verifies the operation of the on board crystal oscillator consisting of Y1 and U65.

Step 501 CPU Clock Pickup Test

This test verifies that the frequency of the E clock output of the CPU (U65) at P1-109 is also within tolerance. Instead of supplying an external clock signal via P1-10, the on-board crystal oscillator is allowed to free run during this test. As a result this test indirectly verifies that the on-board crystal oscillator is functioning at the correct frequency and that its output is effectively picked up by the CPU. The frequency of the CPU E clock signal at P1-109 is measured and verified to be between 996.25 kHz and 1.00375 MHz. The E clock output frequency should be exactly 1 / 4 of the frequency of the sinusoidal signal on P1-10 due to the digital nature of the internal clock divider of the CPU. Therefore the crystal oscillator frequency is verified to be between 3.985 MHz and 4.015 MHz using the Counter/Timer. P1-10 is isolated for the test by energizing ITA relay A1K1, which is Normally Closed (N.C.), which is accomplished by connecting GND to the relay coil.

Connection Path as follows:


ATE
Resources
CON A4
P13-93
S202
P10-194
P13-32
S501
P10-129
ITA J6-
P1-
109
10
30,60,61,91
C/T-IN1
P19-18
DTS CH 17
P6-23
PPU 1-LO
P1-2, 34
PPU 1-SLO
P1-35
PPU 1-SHI
P1-3
PPU 1-HI
P1-1, 33
P10-75
S301
P10-106
N.C.
A1K1

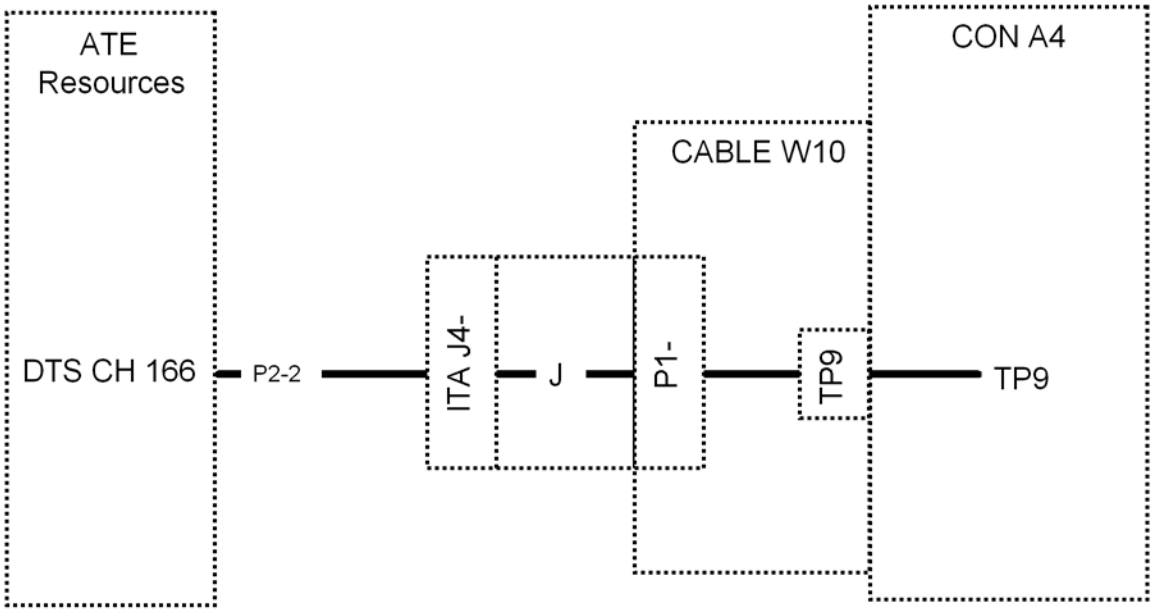
MODULE 6 RESET CIRCUIT TEST

Module 6 tests the CPU reset circuitry. The CPU reset circuitry consists of a voltage threshold detection circuit (U82, R9, R10, R11 and R14), and a one-shot circuit (U63, C21, R8 and R12). The voltage threshold detection circuit produces a logic low signal on TP9 when the input power supply voltage of the CCA is less than 4.7816 Volts and otherwise produces a logic high signal on TP9. The TP9 signal is delivered to the positive trigger of the one-shot circuit. When the rising CCA power supply voltage crosses this threshold, a positive going transition occurs at the one-shot positive trigger, triggering it and producing a nominal 54.8 mS, low /RESET pulse at the /Q output. The low /RESET pulse resets the CPU (U65) and the programmable timer module (PTM U51). The 54.8 mS pulse is required to ensure that the /RESET pulse is of adequate length. The one-shot will be retriggered each time the power supply voltage crosses the threshold in the positive direction to ensure that the CPU and PTM components are reset each time the power supply falls below the threshold and then has stabilized at an acceptable operating level.

Step 601 Under-voltage Test

In this test the power supply voltage is changed from the nominal 5.1 V to 4.5 V and TP9 is verified to be logic low.

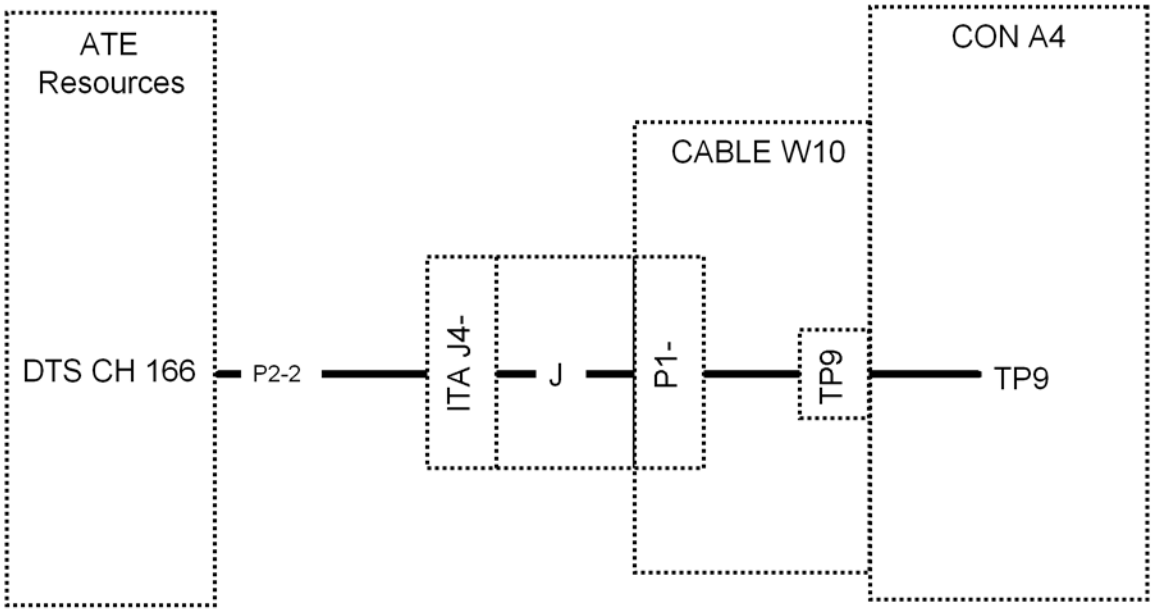
Connection Path as follows:



Step 602 Under-voltage Recovery Test

In this test the power supply voltage has been returned to 5.1 V (see Step 601) and TP9 is verified to have returned to logic high.

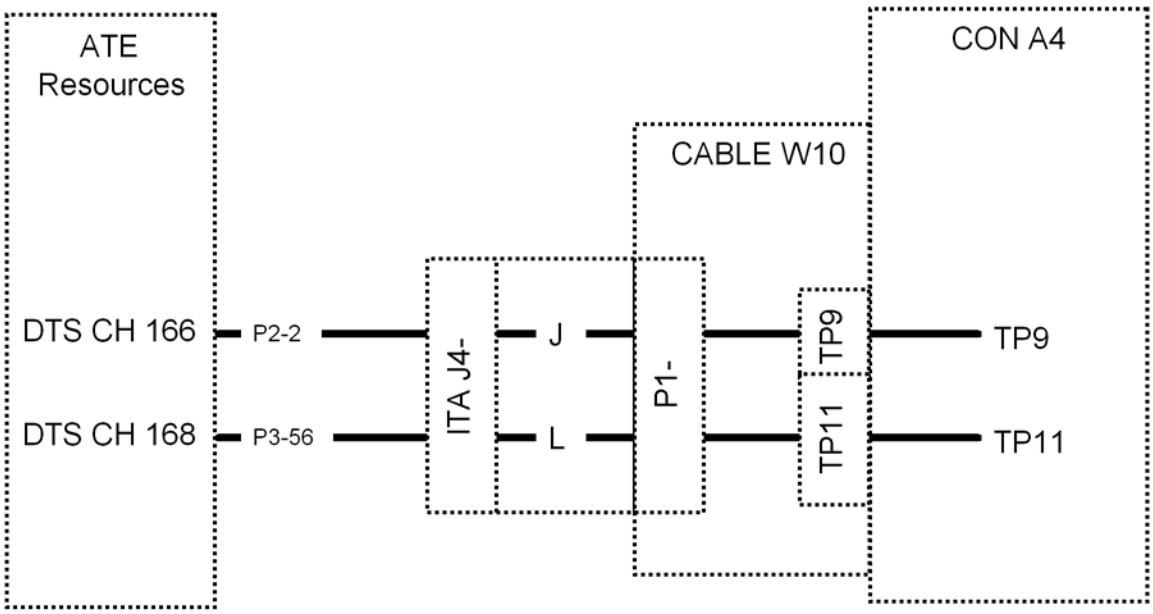
Connection Path as follows:



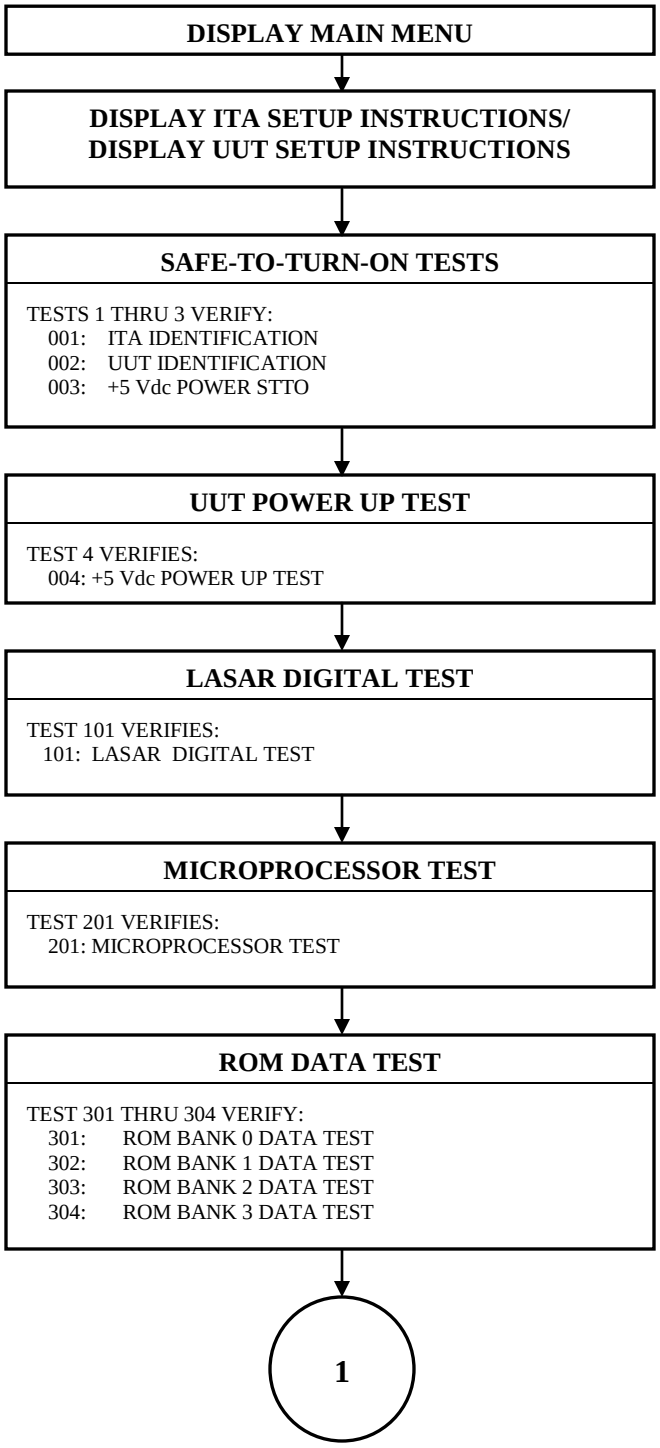
Step 603 One Shot Pulse Width Test

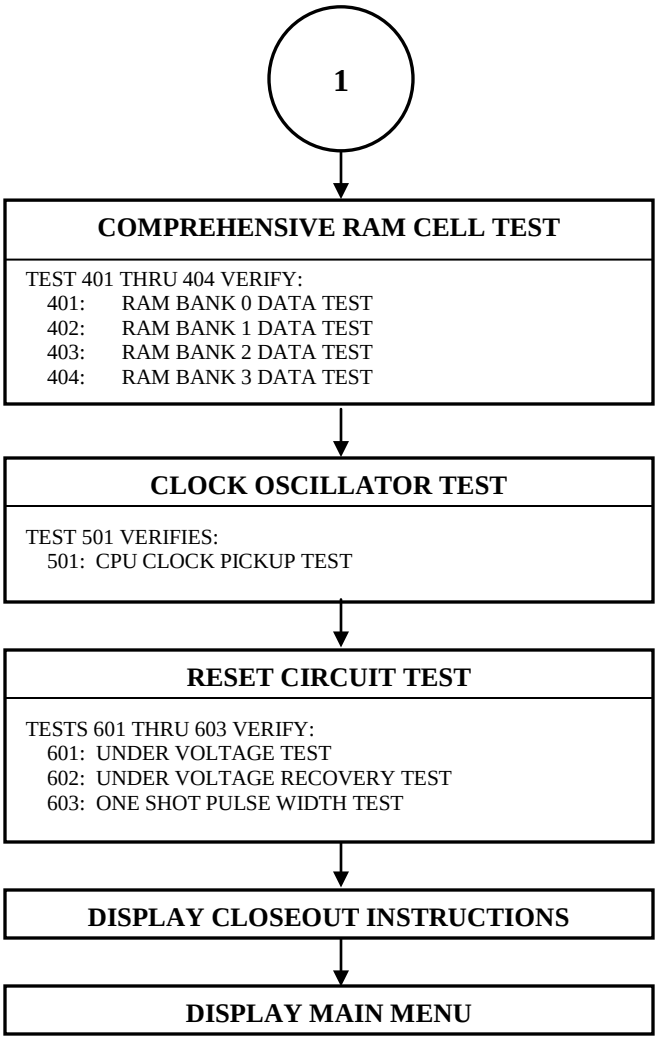
This test consists of a manually generated digital test binary file, 'PW.DTB', executed using the M910NAM non ATLAS module. In this test TP9 is back driven to logic low, then returned to the off state at which point it is pulled back to logic high by the UUT. This logic low to high transition occurs at the positive trigger input of the one-shot (U63, C21, R8 and R12). The one-shot triggers and an envelope test is performed to verify the correct duration of the /RESET pulse at TP11.

Connection Path as follows:



FUNCTIONAL FLOW CHART (FFC)




1
COMPREHENSIVE RAM CELL TEST
TEST 401 THRU 404 VERIFY:
401: RAM BANK 0 DATA TEST
402: RAM BANK 1 DATA TEST
403: RAM BANK 2 DATA TEST
404: RAM BANK 3 DATA TEST
CLOCK OSCILLATOR TEST
TEST 501 VERIFIES:
501: CPU CLOCK PICKUP TEST
RESET CIRCUIT TEST
TESTS 601 THRU 603 VERIFY:
601: UNDER VOLTAGE TEST
602: UNDER VOLTAGE RECOVERY TEST
603: ONE SHOT PULSE WIDTH TEST
DISPLAY CLOSEOUT INSTRUCTIONS
DISPLAY MAIN MENU