English Language Test Description

Contract Number: N00244-09-C-0054

For

Unit Under Test

UUT Nomenclature: DISPLAY BOARD CCA
UUT Part Number: 5428412
UUT Reference Designator: DDM A1

From

Assault Amphibious Vehicle
AN/PSM-115

ATE (Automated Test Equipment) SYSTEM

AN/USM-657B(V)2 Third Echelon Test System (TETS)
AN/USM-717(V)2 Virtual Instrument Portable Equipment Repair / Tester (VIPER/T)

Developed by

ManTech Telecommunications and Information Systems Corp.
14119A Sullyfield Circle
Chantilly, Virginia 20151

Prepared By	Signature	Date Prepared	Date Submitted

Approved By	Signature	Date Received	Date Approved

ELTD REVISION SUMMARY

Revision Number	Date	Reason	Approved By – Date Approved
-	05/25/2010	ORIGINAL ISSUE	N. Dhami – 05/25/2010
A	07/20/2010	Per ECO-AAV-2010-0029	

1. Introduction

The Unit Under Test (UUT) for this English Language Test Description (ELTD) is the Display Board Circuit Card Assembly (CCA), Part Number 5428412. The CCA is reference designator DDM A1 in the Drivers Display Module Line Replaceable Unit (LRU) part number 5429249. The LRU resides in the Assault Amphibious Vehicle (AAV) Weapon System.

1.1. Scope

An ELTD is a detailed supplementary document consisting of textual test descriptions with graphical representation of signal interconnectivity and a functional flow chart.

1.2. Purpose

The purpose of this document is to provide English language test descriptions for the TP_AAV_DDM_A1 test program, to a level of detail used for maintenance purposes. The TP_AAV_DDM_A1 test program makes up part of the AN/PSM-115 Application Program Set (APS).

1.3. Content Arrangement

The document is laid out in the sequence the Test Program Set (TPS) would be executed when a 95 “Run All Mods” is entered in the main menu. A paragraph at the beginning of each module will describe the test description for that module. Each step will contain a description for that particular test followed by a graphical representation of the connections made from the receiver, through the Interface Test Adapter (ITA) and DDM Adapter to the Display Board CCA. A Functional Flow Chart resides at the end of the document.

2. English Language Test Description (ELTD)

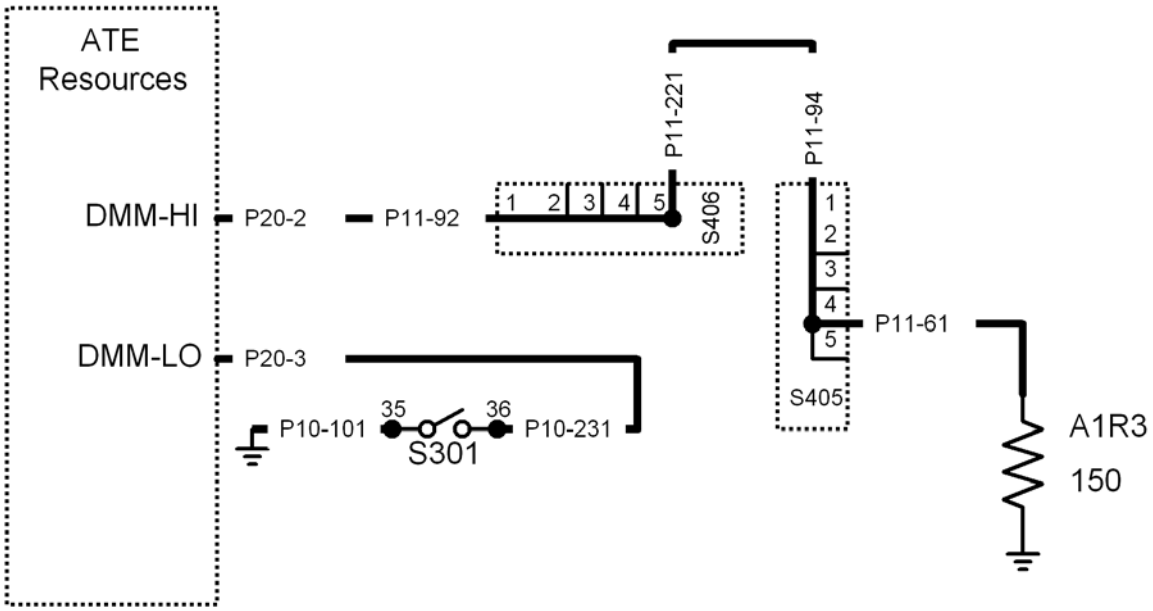
WEAPON SYSTEM: Assault Amphibious Vehicle (AAV)
UNIT UNDER TEST: 5428412
TEST PROGRAM SET: TP_AAV_DDM_A1

SAFE TO TURN ON TESTS

Step 1 ITA Identification

Test step 1 verifies the correct ITA is installed by using the DMM to measure the resistance of ITA A1R3. The resistance should be from 149 ohms to 155 ohms.

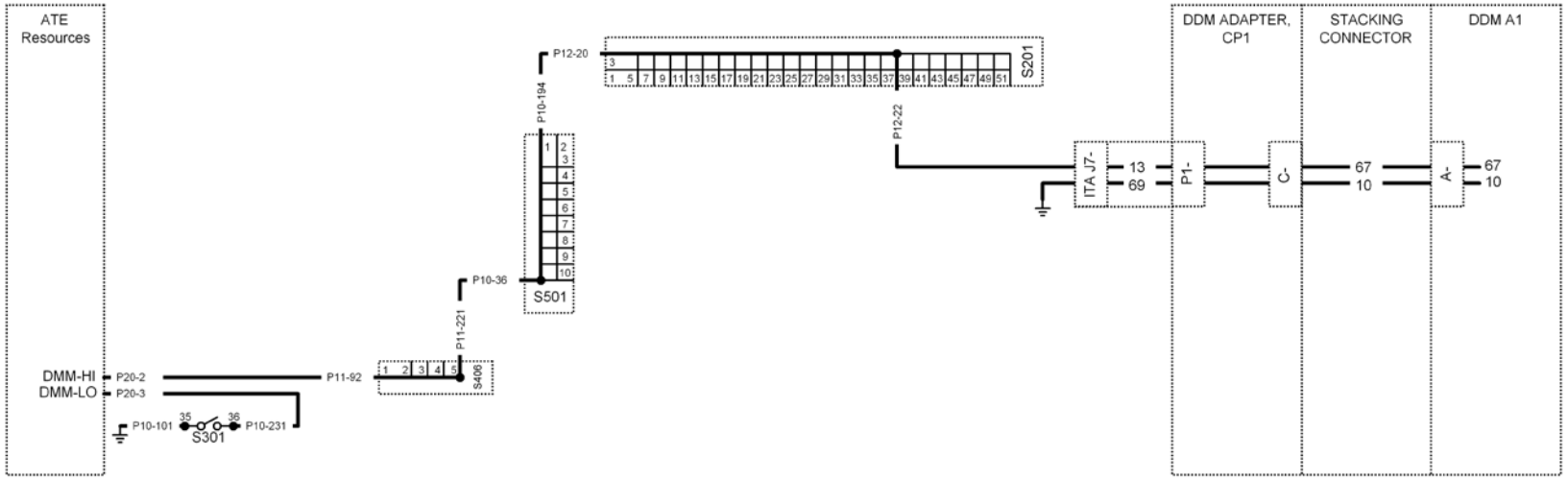
Connection Path as follows:



Step 2 UUT Identification (C-67/GND)

Test step 2 verifies the correct UUT is connected to the ITA by using the DMM to measure the resistance of R9 and R10 between C-67 and ground. The resistance should be less than 5,000 ohms.

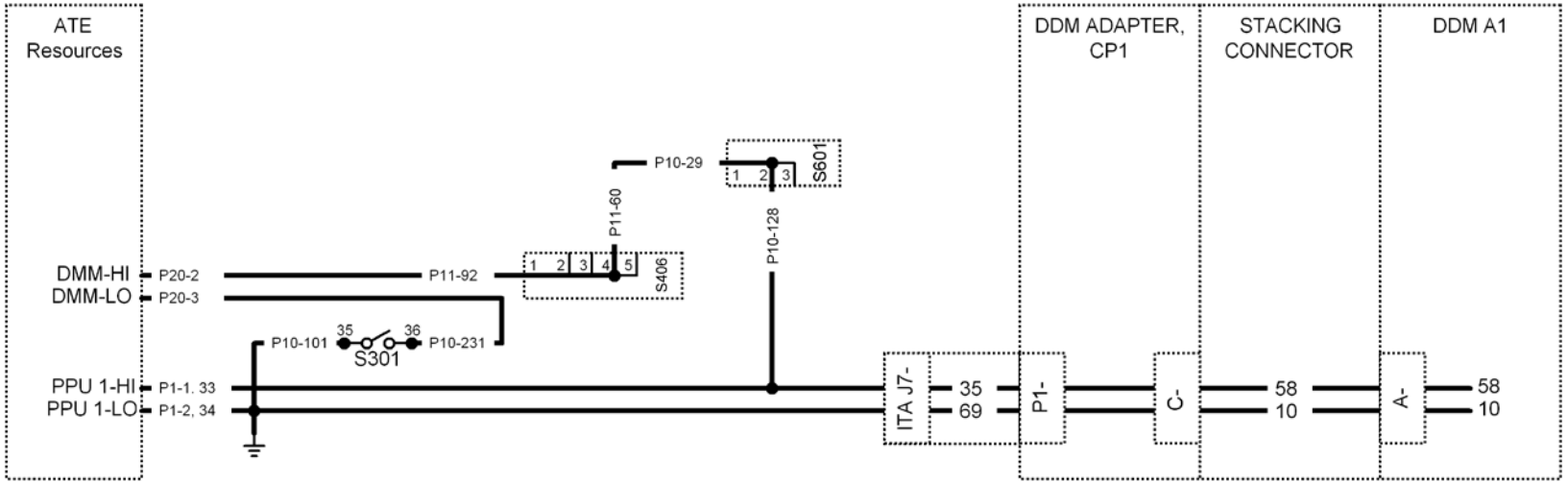
Connection Path as follows:


ATE Resources
DMM-HI
DMM-LO
P20-2
P20-3
P11-92
P10-101
P10-231
S301
35
36
P11-221
S406
P10-36
S501
P10-194
P12-20
S201
P12-22
ITA J7-
13
69
DDM ADAPTER, CP1
P1-
C-
STACKING CONNECTOR
67
10
DDM A1
A-
67
10

Step 3 +5 VDC Power STTO

Test step 3 verifies the +5 Vdc is safe to apply power by connecting PPU1 to the UUT but only applying +1.0 Vdc at 0.100 A. The DMM is used to measure the voltage from C-58 to GND. The voltage should be greater than 0.9 Vdc. If an overload condition is present PPU1 will exceed its current limit and turn off before the measurement causing the test to fail.

Connection Path as follows:


ATE
Resources
DDM ADAPTER,
CP1
STACKING
CONNECTOR
DDM A1
DMM-HI
DMM-LO
PPU 1-HI
PPU 1-LO
P20-2
P20-3
P1-1, 33
P1-2, 34
P11-92
P10-101
P10-231
S301
P10-29
P11-60
P10-128
S601
S406
1 2 3
1 2 3 4 5
35
36
ITA J7-
35
69
P1-
C-
58
10
A-
58
10

UUT POWER UP

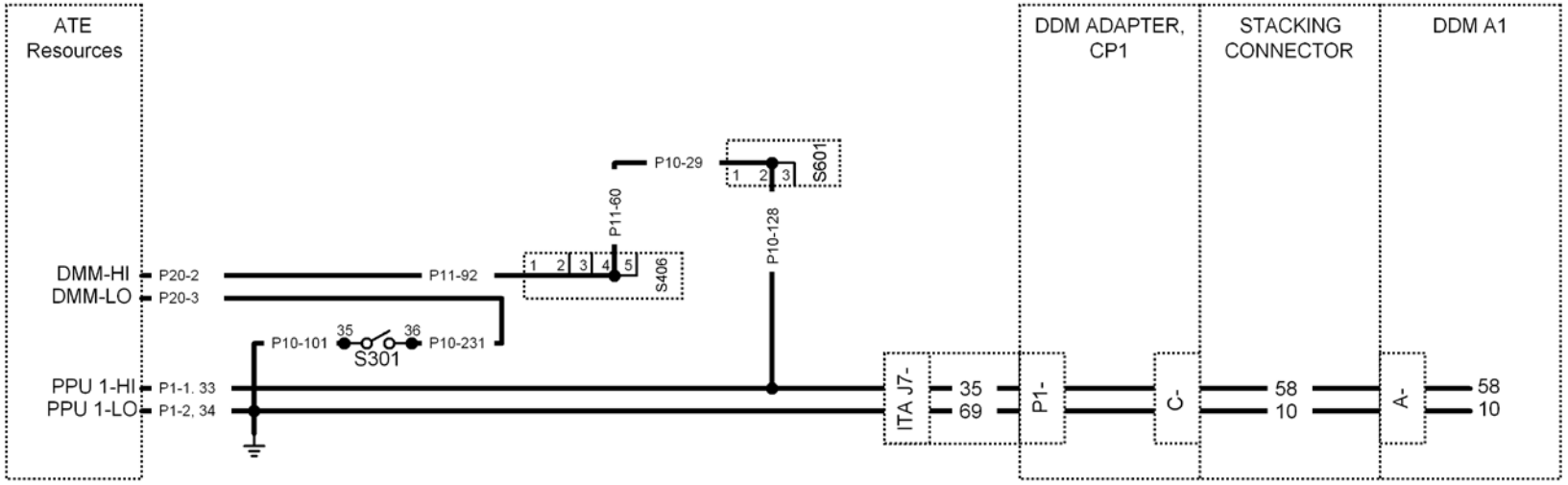
+5 Vdc at 1.0 A with a tolerance of ±0.25 Vdc and +250 Vdc at 0.3 A with a tolerance of ±0.25 Vdc are required to power the UUT.

UUT POWER UP TESTS

Step 4 +5VDC Power On Test

Test step 4 verifies PPU1 can deliver +5 Vdc to the UUT by using the DMM to measure the voltage between C-58 and GND. The voltage should be from 4.75 Vdc to 5.25 Vdc. PPU1 remains connected to the UUT for the remainder of testing.

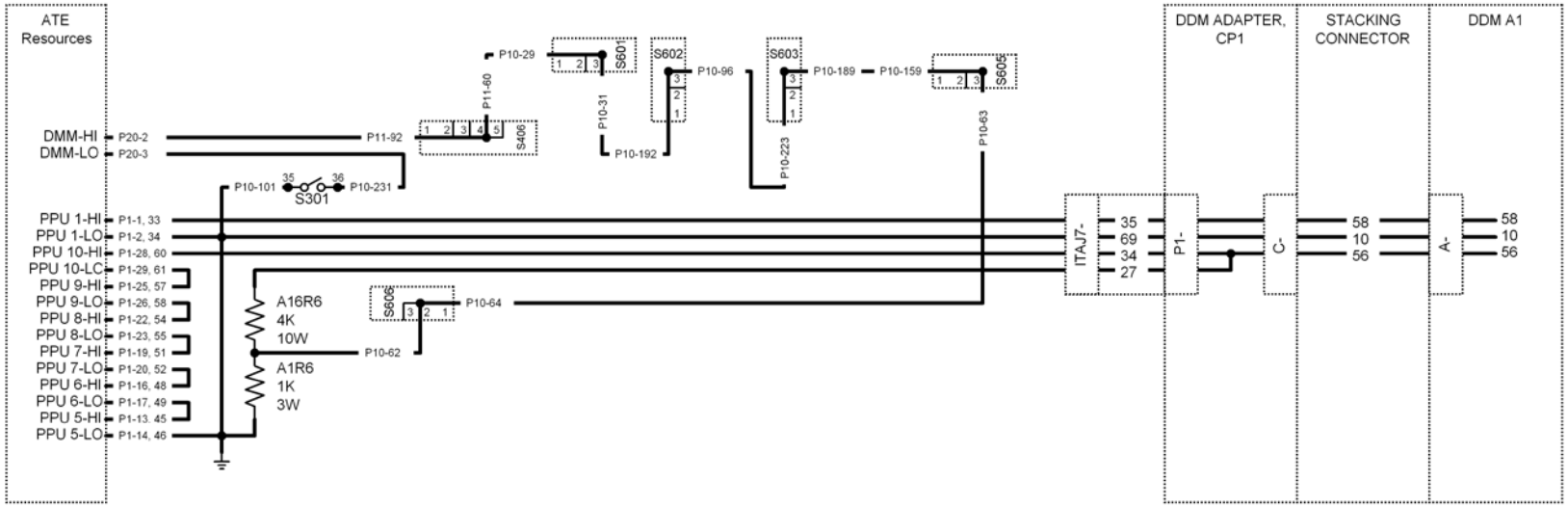
Connection Path as follows:


ATE
Resources
DDM ADAPTER,
CP1
STACKING
CONNECTOR
DDM A1
DMM-HI
DMM-LO
PPU 1-HI
PPU 1-LO
P20-2
P20-3
P1-1. 33
P1-2, 34
P11-92
P11-60
P10-29
P10-128
P10-101
P10-231
S301
S406
S601
1 2 3 4 5
1 2 3
35
36
ITA J7-
35
69
P1-
C-
58
10
A-
58
10

Step 5 +250VDC Power On Test

Test step 5 verifies PPU5 through PPU10 can deliver +250 Vdc to the UUT by using the DMM to measure the voltage across 1A1R6. 1A1R6 is part of a voltage divider that consists of an upper divider resistor 1A16R6 (4K, 12.5 W) and lower divider resistor 1A1R6 (1K, 3W). 1A16R6 is connected to the UUT 250 V output C-56. 1A16R6 and 1A1R6 form a series 5K circuit to ground. Then the voltage is measured across 1A1R6 to obtain a 1/5th, or 20% voltage reading from the 250 VDC output. The voltage should be from 47.5 Vdc to 5.25 Vdc. This effectively applies a tolerance of 237.5 Vdc to 262.5 Vdc to the 250 Vdc nominal UUT output at C-56. PPU5 through PPU10 remains connected to the UUT for the remainder of testing.

Connection Path as follows:


ATE Resources
DMM-HI P20-2
DMM-LO P20-3
PPU 1-HI P1-1, 33
PPU 1-LO P1-2, 34
PPU 10-HI P1-28, 60
PPU 10-LO P1-29, 61
PPU 9-HI P1-25, 57
PPU 9-LO P1-26, 58
PPU 8-HI P1-22, 54
PPU 8-LO P1-23, 55
PPU 7-HI P1-19, 51
PPU 7-LO P1-20, 52
PPU 6-HI P1-16, 48
PPU 6-LO P1-17, 49
PPU 5-HI P1-13, 45
PPU 5-LO P1-14, 46
P11-92
P11-60
S406
P10-29
S601
P10-31
P10-192
S602
P10-96
S603
P10-189
P10-159
S605
P10-223
P10-63
P10-101
S301
P10-231
A16R6
4K
10W
A1R6
1K
3W
S606
P10-64
P10-62
ITAJ7-
35
69
34
27
P1-
C-
A-
DDM ADAPTER, CP1
STACKING CONNECTOR
DDM A1
58
10
56
58
10
56

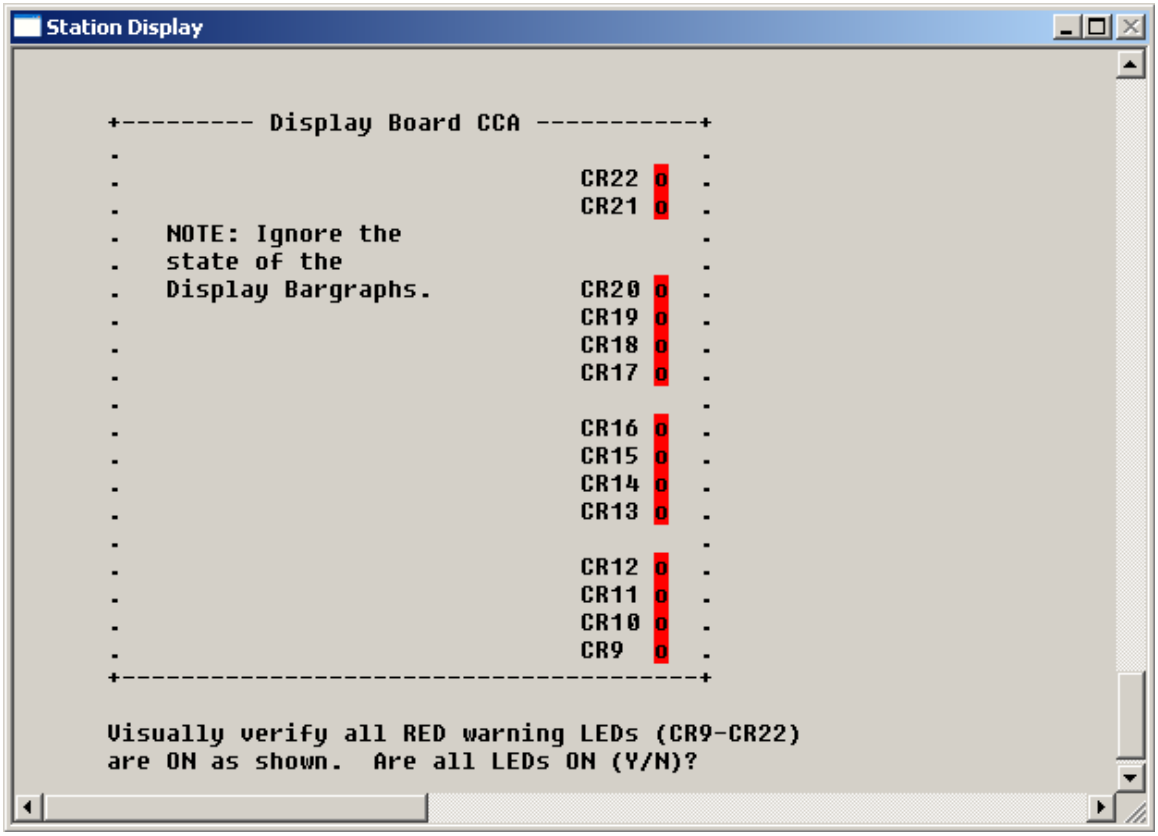
MODULE 1 WARNING LAMP DISPLAY TESTS

Module 1 tests the display board to ensure everything is displaying correctly except for the diming circuitry. This includes warning LEDs, bar graphs all on or off, at different levels, and with different variations.

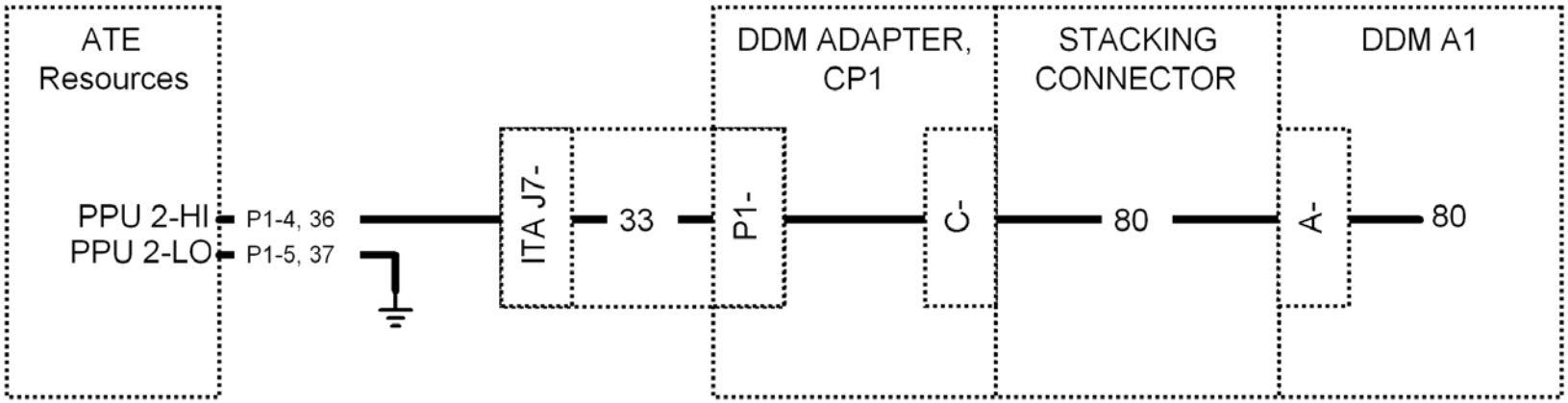
Step 101 Warning Lamp Test

Test step 101 verifies that LEDs CR9-CR22 and current limiting resistors R67-R73 are functional by verifying that the LEDs light. The operator must visually verify operation of the LEDs.

Operator Evaluation:



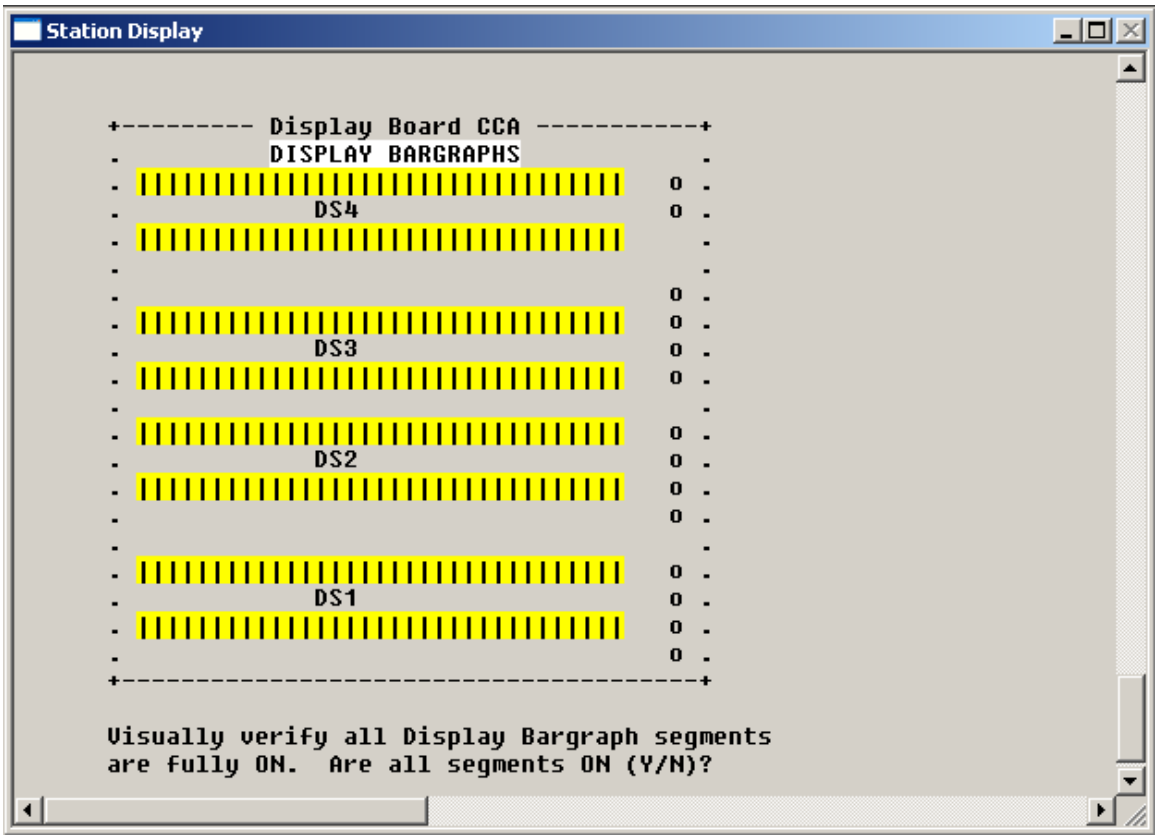
Connection Path as follows:


ATE
Resources
PPU 2-HI
PPU 2-LO
P1-4, 36
P1-5, 37
ITA J7-
33
DDM ADAPTER,
CP1
P1-
C-
STACKING
CONNECTOR
80
DDM A1
A-
80

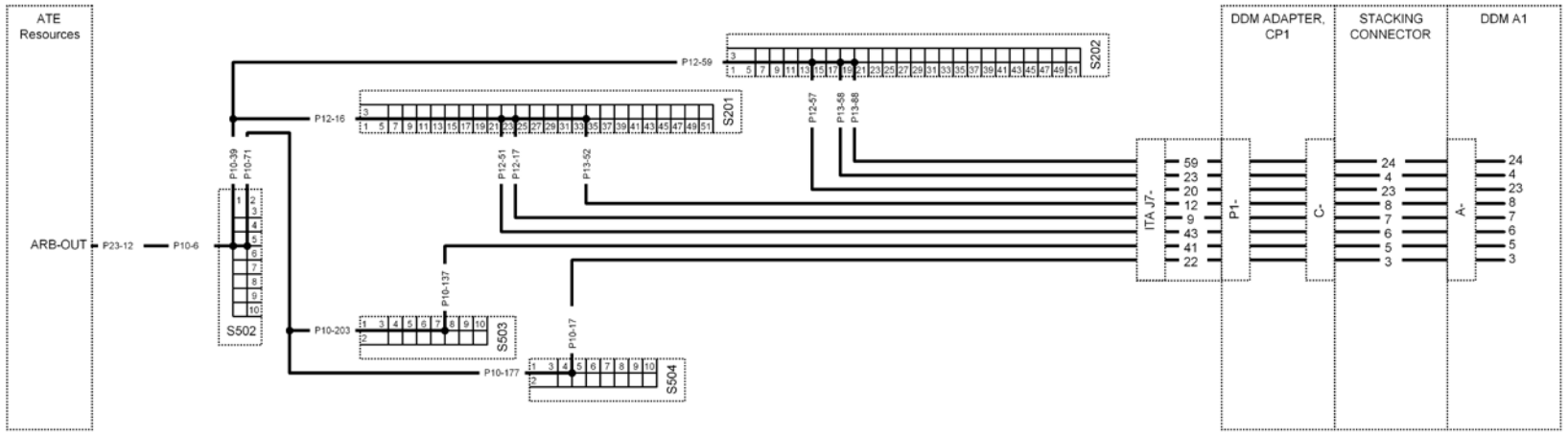
Step 102 Display Bar Graph ON Test

Test step 102 verifies that bar graph displays DS1-DS4 and associated driving circuitry are functional by verifying that all segments of the bar graph displays are able to light. The operator must visually verify operation of the bar graph displays.

Operator Evaluation:



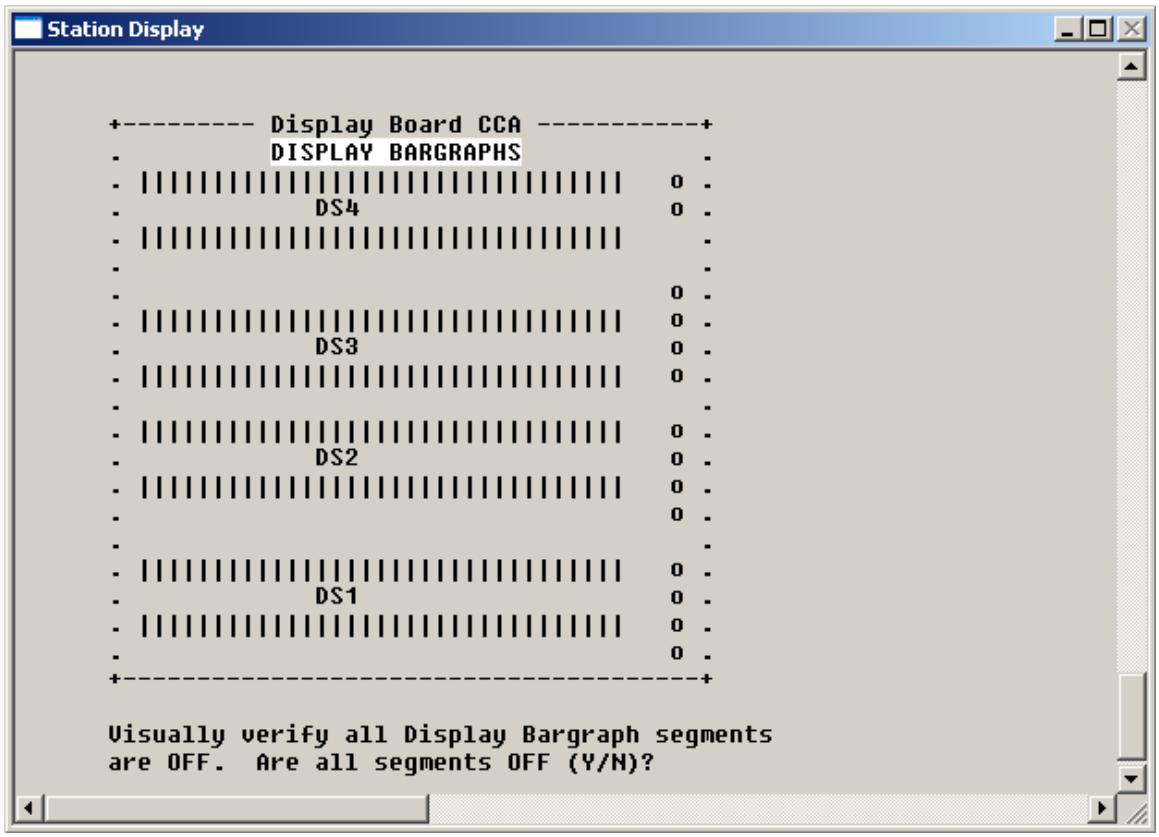
Connection Path as follows:


ATE Resources
ARB-OUT
P23-12
P10-6
P10-39
P10-71
S502
P12-59
S202
P12-16
S201
P12-57
P13-58
P13-88
P12-51
P12-17
P13-52
P10-137
P10-203
S503
P10-17
P10-177
S504
ITA J7-
59
23
20
12
9
43
41
22
DDM ADAPTER, CP1
P1-
C-
STACKING CONNECTOR
A-
DDM A1
24
4
23
8
7
6
5
3

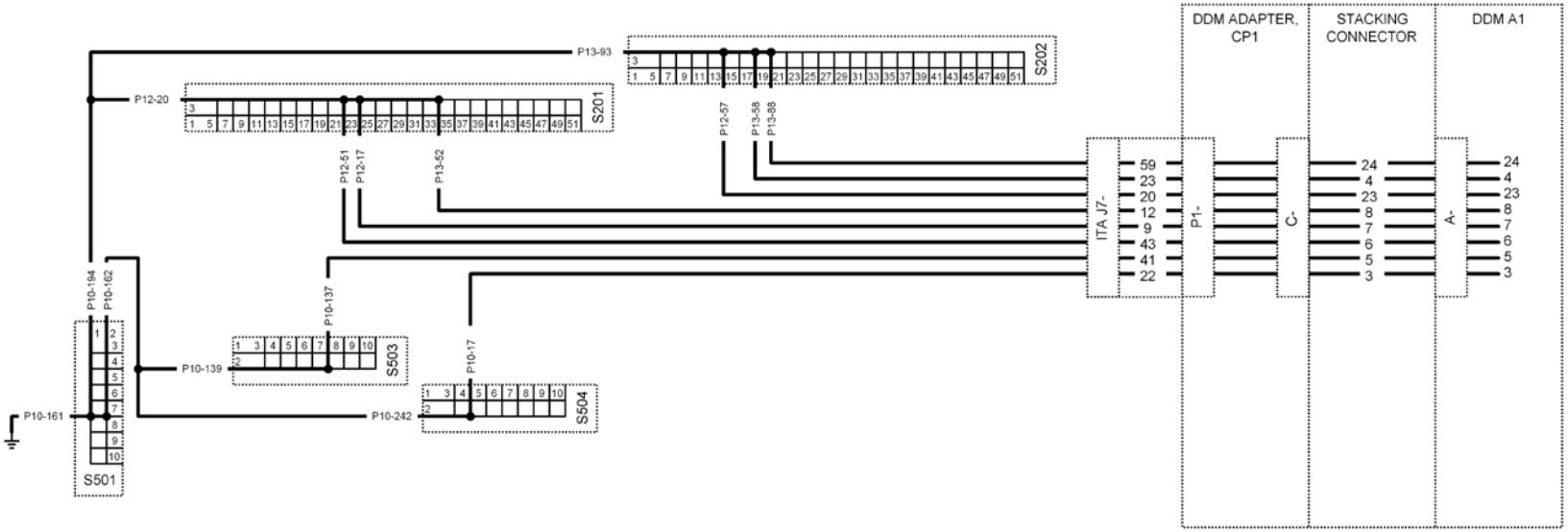
Step 103 Display Bar Graph OFF Test

Test step 103 verifies that bar graph displays DS1-DS4 and associated driving circuitry are functional by verifying that all segments of the bar graph displays are not lit. The operator must visually verify operation of the bar graph displays.

Operator Evaluation:



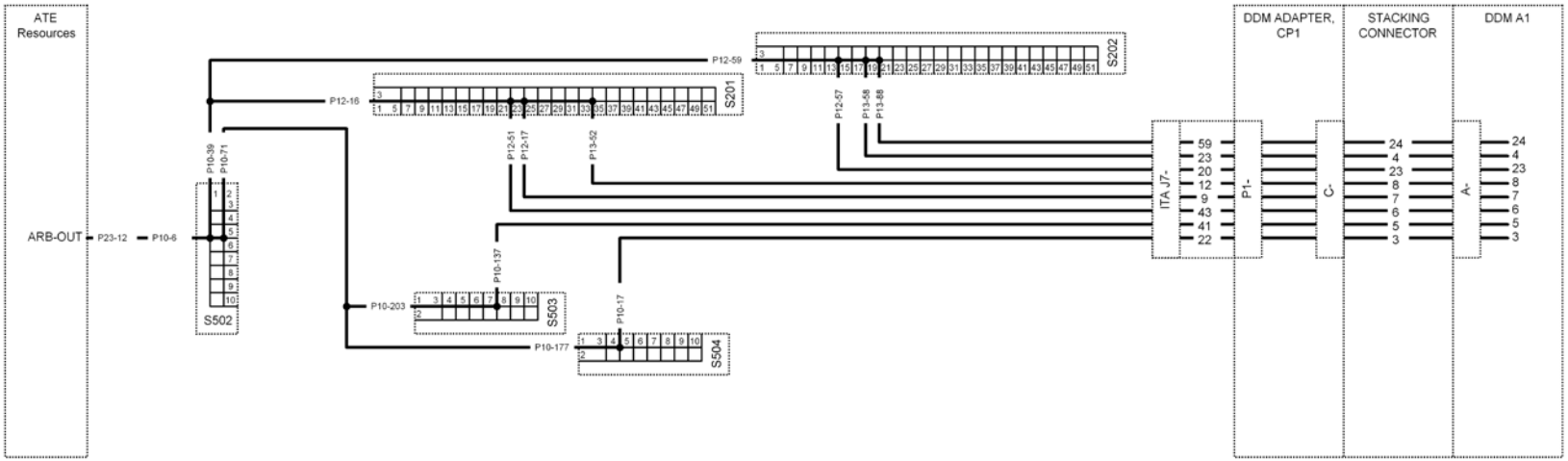
Connection Path as follows:


DDM ADAPTER, CP1
STACKING CONNECTOR
DDM A1
P13-93
P12-20
S202
S201
P12-57
P13-58
P13-88
P12-51
P12-17
P13-52
ITA J7-
59
23
20
12
9
43
41
22
P1-
C-
A-
24
4
23
8
7
6
5
3
P10-194
P10-162
P10-137
P10-17
P10-139
P10-161
P10-242
S503
S504
S501

Step 104 Display Bar Graph ON at 50% Test

Test step 104 verifies that bar graph displays DS1-DS4 and associated driving circuitry are able to display a 50% indication correctly by verifying that 50% of the segments of the bar graph light while a 50% input signal of 1.25 V is applied to all bar graph inputs. The operator must visually verify operation of the bar graph displays.

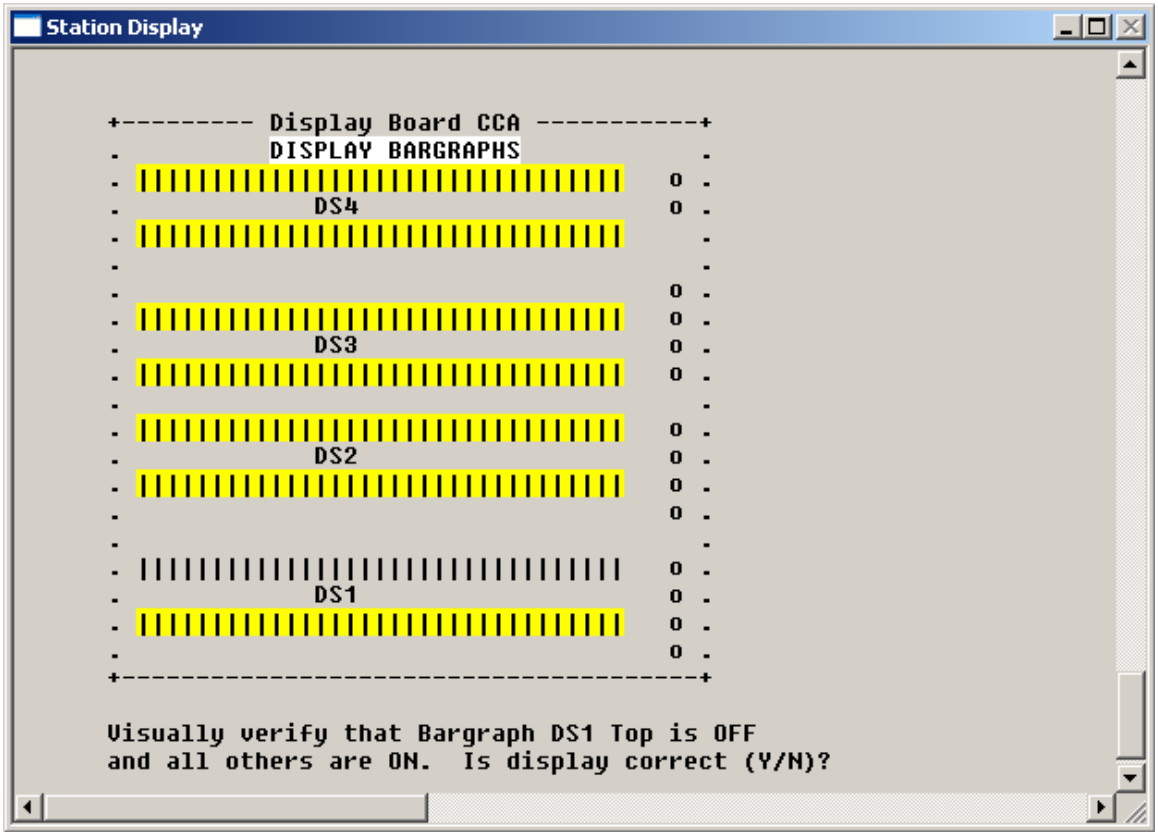
Connection Path as follows:


ATE Resources
ARB-OUT
P23-12
P10-6
P10-39
P10-71
S502
P12-59
P12-16
S201
S202
P12-51
P12-17
P13-52
P10-137
P10-203
S503
P10-177
P10-17
S504
P12-57
P13-58
P13-88
ITA J7-
59
23
20
12
9
43
41
22
DDM ADAPTER, CP1
P1-
C-
STACKING CONNECTOR
24
4
23
8
7
6
5
3
DDM A1
A-
24
4
23
8
7
6
5
3

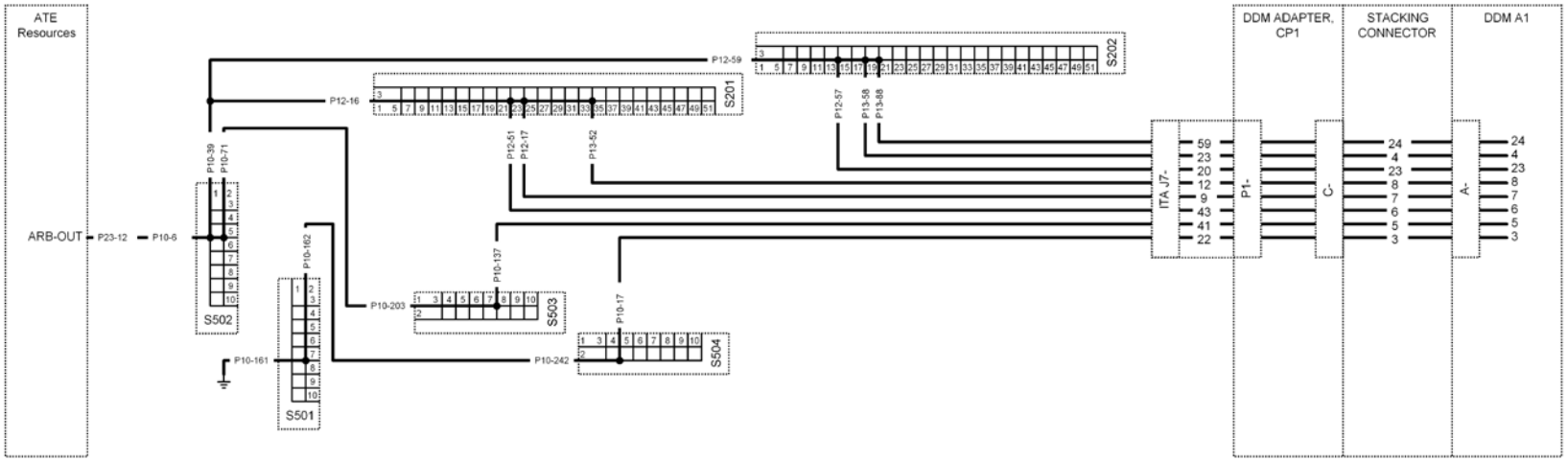
Step 105 CR7 Short Test

Test step 105 verifies that the two bar graphs of display DS1 and associated driving circuitry are independently controllable by verifying that single bar graph DS1 can indicate 0% while all other bar graphs indicate 100%. The operator must visually verify operation of the bar graph displays.

Operator Evaluation:



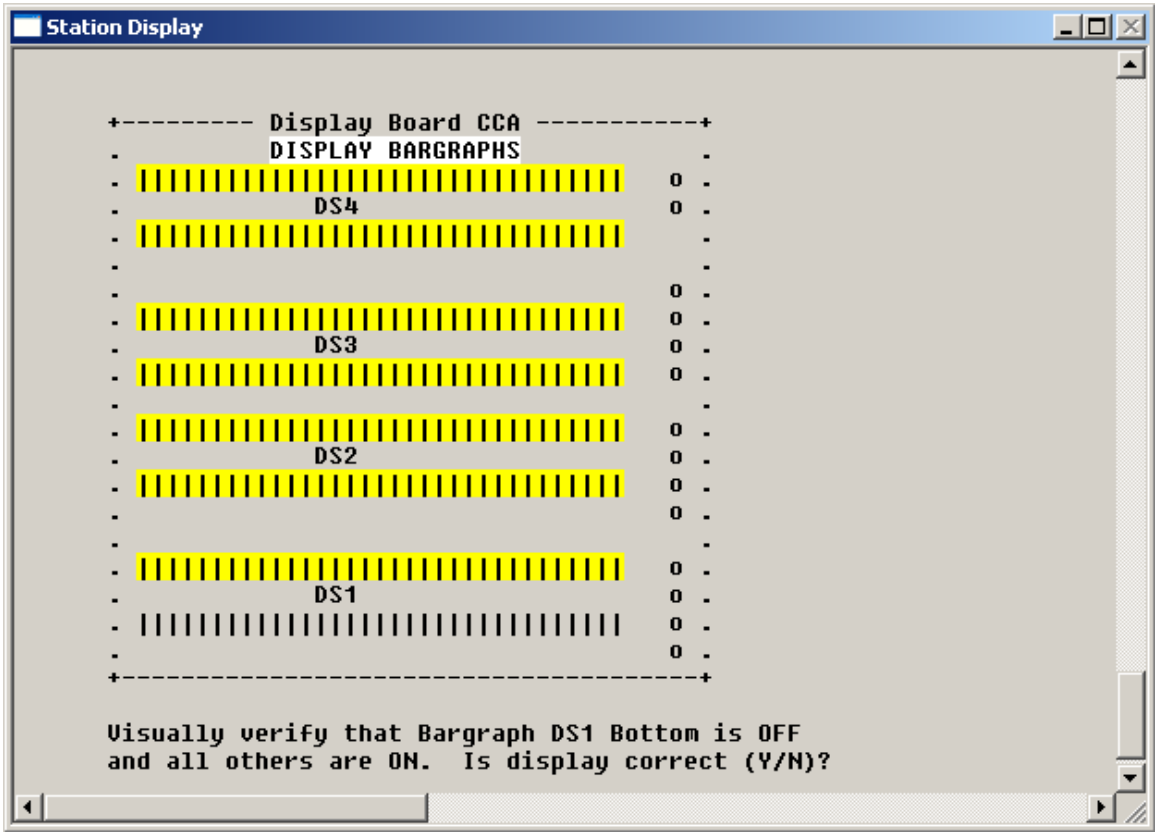
Connection Path as follows:


ATE Resources
ARB-OUT
P23-12
P10-6
P10-39
P10-71
S502
P10-162
S501
P10-161
P10-203
S603
P10-137
P10-17
S504
P10-242
P12-59
S202
P12-16
S201
P12-57
P13-58
P13-88
P12-51
P12-17
P13-52
ITA J7-
59
23
20
12
9
43
41
22
DDM ADAPTER, CP1
P1-
C-
STACKING CONNECTOR
24
4
23
8
7
6
5
3
DDM A1
A-
24
4
23
8
7
6
5
3

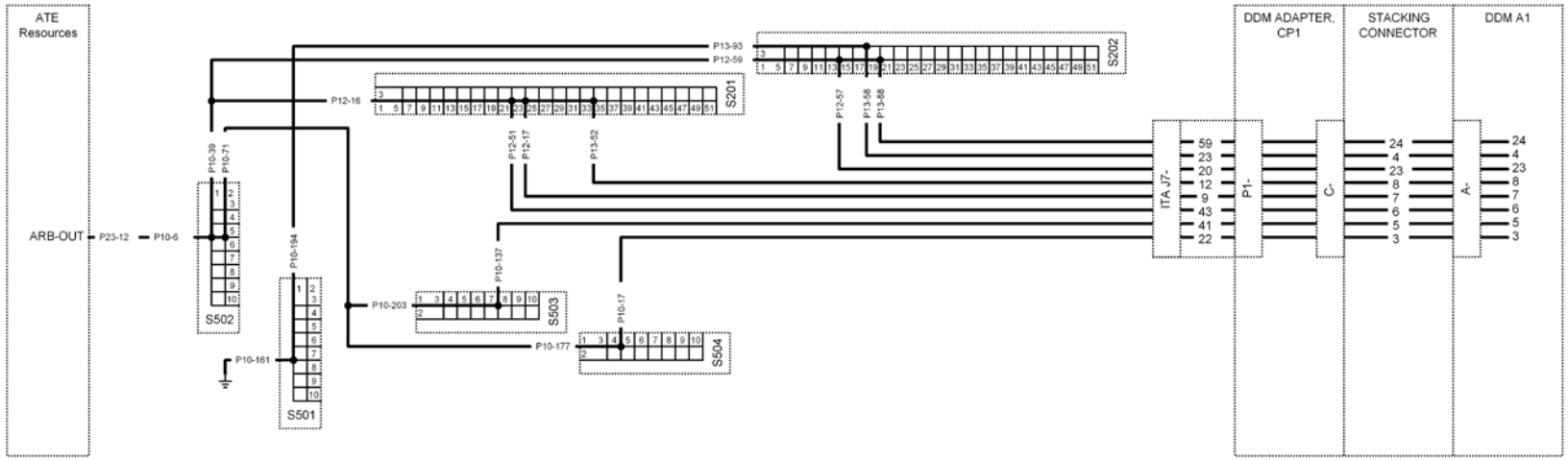
Step 106 CR8 Short Test

Test step 106 verifies that the two bar graphs of display DS1 and associated driving circuitry are independently controllable by verifying that single bar graph DS1 can indicate 0% while all other bar graphs indicate 100%. The operator must visually verify operation of the bar graph displays.

Operator Evaluation:



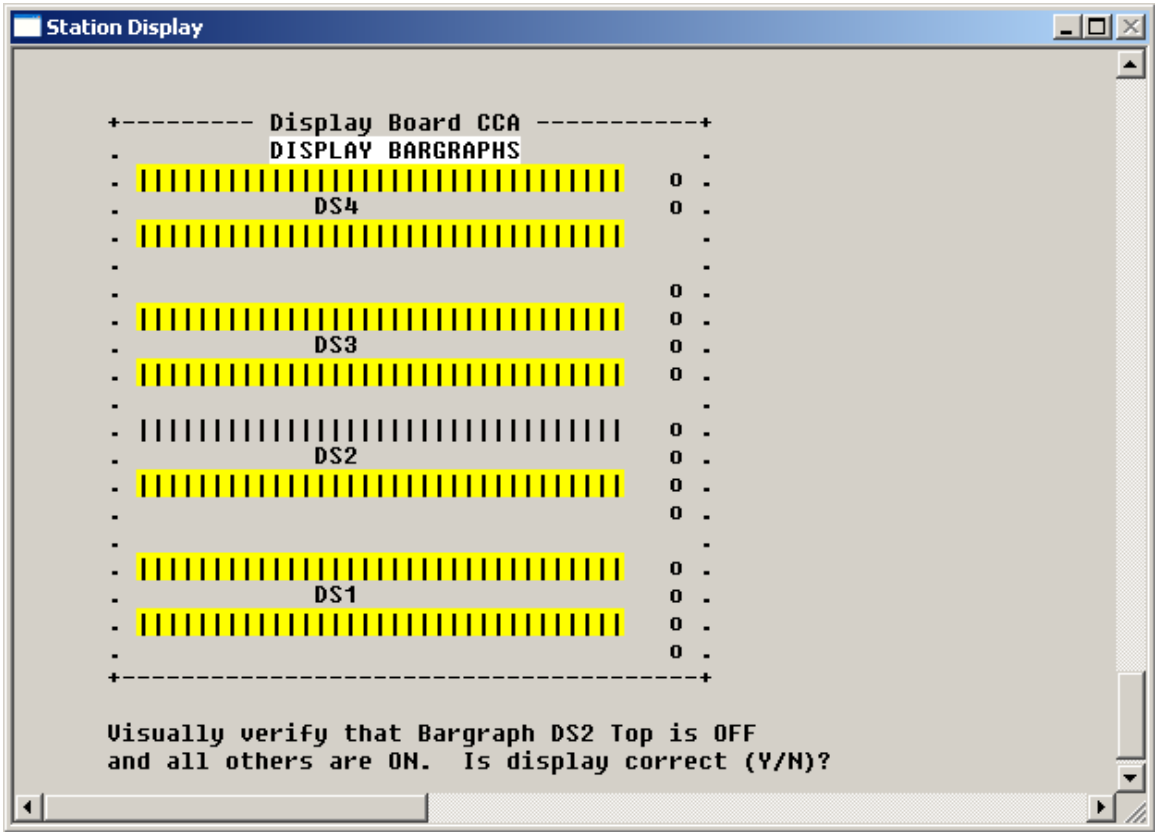
Connection Path as follows:


ATE Resources
ARB-OUT
P23-12
P10-6
P10-39
P10-71
S502
P10-194
S501
P10-161
P10-203
S503
P10-137
P10-177
S504
P10-17
P13-93
P12-59
S202
P12-16
S201
P12-51
P12-17
P13-52
P12-57
P13-58
P13-88
ITA J7-
59
23
20
12
9
43
41
22
P1-
C-
A-
DDM ADAPTER, CP1
STACKING CONNECTOR
DDM A1
24
4
23
8
7
6
5
3

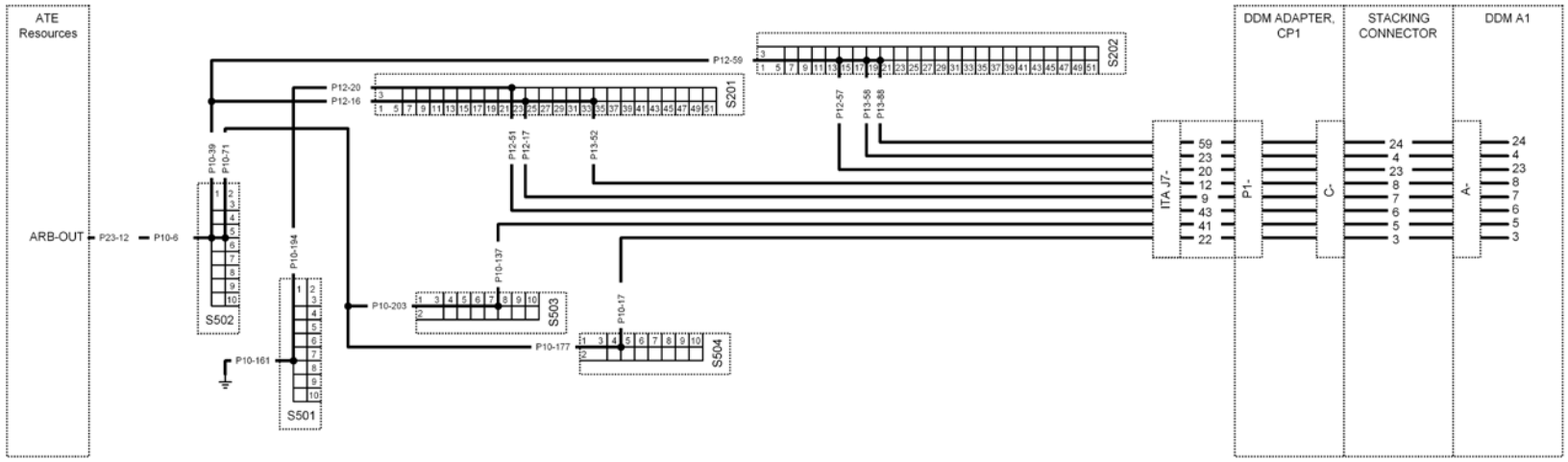
Step 107 CR6 Short Test

Test step 107 verifies that the two bar graphs of display DS2 and associated driving circuitry are independently controllable by verifying that single bar graph DS2 can indicate 0% while all other bar graphs indicate 100%. The operator must visually verify operation of the bar graph displays.

Operator Evaluation:



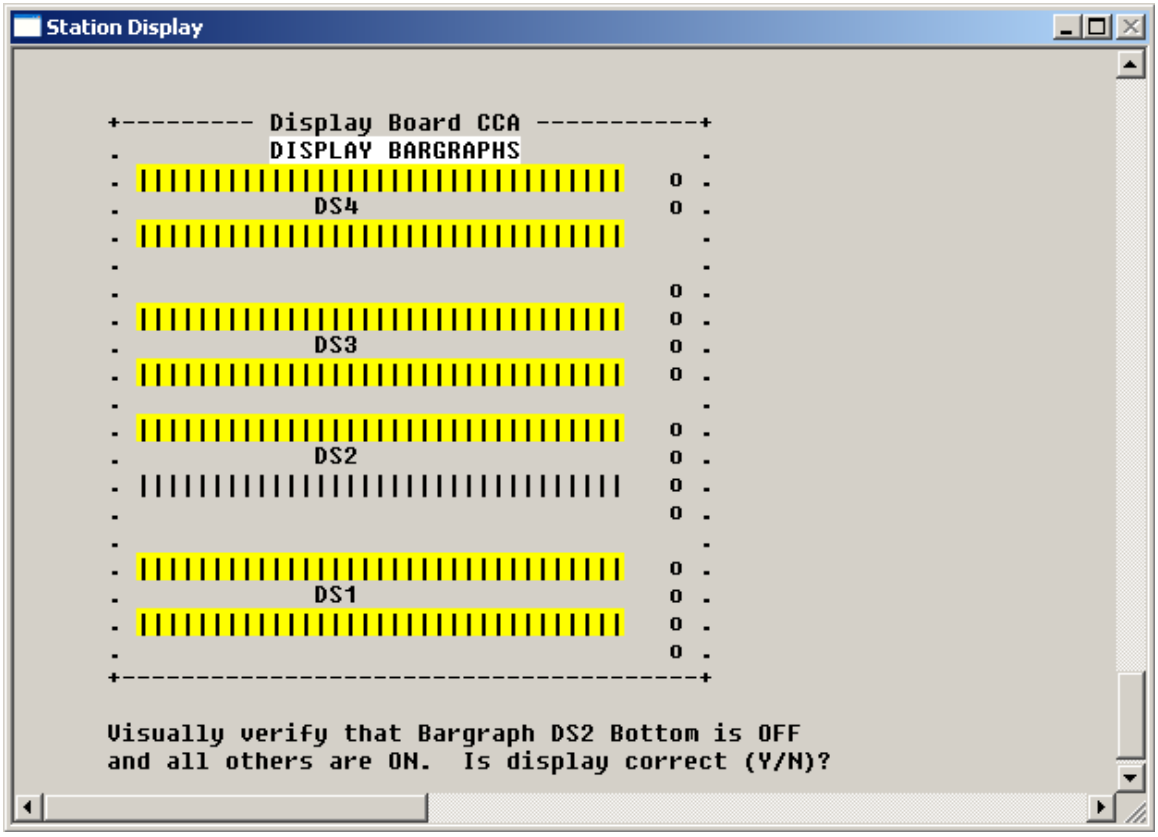
Connection Path as follows:


ATE Resources
ARB-OUT
P23-12
P10-6
P10-39
P10-71
S502
P10-194
S501
P10-161
P10-203
S503
P10-137
P10-177
S504
P10-17
P12-59
S202
P12-20
P12-16
S201
P12-51
P12-17
P13-52
P12-57
P13-58
P13-88
ITA J7-
P1-
C-
A-
DDM ADAPTER, CP1
STACKING CONNECTOR
DDM A1

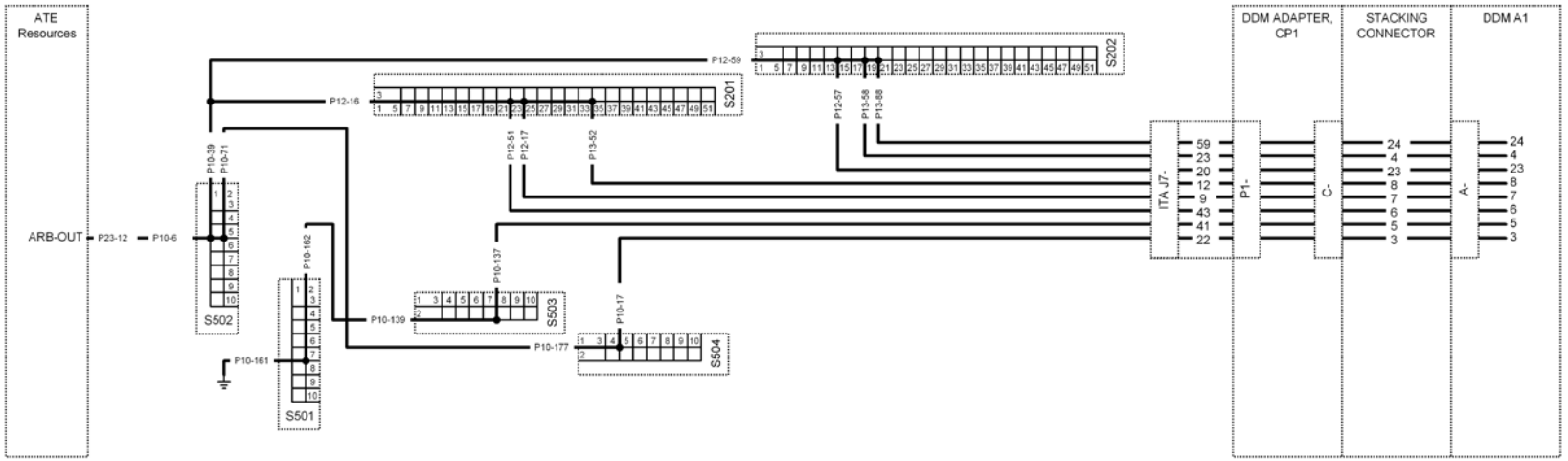
Step 108 CR5 Short Test

Test step 108 verifies that the two bar graphs of display DS2 and associated driving circuitry are independently controllable by verifying that single bar graph DS2 can indicate 0% while all other bar graphs indicate 100%. The operator must visually verify operation of the bar graph displays.

Operator Evaluation:



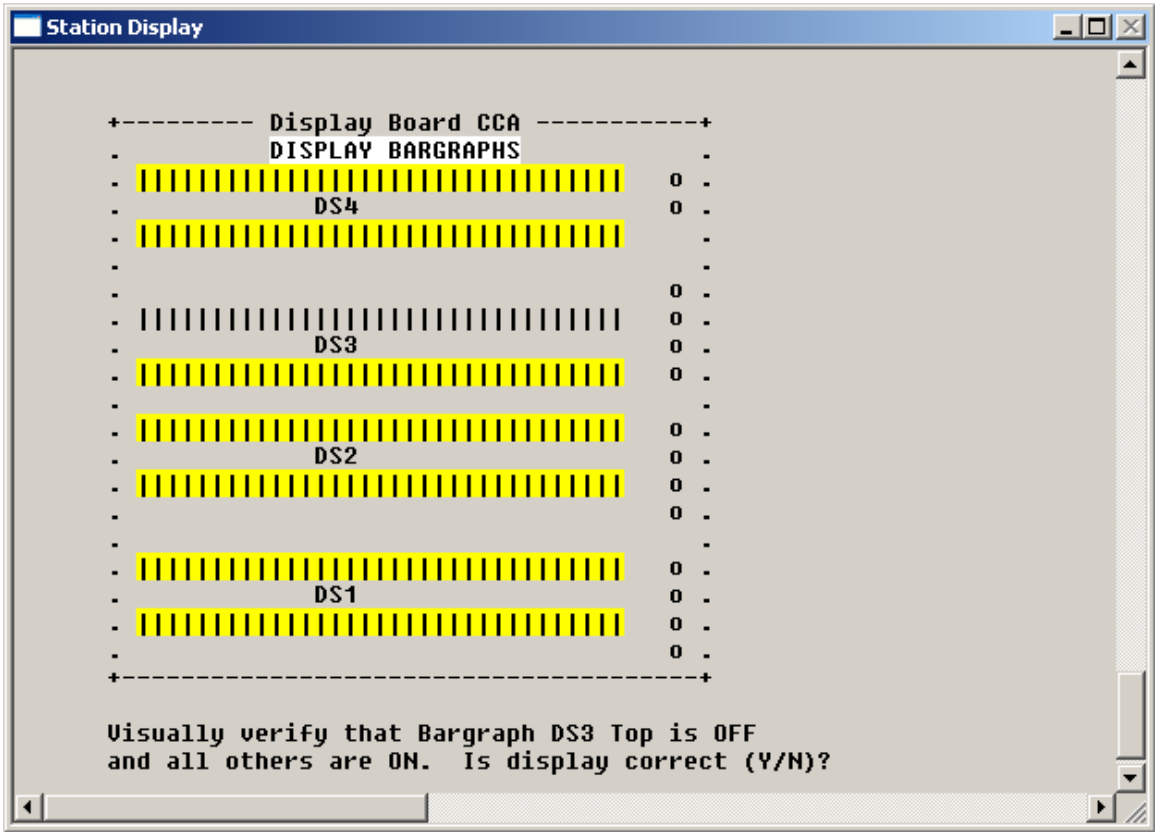
Connection Path as follows:


ATE Resources
ARB-OUT
P23-12
P10-6
P10-39
P10-71
P10-162
P10-161
P10-139
P10-137
P10-177
P10-17
P12-59
P12-16
P12-57
P13-58
P13-88
P12-51
P12-17
P13-52
S201
S202
S501
S502
S503
S504
ITA J7-
P1-
C-
A-
DDM ADAPTER, CP1
STACKING CONNECTOR
DDM A1

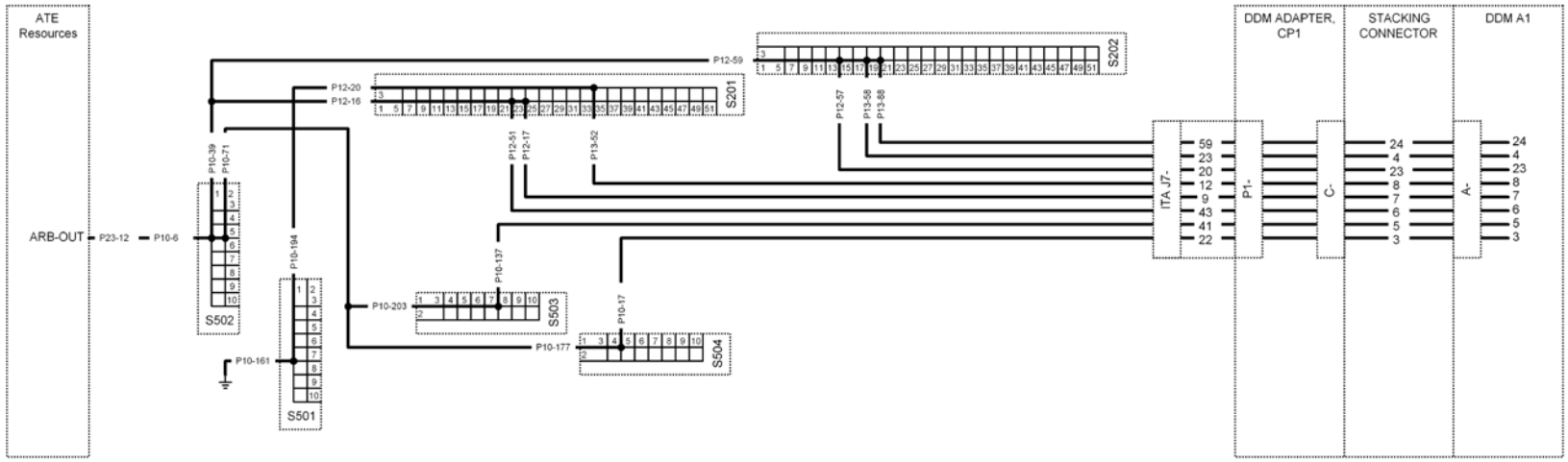
Step 109 CR4 Short Test

Test step 109 verifies that the two bar graphs of display DS3 and associated driving circuitry are independently controllable by verifying that single bar graph DS3 can indicate 0% while all other bar graphs indicate 100%. The operator must visually verify operation of the bar graph displays.

Operator Evaluation:



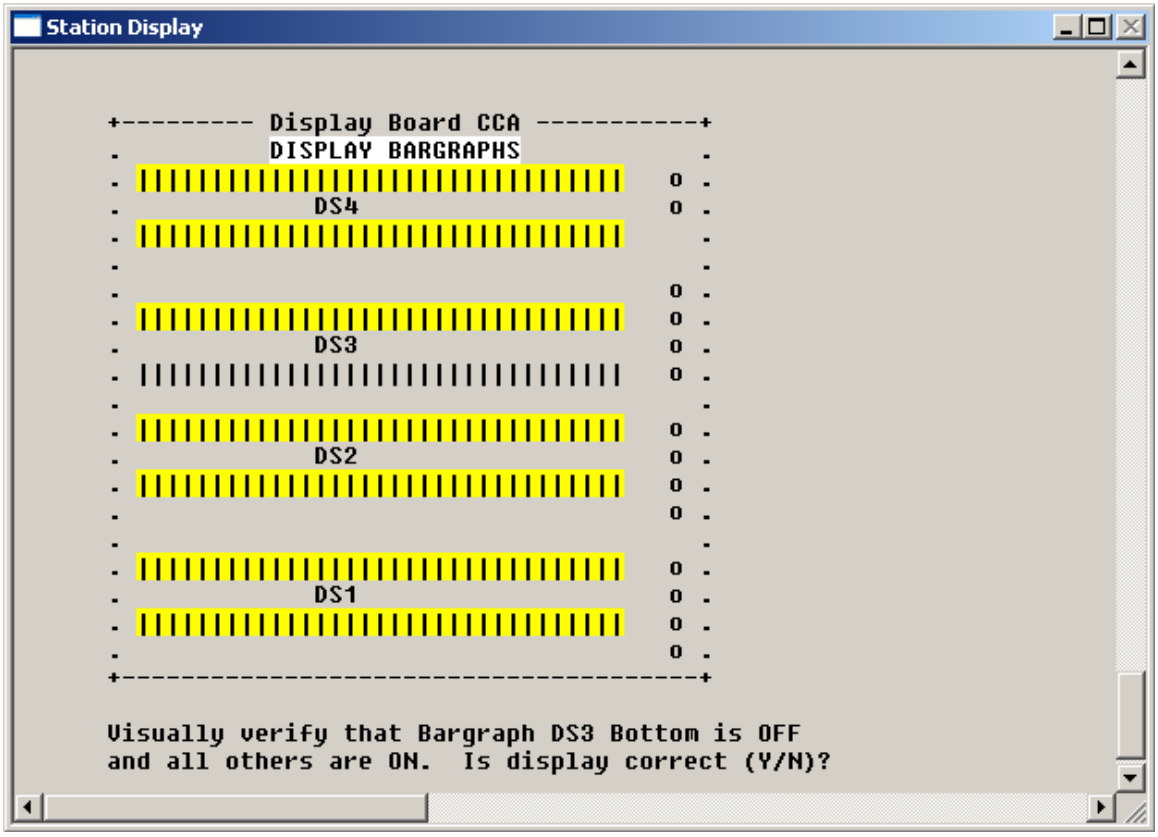
Connection Path as follows:


ATE Resources
ARB-OUT
P23-12
P10-6
P10-39
P10-71
S502
P10-194
S501
P10-161
P10-203
S503
P10-137
P10-177
S504
P10-17
P12-59
S202
P12-20
P12-16
S201
P12-51
P12-17
P13-52
P12-57
P13-58
P13-88
ITA J7-
59
23
20
12
9
43
41
22
P1-
C-
A-
DDM ADAPTER, CP1
STACKING CONNECTOR
DDM A1
24
4
23
8
7
6
5
3

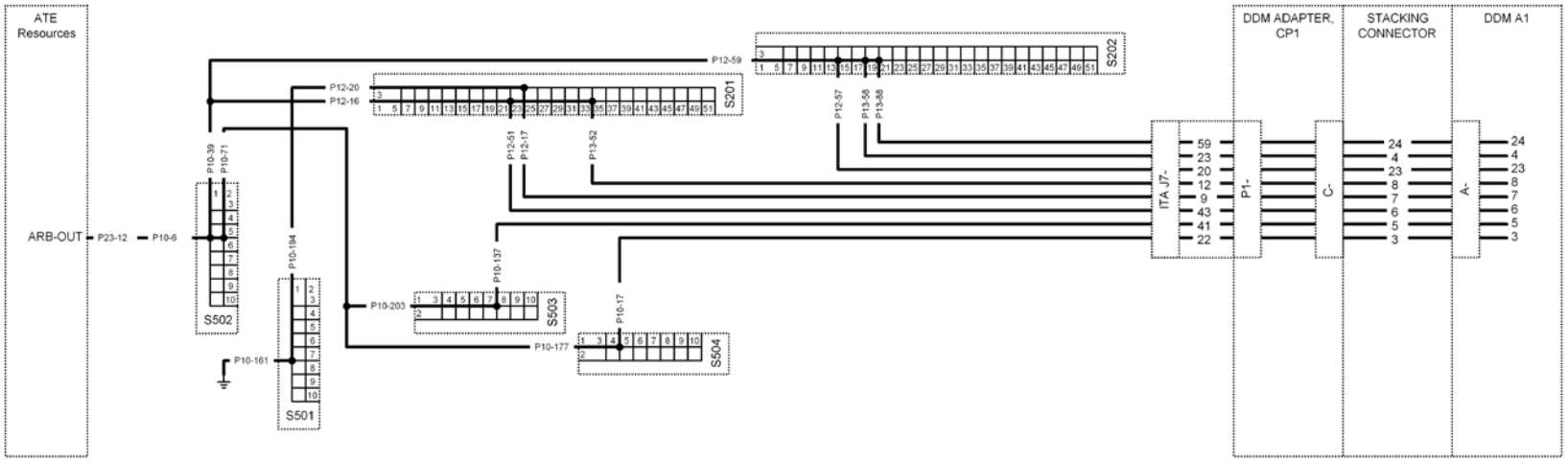
Step 110 CR3 Short Test

Test step 110 verifies that the two bar graphs of display DS3 and associated driving circuitry are independently controllable by verifying that single bar graph DS3 can indicate 0% while all other bar graphs indicate 100%. The operator must visually verify operation of the bar graph displays.

Operator Evaluation:



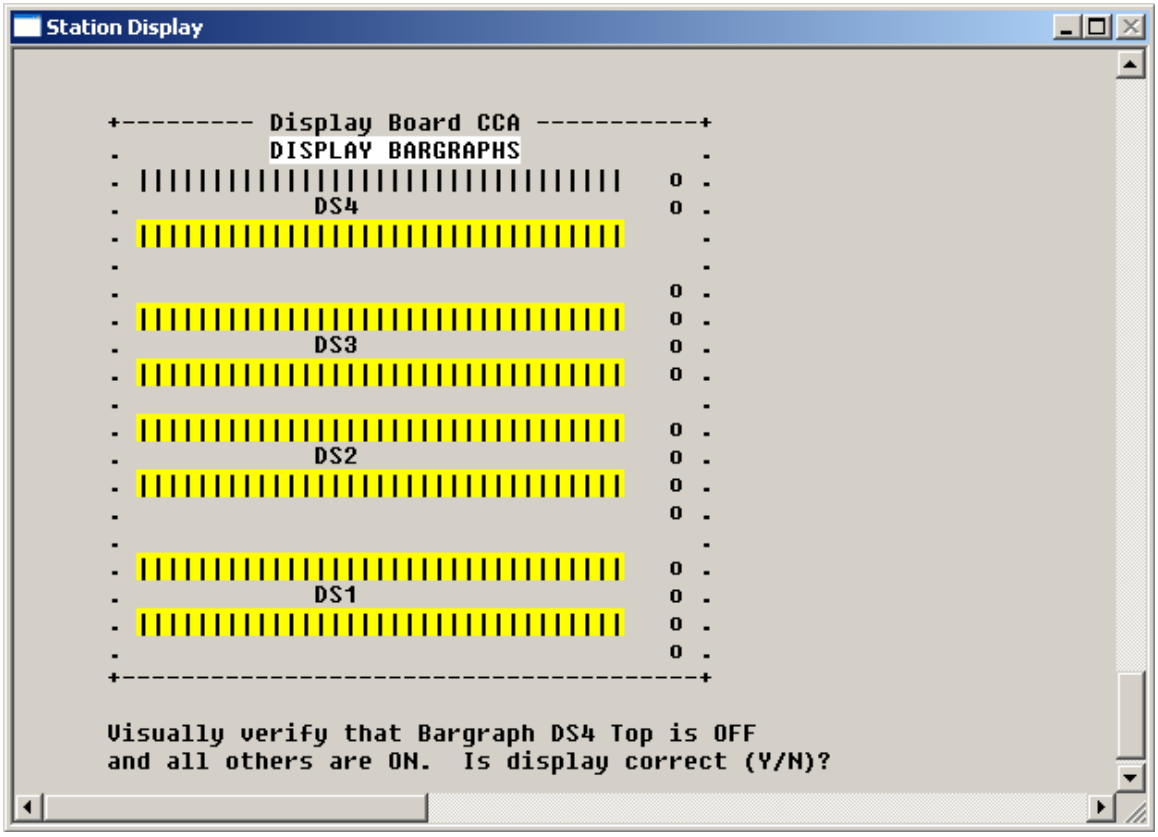
Connection Path as follows:


ATE Resources
ARB-OUT
P23-12
P10-6
P10-39
P10-71
S502
P10-194
S501
P10-161
P10-203
S503
P10-137
P10-177
S504
P10-17
P12-59
P12-20
P12-16
S202
S201
P12-57
P13-58
P13-88
P12-51
P12-17
P13-52
ITA J7-
59
23
20
12
9
43
41
22
DDM ADAPTER, CP1
P1-
C-
STACKING CONNECTOR
24
4
23
8
7
6
5
3
DDM A1
A-
24
4
23
8
7
6
5
3

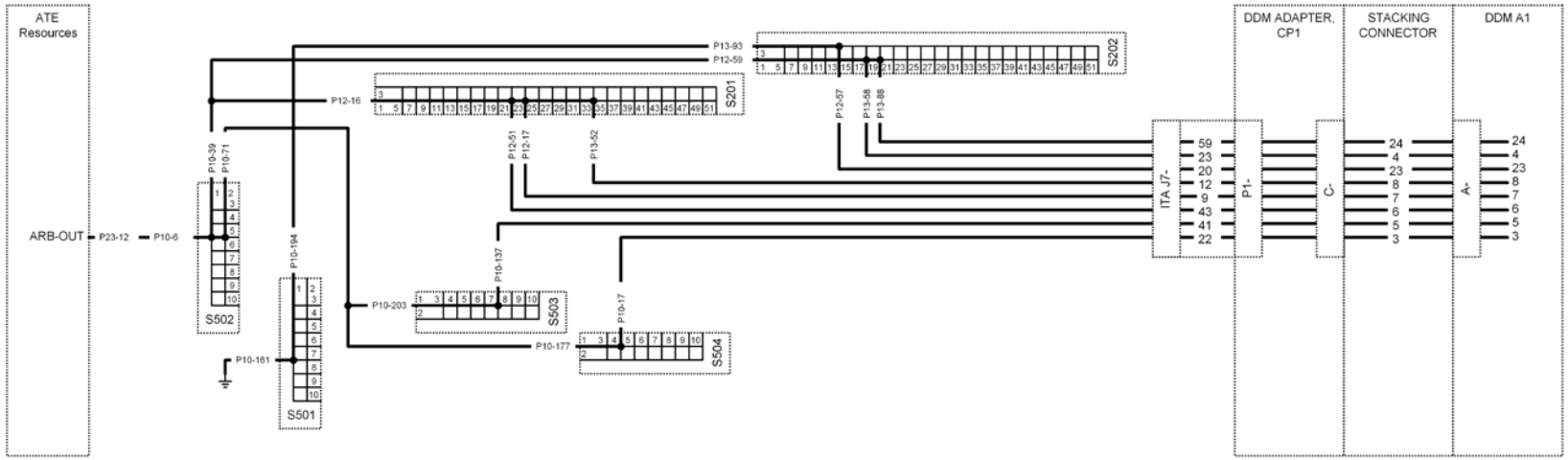
Step 111 CR2 Short Test

Test step 111 verifies that the two bar graphs of display DS4 and associated driving circuitry are independently controllable by verifying that single bar graph DS4 can indicate 0% while all other bar graphs indicate 100%. The operator must visually verify operation of the bar graph displays.

Operator Evaluation:



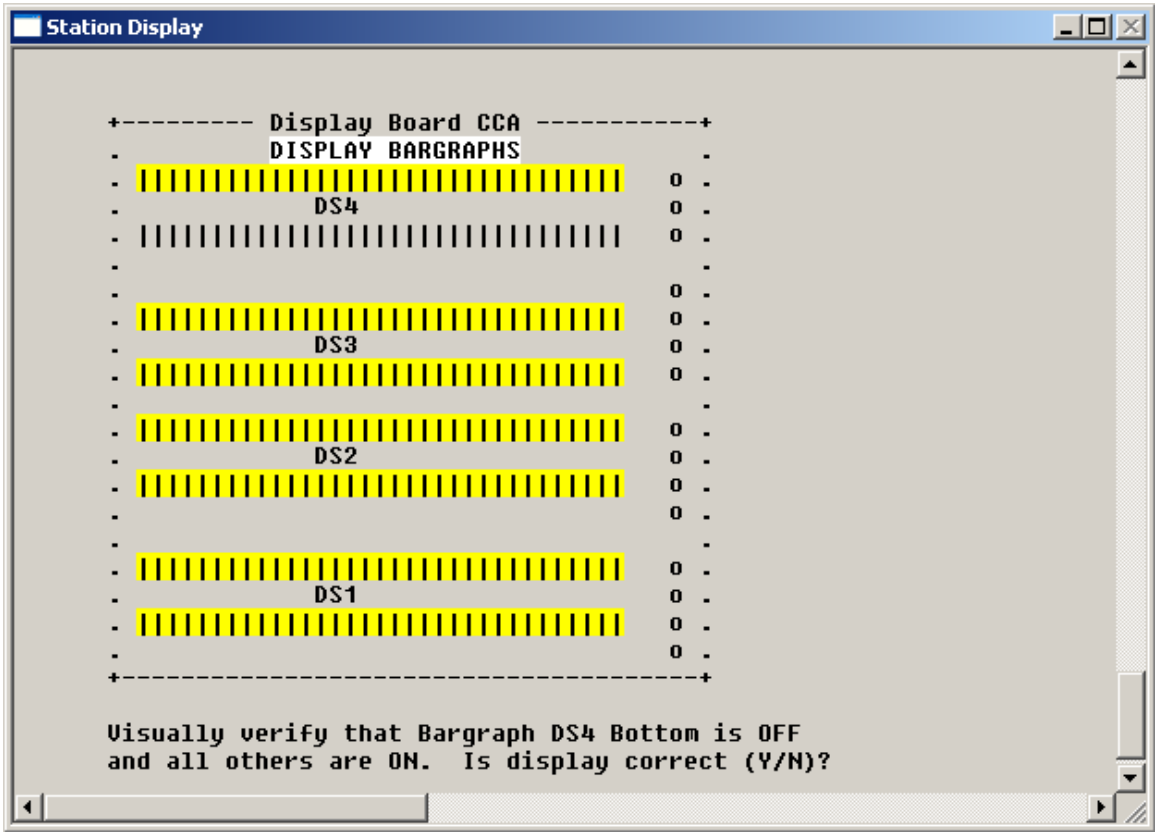
Connection Path as follows:


ATE Resources
ARB-OUT
P23-12
P10-6
P10-39
P10-71
S502
P10-194
S501
P10-161
P12-16
P13-93
P12-59
S201
S202
P10-203
S503
P10-177
P10-17
S504
P12-51
P12-17
P13-52
P10-137
P12-57
P13-58
P13-88
ITA J7-
59
23
20
12
9
43
41
22
DDM ADAPTER, CP1
P1-
C-
STACKING CONNECTOR
A-
DDM A1
24
4
23
8
7
6
5
3

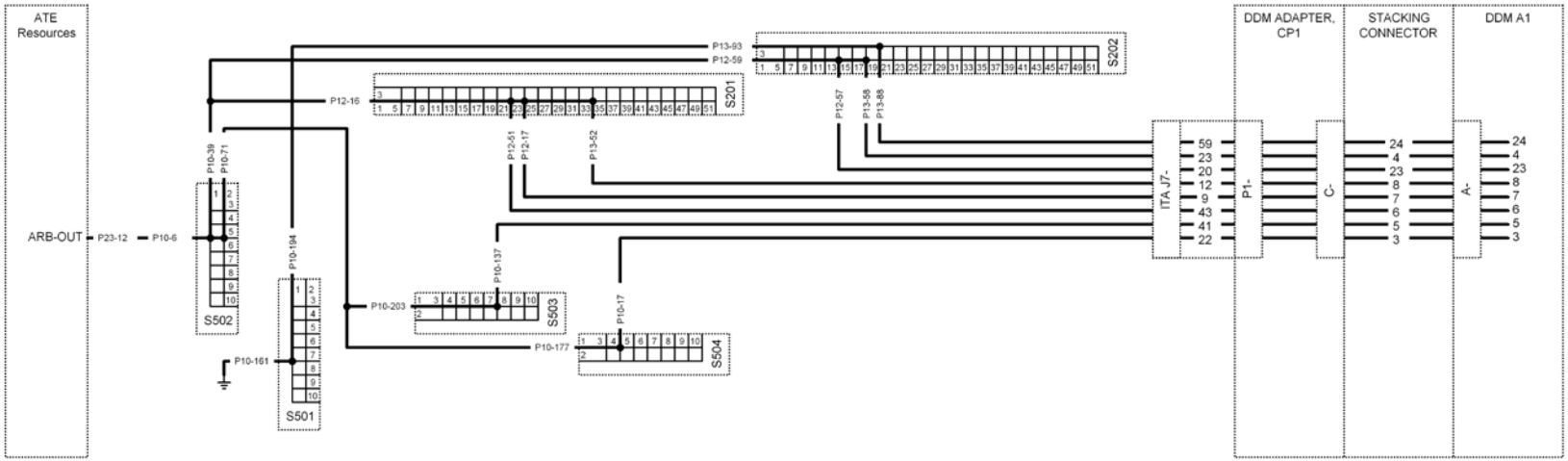
Step 112 CR1 Short Test

Test step 112 verifies that the two bar graphs of display DS4 and associated driving circuitry are independently controllable by verifying that single bar graph DS4 can indicate 0% while all other bar graphs indicate 100%. The operator must visually verify operation of the bar graph displays.

Operator Evaluation:



Connection Path as follows:


ATE Resources
ARB-OUT
P23-12
P10-6
P10-39
P10-71
S502
P10-194
S501
P10-161
P10-203
S503
P10-177
S504
P10-137
P10-17
P12-16
P13-93
P12-59
S201
S202
P12-61
P12-17
P13-52
P12-57
P13-58
P13-88
ITA J7-
59
23
20
12
9
43
41
22
DDM ADAPTER, CP1
P1-
STACKING CONNECTOR
C-
DDM A1
A-
24
4
23
8
7
6
5
3

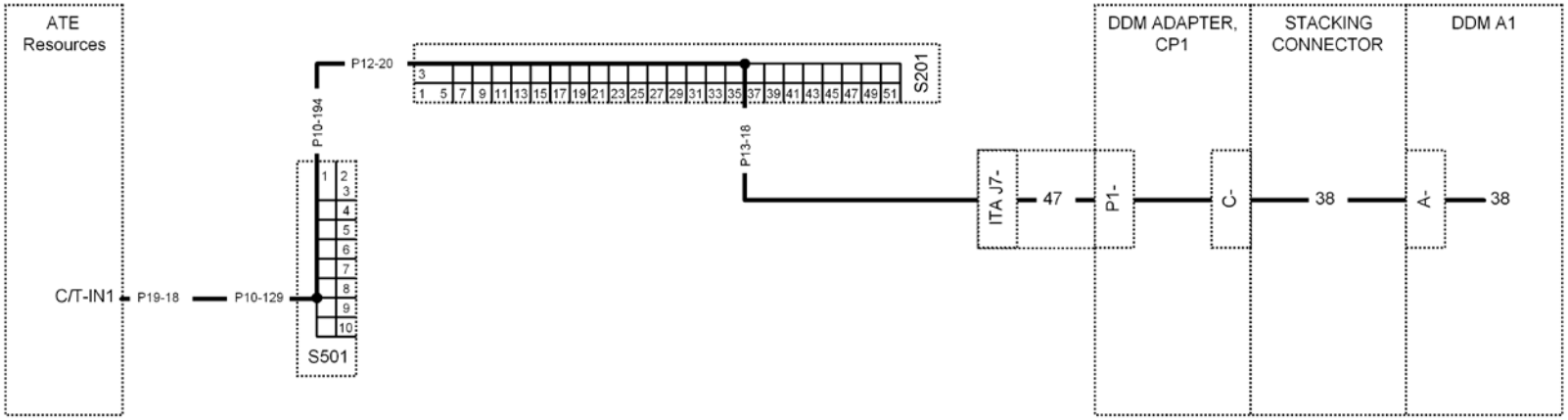
MODULE 2 DIMING CIRCUIT TESTS

Module 2 tests the diming circuitry of the display board to ensure everything is functioning correctly.

Step 201 RESET Out Frequency (C-38) Test

Test step 201 verifies that the oscillator (U11, R32, R33, C5, and C6), frequency divider (U10), counter (U12) and PROM (U5) are functioning correctly by using the DSO to measure the waveform present as the bit 6 output of the PROM (U5-12) through C-38. The average frequency should be between 100 Hz and 200 Hz. The frequency measured will be saved for use in step 202.

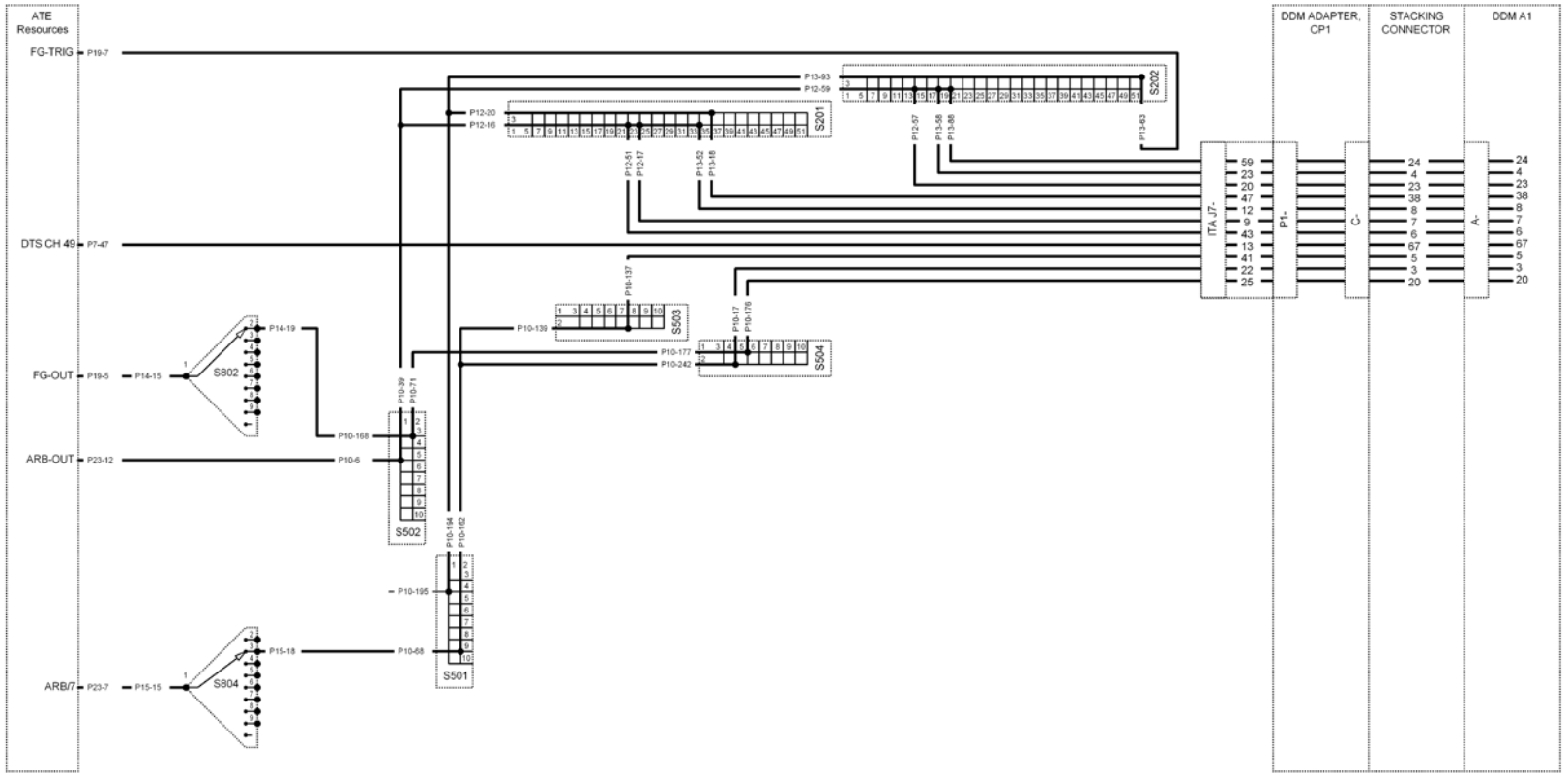
Connection Path as follows:


ATE
Resources
C/T-IN1
P19-18
P10-129
P10-194
P12-20
S501
S201
P13-18
ITA J7-
47
P1-
C-
38
A-
38
DDM ADAPTER,
CP1
STACKING
CONNECTOR
DDM A1

Step 202 Dimming Circuit Test

Test step 202 verifies that the bar graph display dimmer circuit is functioning correctly. The operator must manually verify the 50% brightness output of the bar graphs. This is accomplished by first providing a visual reference by lighting the bar graphs at 100% brightness. The operator is asked to note the brightness, and then the dimmer circuit is activated and the operator is asked to verify that the circuit has dimmed to approximately 50% of the initial brightness. If the bar graphs fail to light completely while the dimmer circuit is enabled, an in-line alignment procedure will be executed in which the operator will align R65 in an attempt to cause the bar graphs to light while the dimmer is enabled. If the in-line alignment is executed, the operator will be instructed to adjust R65 clockwise while the dimmer circuit is enabled to a point where the bar graph displays are "just on". From that point the operator will be asked to adjust R65 1 full turn in the clockwise direction. At this point the 50% brightness test is repeated. The operator is shown the 100% visual reference and then the dimmer circuit is enabled once again and the operator is asked to verify 50% brightness. The frequency used to drive the display to 50% is one half of the value measured in step 201.

Connection Path as follows:


ATE Resources
FG-TRIG
P19-7
DTS CH 49
P7-47
FG-OUT
P19-5
P14-15
S802
P14-19
ARB-OUT
P23-12
P10-6
P10-168
S502
P10-39
P10-71
ARB/7
P23-7
P15-15
S804
P15-18
P10-68
S501
P10-195
P10-194
P10-182
S201
P12-20
P12-16
S202
P13-93
P12-59
P13-63
P12-57
P13-58
P13-88
P12-51
P12-17
P13-52
P13-18
S503
P10-137
P10-139
S504
P10-17
P10-176
P10-177
P10-242
ITA J7-
P1-
C-
A-
DDM ADAPTER, CP1
STACKING CONNECTOR
DDM A1
59 23 20 47 12 9 43 13 41 22 25
24 4 23 38 8 7 6 67 5 3 20
24 4 23 38 8 7 6 67 5 3 20

FUNCTIONAL FLOW CHART (FFC)