English Language Test Description

Contract Number: N00244-09-C-0054

For

Unit Under Test

UUT Nomenclature: Intercommunication Set LRU
UUT Part Number: AN/MIQ-1(V)3
UUT Reference Designator: ICS LRU

From

Assault Amphibious Vehicle
AN/PSM-115

ATE (Automated Test Equipment) SYSTEM

AN/USM-657B(V)2 Third Echelon Test System (TETS)
AN/USM-717(V)2 Virtual Instrument Portable Equipment Repair / Tester (VIPER/T)

Developed by

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Prepared By	Signature	Date Prepared	Date Submitted
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Approved By	Signature	Date Received	Date Approved

ELTD REVISION SUMMARY

Revision Number	Date	Reason	Approved By – Date Approved
-	05/19/2010	ORIGINAL ISSUE	

1. Introduction

The Unit Under Test (UUT) for this English Language Test Description (ELTD) is the Intercommunication Set Line Replaceable Unit (LRU), Part Number AN/MIQ-1(V)3. The LRU resides in the Assault Amphibious Vehicle (AAV) Weapon System.

1.1. Scope

An ELTD is a detailed supplementary document consisting of textual test descriptions with graphical representation of signal interconnectivity and a functional flow chart.

1.2. Purpose

The purpose of this document is to provide English language test descriptions for the TP_AAV_ICS_LRU test program, to a level of detail used for maintenance purposes. The TP_AAV_ICS_LRU test program makes up part of the AN/PSM-115 Application Program Set (APS).

1.3. Content Arrangement

The document is laid out in the sequence the Test Program Set (TPS) would be executed when a 95 “Run All Mods” is entered in the main menu. A paragraph at the beginning of each module will describe the test description for that module. Each step will contain a description for that particular test followed by a graphical representation of the connections made from the receiver, through the Interface Test Adapter (ITA) and cable W6 to the Power Amplifier CCA. A Functional Flow Chart resides at the end of the document.

2. English Language Test Description (ELTD)

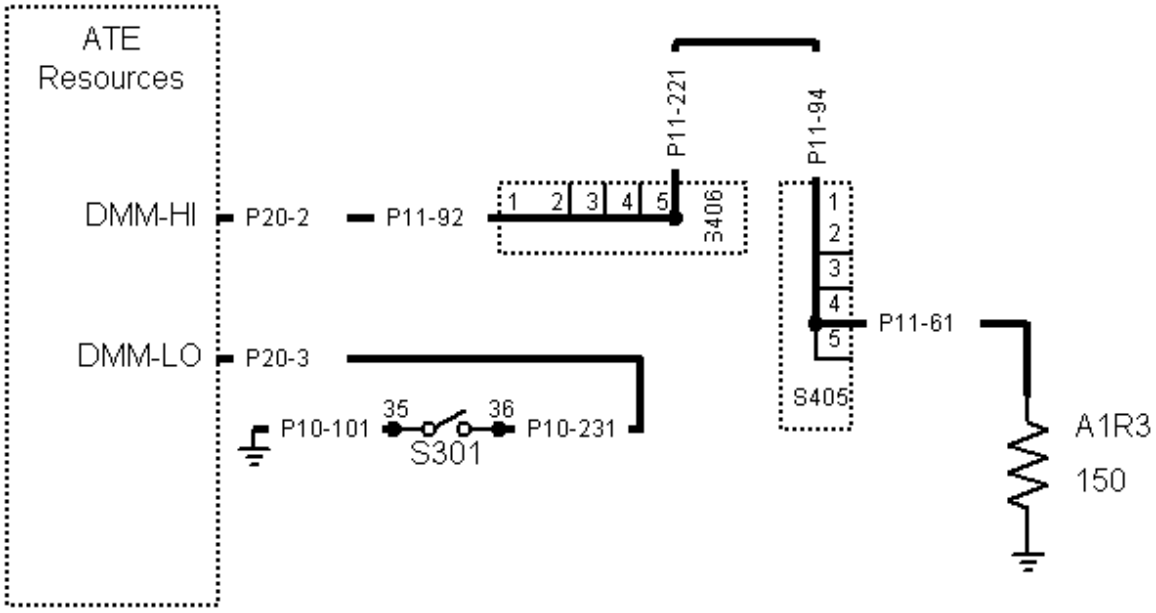
WEAPON SYSTEM: Assault Amphibious Vehicle (AAV)
UNIT UNDER TEST: AN/MIQ-1(V)3
TEST PROGRAM SET: TP_AAV_ICS_LRU

SAFE TO TURN ON TESTS

Step 1 ITA Identification

Test step 1 verifies the correct ITA is installed by using the DMM to measure the resistance of ITA A1R3. The resistance should be from 149 ohms to 155 ohms.

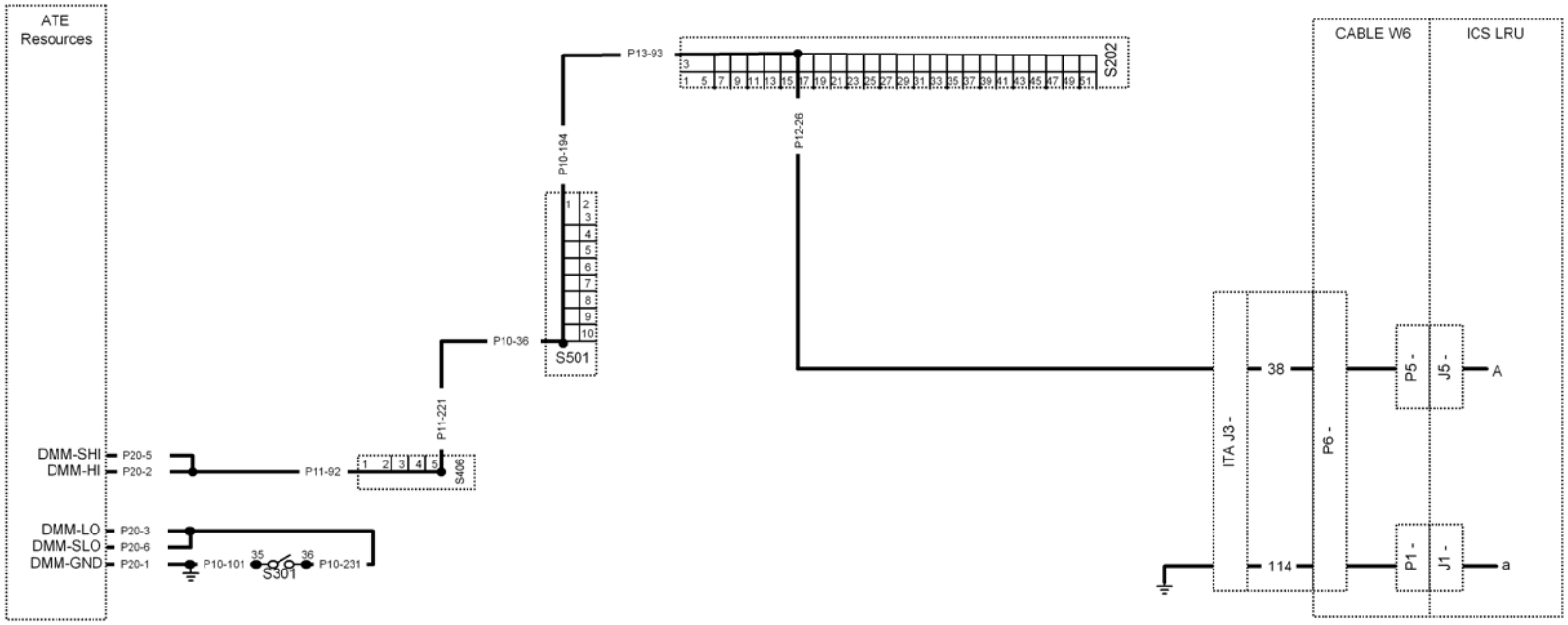
Connection Path as follows:



Step 2 UUT Identification

This step verifies the UUT connected is the Intercommunications Set LRU, P/N AN/MIQ-1(V)3. The DMM is used to verify less than 20 ohms resistance from J5-A to J1-a (GND).

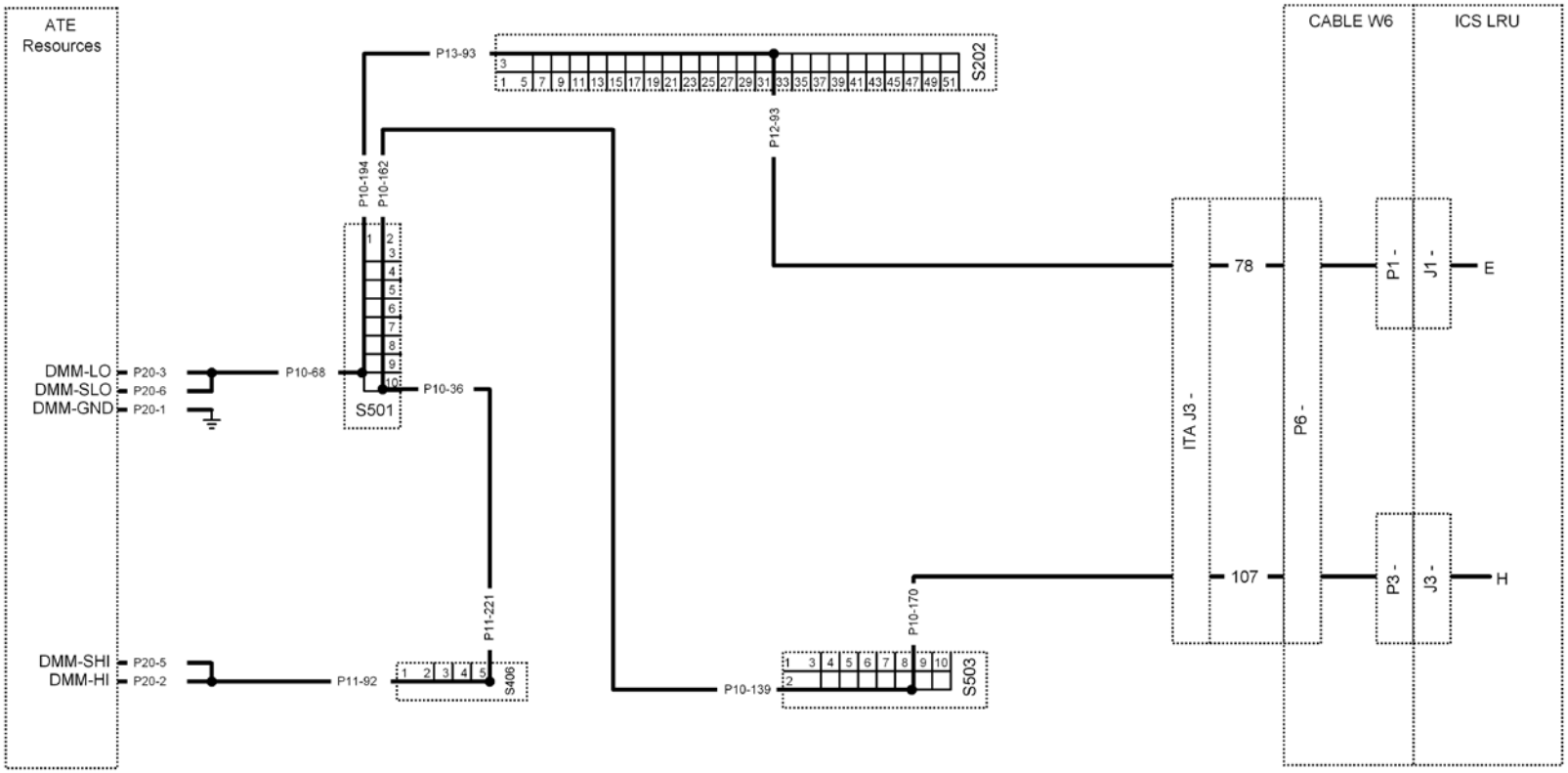
Connection Path as follows:


ATE
Resources
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P10-101
S301
P10-231
P11-92
S406
P11-221
P10-36
S501
P10-194
P13-93
S202
P12-26
CABLE W6
ICS LRU
ITA J3 -
38
114
P6 -
P5 -
J5 -
A
P1 -
J1 -
a

Step 3 UUT Version: (V)2 Identification

This step checks the presence of a CVSD 2 (A2) CCA by using the DMM to test for less than 100 ohms from J3-H to J1-E (A2, Pin 7 to GND). If the reading is greater than 100 ohms, then the UUT is an AN/MIQ-1(V)1 (no A2 CVSD card installed). The version number is used in Test Module 5 to run tests on the installed CVSD CCAs. Part number AN/MIQ-1(V)1 is no longer required to be supported by this test program. However, it has been left unchanged for simplicity and backwards compatibility in the re-host effort and will still correctly identify LRU part number AN/MIQ-1(V)3.

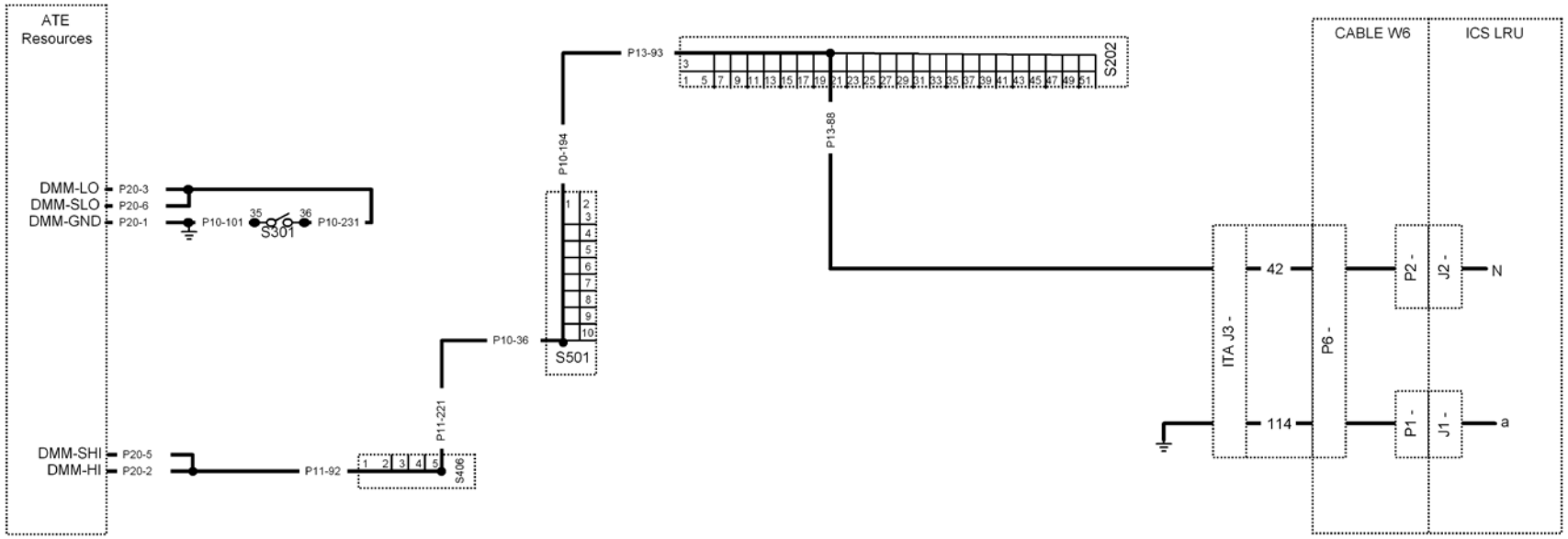
Connection Path as follows:


ATE Resources
DMM-LO
DMM-SLO
DMM-GND
DMM-SHI
DMM-HI
P20-3
P20-6
P20-1
P20-5
P20-2
P10-68
P10-36
P11-92
P11-221
P10-194
P10-162
P13-93
P12-93
P10-139
P10-170
S501
S406
S202
S503
CABLE W6
ICS LRU
ITA J3 -
P6 -
78
107
P1 -
J1 -
P3 -
J3 -
E
H

Step 4 UUT Version: (V)3 Identification

This step checks the presence of a CVSD 3 (A3) CCA by using the DMM to test for measure for continuity from J2-N to GND (A3, Pin 7 to GND). If the reading is less than 100 ohms, then the UUT is an AN/MIQ-1(V)3. If the reading is greater than 100 ohms, then the UUT is an AN/MIQ-1(V)2. The version number is used in Test Module 5 to run tests on the installed CVSD CCAs. Part number AN/MIQ-1(V)2 is no longer required to be supported by this test program. However, it has been left unchanged for simplicity and backwards compatibility in the re-host effort and will still correctly identify LRU part number AN/MIQ-1(V)3.

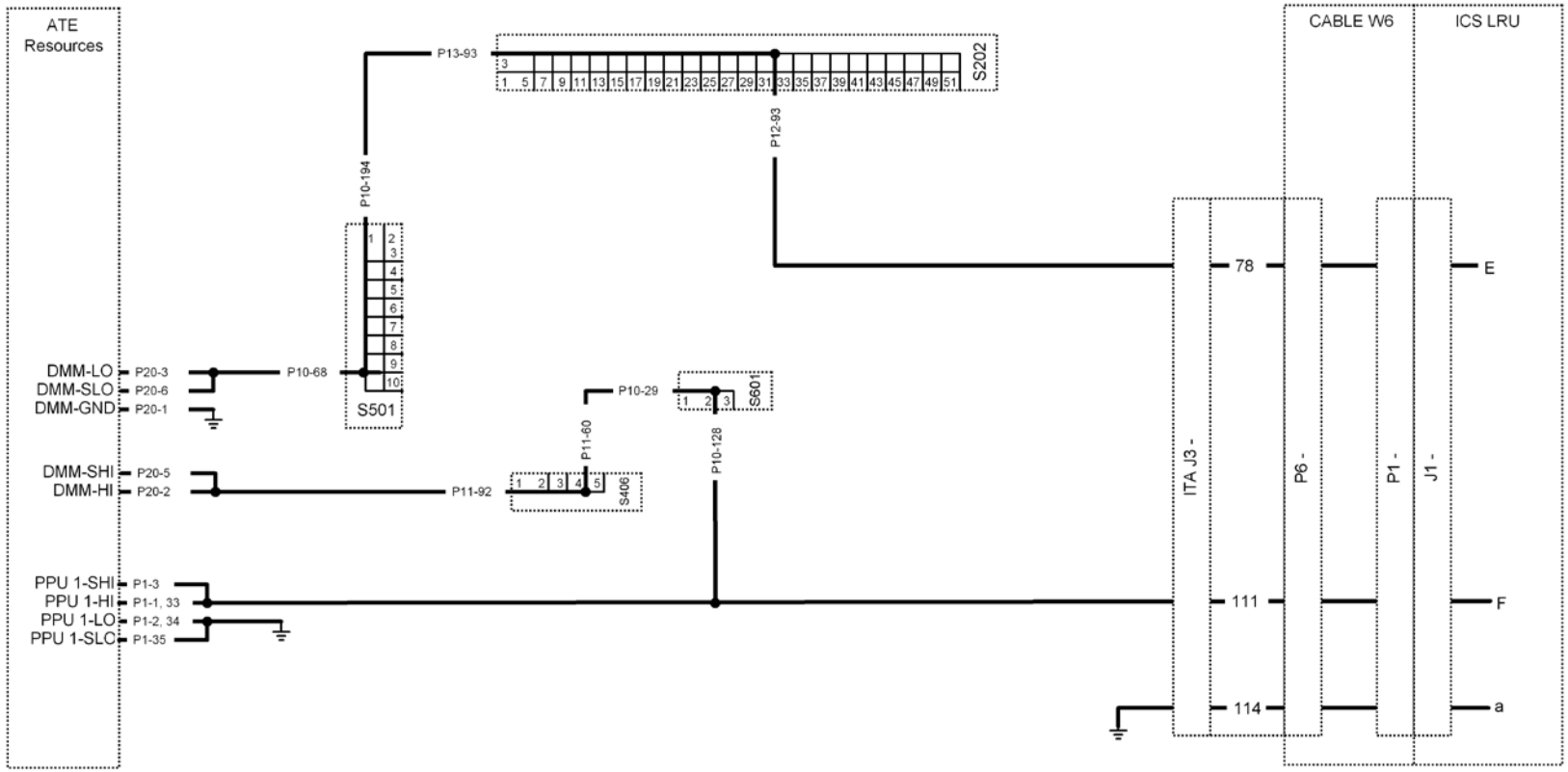
Connection Path as follows:


ATE
Resources
DMM-LO
DMM-SLO
DMM-GND
DMM-SHI
DMM-HI
P20-3
P20-6
P20-1
P20-5
P20-2
P10-101
S301
P10-231
P10-194
P13-93
S202
P13-88
P10-36
S501
P11-221
P11-92
S406
CABLE W6
ICS LRU
ITA J3 -
42
114
P6 -
P2 -
J2 -
N
P1 -
J1 -
a

Step 5 +15 VDC Input Power STTO Test

This step verifies the UUT +15V power input circuitry is free of shorts that would constitute an Unsafe-to-Turn-On condition. DCPS (PPU) #1 is applied at J1-F/J1-E at a low voltage of 2V at 0.2 amps. The DMM is used to verify that the PPU did not sense an over-current condition by verifying nominally 2VDC at J1-F/J1-E (GND).

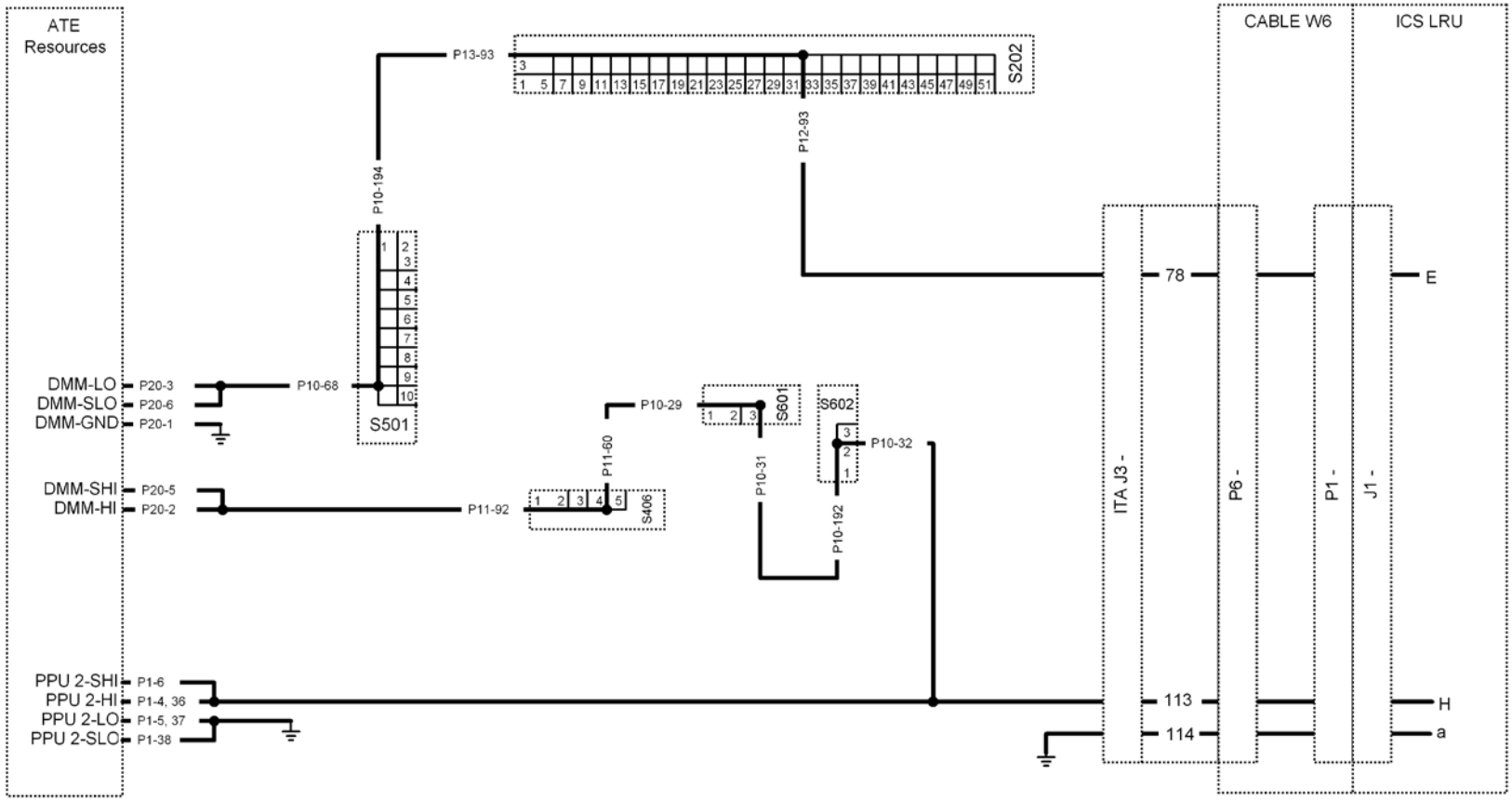
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P13-93
S202
P12-93
P10-194
S501
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-68
P10-29
S601
P11-60
P10-128
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
S406
PPU 1-SHI
PPU 1-HI
PPU 1-LO
PPU 1-SLC
P1-3
P1-1, 33
P1-2, 34
P1-35
ITA J3 -
P6 -
P1 -
J1 -
78
111
114
E
F
a

Step 6 +24 VDC Input Power STTO Test

This step verifies the UUT +24V power input circuitry is free of shorts that would constitute an Unsafe-to-Turn-On condition. DCPS (PPU) #2 is applied at J1-H/J1-E at a low voltage of 2V at 0.2 amps. The DMM is used to verify that the PPU did not sense an over-current condition by verifying nominally 2VDC at J1-H/J1-E (GND).

Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P13-93
S202
P12-93
P10-194
S501
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-68
P10-29
S601
S602
P10-32
P10-31
P10-192
P11-60
S406
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
ITA J3 -
P6 -
P1 -
J1 -
78
E
113
H
114
a
PPU 2-SHI
PPU 2-HI
PPU 2-LO
PPU 2-SLO
P1-6
P1-4, 36
P1-5, 37
P1-38

UUT POWER UP

The UUT requires the following input power which remains applied for the duration of the test program:

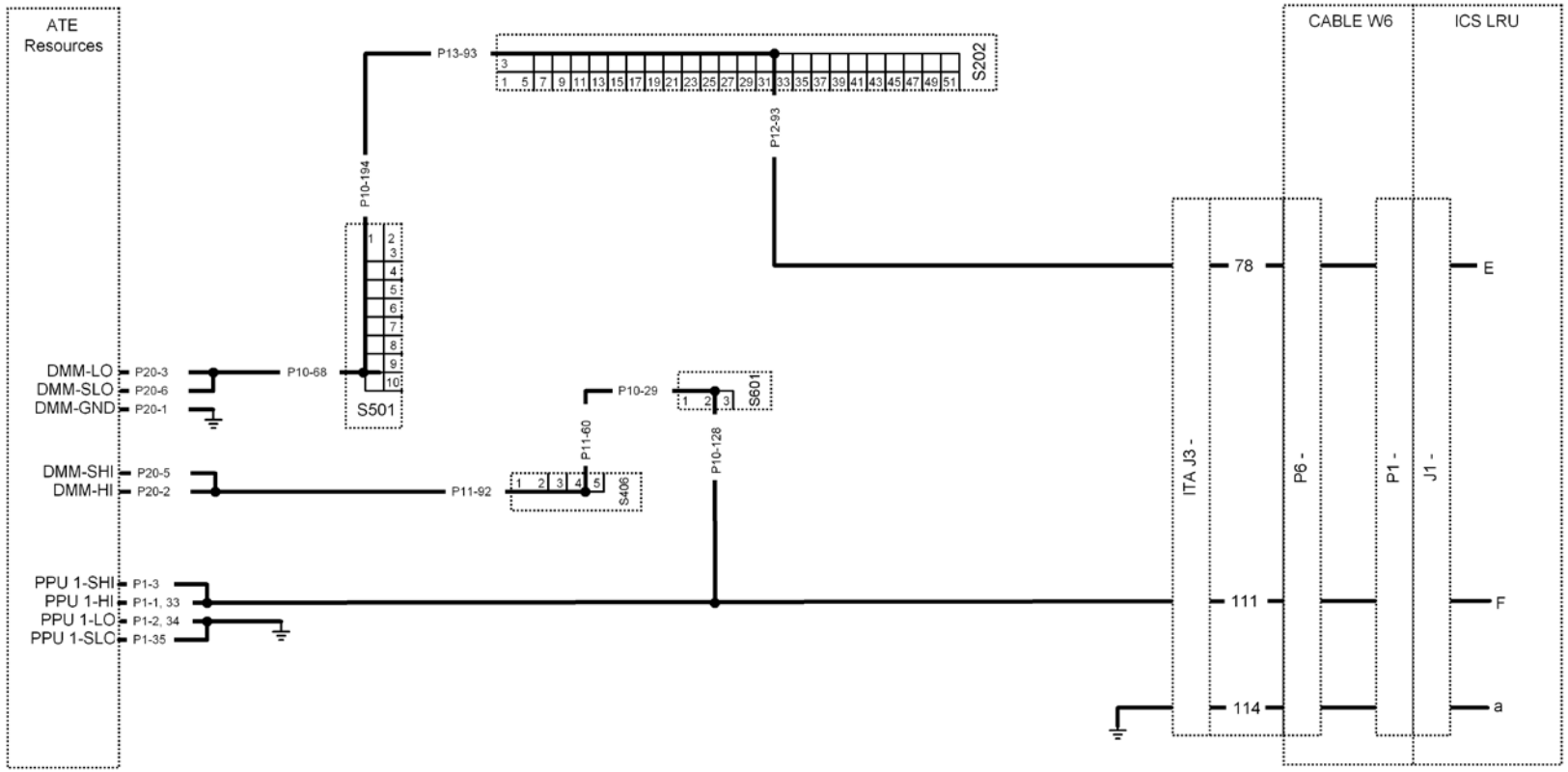
UUT PINS	VOLTAGE	CURRENT	PPU USED
J1-F(+)/J1-a(-)	+15.0VDC +/-0.5VDC	1.0 A	DCPS 1
J1-H(+)/J1-G(-)	+24.0VDC +/-0.5VDC	3.0 A	DCPS 2

UUT POWER UP TESTS

Step 7 +15 VDC Power Up Test

This step applies UUT +15V power and verifies the UUT +15V power input circuit is free of shorts that were not detected by the Safe-to-Turn-On Test by using the DMM to measure the voltage between J1-F / J1-E (GND). The voltage should be from 14.5 Vdc to 15.5 Vdc.

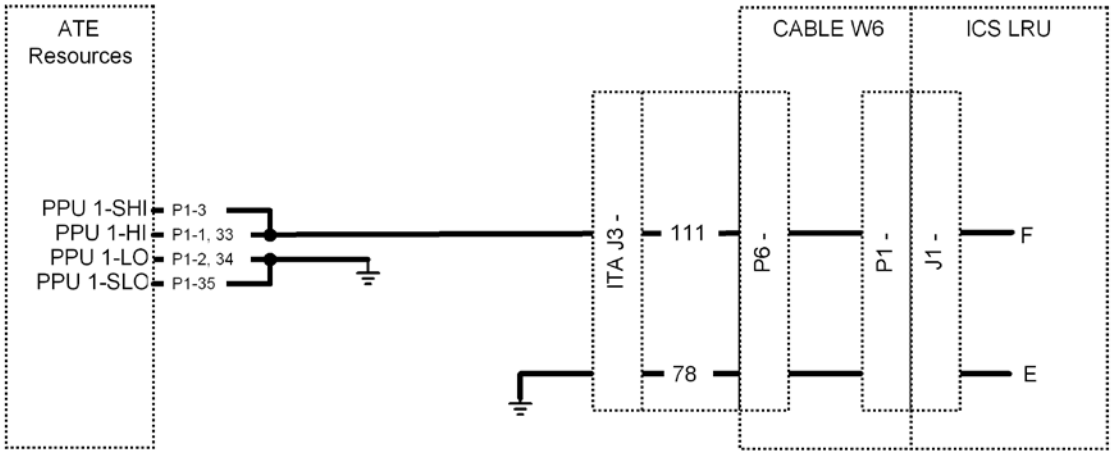
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P13-93
S202
P12-93
P10-194
S501
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-68
P10-29
S601
P11-60
P10-128
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
S406
PPU 1-SHI
PPU 1-HI
PPU 1-LO
PPU 1-SLC
P1-3
P1-1, 33
P1-2, 34
P1-35
ITA J3 -
P6 -
P1 -
J1 -
78
111
114
E
F
a

Step 8 Power Filter (A6) Continuity Test

This step verifies continuity of TEMPEST Filter Assembly, A6 by reading the current flow on the +15 VDC load of DCPS #1. The power supply current read-back function is used to verify greater than 200mA at J1-F / J1-E (GND).

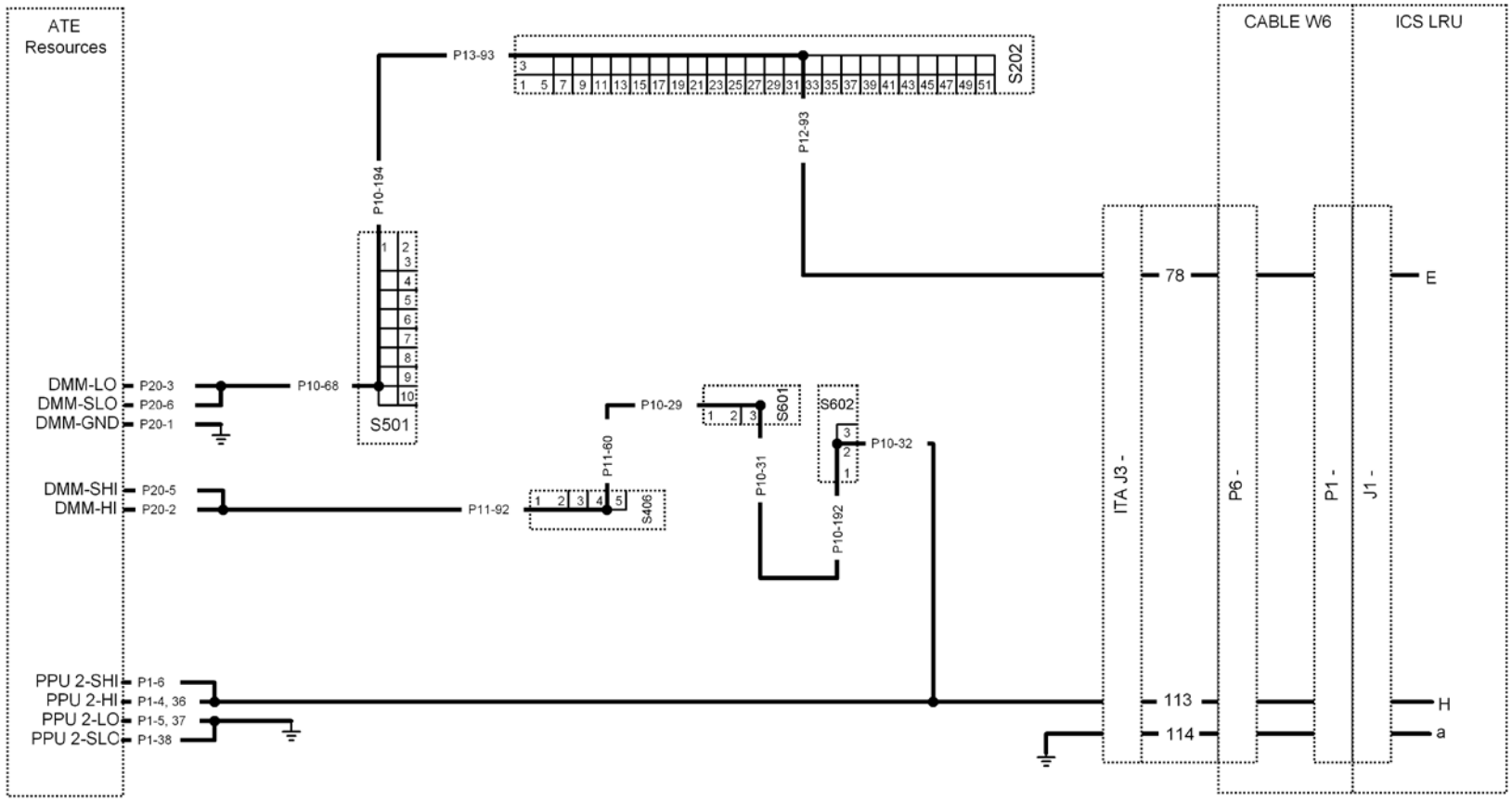
Connection Path as follows:



Step 9 +24 VDC Power Up Test

This step applies UUT +24V power and verifies the UUT +24V power input circuit is free of shorts that were not detected by the Safe-to-Turn-On Test by using the DMM to measure the voltage between J1-H / J1-E (GND). The voltage should be from 23.5 Vdc to 24.5 Vdc.

Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P13-93
S202
P12-93
P10-194
S501
DMM-LO P20-3
DMM-SLO P20-6
DMM-GND P20-1
P10-68
DMM-SHI P20-5
DMM-HI P20-2
P11-92
P11-60
S406
P10-29
S601
P10-31
S602
P10-32
P10-192
ITA J3 -
P6 -
P1 -
J1 -
78
E
113
H
114
a
PPU 2-SHI P1-6
PPU 2-HI P1-4, 36
PPU 2-LO P1-5, 37
PPU 2-SLO P1-38

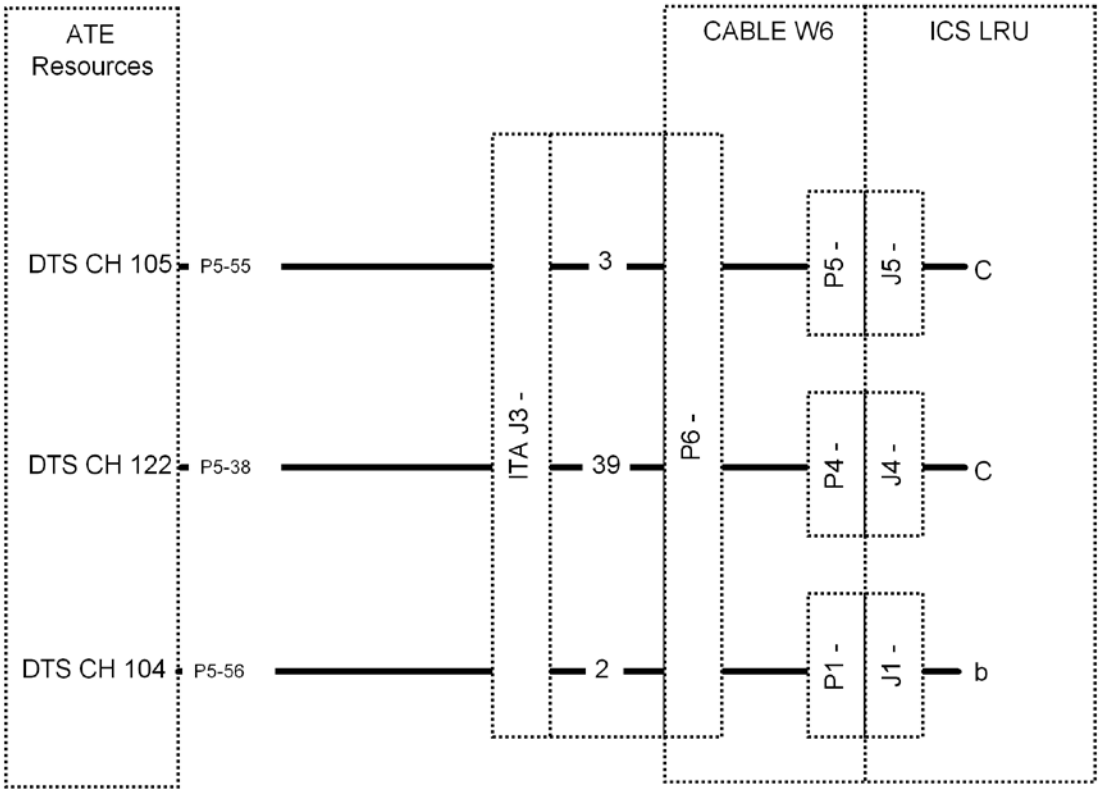
MODULE 1 PUSH-TO-TALK TESTS

Module 1 verifies the functionality of the radio and intercom key-line logic on CCA A4 by verifying that key-line events cause the appropriate interrupt indications on the Serial Data Out line.

Step 101 Input Pull-Ups Test

This step uses the DTS to statically verify the input pullups on CCA A4 KEYLINE inputs at J1-b (ICKEYL ENABLE), J4-C (RADKEY), and J5-C (ICKEY).

Connection Path as follows:



Step 102 'SDO' Line Quiescent State Test

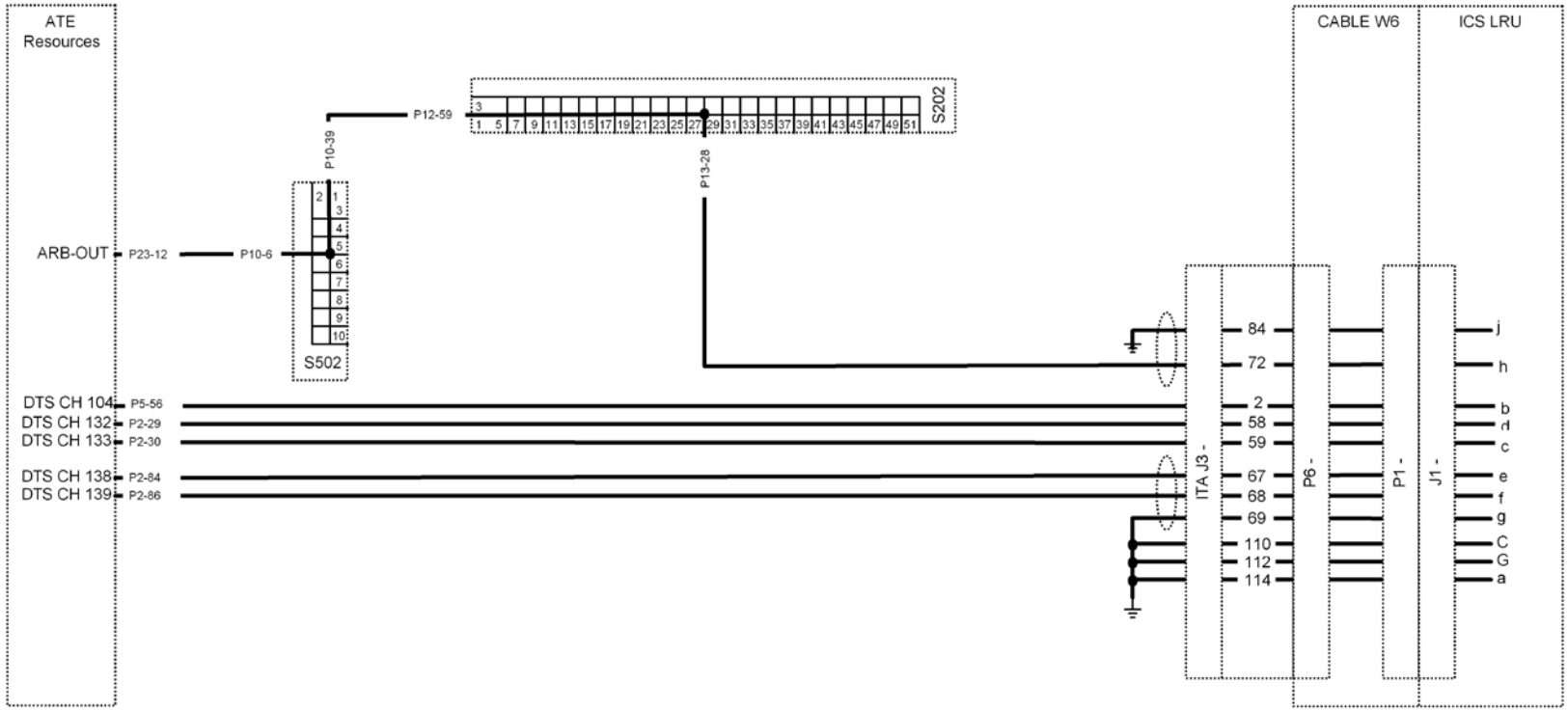
This test verifies the quiescent state of the logic on CCA A4. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to apply a logic LO at ICKEYL ENABLE input to inhibit false interrupts and to send a differential CLEAR-F command on 'Serial Data In', J1-d(+)/J1-c(-), to place the A4 logic in a reset or quiescent state as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The differential 'Serial Data Out' line, J1-e/J1-f, is then verified by the DTS to be HI: J1-e(+) = B’1’ / J1-f(-) = B’0’.

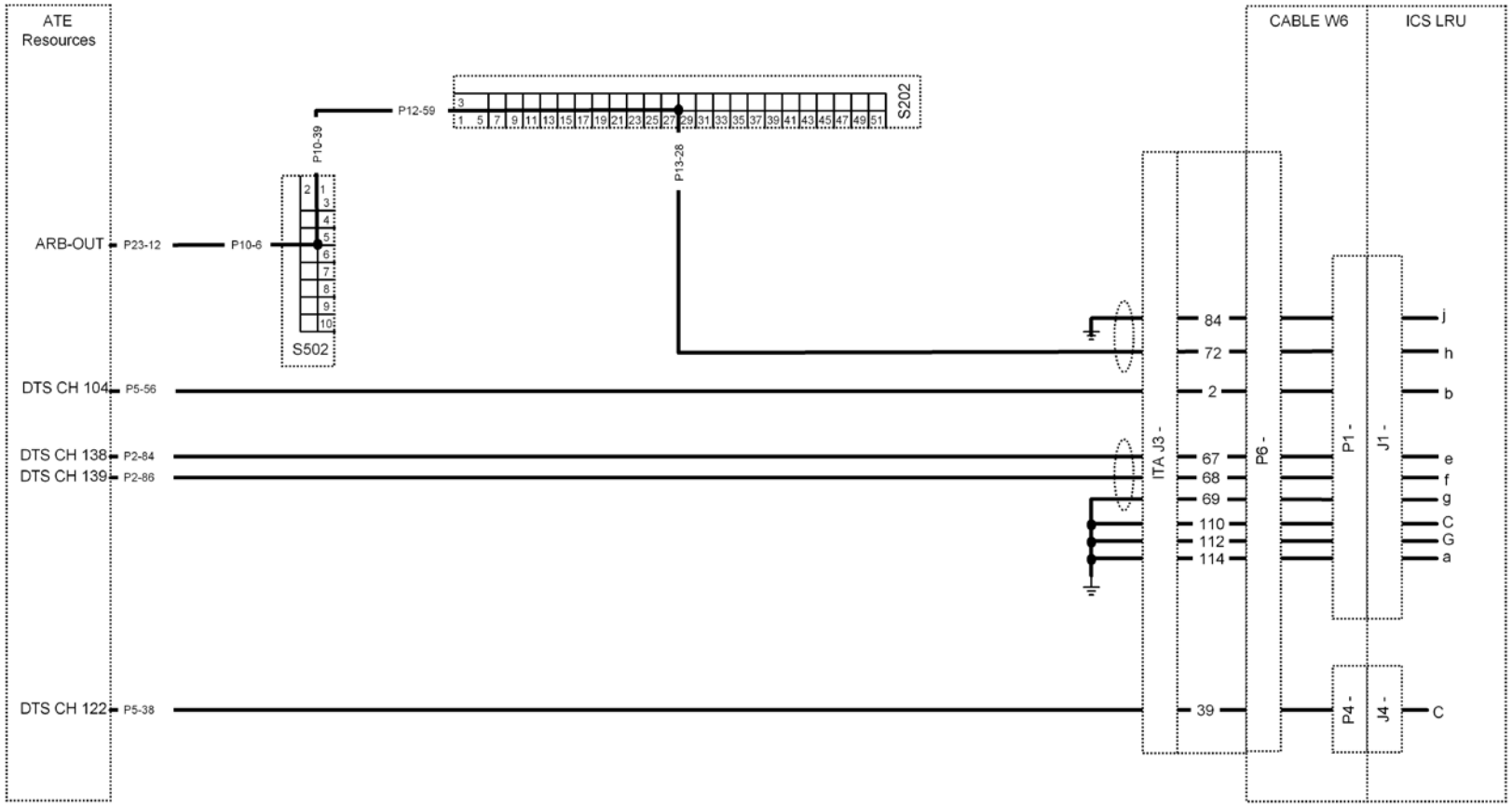
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
S502
ARB-OUT
P23-12
P10-6
DTS CH 104
P5-56
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
2
58
59
67
68
69
110
112
114
j
h
b
d
c
e
f
g
C
G
a

Step 103 RADKEY Down - Request-for-Attention Generation Test

This test verifies the 'RADKEY' keyline Request-For-Attention logic on CCA A4 detects a Key-Down event (LO at J4-C). With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h and a logic LO at ICKEYL ENABLE input, J1-b (see Step 102), the DTS is used to apply a logic LO at RADKEY input J4-C to simulate a Key-Down event. The 'Serial Data Out' line, J1-e/J1-f, is then verified statically by the DTS to have toggled LO: J1-e(+) = B'0' / J1-f(-) = B'1', indicating a Request-For-Attention is generated.

Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
ARB-OUT
P23-12
P10-6
P10-39
S502
P12-59
S202
P13-28
DTS CH 104
P5-56
DTS CH 138
P2-84
DTS CH 139
P2-86
DTS CH 122
P5-38
ITA J3 -
P6 -
P1 -
J1 -
P4 -
J4 -
84
72
2
67
68
69
110
112
114
39
j
h
b
e
f
g
C
G
a
C

Step 104 RADKEY Request-for-Attention Reset Test

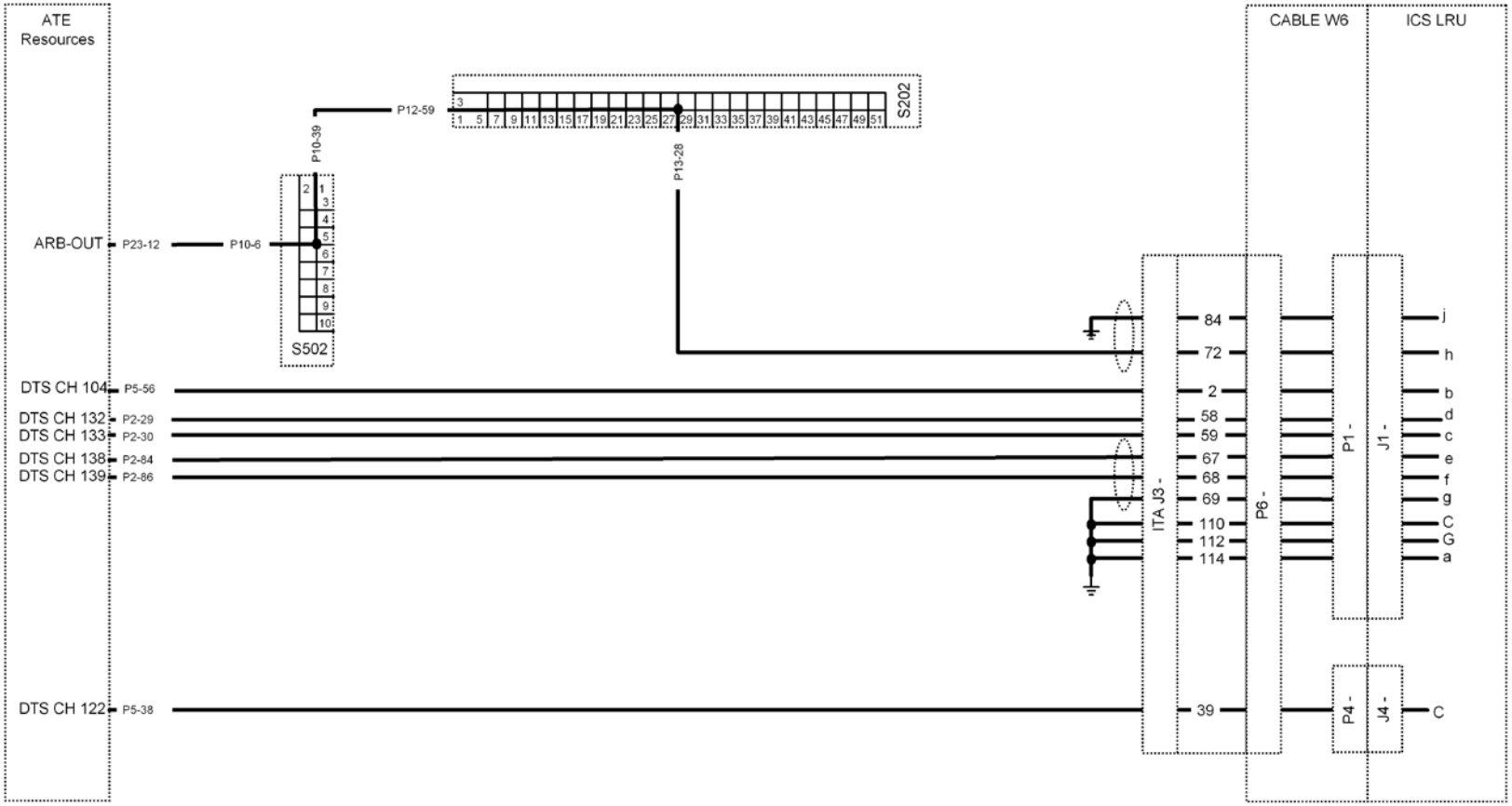
This test verifies the logic on CCA A4 resets the Request Generator circuitry upon receipt of a serial REQUEST-ACKNOWLEDGE. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, a logic LO at ICKEYL ENABLE input, J1-b (see Step 102), and a logic LO at RADKEY input, J4-C (see Step 103), the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a REQUEST-ACKNOWLEDGE as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (EVEN)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The differential 'Serial Data Out' line, J1-e/J1-f, is then verified by the DTS to have toggled HI: J1-e(+) = B’1’ / J1-f)-) = B’0’, indicating the Request Generator circuitry on A4 has been reset.

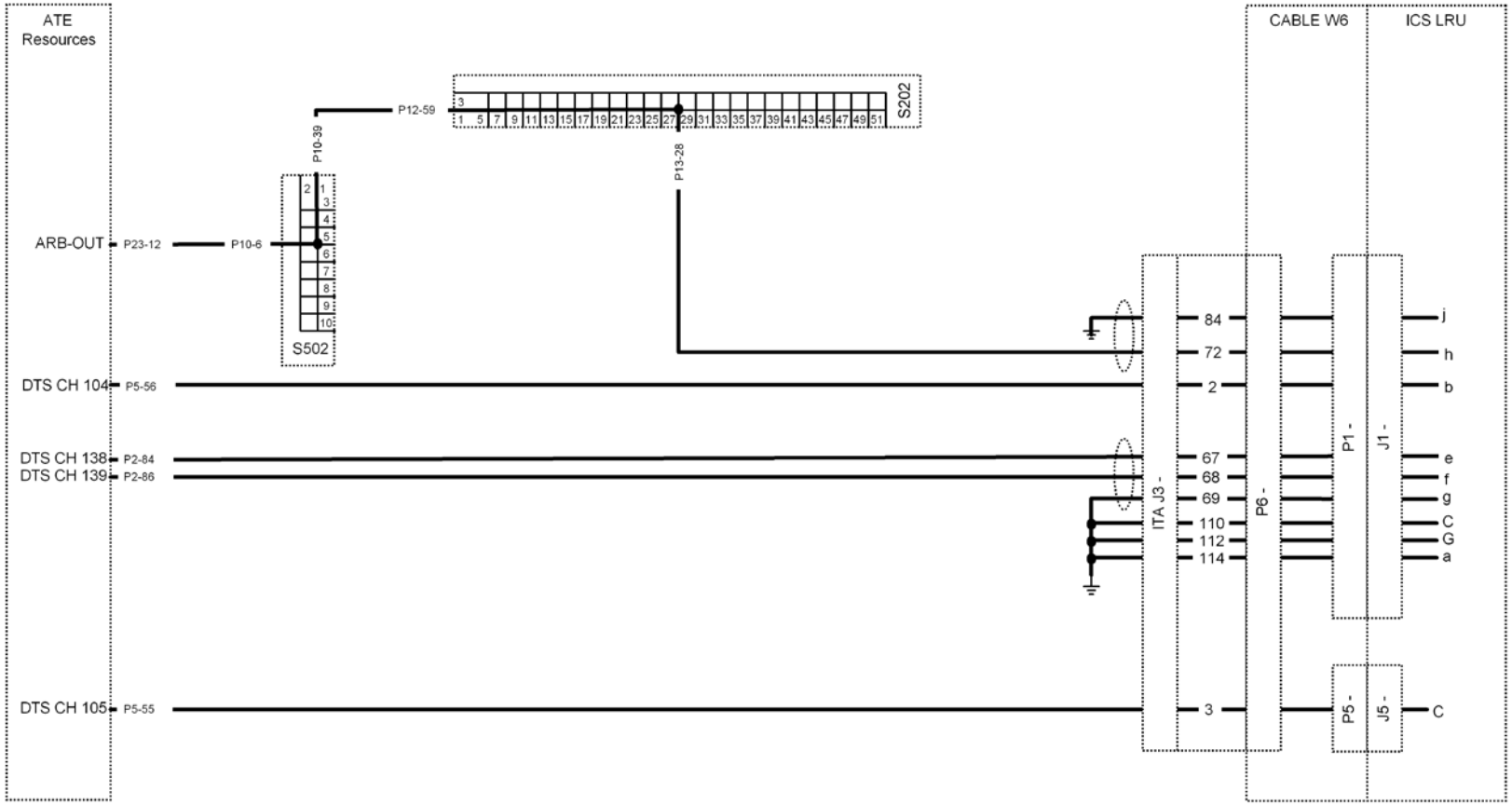
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 104
P5-56
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
DTS CH 122
P5-38
ITA J3 -
P6 -
P1 -
J1 -
P4 -
J4 -
84
72
2
58
59
67
68
69
110
112
114
39
j
h
b
d
c
e
f
g
C
G
a
C

Step 105 ICKEY Down - Request Generator Test

This test verifies the 'ICKEY' keyline Request-For-Attention logic on CCA A4 detects a Key-Down event (LO at J5-C). With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h and a logic LO at ICKEYL ENABLE input, J1-b (see Step 102), the DTS is used to apply a logic LO at ICKEY input J5-C to simulate a Key-Down event. The 'Serial Data Out' line, J1-e/J1-f, is then verified statically by the DTS to have toggled LO: J1-e(+) = B'0' / J1-f(-) = B'1', indicating a Request-For-Attention is generated.

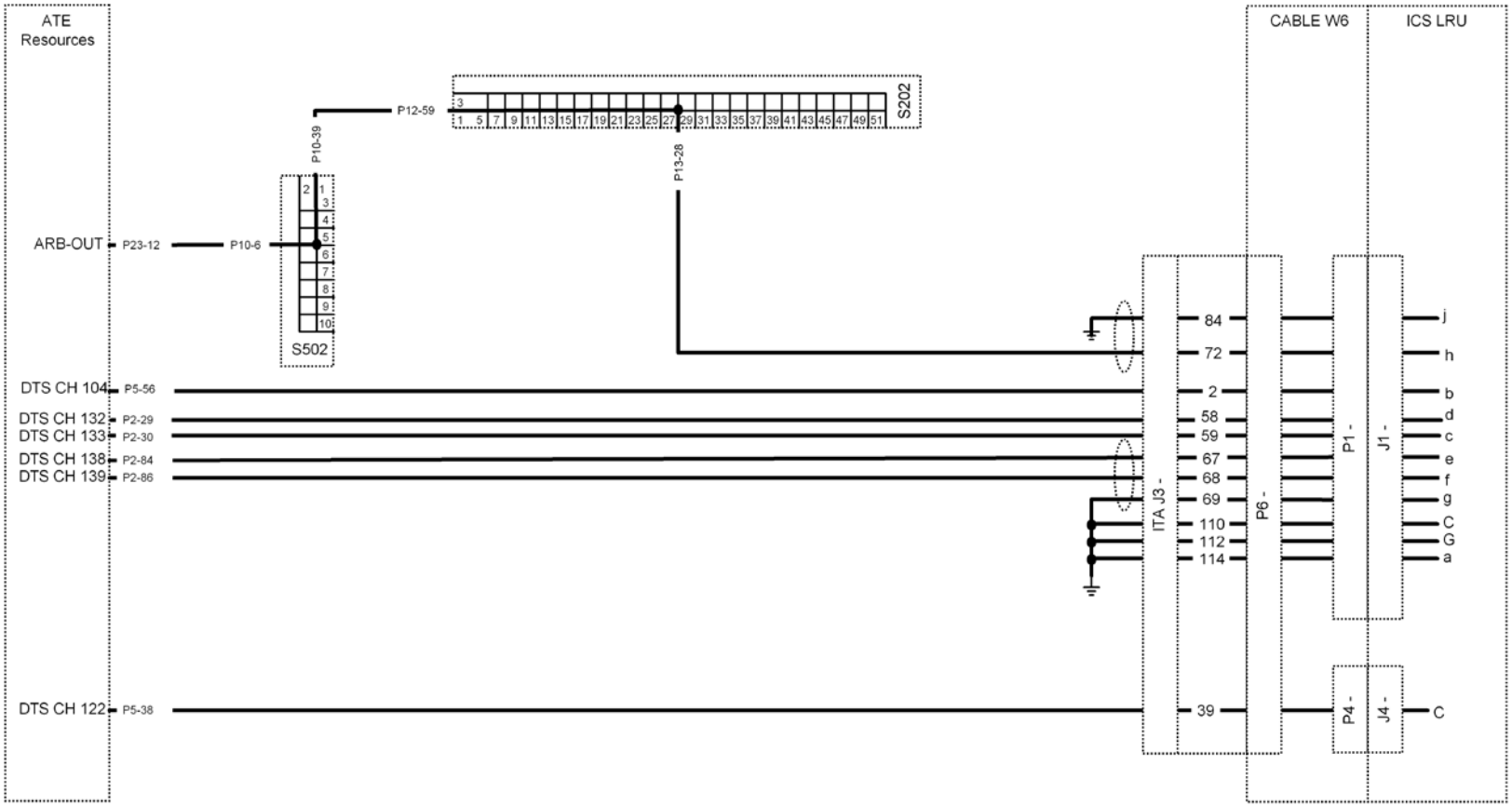
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
ARB-OUT
P23-12
P10-6
P10-39
P12-59
P13-28
S202
S502
DTS CH 104
P5-56
DTS CH 138
P2-84
DTS CH 139
P2-86
DTS CH 105
P5-55
ITA J3 -
P6 -
P1 -
J1 -
P5 -
J5 -
84
72
2
67
68
69
110
112
114
3
j
h
b
e
f
g
C
G
a
C

Step 106 RADKEY Operation Test

This step verifies that the RADKEY DOWN and UP events are detected and the data character codes are correctly transmitted by the A4 CCA. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h and a logic LO at ICKEYL ENABLE input, J1-b (see Step 102), the DTS (M910NAM executing DTB file RAD-KEY.dtb) is used to (1) Perform a KEY-DOWN event; (2) Output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE' to prompt the UUT to transmit the code for the RADKEY DOWN (B'11001100000'). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct RADKEY DOWN code (each bit is 16 clock periods in duration); (3) Perform a KEY-UP event; and (4) Verify the correct RADKEY UP code (B'10000100000') on the 'Serial Data Out' line, J1-e/J1-f.

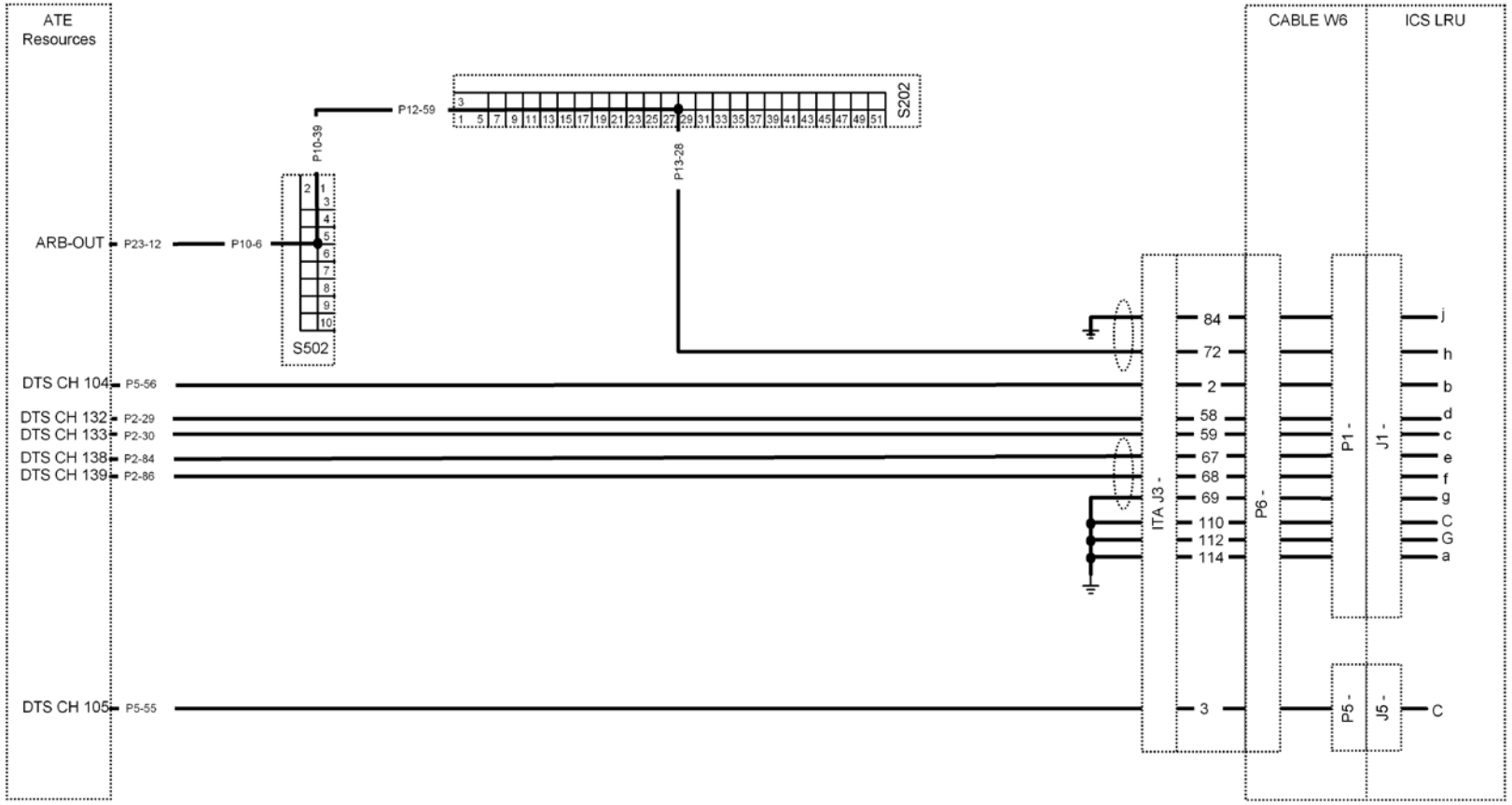
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
S502
ARB-OUT
P23-12
P10-6
DTS CH 104
P5-56
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
DTS CH 122
P5-38
ITA J3 -
P6 -
P1 -
J1 -
P4 -
J4 -
84
72
2
58
59
67
68
69
110
112
114
39
j
h
b
d
c
e
f
g
C
G
a
C

Step 107 ICKEY Operation Test

This step verifies that the ICKEY DOWN and UP events are detected and the data character codes are correctly transmitted by the A4 CCA. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h and a logic LO at ICKEYL ENABLE input, J1-b (see Step 102), the DTS (M910NAM executing DTB file IC-KEY.dtb) is used to (1) Perform a KEY-DOWN event; (2) Output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE' to prompt the UUT to transmit the code for the ICKEY DOWN (B'11010100000'). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct ICKEY DOWN code (each bit is 16 clock periods in duration); (3) Perform a KEY-UP event; and (4) Verify the correct IC-KEY UP code (B'10000100000')) on the 'Serial Data Out' line, J1-e/J1-f.

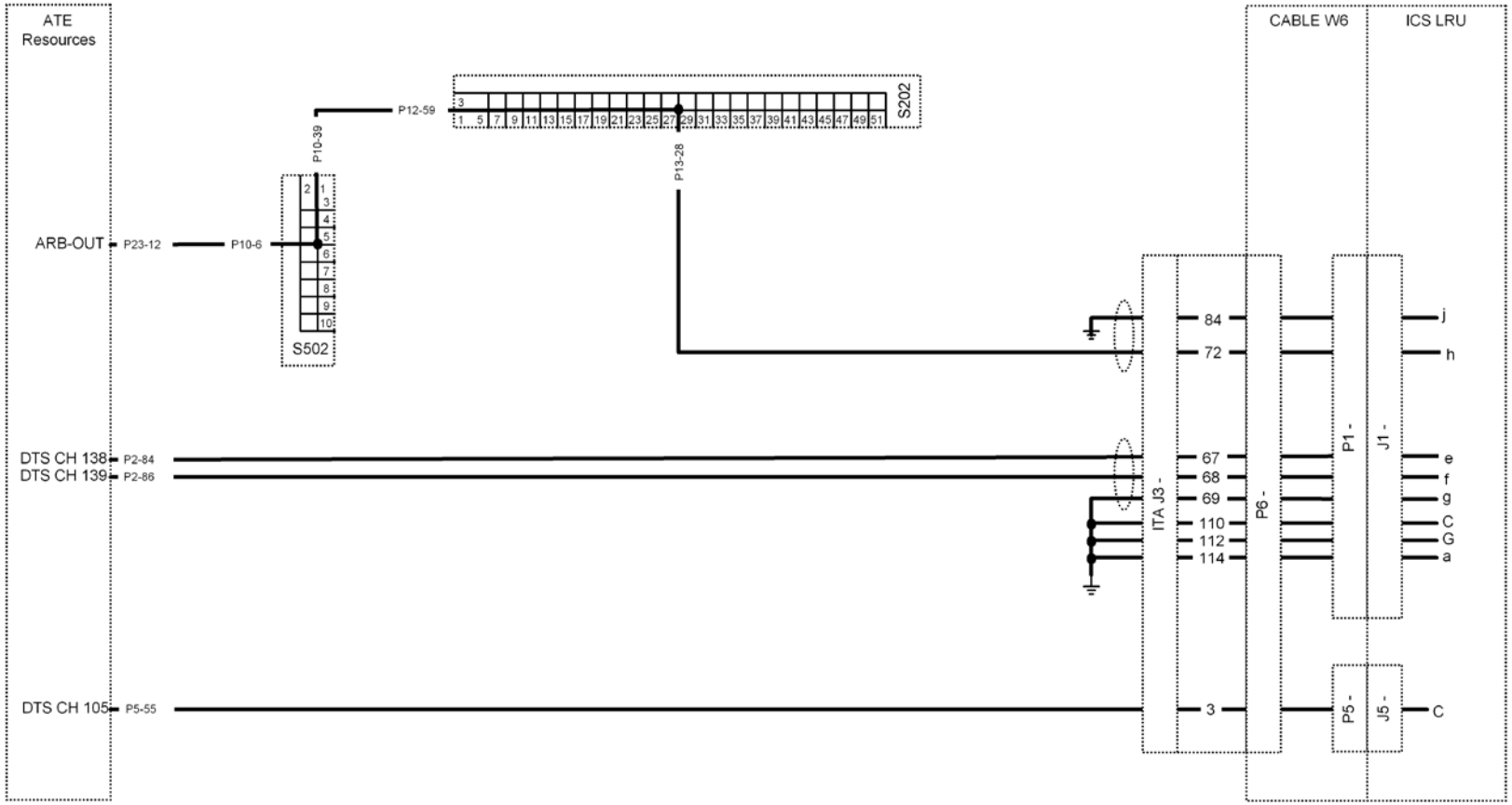
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 104
P5-56
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
DTS CH 105
P5-55
ITA J3 -
P6 -
P1 -
J1 -
P5 -
J5 -
84
72
2
58
59
67
68
69
110
112
114
3
j
h
b
d
c
e
f
g
C
G
a
C

Step 108 ICKEY ENABLE (J1-b): Keyline Disabled Test

This step verifies that the ICKEY input is inhibited from generating a Request-For-Attention with the ICKEYL ENABLE signal removed. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h (see Step 102), and the ICKEYL ENABLE input at J1-b open, the DTS is used to apply a logic LO at ICKEY input J5-C to simulate a Key-Down event. The differential 'Serial Data Out' line, J1-e/J1-f, is then verified to have remained HI: J1-e(+) = B’1’ / J1-f)-) = B’0’, indicating a Request-For-Attention is inhibited.

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 138
P2-84
DTS CH 139
P2-86
DTS CH 105
P5-55
ITA J3 -
P6 -
P1 -
J1 -
P5 -
J5 -
84
72
67
68
69
110
112
114
3
j
h
e
f
g
C
G
a
C

MODULE 2 LAMP/KEYLINE RELAY TESTS

Module 2 verifies the functionality of portions of the decoder logic on CCA A4, front panel lamps, the lamp dimmer circuitry on CCA A5, and chassis mounted components Q1, R2 (BIGHTNESS Control), and keyline relays K1 and K2. Each front panel lamp is illuminated one at a time and the operator is prompted to verify that only the lamp being tested is illuminated.

Step 201 'CDR POS 1' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'CDR POS 1' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'10001000000') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'CDR POS 1' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'CDR POS 1' lamp is illuminated as shown in Figure 5-1.

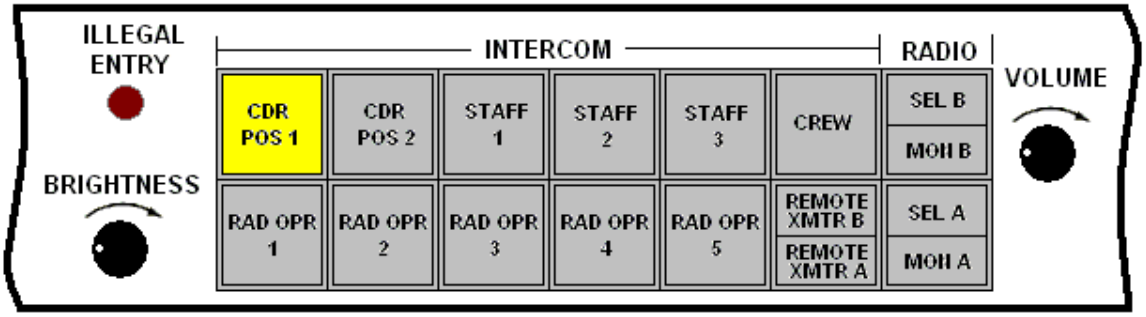
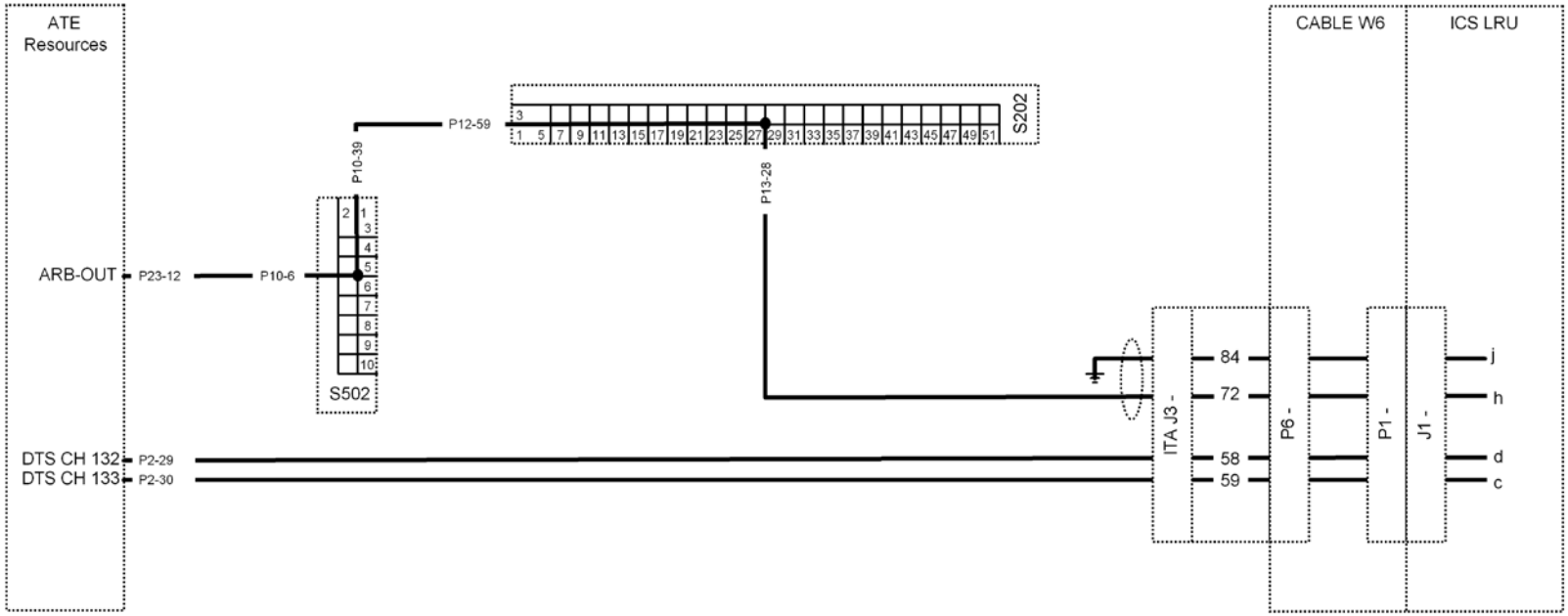


Figure 5-1

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'CDR POS 1' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 202 'CDR POS 2' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'CDR POS 2' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'11001000010') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'CDR POS 2' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'CDR POS 2' lamp is illuminated as shown in Figure 5-2.

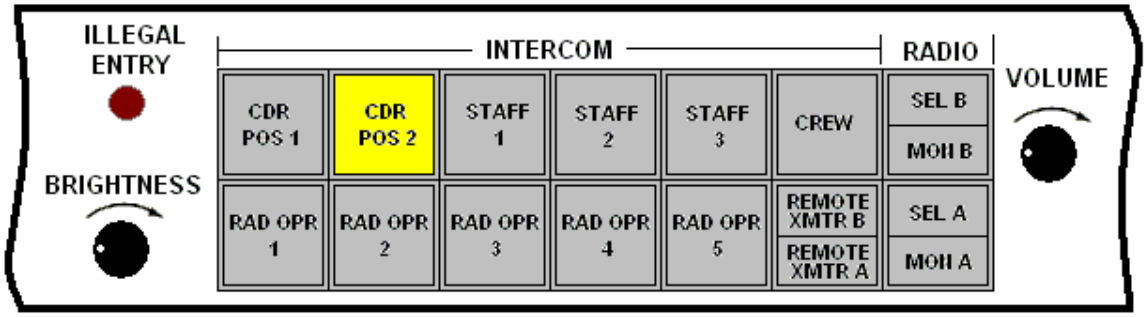
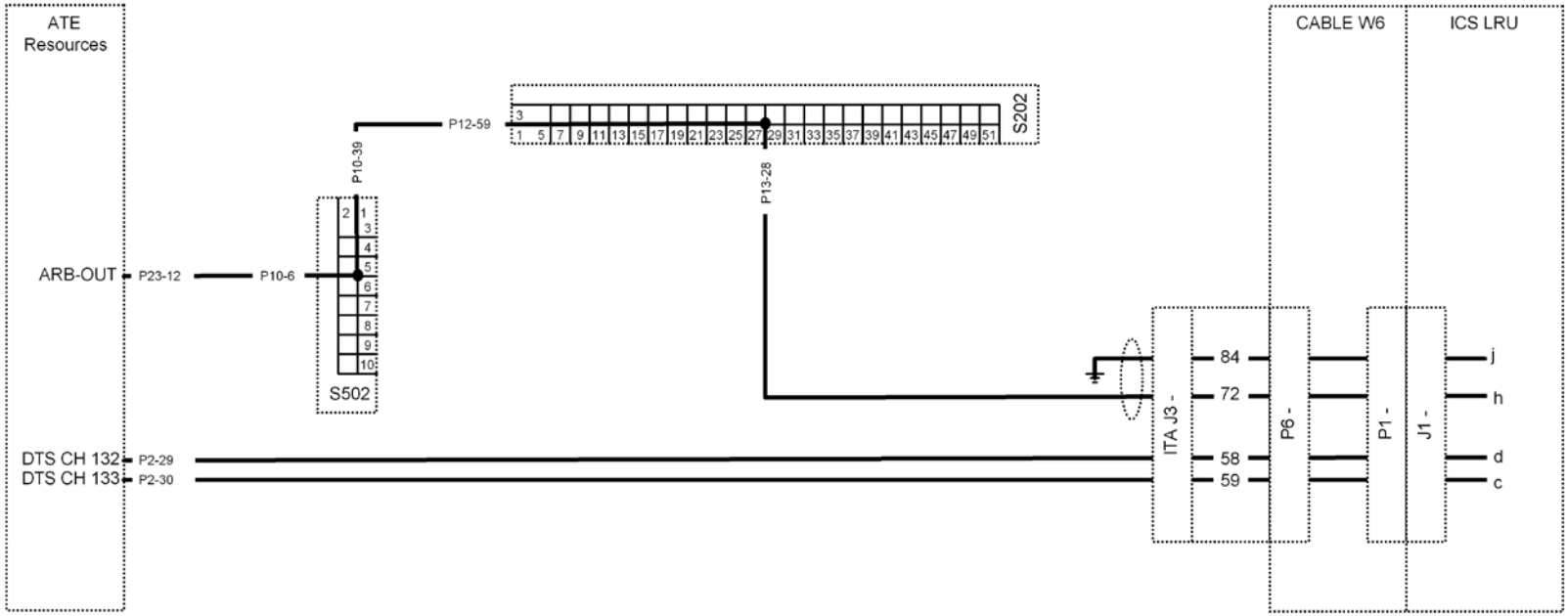


Figure 5-2

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'CDR POS 2' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 203 'STAFF 1' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'STAFF 1' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'11001000100') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'STAFF 1' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'STAFF 1' lamp is illuminated as shown in Figure 5-3.

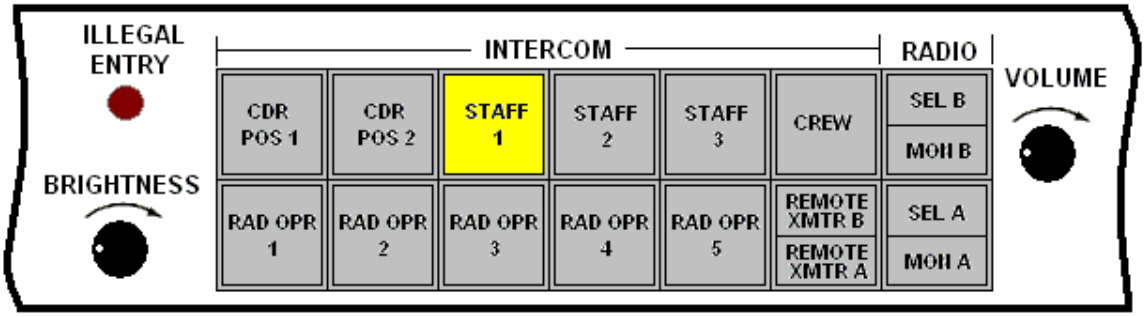
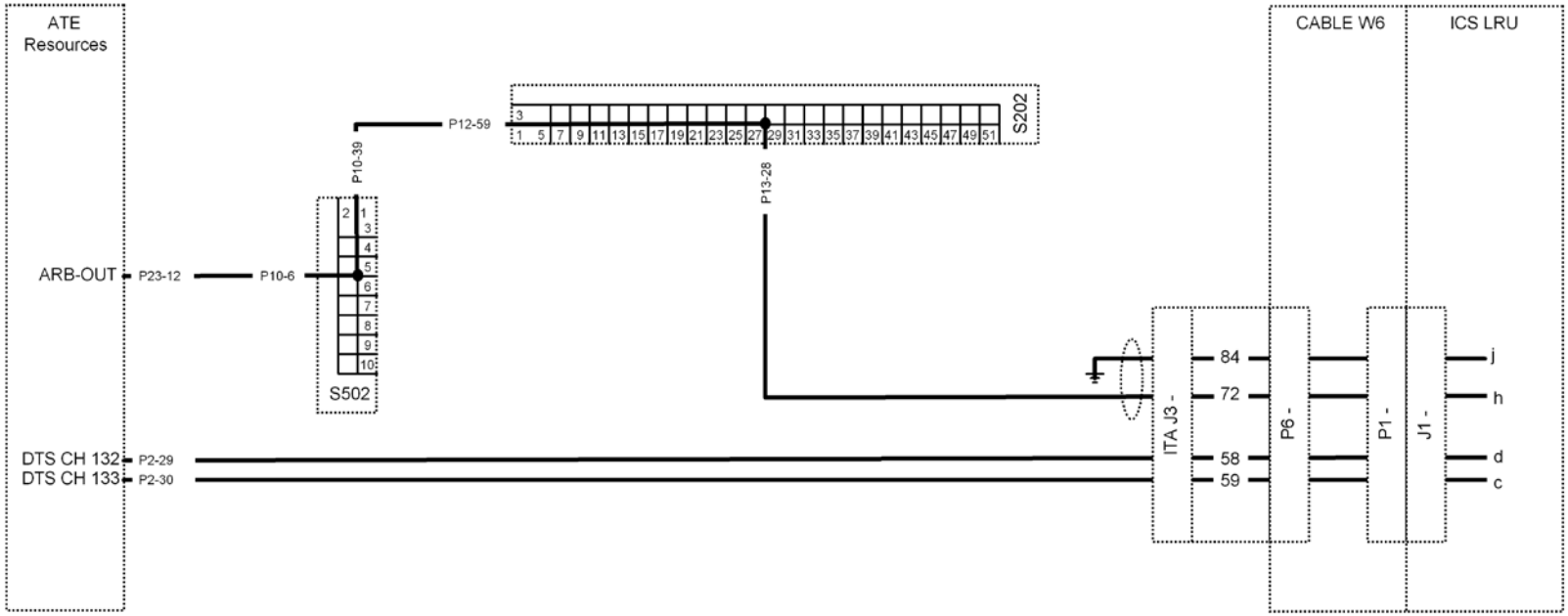


Figure 5-3

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'STAFF 1' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
P2-29
DTS CH 133
P2-30

Step 204 'STAFF 2' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'STAFF 2' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'10001000110') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'STAFF 2' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 '32KHz CLOCK' periods.

The operator is then prompted to verify that only the 'STAFF 2' lamp is illuminated as shown in Figure 5-4.

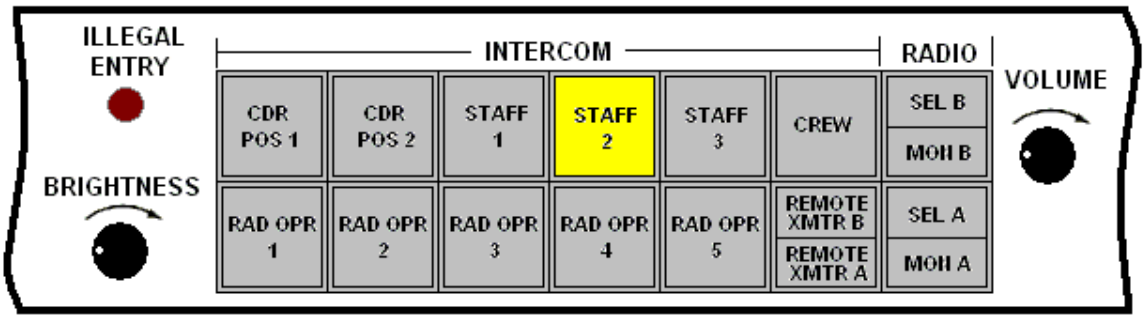
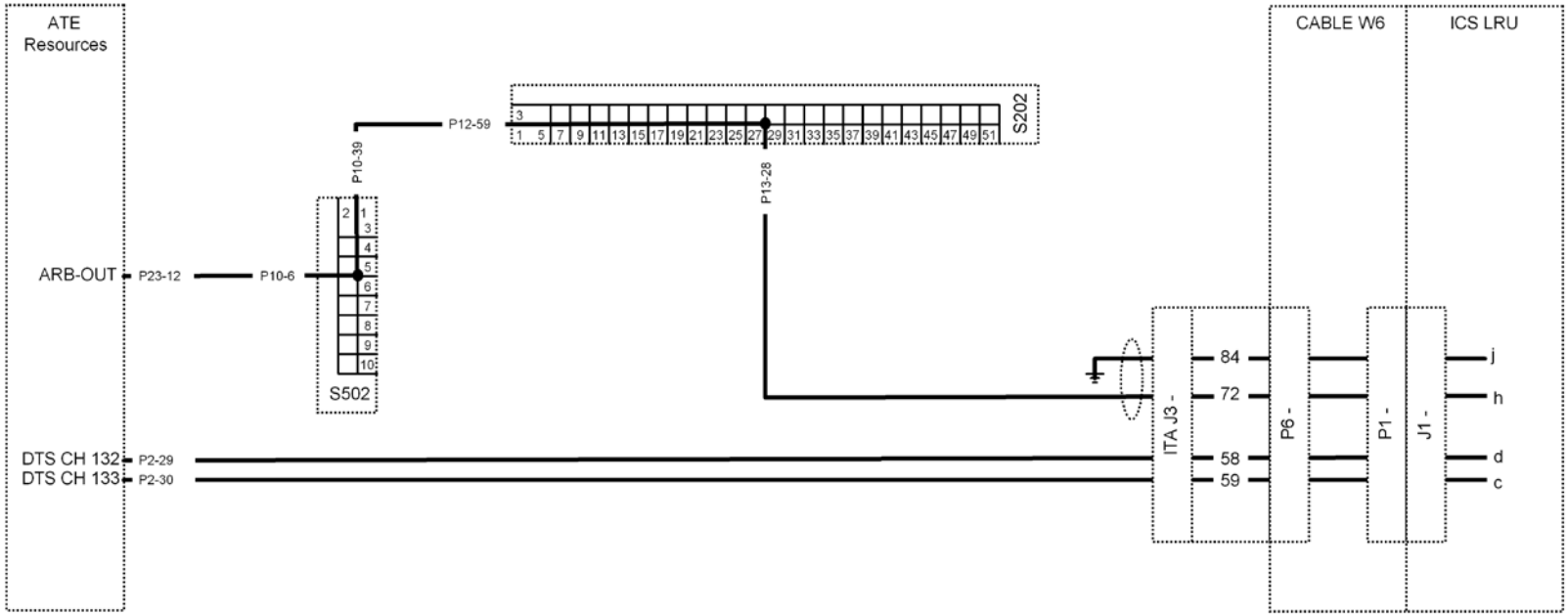


Figure 5-4

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'STAFF 2' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 205 'STAFF 3' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'STAFF 3' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'11001001000') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'STAFF 3' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'STAFF 3' lamp is illuminated as shown in Figure 5-5.

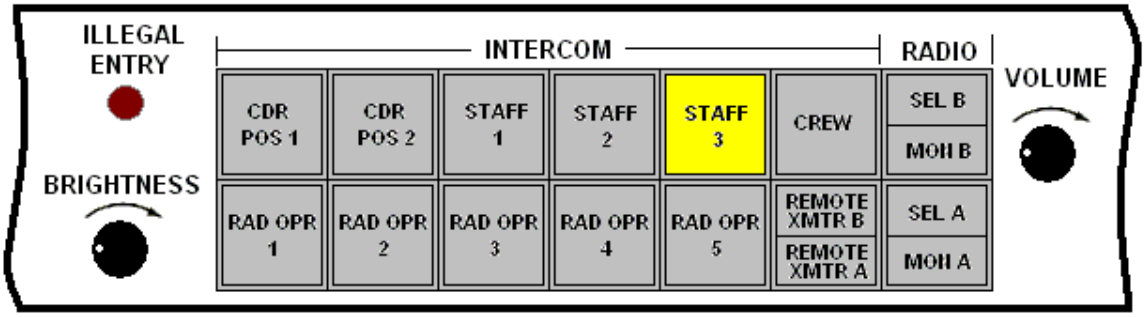
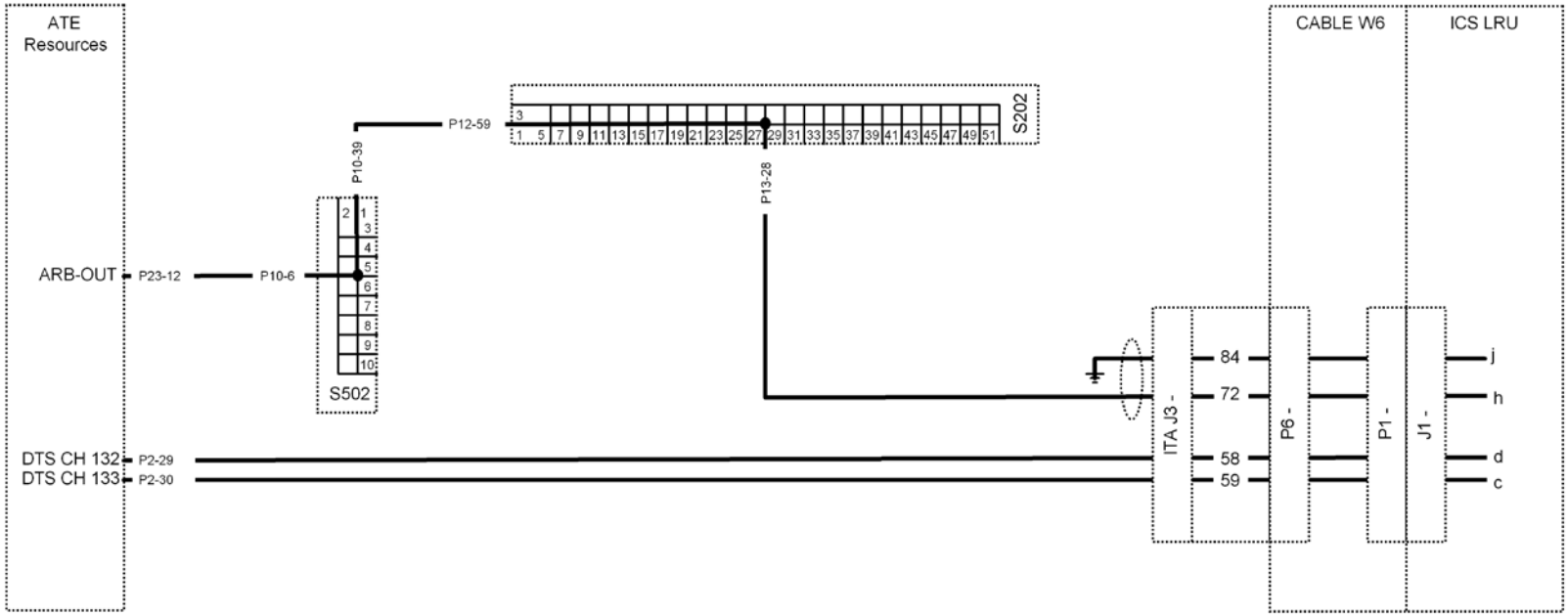


Figure 5-5

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'STAFF 3' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 206 'CREW' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'CREW' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'10001010100 ') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'CREW' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'CREW' lamp is illuminated as shown in Figure 5-6.

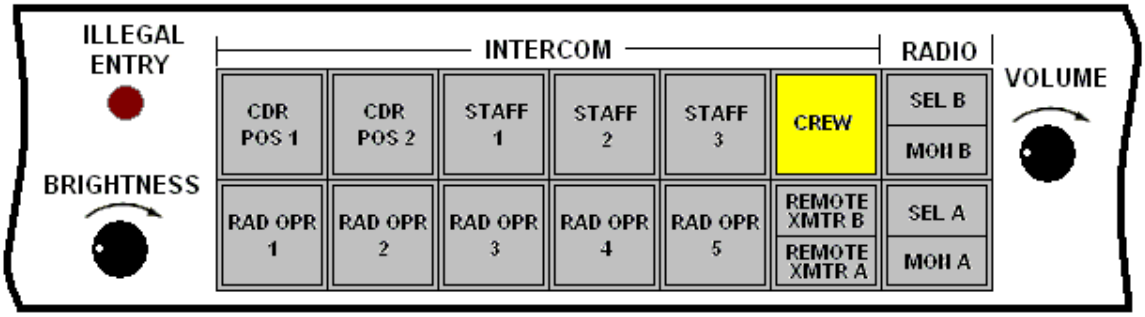
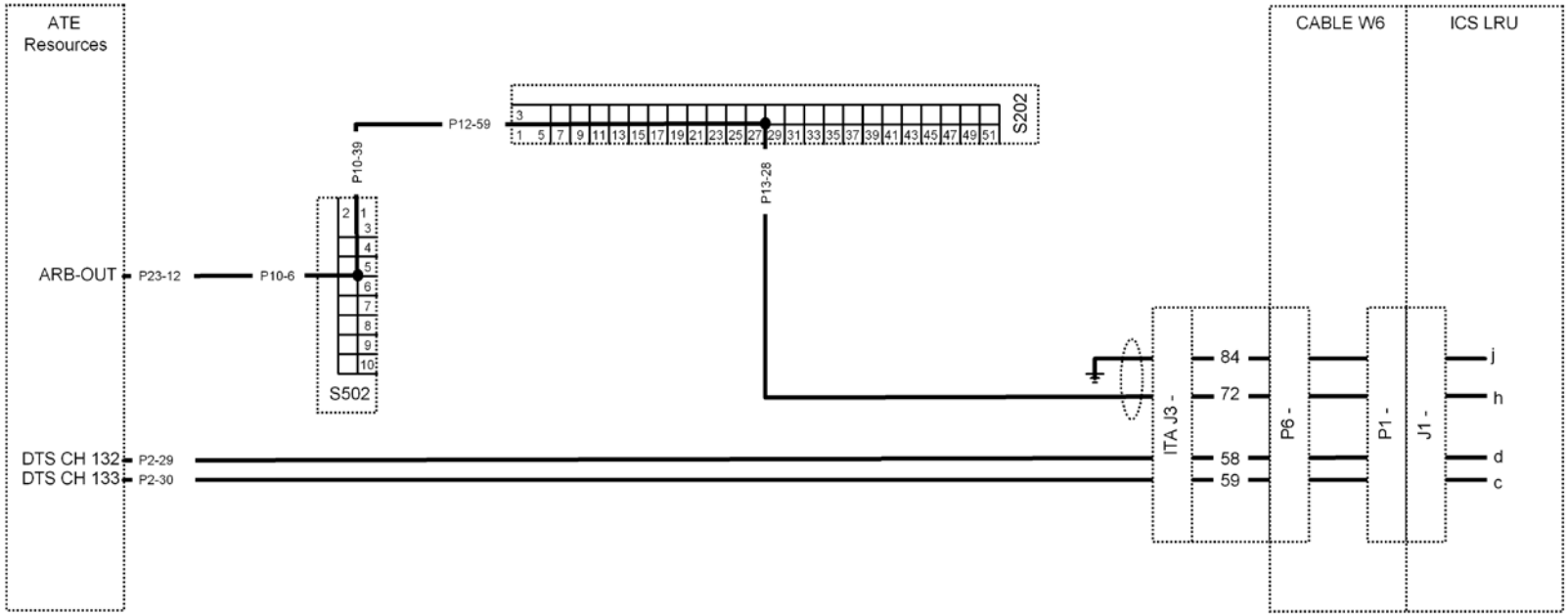


Figure 5-6

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'CREW' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 207 'SEL B' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'SEL B' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'11001010110') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'SEL B' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 '32KHz CLOCK' periods.

The operator is then prompted to verify that only the 'SEL B' lamp is illuminated as shown in Figure 5-7.

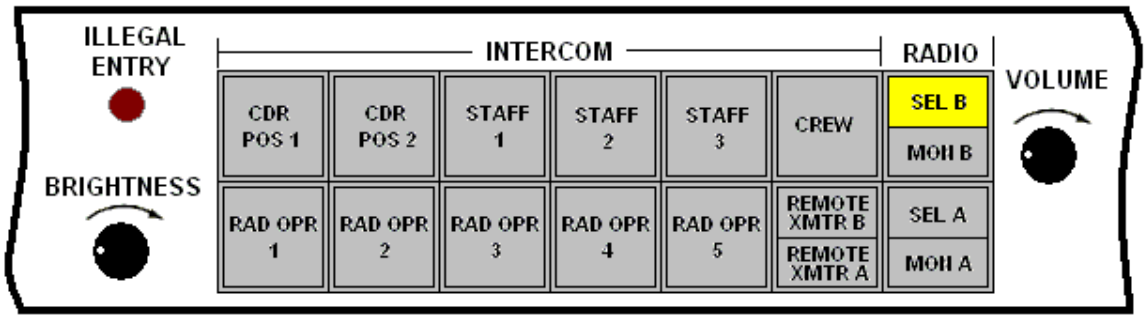
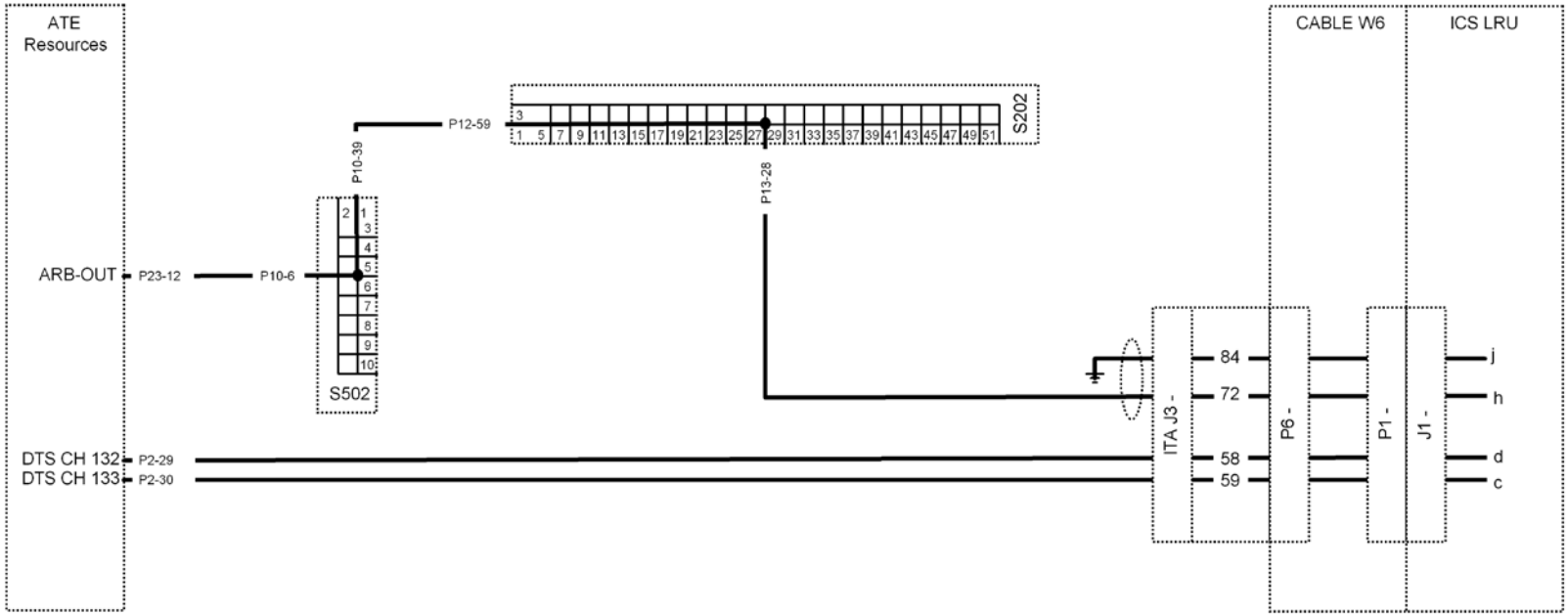


Figure 5-7

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'SEL B' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 208 'MON B' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'MON B' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'10001011000') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'MON B' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 '32KHz CLOCK' periods.

The operator is then prompted to verify that only the 'MON B' lamp is illuminated as shown in Figure 5-8.

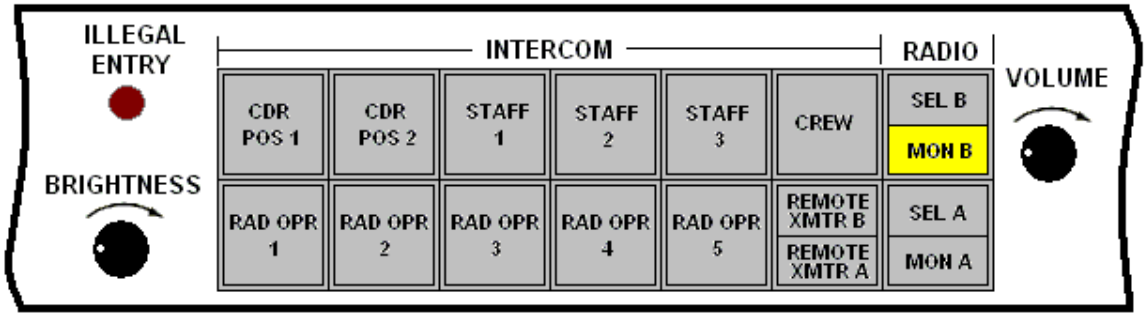
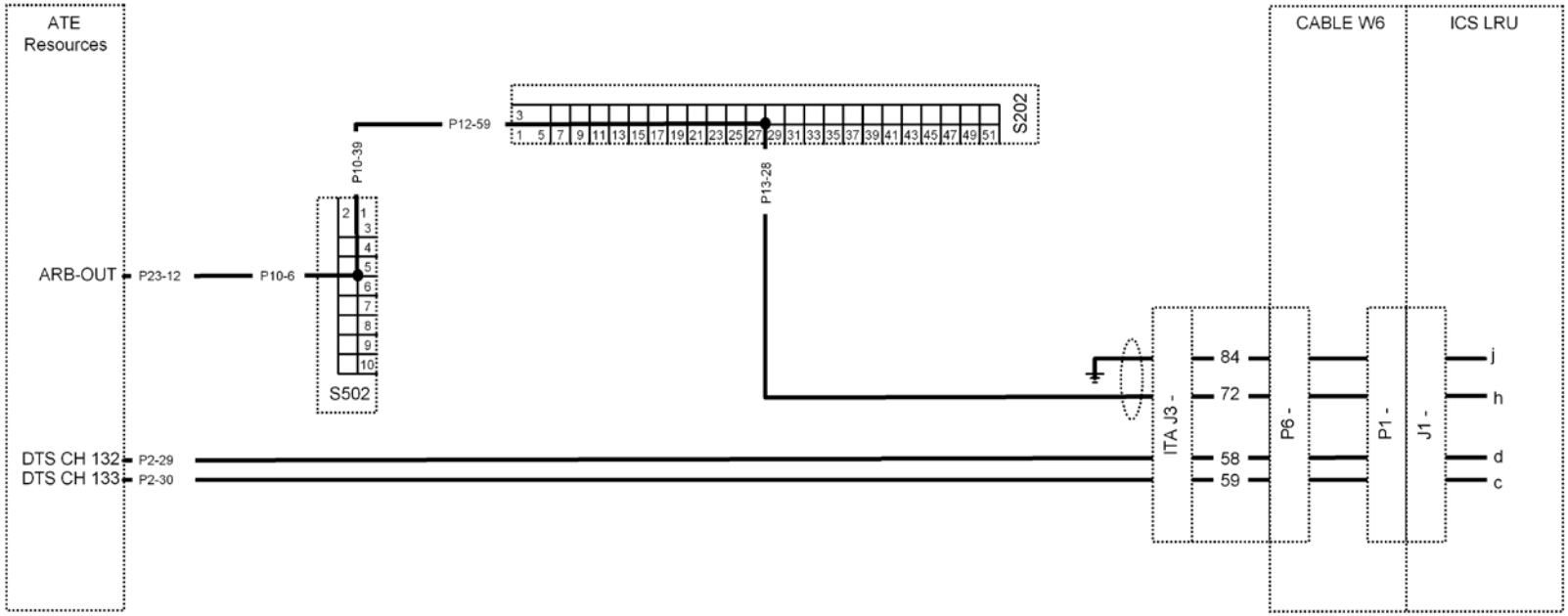


Figure 5-8

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'MON B' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 209 'RAD OPR 1' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'RAD OPR 1' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'10001001010') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'RAD OPR 1' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'RAD OPR 1' lamp is illuminated as shown in Figure 5-9.

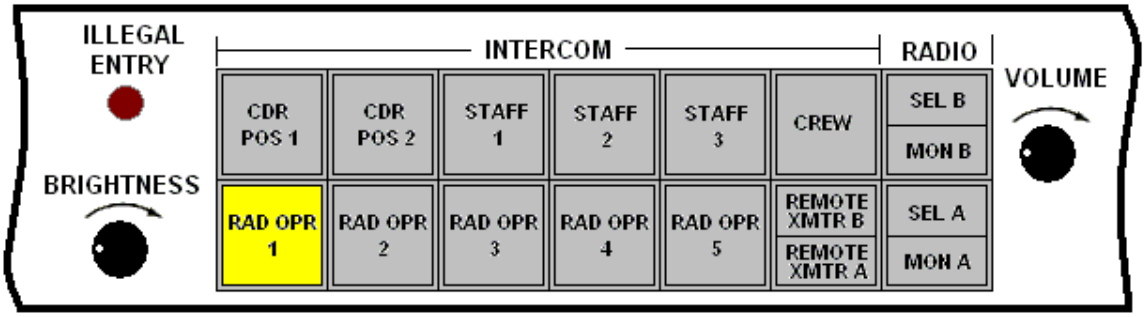
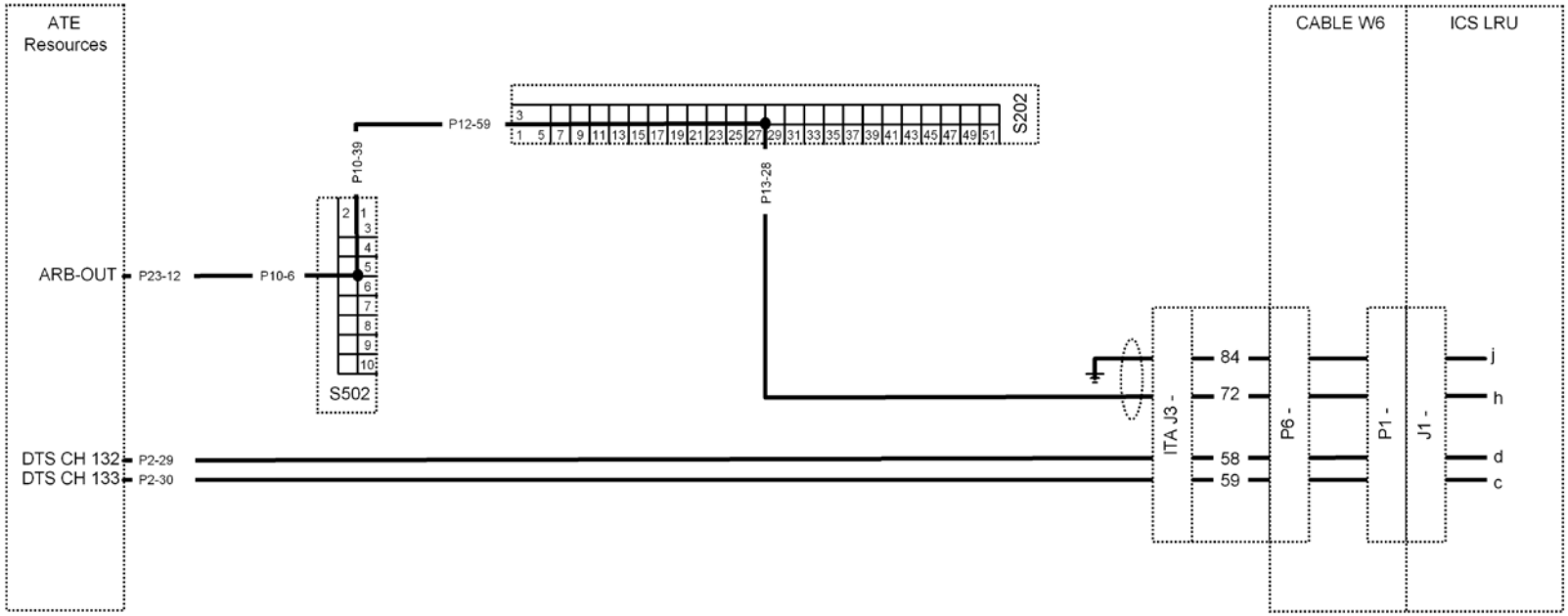


Figure 5-9

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'RAD OPR 1' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 210 'RAD OPR 2' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'RAD OPR 2' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'10001001100') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'RAD OPR 2' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'RAD OPR 2' lamp is illuminated as shown in Figure 5-10.

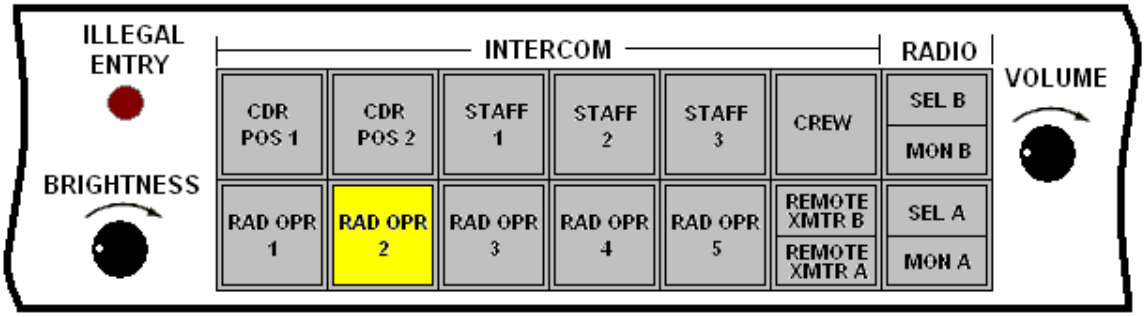
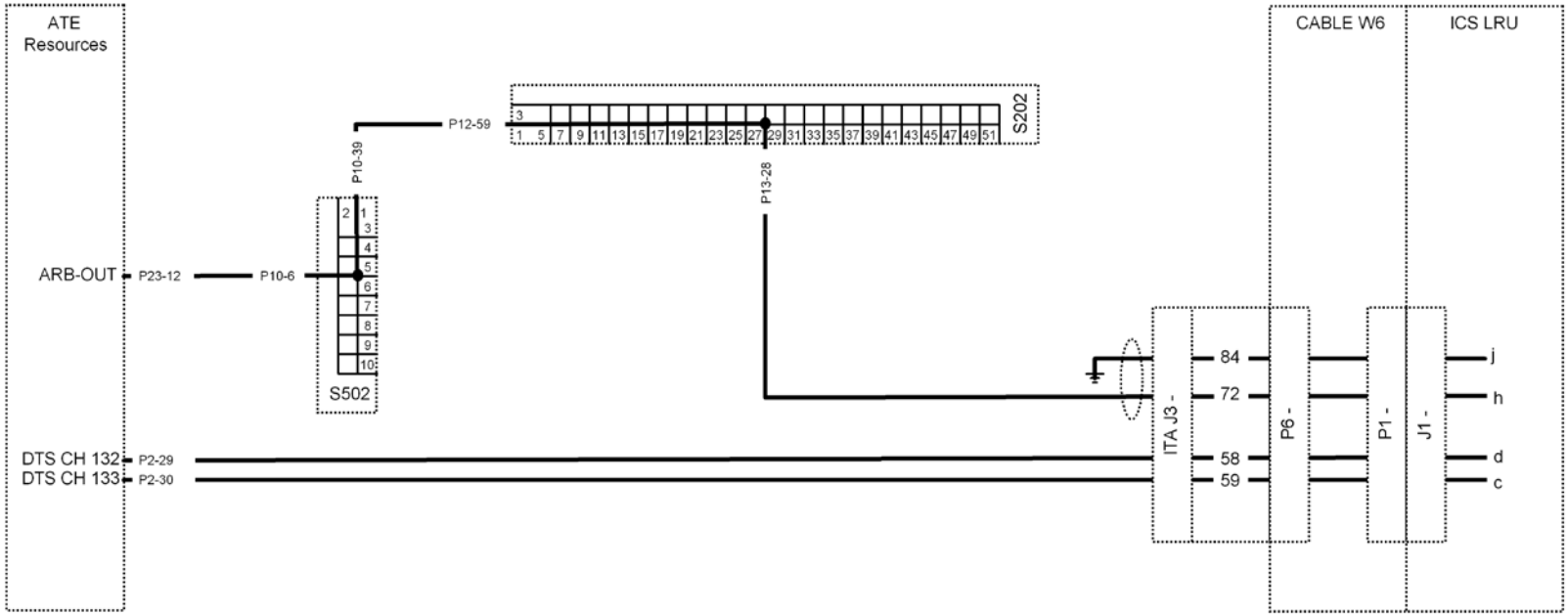


Figure 5-10

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'RAD OPR 2' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 211 'RAD OPR 3' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'RAD OPR 3' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'11001001110') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'RAD OPR 3' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'RAD OPR 3' lamp is illuminated as shown in Figure 5-11.

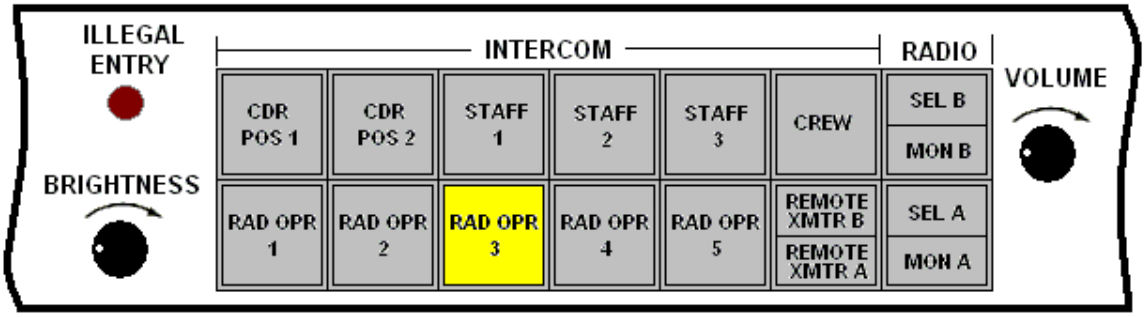
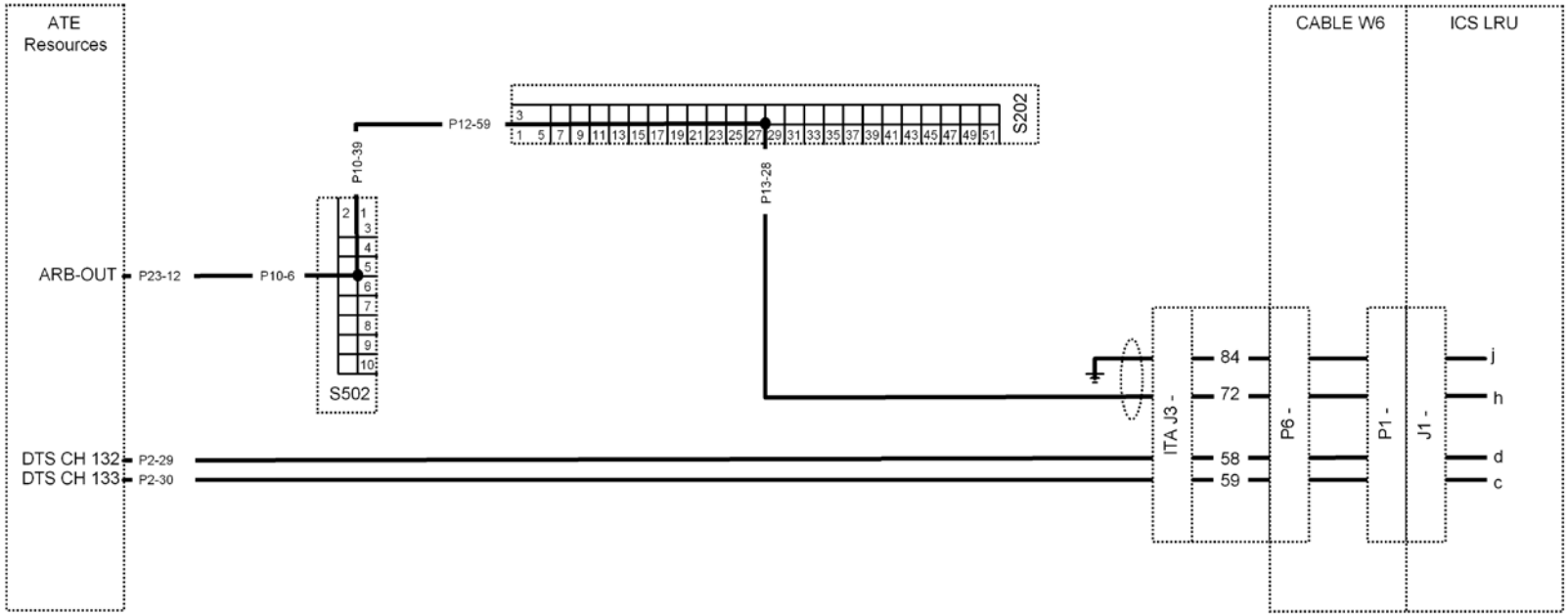


Figure 5-11

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'RAD OPR 3' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 212 'RAD OPR 4' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'RAD OPR 4' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'11001010000') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'RAD OPR 4' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'RAD OPR 4' lamp is illuminated as shown in Figure 5-12.

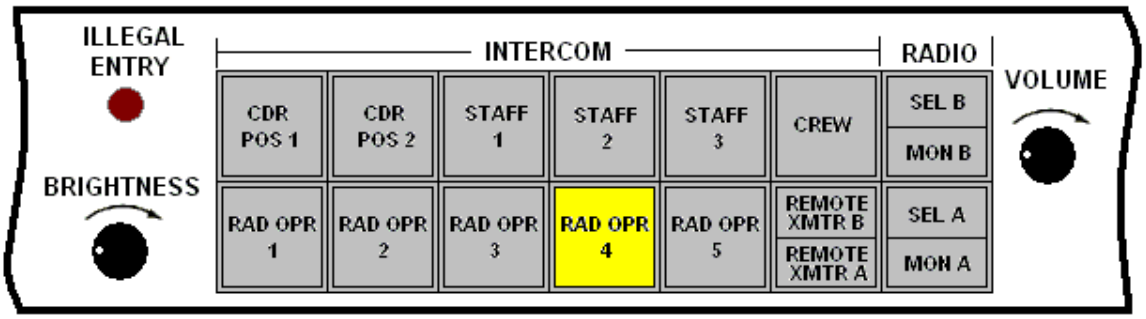
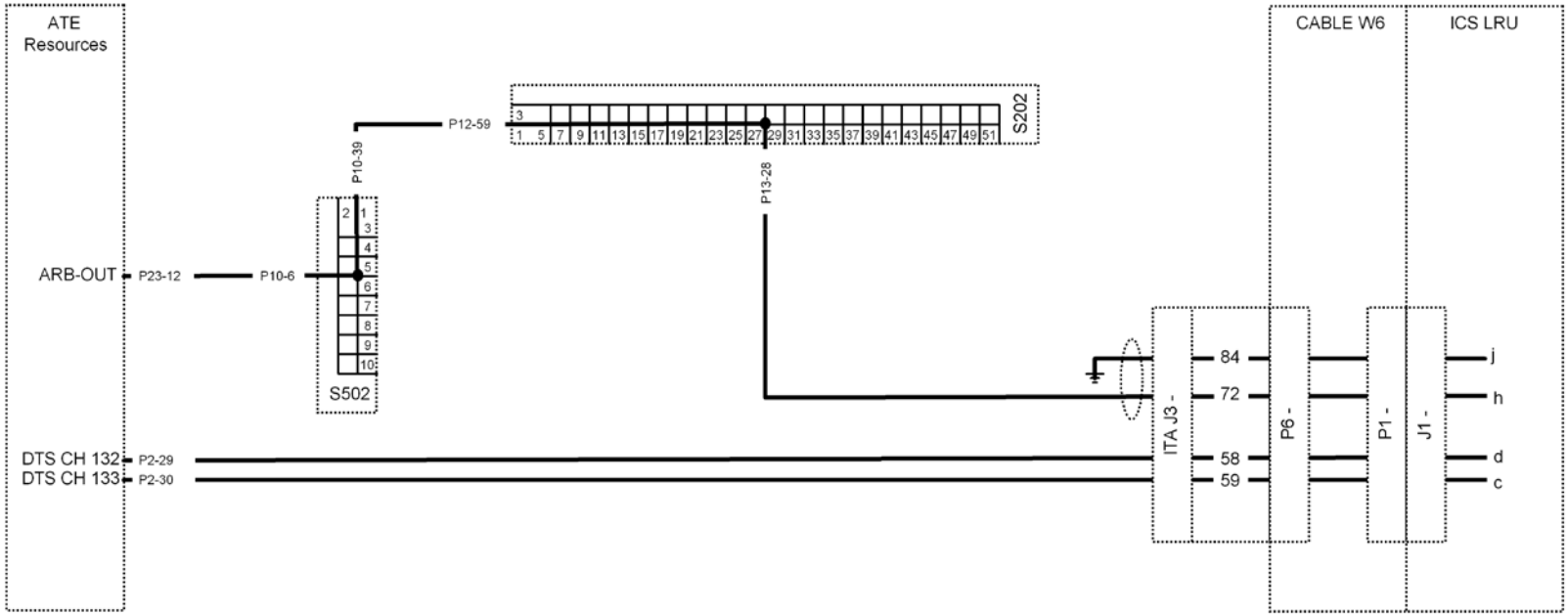


Figure 5-12

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'RAD OPR 4' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 213 'RAD OPR 5' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'RAD OPR 5' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'10001010010') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'RAD OPR 5' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'RAD OPR 5' lamp is illuminated as shown in Figure 5-13.

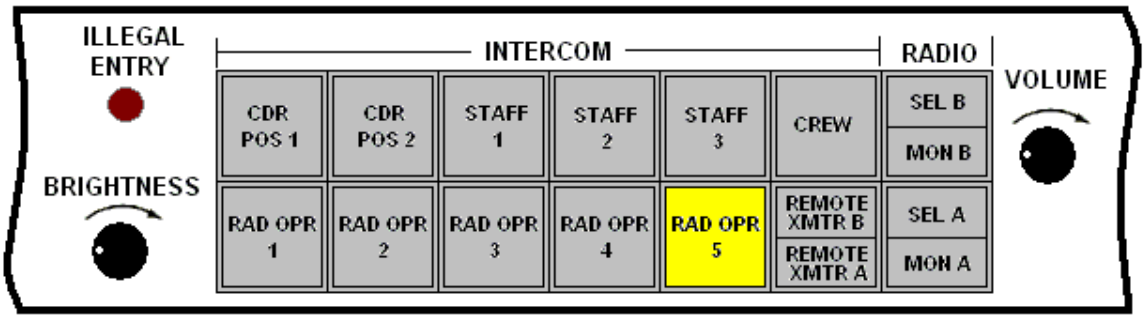
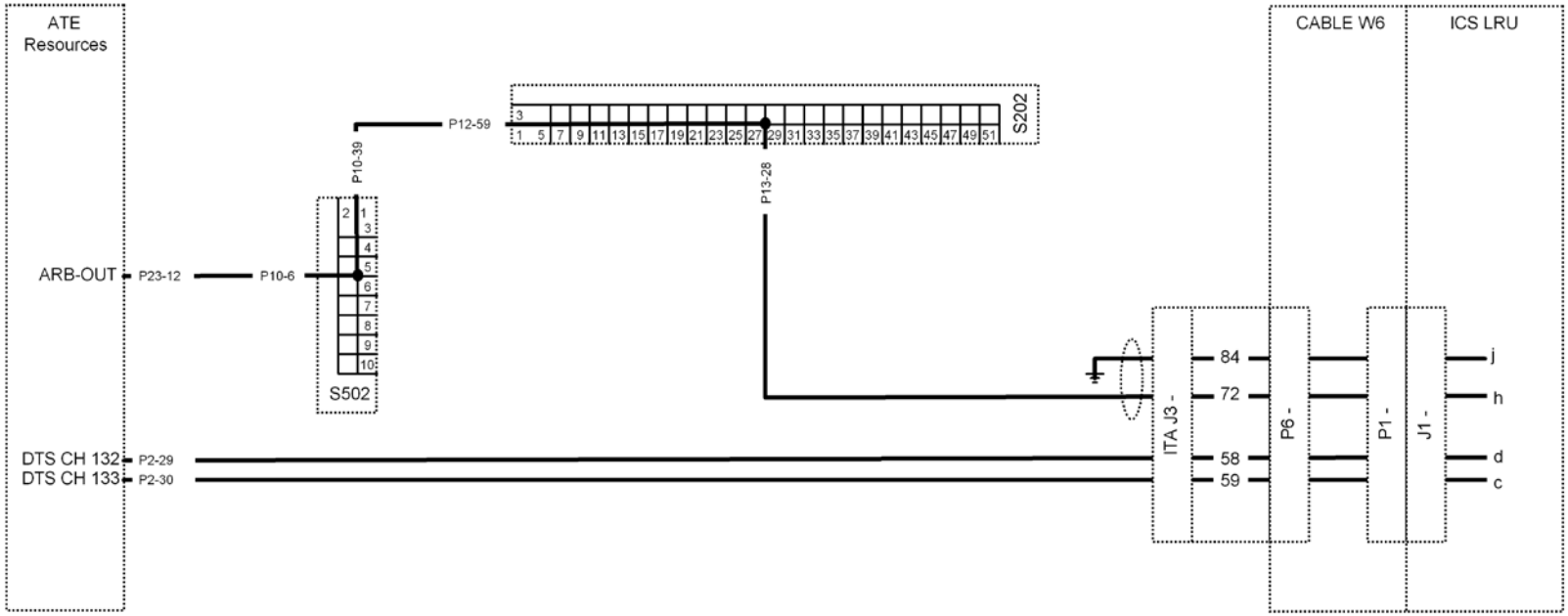


Figure 5-13

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'RAD OPR 5' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 214 'REMOTE XMTR B' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'REMOTE XMTR B' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'10001011110') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'REMOTE XMTR B' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'REMOTE XMTR B' lamp is illuminated as shown in Figure 5-14.

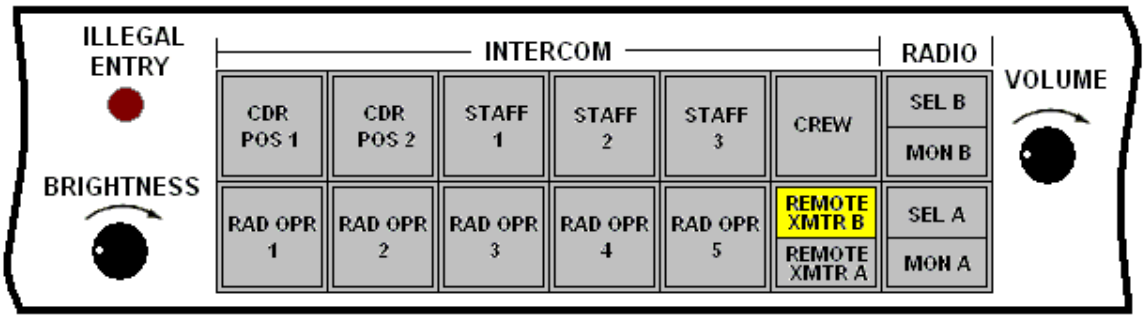
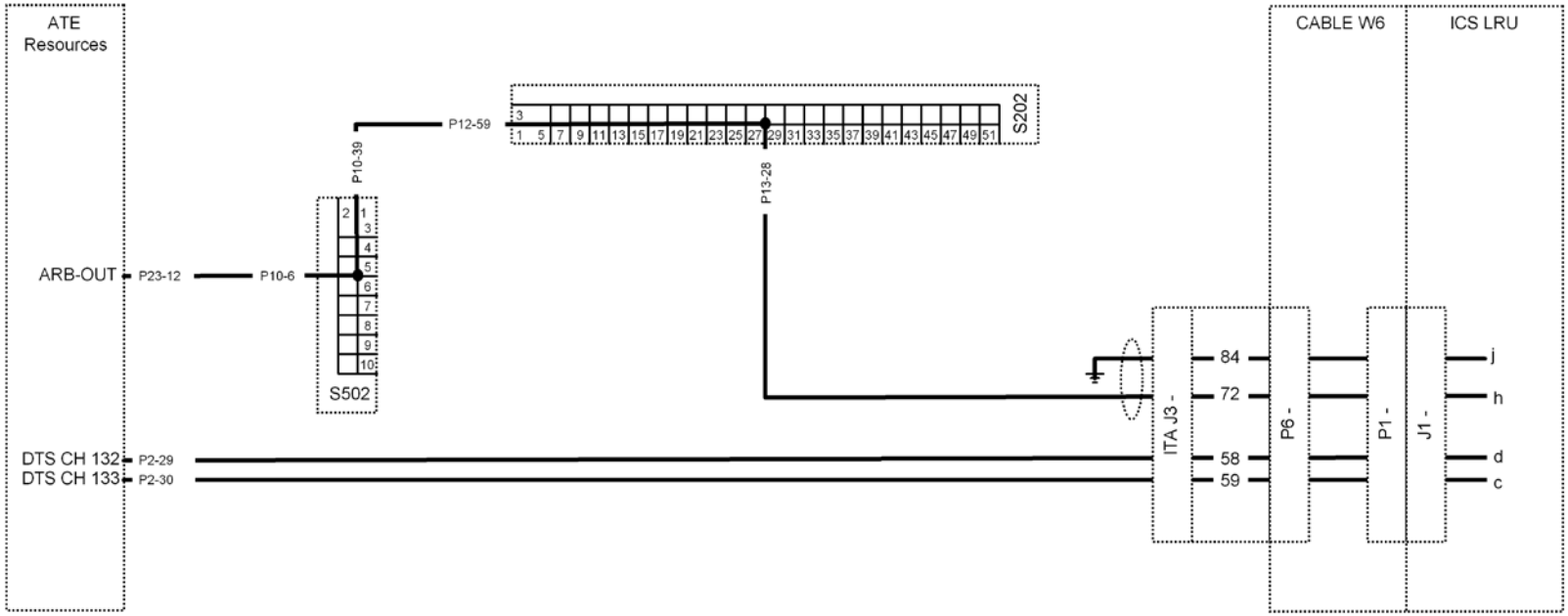


Figure 5-14

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'REMOTE XMTR B' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 215 'REMOTE XMTR A' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'REMOTE XMTR A' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'11001100000') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'REMOTE XMTR A' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'REMOTE XMTR A' lamp is illuminated as shown in Figure 5-15.

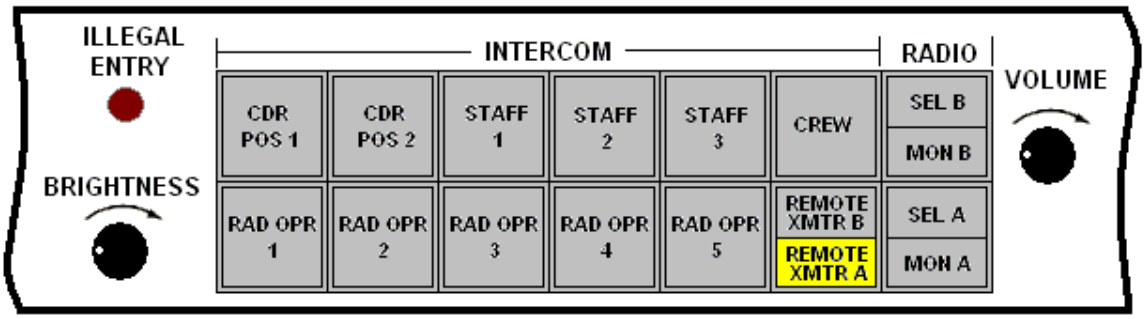
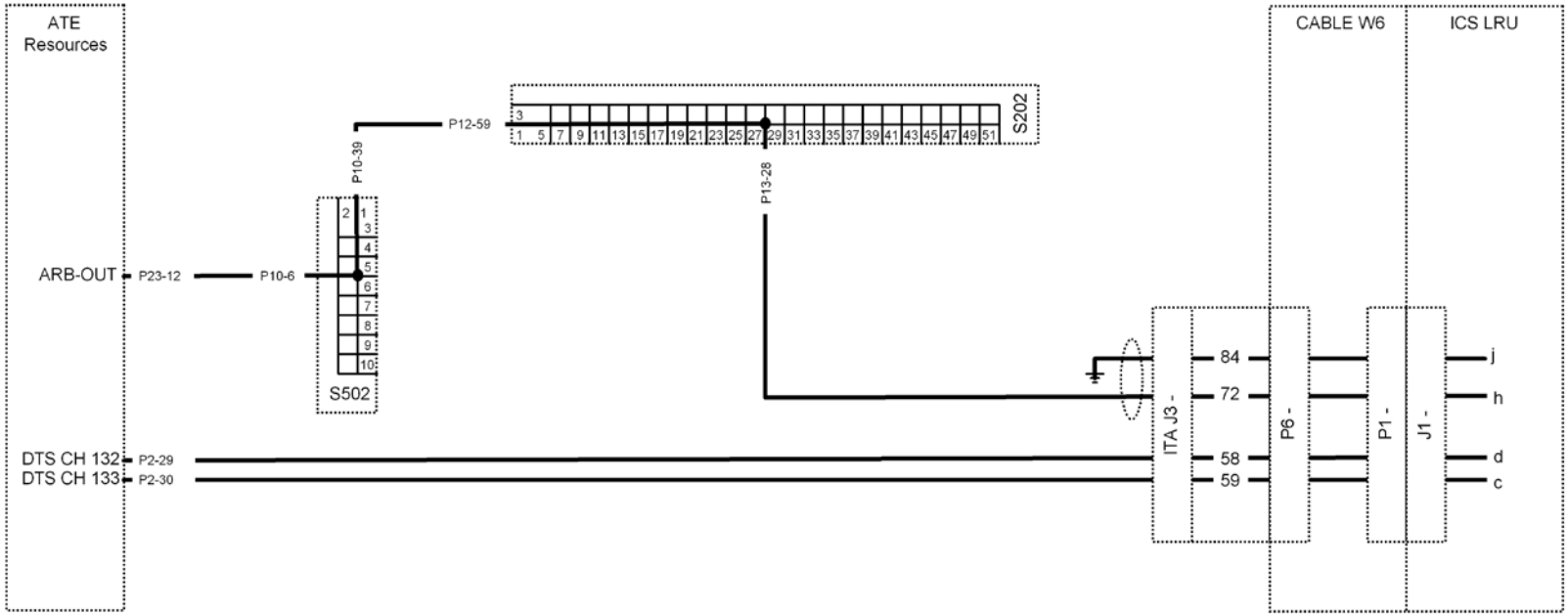


Figure 5-15

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'REMOTE XMTR A' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 216 'SEL A' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'SEL A' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'11001011010') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'SEL A' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'SEL A' lamp is illuminated as shown in Figure 5-16.

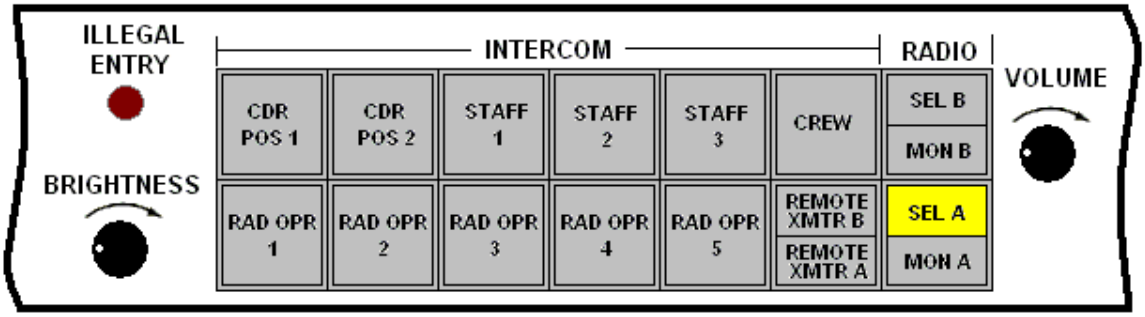
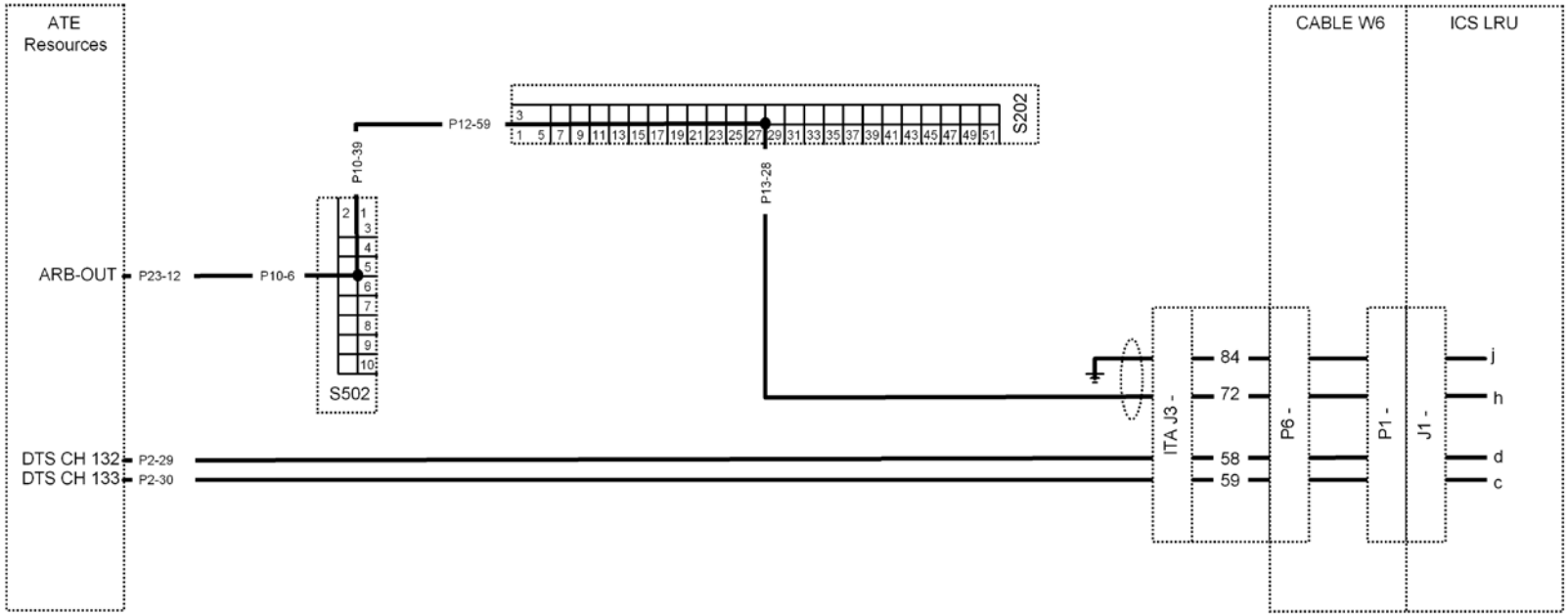


Figure 5-16

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'SEL A' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 217 'MON A' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'MON A' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'11001011100') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'MON A' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'MON A' lamp is illuminated as shown in Figure 5-17.

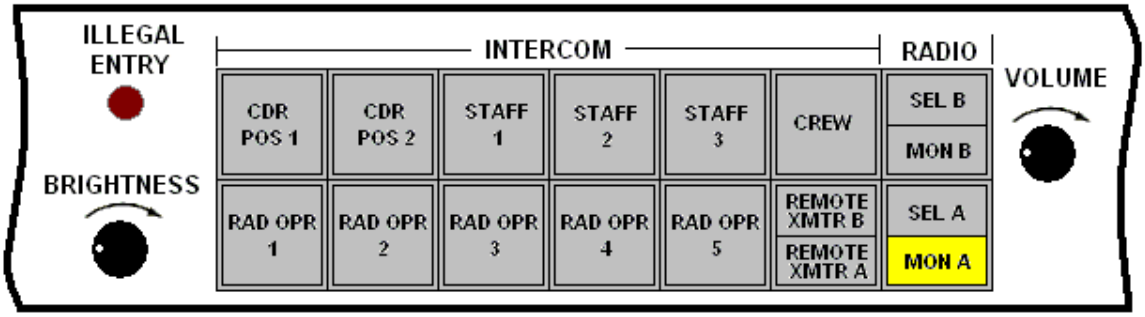
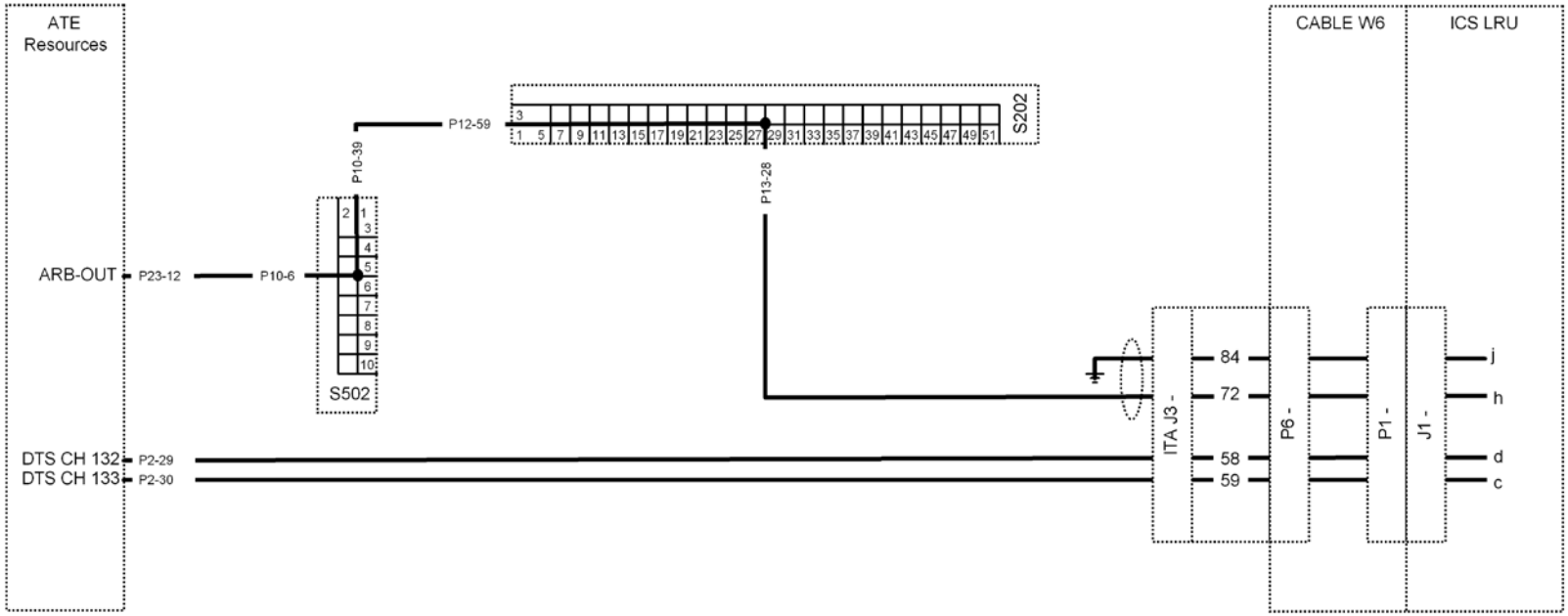


Figure 5-17

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'MON A' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c

Step 218 'ILLEGAL ENTRY' Lamp Operation Test

This test verifies functionality of the CCA A4 Decoder and Lamp Driver circuitry used to illuminate the front panel 'ILLEGAL ENTRY' indicator lamp. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command (B'10001100010') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'ILLEGAL ENTRY' lamp as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The operator is then prompted to verify that only the 'ILLEGAL ENTRY' lamp is illuminated as shown in Figure 5-18.

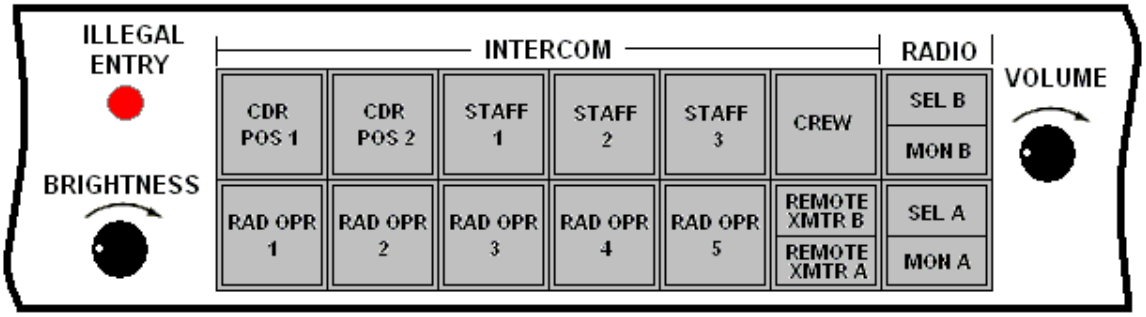
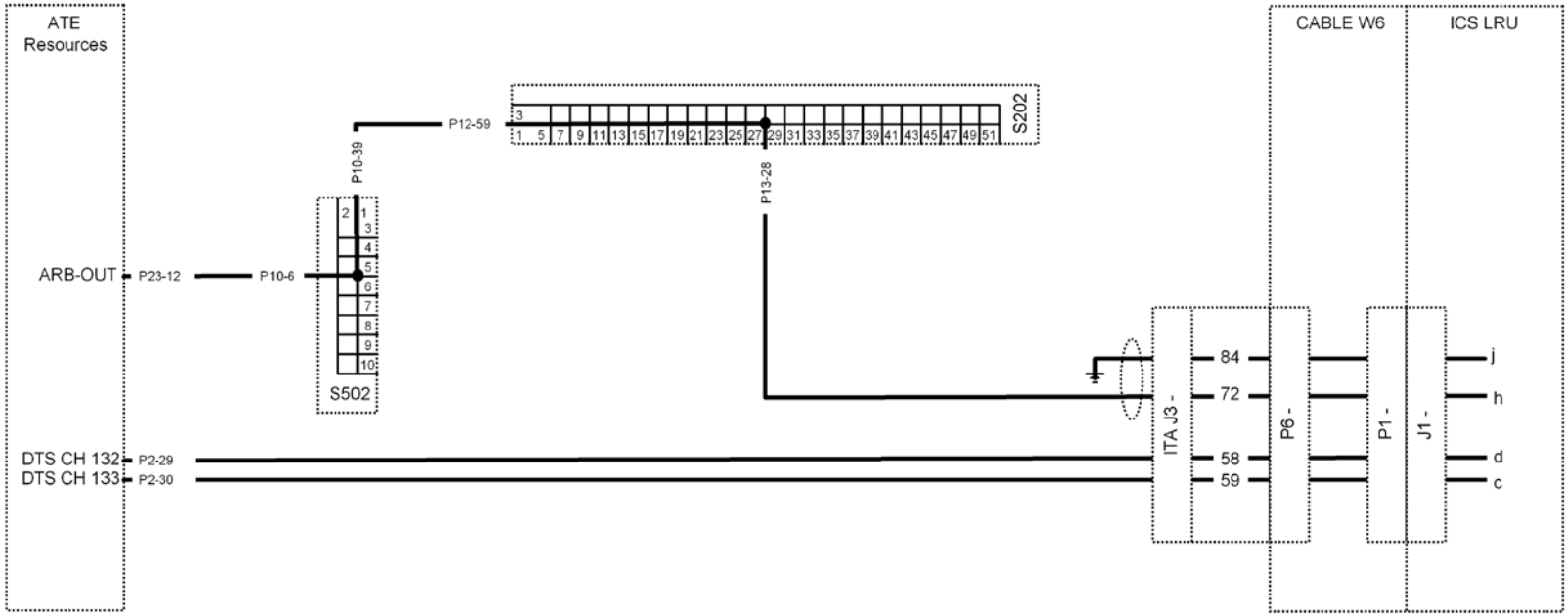


Figure 5-18

Following operator verification of the UUT front panel indication, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'ILLEGAL ENTRY' lamp (required by the next test).

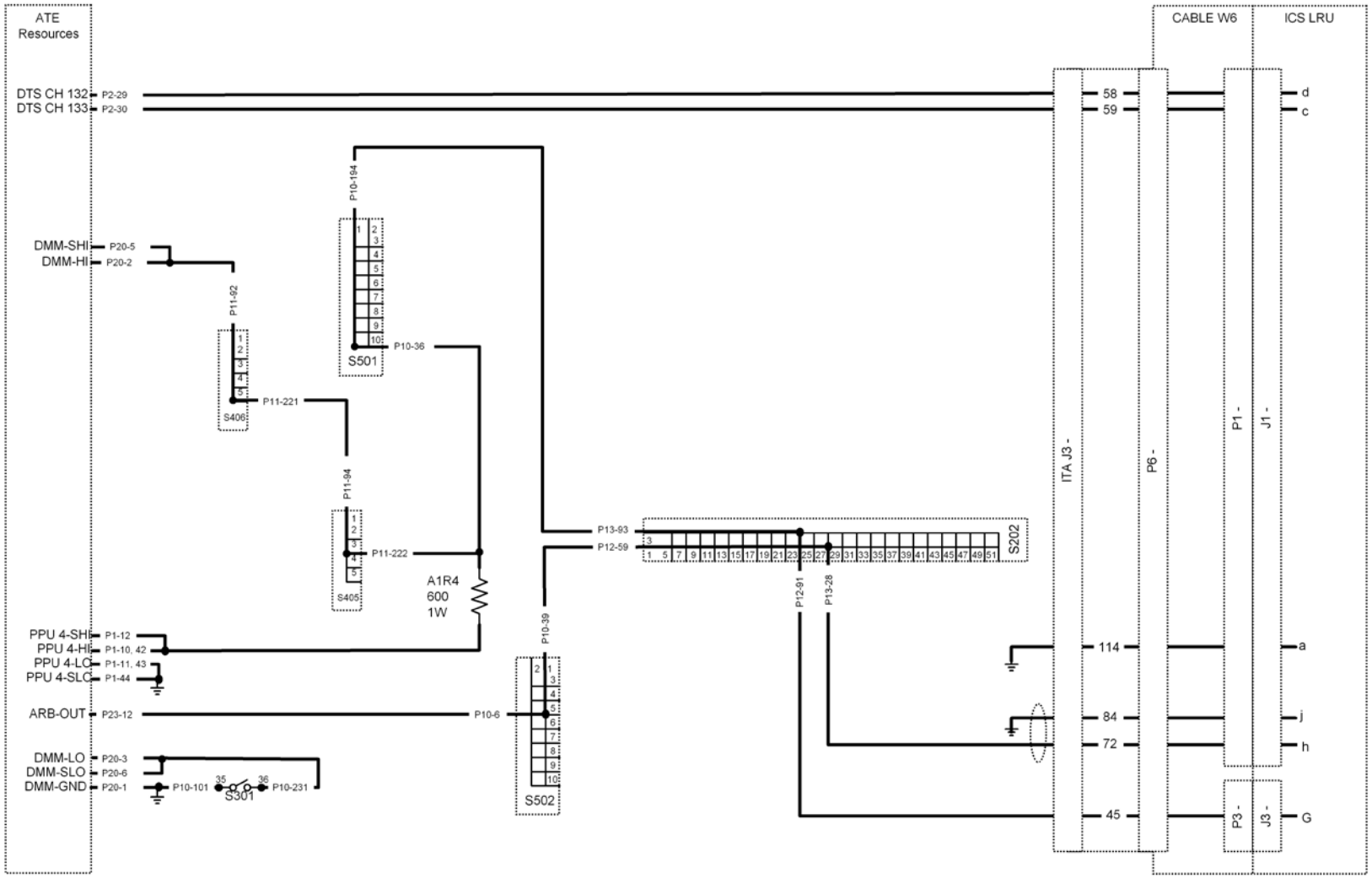
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
S202
P12-59
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
j
h
d
c
DTS CH 132
DTS CH 133
P2-29
P2-30

Step 219 K1 ('KEY A') Relay De-Energized Test

This step verifies that Keyline A relay, K1 contacts are not stuck in the closed position due to a faulty relay or decoder/driver logic on CCA A4. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h (see Step 201), the DTS is used to send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to place the A4 logic in a reset state. A 12V (100mA) 600 ohm 1 W pull-up is connected at J3-G using DCPS 4 thru ITA resistor 1A1R4. The DMM is used to verify nominally 12VDC (>11.5) at J3-G/GND, to verify that K1 contacts are de-energized (open).

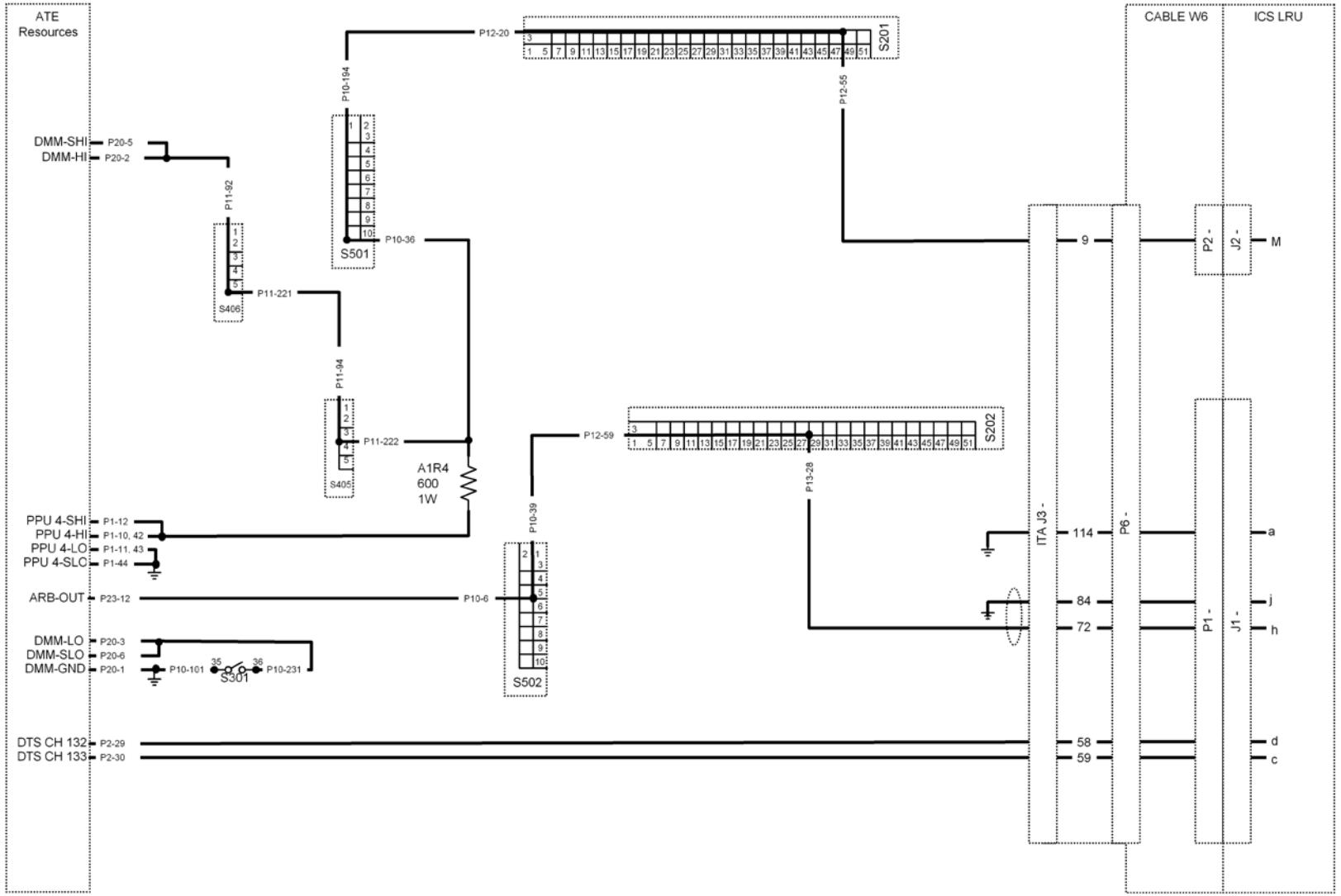
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
DTS CH 132 P2-29
DTS CH 133 P2-30
DMM-SHI P20-5
DMM-HI P20-2
P11-92
S406
P11-221
P10-164
S501
P10-36
P11-94
S405
P11-222
A1R4
600
1W
P13-93
P12-59
S202
P12-91
P13-28
ITA J3 -
P6 -
P1 -
J1 -
58
59
d
c
PPU 4-SHI P1-12
PPU 4-HI P1-10, 42
PPU 4-LO P1-11, 43
PPU 4-SLO P1-44
ARB-OUT P23-12
P10-6
P10-39
S502
DMM-LO P20-3
DMM-SLO P20-6
DMM-GND P20-1
P10-101
S301
P10-231
114
84
72
45
a
j
h
G
P3 -
J3 -

Step 220 K2 ('KEY B') Relay De-Energized Test

This step verifies that Keyline B relay, K2 contacts are not stuck in the closed position due to a faulty relay or decoder/driver logic on CCA A4. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h (see Step 201), and a 12V (100mA) 600 ohm 1 W pull-up connected at J2-M using DCPS 4 thru ITA resistor 1A1R4, the DMM is used to verify nominally 12VDC (>11.5) at J2-M/GND, to verify that K2 contacts are de-energized (open).

Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
DMM-SHI P20-5
DMM-HI P20-2
PPU 4-SHI P1-12
PPU 4-HI P1-10, 42
PPU 4-LO P1-11, 43
PPU 4-SLC P1-44
ARB-OUT P23-12
DMM-LO P20-3
DMM-SLO P20-6
DMM-GND P20-1
DTS CH 132 P2-29
DTS CH 133 P2-30
P10-194
P12-20
S201
P12-55
P11-92
S406
P11-221
P11-94
S405
P11-222
P10-36
S501
A1R4
600
1W
P12-59
S202
P13-28
P10-39
S502
P10-6
P10-101
S301
P10-231
ITA J3 -
9
114
84
72
58
59
P6 -
P2 -
J2 -
M
P1 -
J1 -
a
j
h
d
c

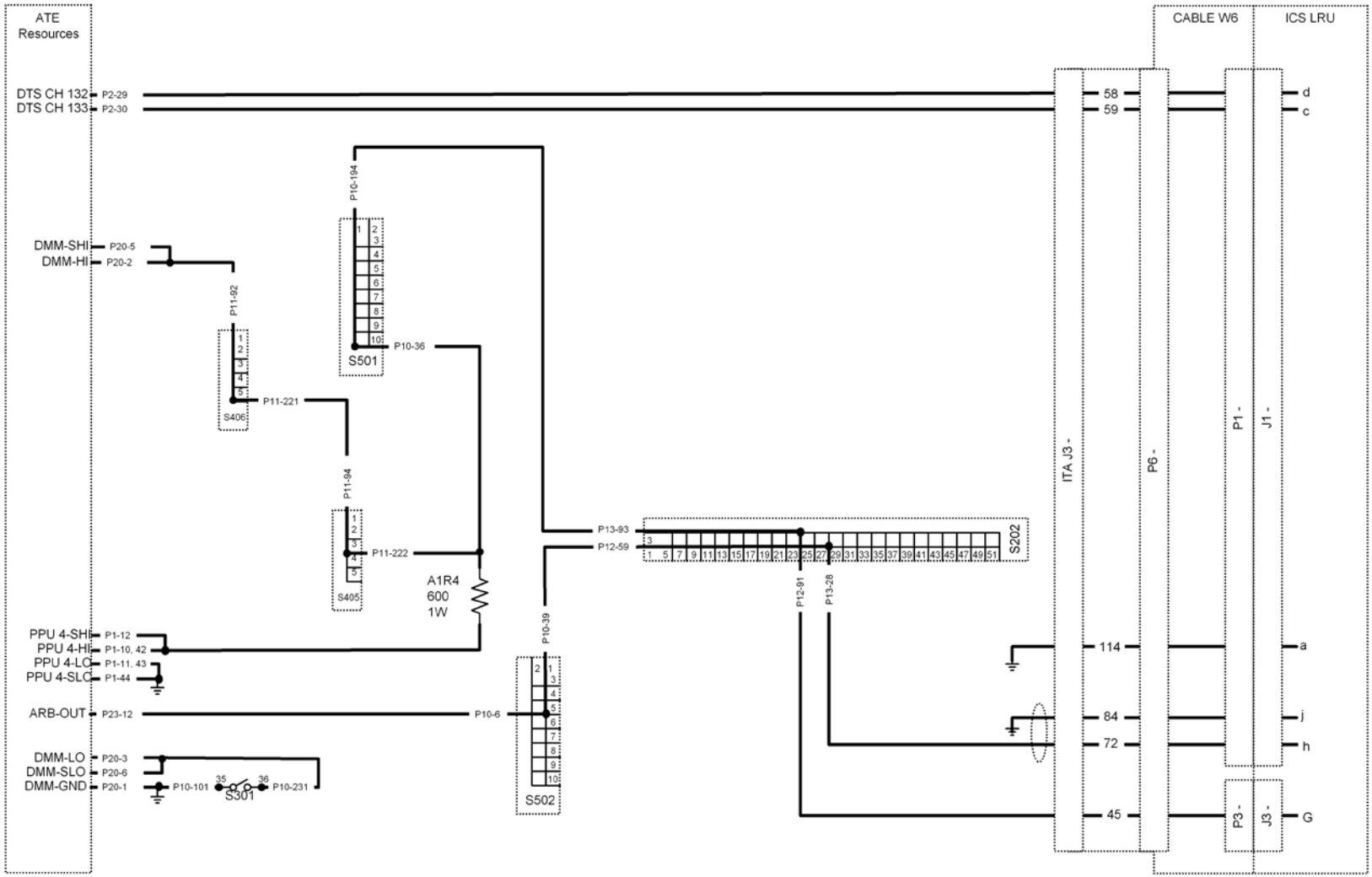
Step 221 K1 ('KEY A') Relay Energized Test

This test verifies functionality of the CCA A4 Decoder and Relay Driver circuitry used to energize K1. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h (see Step 201), and a 12V 600 ohm 1 W pull-up connected at J3-G (see Step 219), the DMM is used to verify nominally 0VDC (<0.5VDC) at J3-G/GND, to verify that K1 contacts are energized (closed) in response to a differential serial data command from the DTS at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'KEY A' command (B' 10001100100') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to causing K1 to energize as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
DTS CH 132 P2-29
DTS CH 133 P2-30
DMM-SHI P20-5
DMM-HI P20-2
P11-92
S406
P11-221
P11-94
S405
P11-222
P10-194
S501
P10-36
A1R4
600
1W
P13-93
P12-59
S202
P12-91
P13-28
P10-39
S502
PPU 4-SHI P1-12
PPU 4-HI P1-10, 42
PPU 4-LO P1-11, 43
PPU 4-SLO P1-44
ARB-OUT P23-12
P10-6
DMM-LO P20-3
DMM-SLO P20-6
DMM-GND P20-1
P10-101
S301
P10-231
ITA J3 -
P6 -
P1 -
J1 -
P3 -
J3 -
58
59
114
84
72
45
d
c
a
j
h
G

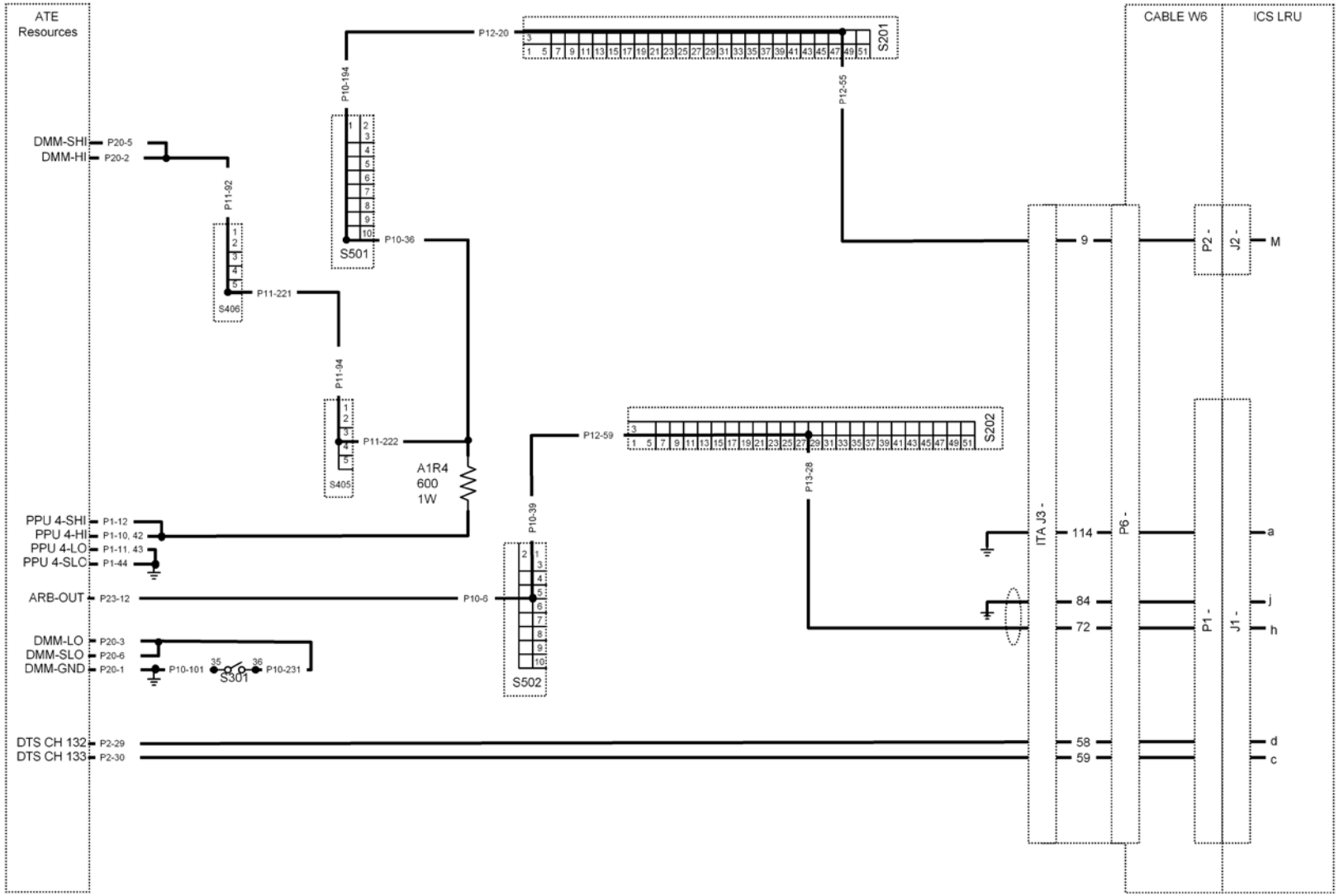
Step 222 K2 ('KEY B') Relay Energized Test

This test verifies functionality of the CCA A4 Decoder and Relay Driver circuitry used to energize K2. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h (see Step 201) the DTS is used to send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to place the A4 logic in a reset state.. A 12V 600 ohm 1 W pull-up is connected at J2-M (see Step 219). The DMM is used to verify nominally 0VDC (<0.5VDC) at J2-M/GND, to verify that K2 contacts are energized (closed) in response to a differential serial data command from the DTS at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'KEY B' command (B'11001100110') at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to causing K2 to energize as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'10' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

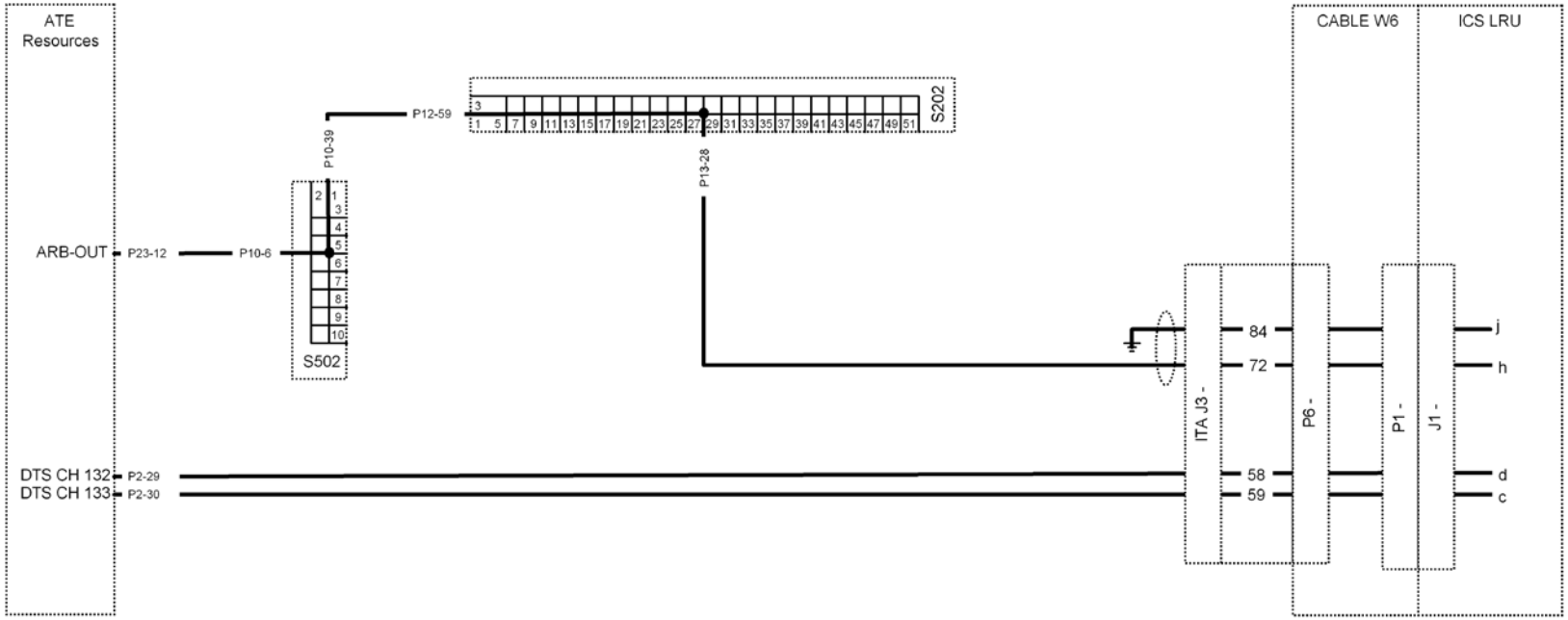
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
DMM-SHI P20-5
DMM-HI P20-2
DMM-LO P20-3
DMM-SLO P20-6
DMM-GND P20-1
PPU 4-SHI P1-12
PPU 4-HI P1-10, 42
PPU 4-LO P1-11, 43
PPU 4-SLO P1-44
ARB-OUT P23-12
DTS CH 132 P2-29
DTS CH 133 P2-30
P10-194
P10-36
P10-39
P10-6
P10-101
P10-231
P11-92
P11-221
P11-94
P11-222
P12-20
P12-55
P12-59
P13-28
S201
S202
S501
S502
S301
S406
S405
A1R4
600
1W
ITA J3 -
P6 -
P2 -
J2 -
P1 -
J1 -
9
114
84
72
58
59
M
a
j
h
d
c

Step 223 'BRIGHTNESS' Control Test

This step verifies the lamp dimmer circuitry on CCA A5, Q1 and the front panel BRIGHTNESS control, R2. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h (see Step 201), the DTS is used to output a series of differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate each the front panel Switch/Indicator lamps previously verified (see Step 201-217). The operator is then prompted to rotate the front panel BRIGHTNESS control from fully CW to fully CCW and verify that the display goes from fully ON to OFF or very dim.

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
84
72
j
h
DTS CH 132
DTS CH 133
P2-29
P2-30
58
59
d
c

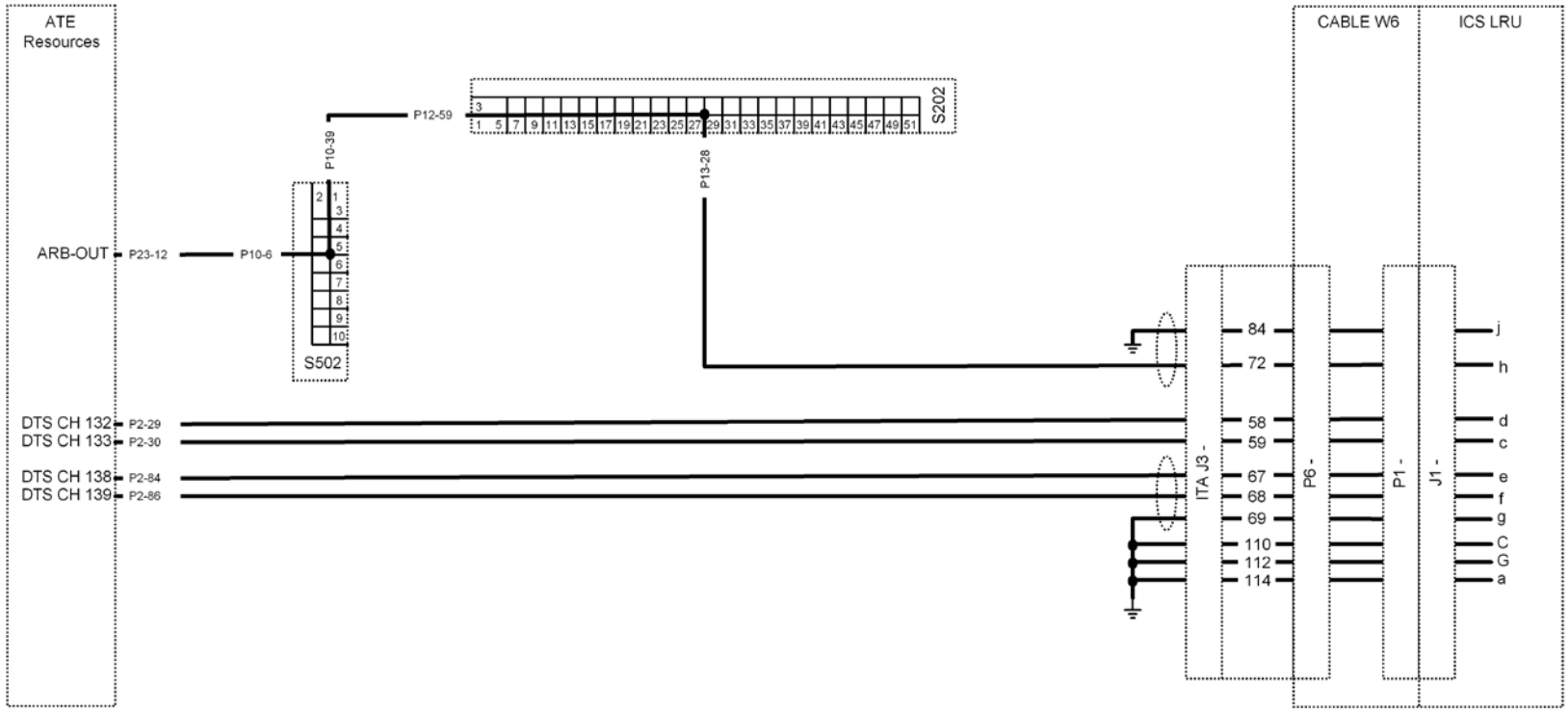
MODULE 3 SWITCH/ENCODER TESTS

Module 3 verifies that each front panel station call switch operates as well as the functionality of the encoder logic on CCA A4. The switch being tested is illuminated and the operator is then prompted to momentarily depress the switch. The transmitted serial data stream is verified to contain the correct switch address for the one being tested.

Step 301 'CDR POS 1' Switch Operation Test

This step verifies that depressing the front panel 'CDR POS 1' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'CDR POS 1' lamp (see Step 201) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'CDR POS 1' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B’0’ / J1-f[-] = B’1’) in response to the switch push, signifying a 'Request-For-Attention' generation.

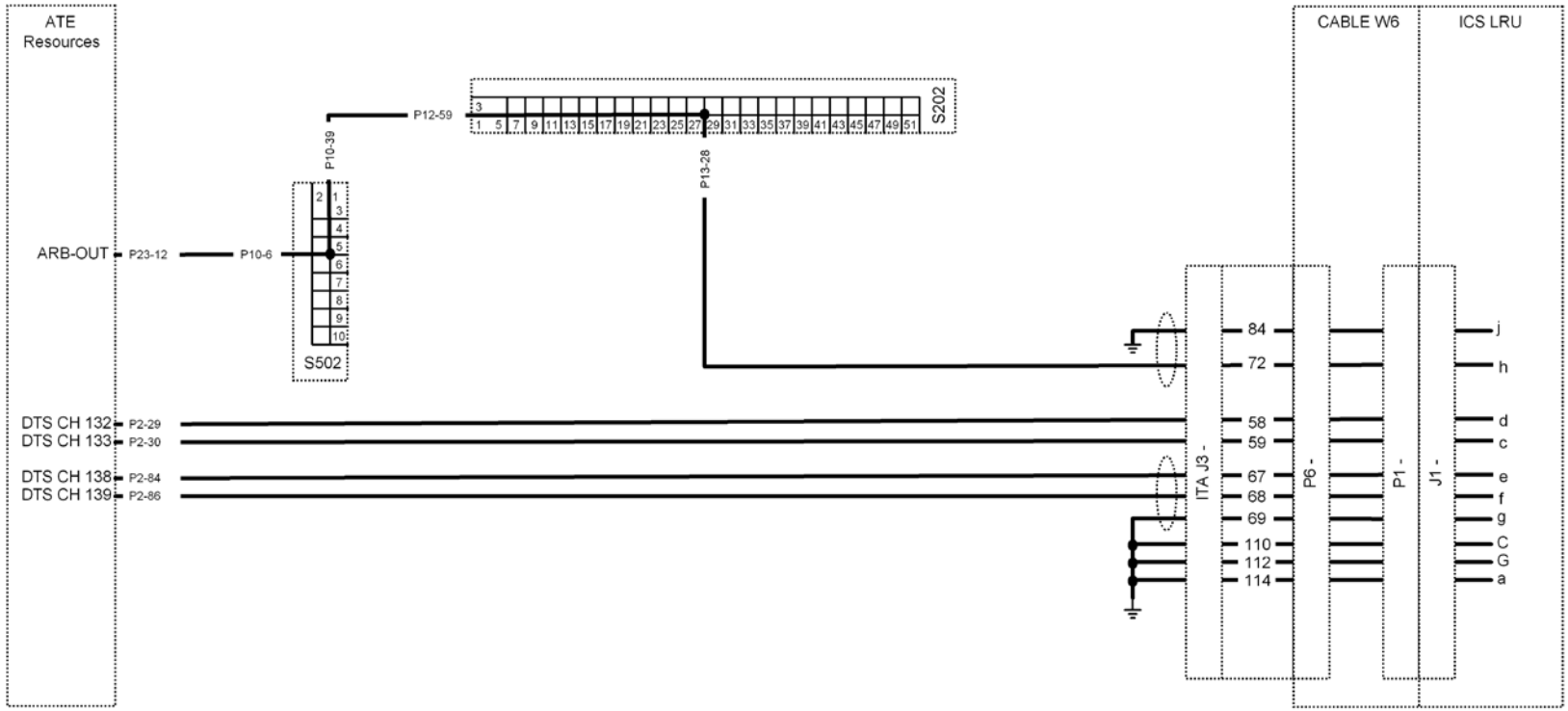
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 302 'CDR POS 1' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'CDR POS 1' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file CDR-POS1.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'CDR POS 1' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'CDR POS 1' lamp (required by the next test).

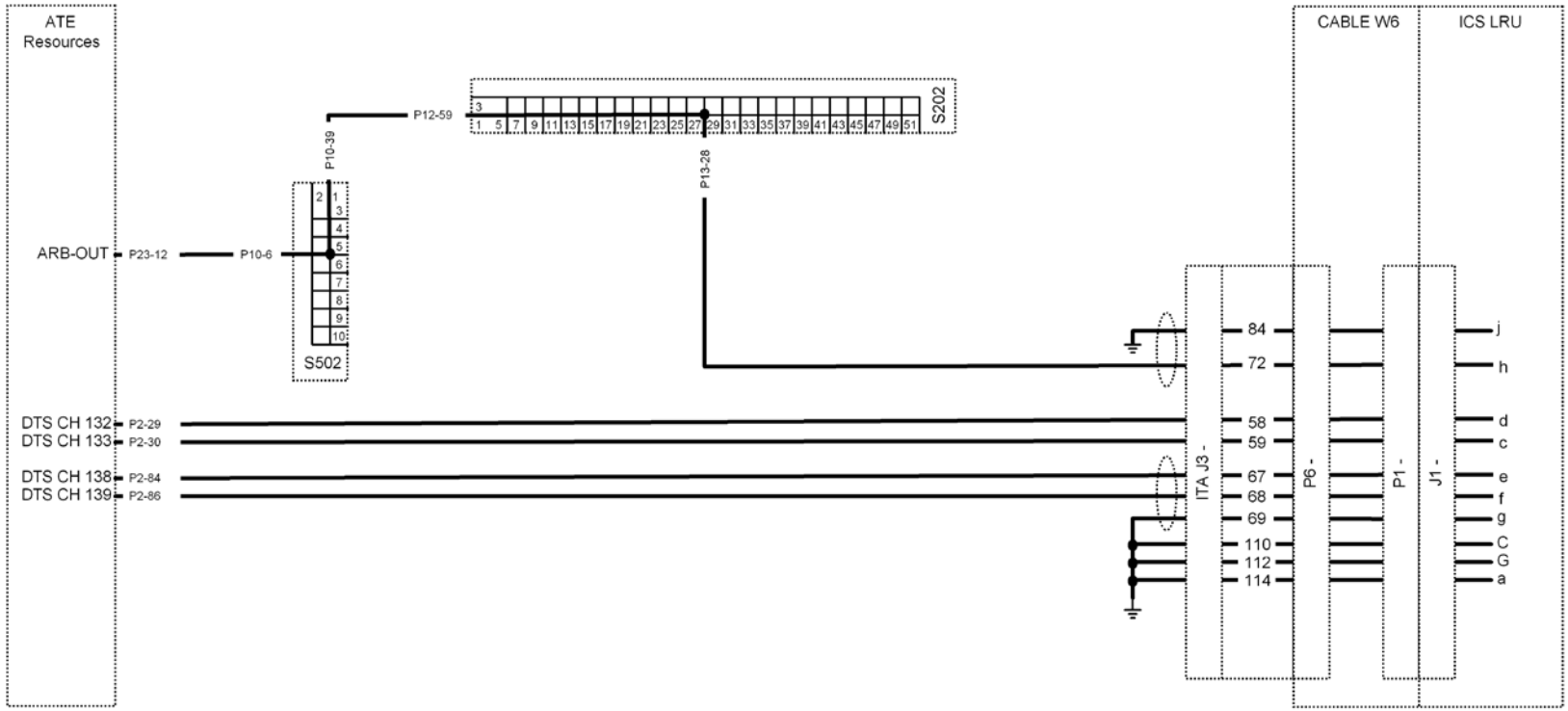
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
P10-39
S202
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 303 'CDR POS 2' Switch Operation Test

This step verifies that depressing the front panel 'CDR POS 2' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'CDR POS 2' lamp (see Step 202) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'CDR POS 2' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B’0’ / J1-f[-] = B’1’) in response to the switch push, signifying a 'Request-For-Attention' generation.

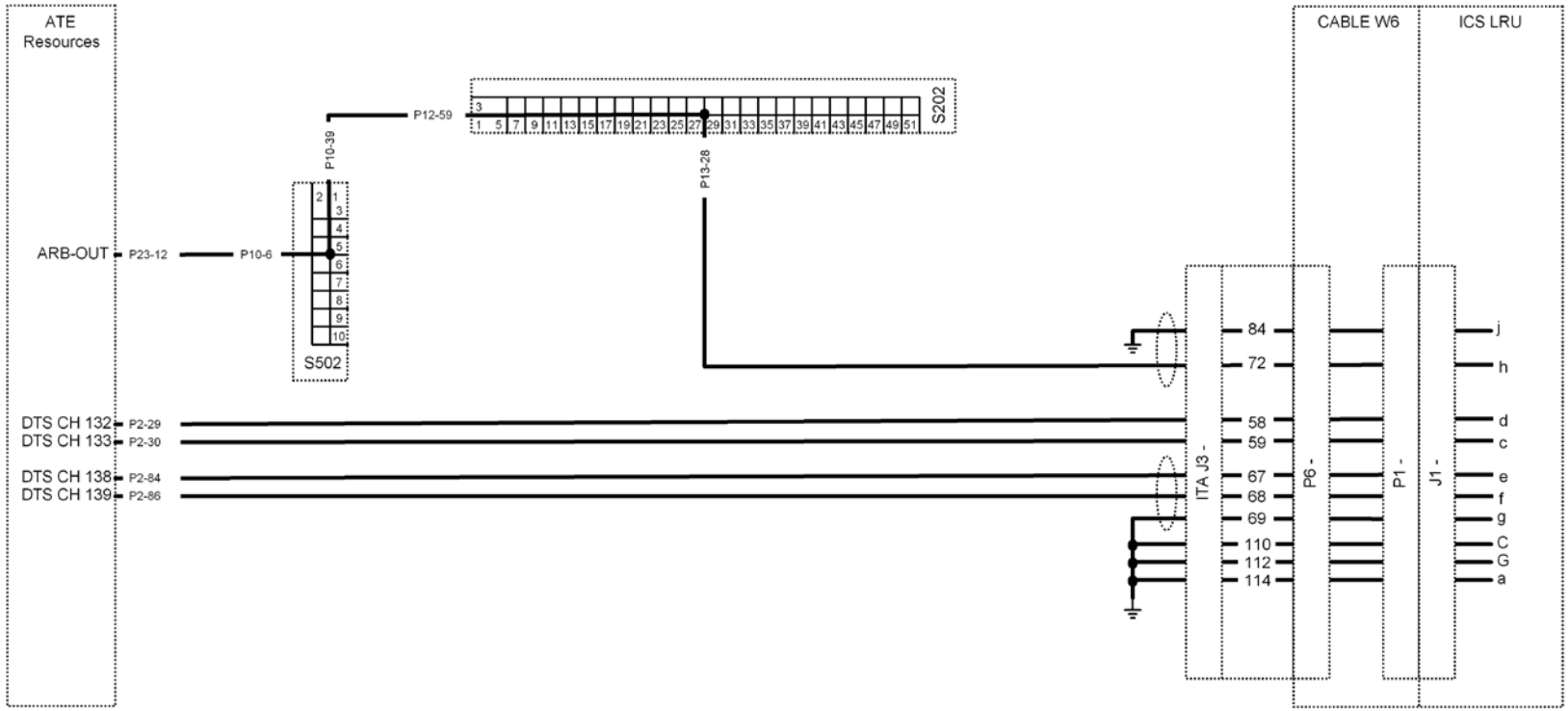
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 304 'CDR POS 2' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'CDR POS 2' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file CDR-POS2.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'CDR POS 2' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'CDR POS 2' lamp (required by the next test).

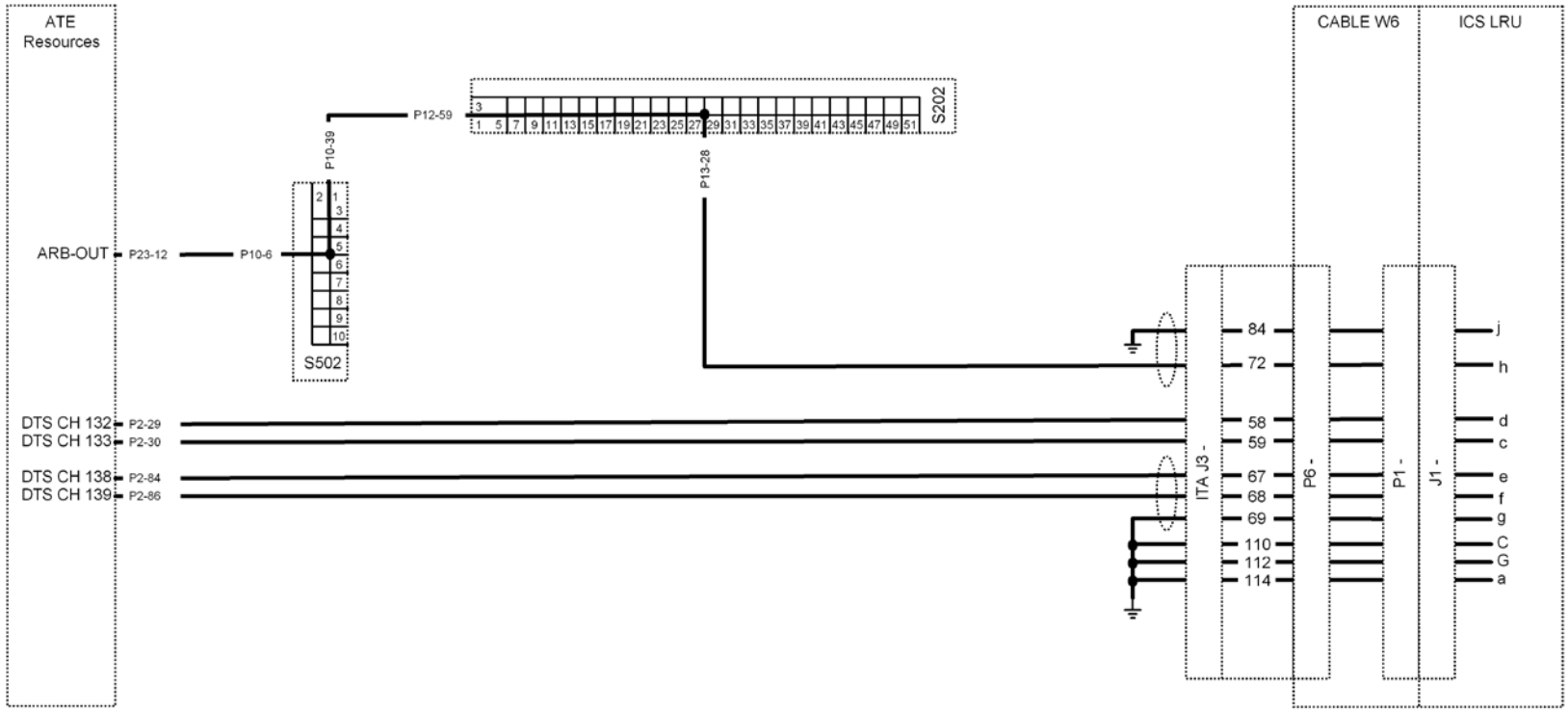
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 305 'STAFF 1' Switch Operation Test

This step verifies that depressing the front panel 'STAFF 1' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'STAFF 1' lamp (see Step 203) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'STAFF 1' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B'0' / J1-f[-] = B'1') in response to the switch push, signifying a 'Request-For-Attention' generation.

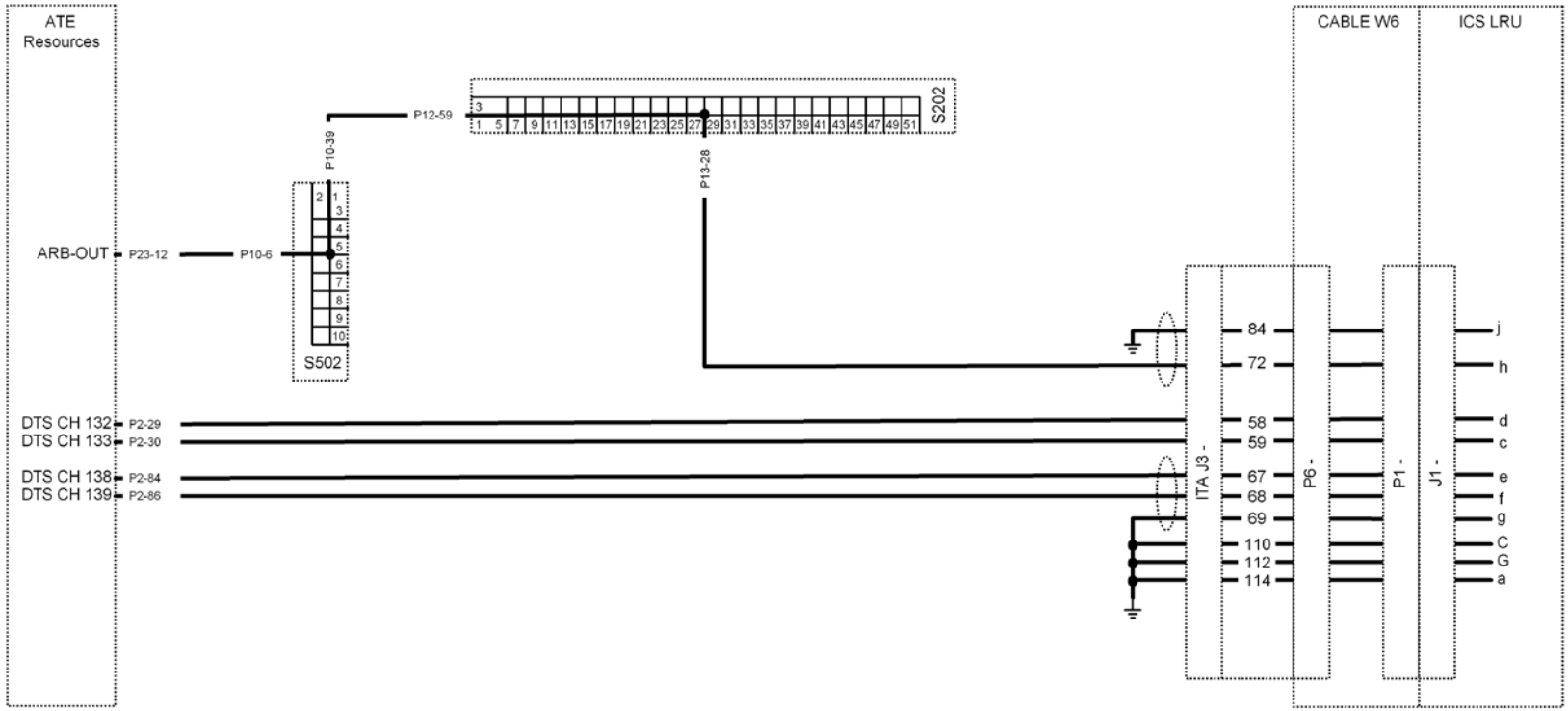
Connection Path as follows:


ATE
Resources
ARB-OUT
P23-12
P10-6
P10-39
P12-59
P13-28
S202
S502
DTS CH 132
DTS CH 133
DTS CH 138
DTS CH 139
P2-29
P2-30
P2-84
P2-86
CABLE W6
ICS LRU
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 306 'STAFF 1' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'STAFF 1' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file STAFF-1.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'STAFF 1' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'STAFF 1' lamp (required by the next test).

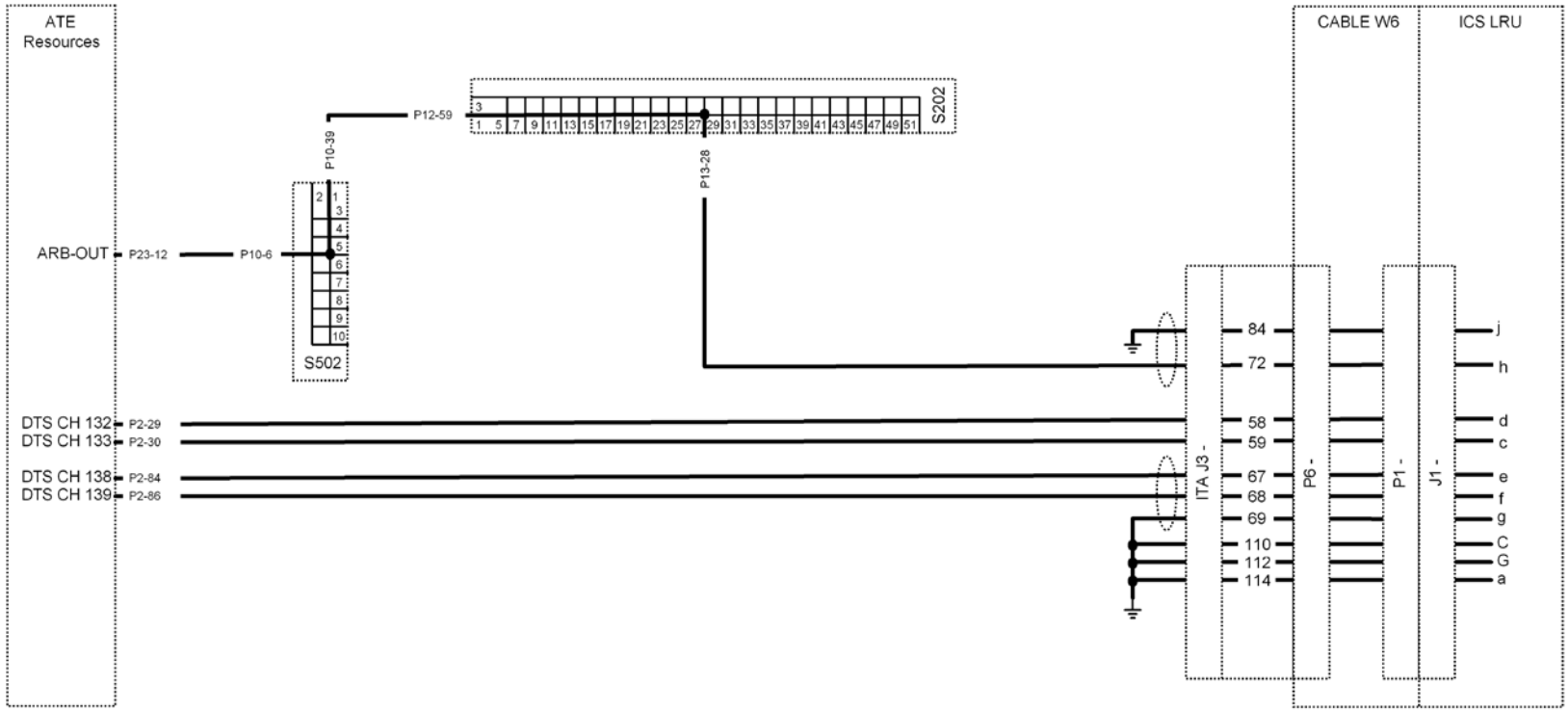
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 307 'STAFF 2' Switch Operation Test

This step verifies that depressing the front panel 'STAFF 2' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'STAFF 2' lamp (see Step 204) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'STAFF 2' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B'0' / J1-f[-] = B'1') in response to the switch push, signifying a 'Request-For-Attention' generation.

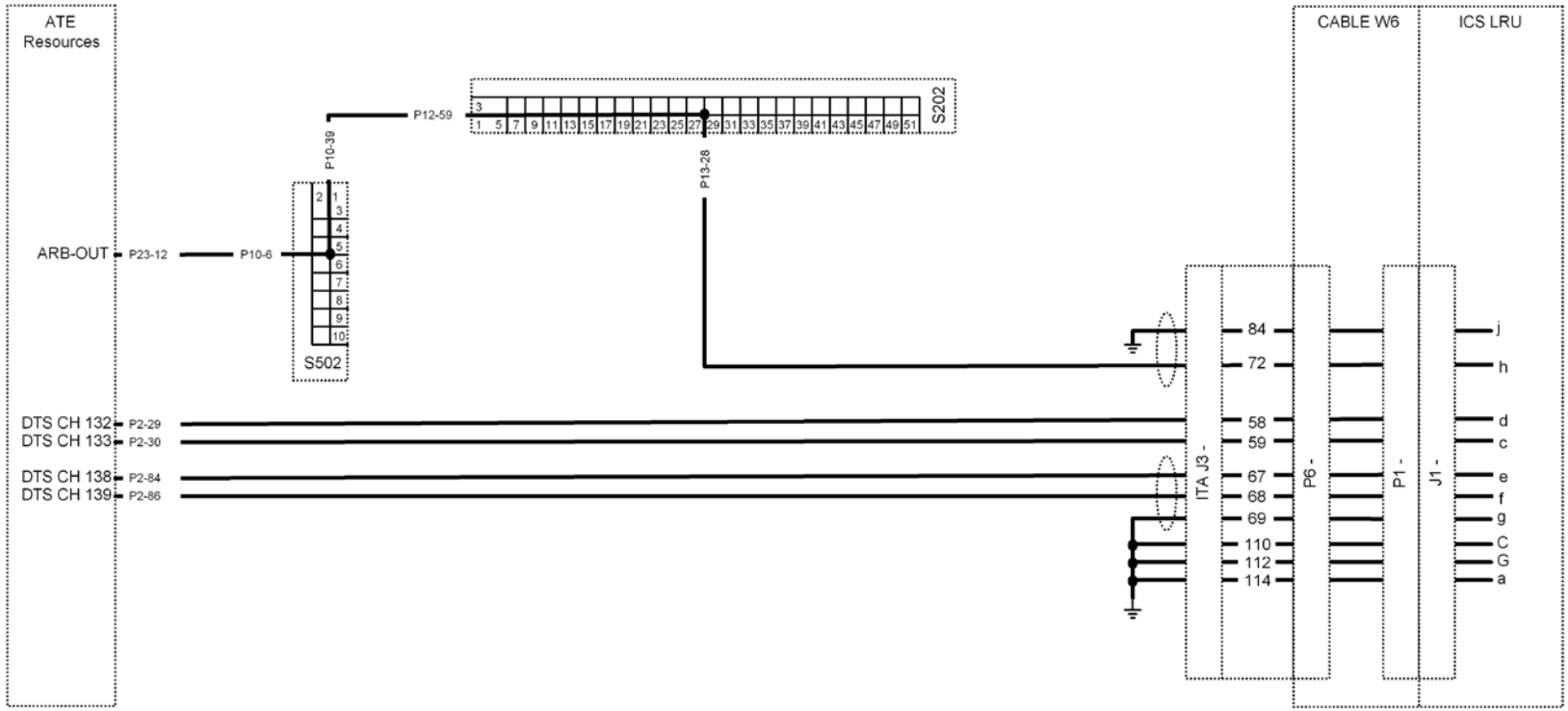
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 308 'STAFF 2' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'STAFF 2' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file STAFF-2.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'STAFF 2' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'STAFF 2' lamp (required by the next test).

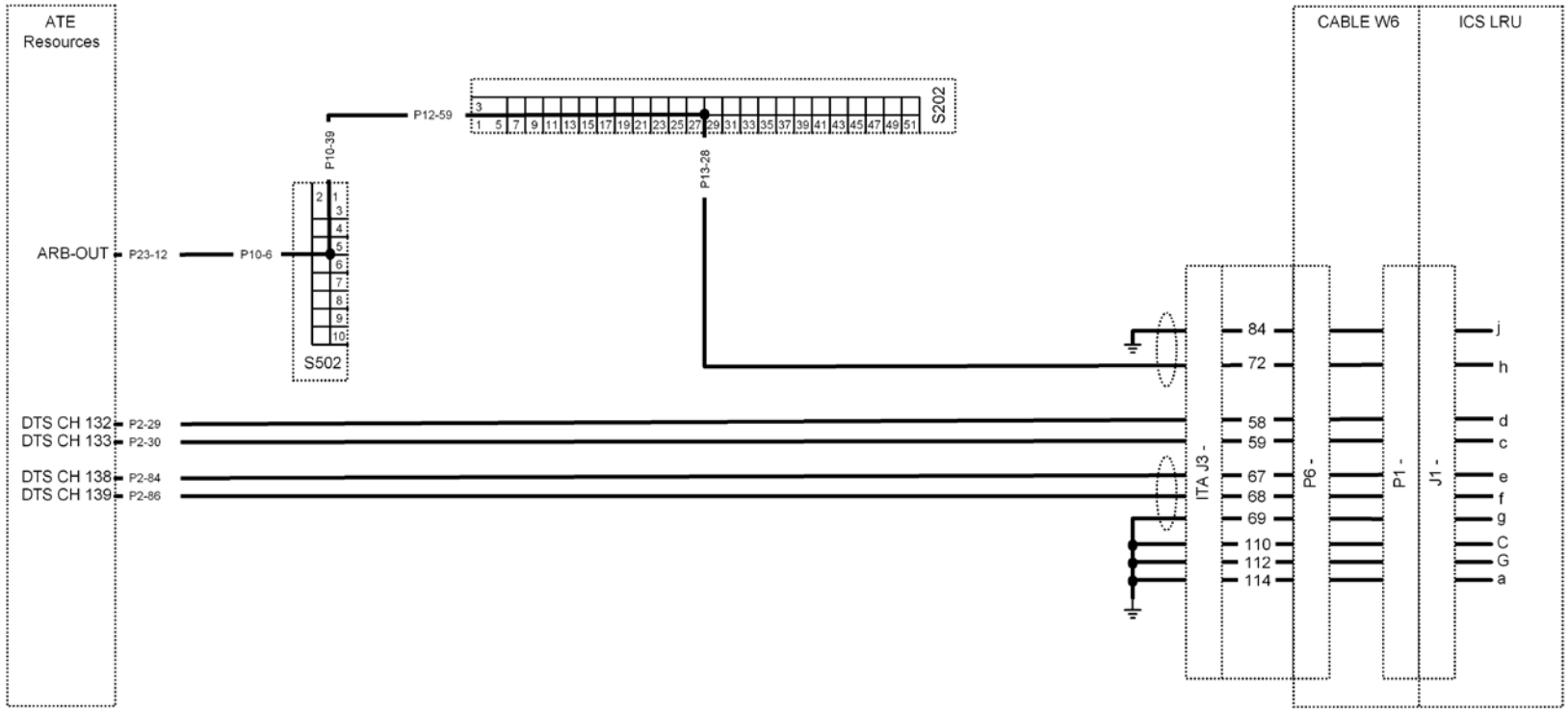
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 309 'STAFF 3' Switch Operation Test

This step verifies that depressing the front panel 'STAFF 3' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'STAFF 3' lamp (see Step 205) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'STAFF 3' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B'0' / J1-f[-] = B'1') in response to the switch push, signifying a 'Request-For-Attention' generation.

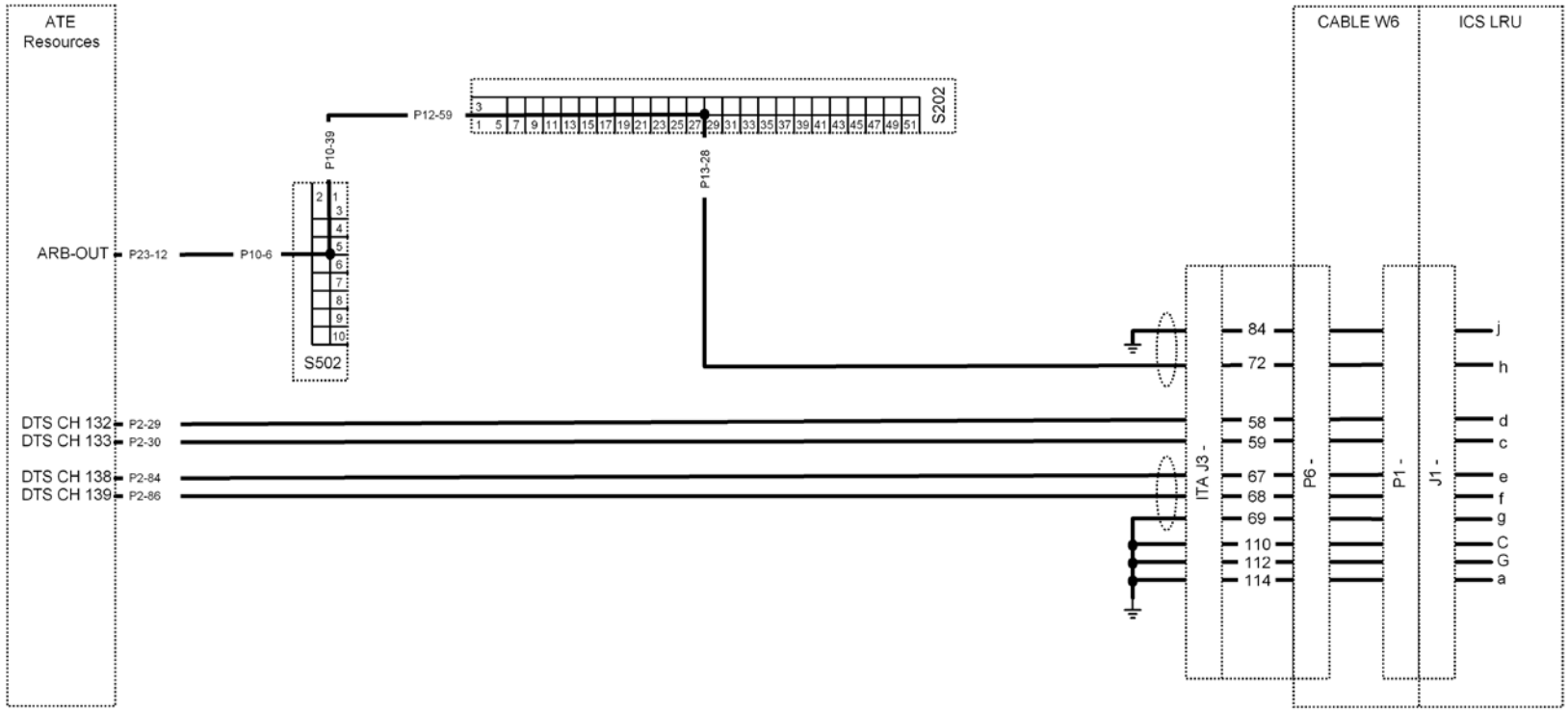
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 310 'STAFF 3' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'STAFF 3' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file STAFF-3.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'STAFF 3' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'STAFF 3' lamp (required by the next test).

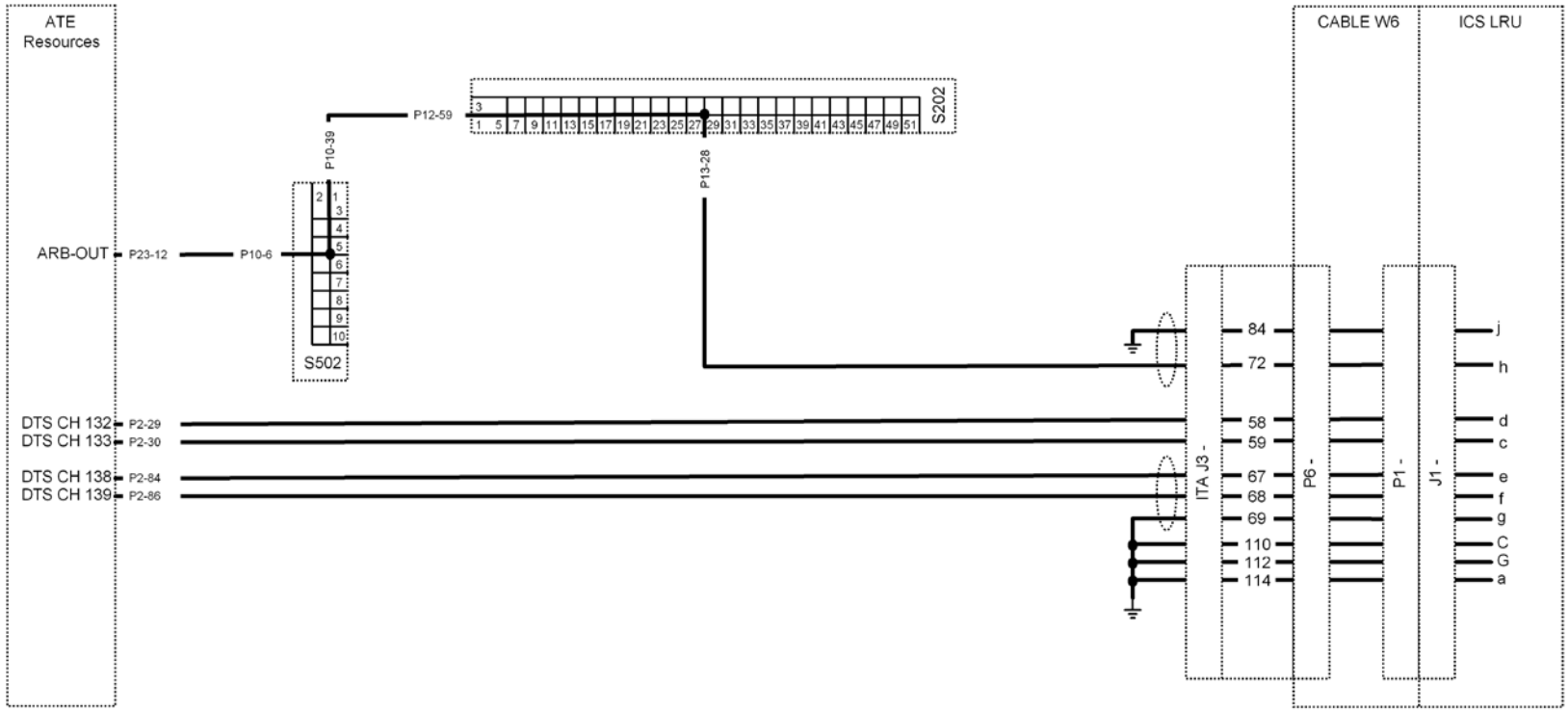
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P12-59
P10-39
S202
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 311 'CREW' Switch Operation Test

This step verifies that depressing the front panel 'CREW' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'CREW' lamp (see Step 206) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'CREW' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B'0' / J1-f[-] = B'1') in response to the switch push, signifying a 'Request-For-Attention' generation.

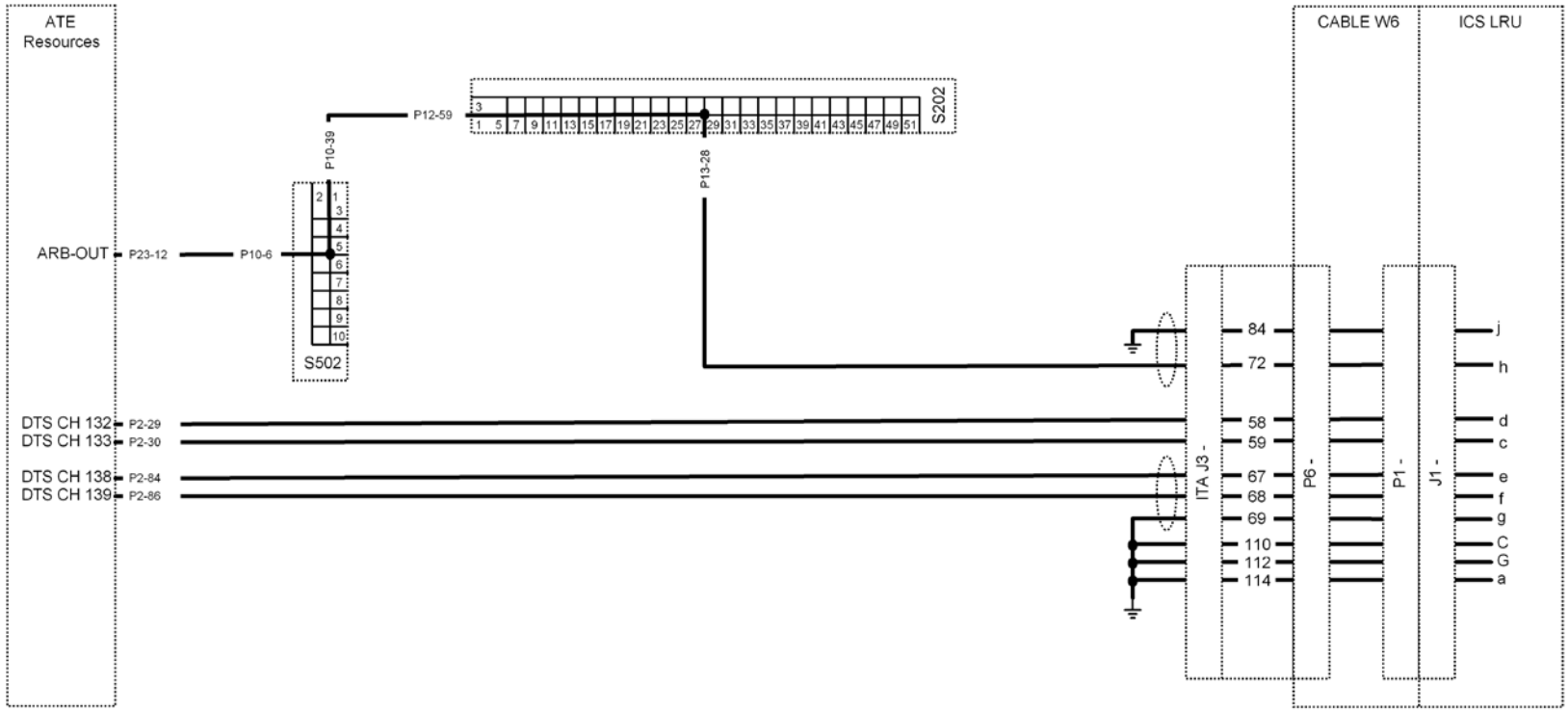
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 312 'CREW' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'CREW' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file CREW.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'CREW' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'CREW' lamp (required by the next test).

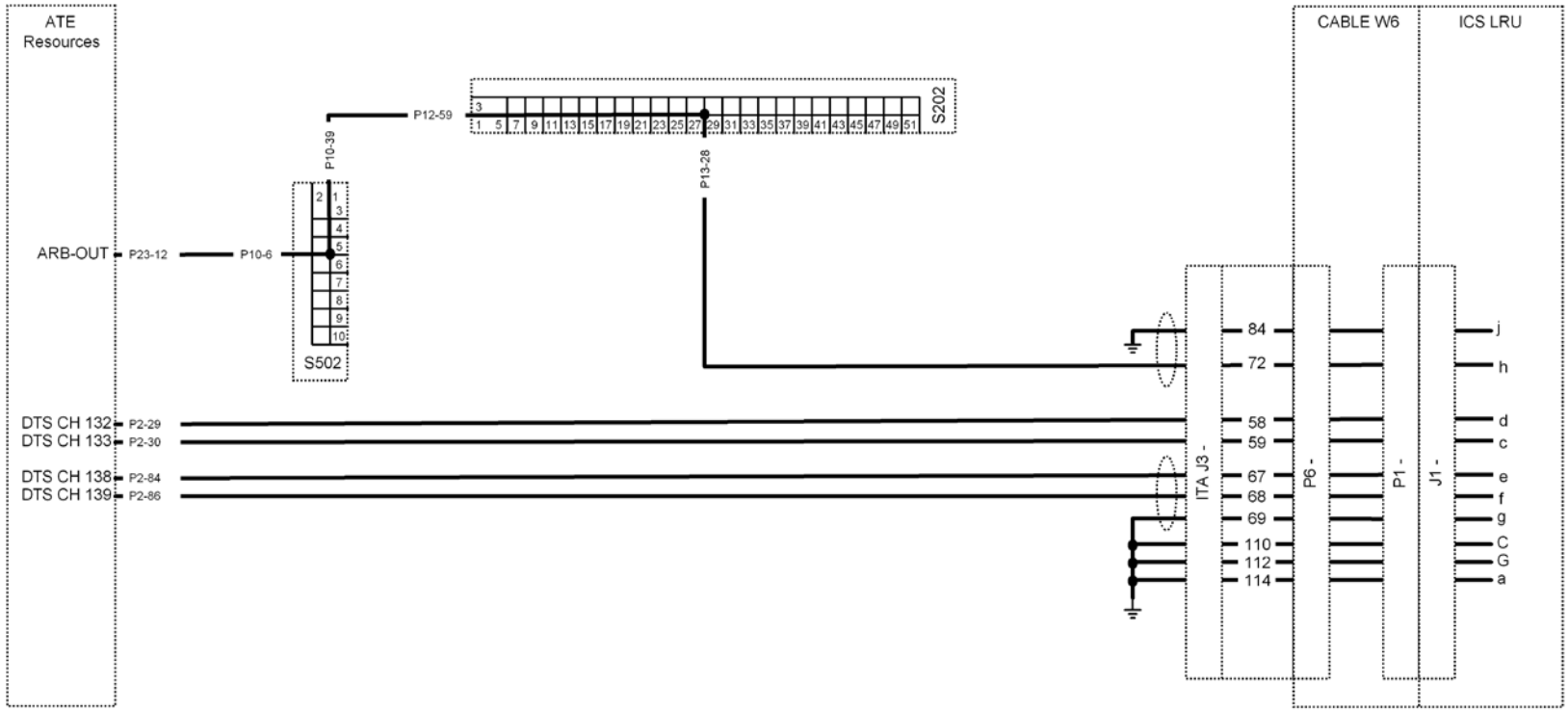
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 313 'SEL B/ MON B' Switch Operation Test

This step verifies that depressing the front panel 'SEL B/ MON B' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'SEL B/ MON B' lamp (see Step 207 and 208) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'SEL B/ MON B' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B'0' / J1-f[-] = B'1') in response to the switch push, signifying a 'Request-For-Attention' generation.

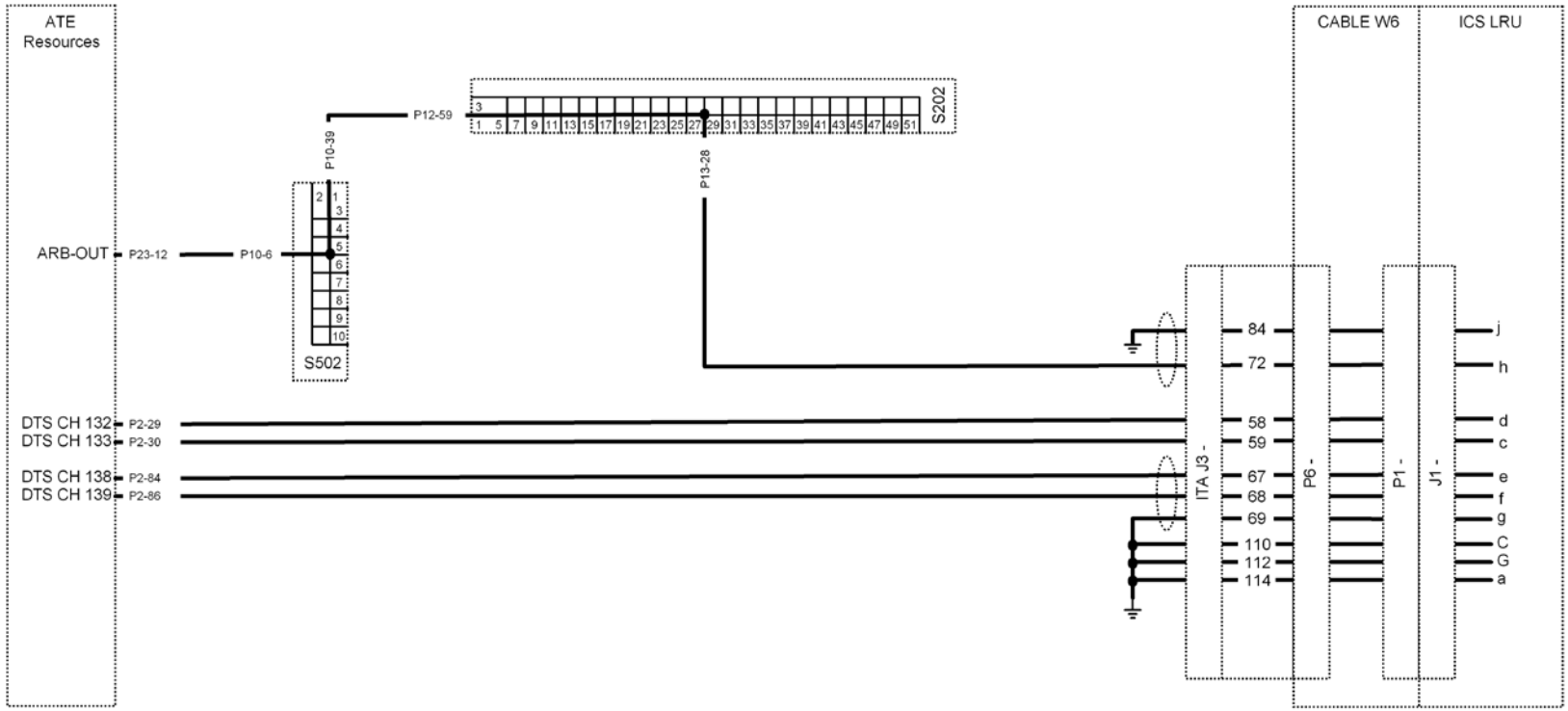
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 314 'SEL B/ MON B' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'SEL B/ MON B' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file SELBMONB.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'SEL B/ MON B' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'SEL B/ MON B' lamp (required by the next test).

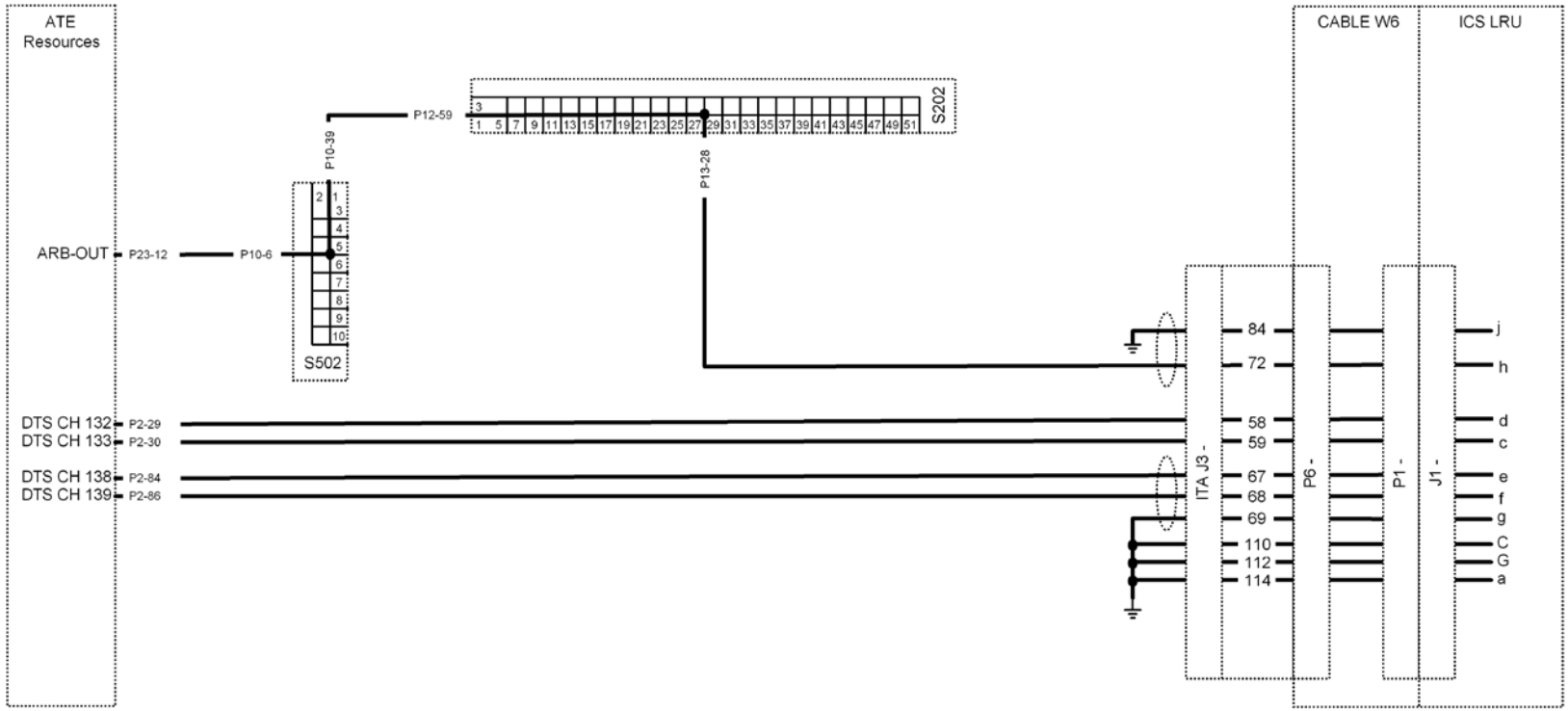
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 315 'RAD OPR 1' Switch Operation Test

This step verifies that depressing the front panel 'RAD OPR 1' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'RAD OPR 1' lamp (see Step 209) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'RAD OPR 1' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B’0’ / J1-f[-] = B’1’) in response to the switch push, signifying a 'Request-For-Attention' generation.

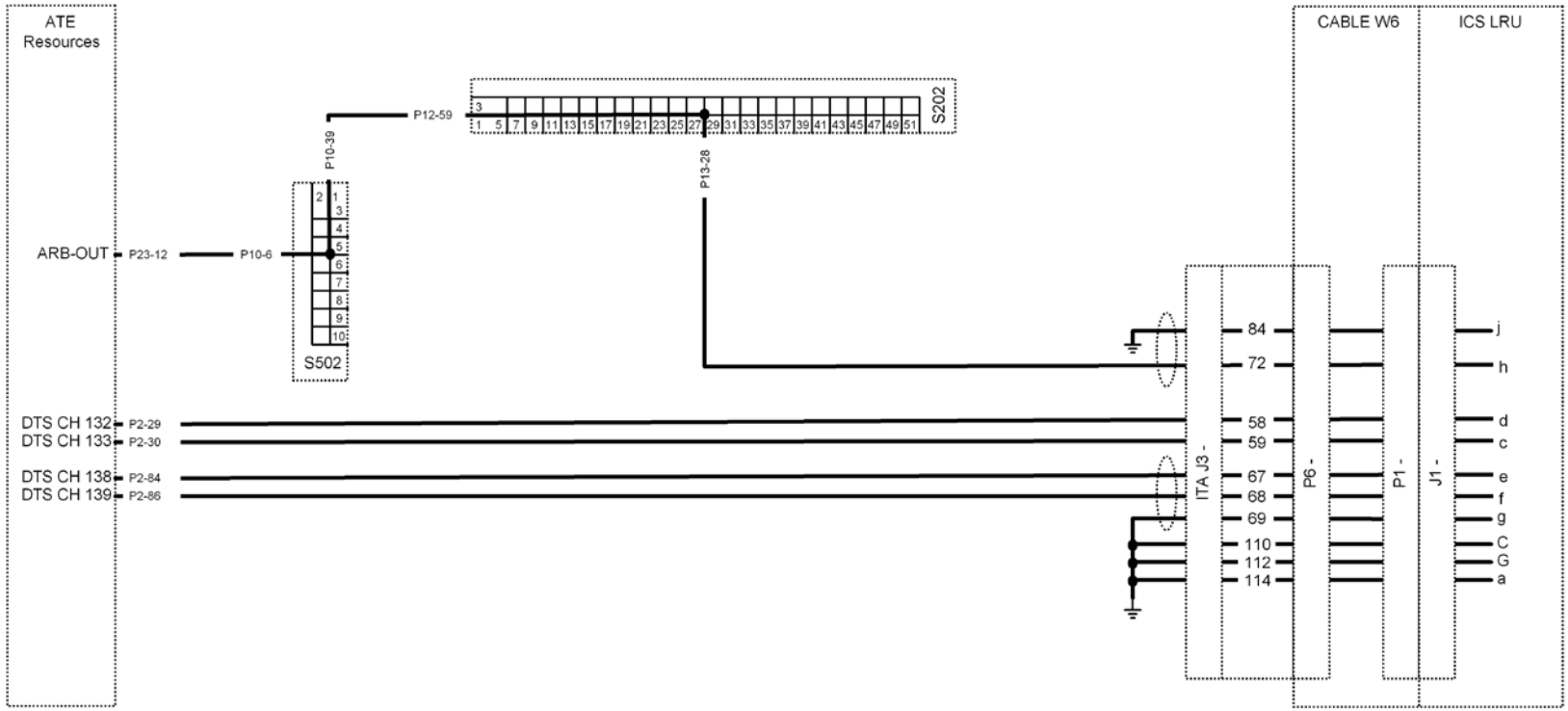
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 316 'RAD OPR 1' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'RAD OPR 1' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file 'RAD-OPR1'.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'RAD OPR 1' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'RAD OPR 1' lamp (required by the next test).

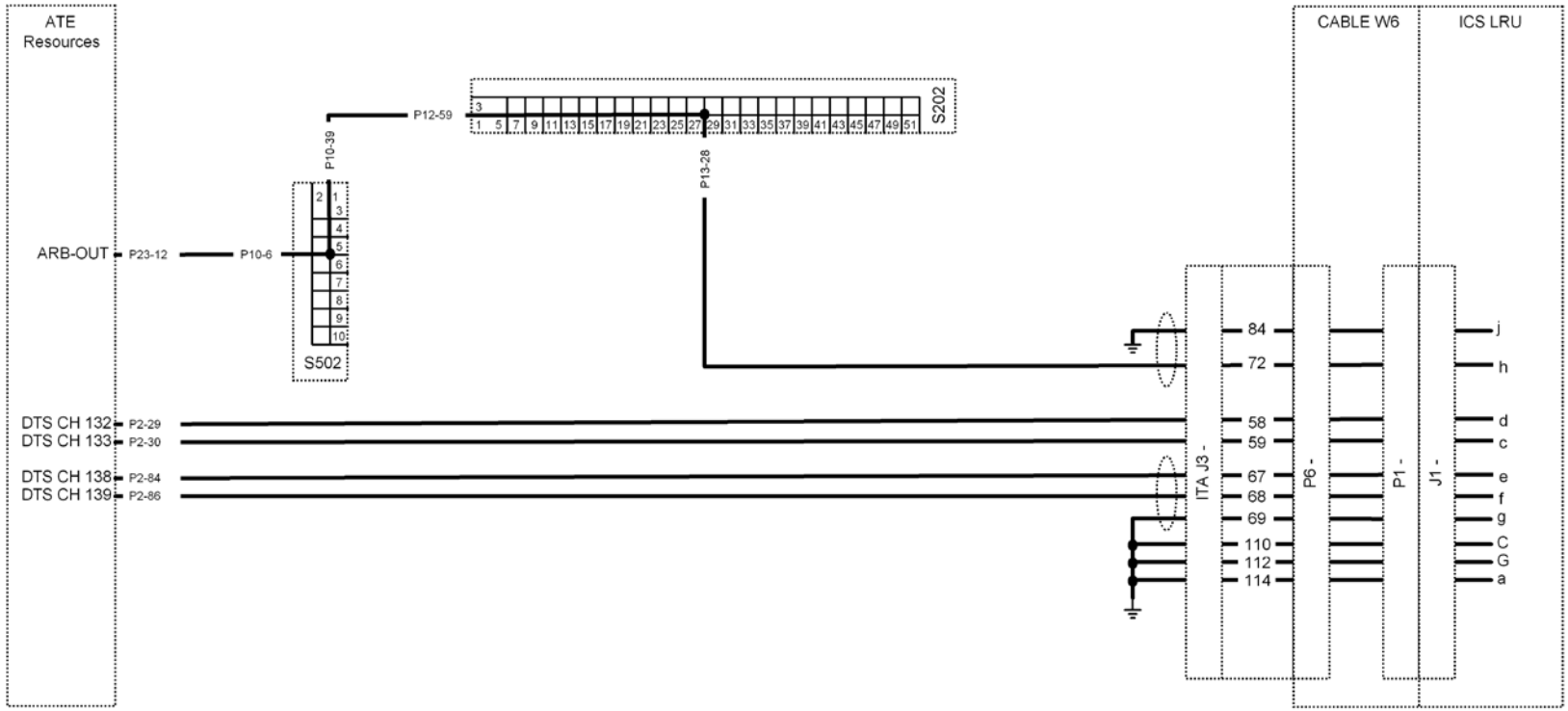
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 317 'RAD OPR 2' Switch Operation Test

This step verifies that depressing the front panel 'RAD OPR 2' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'RAD OPR 2' lamp (see Step 210) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'RAD OPR 2' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B'0' / J1-f[-] = B'1') in response to the switch push, signifying a 'Request-For-Attention' generation.

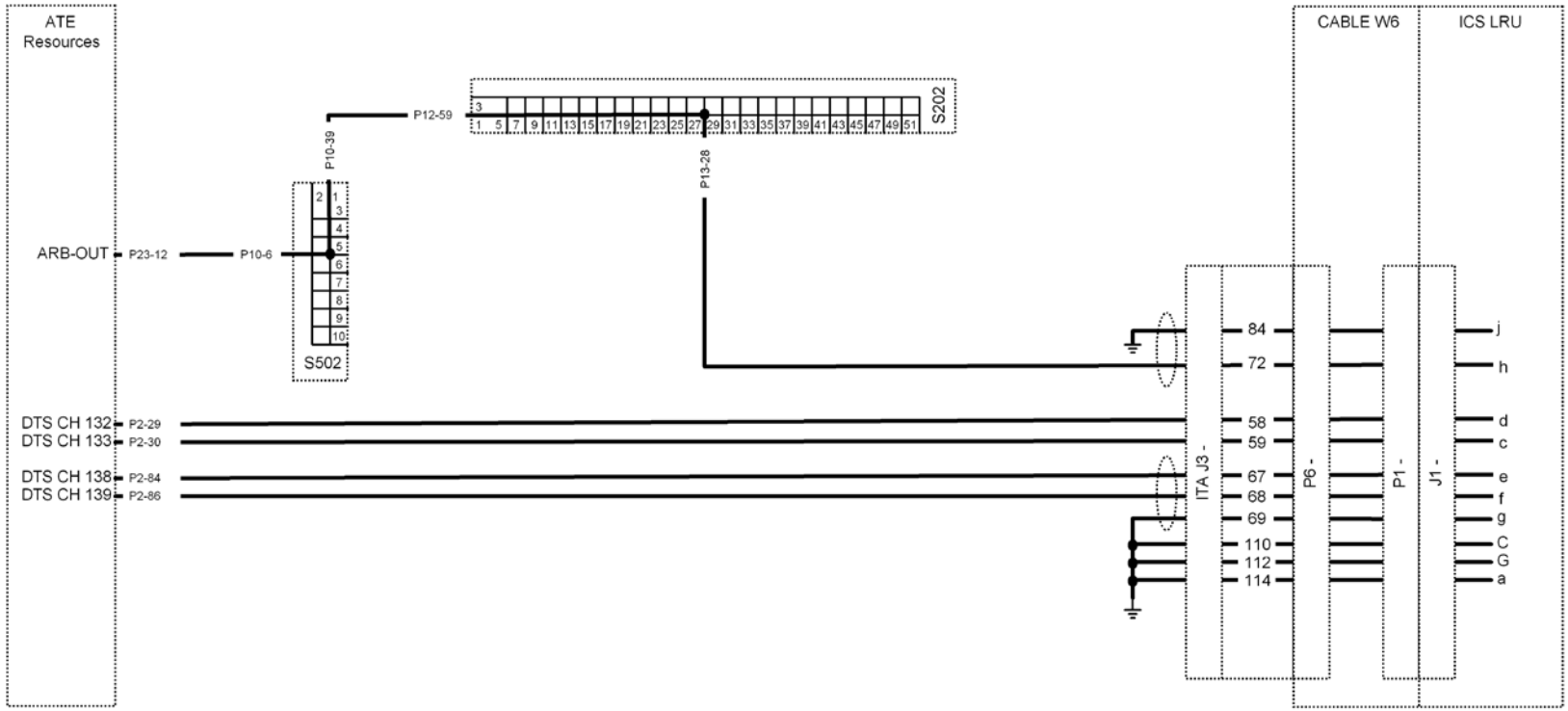
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 318 'RAD OPR 2' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'RAD OPR 2' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file 'RAD-OPR2'.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'RAD OPR 2' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'RAD OPR 2' lamp (required by the next test).

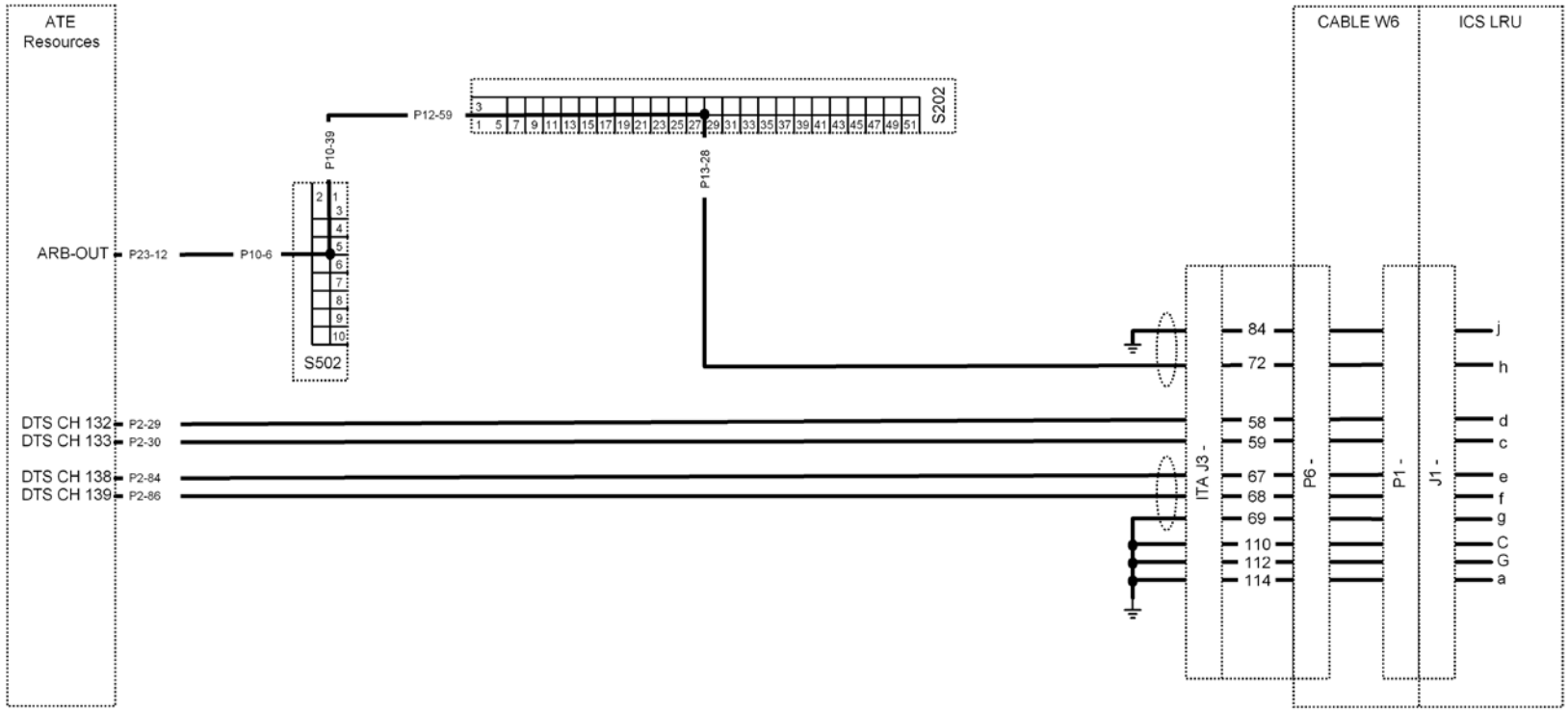
Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
d
c
e
f
g
C
G
a

Step 319 'RAD OPR 3' Switch Operation Test

This step verifies that depressing the front panel 'RAD OPR 3' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'RAD OPR 3' lamp (see Step 211) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'RAD OPR 3' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B’0’ / J1-f[-] = B’1’) in response to the switch push, signifying a 'Request-For-Attention' generation.

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
69
110
112
114
j
h
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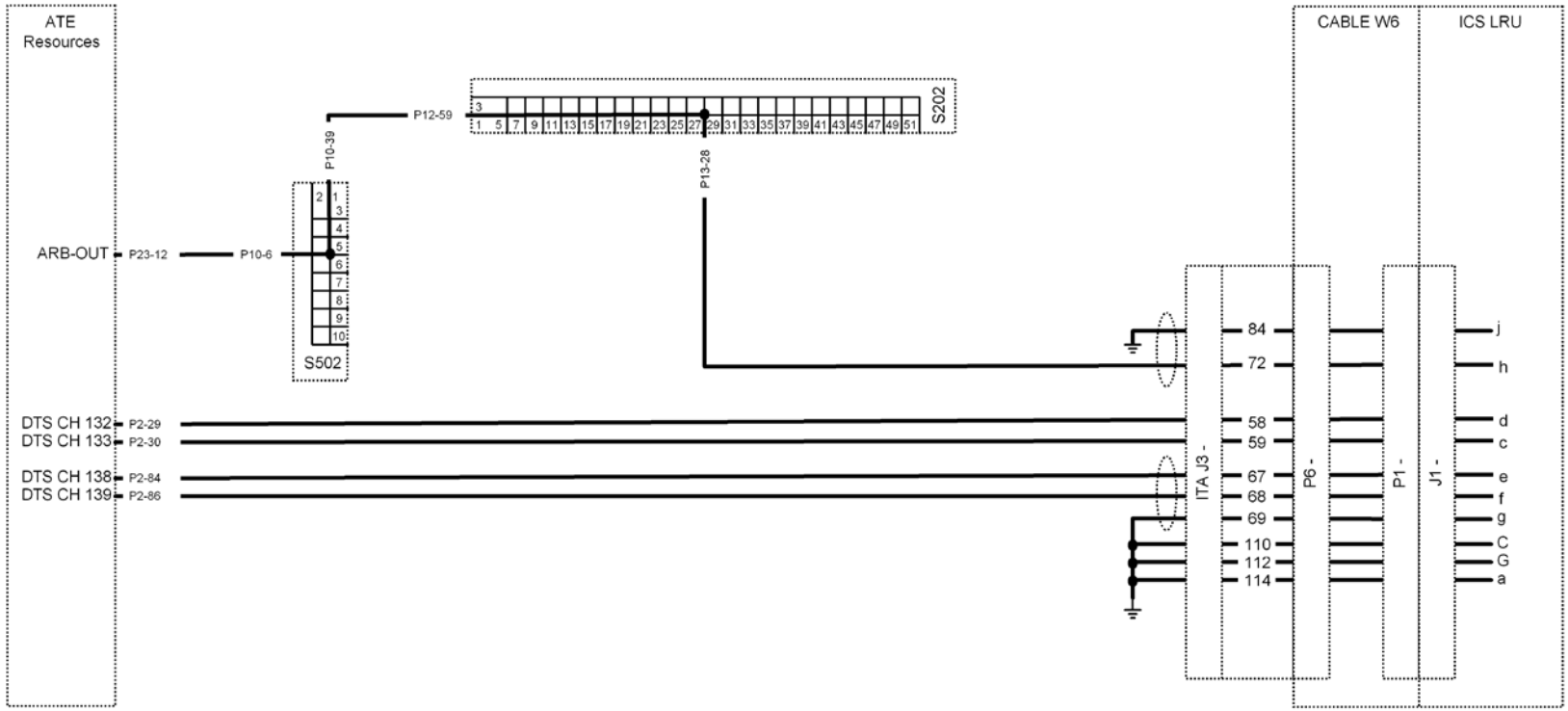
c
e
f
g
C
G
a

Step 320 'RAD OPR 3' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'RAD OPR 3' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file 'RAD-OPR3'.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'RAD OPR 3' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'RAD OPR 3' lamp (required by the next test).

Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
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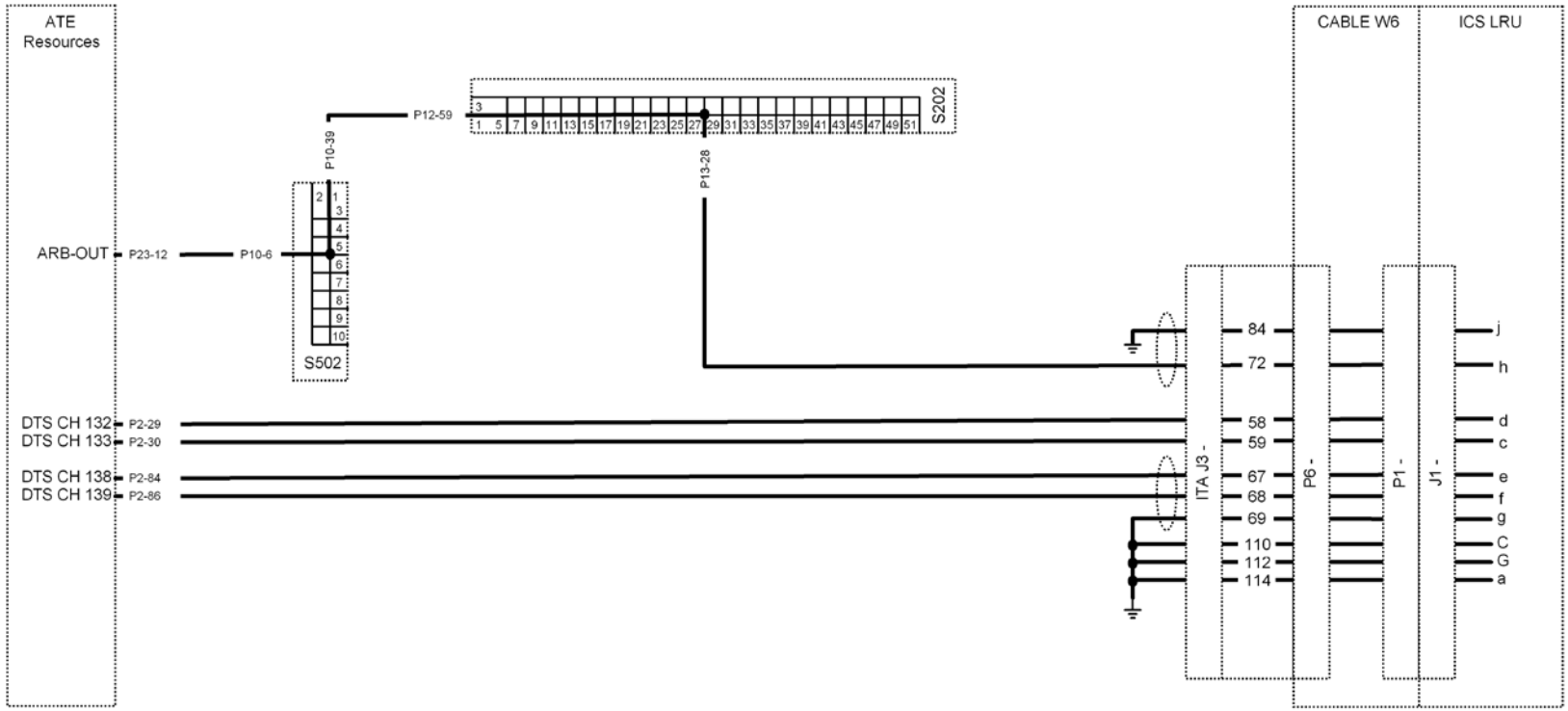
Step 321 'RAD OPR 4' Switch Operation Test

This step verifies that depressing the front panel 'RAD OPR 4' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'RAD OPR 4' lamp (see Step 212) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'RAD OPR 4' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B’0’ / J1-f[-] = B’1’) in response to the switch push, signifying a 'Request-For-Attention' generation.

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
59
67
68
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110
112
114
j
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c
e
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g
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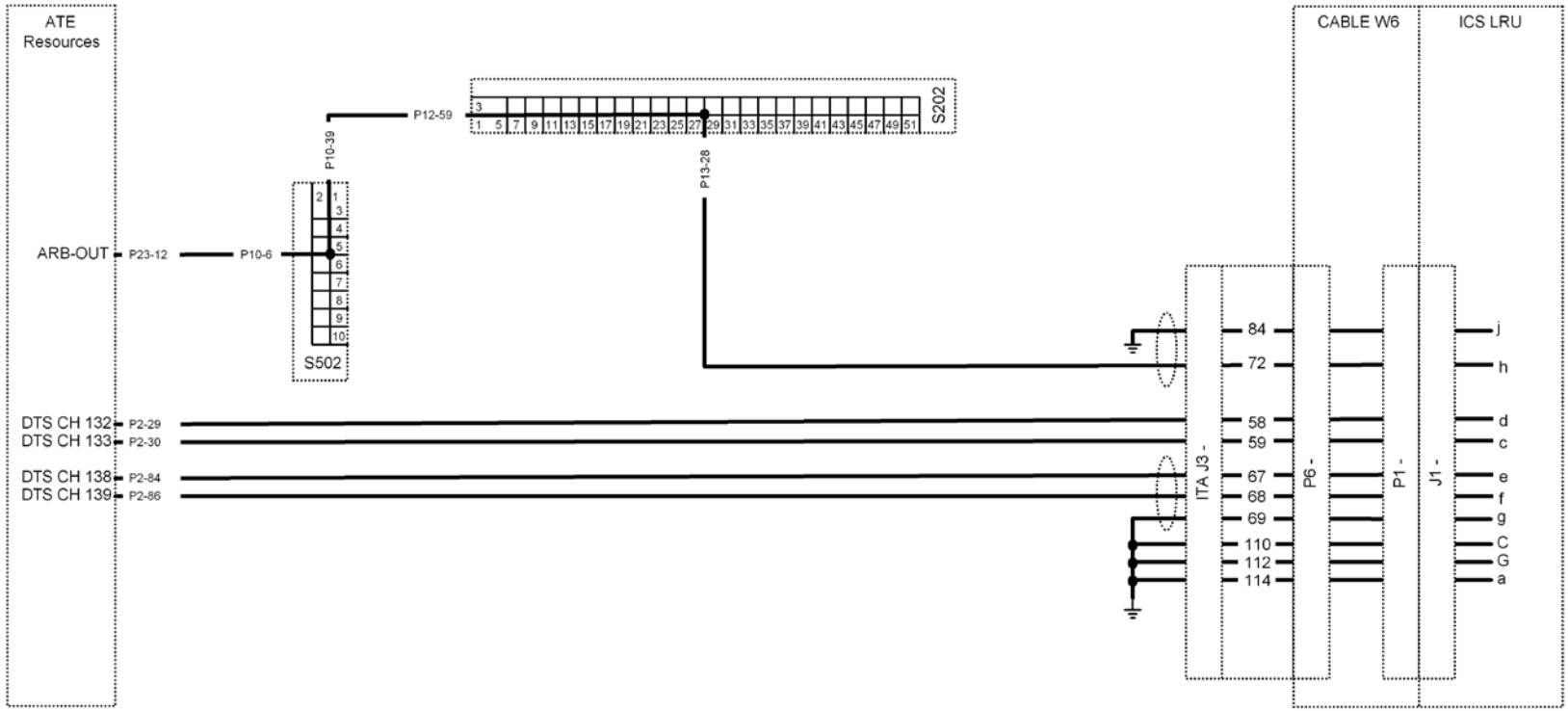
Step 322 'RAD OPR 4' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'RAD OPR 4' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file 'RAD-OPR4'.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'RAD OPR 4' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'RAD OPR 4' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
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59
67
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110
112
114
j
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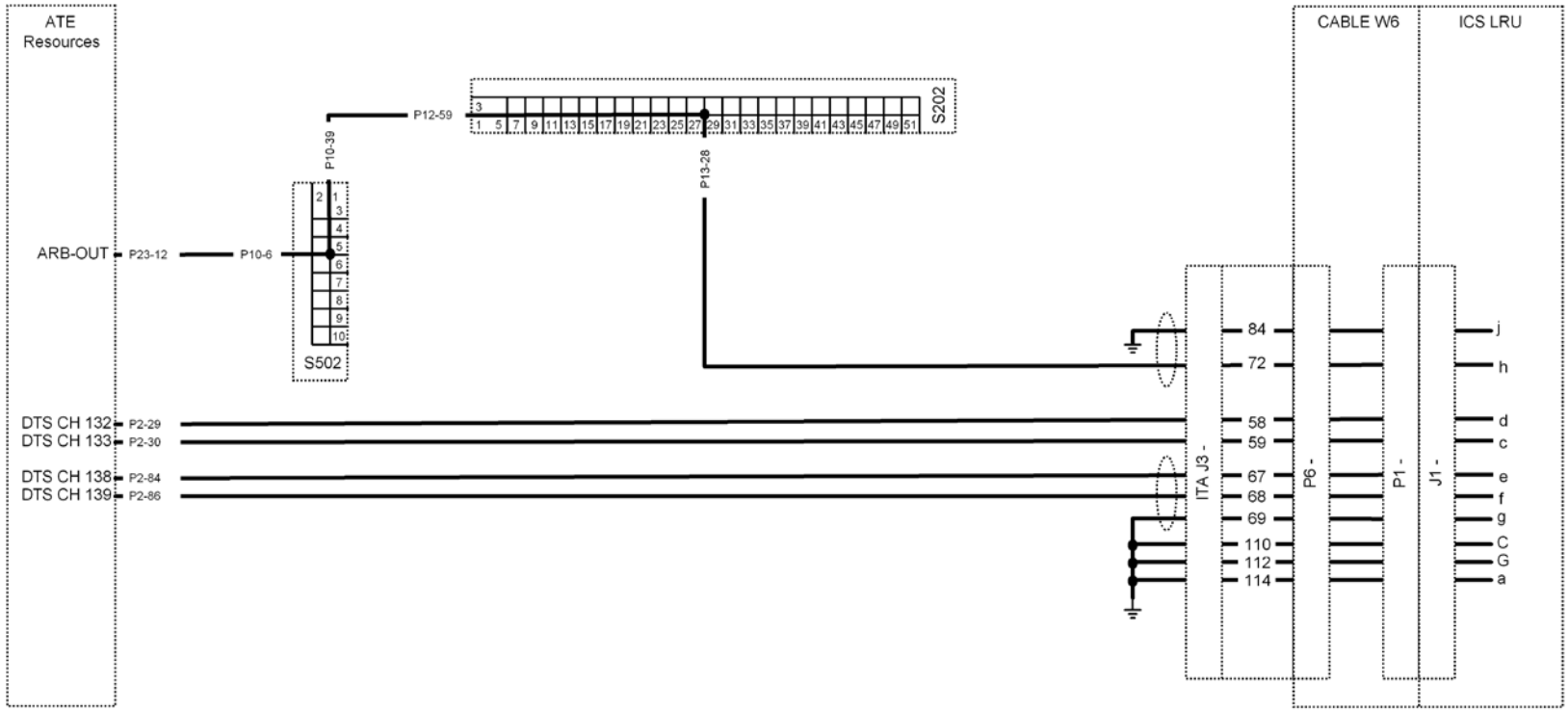
c
e
f
g
C
G
a

Step 323 'RAD OPR 5' Switch Operation Test

This step verifies that depressing the front panel 'RAD OPR 5' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'RAD OPR 5' lamp (see Step 213) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'RAD OPR 5' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B’0’ / J1-f[-] = B’1’) in response to the switch push, signifying a 'Request-For-Attention' generation.

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
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110
112
114
j
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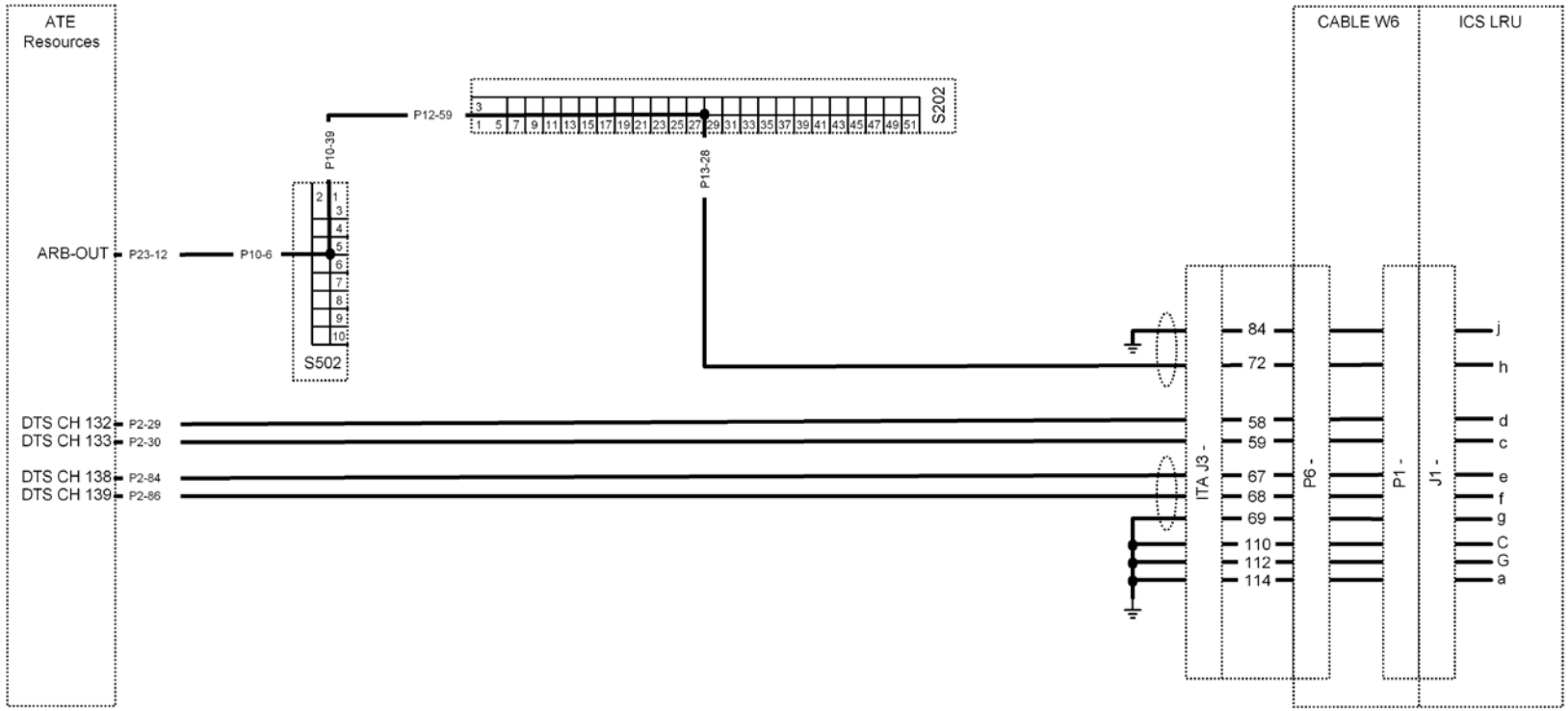
c
e
f
g
C
G
a

Step 324 'RAD OPR 5' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'RAD OPR 5' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file 'RAD-OPR5'.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'RAD OPR 5' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'RAD OPR 5' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
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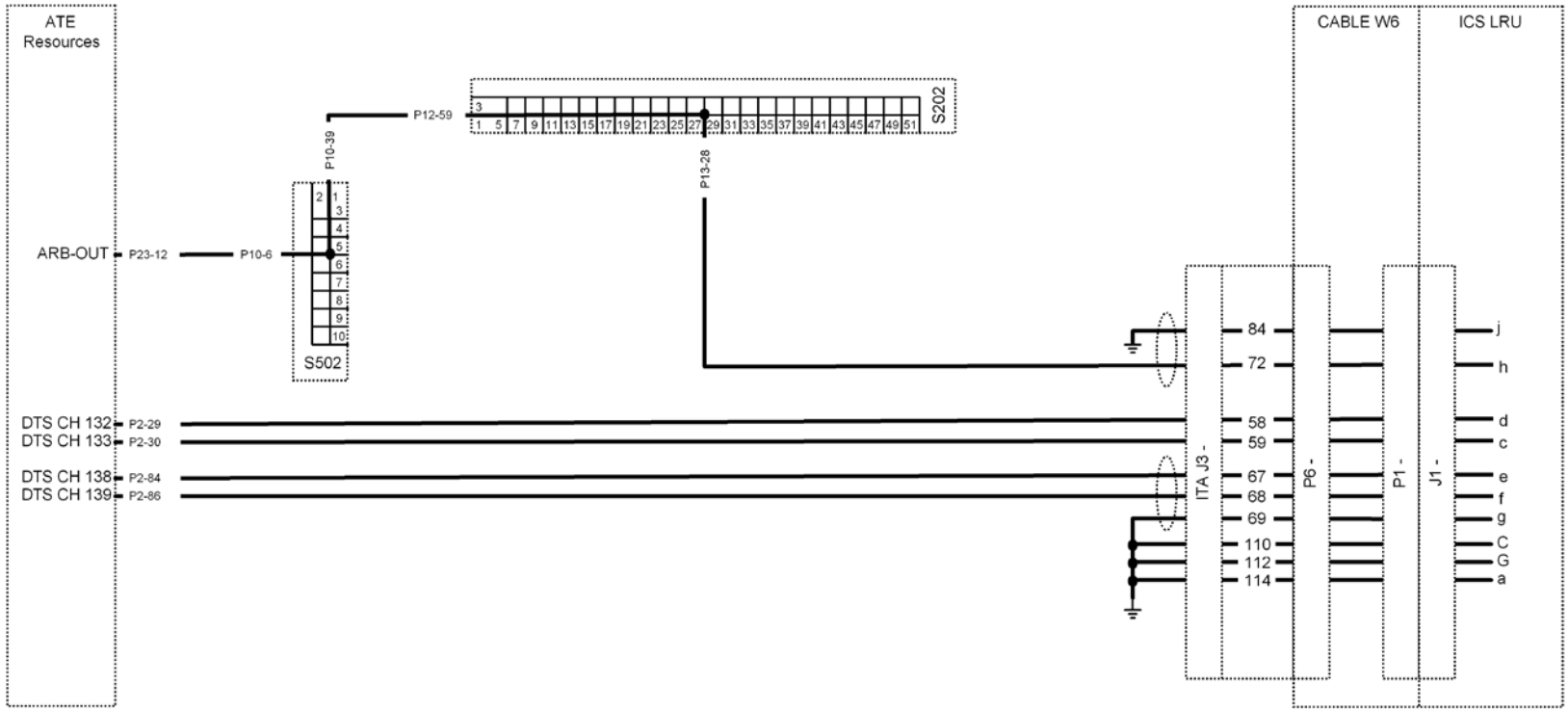
Step 325 'SEL A/ MON A' Switch Operation Test

This step verifies that depressing the front panel 'SEL A/ MON A' switch causes logic on CCA A4 to generate a 'Request-For-Attention'. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA to illuminate the front panel 'SEL A/ MON A' lamp (see Step 216 and 217) to assist the operator in locating the switch, but not required for the test to pass. The operator is instructed to momentarily depress the 'SEL A/ MON A' switch. The DTS is used to verify the 'Serial Data Out' line has toggled LO (J1-e[+] = B’0’ / J1-f[-] = B’1’) in response to the switch push, signifying a 'Request-For-Attention' generation.

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
58
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67
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69
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114
j
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e
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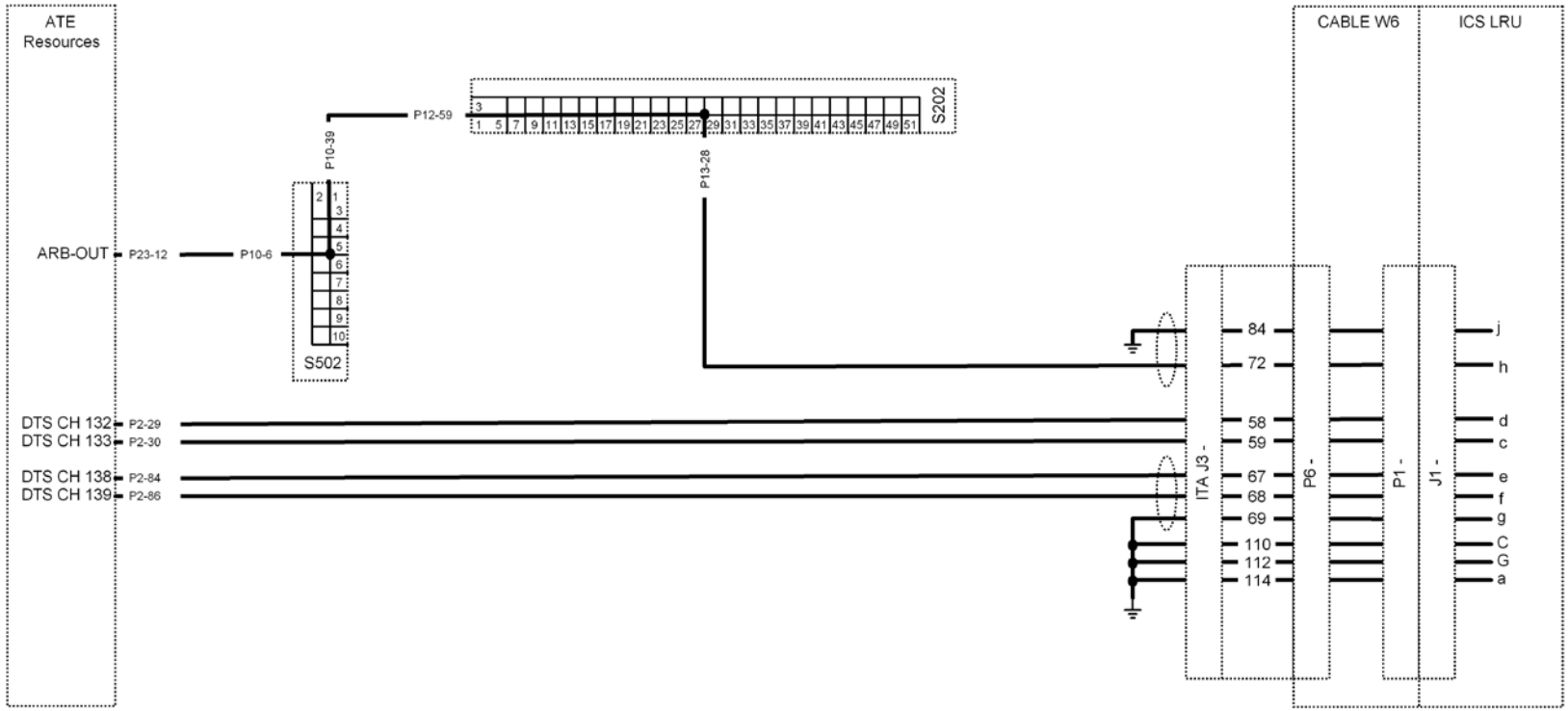
G
a

Step 326 'SEL A/ MON A' Switch Data Transmission Test

This step causes the encoder logic on CCA A4 to transmit a serial data character code representing the address of the 'SEL A/ MON A' switch previously depressed. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file SELAMONA.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE'. This prompts the UUT to transmit the code for the depressed switch on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character for valid Start/Stop bits, correct parity, and the correct 'SEL A/ MON A' switch code (each bit is 16 (32 KHz) clock periods in duration). The DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to turn off the 'SEL A/ MON A' lamp (required by the next test).

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
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67
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110
112
114
j
h
d
c
e
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g
C
G
a

MODULE 4 COMMUNICATION ERROR HANDLING TESTS

Module 4 verifies that data communication error handling logic on CCA A4 responds accurately to all possible data error conditions relative to the Serial Data In.

Step 401 Parity Error Generation Test

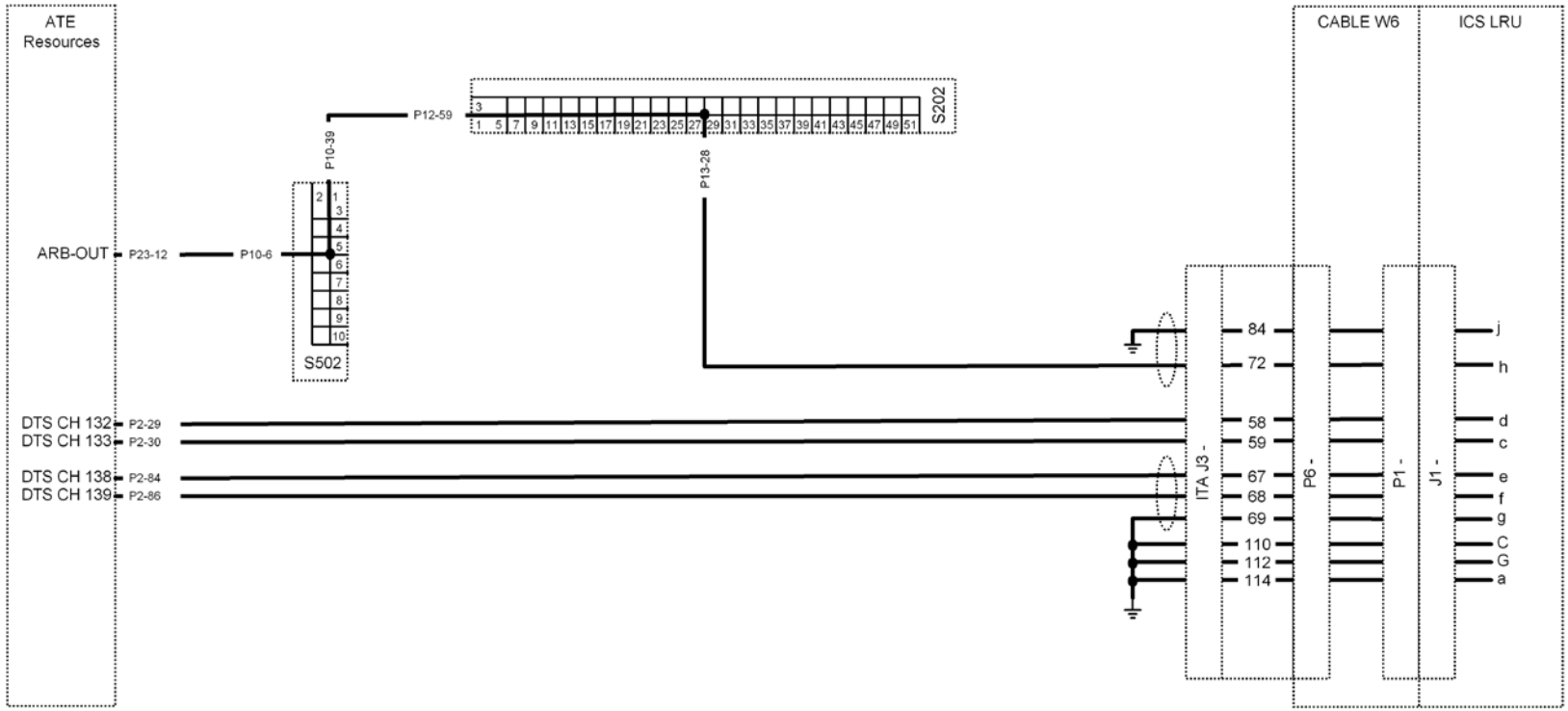
This step verifies the ability of the logic on CCA A4 to detect and, once polled with a STATUS-REQUEST, report an error status indicated by transmitter bit 'T7' set to a HI. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which contains an EVEN number of ONES (B'10001100110'), which will generate a parity error status as follows:.

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The DTS (M910NAM executing DTB file ERR-STAT.dtb) is then used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'STATUS-REQUEST'. This prompts the UUT to transmit the UUT status over the differential 'Serial Data Out' line, J1-e(+)/J1-f(-) and the Status Bit (T7) is tested to be set HI.

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
84
72
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110
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114
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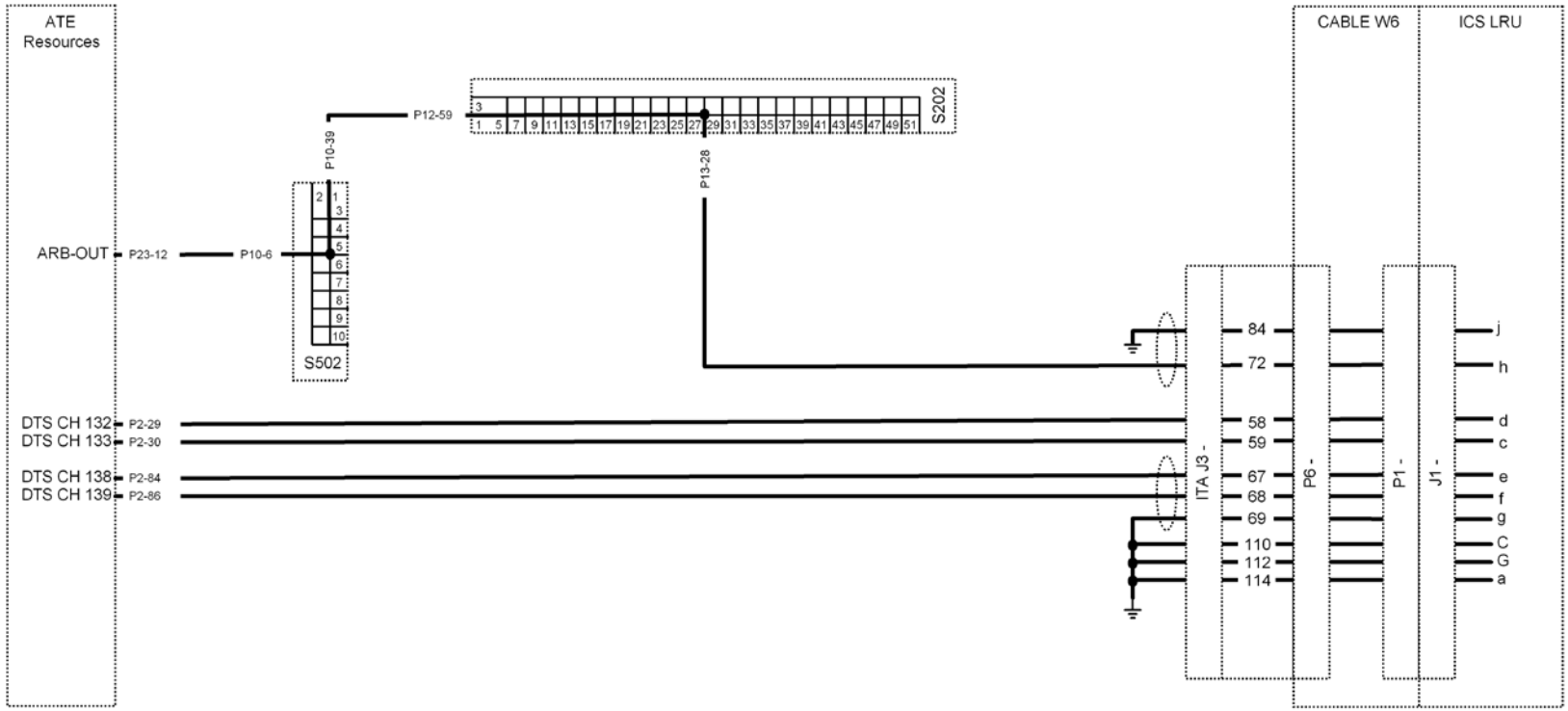
G
a

Step 402 Error Status Cleared via ‘Status-Request’ Test

This step verifies that a STATUS-REQUEST will reset a data communication error status condition. With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file NO-ERROR.dtb) is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'STATUS-REQUEST'. This prompts the UUT to transmit the status code on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). The DTB file verifies the transmitted character to determine that the error status is reset, indicated by status bit (T7) is a logic LO (each bit is 16 clock periods in duration).

Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
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c
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f
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C
G
a

Step 403 Framing Error Test

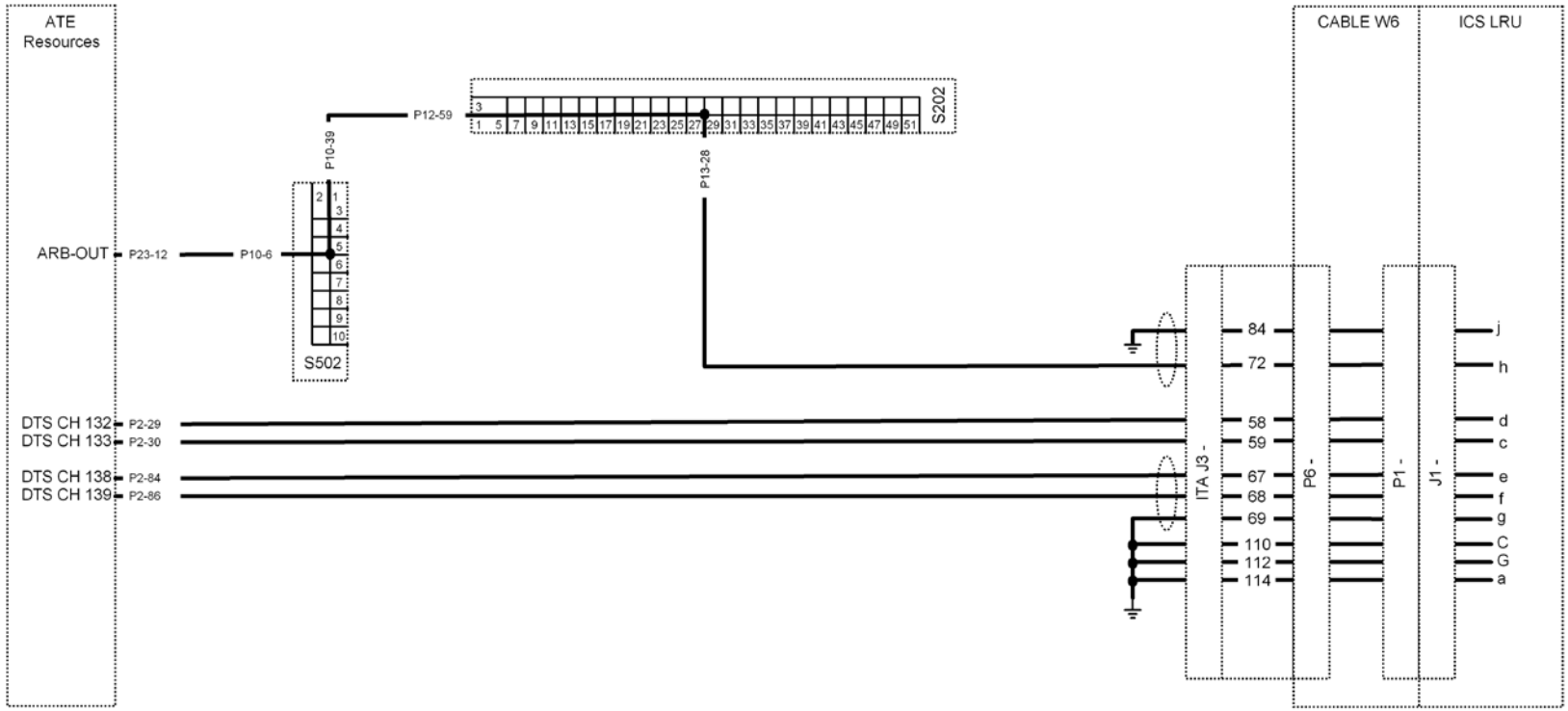
This step verifies the ability of the logic on CCA A4 to detect a Framing Error status indicated by the 'Serial Data Out Line' going LO. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-) to initially set 'Serial Data Out' line J1-e(+)/J1-f(-) to a HI state. Then a differential serial data command on 'Serial Data In', J1-d(+)/J1-c(-) which contains a LO in the STOP BIT (B'00000001110') position which is normally always HI as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'01' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The 'Serial Data Out' line J1-e(+)/J1-f(-) is then verified to be LO, generating a Request-For-Attention as a result of the Framing Error.

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
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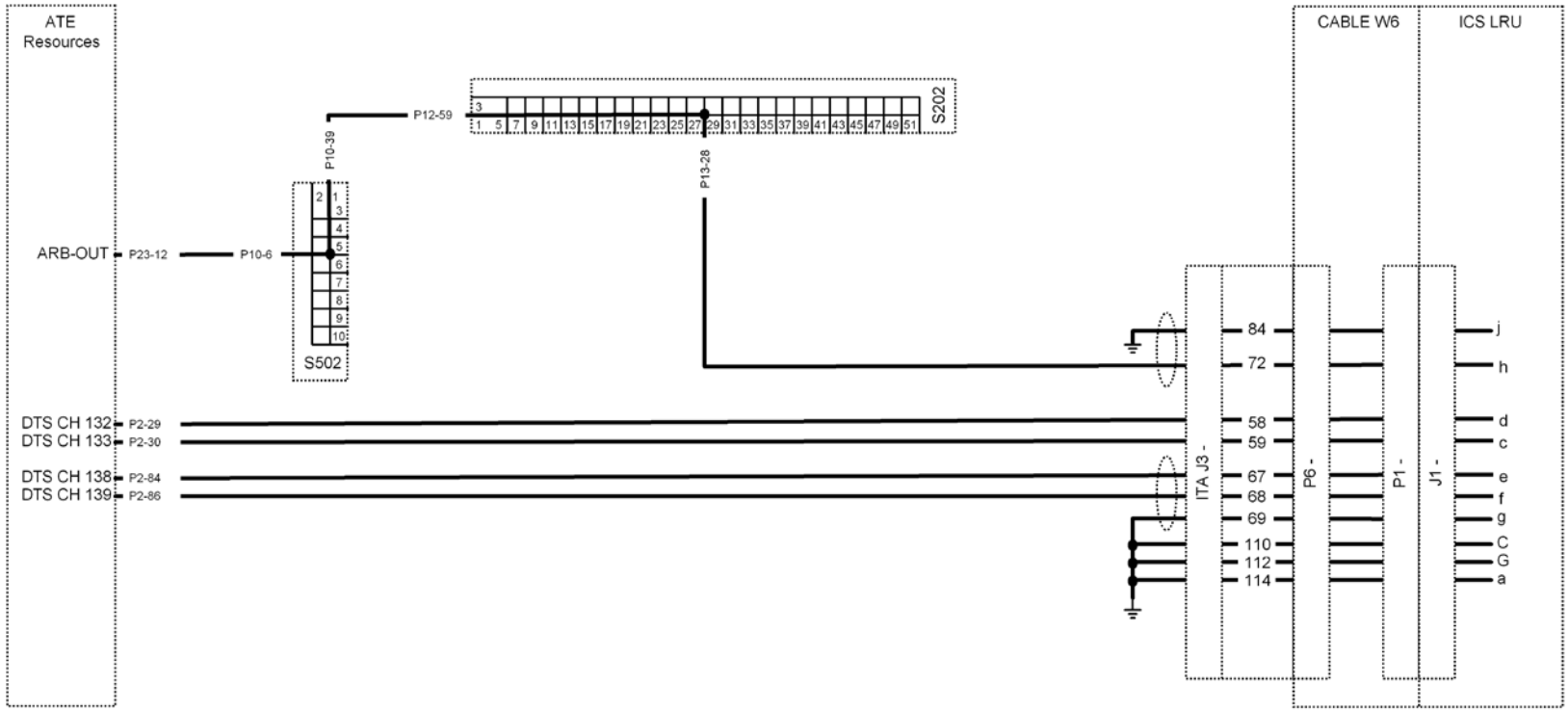
Step 404 Framing Error - Cleared Test

This step verifies that a Framing Error (generated by Step 403) status can be reset via a CLEAR-F command. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, the DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'CLEAR-F' command (see Step 102). Then the differential 'Serial Data Out' line J1-e(+)/J1-f(-) is verified to be HI as a result of the Framing Error being reset.

Connection Path as follows:


ATE
Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
ITA J3 -
P6 -
P1 -
J1 -
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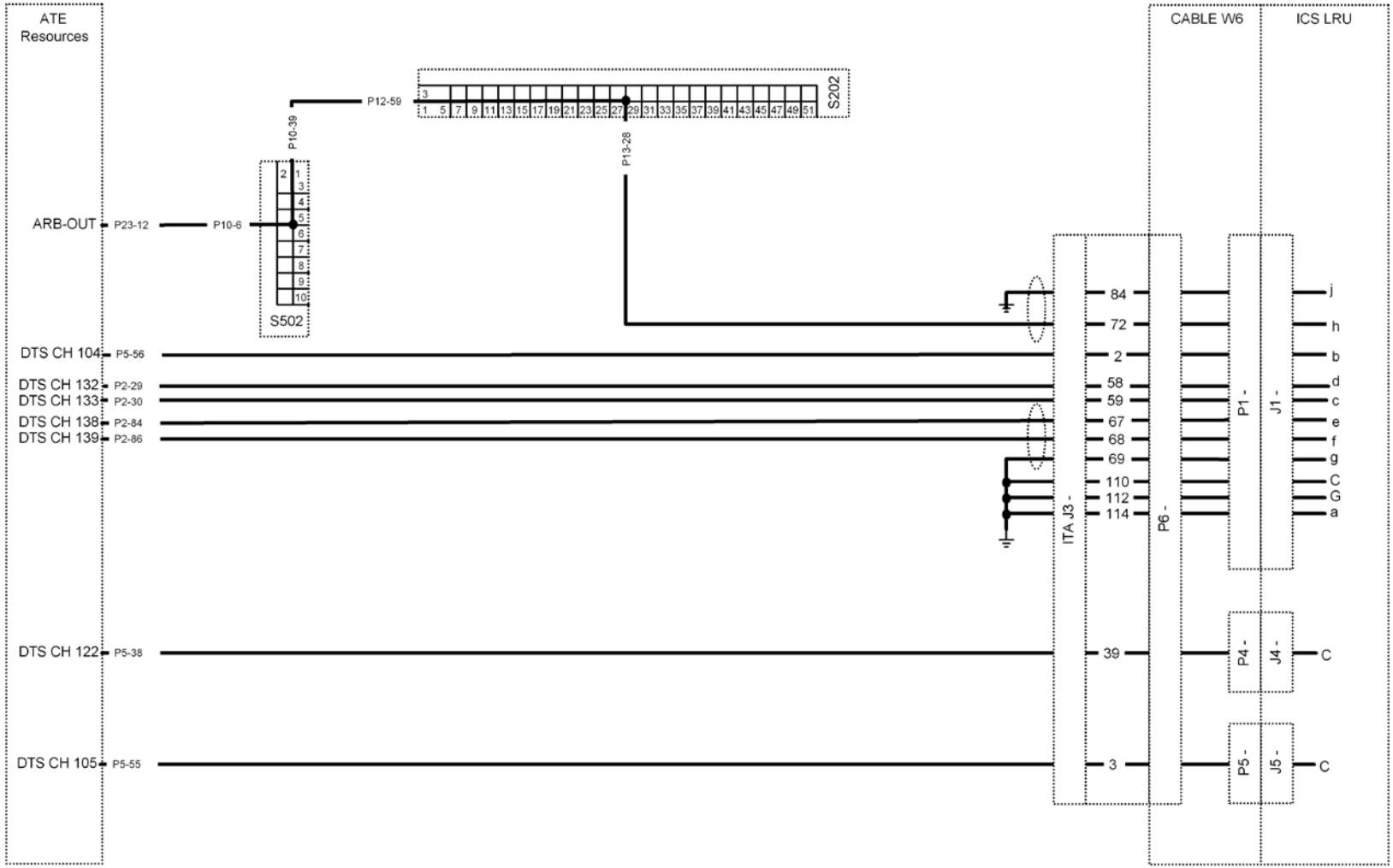
G
a

Step 405 Request Inhibit Test

This step verifies the ability of the Request-Inhibit logic on CCA A4 to prevent a new Request-For-Attention being generated (driving the 'Serial Data Out' line LO), until the previous request is processed (its character code completely transmitted). With a differential (4.0 Vpp) 32 KHz clock applied (using the ARB) at J1-j/J1-h, the DTS (M910NAM executing DTB file Rq-Inhib.dtb) is used to first, cause a RADKEY Down event by driving the RADKEY input (J4-C) LO, then sending a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a 'REQUEST-ACKNOWLEDGE' to prompt the UUT to transmit the data character code on the differential 'Serial Data Out' line, J1-e(+)/J1-f(-). While the data character is being transmitted, the DTB file drives the ICKEY input (J5-C) low, attempting to generate another Request-For-Attention. The DTB file then verifies the transmitted character to be a valid RADKEY Down code (B'11001100000') to indicate that the second request is inhibited.

Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P12-59
S202
P10-39
P13-28
ARB-OUT
P23-12
P10-6
S502
DTS CH 104
P5-56
DTS CH 132
P2-29
DTS CH 133
P2-30
DTS CH 138
P2-84
DTS CH 139
P2-86
DTS CH 122
P5-38
DTS CH 105
P5-55
ITA J3 -
P6 -
P1 -
J1 -
P4 -
J4 -
P5 -
J5 -
84
72
2
58
59
67
68
69
110
112
114
39
3
j
h
b
d
c
e
f
g
C
G
a
C
C

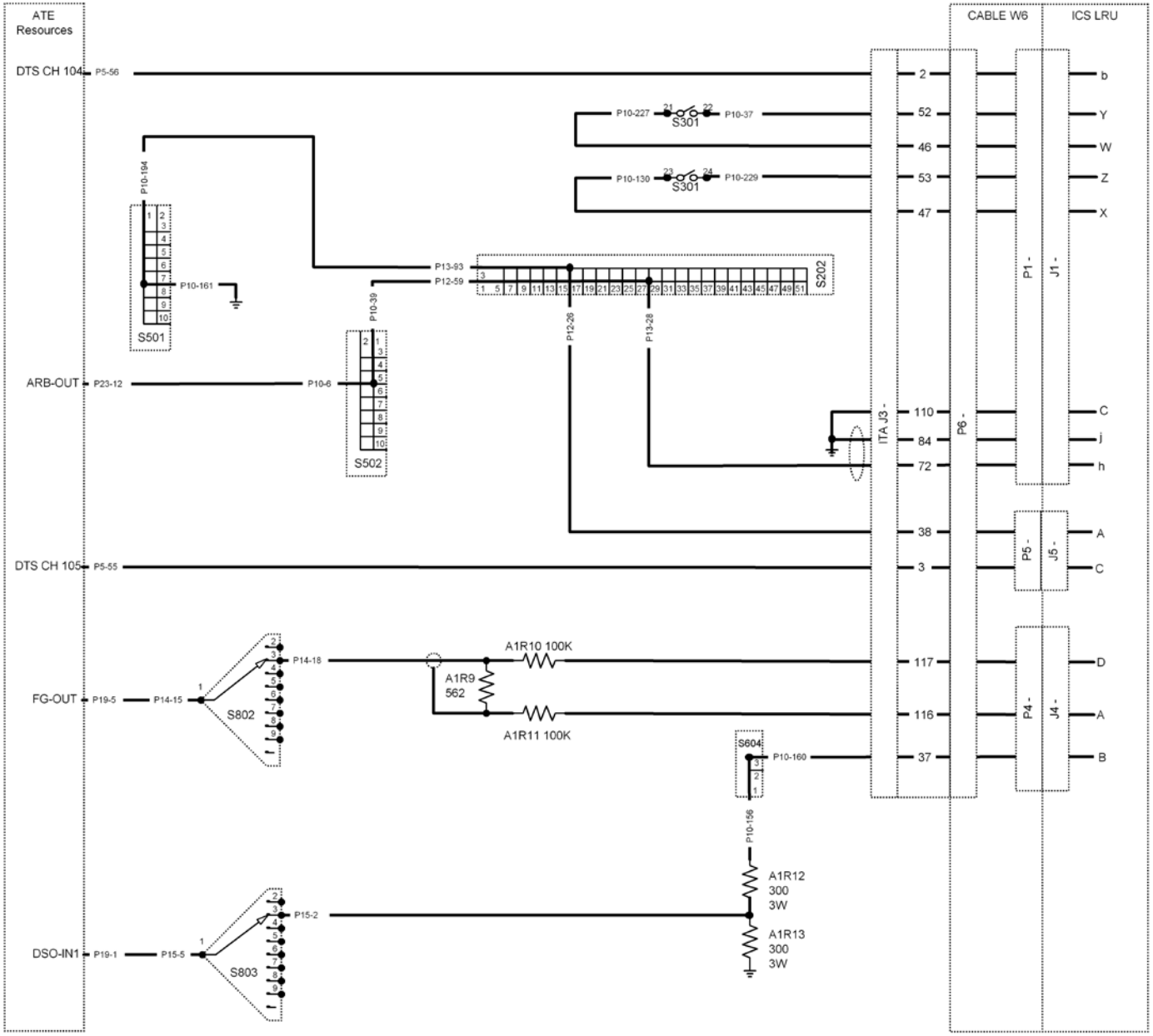
MODULE 5 CVSD TESTS

Module 5 verifies the functionality of the CVSD (audio) channel(s) with which the UUT is configured based upon the version number detected by steps 3 and 4. Also tested are portions of the decoder logic on CCA A4 affecting CVSD operation not previously tested, the audio amplifier circuitry on CCA A5, and chassis mounted component R1 (VOLUME Control).

Step 501 Headset Audio Amplitude (ICKEY Enabled) Test

This step verifies the overall gain through CVSD channel 1, consisting of CCA A1, the Audio Amplifier portion of CCA A5, the CVSD enabling logic (via ICKEY line) on CCA A4, and front panel VOLUME control R1. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, a logic LO (using the DTS) is applied at ICKEYL ENABLE, J1-b and a 10 Vpp sine-wave is applied from the Function Generator through the ITA attenuator circuit (1A1R9/1A1R10/1A1R11) to the CCA A1 'MIC IN' input at J4-D/J4-A. Because of the 50-ohm input impedance of the Function Generator only 5 Vpp is programmed, but during execution this voltage is doubled before it is applied. CVSD operation is enabled by applying a logic LO at the ICKEY keyline input at J5-C. The VOLUME control is set to fully clockwise (maximum gain) by the operator and the differential CVSD digital output of CCA A1 (J1-W/J1-X) is looped back to the CVSD input (J1-Y/J1-Z). The Digitizing Oscilloscope is used to verify the HEADSET audio output (J4-B) level is greater than 40 Vpp. The actual reading will be one-half the UUT output level due to the effect of the ITA voltage divider made up of 1A1R12 and 1A1R13 (each 300 ohm and 3 W), which also serves as a 600 ohm load specified for the HEADSET audio output.

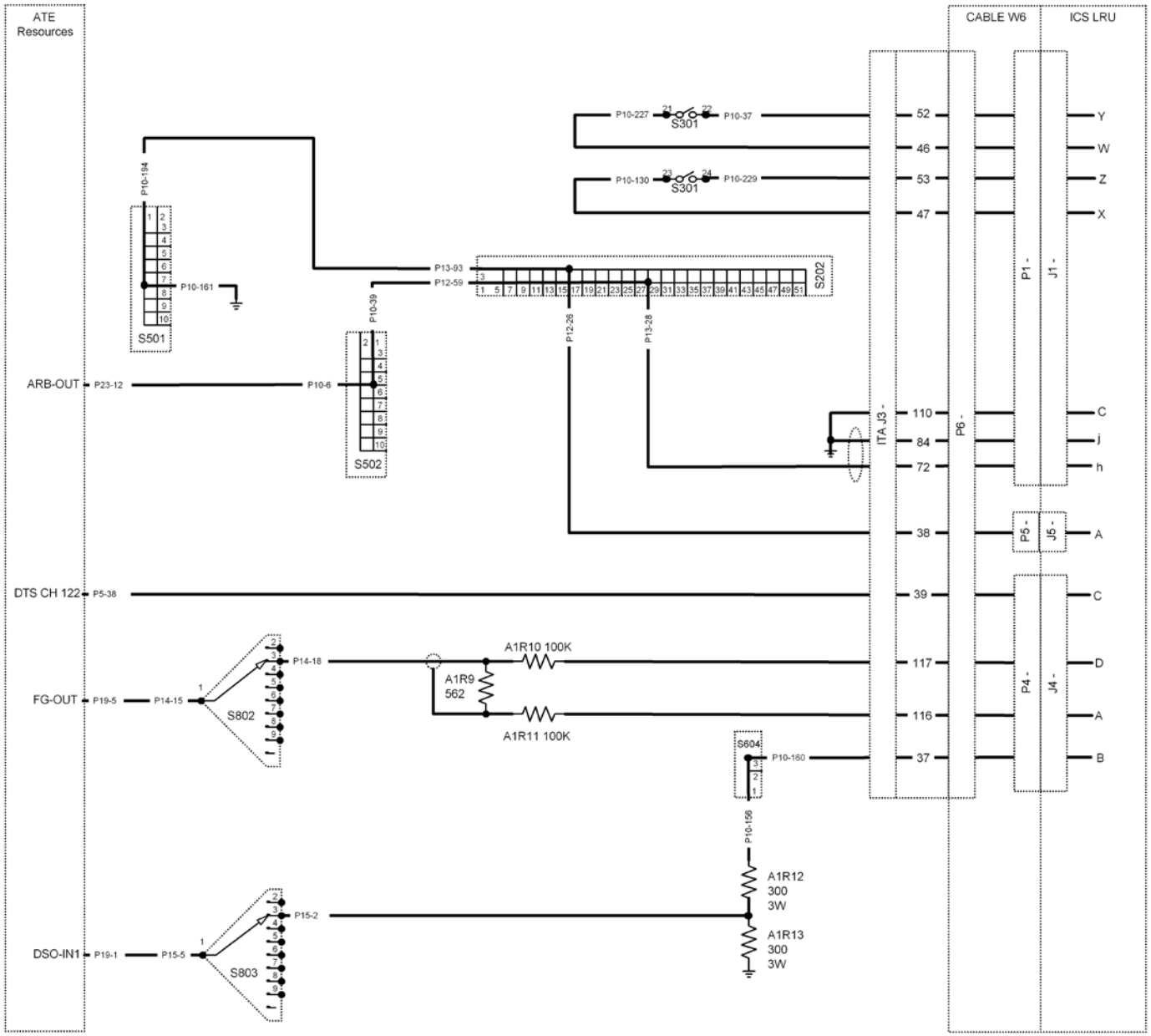
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
DTS CH 104
P5-56
P10-227
S301
P10-37
P10-130
S301
P10-229
P10-194
P10-161
S501
P13-93
P12-59
S202
P10-39
P12-26
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
P6 -
P1 -
J1 -
2
52
46
53
47
b
Y
W
Z
X
110
84
72
C
j
h
38
A
DTS CH 105
P5-55
3
C
P5 -
J5 -
A1R10 100K
A1R9
562
A1R11 100K
P14-18
FG-OUT
P19-5
P14-15
S802
117
116
D
A
P4 -
J4 -
S604
P10-160
37
B
P10-156
A1R12
300
3W
A1R13
300
3W
P15-2
DSO-IN1
P19-1
P15-5
S803

Step 502 Headset Audio Amplitude (RADKEY Enabled) Test

This step repeats Step 501with the exception being that CVSD is enabled via the RADKEY keyline by using the DTS to apply a logic LO at J4-C. The Digitizing Oscilloscope is used to verify the HEADSET audio output (J4-B) level is greater than 40 Vpp. The actual reading will be one-half the UUT output level due to the effect of the ITA voltage divider made up of 1A1R12 and 1A1R13 (each 300 ohm and 3 W), which also serves as a 600 ohm load specified for the HEADSET audio output.

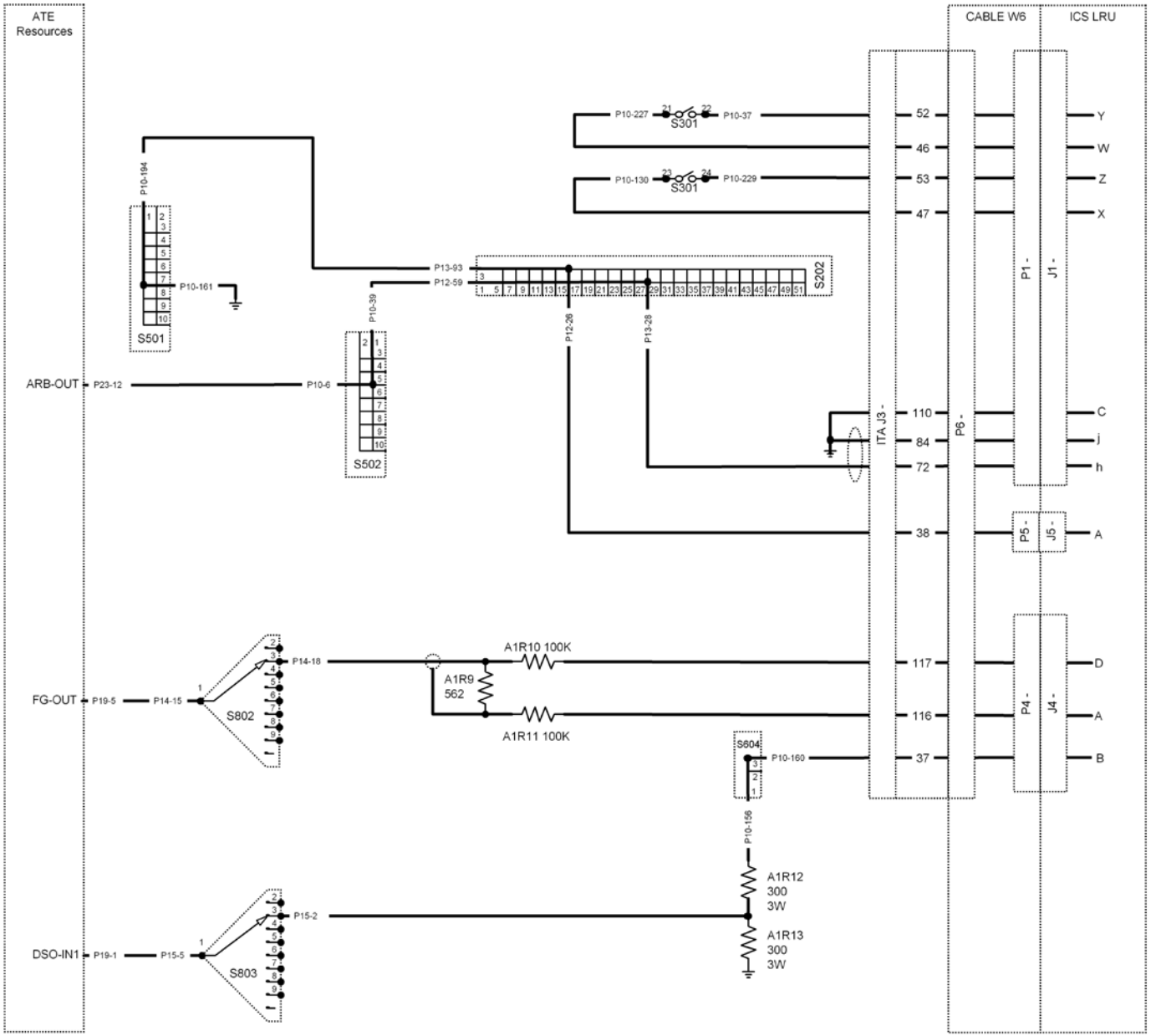
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P10-227
S301
P10-37
P10-130
S301
P10-229
52
46
53
47
Y
W
Z
X
P10-194
P10-161
S501
P13-93
P12-59
S202
P10-39
P12-28
P13-28
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
110
84
72
C
j
h
P1 -
J1 -
P6 -
P5 -
J5 -
38
A
DTS CH 122
P5-38
39
C
P14-18
A1R10 100K
A1R9
562
A1R11 100K
117
116
D
A
FG-OUT
P19-5
P14-15
S802
P4 -
J4 -
S604
P10-160
37
B
P10-156
A1R12
300
3W
A1R13
300
3W
P15-2
DSO-IN1
P19-1
P15-5
S803

Step 503 CVSD Disabled Test

This step verifies that with no CVSD enabling keyline (RADKEY/ICKEY), no audio output is present at the HEADSET AUDIO out. The same stimulus as Step 501 is applied, with the exception being that no enabling keyline input is applied. The Digitizing Oscilloscope is used to verify less than 0.5 Vpp of audio at J4-B.

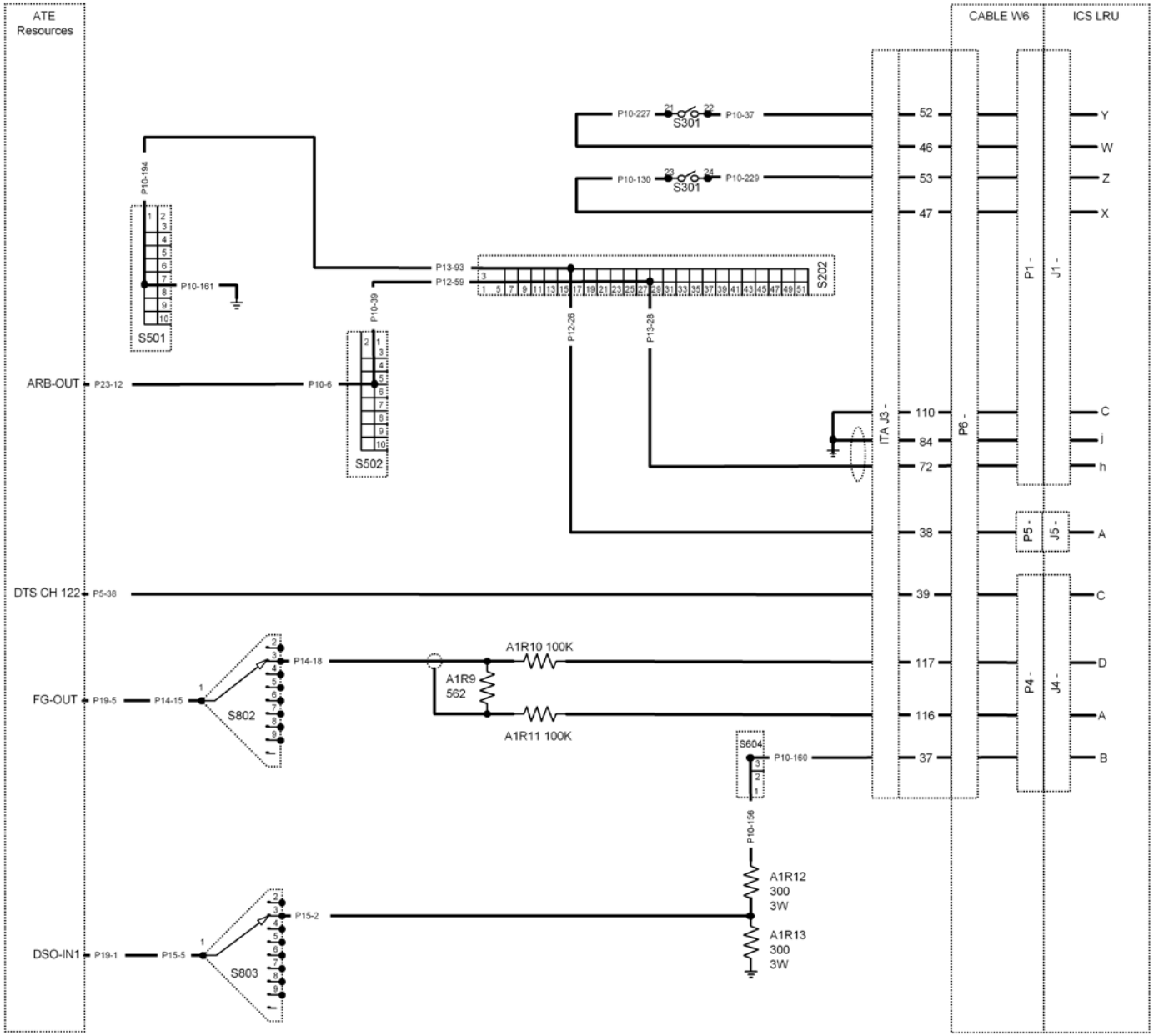
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P10-227
S301
P10-37
P10-130
S301
P10-229
52
46
53
47
Y
W
Z
X
P10-194
P10-161
S501
P13-93
P12-59
S202
P10-39
P12-26
P13-28
S502
ARB-OUT
P23-12
P10-6
ITA J3 -
110
84
72
C
J
h
P6 -
P1 -
J1 -
38
P5 -
J5 -
A
A1R10 100K
A1R9
562
A1R11 100K
P14-18
FG-OUT
P19-5
P14-15
S802
117
116
D
A
P4 -
J4 -
S604
P10-160
37
B
P10-156
A1R12
300
3W
A1R13
300
3W
P15-2
DSO-IN1
P19-1
P15-5
S803

Step 504 Headset Audio Volume Control Test

This step verifies that with the front panel VOLUME control, R1 set fully CCW (minimum gain), no audio output is present at the HEADSET AUDIO out. The same stimulus as Step 501 is applied, with CVSD enabled by applying a logic LO at RADKEY keyline input, J4-C. The operator is instructed to rotate the VOLUME control fully CCW, then the Digitizing Oscilloscope is used to verify less than 0.5 Vpp of audio at J4-B.

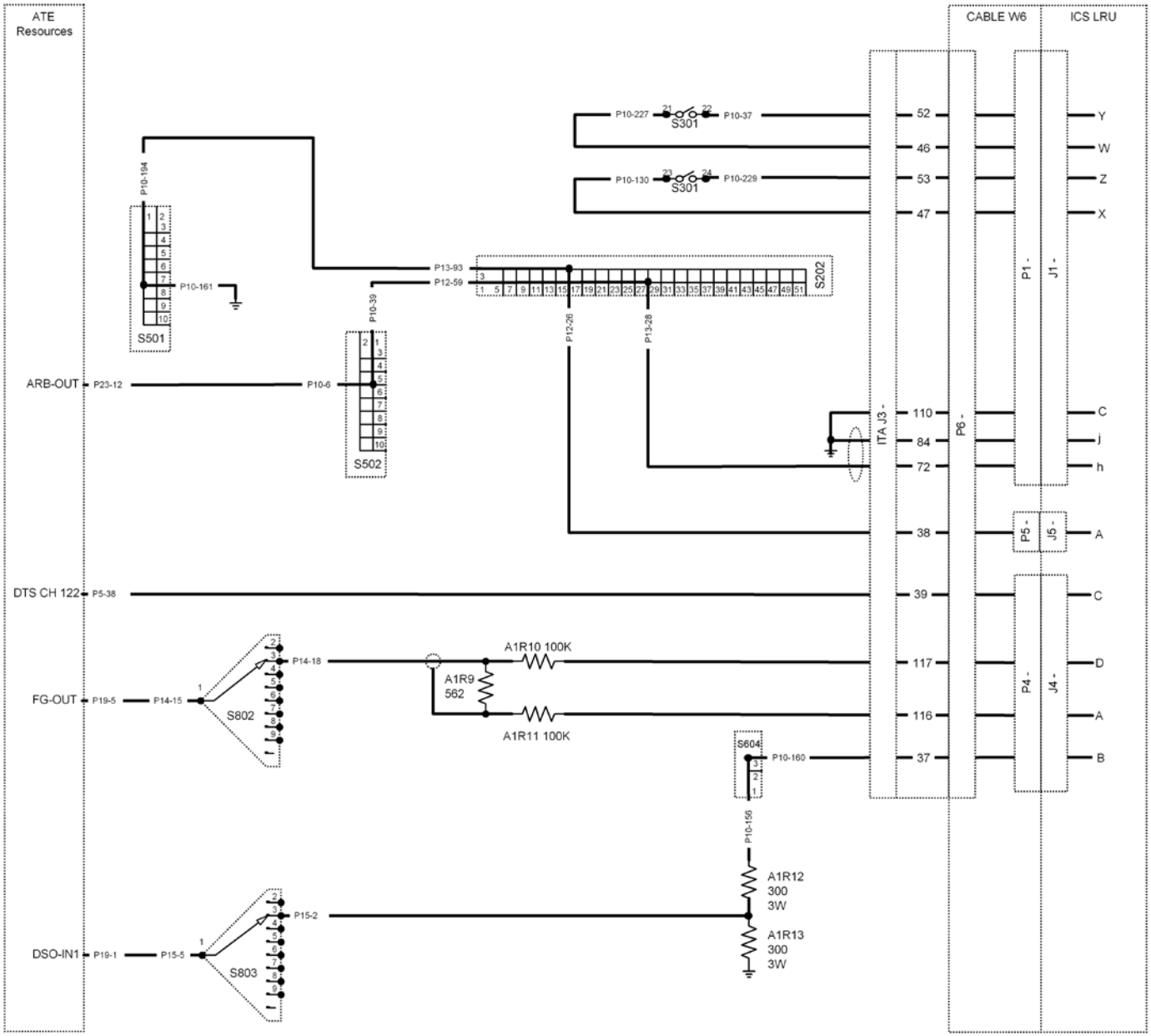
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P10-227
S301
P10-37
P10-130
S301
P10-229
52
46
53
47
Y
W
Z
X
P10-194
P13-93
P12-59
S202
P10-161
S501
P10-39
P12-26
P13-28
P1 -
J1 -
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
110
84
72
C
j
h
P6 -
P5 -
J5 -
38
A
DTS CH 122
P5-38
39
C
A1R10 100K
P14-18
A1R9
562
A1R11 100K
117
116
D
A
FG-OUT
P19-5
P14-15
S802
P4 -
J4 -
S604
P10-160
37
B
P10-156
A1R12
300
3W
P15-2
A1R13
300
3W
DSO-IN1
P19-1
P15-5
S803

Step 505 Headset Audio Distortion Test

This step test uses the Digitizing Oscilloscope in waveform sampling mode to capture one complete cycle (1 KHz), sample 5000 voltage points and perform distortion analysis. The percentage distortion is calculated as the difference between the Voltage-PP of the signal versus the True-RMS voltage of an undistorted waveform of the same amplitude. With the same stimulus as Step 501 applied, with CVSD enabled by applying a logic LO at RADKEY keyline input, J4-C, the operator is instructed to adjust the VOLUME control, R1 for an output reading of 19.0 to 20.5 Vpp (38 to 41 Vpp at UUT output J4-B) to place the signal in a known amplitude window for waveform analysis. The results of 5 waveform captures are averaged to obtain the distortion value and the result is verified to be less than 5%.

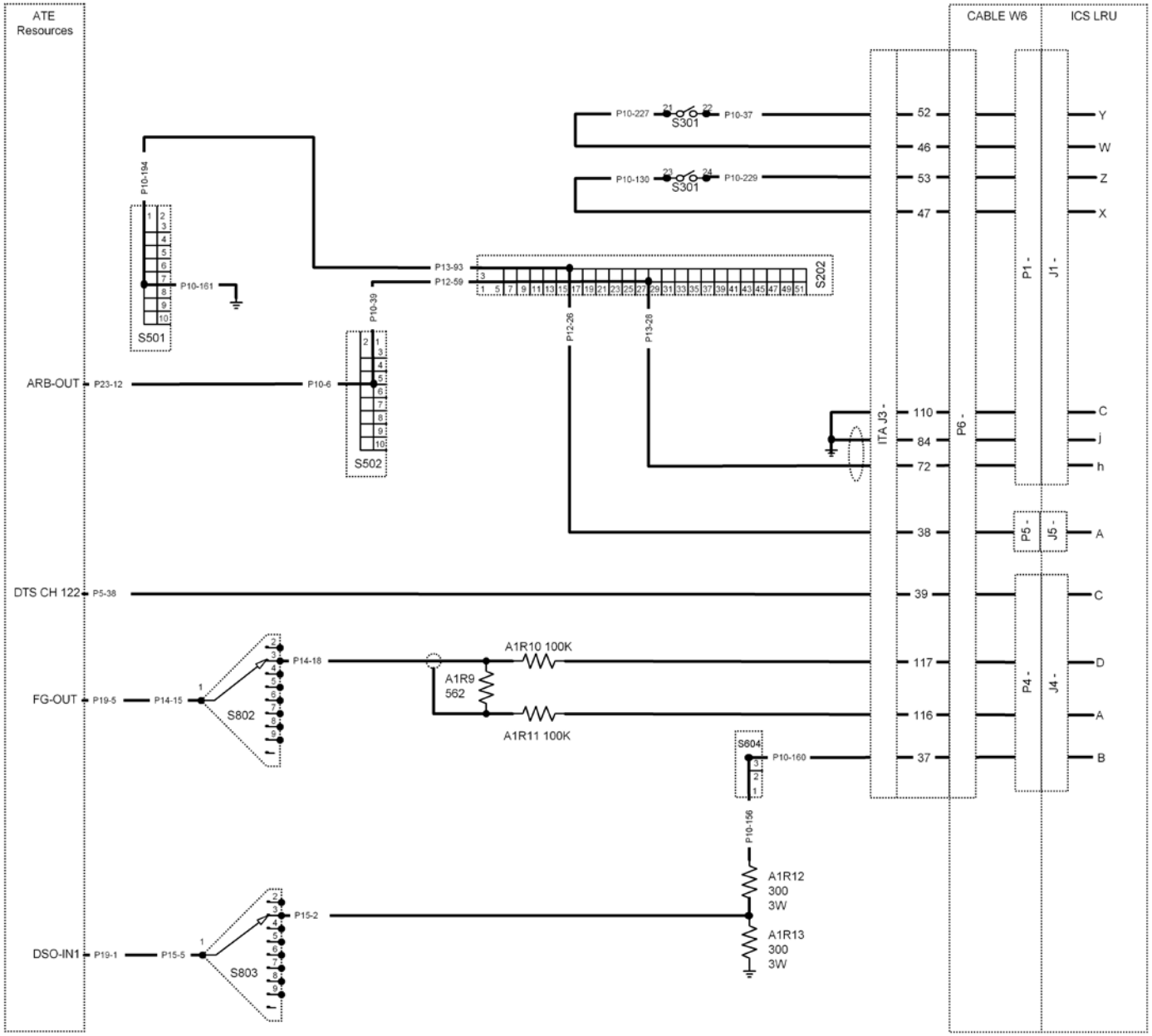
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P10-227
S301
P10-37
P10-130
S301
P10-229
52
46
53
47
Y
W
Z
X
P10-194
P10-161
S501
P13-93
P12-59
S202
P10-39
P12-26
P13-28
S502
ARB-OUT
P23-12
P10-6
ITA J3
110
84
72
C
j
h
P6
P1
J1
P5
J5
38
A
DTS CH 122
P5-38
39
C
P14-18
A1R10 100K
A1R9
562
A1R11 100K
117
D
FG-OUT
P19-5
P14-15
S802
116
A
P4
J4
S604
P10-160
37
B
P10-156
A1R12
300
3W
A1R13
300
3W
P15-2
DSO-IN1
P19-1
P15-5
S803

Step 506 Low-Pass Filter (3dB Rolloff Point) Test

This step verifies that the 3dB roll-off (1/2 power) point of the Low-Pass filter circuit on CCA A1 is within the specified range of 2.5 to 4.0 KHz. With the same stimulus as in Step 501 applied and the front panel VOLUME control, R1 adjusted for an output reading of 19.0 to 20.5 Vpp (38 to 41 Vpp at UUT output J4-B) at 1.0 KHz, the output frequency of the Function Generator (applied at J4-D) is adjusted to 2.3 KHz and a reference output reading is made and stored. Then the frequency is swept from 2.4 KHz to a maximum of 4.2 KHz (in 100 Hz increments), until the 3dB rolloff point is detected. This point is that at which the amplitude is less than 0.707 times that of the reference reading at 2.3 KHz.

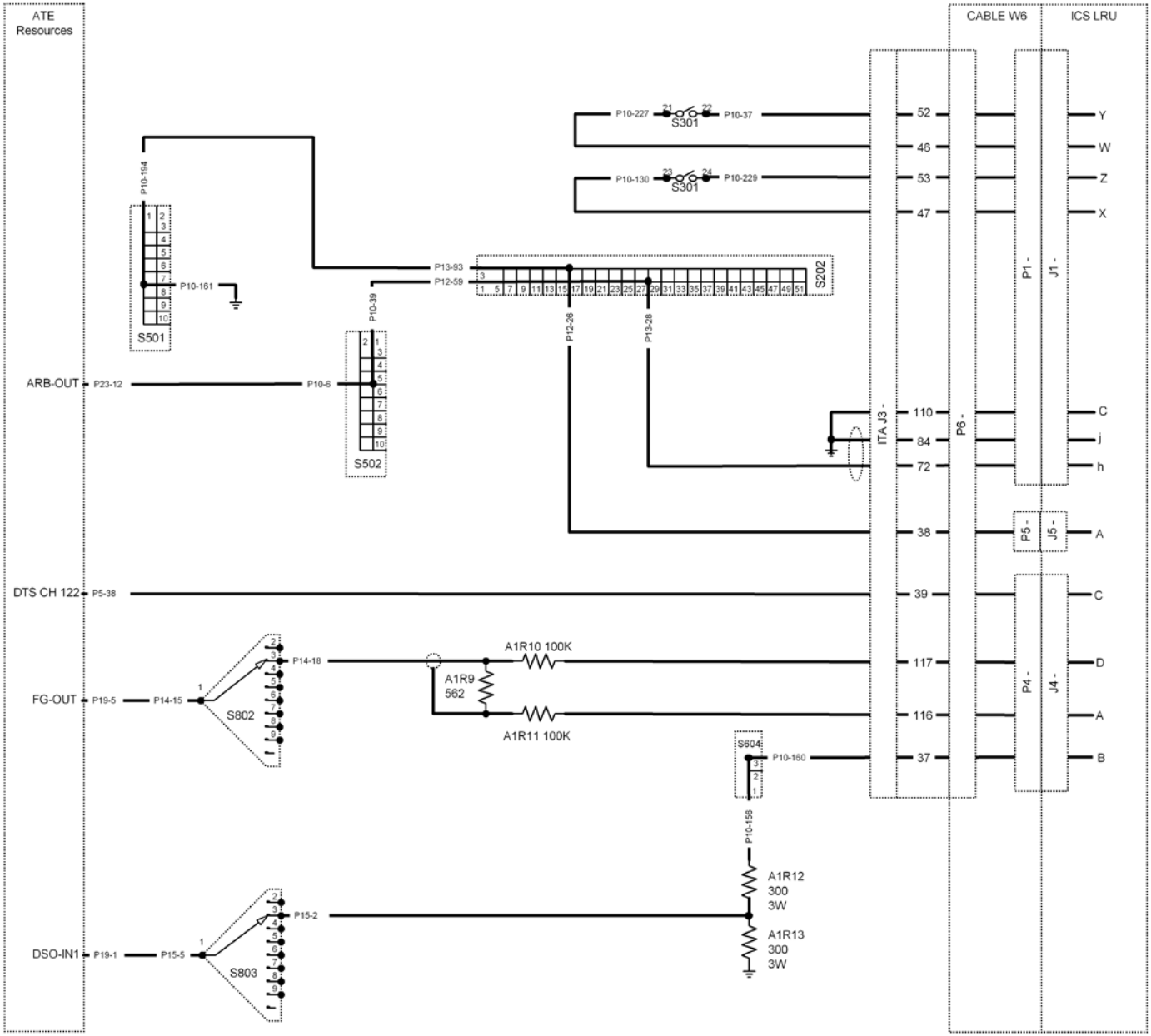
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P10-227
S301
P10-37
P10-130
S301
P10-229
52
46
53
47
Y
W
Z
X
P10-194
P10-161
S501
P13-93
P12-59
S202
P10-39
P12-26
P13-28
S502
ARB-OUT
P23-12
P10-6
ITA J3
110
84
72
C
j
h
P6
P1
J1
P5
J5
38
A
DTS CH 122
P5-38
39
C
P14-18
A1R10 100K
A1R9
562
A1R11 100K
117
116
D
A
FG-OUT
P19-5
P14-15
S802
P4
J4
S604
P10-160
37
B
P10-156
A1R12
300
3W
A1R13
300
3W
P15-2
DSO-IN1
P19-1
P15-5
S803

Step 507 High-Pass Filter (3dB Rolloff Point) Test

This step verifies that the 3dB roll-off (1/2 power) point of the High-Pass filter circuit on CCA A1 is within the specified range of 150 to 400 Hz. With the same stimulus as in Step 501 applied and the front panel VOLUME control, R1 adjusted for an output reading of 19.0 to 20.5 Vpp (38 to 41 Vpp at UUT output J4-B) at 1.0 KHz, the output frequency of the Function Generator (applied at J4-D) is adjusted to 430 Hz and a reference output reading is made and stored. Then the frequency is swept down from 420 KHz to a minimum of 140 Hz (in 10 Hz increments), until the 3dB rolloff point is detected. This point is that at which the amplitude is less than 0.707 times that of the reference reading at 430 Hz.

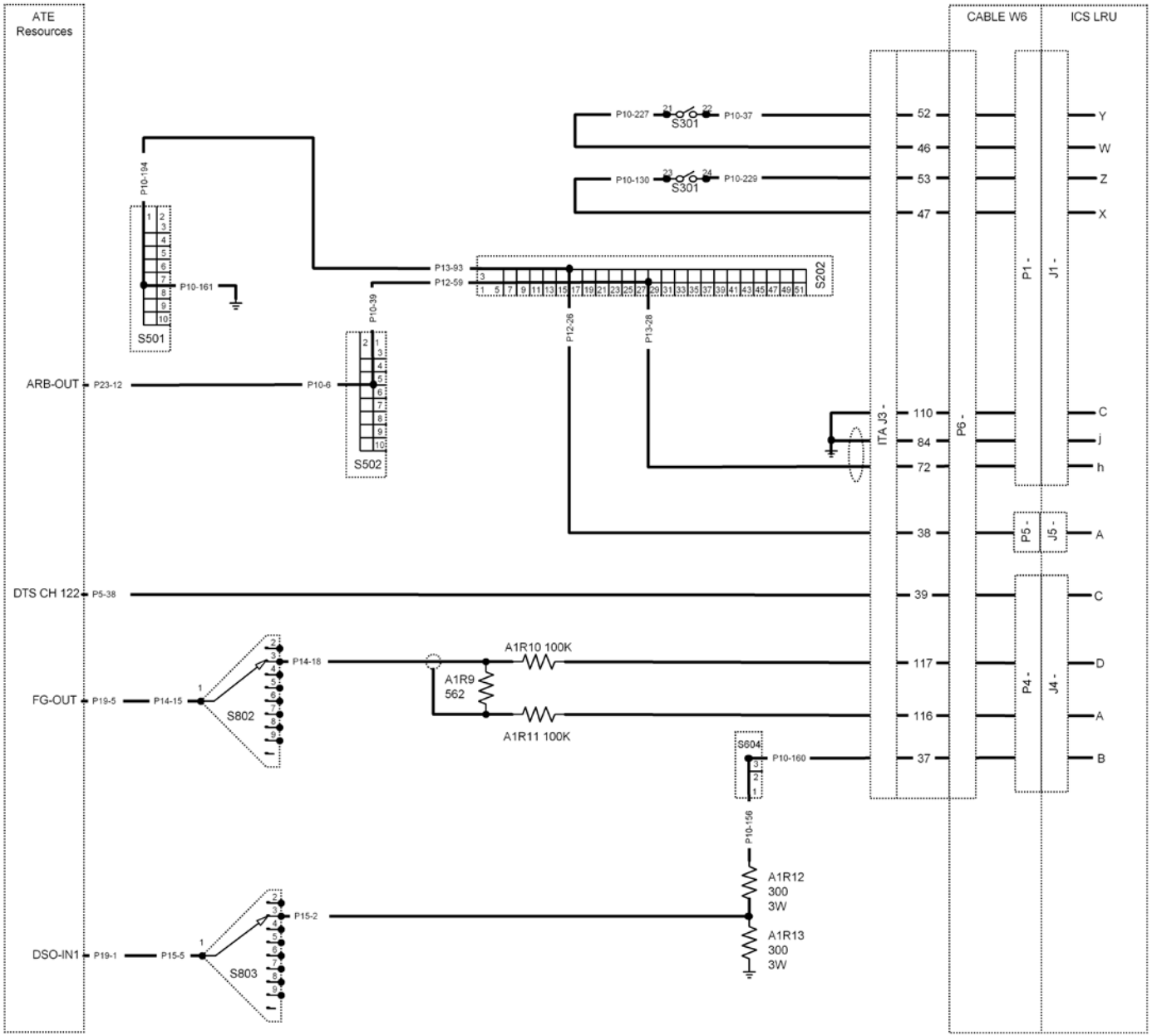
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P10-227
S301
P10-37
P10-130
S301
P10-229
52
46
53
47
Y
W
Z
X
P10-194
P13-93
P12-59
S202
P10-161
S501
P10-39
P12-26
P13-28
P1 -
J1 -
ARB-OUT
P23-12
P10-6
S502
ITA J3 -
110
84
72
P6 -
C
j
h
38
P5 -
J5 -
A
DTS CH 122
P5-38
39
C
P14-18
A1R10 100K
A1R9
562
A1R11 100K
117
116
D
A
FG-OUT
P19-5
P14-15
S802
S604
P10-160
37
B
P10-156
A1R12
300
3W
A1R13
300
3W
P15-2
DSO-IN1
P19-1
P15-5
S803
P4 -
J4 -

Step 508 Flatness Test

This step verifies that the gain of the CVSD #1 channel is flat (within 3 dB) across the specified band of 400 Hz to 2.5 KHz. With the same stimulus as in Step 501 applied and the front panel VOLUME control, R1 adjusted for an output reading of 19.0 to 20.5 Vpp (38 to 41 Vpp at UUT output J4-B) at 1.0 KHz, the output frequency of the Function Generator (applied at J4-D) is swept from 400 Hz to 2.5 KHz (in 100 Hz increments). The amplitude at each frequency is stored. The procedure then locates the highest amplitude (Vmax) point and the lowest amplitude (Vmin) point. Overall flatness (in decibels) is calculated by the formula: 20*Log(Vmax/Vmin). The tolerance is based upon +/-3 dB flatness allowed for the A1 and A5 CCAs each. The Root-Sum-Square (RSS) calculation is used to obtain the upper-limit of 4.24 db (the square-root of 18).

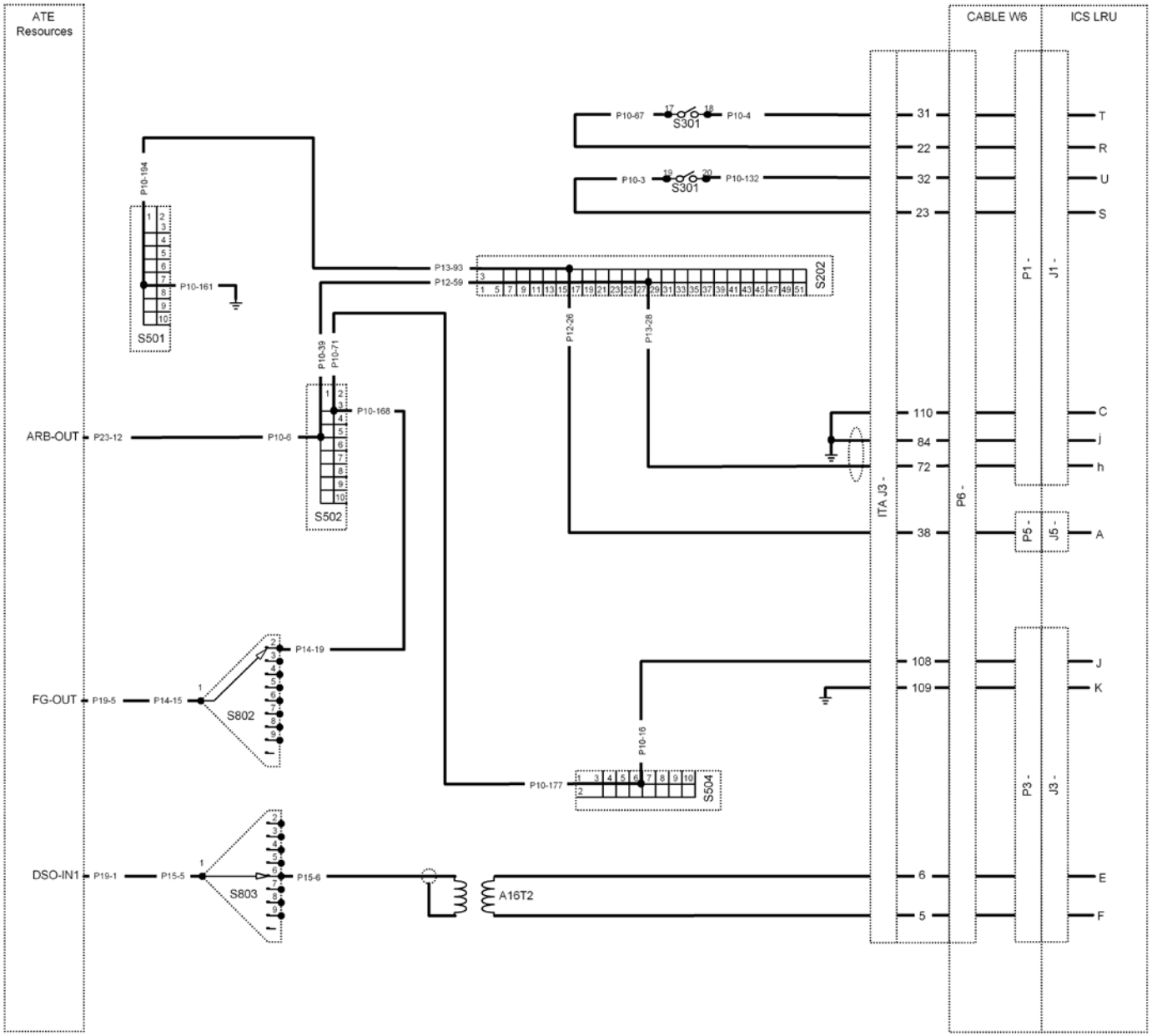
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P10-227
S301
P10-37
P10-130
S301
P10-229
52
46
53
47
Y
W
Z
X
P10-194
P10-161
S501
P13-93
P12-59
S202
P10-39
P12-26
P13-26
S502
ARB-OUT
P23-12
P10-6
ITA J3 -
P6 -
P1 -
J1 -
110
84
72
C
j
h
P5 -
J5 -
38
A
DTS CH 122
P5-38
39
C
P14-18
A1R10 100K
A1R9
562
A1R11 100K
FG-OUT
P19-5
P14-15
S802
117
116
D
A
P4 -
J4 -
S604
P10-160
37
B
P10-156
A1R12
300
3W
A1R13
300
3W
P15-2
DSO-IN1
P19-1
P15-5
S803

Step 509 CVSD 2 Radio Audio Amplitude Test

This step verifies the overall gain through CVSD channel 2 (CCA A2) on AN/MIQ(V)2 and (V)3 LRUs. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, a 10 Vpp sine-wave is applied from the Function Generator to the CCA A2 'RADIO IN' input at J3-J. Because of the 50-ohm input impedance of the Function Generator only 5 Vpp is programmed, but during execution this voltage is doubled before it is applied. The differential CVSD digital output of CCA A2 (J1-R/J1-S) is looped back to the CVSD input (J1-T/J1-U). The Digitizing Oscilloscope is used to verify the RADIO OUT (J3-F/J3-E) level is greater than 0.02828 Vpp via ITA 1:20 step-up audio transformer, T2. This meets the specified 0.5 mVRMS minimum tolerance for this test.

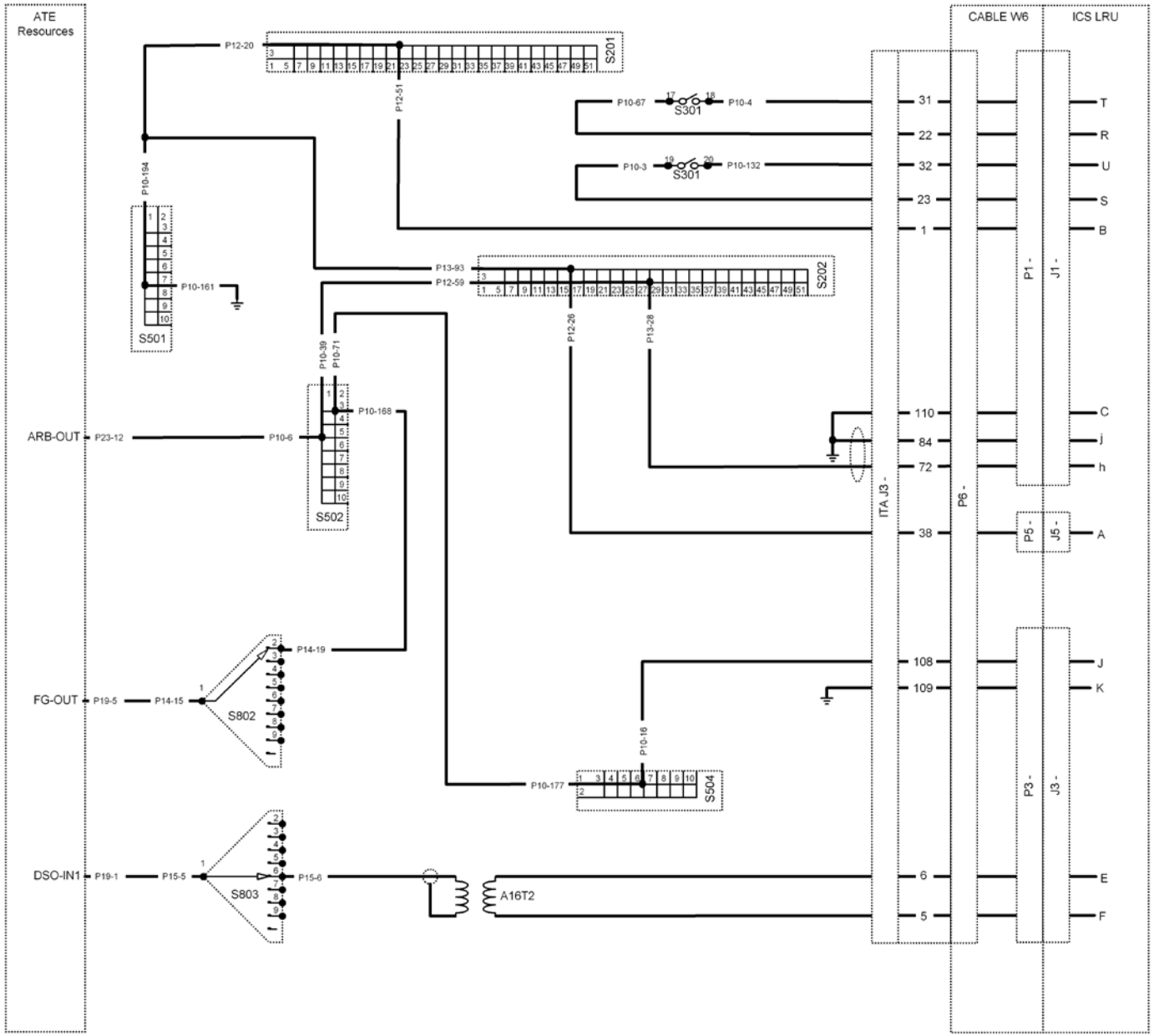
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P10-67
S301
P10-4
P10-3
S301
P10-132
P10-194
P10-161
S501
P13-93
P12-59
S202
P12-26
P13-28
P10-39
P10-71
P10-168
S502
ARB-OUT
P23-12
P10-6
P14-19
FG-OUT
P19-5
P14-15
S802
P10-16
P10-177
S504
DSO-IN1
P19-1
P15-5
S803
P15-6
A16T2
ITA J3 -
P6 -
P1 -
J1 -
P5 -
J5 -
P3 -
J3 -
31
22
32
23
110
84
72
38
108
109
6
5
T
R
U
S
C
j
h
A
J
K
E
F

Step 510 MIC-OUT Level Control Test

This step verifies the gain through CVSD channel 2 (CCA A2) on AN/MIQ(V)2 and (V)3 LRUs is increased by at least a factor of four (4) times when the 'MIC OUT LEVEL CONT' is set LO. With the same stimulus as in Step 509 applied, J1-B is switched to GND. The Digitizing Oscilloscope is used to verify the RADIO OUT(J3-F/J3-E) level is greater than four (4) times the value measured in Step 509 via ITA 1:20 step-up audio transformer, T2.

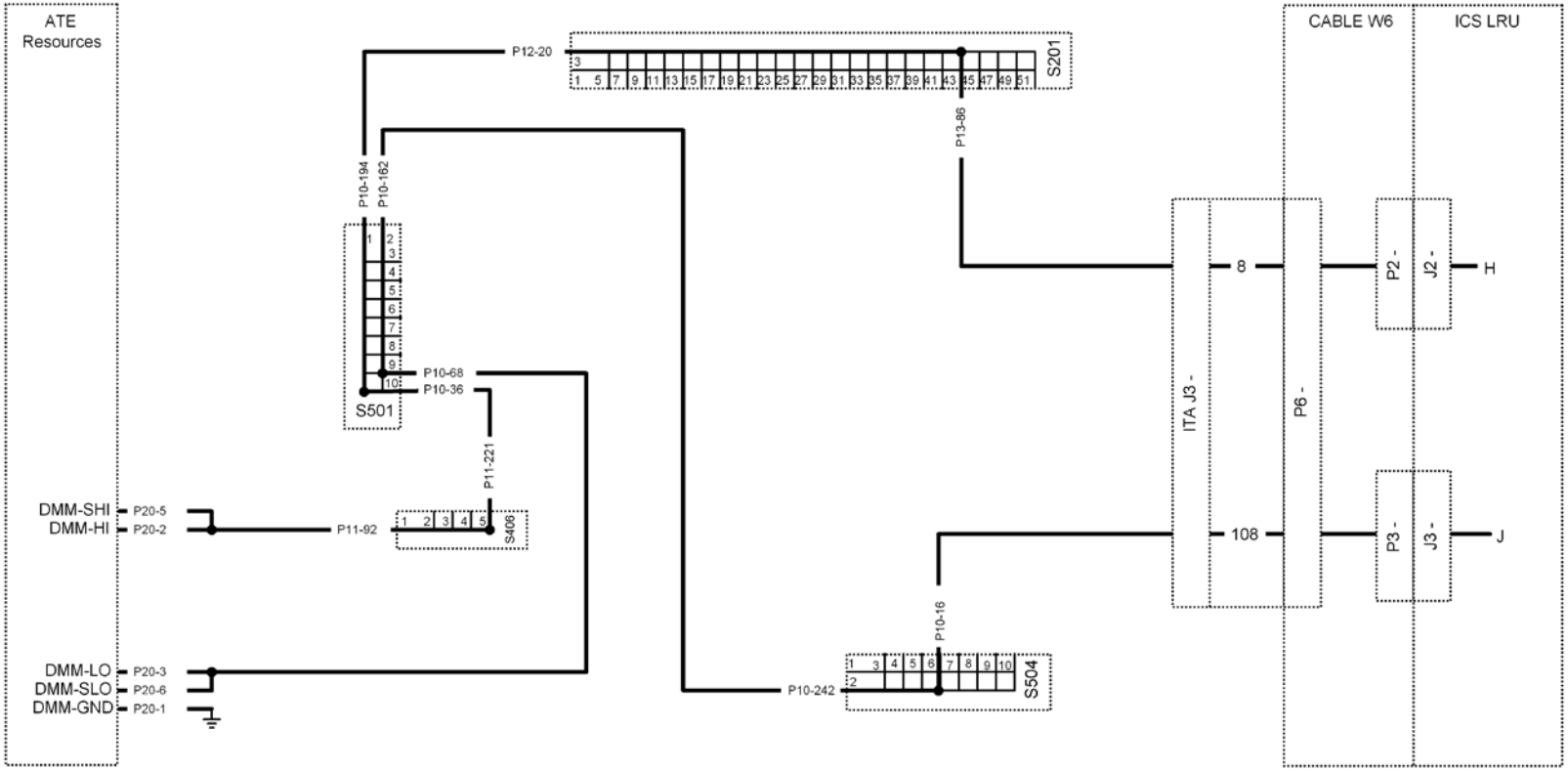
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P12-20
S201
P12-51
P10-67
S301
P10-4
P10-3
S301
P10-132
P10-194
P10-161
S501
P13-93
P12-59
S202
P12-26
P13-28
P10-39
P10-71
P10-168
S502
ARB-OUT
P23-12
P10-6
FG-OUT
P19-5
P14-15
S802
P14-19
P10-177
P10-16
S504
DSO-IN1
P19-1
P15-5
S803
P15-6
A16T2
ITA J3 -
P6 -
P1 -
J1 -
P5 -
J5 -
P3 -
J3 -
31
22
32
23
1
110
84
72
38
108
109
6
5
T
R
U
S
B
C
j
h
A
J
K
E
F

Step 511 Crew Intercom Input Attenuation (J2-H/J3-J) Test

This step, in conjunction with steps 512 and 513, verifies the input attenuation circuit at 'Crew INTERCOM IN', J2-H/J2-G of CVSD channel 2 (CCA A2) on AN/MIQ(V)2 and (V)3 LRUs. The DMM is used to verify between 1350 ohms and 1650 ohms (nominal 1500 ohms) across J2-H/J3-J.

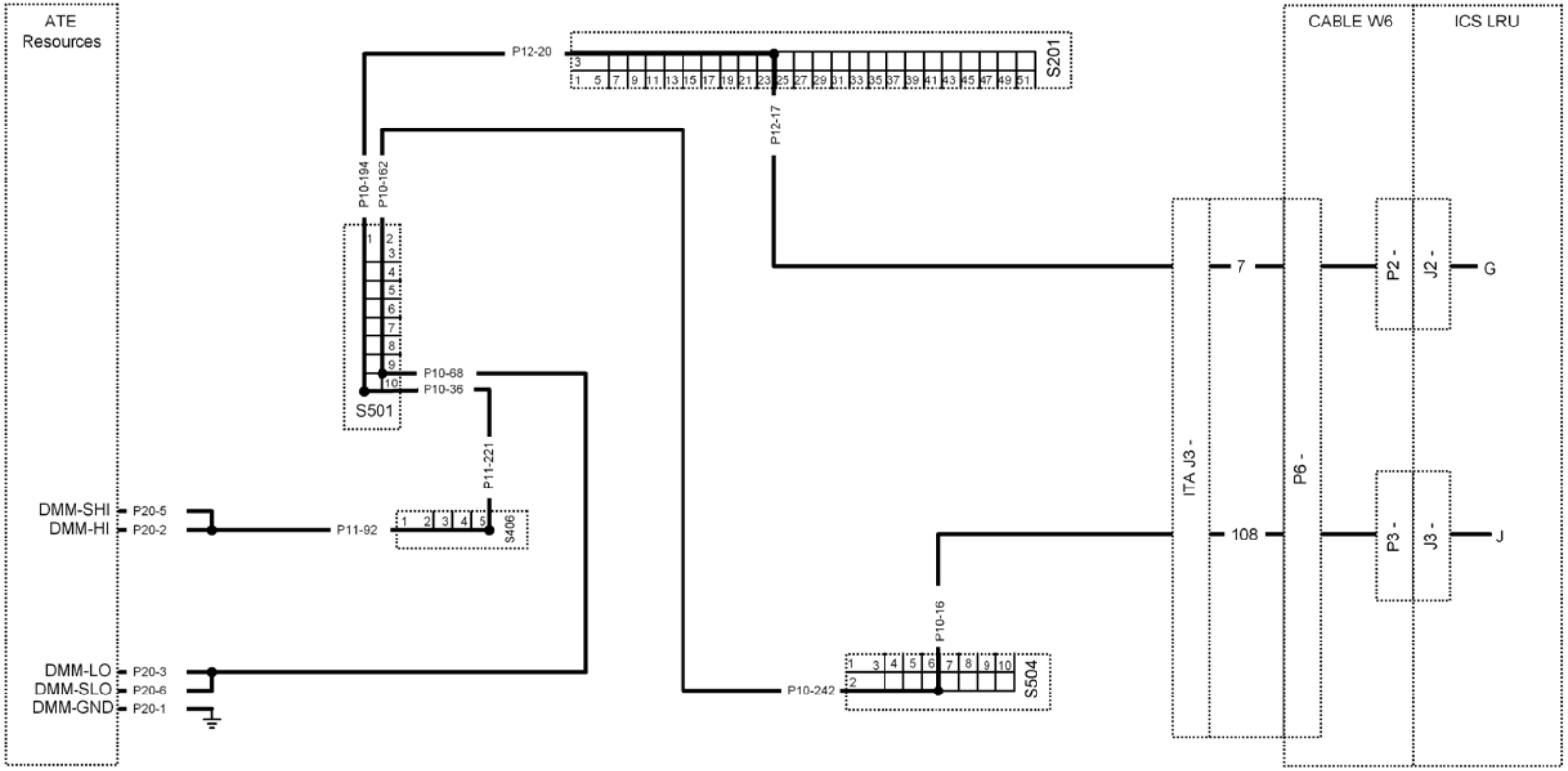
Connection Path as follows:


ATE
Resources
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
P11-221
S406
P10-194
P10-162
P10-68
P10-36
S501
P12-20
S201
P13-86
P10-16
P10-242
S504
CABLE W6
ICS LRU
ITA J3 -
P6 -
8
108
P2 -
J2 -
H
P3 -
J3 -
J

Step 512 Crew Intercom Input Attenuation (J2-G/J3-J) Test

This step, in conjunction with steps 511 and 513, verifies the input attenuation circuit at 'Crew INTERCOM IN', J2-H/J2-G of CVSD channel 2 (CCA A2) on AN/MIQ(V)2 and (V)3 LRUs. The DMM is used to verify between 1850 ohms and 2150 ohms (nominal 2000 ohms) across J2-G/J3-J.

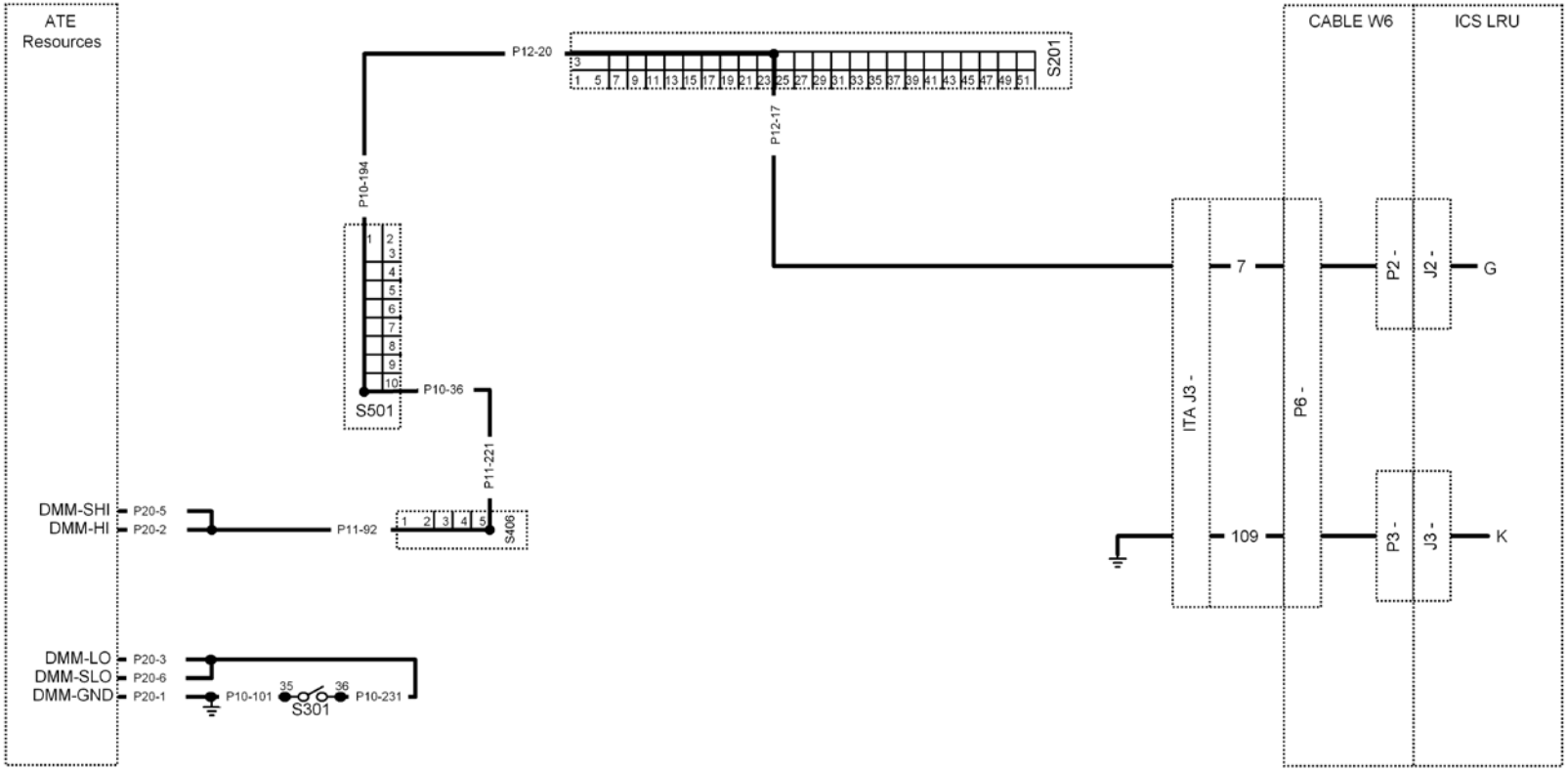
Connection Path as follows:


ATE
Resources
DMM-SHI
DMM-HI
DMM-LO
DMM-SLO
DMM-GND
P20-5
P20-2
P20-3
P20-6
P20-1
P11-92
P11-221
S406
P10-194
P10-162
P10-68
P10-36
S501
P12-20
P12-17
S201
P10-242
P10-16
S504
CABLE W6
ICS LRU
ITA J3 -
P6 -
7
108
P2 -
J2 -
G
P3 -
J3 -
J

Step 513 Crew Intercom Input Attenuation (J2-G/J3-K) Test

This step, in conjunction with steps 511 and 512, verifies the input attenuation circuit at 'Crew INTERCOM IN', J2-H/J2-G of CVSD channel 2 (CCA A2) on AN/MIQ(V)2 and (V)3 LRUs. The DMM is used to verify between 1350 ohms and 1650 ohms (nominal 1500 ohms) across J2-G/J3-K.

Connection Path as follows:


ATE
Resources
P12-20
S201
P12-17
P10-194
S501
P10-36
P11-221
DMM-SHI
DMM-HI
P20-5
P20-2
P11-92
S406
DMM-LO
DMM-SLO
DMM-GND
P20-3
P20-6
P20-1
P10-101
S301
P10-231
CABLE W6
ICS LRU
ITA J3 -
P6 -
7
109
P2 -
J2 -
G
P3 -
J3 -
K

Step 514 CVSD 2 Loopback Test

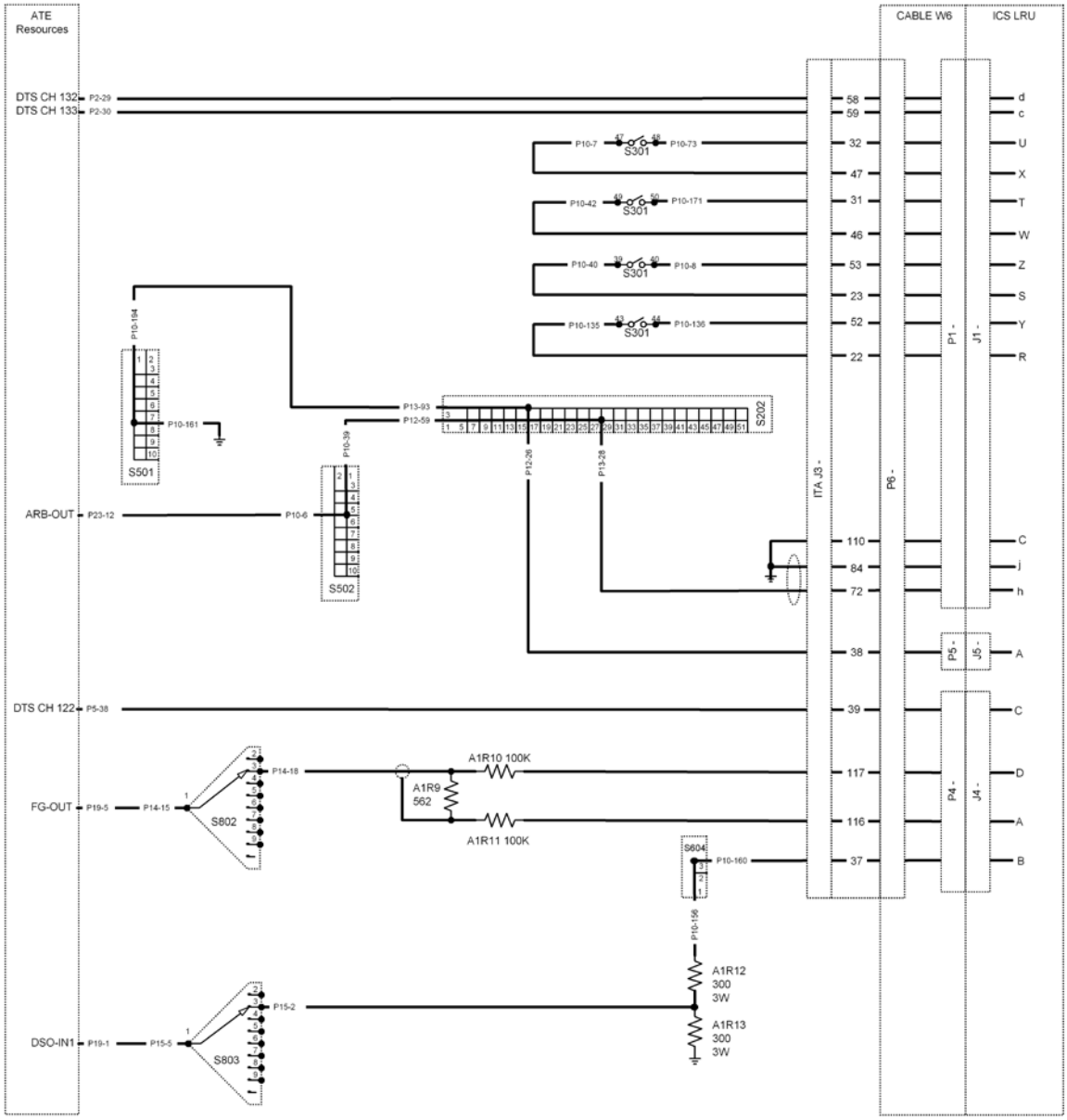
This step verifies the functionality of the CVSD 2 loopback (self-test) function. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, a 10 Vpp sine-wave is applied from the Function Generator through the ITA attenuator circuit (1A1R9/1A1R10/1A1R11) to the CCA A1 'MIC IN' input at J4-D/J4-A. Because of the 50-ohm input impedance of the Function Generator only 5 Vpp is programmed, but during execution this voltage is doubled before it is applied. CVSD operation is enabled by applying a logic LO at the RADKEY keyline input at J4-C. The front panel VOLUME control, R1 is set to fully clockwise (maximum gain). The differential CVSD digital output of CCA A1 (J1-W/J1-X) is connected to the CVSD digital input (J1-T/J1-U) of CCA A2. The DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a CVSD LOOPBACK (self-test) command (B’10001101000’) as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

The CVSD digital output of CCA A2 (J1-R/J1-S) is connected to the CVSD digital input (J1-Y/J1-Z) of CCA A1. The Digitizing Oscilloscope is used to verify the HEADSET audio output (J4-B) level is greater than 5 Vpp. The actual reading will be one-half the UUT output level due to the effect of the ITA voltage divider made up of 1A1R12 and 1A1R13 (each 300 ohm and 3 W), which also serves as a 600 ohm load specified for the HEADSET audio output. Upon completion of the test, the DTS is used to then send a differential CLEAR-F command (see Step 102) on 'Serial Data In', J1-d(+)/J1-c(-), to remove the CVSD LOOPBACK command.

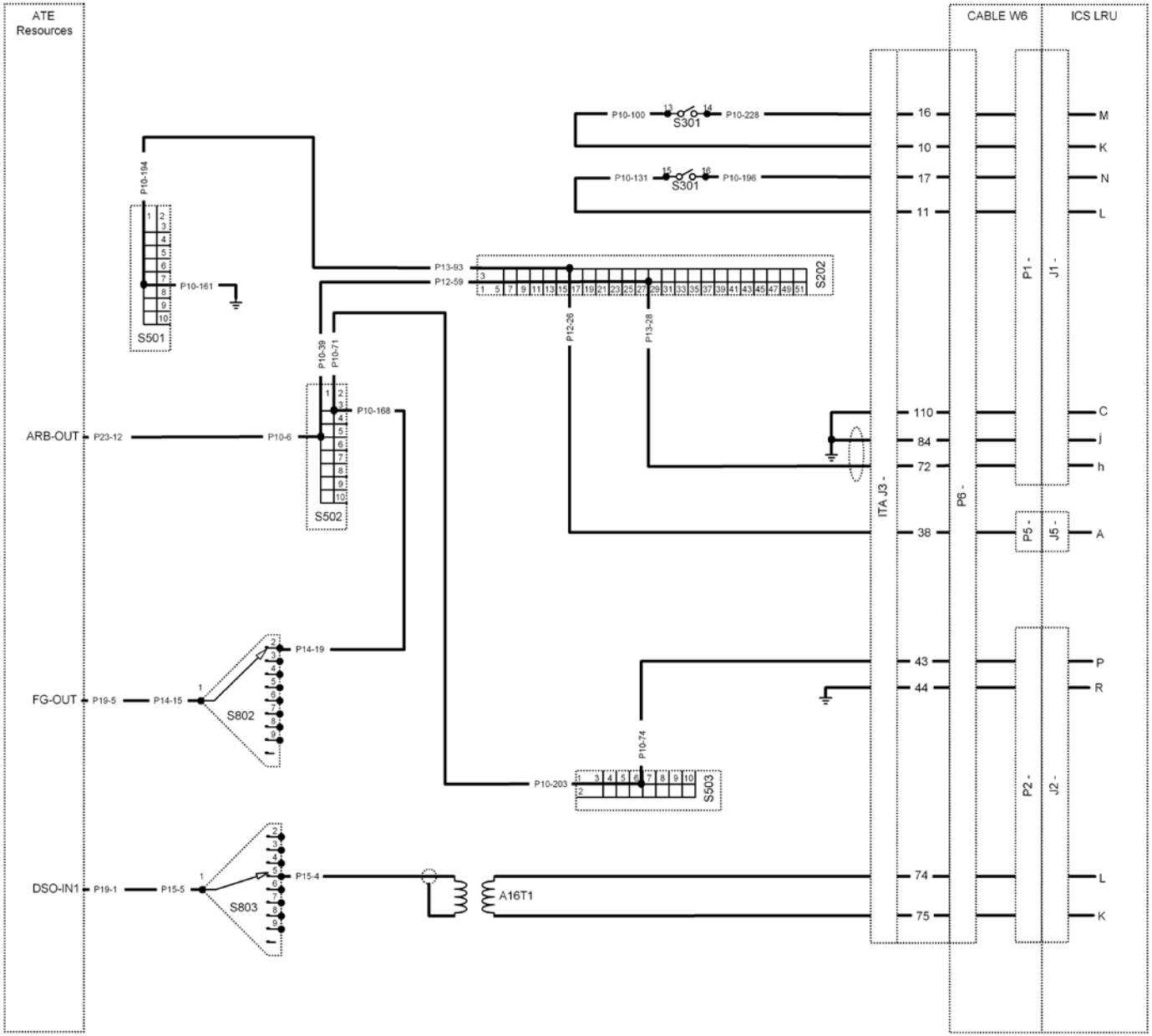
Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
DTS CH 132 P2-29
DTS CH 133 P2-30
P10-7 S301 P10-73
P10-42 S301 P10-171
P10-40 S301 P10-8
P10-135 S301 P10-136
P10-194
P10-161
S501
P13-93
P12-59
S202
P12-26
P13-28
P10-39
S502
ARB-OUT P23-12 P10-6
ITA /J3 -
P6 -
P1 -
J1 -
P5 -
J6 -
P4 -
J4 -
58 59 32 47 31 46 53 23 52 22 110 84 72 38 39 117 116 37
d c U X T W Z S Y R C J h A C D A B
DTS CH 122 P5-38
FG-OUT P19-5 P14-15 S802 P14-18
A1R10 100K
A1R9 562
A1R11 100K
S604
P10-160
P10-156
A1R12 300 3W
A1R13 300 3W
DSO-IN1 P19-1 P15-5 S803 P15-2

Step 515 CVSD 3 Radio Audio Amplitude Test

This step verifies the overall gain through CVSD channel 3 (CCA A3) on AN/MIQ(V)3 LRUs. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h (see Step 501), a 10 Vpp sine-wave is applied from the Function Generator to the CCA A3 'RADIO IN' input at J2-P. Because of the 50-ohm input impedance of the Function Generator only 5 Vpp is programmed, but during execution this voltage is doubled before it is applied. The differential CVSD digital output of CCA A3 (J1-L/J1-K) is looped back to the CVSD input (J1-M/J1-N). The Digitizing Oscilloscope is used to verify the RADIO OUT (J2-L/J2-K) level is greater than 0.02828 Vpp via ITA 1:20 step-up audio transformer, T1. This meets the specified 0.5 mVRMS minimum tolerance for this test.

Connection Path as follows:


ATE Resources
CABLE W6
ICS LRU
P10-100
S301
P10-228
P10-131
S301
P10-196
16
10
17
11
M
K
N
L
P10-194
P10-161
S501
P13-93
P12-59
S202
P12-26
P13-28
P10-39
P10-71
P10-168
ARB-OUT
P23-12
P10-6
S502
110
84
72
C
j
h
ITA J3 -
P6 -
P1 -
J1 -
P5 -
J5 -
38
A
P14-19
FG-OUT
P19-5
P14-15
S802
43
44
P
R
P10-74
P10-203
S503
P2 -
J2 -
DSO-IN1
P19-1
P15-5
S803
P15-4
A16T1
74
75
L
K

Step 516 CVSD 3 Loopback Test

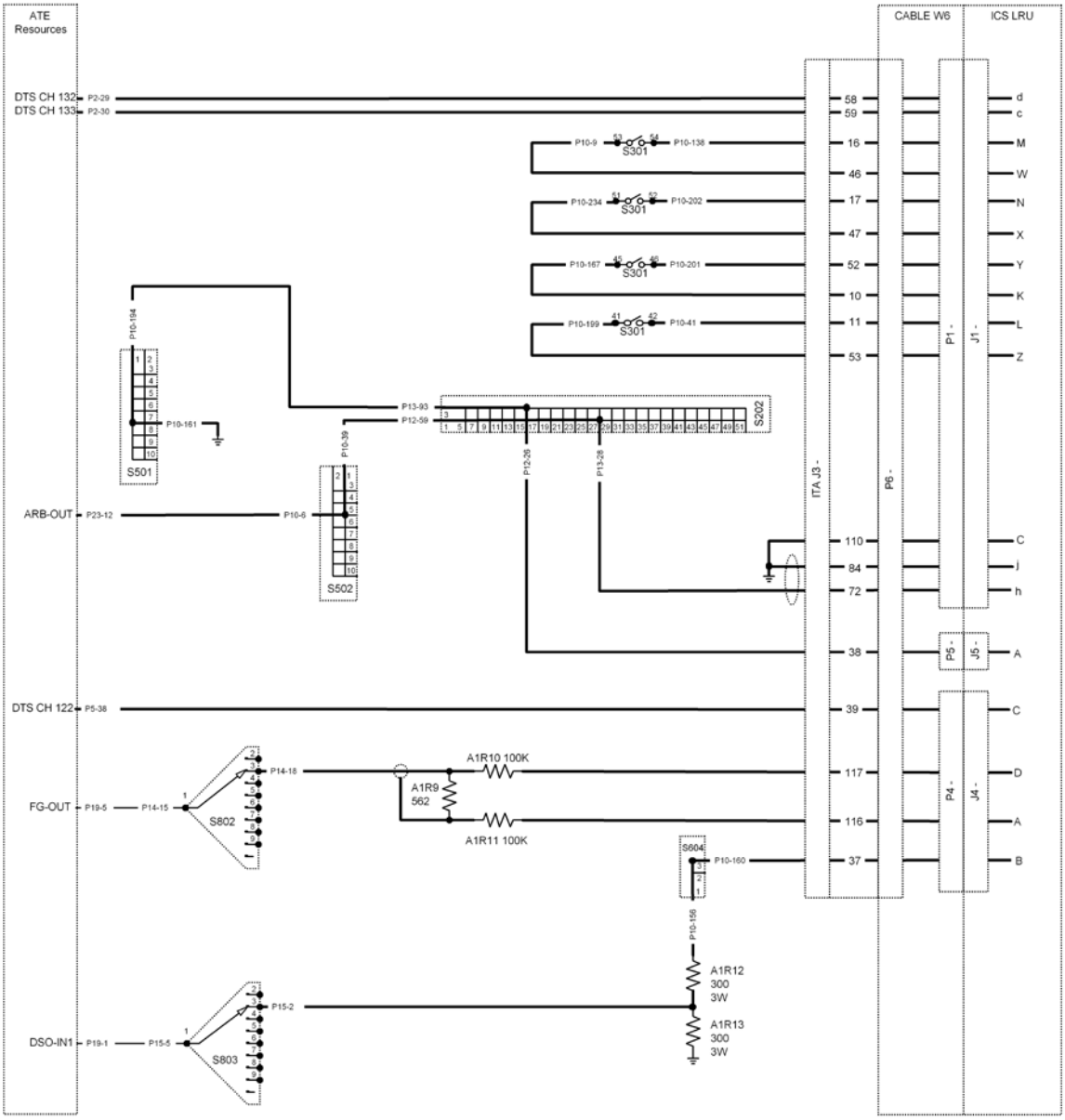
This step verifies the functionality of the CVSD 3 loopback (self-test) function. With a differential (4.0 Vpp) 32 KHz clock applied at J1-j/J1-h, a 10 Vpp sine-wave is applied from the Function Generator through the ITA attenuator circuit (1A1R9/1A1R10/1A1R11) to the CCA A1 'MIC IN' input at J4-D/J4-A. Because of the 50-ohm input impedance of the Function Generator only 5 Vpp is programmed, but during execution this voltage is doubled before it is applied. CVSD operation is enabled by applying a logic LO at the RADKEY keyline input at J4-C. The front panel VOLUME control, R1 is set to fully clockwise (maximum gain). The differential CVSD digital output of CCA A1 (J1-W/J1-X) is connected to the CVSD digital input (J1-M/J1-N) of CCA A3. The DTS is used to output a differential serial data command at 'Serial Data In', J1-d(+)/J1-c(-) which is decoded by the A4 CCA as a CVSD LOOPBACK (self-test) command (B’10001101000’) as follows:

Stimulate: B'01' using DTS for 0.5mSec. [START Bit]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 0]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 1]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 2]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 3]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 4]
Stimulate: B'10' using DTS for 0.5mSec. [DATA Bit 5]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 6]
Stimulate: B'01' using DTS for 0.5mSec. [DATA Bit 7]
Stimulate: B'01' using DTS for 0.5mSec. [PARITY Bit (Set for ODD)]
Stimulate: B'10' using DTS for 0.5mSec. [STOP Bit]

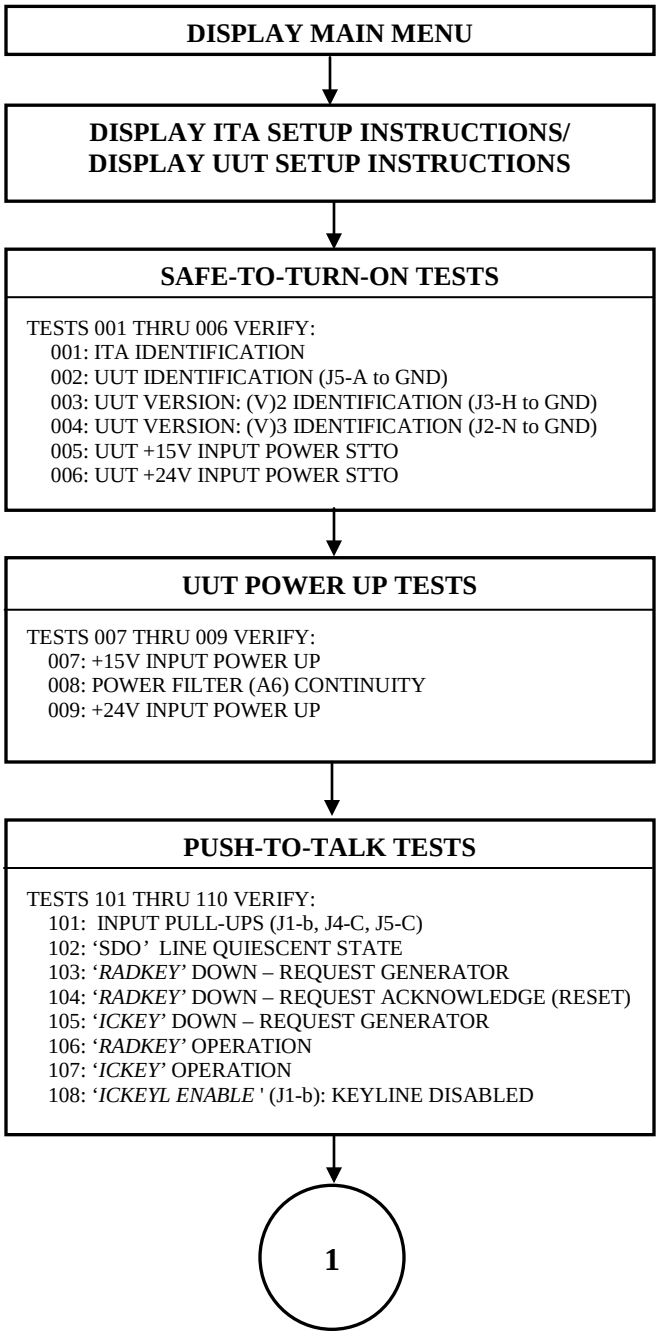
NOTE: 0.5mSec is 16 ‘32KHz CLOCK’ periods.

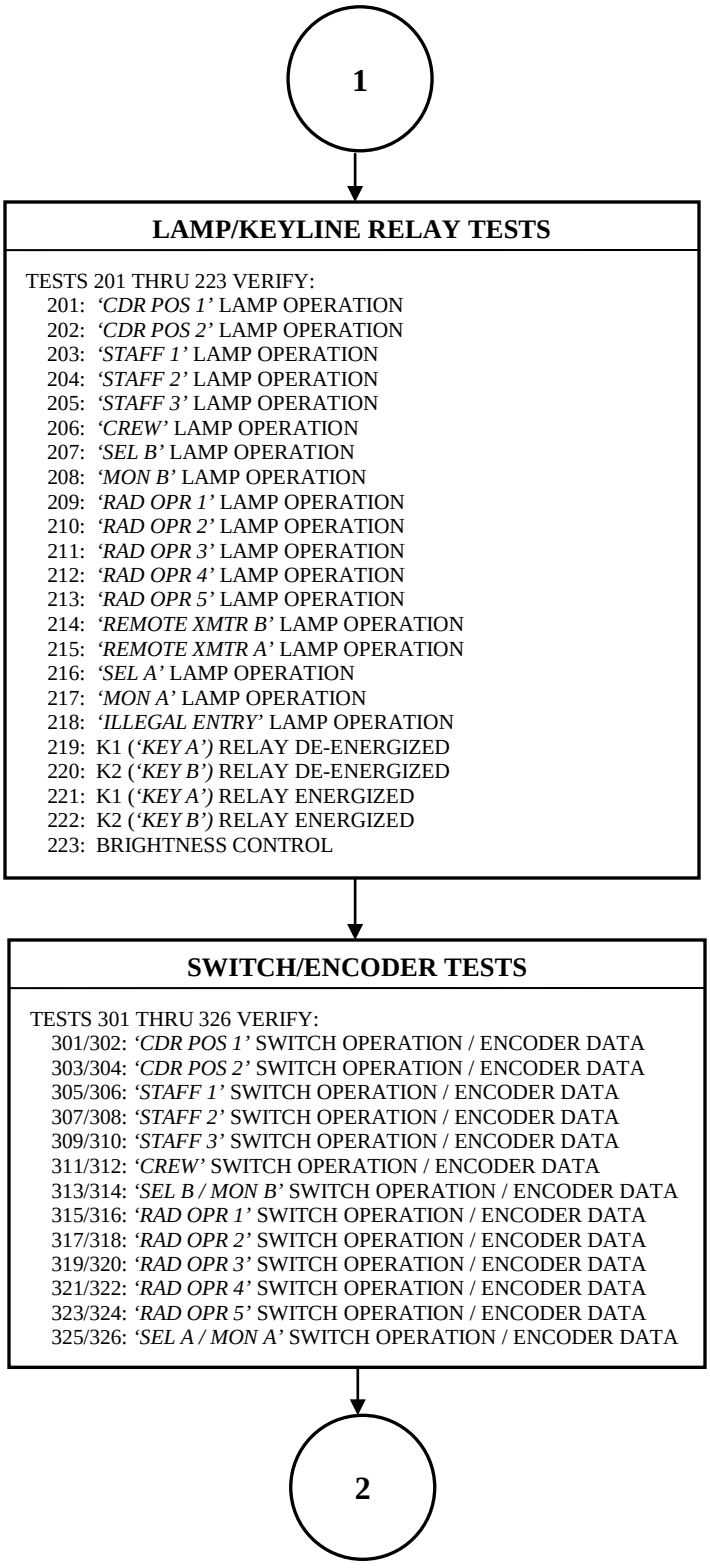
The CVSD digital output of CCA A3 (J1-K/J1-L) is connected to the CVSD digital input (J1-Y/J1-Z) of CCA A1. The Digitizing Oscilloscope is used to verify the HEADSET audio output (J4-B) level is greater than 5 Vpp. The actual reading will be one-half the UUT output level due to the effect of the ITA voltage divider made up of 1A1R12 and 1A1R13 (each 300 ohm and 3 W), which also serves as a 600 ohm load specified for the HEADSET audio output.

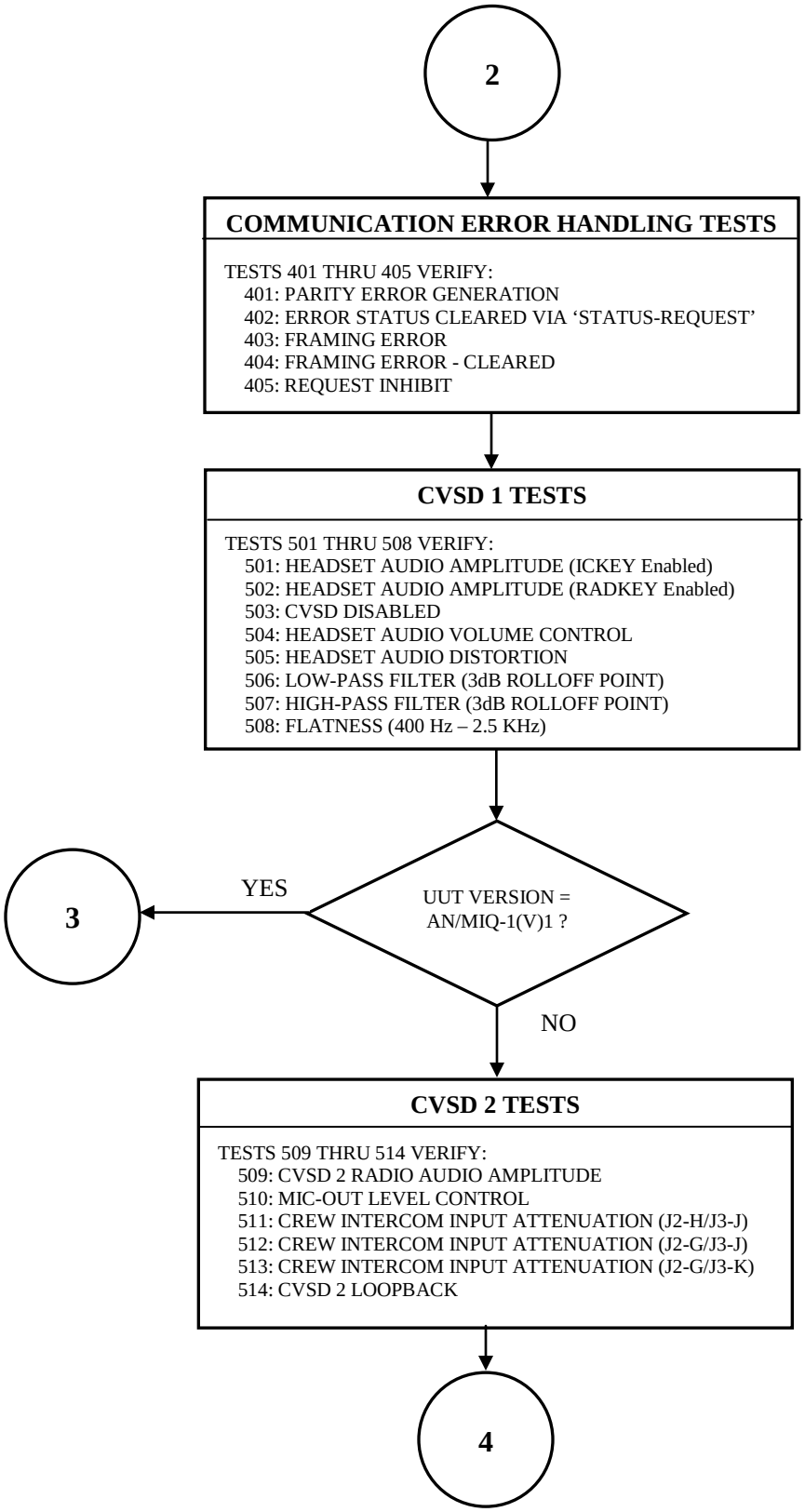
Connection Path as follows:

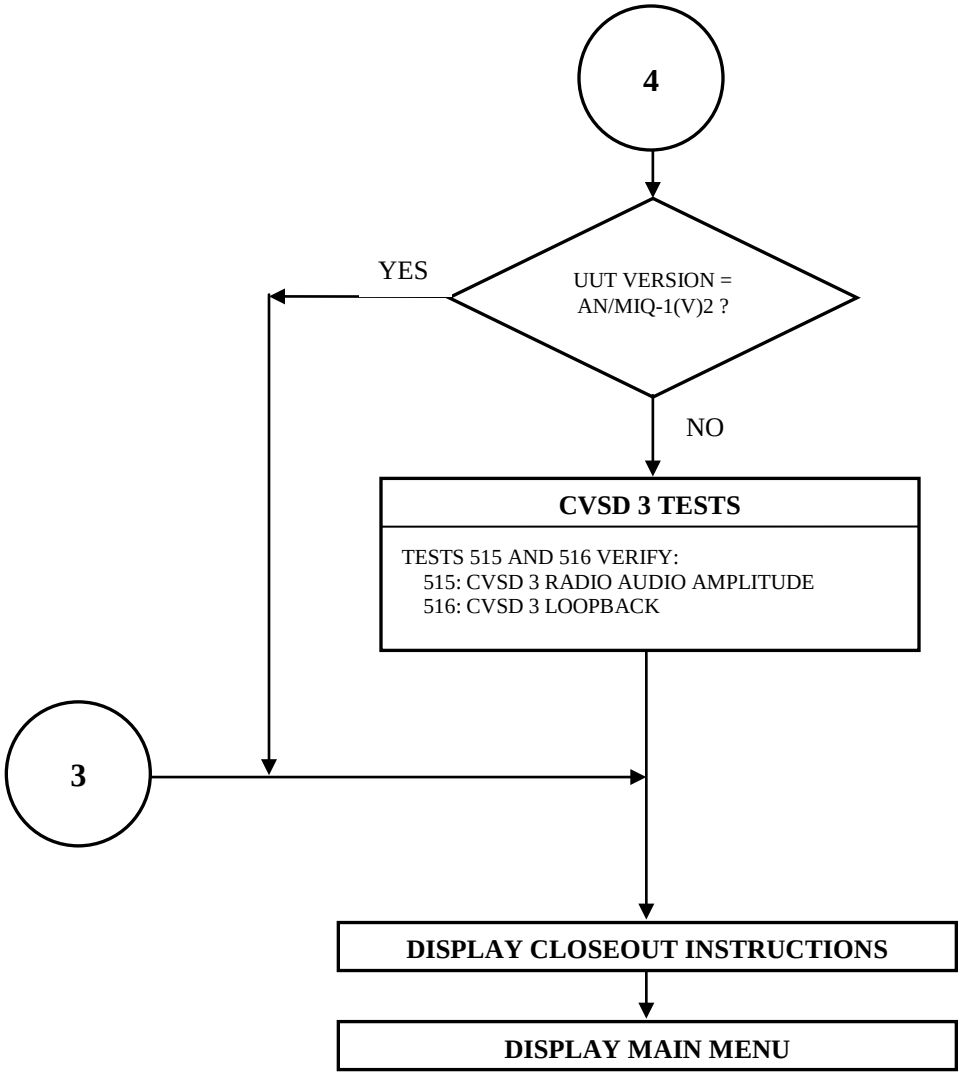

ATE Resources
CABLE W6
ICS LRU
DTS CH 132 P2-29
DTS CH 133 P2-30
P10-9
S301
P10-138
P10-234
P10-202
P10-167
P10-201
P10-199
P10-41
P10-194
S501
P10-161
P13-93
P12-59
S202
P10-39
S502
ARB-OUT P23-12
P10-6
P12-26
P13-28
ITA J3 -
P6 -
P1 -
J1 -
P5 -
J5 -
P4 -
J4 -
DTS CH 122 P5-38
FG-OUT P19-5
P14-15
S802
P14-18
A1R10 100K
A1R9
562
A1R11 100K
S604
P10-160
P10-156
A1R12
300
3W
A1R13
300
3W
DSO-IN1 P19-1
P15-5
S803
P15-2

FUNCTIONAL FLOW CHART (FFC)




1
LAMP/KEYLINE RELAY TESTS
TESTS 201 THRU 223 VERIFY:
201: 'CDR POS 1' LAMP OPERATION
202: 'CDR POS 2' LAMP OPERATION
203: 'STAFF 1' LAMP OPERATION
204: 'STAFF 2' LAMP OPERATION
205: 'STAFF 3' LAMP OPERATION
206: 'CREW' LAMP OPERATION
207: 'SEL B' LAMP OPERATION
208: 'MON B' LAMP OPERATION
209: 'RAD OPR 1' LAMP OPERATION
210: 'RAD OPR 2' LAMP OPERATION
211: 'RAD OPR 3' LAMP OPERATION
212: 'RAD OPR 4' LAMP OPERATION
213: 'RAD OPR 5' LAMP OPERATION
214: 'REMOTE XMTR B' LAMP OPERATION
215: 'REMOTE XMTR A' LAMP OPERATION
216: 'SEL A' LAMP OPERATION
217: 'MON A' LAMP OPERATION
218: 'ILLEGAL ENTRY' LAMP OPERATION
219: K1 ('KEY A') RELAY DE-ENERGIZED
220: K2 ('KEY B') RELAY DE-ENERGIZED
221: K1 ('KEY A') RELAY ENERGIZED
222: K2 ('KEY B') RELAY ENERGIZED
223: BRIGHTNESS CONTROL
SWITCH/ENCODER TESTS
TESTS 301 THRU 326 VERIFY:
301/302: 'CDR POS 1' SWITCH OPERATION / ENCODER DATA
303/304: 'CDR POS 2' SWITCH OPERATION / ENCODER DATA
305/306: 'STAFF 1' SWITCH OPERATION / ENCODER DATA
307/308: 'STAFF 2' SWITCH OPERATION / ENCODER DATA
309/310: 'STAFF 3' SWITCH OPERATION / ENCODER DATA
311/312: 'CREW' SWITCH OPERATION / ENCODER DATA
313/314: 'SEL B / MON B' SWITCH OPERATION / ENCODER DATA
315/316: 'RAD OPR 1' SWITCH OPERATION / ENCODER DATA
317/318: 'RAD OPR 2' SWITCH OPERATION / ENCODER DATA
319/320: 'RAD OPR 3' SWITCH OPERATION / ENCODER DATA
321/322: 'RAD OPR 4' SWITCH OPERATION / ENCODER DATA
323/324: 'RAD OPR 5' SWITCH OPERATION / ENCODER DATA
325/326: 'SEL A / MON A' SWITCH OPERATION / ENCODER DATA
2


2
COMMUNICATION ERROR HANDLING TESTS
TESTS 401 THRU 405 VERIFY:
401: PARITY ERROR GENERATION
402: ERROR STATUS CLEARED VIA 'STATUS-REQUEST'
403: FRAMING ERROR
404: FRAMING ERROR - CLEARED
405: REQUEST INHIBIT
CVSD 1 TESTS
TESTS 501 THRU 508 VERIFY:
501: HEADSET AUDIO AMPLITUDE (ICKEY Enabled)
502: HEADSET AUDIO AMPLITUDE (RADKEY Enabled)
503: CVSD DISABLED
504: HEADSET AUDIO VOLUME CONTROL
505: HEADSET AUDIO DISTORTION
506: LOW-PASS FILTER (3dB ROLLOFF POINT)
507: HIGH-PASS FILTER (3dB ROLLOFF POINT)
508: FLATNESS (400 Hz – 2.5 KHz)
UUT VERSION = AN/MIQ-1(V)1 ?
YES
3
NO
CVSD 2 TESTS
TESTS 509 THRU 514 VERIFY:
509: CVSD 2 RADIO AUDIO AMPLITUDE
510: MIC-OUT LEVEL CONTROL
511: CREW INTERCOM INPUT ATTENUATION (J2-H/J3-J)
512: CREW INTERCOM INPUT ATTENUATION (J2-G/J3-J)
513: CREW INTERCOM INPUT ATTENUATION (J2-G/J3-K)
514: CVSD 2 LOOPBACK
4


4
UUT VERSION = AN/MIQ-1(V)2 ?
YES
NO
CVSD 3 TESTS
TESTS 515 AND 516 VERIFY:
515: CVSD 3 RADIO AUDIO AMPLITUDE
516: CVSD 3 LOOPBACK
3
DISPLAY CLOSEOUT INSTRUCTIONS
DISPLAY MAIN MENU