Hardware/Software Manual for MIL-STD-1553 BC/RT/MT PCMCIA Interface Card

MN-65553-001

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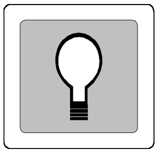
HOW TO USE THIS MANUAL

This manual uses typographical and iconic conventions to assist the reader in understanding the content. This section will define the text formatting and icons used in the rest of the manual. This manual is formatted with a 'Scholar Margin' where many tips, symbols or icons will be located.

Text Usage

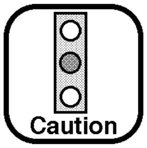
- **BOLD**– text that is written in bold letters indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC***– will designate DDC Part Numbers.
- `Courier New-` is used to indicate code examples.
- <…> - Indicates user entered text or commands.

Symbols and icons



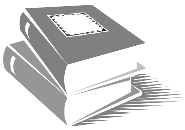
The Tip icon will be used to identify a handy bit of supplementary information that may be useful to the user.

The Note icon signifies important supplementary information that will be useful to the user.



The Caution icon identifies important information that presents a possibility of damage to the product if not heeded.

Much stronger than a Caution, the Warning icon presents information pertaining to hazards that will cause damage to the product and possible injury to the user.



The Reference icon indicates that there is related material in this manual or in another specified document.

The Disk Icon describes information that is related to software.

Special Handling and Cautions

The ***BU-65553*** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.

Warning

- The BU-65553 can be inserted and removed with power on the computer.
- Ensure that standard ESD precautions are followed.
- Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

Trademarks

All trademarks are the property of their respective owners.

Special Notes

Unless otherwise noted, an asterisk after a signal name (i.e., MSTCLR*) indicates that the signal is an active low.

INTRODUCTION

The BU-65553 Enhanced Mini-ACE PCMCIA Card has the same basic architecture as previous versions of the DDC 1553 terminal PCMCIA cards. The Card provides a full, intelligent interface between a dual redundant MIL-STD-1553 Data Bus and a PCMCIA socket. It can be used as a 1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT). The software gives the user total control in determining the mode of operation. The PC Card is packaged in a PCMCIA Type II PC card and is fully compliant with the PCMCIA 2.10 standard along with MIL-STD-1553A and B (Notice 2). Other features of the card include:

- Autonomous Programmable BC
- Circular Buffers with roll over and half roll over interrupts
- Programmable Automatic BC Retries
- 64 Kbytes of shared static RAM per installed channel
- Selective Message Monitor
- Simultaneous RT/Monitor Mode
- Flexible Interrupt Generation
- Programmable Illegalization
- 100% software compatibility with previous versions
- All software and updates are posted on the DDC Web site

What is included in this manual?

This manual contains a detailed installation guide for the PC Card (PCMCIA) and a basic overview of the software supplied with the card.

This manual also provides an introduction to the Enhanced Mini-ACE (EMACE) Library. Complete documentation for the EMACE Library is provided in the Enhanced Mini-ACE Runtime Library Manual (#MN-69090XX-001). If it is desired to program the ***BU-65553*** in previous version of the ACE library, please refer to the ***BUS-69080/69082/69083*** Runtime Library Manual (#MN-69080-001). For those who are interested in detailed information on the operation of the control registers and memory mapped data structures, a copy of the Enhanced Mini-ACE User's Guide (#MN-65170XX-001) may be obtained from DDC.

System Requirements

PC Support

- An IBM compatible PC with a ‘486 processor or better. DDC recommends a 200Mhz Pentium or faster
- Windows® 95, 98, Windows NT® operating system
- A single Type II PCMCIA slot

Technical Support

In the event that problems arise beyond the scope of this manual you can get in touch with DDC by calling:

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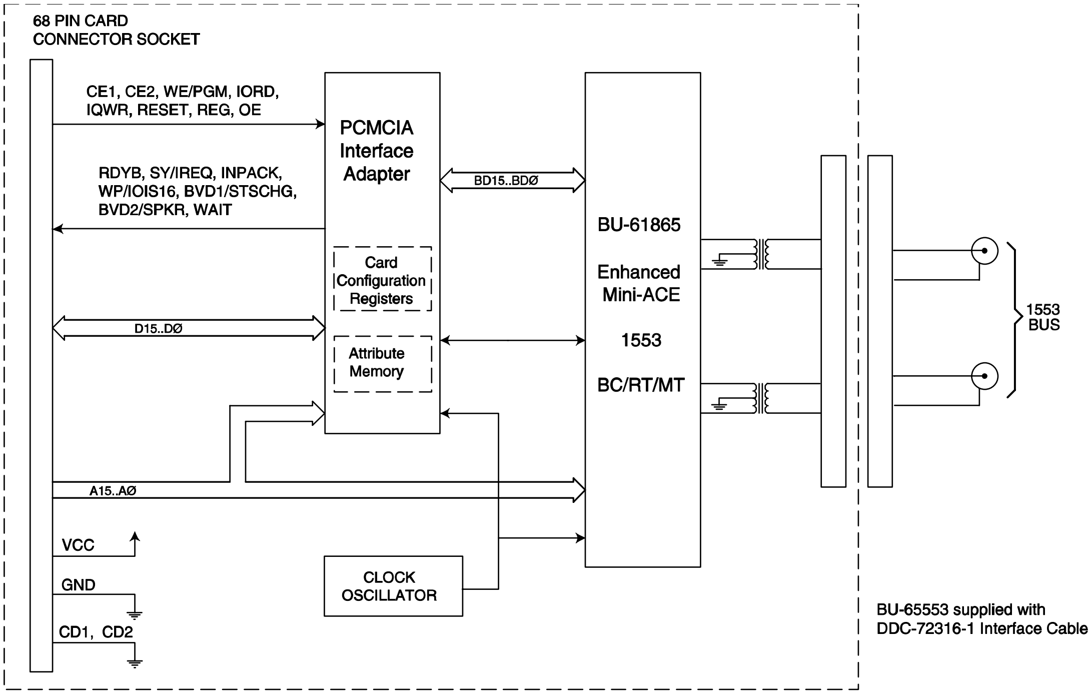


Figure 1. BU-65553 Block Diagram

HARDWARE INSTALLATION

The installation of the PC Card is greatly simplified due to the PCMCIA design. These cards may be plugged into one of the PCMCIA slots provided in a laptop or desktop PC computer. The PC Card is designed so that it may be inserted or removed from a PC with the power turned on. If Windows 95/98 is being used, the operating system will recognize the card when it is installed and start the appropriate device driver. If Windows NT is being used, the PC Card must be inserted in the PC prior to the operating system boot. This is because Windows NT release 4.XX is not natively Plug-and-Play. Windows 2000 is the newest release of the Microsoft operating system. It provides the stability of Windows NT with the Plug-and-Play capabilities of Windows 95.

Warning

Care should be taken to reduce damage to the hardware due to Electro-Static Discharge (ESD).

Hardware Configuration

The ***BU-65553*** is a compatible PCMCIA Plug and Play card, and as such does not require any jumpers or switches to set the Base address or interrupt values. Under Windows 95/98 the device driver performs the configuration of the PC Card during the operating system enumeration of the PC buses. When the operating system detects a card connected to the PCMCIA slot, it will query the card for configuration requirements. These requirements will describe the usage of such resources as memory and interrupts. The resource requirements are stored in **Tuples** that are non-volatile memory in the PCMCIA card. The tuples contain information such as the manufacturer, card ID, and resource allocation requirements. In many cases there will be suggested resource allocations that should be tried by the operating system first. Then, if these suggested allocations fail, the system will try to fit the memory and interrupt resources among the established allocations. The tuples are configured at DDC to contain the optimum values for the operation of the PC Card.

System Requirements

When running under DOS / Windows 3.XX, the software interface of the PC Card requires that the host system run a REAL MODE Card Services driver which is compliant to PCMCIA Specification Release 2.10 or greater. If the host system is running Windows 95/98 or NT there is no need to run the REAL MODE Card Services driver, instead the Windows default 32 bit PROTECTED MODE Card Services driver should be used. This driver is also fully compatible with the 1553 PC Card.

The software supplied with the PC Card requires DOS version 3.0 or greater and MS Windows 3.X, Windows 95/98, or Windows NT. When running DOS, Windows 3.1 is required for installation. The 16-bit ACE Library contains source code that may be ported to other operating systems. The system requirements for the ACE software are described in the table below.

Table 1. ACE Software Requirements

Part Number	Description	Requirements
BUS-69080	16-Bit DOS Runtime Library	DOS 3.0 or newer Windows 3.X 3.0 Meg Disk
BUS-69081	16-Bit Windows 3.X Menu	Windows 3.X 1 Meg Disk
BUS-69082	32-Bit Windows 95 DLL/VxD	Win 95 8 Meg RAM 486 or better CPU 2.5 Meg Disk
BUS-69083	32-Bit Windows NT DLL/VxD	Win NT 8 Meg RAM 486 or better CPU 2.5 Meg Disk
BUS-69084	32-Bit Windows 95 Menu	Win 95 8 Meg RAM 486 or better CPU 1.0 Meg Disk
BUS-69085	32-Bit Windows NT Menu	Win NT 8 Meg RAM 486 or better CPU 1.0 Meg Disk

ACE Runtime Library

The ACE Runtime Library is supplied for DOS/Windows 3.1X, Windows 95/98 and Windows NT. The DOS/Windows 3.1X version includes source code, sample files, and utilities and can easily be installed under both DOS and Windows 3.X. The 32-Bit Windows version includes sample files for C/C++, Visual Basic and LabVIEW. All versions include the source and executable for the examples. The user is free to use the example source code, in part or in its entirety, for personal use.

If you are installing the Runtime Library under DOS/Windows, 3.1X advance to “16 Bit ACE Runtime Library (BUS-69080)” on page 36. If you are running under Windows 95/98 you have the choice of installing the 16 bit or the 32 bit libraries.

Note: *The 16-bit version of the Runtime Library cannot be run under Windows NT.*

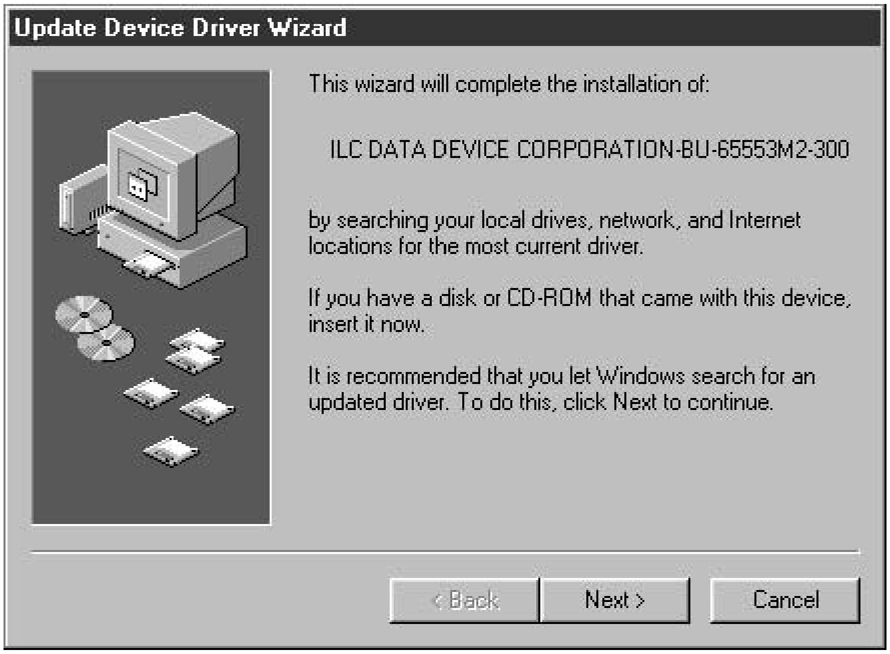
Driver installation

This section will install the driver(s) needed to operate the hardware properly.

1) Install the card as described in the previous **HARDWARE INSTALLATION** section.

2) Turn on the computer.

3) The **Update Device Driver Wizard** window will appear after boot-up.



Update Device Driver Wizard

This wizard will complete the installation of:

ILC DATA DEVICE CORPORATION-BU-65553M2-300

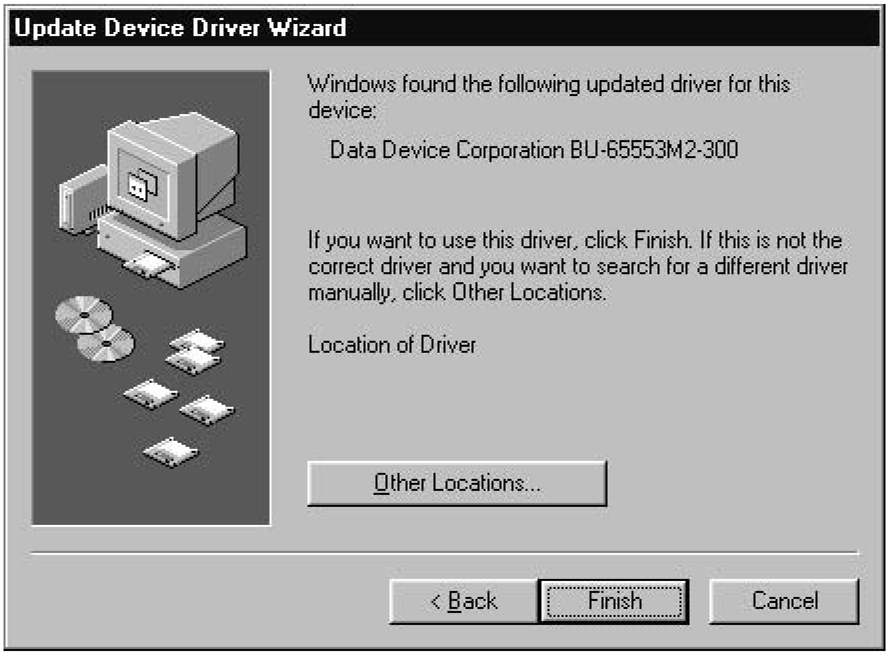
by searching your local drives, network, and Internet locations for the most current driver.

If you have a disk or CD-ROM that came with this device, insert it now.

It is recommended that you let Windows search for an updated driver. To do this, click Next to continue.

Figure 2. Device Driver Wizard

4) Click the **Next** button to continue with the driver installation.



Update Device Driver Wizard

Windows found the following updated driver for this device:

Data Device Corporation BU-65553M2-300

If you want to use this driver, click Finish. If this is not the correct driver and you want to search for a different driver manually, click Other Locations.

Location of Driver

Figure 3. Search for Driver

5) Once Windows finds the driver for the device, click the **Finish** button.

6) The driver is now installed.

SOFTWARE INSTALLATION

If using Windows 95/98, perform the following installation instructions. If using another operating system, skip to the relevant installation section.

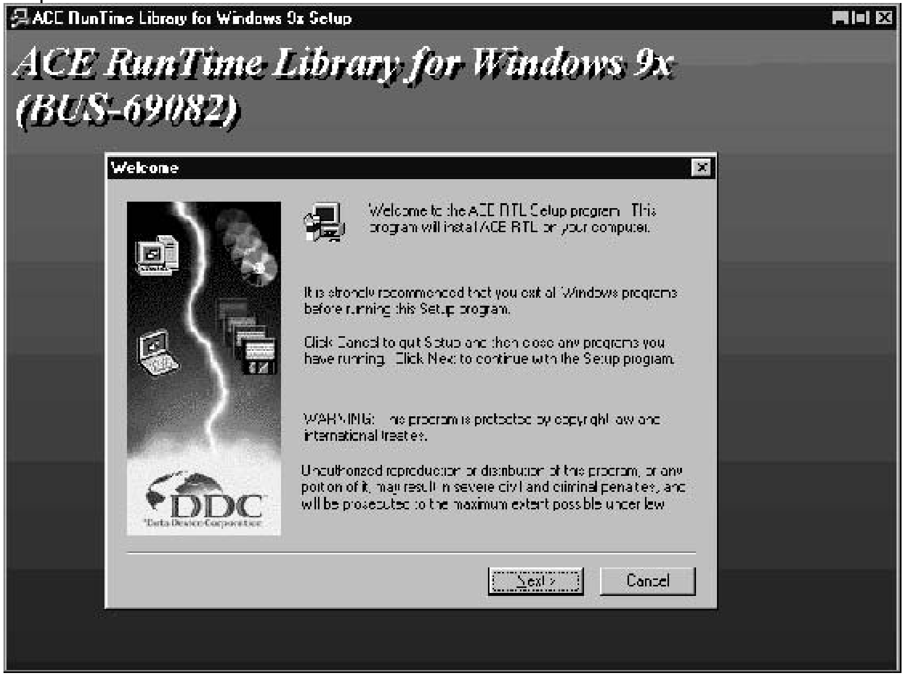
WINDOWS 95/98

Install the card as described in the previous **HARDWARE INSTALLATION** section.

1) Turn on the computer.

2) After boot-up, insert the software CD or floppy disk labeled Disk 1 into the appropriate drive.

3) If the **ACE Runtime Library for Windows 9x Setup** screen does not display, click the Start button on the Windows taskbar, and click Run. Type <A:\setup> (where 'A' is the letter corresponding to the drive containing the software you inserted in step 2) in the open box.



ACE RunTime Library for Windows 9x (BUS-69082)

Welcome to the ACE RTL Setup program. This program will install ACE RTL on your computer.

It is strongly recommended that you exit all Windows programs before running this Setup program.

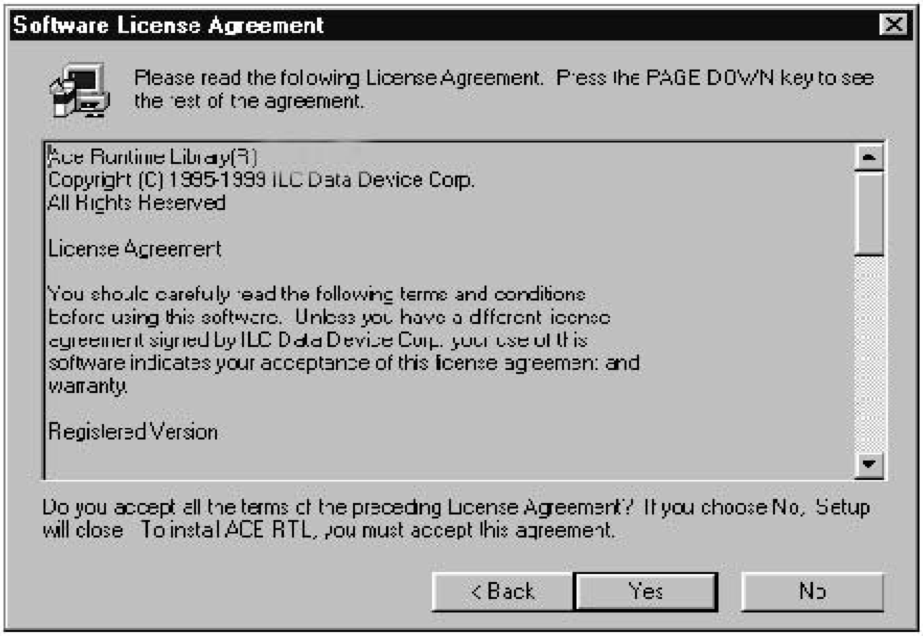
Click Cancel to quit Setup and then close any programs you have running. Click Next to continue with the Setup program.

WARNING: This program is protected by copyright law and international treaties.

Unauthorized reproduction or distribution of this program, or any portion of it, may result in severe civil and criminal penalties, and will be prosecuted to the maximum extent possible under law.

Figure 4.   Windows 95/98 RTL Install Welcome

4) The setup screen shows the software you are about to install. Click the **Next** button to start the installation process.



Software License Agreement

Please read the following License Agreement. Press the PAGE DOWN key to see the rest of the agreement.

Ace Runtime Library(R)
Copyright (C) 1995-1999 ILC Data Device Corp.
All Rights Reserved

License Agreement

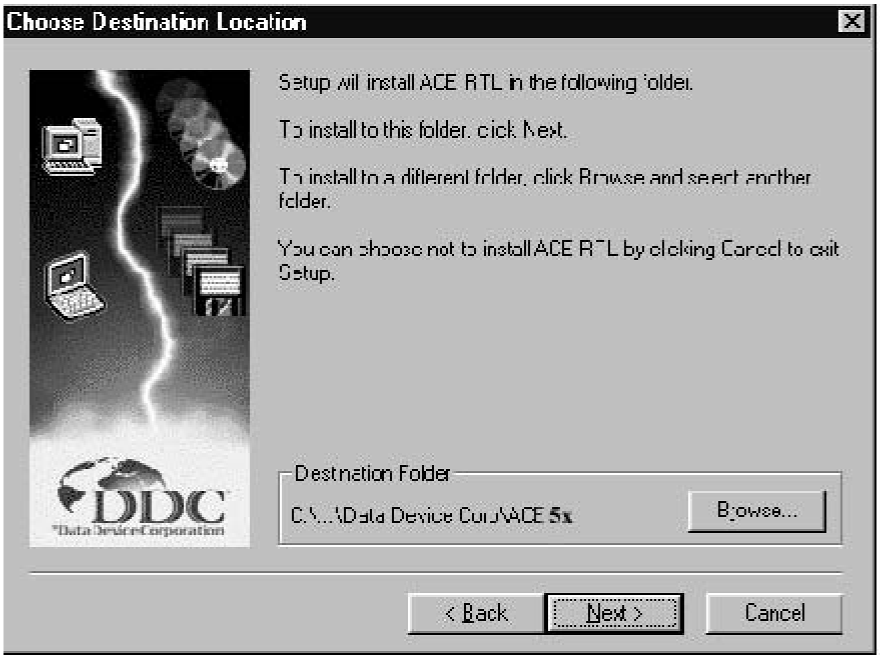
You should carefuly read the following terms and conditions before using this software. Unless you have a different license agreement signed by ILC Data Device Corp. your use of this software indicates your acceptance of this license agreement and warranty.

Registered Version

Do you accept all the terms of the preceding License Agreement? If you choose No, Setup will close. To install ACE RTL, you must accept this agreement.

Figure 5. License Agreement

5) Read the license agreement, and click the **Yes** button. If you don’t accept the license agreement, the Setup application will end.



Setup will install ACE RTL in the following folder.

To install to this folder, click Next.

To install to a different folder, click Browse and select another folder.

You can choose not to install ACE RTL by clicking Cancel to exit Setup.

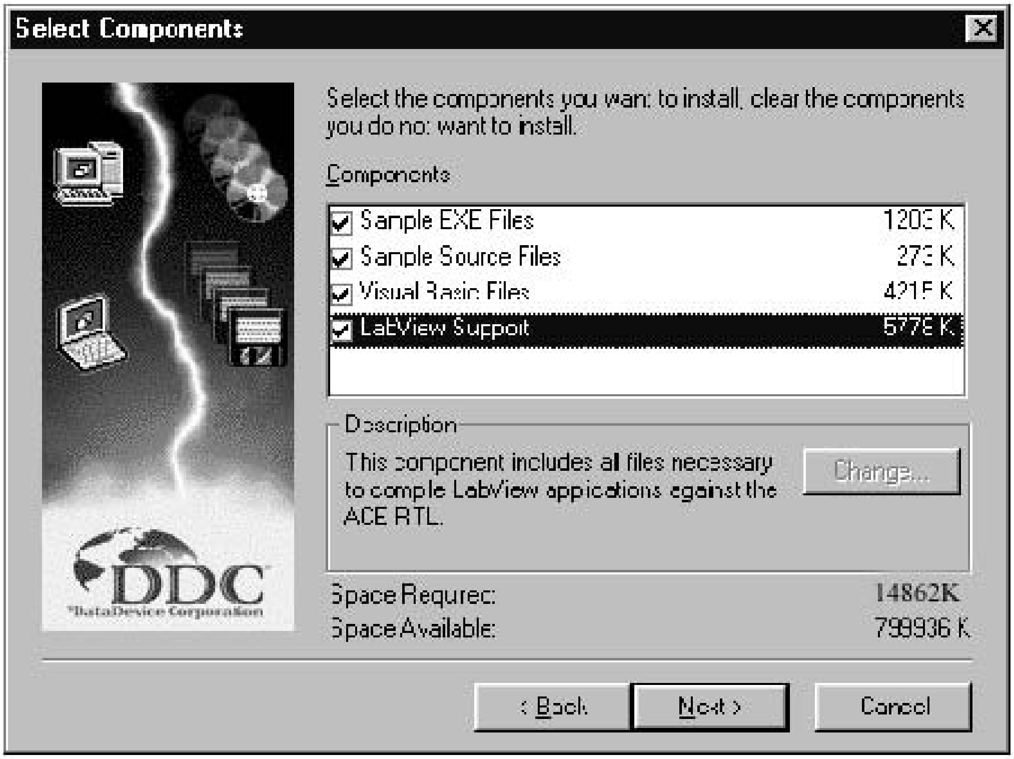
Destination Folder

C:\...\Data Device Corp\ACE 5x

Figure 6. Installation Destination

6) This screen shows where the software will be installed. You can accept the default folder, or choose your own destination by clicking the **<u>B</u>rowse** button.

7) After the location is selected, Click **<u>N</u>ext** to continue.



Select Components

Select the components you want to install, clear the components you do not want to install.

Components

- ☑ Sample EXE Files 1203 K
- ☑ Sample Source Files 273 K
- ☑ Visual Basic Files 4215 K
- ☑ LabView Support 5776 K

Description

This component includes all files necessary to compile LabView applications against the ACE RTL.

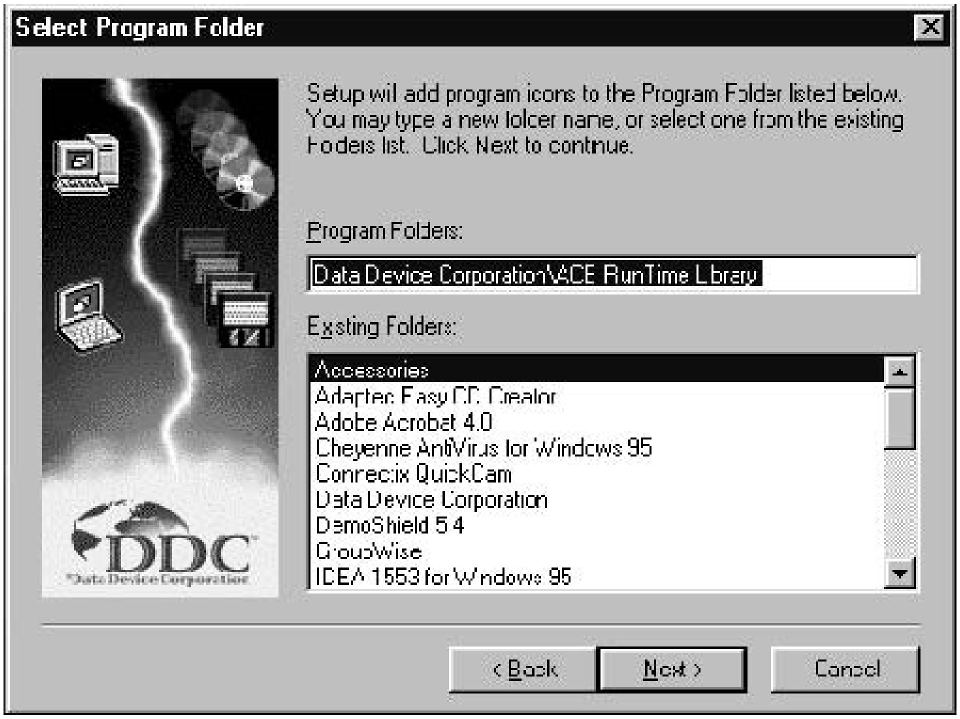
Space Required: 14862K

Space Available: 799936 K

Figure 7. Select Components

8) Select the component(s) you want to install by checking the box next the item.

9) Click the **<u>N</u>ext** button to continue.



Select Program Folder

Setup will add program icons to the Program Folder listed below. You may type a new folder name, or select one from the existing Folders list. Click Next to continue.

Program Folders:

Data Device Corporation\ACE RunTime Library

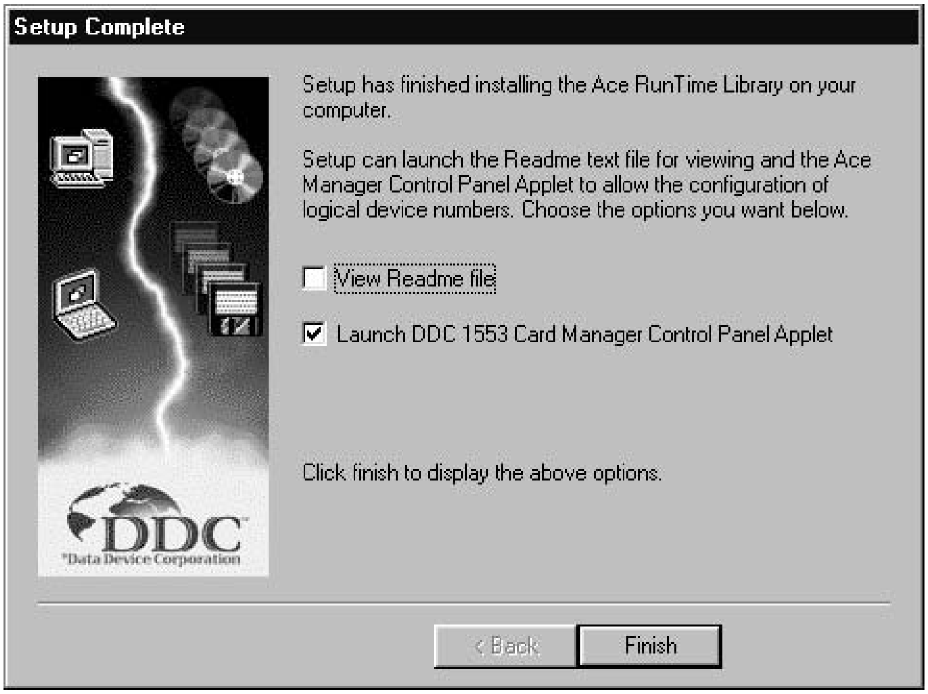
Existing Folders:

Accessories
Adaptec Easy CD Creator
Adobe Acrobat 4.0
Cheyenne AntiVirus for Windows 95
Connectix QuickCam
Data Device Corporation
DemoShield 5.4
GroupWise
IDEA 1553 for Windows 95

Figure 8. Select Program Folder

10) Select an existing Program Folder from the list shown or create a new one by typing a name in the space provided.

11) Click the **NEXT** button to continue.



Setup Complete

Setup has finished installing the Ace RunTime Library on your computer.

Setup can launch the Readme text file for viewing and the Ace Manager Control Panel Applet to allow the configuration of logical device numbers. Choose the options you want below.

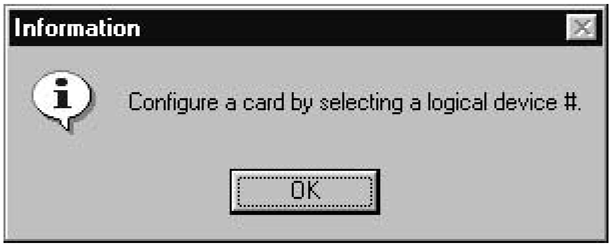
□ View Readme file

☑ Launch DDC 1553 Card Manager Control Panel Applet

Click finish to display the above options.

Figure 9. Setup Complete

12) Click the **Finish** button to finish the installation

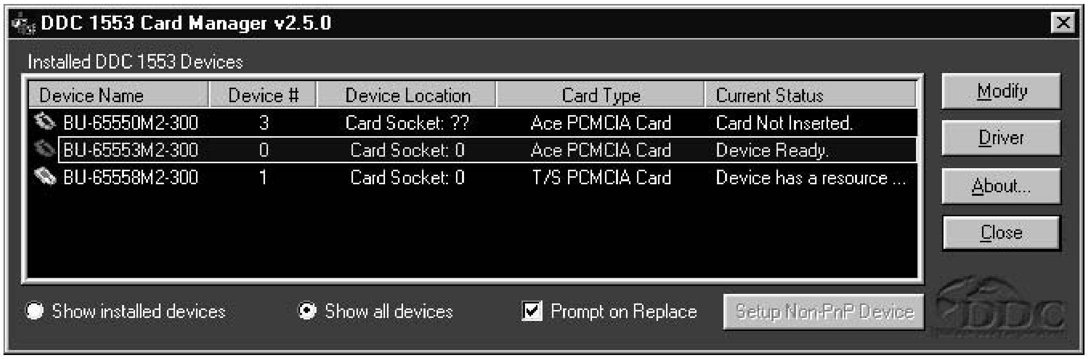


Information

Configure a card by selecting a logical device #.

Figure 10. Information

13) Click **OK** to proceed to the card manager



DDC 1553 Card Manager v2.5.0

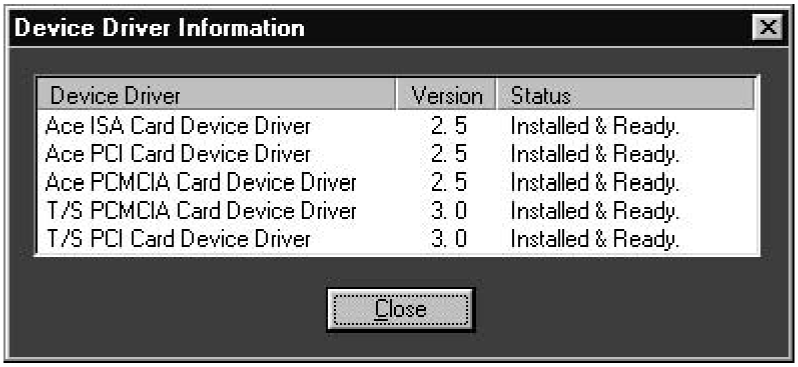
Installed DDC 1553 Devices

Device Name	Device #	Device Location	Card Type	Current Status
BU-65550M2-300	3	Card Socket: ??	Ace PCMCIA Card	Card Not Inserted.
BU-65553M2-300	0	Card Socket: 0	Ace PCMCIA Card	Device Ready.
BU-65558M2-300	1	Card Socket: 0	T/S PCMCIA Card	Device has a resource ...

○ Show installed devices ● Show all devices ☑ Prompt on Replace

Figure 11. Windows 95/98 1553 Card Manager

14) Choose the device named BU-65553M, then click **Driver**

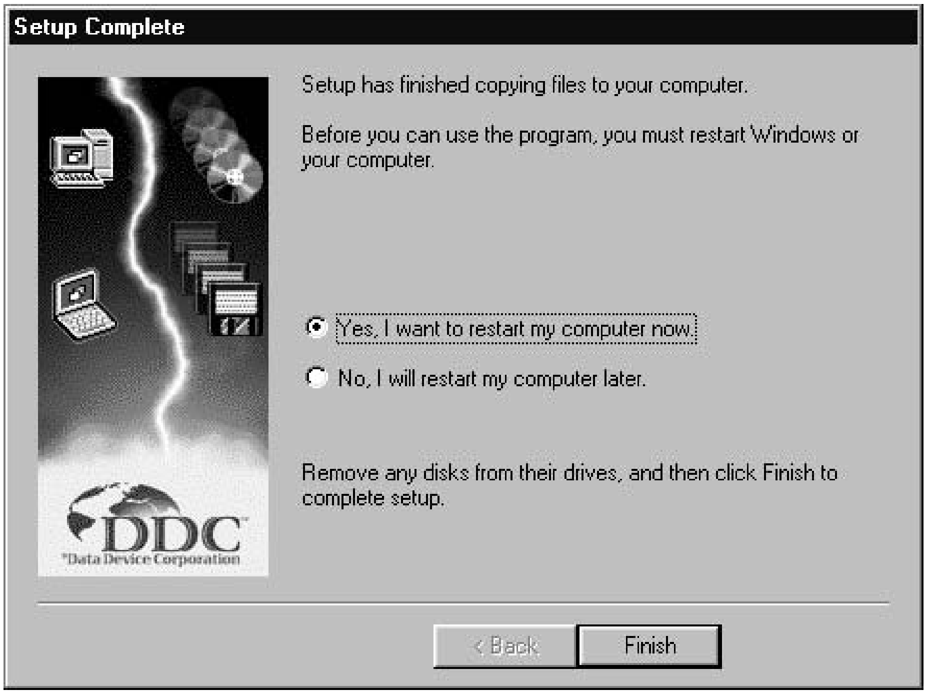


Device Driver	Version	Status
Ace ISA Card Device Driver	2. 5	Installed & Ready.
Ace PCI Card Device Driver	2. 5	Installed & Ready.
Ace PCMCIA Card Device Driver	2. 5	Installed & Ready.
T/S PCMCIA Card Device Driver	3. 0	Installed & Ready.
T/S PCI Card Device Driver	3. 0	Installed & Ready.

Figure 12. Windows 95/98 1553 Device Driver Information

15) Make sure the driver’s status shows “Installed & Ready”.

16) Click on the **Close** button.



Setup Complete

Setup has finished copying files to your computer.

Before you can use the program, you must restart Windows or your computer.

● Yes, I want to restart my computer now.

○ No, I will restart my computer later.

Remove any disks from their drives, and then click Finish to complete setup.

Figure 13. Windows 95/98 RTL Setup Complete

17) Setup has finished installing the software.

18) Click **Finish** to restart the computer.

WINDOWS NT 4.0 / 2000

If using Windows NT 4.0 or 2000, perform the following installation instructions. If using another operating system, skip to the relevant installation section.

1) Install the card as described in the previous **HARDWARE INSTALLATION** section.

2) Turn on the computer.

3) After boot-up, insert the software CD or floppy disk labeled Disk 1 into the computer.

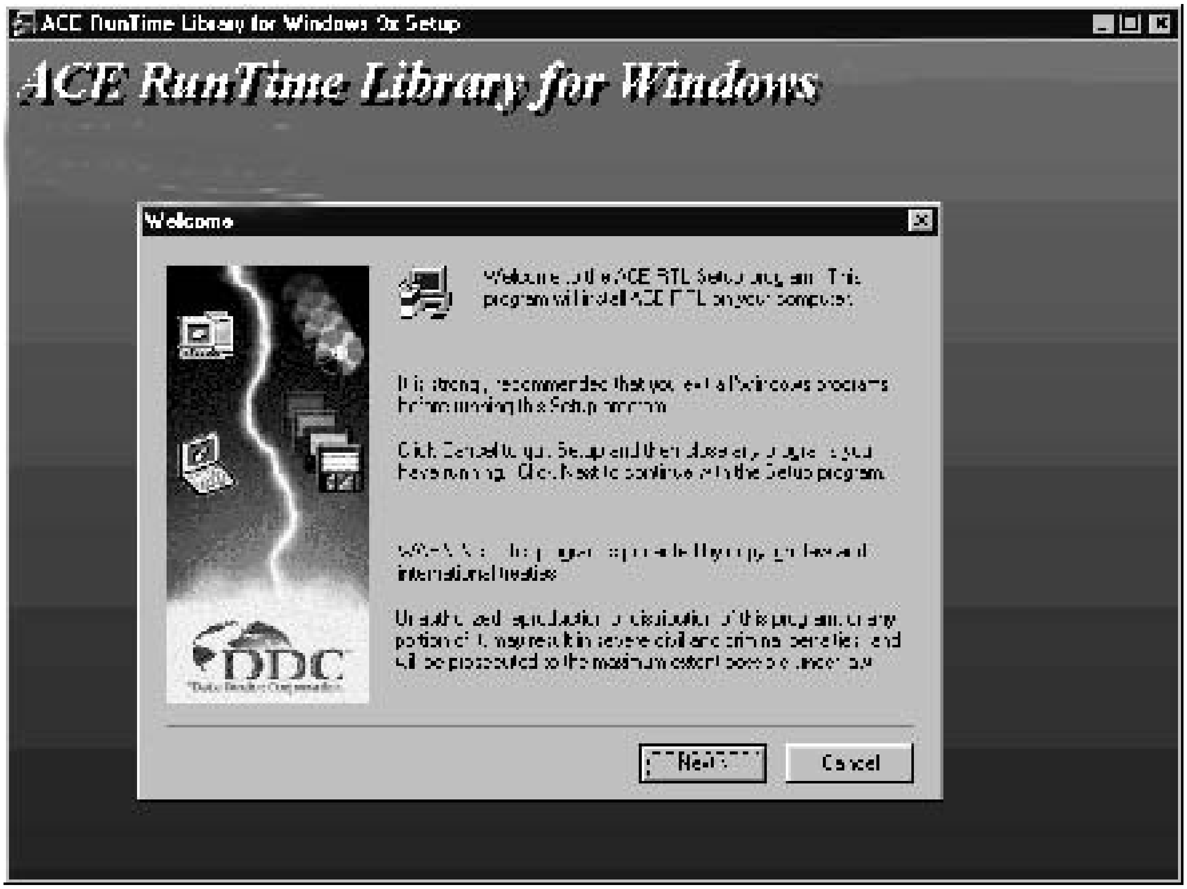
4) Click on the Windows **Start** button.

5) Click on **Run**.

6) In the **Open** window type <***A:\Setup.exe***>(where A is the letter corresponding to the drive containing the software you inserted in step 3) above.

7) Click **OK.**

8) If the **ACE Runtime Library for Windows Setup** screen does not display, click the Start button on the Windows taskbar, and click Run. Type <A:\setup> (where ‘A’ is the letter corresponding to the drive containing the software you inserted in step 3) in the open box.


ACE RunTime Library for Windows 9x Setup
ACE RunTime Library for Windows
Welcome
DDC
Data Device Corporation
Next >
Cancel

Welcome to the ACE RTL Setup program. This program will install ACE RTL on your computer.

It is strongly recommended that you exit all Windows programs before running this Setup program.

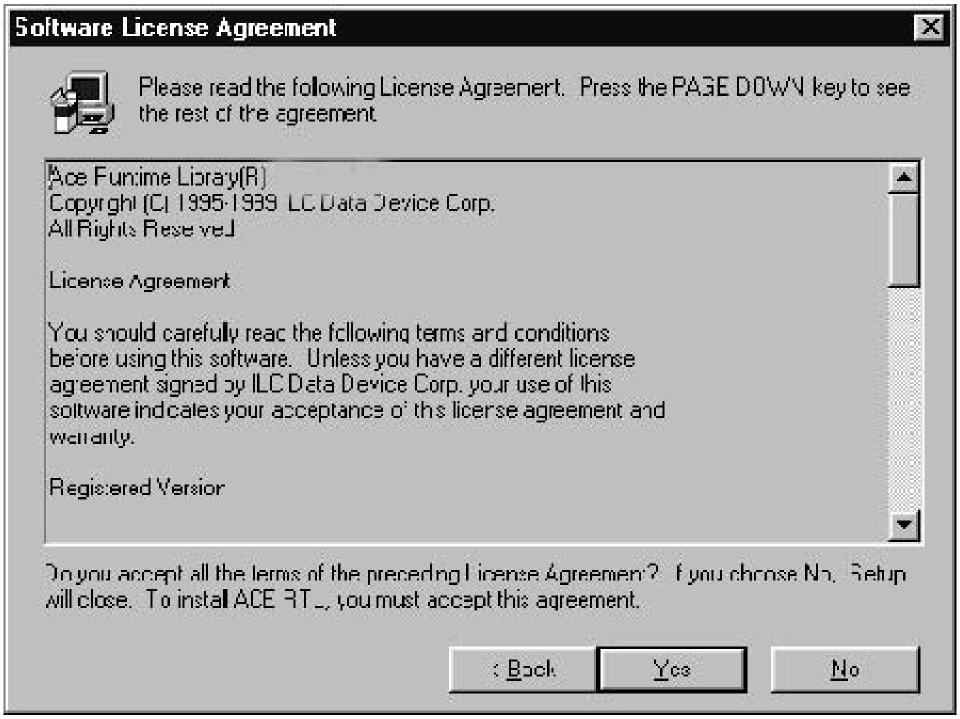
Click Cancel to quit Setup and then close any programs you have running. Click Next to continue with the Setup program.

WARNING: This program is protected by copyright law and international treaties.

Unauthorized reproduction or distribution of this program, or any portion of it, may result in severe civil and criminal penalties, and will be prosecuted to the maximum extent possible under law.

Figure 14. Windows NT/2000 RTL Install Welcome

9) The setup screen shows the software you are about to install. Click the **N̲ext** button to start the installation process.



Please read the following License Agreement. Press the PAGE DOWN key to see the rest of the agreement.

Ace Runtime Library(R)
Copyright (C) 1995-1999 ILC Data Device Corp.
All Rights Reserved

License Agreement

You should carefully read the following terms and conditions before using this software. Unless you have a different license agreement signed by ILC Data Device Corp. your use of this software indicates your acceptance of this license agreement and warranty.

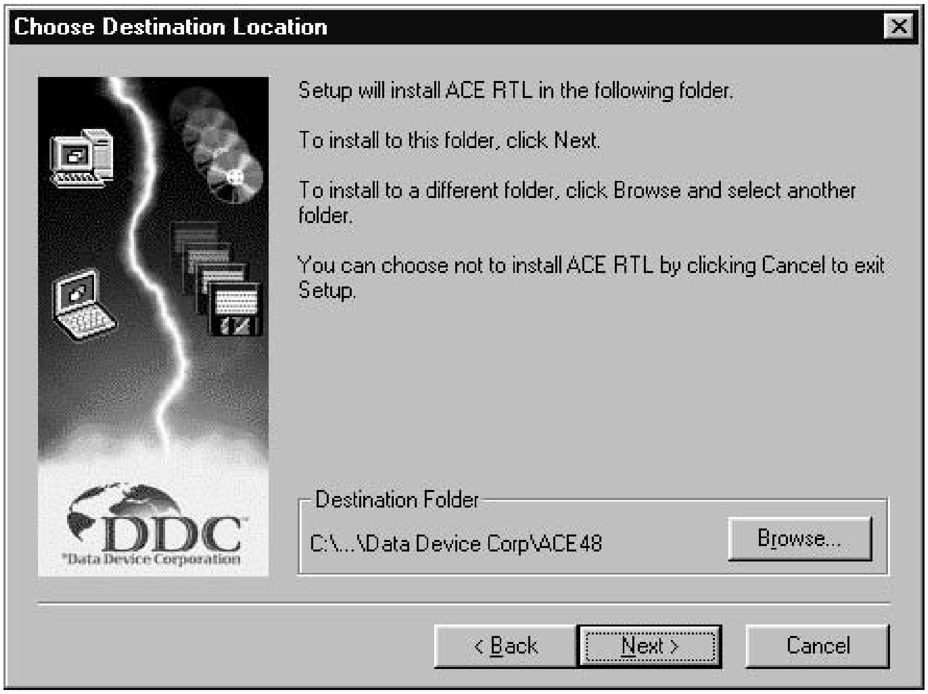
Registered Version

Do you accept all the terms of the preceding License Agreement? If you choose No, Setup will close. To install ACE RTL, you must accept this agreement.

Figure 15. License Agreement

10) Read the license agreement, and click the **Yes** button. If you don't accept the license agreement, the Setup application will end.

11) This screen shows where the software will be installed. You can accept the default folder, or choose your own destination by clicking the **Browse** button.



Choose Destination Location

Setup will install ACE RTL in the following folder.

To install to this folder, click Next.

To install to a different folder, click Browse and select another folder.

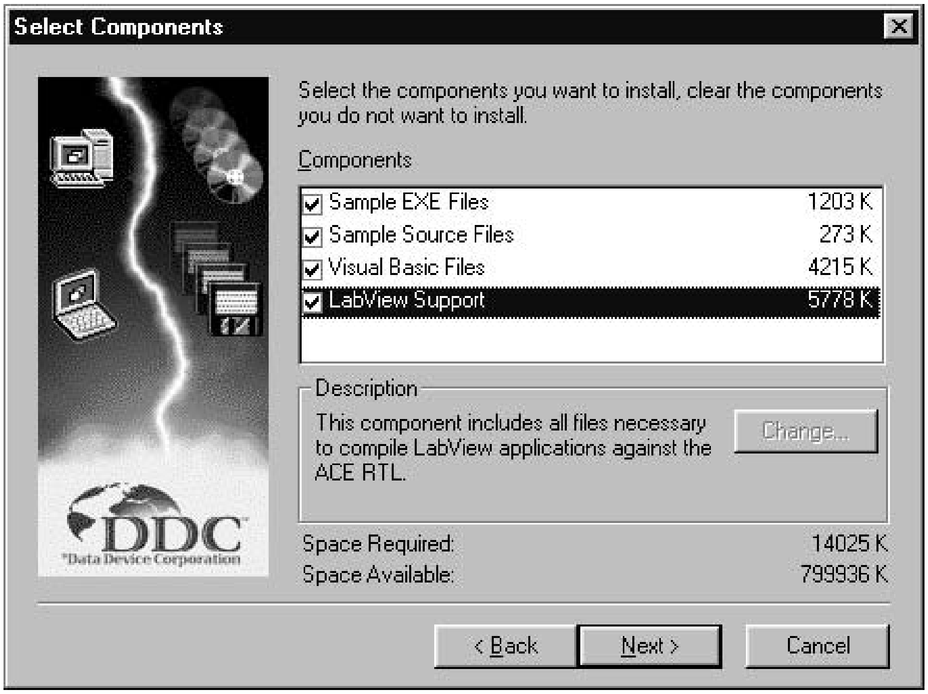
You can choose not to install ACE RTL by clicking Cancel to exit Setup.

Destination Folder

C:\...\Data Device Corp\ACE48

Figure 16. Installation Destination

12) After the location is selected, Click **Next** to continue.



Select Components

Select the components you want to install, clear the components you do not want to install.

Components

☑ Sample EXE Files	1203 K
☑ Sample Source Files	273 K
☑ Visual Basic Files	4215 K
☑ LabView Support	5778 K

Description

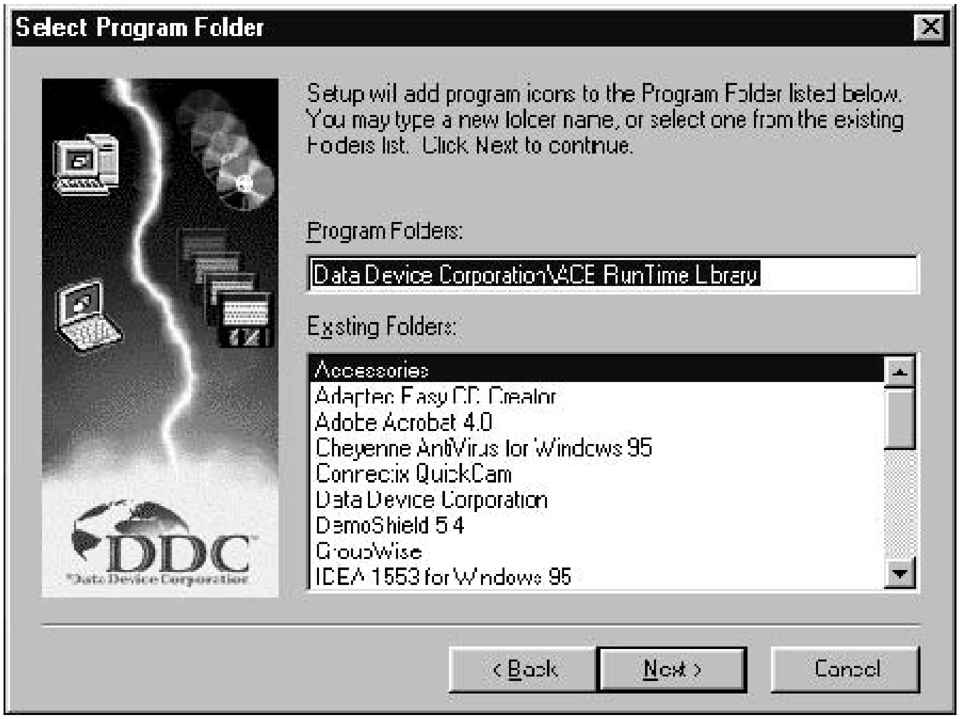
This component includes all files necessary to compile LabView applications against the ACE RTL.

Space Required:	14025 K
Space Available:	799936 K

Figure 17. Select Components

13) Select the component(s) you want to install by checking the box next to it.

14) Click the **Next** button to continue.



Setup will add program icons to the Program Folder listed below. You may type a new folder name, or select one from the existing Folders list. Click Next to continue.

Program Folders:

Data Device Corporation\ACE RunTime Library

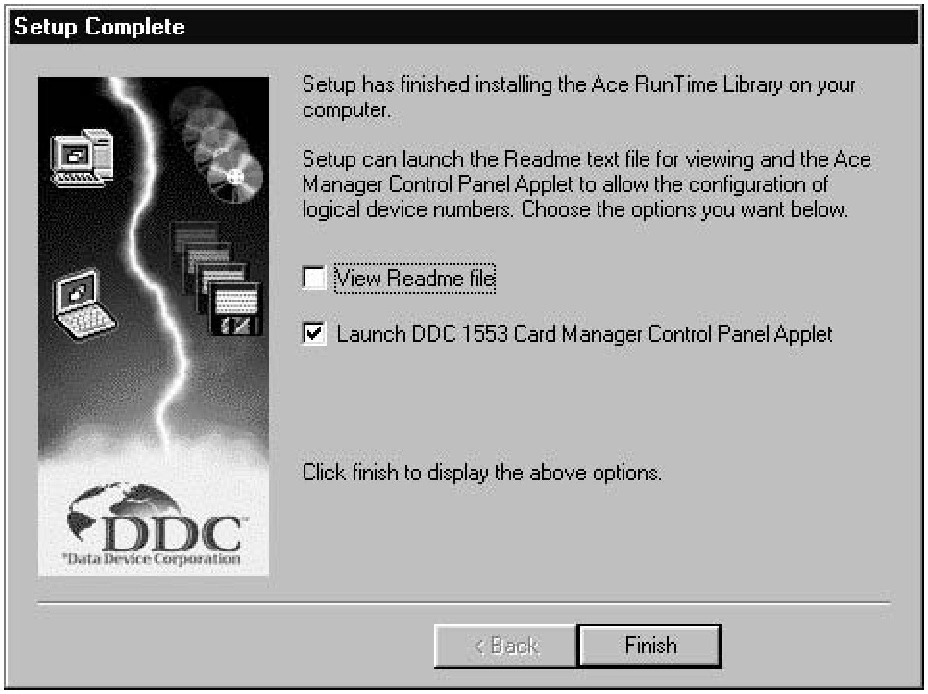
Existing Folders:

Accessories
Adaptec Easy CD Creator
Adobe Acrobat 4.0
Cheyenne AntiVirus for Windows 95
Connectix QuickCam
Data Device Corporation
DemoShield 5.4
GroupWise
IDEA 1553 for Windows 95

Figure 18. Select Program Folder

15) Select an existing Program Folder from the list shown or create a new one by typing a name in the space provided.

16) Click the **<u>N</u>EXT** button to continue.



Setup Complete

Setup has finished installing the Ace RunTime Library on your computer.

Setup can launch the Readme text file for viewing and the Ace Manager Control Panel Applet to allow the configuration of logical device numbers. Choose the options you want below.

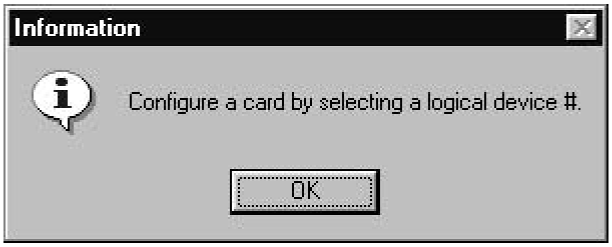
□ View Readme file

☑ Launch DDC 1553 Card Manager Control Panel Applet

Click finish to display the above options.

Figure 19. Setup Complete

17) Click the **Finish** button to finish the installation



Information

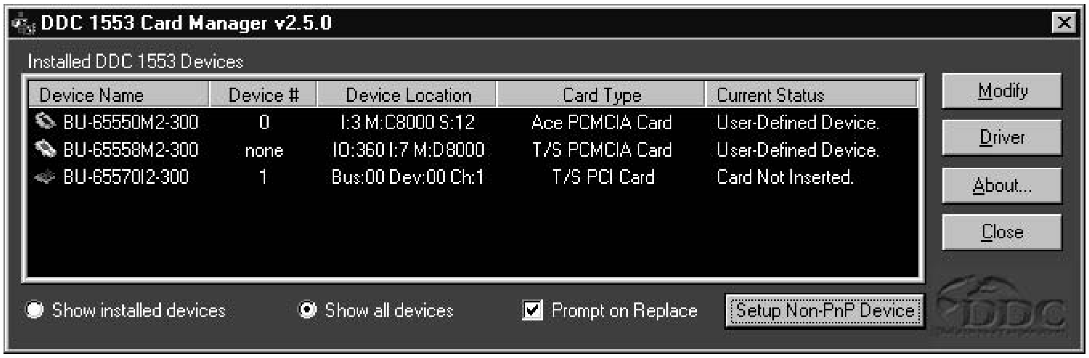
Configure a card by selecting a logical device #.

Figure 20. Information

18) Click **OK** to proceed to the card manager

19) Run the DDC 1553 Card Manager. This shows all installed 1553 devices (default for PCMCIA is 65550M2-300).

Note: *If you are using Windows 2000, the DDC 1553 Card Manager will operate as if the operating system were Windows 95/98.*



Installed DDC 1553 Devices

Device Name	Device #	Device Location	Card Type	Current Status
BU-65550M2-300	0	I:3 M:C8000 S:12	Ace PCMCIA Card	User-Defined Device.
BU-65558M2-300	none	IO:360 I:7 M:D8000	T/S PCMCIA Card	User-Defined Device.
BU-65570I2-300	1	Bus:00 Dev:00 Ch:1	T/S PCI Card	Card Not Inserted.

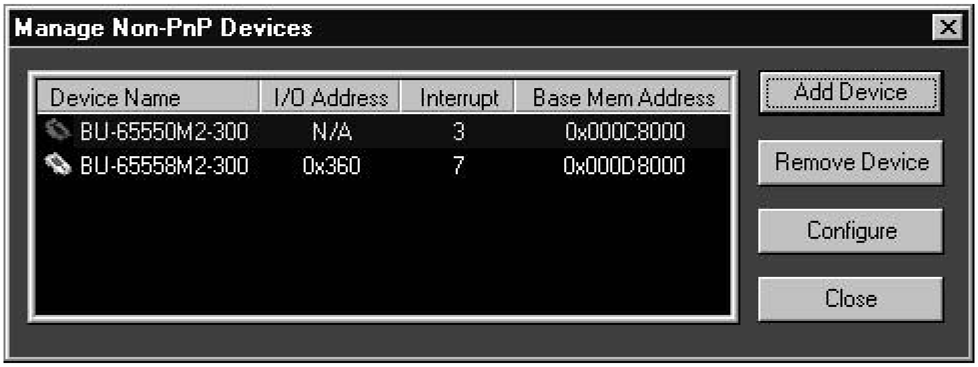
○ Show installed devices ● Show all devices ☑ Prompt on Replace

Figure 21. DDC 1553 Card Manager

20) Remove all 6555X (except 65558) cards by selecting the card and pressing the **Delete** key. This is done because Windows NT does not support multiple PCMCIA cards that use the same driver.

21) Click on the **Setup Non-PnP** (Non-Plug and Play) Device button.

22) The Manage Non-PnP Devices screen will appear. Highlight the BU-6555X entry and click on the **Remove Device** button. This will halt the driver and remove all devices that use it.

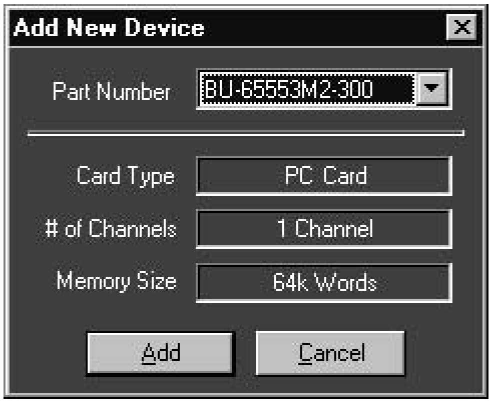


Device Name	I/O Address	Interrupt	Base Mem Address
BU-65550M2-300	N/A	3	0x000C8000
BU-65558M2-300	0x360	7	0x000D8000

Figure 22. Manage Non-PnP Devices

23) Once all ACE PCMCIA cards are removed, click on the **Add Device** button to install the correct driver configuration for the BU-65553M2-300.

24) The Add New Device dialog will appear. Select the BU-65553M2-300 from the drop-down list.



Add New Device

Part Number: BU-65553M2-300

Card Type: PC Card

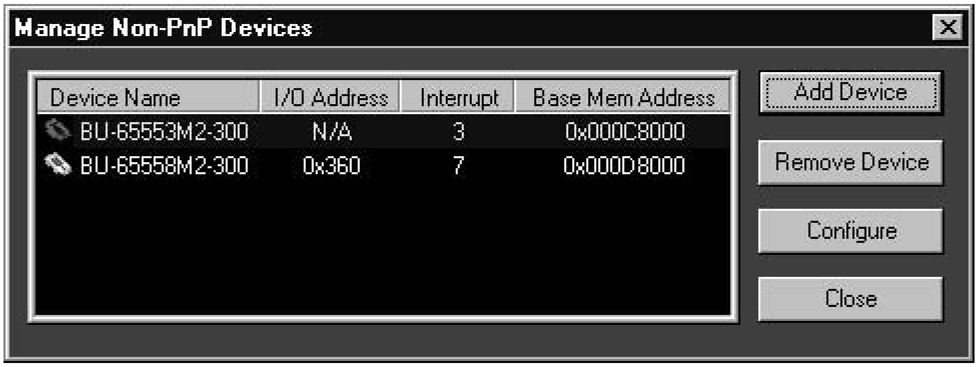
# of Channels: 1 Channel

Memory Size: 64k Words

Figure 23. Add New Device

25) Verify that entries are correct, and click on the **<u>A</u>dd** button.

26) The Manage Non-PnP Devices dialog box will reappear. Click on the **<u>C</u>lose** button.

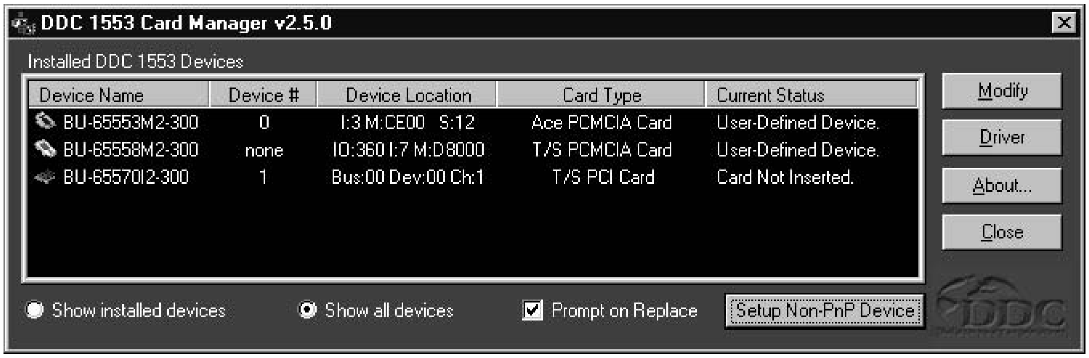


Manage Non-PnP Devices

Device Name	I/O Address	Interrupt	Base Mem Address
BU-65553M2-300	N/A	3	0x000C8000
BU-65558M2-300	0x360	7	0x000D8000

Figure 24. Manage Non-PnP Devices

27) The main DDC 1553 Card Manager window will reappear. Highlight the BU-65553M2-300 device and click the **Modify** button.



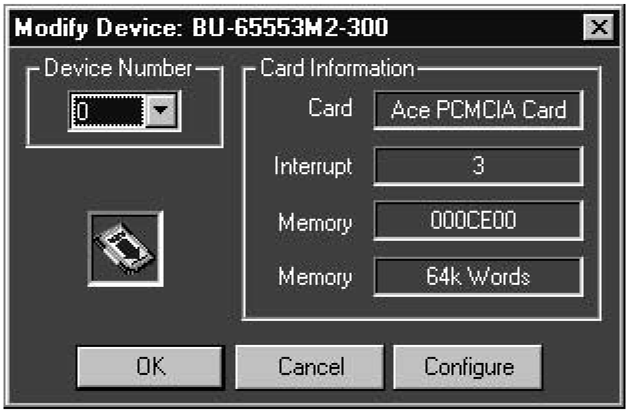
Installed DDC 1553 Devices

Device Name	Device #	Device Location	Card Type	Current Status
BU-65553M2-300	0	I:3 M:CE00 S:12	Ace PCMCIA Card	User-Defined Device.
BU-65558M2-300	none	IO:360 I:7 M:D8000	T/S PCMCIA Card	User-Defined Device.
BU-65570I2-300	1	Bus:00 Dev:00 Ch:1	T/S PCI Card	Card Not Inserted.

○ Show installed devices ● Show all devices ☑ Prompt on Replace

Figure 25. DDC 1553 Card Manager

28) The Modify Device screen for the selected card will come up.



Device Number: 0

Card Information

Card: Ace PCMCIA Card

Interrupt: 3

Memory: 000CE00

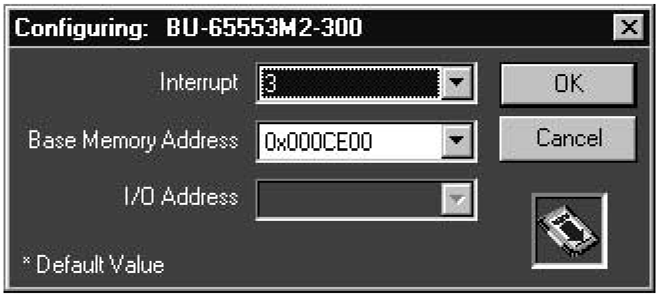
Memory: 64k Words

Figure 26. Modify Device

29) All cards must have a unique device number. Select a number from the drop-down list (If the number selected is being used by another DDC card, then the other card will be reset to NONE, and the new card will use the selected number).

30) Click the **Configure** button to modify the cards resources.

31) The Configuring: BU-65550M2-300 window appears.



Configuring: BU-65553M2-300

Interrupt: 3

Base Memory Address: 0x000CE00

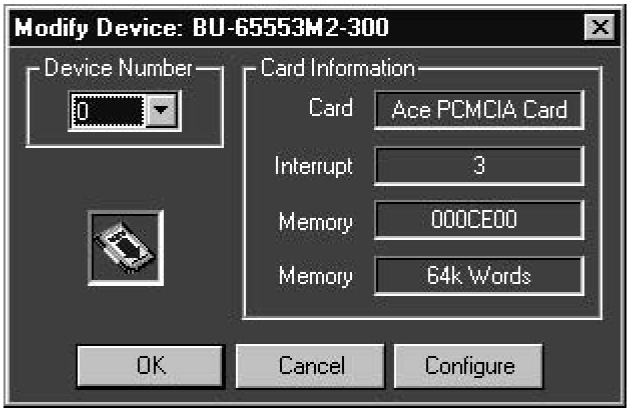
I/O Address:

Figure 27. Configuring

32) The BU-65553M2-300 card requires one interrupt and one memory address. Enter the available resources that were discovered previously from /Administrative Tools/NT Diagnostics.

33) When the resource settings are correct, click **OK**.

34) You will return to the Modify Device screen. Click **OK**.



Modify Device: BU-65553M2-300

Device Number: 0

Card Information

Card: Ace PCMCIA Card

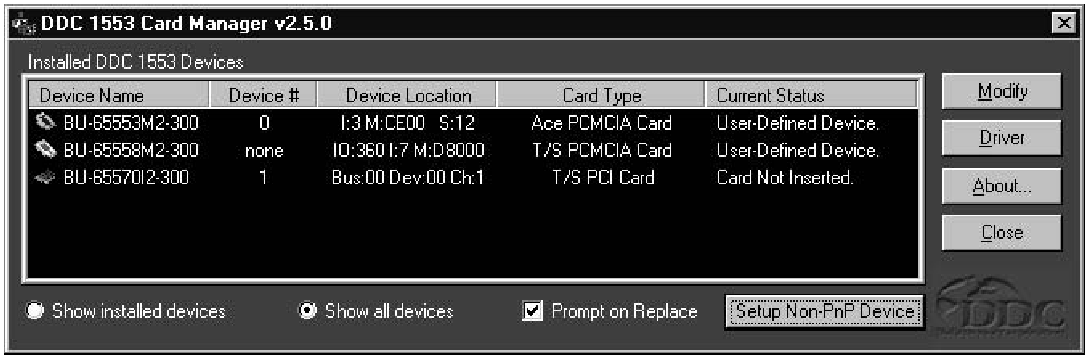
Interrupt: 3

Memory: 000CE00

Memory: 64k Words

Figure 28. Modify Device

35) The DDC 1553 card manager dialog box will reappear. Click the **Close** button.



DDC 1553 Card Manager v2.5.0

Installed DDC 1553 Devices

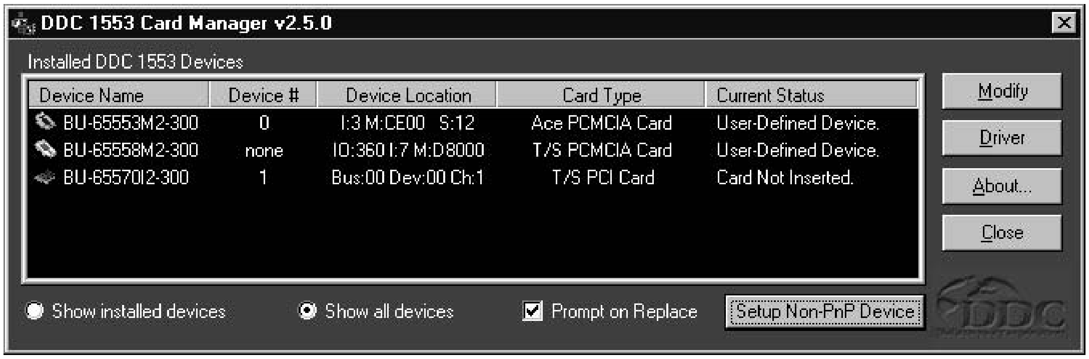
Device Name	Device #	Device Location	Card Type	Current Status
BU-65553M2-300	0	I:3 M:CE00 S:12	Ace PCMCIA Card	User-Defined Device.
BU-65558M2-300	none	IO:360 I:7 M:D8000	T/S PCMCIA Card	User-Defined Device.
BU-65570I2-300	1	Bus:00 Dev:00 Ch:1	T/S PCI Card	Card Not Inserted.

○ Show installed devices ● Show all devices ☑ Prompt on Replace

Figure 29. DDC 1553 Card Manager

36) The computer must be restarted with the 65553M2-300 card inserted in order for all changes to take effect.

37) Once the computer has rebooted, start the card manager dialog and Click the **Driver** button.



DDC 1553 Card Manager v2.5.0

Installed DDC 1553 Devices

Device Name	Device #	Device Location	Card Type	Current Status
BU-65553M2-300	0	I:3 M:CE00 S:12	Ace PCMCIA Card	User-Defined Device.
BU-65558M2-300	none	IO:360 I:7 M:D8000	T/S PCMCIA Card	User-Defined Device.
BU-65570I2-300	1	Bus:00 Dev:00 Ch:1	T/S PCI Card	Card Not Inserted.

○ Show installed devices ● Show all devices ☑ Prompt on Replace

Figure 30. DDC 1553 Card Manager

38) The Device Driver Status screen will come up. This window shows the possible action that may be taken for the selected device.

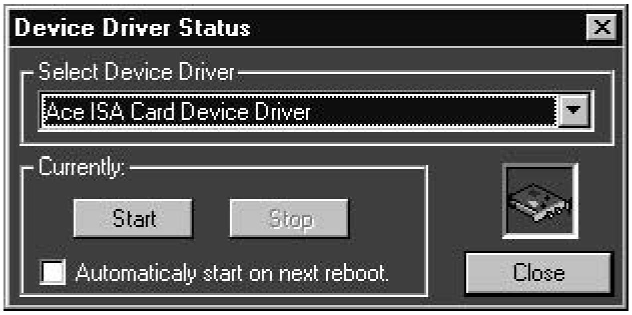


Figure 31. Device Driver Status

39) The device driver is in the halt state if the start button is active. If the stop button is active, the device driver is running.

40) The device driver can be set to start at boot-up if the Automatically start on the next reboot is checked. Click the **Close** button to continue.

DOS

If you are using DOS, perform the following installation instructions. If you are using another operating system, skip to the relevant installation section.

1) Install the card as described in the previous **HARDWARE INSTALLATION** section.

2) Turn on the computer.

3) Insert the software CD or floppy disk(s) into the computer.

4) At the ”C” prompt, type <**A:\>** (where A is the letter corresponding to the drive containing the software you inserted in step 3) and press **Enter.**

5) At the ”A” prompt, type <**setup.exe>** and press **Enter.**

6) The license agreement, disc copy, and installation progress bars will appear on the screen. Press the **DOWN** key to scroll through the information.

7) Press **ENTER** to continue, or press **ESC** to abort.

8) Select (highlight) the BU-65553-64K PCMCIA card entry by using the **UP** and **DOWN ARROW KEYS** to move the highlight and then press **ENTER** to continue.

9) The software and DDC information will be displayed. Press **ENTER** to continue, or press **ESC** to abort.

10) Select (highlight) the drive where the software will be installed in (the default drive is C). Press **ENTER** to continue.

11) Enter the directory where the software will be installed in (the default directory is \acesoft). Press **ENTER** to continue.

12) When all is complete the install will look to change auto exe.bat. This adds the statement: set acesoft = c:\acesoft (default) if a different directory was used in installation, it will be reflected here. **Y**= make change, **N** = don’t make change.

13) If ‘N’ is selected, install will instruct the user as to the necessary change. Press **Any key** to continue. Installation is complete. You must reboot the computer for the change in auto exe.bat to take affect. Test with selftest 2 in install \ dosexe *Don’t forget to place the card in the correct place as for ace.cfg.

32 Bit EMACE Drivers and Libraries for Windows 95/98

EMACE RUNTIME LIBRARY INSTALLATION.

Once the new drivers have been correctly installed, the new software libraries may be installed. The installation of the 32-bit software and menus use the InstallShield® utility. This allows for a consistent user interface when installing and removing software. If you are not familiar with this utility, follow the instructions below. If you wish to remove any of the 32 bit EMACE products, you can use the START/SETTINGS/CONTROL PANEL/Add/Remove Software utility.

The driver installation will be initiated automatically the first time the PC is powered up after the PC Card has been installed. When the Windows enumerator discovers the new hardware, the “Hardware Setup Wizard” will instruct the user to provide a disk with the appropriate drivers.

With the drivers loaded, the BU-69090 libraries may be loaded next.

1) Insert the Software CD or floppy disk labeled disk 1 into the approriate drive and run setup.exe from the Start/Run selection. InstallShield will proceed with the installation.

2) You must accept the license agreement by pressing the ‘YES’ button.

3) The next screen presents the default selection for the install directory. Click the ‘BROWSE’ button or type in the desired directory or select it from the directory tree to change the installation directory.

4) The next screen will present the default group that the software will be selectable from.

5) Finally, the Library software will be copied to the selected directory on the hard drive.

FINAL INSTALLATION PROCEDURES

After you have installed the hardware drivers, and the software libraries, and re-started your computer, there is one more installation step to perform.

1) Click into ‘Control Panel’ (START/SETTINGS/CONTROL PANEL).

2) Now double-click on the ‘DDC 1553 Card Manager’ icon. This will show all of the DDC devices you have installed in the computer. For each device entry you must select a Device Number. You do this by double clicking on the device part number, and then unselect the NONE box and select one of the device numbers from the drop-down list. The new Card Manager allows for up to 32 devices.

3) Select OK and you are ready to go.

Please refer to Testing the Installation on page 35.

32 Bit EMACE Drivers and Libraries for Windows NT

The installation for the new EMACE library and drivers is slightly different for Windows NT than it is for Windows 95/98. Windows NT 4.0 will not automatically recognize the PC Card even though the card provides for PnP compatibility. The drivers for the card will be installed with the rest of the EMACE Runtime Library when disk 1 is inserted and the SETUP.EXE program is run.

Install the drivers and library by inserting the Software CD or floppy disk labeled disk 1, and running the setup.exe program. This will install the system files, the library files and the control panel ‘DDC 1553 Card Manager’ applet. When the setup program is running, a dialog will be presented to the user to select the card type to install. If the computer has multiple ACE cards, select one type now, the others may be installed later using the ‘DDC 1553 Card Manager’ applet.

When the setup.exe program is complete, you must reboot the computer.

FINAL INSTALLATION PROCEDURES

The final steps in installing the new EMACE software require a device number be assigned for each installed card. This procedure is identical to the one used for the standard ACE in Windows NT. Refer to the previous section for the proper operations.

Testing the Installation

Once the hardware and software are installed, you can test the installation by running one of the sample programs that is shipped with the software. Follow the steps below to test the installation.

1) From a Command prompt, change to the directory ‘C:\Program Files\Data Device Corporation\ACE5x\EXE’. If the installation is to a different directory, please modify this command.

2) Run the selftst2.exe program with the command line `< SELFTST2 0 >`. This program requires a device parameter. The 0 indicates that the hardware is defined as device #0 in the ACE Manager applet. This parameter should be modified as required per the installation. If you have more than one device installed in the system, then running SELFTST2 with the appropriate parameter, 0, 1, 2 or 3 should test each of the cards individually.

If all went well, you should have passed all elements of the test, and are now ready to use your 1553 card/software.

If SELFTST2.EXE did not pass, refer to Troubleshooting the Installation on page 35 of this manual or contact Technical Support.

Troubleshooting the Installation

In most cases, the installation should complete without any problems, and running the self-test should result in all tests passing. The most common problems result from incorrect resource selection. These errors will be detected during the installation of the software or when the resources are being selected in the control panel applet. The first step to correcting this type of problem is to run the NT Diagnostics program in order to locate unused resources (interrupt, I/O and Memory). Once the necessary resources have been located, they should be specified in ACE Manager for Windows NT control panel applet for the installed device.

There are some other situations that can cause problems during the installation. The most common of these are listed below.

BU-107 is returned when an attempt to run selftst2 or any of the other sample programs. This fault is almost always related to the lack of a device number. Please refer to Final Installation Procedures on page 33 for Windows 95/98 or page 34 for Windows NT.

16 Bit ACE Runtime Library (BUS-69080)

Presently, there is no support for the new EMACE library from DOS or Windows 3.1. If it is required to use the BU-65553 in the DOS or Windows 3.x operating system environments, the user will have to use the card in the previous version of ACE/mini-ACE mode. The following paragraphs describe the installation and setup of the 16-bit software.

INSTALLING 16-BIT LIBRARY IN WINDOWS 95/98

In many cases, existing software created for ACE boards might have been compiled with a 16-bit compiler, and was targeted to DOS. New computers are now supplied with Windows 95/98, and do not have a native DOS setup. It is possible to run the old software on the new computers by following the following steps.

First, and most important, the ACE board must be installed in the Windows 95 environment. This means installing the board (ISA, PCMCIA, or PCI) and then having Windows install the proper drivers required for the hardware. Please refer to the preceding sections on installation.

Next, the Control Panel **|** System **|** Device Manager should be checked to ensure that the hardware was installed correctly, and that it is working correctly. This may be performed by accessing the Data Device Corp part is located under the MIL-STD-1553 device entry. If it is, then the Properties **|** Resources for this should be checked. No conflicts should be present. If the card type is a PCMCIA PC Card, then in the Properties you will see an Interrupt and either 2 or 3 Memory entries. If 3 memory entries are present, the second and third entries must be contiguous. If they are not, they must be manually changed as described earlier in the installation section. In all cases, the ”Use Automatic Settings” MUST be unchecked. This is the only way to ensure that windows will not move the resources each time the computer is booted. This is only important when running the 16-bit software.

After the control panel properties have been checked and modified, the Config.sys file must be updated to include an EMM386 statement that excludes all memory ranges used by the ACE card. The statement will look like ”DEVICE=C:\WINDOWS\EMM386 RAM X=D000-D7FF”. This will protect the card memory when running in the DOS mode. Access the Config.sys file by selecting the START **|** RUN and typing SYSEDIT.EXE in the edit box.

Now, the 16 bit BUS-69080 software should be loaded in the computer. This will provide the required files for compiling and running the 16-bit software. Primarily, it provides the environment variable ”ACESOFT” and the configuration file ”ACE.CFG”. There are a handful of cfg files. In order to use the PCMCIA cards with 16-bit software under Windows 95, the 65550W.CFG file should be copied to ACE.CFG. The contents of the ACE.CFG file should be changed to reflect the resources that are used by the ACE card that are described in the device manager. This would include the interrupt, the first (register) and second (memory) memory range, and the size. The memory values must be of the format “0XXXX“, where the XXXX are the significant values as found in the properties. For example, if Windows reports that the first memory range is 000D1000-000D1FFF, then the value placed in the ACE.CFG register value should be 0D100. NOTE: That the first two 0's and the last 0 are dropped. This should be also be performed for the memory address range. The interrupt is straight forward, and the size should be 1000 (4K cards), 3000 (12K cards), 10000 (64K cards).

Ensure that the environment variable is set by looking at the Autoexec.bat (also accessed from SYSEDIT), and verifying that it includes the statement “SET ACESOFT=C:\ACESOFT“. If you installed the software to a different disk, or a different directory, then change the statement accordingly.

Now you should reboot the computer. After the computer is running again, access a DOS prompt and run C:\ACESOFT\DOSEXE\SELFTST2. If all went well, the results will be passed on all tests.

If there are problems, the usual cause is that the resources do not match those used by Windows 95/98. Check the resources used by the card in the device manager and make sure that these values are repeated in the ACE.CFG file. Also ensure that the environment variable is pointing to the directory in which the ACE.CFG file is located.

ACE Windows Menu

The ACE Menu is a powerful user interface to the MIL-STD-1553 bus and runs on top of Windows. The ACE Menu for Windows 95/98 and Windows NT are included as standard software supplied with the ***BU-65553*** PC Cards. The ACE Menu software, setup files, and stack files are 100% compatible with all other ACE based 1553 PC boards supplied by DDC. This software presently supports only the ACE capabilities of the ***BU-65553*** card.

When using the ACE Menu, the user has full control of the Bus Controller, Remote Terminal, Monitor and Self-Test functions from an easy to use interface. Using the intuitively designed controls in this menu, the user has the capability of setting up messages, minor frames, major frames, timing, filtering and many other functions required by the beginning and advanced MIL-STD-1553 user. Without programming a line of code, the ACE Menu enables the user to quickly get started using the ACE family products.

32 Bit ACE Menu Software (BUS-69084 / BUS-69085)

The ACE Menu for Windows 95/98 and Windows NT is a native 32-bit program that provides a simple to use Graphical User Interface (GUI). This GUI will help the user quickly setup and run Bus Controller, Remote Terminal or Monitor sessions on a PC equipped with a ***BU-65553*** PC Card or any of the other DDC ACE based 1553 PC cards.

The ACE 32 Bit Menu requires approximately 1 Meg of hard disk space. The installation uses InstallShield, which provides a standard user interface for installation and removal of software products.

As a general guide, all active programs should be closed during installation of any software. Once all programs have been terminated, you may proceed with installation. During installation, it will be assumed that the floppy drive used is the A: drive and the target drive for installation is denoted as “C:”. If your system requirements are different, please substitute the appropriate values.

INSTALL 32-BIT ACE MENU FOR WINDOWS 95/98 AND WINDOWS NT

Note that the text is written for Windows 95/98. If the user is installing for Windows NT the substitution of Windows NT for Windows 95/98 should be made. In order to run the ACE Menu, the drivers for the card must be successfully installed. Please refer to sections '32 Bit EMACE Drivers and Libraries for Windows 95/98' on page 32and '32 Bit EMACE Drivers and Libraries for Windows NT' on page 34 for details on installing and configuring the device drivers.

1) Insert the Software CD or floppy disk labeled disk 1 into the appropriate drive. Click the START button and then select RUN. When the RUN window appears, enter A:\SETUP.EXE in the edit window, or you may use the BROWSE button to obtain the setup program on A: drive. Next click the OK button to continue.

2) The next window will be the DDC CORPORATION banner and Install Shield setup.

3) After Install Shield has successfully setup, you will see a window containing 'ACE MENU for Windows 9x ver. 3.1 (BUS-69084)' and an Install Shield welcome. Click NEXT to continue, or CANCEL to halt installation.

4) You will now have to agree to a License for use. If you select YES, you will be bound by the License, if you select NO, then installation will halt, and if you select BACK, install shield will take you back to the previous screen.

5) Next, select the installation destination drive and directory. The default value for this entry is 'C:\Program Files\Data Device Corp\AceMenu'. You may use the BROWSE button to select an existing drive and directory. The NEXT button continues the installation, the BACK button takes you back to the License agreement, and the CANCEL button halts installation.

6) Select a program folder that will contain the program and help files for the ACE Menu. This folder will show up in the START/PROGRAMS popup window, with the same name that is entered here. The default value for this entry is 'Data Device Corporation\Ace Menu 3.1'. The NEXT button continues the installation, the BACK button takes you back to the directory selection window, and the CANCEL button halts installation.

7) At this point, the files required for ACE Menu will be copied to the hard drive and the folders will be created.

8) The last window to be displayed is SETUP COMPLETE. Click the FINISH button to complete the InstallShield setup.

You do not have to reboot the system for this installation.

Please note that if you are installing the new version of the ACE Menu over the old version, you should ensure that the old version was removed with the uninstall utility provided in the control panel application 'ADD / REMOVE PROGRAMS'. If the old version is not removed there is a possibility that the old ACE Menu will be run with the new drivers. This will create a situation where the driver will report that the hardware could not be opened. You will have to manually remove the entry in the startup menu. This may be performed by accessing START / SETTINGS / TASKBAR… then click the 'Start Menu Programs' tab. From here you should click the 'Advanced' button, and then expand the 'Programs' folder entry. Finally, highlight the 'ACE Menu for Windows 95' folder, and press the delete button.

You are now ready to run ACE Menu for Windows 95/98/NT. Select '**START/PROGRAMS/Data Device Corporation/ACE Menu 3.1/ACE Menu for Windows'**. This will start the menu program and you should see the 'Ace32 Windows Application' window appear. To insure everything is working correctly, access the FILE menu and click the NEW menu entry. Now you should click the TEST button or select Test from the menu. Next click the ALL button. This will perform a basic self-test of the ACE hardware registers, protocol, memory, and interrupts. If the test passes, then you are ready for operation. If the test fails, check the installation of the ACE library and drivers.

From here you should refer to the ACE Menu User's guide, Help and ReadMe files.

INSTALL 16-BIT ACE MENU SOFTWARE (BUS-69081)

The 16-bit menu software will only run in the Windows shell. If it is installed under DOS, it will attempt to setup the Windows groups and the group names. This software requires the successful installation of the BUS-69080 ACE 16-bit software.

From DOS

Windows 3.X will automatically be spawned and the INSTALL.EXE program will be run from Windows. Please refer to the section From Windows for the steps needed to complete the installation.

From Windows

1) Insert the installation disk into the appropriate disk drive and select **RUN** from Program Manager's file menu. In the RUN window, type <**A:\INSTALL.EXE**>, where 'A:' is the letter of the disk drive you are installing from and click OK.

2) You will now be asked to select a card, choose one of the following by single clicking to highlight the choice. When the selection is made, click the 'OK' button to continue. As with the Run Time Library, the DOS and Windows 3.x version of the menu do not directly support the ***BU-65553***, so the user will have to select one of the previous versions of the PCMCIA card during installation.

   BU-65550 **PCMCIA Windows 3.1**

   BU-65550 **PCMCIA Windows 95**

   BU-65539 **16 BIT ISA CARD**

3) Next, you will be asked to provide the Windows Program Manager Group name for the ACEMENU group, the default value is: **ACE MENU V 2.5**.

4) The next message will explain that ACE MENU 2.5 will be installed, and that the Autoexec.bat file will be modified. Click 'OK' to continue or 'Cancel' to abort the installation. Note that the Autoexec.bat file will not be changed at this point. The option to do so automatically or manually will be presented in a different message.

5) On the next screen, you will be prompted to select the drive to install the software. Again, the selected choice should be highlighted. To change the selection, single click the desired option or scroll up or down by using the arrow keys. Click ‘OK’ to continue, ‘Cancel’ to abort.

6) The subdirectory will be entered next. This default subdirectory is \ACEMENU. A different subdirectory may be entered into the edit box. Click ‘OK’ to continue, ‘Cancel’ to abort.

7) At this point all subdirectories will be created, and all files will be transferred to the hard drive. A progress bar will be displayed showing the percent complete.

8) The Group and program Icons will be installed after all files have been transferred. A message will be displayed informing you that these items and all required PIF files will be created. Click ‘OK’ to continue or ‘Cancel’ to abort.

9) The next message will ask if automatic modification of the Autoexec.bat file may be performed. These changes are required by the ACE Menu program to locate information about the installation directory. Click ‘Yes’ to allow automatic modification or ‘No’ to skip automatic modification. If ‘No’ is chosen, the next message will display the required changes to the Autoexec.bat file that you will have to make manually. The default change will add the statement ‘SET ACEMENU=C:\ACEMENU’ to the Autoexec.bat. This will be different if the install directory was changed from the default location.

10) The next message informs you that the ACEMENU is finished installing and that the computer must be re-booted to allow the required changes to the Autoexec.bat file to take affect. Click ‘OK’ to continue or ‘Cancel’ to abort.

11) The last message indicates that the installation program will exit. Click ‘OK’ to continue.

Other Considerations For Installation

SYSTEM RESOURCES

There are special considerations that must be addressed when working in DOS/Windows 3.1X, and Windows NT that are not as important when working under Windows 95/98. The managing of system resources (memory and interrupts) is very closely monitored in Windows 95/98, and practically non-existent in the other systems. The burden is on the user to make sure all system resources are correctly specified as used and free. Once the user has determined what memory resources and interrupts are available, then the DOS/Windows 3.X and Windows NT installation may be completed. When using Windows 95/98, most of the user decisions go away because the operating system keeps a close watch on its resources. In some cases though, even when using Windows 95/98, some tweaking of resources used must be performed. This was demonstrated in the Windows 95/98 driver installation section.

CONFIGURATION FILES FOR 16 BIT SOFTWARE

The 16-bit BUS-69080 ACE Runtime Library and BUS-69081 ACE Menu make use of configuration files. The programmer also has the ability to use configuration files in his applications when developing 16-bit programs in the Windows 95 environment. The configuration file used by the Library is named, by default, ACE.CFG and the configuration file used by the Menu is named ACEMENU.CFG. The format of the file is the same for both the library and the menu. The files can be found in their respective software directories, which are pointed to by the ACESOFT and ACEMENU environmental variables.

The configuration files are used to store hardware dependent parameters. The file format is the same for both the library and the menu. The files have the following syntax:

```
<keyword>=<value>
```

***Note:** The configuration files are used differently with the DOS/Windows 3.1x real mode drivers as compared to the Windows 95 protected mode drivers. The differences in the configuration file contents are described in the paragraphs, which follow.*

CONFIGURATION FILES FOR DOS AND WINDOWS 3.1X

When using DOS real mode Card Services drivers for operation in either DOS or Windows 3.x the configuration file requires two entries:

`card=65550`	(Used to identify the card)
`slot=0`	(Used to specify which slot the PC Card is plugged into)

As per the PC Card standard, slots must be numbered sequentially starting from slot zero. The configuration files for ‘real mode’ support will rarely need to be modified.

16-BIT CONFIGURATION FILES FOR WINDOWS 95

When using Windows 95/98 protected mode Card Services for operation in Windows 95/98 the configuration file requires the following five entries:

```
card=65550W

register=0D100

memory=0D200

size=3000

interrupt=10
```

Card: This keyword determines the type of card you are using. The “W“ in the value indicates Windows 95/98 protected mode Card Services support. For 4K byte cards, the Card entry should contain 65551W, for all other memory configurations, the Card entry should have 65550W.

Register: This keyword contains the base address of the PC Card registers in hexadecimal. (size: 8K bytes)

Memory: This keyword contains the base address of the PC Card memory in hexadecimal. (size: ***BU-65550*** = 24K bytes, ***BU-65551*** = 8K bytes, ***BU-65552*** = 128K bytes)

Size: This keyword determines how much memory is allocated for the card. The ***BU-65550*** requires 0x3000 in hexadecimal (12K words). For the ***BU-65551***, this value should be 0x1000 (4K words). The BU-65552 should be set to 0x10000 (64K words).

Interrupt: This keyword contains the interrupt request level that the PC Card will use.

IMPORTANT NOTE: *The REGISTER, MEMORY, and INTERRUPT keywords may need to be changed manually. Do not change the order of the keywords or insert any blank lines between or above the keywords. More information on allocating Windows 95 resources and changing configuration file parameters can be found in the Hardware Installation section.*

The Register Key specifies the memory window used by the PC Cards registers. This key may be filled using one of the following values.

Register Range

D0000-D0FFF   Memory Range #1 -possible locations in the D000 segment.

D1000-D1FFF

D2000-D2FFF

D3000-D3FFF

•

•

•

DF000-DFFFF

The Memory Key specifies the start of the memory window used by the PC Cards memory. This key may be filled using one of the following values.

Memory Range

D2000-D3FFF

D6000-D7FFF

DA000-DBFFF

If the 16-bit software is being installed in a Windows 95/98 environment, the memory base addresses should be selected based on the address that was given by the installation of the 32-bit version. With this in mind, it is usually a better choice to install the 32-bit version of the software even though it is not the target usage. When the 32-bit software is installed, the operating system will provide the addresses that can be used in the configuration of the 16-bit software version.

MEMORY BASE ADDRESS SELECTION

All versions of the ACE PCMCIA card require 32K bytes (16 K words), a half segment, between 640K and 1024K in the PC's first megabyte of RAM to memory map the card. The ***BU-65553*** also requires an additional 4K block of memory in the same upper memory area. Due to I/O address mapping, the memory base address is software programmable and may be configured to any part of a segment without setting jumpers on the card. It should be noted, however, that some or all of the upper memory may be used by other devices (refer to the next section on Extended Memory Managers). Table 2 gives a typical memory map to help in choosing a memory that is not in use. The default memory base address is D000 and is usually free. If you are operating under DOS/Windows 3.X, you may want to try using Microsoft's MSD.EXE program. This is supplied with the later versions of DOS, and gives a fairly accurate picture of the memory and interrupt usage.

Table 2. Upper Memory Allocations

MEMORY BASE HEX ADDRESS	DESCRIPTION
0000-9FFF	640 K Base Memory
A000-AFFF	64 K
B000-BFFF	64 K May be used for Video Ram
C000-CFFF	64 K Reserved for BIOS Extensions
D000-DFFF	64 K
E000-EFFF	64 K ***Note:*** *on the newer Pentium class computers this area may be used during boot, and could give sporadic results if used.*
F000-FFFF	64 K Reserved for BIOS

INTERRUPT LEVEL SELECTION

The interrupt request level (IRQ) is also software programmable and can be 3, 4, 5, 7, 10, 11, 12 14, or 15. Selecting level 0, 1, 2, 6, 8, 9, or 13 will disable interrupts. Table 3 shows a typical interrupt map to help guide your selection. The default interrupt value is 10.

Table 3. Typical Interrupt Map

INTERRUPT LEVEL	ISA DEFAULT	**AVAILABILITY**
IRQ 3	COM 2	Sometimes
IRQ 4	COM 1	No
IRQ 5	LPT 2 (default for IDEA Card)	Yes
IRQ 7	LPT 1	No
IRQ 10	Available	Yes
IRQ 11	Available	Yes
IRQ 12	Available	Yes
IRQ 14	Hard Disk Controller	No
IRQ 15	Available	Yes

MODIFYING THE WINDOWS 95 OR NT DEVICE RESOURCES FOR THE PC CARD

If you find it necessary to modify the register or memory parameters setup by Windows 95/98 or NT for the 1553 PC Card, perform the following procedures. It is not likely that this should be required and DDC does not recommend altering these settings.

Double click on the SYSTEM icon in the Control Panel and bring up the Device Manager tab. With the PC Card inserted you will notice a new device class ‘MIL-STD-1553’. The hardware resources for the card may now be configured. Windows 95/98 automatically allocates hardware resources on installation and they should not be in conflict with other devices on your system. For Windows NT, these settings would be entered and modified manually via the ‘DDC 1553 CARD MANAGER’ Control Panel applet.

Resource allocation is accomplished by double clicking on the new MIL-STD-1553 Device Class and then double clicking on the ’Data Device Corp. BU-6555XXX-XXX’ device. The tree is displayed below:

```
+ MIL-STD-1553
  └──────── Data Device Corp.  BU-6555XXX-XXX
```

The properties dialogue box for the PC Card should now be displayed. Click on the Resource tab to show the currently configured hardware resources. To change these settings, uncheck the ’Use automatic settings’ check box.

***NOTE**: To examine the memory and interrupt resources for your particular system, double click on the ’*Computer’ *Device Class in the Device Manager tab of System Properties.*

After removing the check from the ’Use automatic settings’ box, double click on the INTERRUPT REQUEST resource. The Edit Interrupt Request dialog box will appear with a VALUE and CONFLICT INFORMATION. The conflict information should read ’No devices are conflicting’, if it does not, then scroll the value until it does. Write down the interrupt request level you will be using for the 1553 card before clicking **OK**. You will need the interrupt value later in order to update the configuration files (ACE.CFG, ACEMENU.CFG) for 16-bit programs.

Next the memory resources must be configured. The ***BU-65553*** uses two memory windows. The first window is 4K bytes long and is used by the registers on the card. This window can be configured by double clicking on the first MEMORY RANGE in the Resource Settings box (at this point you should still be in ***BU-6555X*** Properties). This will bring up the Edit Memory Range dialogue box. Similar to the Edit Interrupt Request box, the Edit Memory Range box contains a VALUE and CONFLICT INFORMATION. If the CONFLICT INFORMATION displays ’No devices conflicting’ after changing to this value then write down the starting address of the memory in segment form (e.g. if using the range of CF000-CFFFF then the starting address in segment form will be 0CF00) and click the **OK** button. If the message indicates that there is a resource conflict, then scroll to the next available resource that is free and click OK. Below are examples of valid memory blocks for a 4K-byte memory range:

Memory Range #1 -possible locations in the D000 segment

D0000-D0FFF

D1000-D1FFF on 4K byte boundaries.

D2000-D2FFF

D3000-D3FFF

-
-
-

DF000-DFFFF

There is one more memory range for the ***BU-65553*** (32K-byte) that needs to be configured. This memory range must start on a 32K-byte boundary. Double click on the second MEMORY RANGE in the Resource Settings box to edit the memory range for the 32K-byte block. Starting at D0000-D7FFF (recommended range), find a free 32K memory range and write down the starting address in segment form (e.g. D0000-D7FFF would have a starting address in segment form of 0D000). Once the address has been written down click the OK button. The following are a few of the 8K byte memory ranges and subsequent 16K byte memory ranges that can be used:

Memory Range #2 (32K-byte)

C8000-CFFFF

D0000-D7FFF

D8000-DFFFF

CONNECTION TO A MIL-STD-1553 BUS

Figure 32 Illustrates the interface between the BU-65553 to a 1553 bus for transformer (long stub) or direct (short stub) coupling, plus the peak-to-peak voltage levels that appear at various points (when transmitting).

Both transformer and direct coupling configurations require the use of an isolation transformer that interfaces directly to the PC Card. For the transformer (long stub) coupling configuration, a second transformer, known as a coupling transformer, is required. In accordance with MIL-STD-1553B, the turns-ratio of the coupling transformer is 1.0 to 1.4.

Both coupling configurations also require an isolation resister to be placed in series with each leg of the transformer connecting to the 1553 bus; this protects the bus against short circuit conditions in the transformers, stubs, or terminal components.

The standard cable provided with the BU-65553 provides for a transformer-coupled connection. The mating connector required on the stub cable is a Trompeter PL75 or equivalent connector. Direct coupling requires the use of an optional cable assembly that may be purchased from DDC.

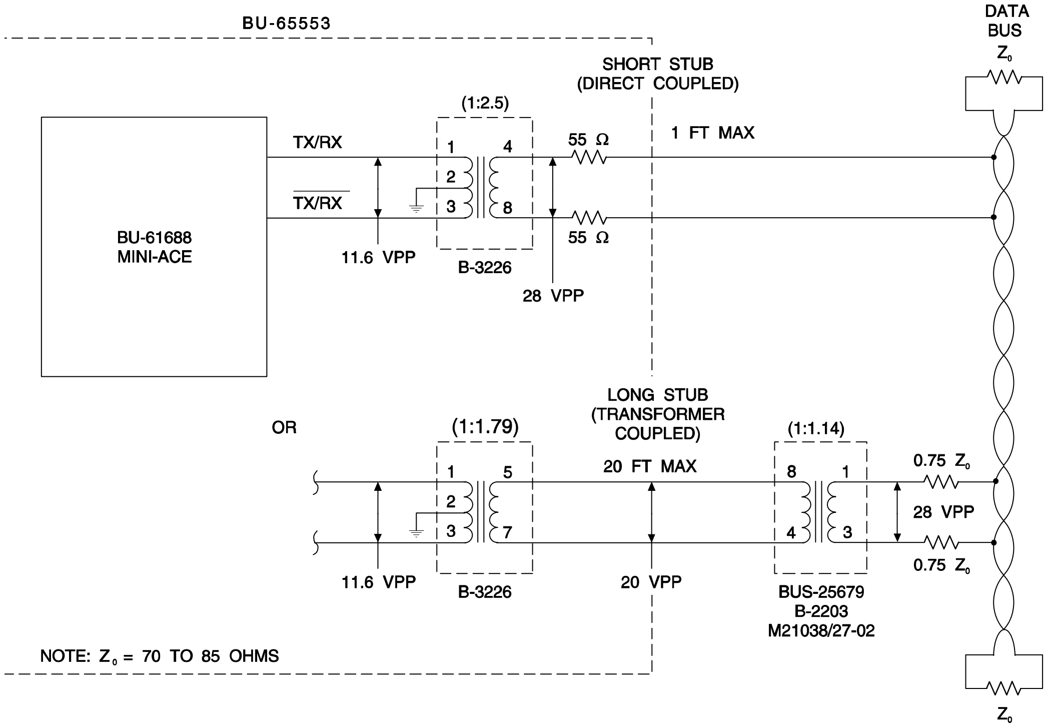


Figure 32. Interface to a MIL-STD-1553 BUS

"Simulated Bus" (Lab Bench) Interconnections

For purposes of software development and system integration, it is generally not necessary to integrate the required couplers, terminators, etc. that comprise a complete MIL-STD-1553B bus. In most instances, a simplified electrical configuration will suffice. The interconnection methods illustrated in Figure 33 allows the unit under test to be interfaced over a "simulated bus" to simulation and test equipment. The length of the "simulated bus" should not exceed 5 feet. It is important to note that the **termination resistors indicated are necessary** (if not already present within the test/simulation equipment) in order to ensure reliable communications between the PC Card and simulation/test equipment. As illustrated in Figure 33, the 78ohm and 39ohm termination resistors should be physically located as close as possible to the test/simulation equipment.

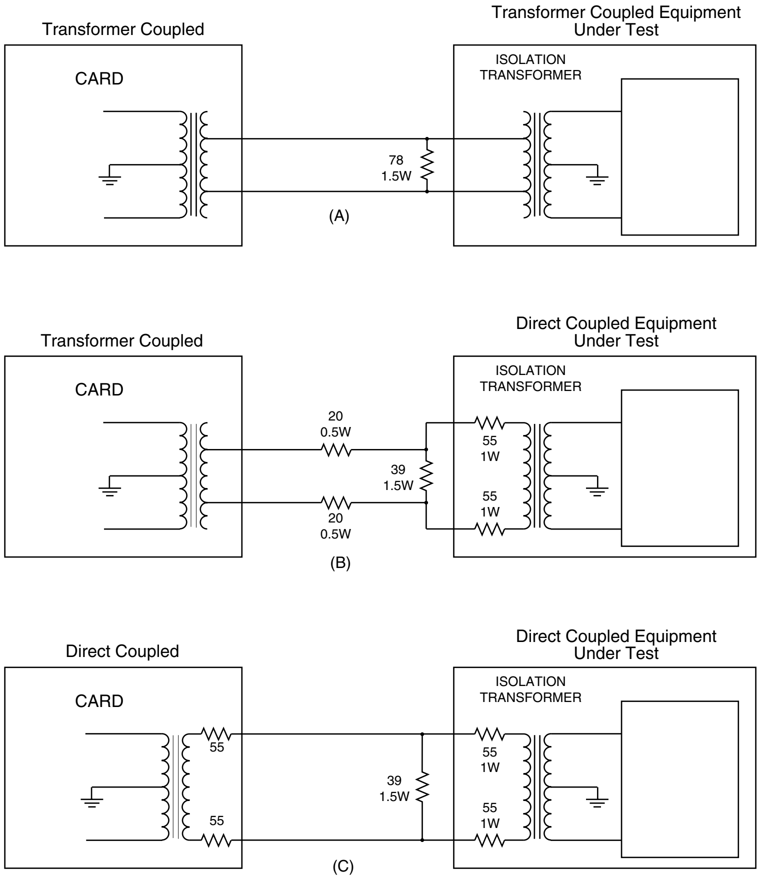


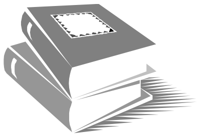
Figure 33. Simulated Bus Interconnections
(A) Transformer Coupled to Transformer Coupled
(B) Transformer Coupled to Direct Coupled
(C) Direct Coupled to Direct Coupled

SOFTWARE DEVELOPMENT LIBRARIES

The software development libraries supplied with the PC Card are written in ‘C’. Previous versions of the PCMCIA card provided 16-bit and 32-bit versions of the Run Time Library. The EMACE version of the card (***BU-65553***) supports both 16-bit and 32-bit, but only the 32-bit version is capable of supporting the advanced operations of the EMACE. If 16-bit or the previous versions of the 32-bit software capabilities is required, please refer to the appropriate documentation. This document includes only the installation and operation of the new EMACE RTL for the 32-bit Windows environments.

All the examples for the 32-bit libraries are supplied as both executable and source. The source is written in ’C’, and found in the \SAMPLE subdirectory for both versions. The executables are found in the \EXE directory for the 32-bit version.

32 Bit ACE and EMACE Runtime Library



The ***BUS-69082*** (Windows 95/98) and ***BUS-69083*** (Windows NT) ACE Runtime Libraries and the BU-69090 EMACE Library provide the framework for developing near ’real-time’ drivers and/or applications for the PC Card. The library, written in C, supports Windows 95/98/NT 32-bit applications using development tools from both Microsoft and Borland. For detailed information on the ACE Runtime Library and its Dynamic Link Library (DLL) refer to the ’BUS-69080, BUS-69082, BUS-69083 ACE RUNTIME LIBRARY SOFTWARE MANUAL’ (MN-69080-001). For details on the EMACE Runtime Library, the user should refer to the EMACE Runtime Library Software Manual (MN-69090XX-001).

PROGRAMMER'S REFERENCE

This chapter describes the hardware design and operation of the ***BU-65553*** PCMCIA card. This information is provided for users who want to create their own applications without using the library software provided with the card. This might be useful in situations where assembly code is being used.

The following sections will provide a basic understanding of the hardware register definitions. If greater detail is required, please refer to the EMACE User's Guide.

All access to the card must be performed through a card services interface. This will provide the appropriate memory mapping necessary for the user application. If the library is used, these operations will be performed automatically for the user.

The address mapping and definition for each of the Enhanced Mini-ACE registers are illustrated in the following tables:

Table 4. Enhanced Mini-ACE Registers

ADDRESS						REGISTER
A5	A4	A3	A2	A1	A0	DESCRIPTION / ACCESSIBILITY
0	0	0	0	0	0/1	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	1	0/1	Configuration Register #1 (RD/WR)
0	0	0	1	0	0/1	Configuration Register #2 (RD/WR)
0	0	0	1	1	0/1	Start/Reset Register (WR)
0	0	0	1	1	0/1	Non-Enhanced BC or RT Command Stack Pointer/Enhanced BC Instruction List Pointer Register (RD)
0	0	1	0	0	0/1	BC Control Word/RT Subaddress Control Word Register (RD/WR)
0	0	1	0	1	0/1	Time Tag Register (RD/WR)
0	0	1	1	0	0/1	Interrupt Status Register #1 (RD)
0	0	1	1	1	0/1	Configuration Register #3 (RD/WR)
0	1	0	0	0	0/1	Configuration Register #4 (RD/WR)
0	1	0	0	1	0/1	Configuration Register #5 (RD/WR)
0	1	0	1	0	0/1	RT/Monitor Data Stack Address Register (RD/WR)
0	1	0	1	1	0/1	BC Frame Time Remaining Register (RD)
0	1	1	0	0	0/1	BC Time Remaining to Next Message Register (RD)
0	1	1	0	1	0/1	BC Frame Time/Enhanced BC Initial Instruction Pointer/RT Last Command/MT Trigger Word Register (RD/WR)
0	1	1	1	0	0/1	RT Status Word Register (RD)
0	1	1	1	1	0/1	RT BIT Word Register (RD)
1	0	0	0	0	0/1	Test Mode Register 0
1	0	0	0	1	0/1	Test Mode Register 1
1	0	0	1	0	0/1	Test Mode Register 2
1	0	0	1	1	0/1	Test Mode Register 3
1	0	1	0	0	0/1	Test Mode Register 4
1	0	1	0	1	0/1	Test Mode Register 5
1	0	1	1	0	0/1	Test Mode Register 6
1	0	1	1	1	0/1	Test Mode Register 7
1	1	0	0	0	0/1	Configuration Register #6 (RD/WR)
1	1	0	0	1	0/1	Configuration Register #7 (RD/WR)
1	1	0	1	0	0/1	RESERVED
1	1	0	1	1	0/1	BC Condition Code Register (RD)
1	1	0	1	1	0/1	BC General Purpose Flag Register (WR)
1	1	1	0	0	0/1	BIT Test Status Register (RD)
1	1	1	0	1	0/1	Interrupt Mask Register #2 (RD/WR)
1	1	1	1	0	0/1	Interrupt Status Register #2 (RD)
1	1	1	1	1	0/1	BC General Purpose Queue Pointer/RT-MT Interrupt Status Queue Pointer Register (RD/WR)

Table 5. Interrupt Mask Register Read/Write 00H)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC MSG/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/ RT MODE CODE/ MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

Table 6. Configuration Register #1 (Read/Write 04H)

BIT	BC FUNCTION (Bits 11-0 Enhanced Mode Only)	RT WITHOUT ALTERNATE STATUS	RT WITH ALTERNATE STATUS (Enhanced Mode Only)	MONITOR FUNCTION (Enhanced Mode Only, bits 12-0)
15 MSB	RT/BC-MT* (Logic 0)	(Logic 1)	(Logic 1)	(Logic 0)
14	MT/BC-RT* (Logic 0)	(Logic 0)	(Logic 0)	(Logic 1)
13	CURRENT AREA B/A*	CURRENT AREA B/A*	CURRENT AREA B/A*	CURRENT AREA B/A*
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	DYNAMIC BUS CONTROL ACCEPTANCE*	S10	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	BUSY*	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	SERVICE REQUEST*	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	SUBSYSTEM FLAG*	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	RTFLAG* (enhanced mode only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTER-MESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLE / SINGLE* RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (read only)	NOT USED	S01	MONITOR ENABLED (read only)
1	BC FRAME IN PROGRESS (read only)	NOT USED	S00	MONITOR TRIGGERED (read only)
0 LSB	BC MESSAGE IN PROGRESS (read only)	RT MESSAGE IN PROGRESS (enhanced mode only) (read only)	RT MESSAGE IN PROGRESS (read only)	MONITOR ACTIVE (read only)

Table 7. Configuration Reg #2 (read/write 08H)

BIT	DESCRIPTION
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE
13	BUSY LOOK UP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDR DISBL
9	TIME TAG RESOLUTION 2 (TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

Table 8. Start/Reset Register (Write 0CH)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	RESERVED
13	RESERVED
12	RESERVED
11	CLEAR RT HALT
10	CLEAR SELF-TEST REGISTER
9	INITIATE RAM SELF-TEST
8	RESERVED
7	INITIATE PROTOCOL SELF-TEST
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

Table 9. BC/RT Command Stack Pointer Register (Read 0CH)

BIT	DESCRIPTION
15(MSB)	COMMAND STACK POINTER 15
X	X
X	X
X	X
0(LSB)	COMMAND STACK POINTER 0

Table 10. BC Control Word Reg (Read/Write 10H)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	MESSAGE ERROR MASK
13	SERVICE REQUEST BIT MASK
12	SUBSYS BUSY BIT MASK
11	SUBSYS FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/B*
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

Table 11. RT Subaddress Control Word Register (Read/Write 10H)

BIT	DESCRIPTION
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

Table 12. Time Tag Register (Read/Write 14H)

BIT	DESCRIPTION
15(MSB)	TIME TAG 15
X	X
X	X
X	X
0(LSB)	TIME TAG 0

Table 13. Interrupt Status Reg (Read/Write 18H)

BIT	DESCRIPTION
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/ RT MODE CODE/ MT PATTERN RIGGER
0(LSB)	END OF MESSAGE

Table 14. Configuration Reg #3 (Read/Write 1CH)

BIT	DESCRIPTION
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/R* ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER ENABLE
2	RTFAIL*/RTFLAG* WRAP ENABLE
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

Table 15. Configuration Reg #4 (Read/Write 20H)

BIT	DESCRIPTION
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENA/XOR*
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/SAME BUS*
7	2ND RETRY ALT/SAME BUS*
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDR WITH CONFIG. REG. #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

Table 16. Configuration Reg #5 (Read/Write 24H)

BIT	DESCRIPTION
15(MSB)	12 MHZ CLOCK SELECT (10 MHZ CLOCK SELECT for BU-61689)
14	SINGLE-ENDED SELECT
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDR LATCH/TRANSPARENT*
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

Table 17. RT/Monitor Data Stack Address Register (Read/Write 28H)

BIT	**DESCRIPTION**
15(MSB)	RT/MONITOR DATA STACK ADDRESS 15
X	X
X	X
X	X
0(LSB)	RT/MONITOR DATA STACK ADDRESS 0

Table 18. BC Frame Time Remaining Register (Read/Write 2CH)

BIT	**DESCRIPTION**
15(MSB)	BC FRAME TIME REMAINING 15
X	X
X	X
X	X
0(LSB)	BC FRAME TIME REMAINING 0

NOTE: *Resolution = 100 µs per LSB*

Table 19. BC Message Time Remaining Register (Read/Write 30H)

BIT	**DESCRIPTION**
15(MSB)	BC MESSAGE TIME REMAINING 15
X	X
X	X
X	X
0(LSB)	BC MESSAGE TIME REMAINING 0

NOTE: *Resolution = 1 µs per LSB*

Table 20. BC Frame Time/RT Last Command/Mt Trigger Reg (Read/Write 34H)

BIT	**DESCRIPTION**
15(MSB)	BIT 15
X	X
X	X
X	X
0(LSB)	BIT 0

Table 21. RT Status Word Register (Read 36H)

BIT	DESCRIPTION
15(MSB)	LOGIC ”0”
14	LOGIC ”0”
13	LOGIC ”0”
12	LOGIC ”0”
11	LOGIC ”0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

Table 22. RT Bit Word Register (Read 3CH)

BIT	DESCRIPTION
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAIL
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Table 23. Configuration Reg #6 (Read/Write 60H)

BIT	DESCRIPTION
15 MSB)	ENHANCED BUS CONTROLLER
14	ENHANCED CPU ACCESS
13	COMMAND STACK POINTER INCREMENT ON EOM (RT, MT)
12	GLOBAL CIRCULAR BUFFER
11	GLOBAL CIRCULAR BUFFER SIZE 2
10	GLOBAL CIRCULAR BUFFER SIZE 1
9	GLOBAL CIRCULAR BUFFER SIZE 0
8	INVALID MESSAGES TO INTERRUPT STATUS QUEUE
7	VALID MESSAGES TO INTERRUPT STATUS QUEUE
6	INTERRUPT STATUS QUEUE ENABLE
5	RT ADDRESS SOURCE
4	ENHANCED MESSAGE MONITOR
3	RESERVED
2	64-WORD REGISTER SPACE
1	CLOCK SELECT 1
0 (LSB)	CLOCK SELECT 0

Table 24. Configuration Reg #7 (Read/Write 64H)

BIT	DESCRIPTION
15 MSB)	MEMORY MANAGEMENT BASE ADDRESS 15
14	MEMORY MANAGEMENT BASE ADDRESS 14
13	MEMORY MANAGEMENT BASE ADDRESS 13
12	MEMORY MANAGEMENT BASE ADDRESS 12
11	MEMORY MANAGEMENT BASE ADDRESS 11
10	MEMORY MANAGEMENT BASE ADDRESS 10
9	RESERVED
8	RESERVED
7	RESERVED
6	RESERVED
5	RESERVED
4	RT HALT
3	1553B RESPONSE TIME
2	ENHANCED TIME TAG SYNCHRONIZE
1	ENHANCED BC WATCHDOG TIMER ENABLED
0 (LSB)	MODE CODE RESET/INCMD* SELECT

Table 25. BC Condition Code Register (Read 6CH)

BIT	DESCRIPTION
15 MSB)	ALWAYS
14	RETRY 1
13	RETRY 0
12	BAD MESSAGE
11	MASKED STATUS SET
10	GOOD BLOCK TRANSFER
9	FORMAT ERROR
8	NO RESPONSE
7	GENERAL PURPOSE FLAG 7
6	GENERAL PURPOSE FLAG 6
5	GENERAL PURPOSE FLAG 5
4	GENERAL PURPOSE FLAG 4
3	GENERAL PURPOSE FLAG 3
2	GENERAL PURPOSE FLAG 2
1	LESS THAN/GENERAL PURPOSE FLAG 1
0 (LSB)	EQUAL FLAG/GENERAL PURPOSE FLAG 0

Table 26. BC General Purpose Flag Register (Write 6CH)

BIT	DESCRIPTION
15 MSB)	CLEAR GENERAL PURPOSE FLAG 7
14	CLEAR GENERAL PURPOSE FLAG 6
13	CLEAR GENERAL PURPOSE FLAG 5
12	CLEAR GENERAL PURPOSE FLAG 4
11	CLEAR GENERAL PURPOSE FLAG 3
10	CLEAR GENERAL PURPOSE FLAG 2
9	CLEAR GENERAL PURPOSE FLAG 1
8	CLEAR GENERAL PURPOSE FLAG 0
7	SET GENERAL PURPOSE FLAG 7
6	SET GENERAL PURPOSE FLAG 6
5	SET GENERAL PURPOSE FLAG 5
4	SET GENERAL PURPOSE FLAG 4
3	SET GENERAL PURPOSE FLAG 3
2	SET GENERAL PURPOSE FLAG 2
1	SET GENERAL PURPOSE FLAG 1
0 (LSB)	SET GENERAL PURPOSE FLAG 0

Table 27. Bit Test Status Register (Read 70H)

BIT	DESCRIPTION
15 MSB)	PROTOCOL BUILT-IN TEST COMPLETE
14	PROTOCOL BUILT-IN TEST IN PROGRESS
13	PROTOCOL BUILT-IN TEST PASSED
12	PROTOCOL BUILT-IN TEST ABORT
11	LOGIC “1”
10	LOGIC “0”
9	LOGIC “0”
8	LOGIC “0”
7	RAM BUILT-IN TEST COMPLETE
6	RAM BUILT-IN TEST IN PROGRESS
5	RAM BUILT-IN TEST PASSED
4	LOGIC “0”
3	LOGIC “0”
2	LOGIC “0”
1	LOGIC “0”
0 (LSB)	LOGIC “0”

Table 28. Interrupt Mask Register #2 (Read/Write 74H)

BIT	DESCRIPTION
15 MSB)	NOT USED
14	BC OP CODE PARITY ERROR
13	ILLEGAL COMMAND
12	GENERAL PURPOSE QUEUE/INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0 (LSB)	NOT USED

Table 29. Interrupt Status Register #2 (Read 78H)

BIT	DESCRIPTION
15 MSB)	MASTER INTERRUPT
14	BC OP CODE PARITY ERROR
13	ILLEGAL COMMAND
12	GENERAL PURPOSE QUEUE/ INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0 (LSB)	INTERRUPT CHAIN BIT

Table 30. BC General Purpose Queue Pointer Register / RT, MT Interrupt Status Queue Pointer Register (Read/Write 7CH)

BIT	DESCRIPTION
15 SB)	QUEUE POINTER BASE ADDRESS 15
X X X	X X X
6	QUEUE POINTER BASE ADDRESS 15
5	QUEUE POINTER ADDRESS 5
X X X	X X X
0 (LSB)	QUEUE POINTER ADDRESS 0

The following tables are not registers, but are words stored in RAM:

Table 31. BC Mode Block Status Word

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

Table 32. RT Mode Block Status Word

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Table 33. 1553 Command Word

BIT	DESCRIPTION
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
X	X
X	X
X	X
11	REMOTE TERMINAL ADDRESS BIT 0
10	TRANSMIT RECEIVE
9	SUBADDRESS/MODE CODE BIT 4
X	X
X	X
X	X
5	SUBADDRESS/MODE CODE BIT 0
4	DATA WORD COUNT/MODE CODE BIT 4
X	X
X	X
X	X
0(LSB)	DATA WORD COUNT/MODE CODE BIT 0

Table 34. Word Monitor Identification Word

BIT	DESCRIPTION
15(MSB)	GAP TIME
X	X
X	X
X	X
8	GAP TIME
7	WORD FLAG
6	THIS_RT*
5	BROADCAST*
4	ERROR
3	COMMAND/DATA*
2	CHANNEL B/A*
1	CONTIGUOUS DATA/GAP*
0(LSB)	MODE_CODE*

Table 35. Message Monitor Mode Block Status Word

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Table 36. 1553B Status Word

BIT	DESCRIPTION
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPTANCE
0(LSB)	TERMINAL FLAG

Register Summary

The following is a summary of the functions of the Enhanced Mini-ACE's 24 non-test registers:

INTERRUPT MASK REGISTERS #1 AND #2

Are used to enable and disable interrupt requests for various conditions.

CONFIGURATION REGISTERS #1 AND #2

Are used to select the Enhanced Mini-ACE's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-On-Error, RT Memory Management mode selection, and control of the Time Tag operation.

START/RESET REGISTER

Is used for "command" type functions such as software reset, BC/MT Start, Interrupt reset, Time Tag Reset, Time Tag Register Test, Initiate protocol self-test, Initiate RAM self-test, Clear self-test register, and Clear RT Halt. The Start/Reset Register also includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

BC/RT COMMAND STACK REGISTER

Allows the host CPU to determine the pointer location for the current or most recent message.

BC INSTRUCTION LIST POINTER REGISTER

May be read to determine the current location of the Instruction List Pointer for the Enhanced BC mode.

BC CONTROL WORD/RT SUBADDRESS CONTROL WORD REGISTER:

In BC mode, allows host access to the current word or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retires and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress

Control Word is used to select the memory management scheme and enable interrupts for the current message. The read/write accessibility can be used as an aid for testing the Enhanced Mini-ACE.

TIME TAG REGISTER

Maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of the RAM.

INTERRUPT STATUS REGISTER #1 AND #2

Allows the host processor to determine the cause of an interrupt request by means of one or two read accesses. The interrupt events of the two Interrupt Status Registers are mapped to correspond to the respective bit positions in the two Interrupt Mask Registers. Interrupt Status Register #2 contains an INTERRUPT CHAIN bit, used to indicate an interrupt event from Interrupt Status Register #1.

CONFIGURATION REGISTERS #3, #4, AND #5

Are used to enable many of the Enhanced Mini-ACE's advanced features that were implemented by the prior generation products, the ACE and Mini-ACE (Plus). For BC, RT, and MT modes, use of the ENHANCED MODE enables the various read-only bits in Configuration Register #1. For the BC mode, the enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retires, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the enhanced mode features include the expanded RT Block Status Word, combined RT/Selective Message Monitor mode, internal wrapping of the RTFAIL* output signal to the RTFLAG* RT Status Word bit; subaddresses, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the enhanced mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

RT/MONITOR DATA STACK ADDRESS REGISTER

Provides a read/write indication of the last data word stored for RT or Monitor modes.

BC FRAME TIME REMAINING REGISTER

Provides a read-only indication of the time remaining in the current BC frame. The resolution of this register is 100 µs/LSB.

BC TIME REMAINING TO NEXT MESSAGE REGISTER

Provides a read-only indication of the time remaining before the start of the next message in a BC frame. The resolution of this register is 1 µs/LSB.

BC FRAME TIME/RT LAST COMMAND/MT TRIGGER WORD REGISTER.

In BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 µs/LS, with a range up to 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the Enhanced Mini-ACE RT. In the Word Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

BC INITIAL INSTRUCTION LIST POINTER REGISTER

Enables the host to assign the starting address for the BC Instruction List.

RT STATUS WORD REGISTER AND BIT WORD REGISTERS

Provide read-only indications of the RT Status and BIT Words.

TEST MODE REGISTERS 0-7.

These registers are included for factory test. In normal operation, these registers do not need to be accessed by the host processor.

CONFIGURATION REGISTERS #6 AND #7

Are used to enable features of Enhanced Mini-ACE's that extend beyond the architecture of the ACE/Mini-ACE (Plus). These include:

- Enhanced BC mode
- RT Global Circular Buffer (including buffer size);
- RT/MT Interrupt Status Queue,
- Valid/invalid message filtering;
- Enabling a software-assigned RT address;
- Clock frequency selection;
- Base address for the "non-data" portion of Enhanced Mini-ACE memory;
- LSB filtering for the Synchronize (with data) time tag operations;
- Enabling a watchdog timer for the Enhanced BC message sequence control engine.

BC CONDITION CODE REGISTER

Used to enable the host processor to read the current value of the Enhanced BC Message Sequence Control Engine's condition flags.

BC GENERAL PURPOSE FLAG REGISTER

Allows the host processor to be able to set, clear, or toggle any of the Enhanced BC Message Sequence Control Engine's General Purpose condition flags.

BIT TEST STATUS REGISTER

Used to provide read-only access of the status of the protocol and RAM built-in self-tests (BIT).

BC GENERAL PURPOSE QUEUE POINTER

Provides a means for initializing the pointer for the General Purpose Queue, for the Enhanced BC mode. In addition, this register enables the host to determine the current location of the General Purpose Queue pointer, which is incremented internally by the Enhanced BC message sequence control engine.

RT/MT Interrupt Status Queue Pointer Register

Provides a means for initializing the pointer for the Interrupt Status Queue, for RT, MT, and RT/MT modes. In addition, this register enables the host to determine the current location of the Interrupt Status Queue pointer, which is incremented internally by the RT/MT message processor.

Low Level Programming

BC Op-Codes

The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in Figure 34. BC Op Code Format, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identify the particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. Table 37 lists all the op codes, along with their respective mnemonic, code value, parameter, and description. Table 38 defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor, by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor, by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 **only** (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note that four (4) instructions are **unconditional**. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip (XQF). For these instructions, the Condition Code Field is “don’t care”. That is, these instructions are **always** executed, regardless of the result of the condition code test.

All other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

As shown in Table 37 many of the operations include a single-word parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message’s control/status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is “don’t care” (not used).

As described above, some of the op codes will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message control/status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case, the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message’s data word block. Note that the data word block stores **only** data words, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and “housekeeping” functions, this architecture enables the use of convenient, usable data structures, such as circular buffers and double buffers.

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack which supports a maximum of **four (4)** entries; there is also a return instruction. In the case of a call stack overrun or underrun, the BC will issue an CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time; start a new BC frame; wait for an external trigger to start a new frame; do comparisons based on frame time and time-to-next message; load the time tag or frame time registers; halt; and issue host interrupts. In the case of host interrupts, the message control processor passes a 4-bit user-defined interrupt vector to the host, by means of the Enhanced Mini-ACE's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general-purpose condition flags.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Odd Parity	OpCode Field					0	1	0	1	0	Condition Code Field				

Figure 34. BC Op Code Format

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches an undefined op code word, an op code word with even parity, or bits 9-5 of an op code word do not have a binary pattern of 01010, the message sequence control processor will immediately halt the BC's operation. In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt.

BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL

The Op Code identifies the instruction to be executed by the BC message sequence controller. These operations are listed in Table 37. Most of the operations are conditional, with execution dependent on the contents of the condition code field, see Table 38.

Table 37. BC Operations for Message Sequence Control

Instruction	Mnemonic	Op Code (hex)	Parameter	Conditional or Unconditional	Description
Execute Message	XEQ	0001	Message Control/Status Block Address	Conditional (See Note)	Executes the message at the specified Message Control/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Jump	JMP	0002	Instruction List Address	Conditional	Jump to the OpCode specified in the Instruction List if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Subroutine Call	CAL	0003	Instruction List Address	Conditional	Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag test TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is four.

NOTE: While the XEQ (Execute Message) instruction is conditional, not all condition codes may be used to enable its use. The ALWAYS and NEVER condition codes may be used. The eight general purpose flag bits, GP0 through GP7, may also be used. However, if GP0 through GP7 are used, it is imperative that the host processor **not** modify the value of the specific general purpose flag bit that enabled a particular message while that message is being processed. Similarly, the LT, GT-EQ, EQ, and NE flags, which the BC only updates by means of the CFT and CMT instructions, may also be used. However, these two flags are dual use. Therefore, if these are used, it is imperative that the host processor **not** modify the value of the specific flag (GP0 or GP1) that enabled a particular message while that message is being processed. The NORESP, FMT ERR, GD BLK XFER, MASKED STATUS SET, BAD MESSAGE, RETRY0, and RETRY1 condition codes are **not** available for use with the XEQ instruction and should not be used to enable its execution.

Table 37. BC Operations for Message Sequence Control

Instruction	Mnemonic	Op Code (hex)	Parameter	Conditional or Unconditional	Description
Subroutine Return	RTN	0004	Not Used (Don't Care)	Conditional	Return to the OpCode popped off the Cal Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Interrupt Request	IRQ	0006	Interrupt Bit Pattern in 4 LS bits	Conditional	Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (IRQ Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will not generate an interrupt.
Halt	HLT	0007	Not Used (Don't Care)	Conditional	Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Delay	DLY	0008	Delay Time Value (resolution = 1 µs/LSB)	Conditional	Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer.
Wait Until Frame Timer = 0	WFT	0009	Not Used (Don't care)	Conditional	Wait until Frame Time counter is equal to Zero before continuing execution of Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.

Table 37. BC Operations for Message Sequence Control

<table>
<tr><th>Instruction</th><th>Mnemonic</th><th>Op Code (hex)</th><th>Parameter</th><th>Conditional or Unconditional</th><th colspan="3">Description</th></tr>
<tr><td>Compare to Frame Timer</td><td>CFT</td><td>000A</td><td>Delay Time Value (resolution = 100 µs/LSB)</td><td>Unconditional</td><td colspan="3">Compare Time Value to Frame Time Counter and set or clear the LT and EQ flag based on the results of the compare.</td></tr>
<tr><td>Compare to Message Timer</td><td>CMT</td><td>000B</td><td>Delay Time Value (resolution = 1 µs/LSB)</td><td>Unconditional</td><td colspan="3">Compare Time Value to Message Time Counter and set or clear the LT and EQ flag based on the results of the compare.</td></tr>
<tr><td>GP Flag Bits</td><td>FLG</td><td>000C</td><td rowspan="6">Used to set, clear, or Toggle GP (General Purpose) flag bits (see description)</td><td rowspan="6">Unconditional</td><td colspan="3">Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 effect GP2, etc., according to the following rules:</td></tr>
<tr><td></td><td></td><td></td><td>Bit 8</td><td>Bit 0</td><td>Effect on GP0</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>0</td><td>No change</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>Set Flag</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>0</td><td>Clear Flag</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td>Toggle Flag</td></tr>
<tr><td>Load Time Tag Counter</td><td>LTT</td><td>000D</td><td>Time Value. Resolution (µs/LSB) is defined by bits 9, 8, and 7 of Configuration Register #2.</td><td>Conditional</td><td colspan="3">Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.</td></tr>
<tr><td>Load Frame Timer</td><td>LFT</td><td>000E</td><td>Time Value (resolution = 100 µs/LSB)</td><td>Conditional</td><td colspan="3">Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.</td></tr>
<tr><td>Start Frame Timer</td><td>SFT</td><td>000F</td><td>Not Used (Don't Care)</td><td>Conditional</td><td colspan="3">Start Frame Time Counter with Time Value in Time Frame register if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.</td></tr>
</table>

Table 37. BC Operations for Message Sequence Control

Instruction	Mnemonic	Op Code (hex)	Parameter	Conditional or Unconditional	Description
Push Time Tag Register	PTT	0010	Not Used (Don't Care)	Conditional	Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Block Status Word	PBS	0011	Not Used (Don't Care)	Conditional	Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Immediate Value	PSI	0012	Immediate Value	Conditional	Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Indirect	PSM	0013	Memory Address	Conditional	Push the data stored at the specified memory location on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Wait for External Trigger	WTG	0014	Not Used (Don't Care)	Conditional	Wait until a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.

Table 37. BC Operations for Message Sequence Control

Instruction	Mnemonic	Op Code (hex)	Parameter	Conditional or Unconditional	Description
Execute and Flip	XQF	0015	Message Control/Status Block Address	Unconditional	Execute (unconditionally) the message for the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, then flip bit 4 in the Message Control/Status Block Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h), rather than the old address, will be processed.

BC CONDITION CODES

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identify the particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent.

Table 38. BC Condition Codes

BIT CODE	NAME (Bit 4 = 0)	INVERSE (Bit 4 = 1)	FUNCTIONAL DESCRIPTION
0000	LT/GP0	GT/GP0*	Less than or GP0 flag. This bit is set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 and NE/GP1* flags will be set, while the GT-EQ/GP0* and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the GT-EQ/GP0 and EQ/GP1* flags will be set, while the LT/GP0 and NE/GP1* flags will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the GT-EQ/GP0* and NE/GP1* flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared. Also, General Purpose Flag 1 may be also be set or cleared by a FLG operation.
0001	EQ/GP1	NE/GP1*	Equal Flag. This bit is set or cleared after CFT or CMT operation. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set and the NE/GP1* bit will be cleared. If the value of the CMT's parameter is not equal to the value of the message time counter, then the NE/GP1* flag will be set and the EQ/GP1bit will be cleared. Also, General Purpose Flag 1 may be also be set or cleared by a FLG operation.
0002	GP2	GP2*	General Purpose Flags set or cleared by FLG operation or by host processor. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER.
0003	GP3	GP3*	
0004	GP4	GP4*	
0005	GP5	GP5*	
0006	GP6	GP6*	
0007	GP7	GP7*	

Table 38. BC Condition Codes

BIT CODE	NAME (Bit 4 = 0)	INVERSE (Bit 4 = 1)	FUNCTIONAL DESCRIPTION
0008	NORESP	RESP	NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Enhanced Mini-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.
`0009	FMT ERR	FMT ERR*	FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.
000A	GD BLK XFER	BAD BLK XFER	For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is always logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has no effect on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free.
000B	MASKED STATUS SET	MASKED STATUS CLR	Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" and the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status bits being set will result in a MASKED STATUS SET condition; and/or (2) If BROADCAST MASK ENABLED/XOR* (bit 11 of Configuration Register #4) is logic "1" and the MASK BROADCAST bit of the message's BC Control Word is logic "0" and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1.".
000C	BAD MESSAGE	GOOD MESSAGE	Indicates either a format error, loop test fail, or no response error for the most recent message. Note that a "Status Set" condition has no effect on the "BAD MESSAGE/GOOD MESSAGE" condition code.
000D	RETRY0	RETRY0*	These two bits reflect the retry status of the most recent

Table 38. BC Condition Codes

<table>
<tr><th>BIT CODE</th><th>NAME
(Bit 4 = 0)</th><th>INVERSE
(Bit 4 = 1)</th><th>FUNCTIONAL DESCRIPTION</th></tr>
<tr><td>000E</td><td>RETRY1</td><td>RETRY1*</td><td>message. The number of times that the message was retried is delineated by these two bits as shown below:
<table>
<tr><th>RETRY COUNT 1
(bit 14)</th><th>RETRY COUNT 0
(bit 13)</th><th>number of
Message Retries</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>N/A</td></tr>
<tr><td>1</td><td>1</td><td>2</td></tr>
</table></td></tr>
<tr><td>000F</td><td>ALWAYS</td><td>NEVER</td><td>The ALWAYS bit should be set (bit 4 = 0) to designate an instruction as unconditional. The NEVER bit (bit 4 = 0) can be used to implement an NOP or "skip" instruction.</td></tr>
</table>

SOFTWARE ARCHITECTURE

This following sections describe the basic software architecture for the BC, RT, and MT modes of operation for the PC Card. The RT and MT operations are virtually identical to the ACE and Mini-ACE devices. The bulk of the change is in the operation of the BC. The following paragraphs will outline the operations of the EMACE. For a more detailed description of the low-level operation of the 1553 interface please refer to the ‘EMACE User’s Guide’.

Bus Controller (BC)

The Enhanced Mini-ACE BC message sequence control capability enables a high degree of offloading of the host processor. This includes using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or “out-of-band” messages.

Execute and Flip Operation*.* The Enhanced Mini-ACE BC’s XQF, or “Execute and Flip” operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF instruction’s pointer parameter by toggling bit 4 in the pointer. That is, if the selected condition flag tests true, the value of the parameter will be updated to the value = old address XOR 0010h. As a result, the **next** time that this line in the instruction list is executed, the Message Control/Status Block at the **updated** address (**old address XOR 0010h**), rather than the one at the old address, will be processed. The operation of the XQF instruction is illustrated in Figure 35.

There are multiple ways of utilizing the “execute and flip” functionality. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to “ping-pong” between a pair of data buffers for a particular message. By so doing, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the "execute and flip" capability is in association with message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses **permanently** for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but saves BC bandwidth, by eliminating future attempts to process messages on an RT's failed channel.

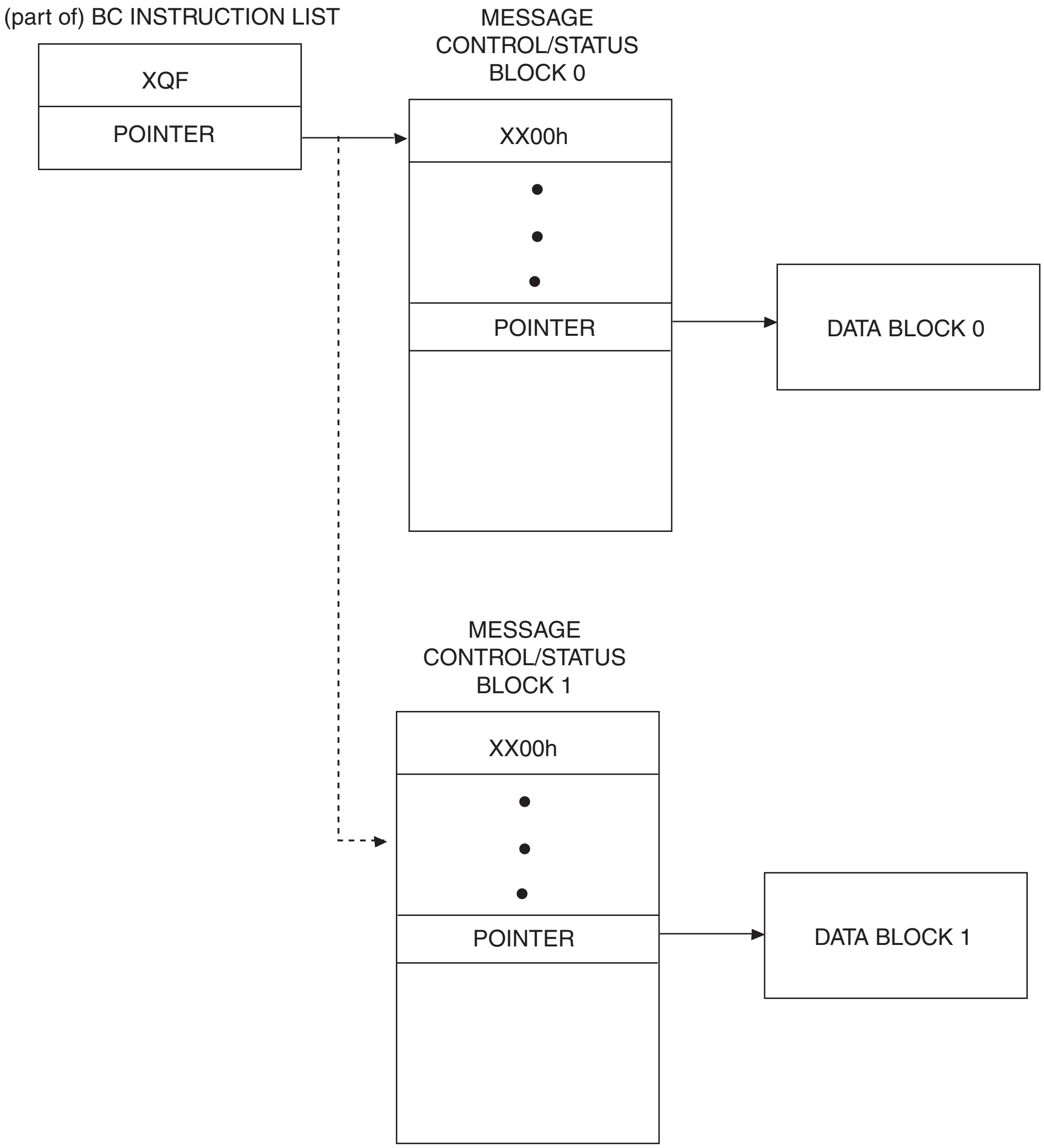

(part of) BC INSTRUCTION LIST
XQF
POINTER
MESSAGE CONTROL/STATUS BLOCK 0
XX00h
POINTER
DATA BLOCK 0
MESSAGE CONTROL/STATUS BLOCK 1
XX00h
POINTER
DATA BLOCK 1

Figure 35. Execute and Flip (XQF) Operation

General Purpose Queue. The Enhanced Mini-ACE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address.

Figure 36 illustrates the operation of the BC General Purpose Queue.

Note: *The BC General Purpose Queue Pointer Register will always point to the* ***next*** *address location (modulo 64); that is, the location* ***following*** *the last location written by the BC message sequence control engine.*

If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary.

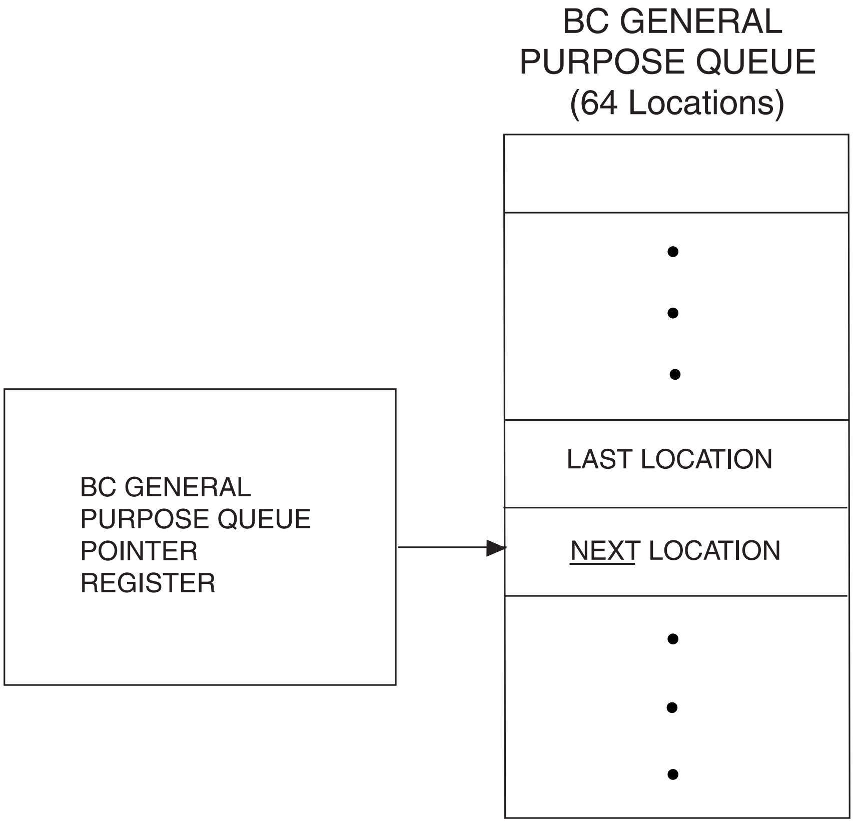


Figure 36. BC General Purpose Queue

Remote Terminal (RT) Architecture

The Remote Terminal protocol design of the PC Card represents DDC's fifth generation implementation of a 1553 RT. One of the salient features of the EMACE's RT architecture is its true multi-protocol functionality. This includes programmable options for support of MIL-STD-1553A, the various McAir protocols, and MIL-STD-1553B Notice 2. The ***BU-6555X*** RT response time is 2 to 5 µs dead time (4 to 7 µs per 1553B), providing compliance to all the 1553 protocols. Additional multi-protocol features of the ***BU-6555X*** include options for full software control of RT Status and Built-in-Test (BIT) words. Alternatively, for 1553B applications, these words may be formulated in real-time by the ***BU-6555X*** protocol logic. The new features of the EMACE are the global circular buffer and the ‘half full’ circular buffer interrupt. The ‘half full’ interrupt is useful when bulk data transfer operations are required.

The PC Card RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. Other key features of the ***BU-6555X*** RT include a set of interrupt conditions, internal command illegalization, and programmable busy by sub-address.

RT MEMORY ORGANIZATION

Table 39 illustrates a typical memory map for the PC Card in RT mode. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. Besides the Stack Pointer, for RT mode there are several other areas of the ACE address space designated as fixed locations. All RT modes of operation require the Area A and Area B Lookup Tables. Also allocated, are several fixed locations for optional features: Command Illegalization Lookup Table, Mode Code Selective Interrupt Table, Mode Code Data Table, and Busy Bit Lookup Table. It should be noted that all optional fixed locations that are not enabled might be used for general-purpose storage (data blocks).

The RT Lookup tables provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst sub-addresses to areas in the RAM. These tables occupy address range locations 0140 to 01BF for Area A and 01C0 to 023F for Area B. The RT lookup tables include Sub-address Control Words and the individual Data Block Pointers. If used, address range 0300-03FF will be dedicated as the illegalizing section of RAM. The actual Stack RAM area and the individual data blocks may be located in any area in the shared RAM address space that is not dedicated to the RT operation.

Table 39. Typical RT Memory Map (shown for 12K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101-0103	RESERVED
0104	Stack Pointer B (fixed location)
0105-0107	RESERVED
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code Data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Data Blocks 1-4
0300-03FF	Command Illegalizing Table (fixed area)
0400-041F	Data Block 5
0420-043F	Data Block 6
X	X
X	X
X	X
2FE0-2FFF	Data Block 356

Note: *Address represents the word offset from the memory base address in the common memory address space.*

RT MEMORY MANAGEMENT

Another salient feature of the ACE series products is the flexibility of its RT memory management architecture. The RT architecture allows the memory management schemes for each transmit, receive, or broadcast sub-address to be programmable on a sub-address basis. Also, in compliance with MIL-STD-1553B Notice 2, the PC Card provides an option to separate data received from broadcast messages from non-broadcast received data.

Besides supporting a global double buffering scheme (as in BC mode), the ACE RT provides a pair of 128-word Lookup Tables for memory management control, programmable on a sub-address basis (refer to Table 40). The 128-word tables include 32-word tables for transmit message pointers and receive message pointers. There is also a third, optional Lookup Table for broadcast message pointers, providing Notice 2 compliance, if necessary.

The fourth section of each of the RT Lookup Tables stores the 32 Sub-address Control Words. The individual Sub-address Control Words may be used to select the RT memory management option and interrupt scheme for each transmit, receive, and (optionally) broadcast sub-address.

For each transmit sub-address, there are two possible memory management schemes: (1) single message; and (2) circular buffer. For each receive (and optionally broadcast) sub-address, there are three possible memory management schemes: (1) single message; (2) double buffered; and (3) circular buffer. For each transmit, receive and broadcast sub-address, there are two interrupt conditions programmable by the respective Sub-address Control Word: (1) after every message to the sub-address; (2) after a circular buffer rollover. An additional table in RAM may be used to enable interrupts following selected mode code messages.

When using the circular buffer scheme for a given sub-address, the size of the circular buffer is programmable by three bits of the Sub-address Control Word (refer to Table 41). The options for circular buffer size are 128, 256, 512, 1024, 2048, 4096, and 8192 Data Words.

Table 40. RT Lookup

AREA A	AREA B	DESCRIPTION	COMMENT
0140	01C0	Rx(/Bcst)_SA0	Receive (/Broadcast) Lookup Table
X	X	X	
X	X	X	
X	X	X	
015F	01DF	Rx(/Bcst)_SA3	
0160	01E0	Tx_SA0	Transmit Lookup Table
X	X	X	
X	X	X	
X	X	X	
017F	01FF	Tx_SA31	
0180	0200	Bcst_SA0	Broadcast Lookup Table (Optional)
X	X	X	
X	X	X	
X	X	X	
019F	021F	Bcst_SA31	
01A0	0220	SACW_SA0	Subaddress Control Word Table (Optional)
X	X	X	
X	X	X	
X	X	X	
01BF	023F	SACW_SA31	

Note: *Address represents the word offset from the memory base address in the common memory address space.*

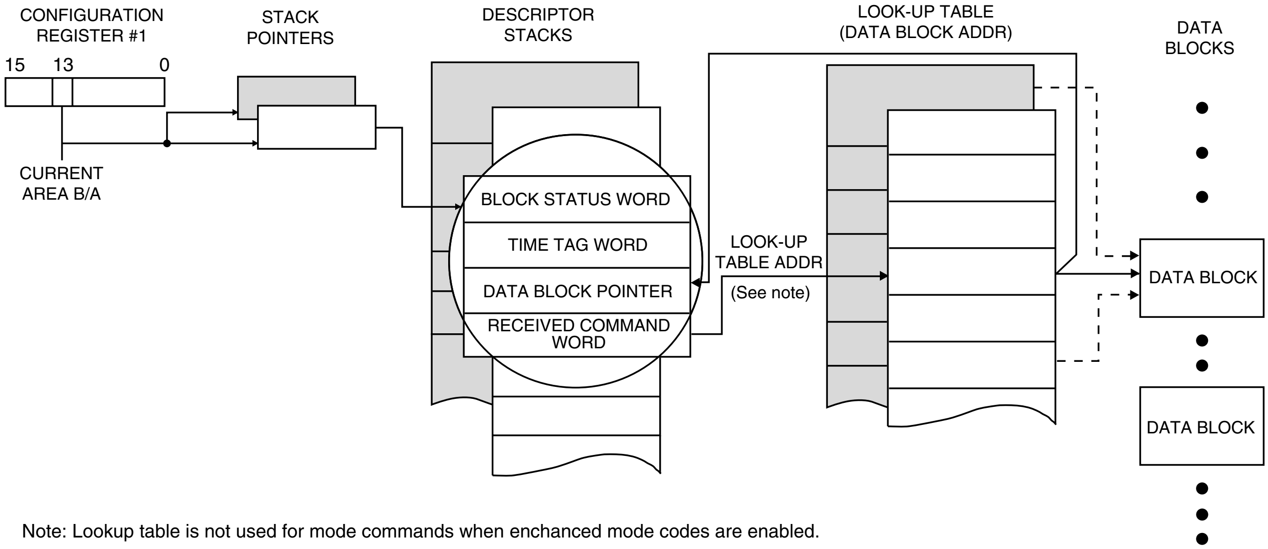
Table 41. Sub-Address Control Word Memory Management Sub-Address Buffer Scheme

MM2	MM1	MM0	DESCRIPTION	COMMENT
0	0	0	Single Message or Double Buffered	
0	0	1	128-Word	Circular Buffer of Specified Size
0	1	0	256-Word	
0	1	1	512-Word	
1	0	0	1024-Word	
1	0	1	2048-Word	
1	1		4096-Word	
1	1	1	8192-Word	

SINGLE MESSAGE MODE

Figure 37 illustrates the RT Single Message memory management scheme. When operating the PC Card in its default mode, the Single Message scheme is implemented for **all** transmit, receive, and broadcast sub-addresses. In the Single Message mode (also in the Double Buffer and Circular Buffer modes), there is a global double buffering scheme, controlled by bit 13 of Configuration Register #1. This selects from between the two sets of the various data structures shown in the figure: the Stack Pointers (fixed addresses), Descriptor Stacks (user defined addresses), RT Lookup Tables (fixed addresses), and RT Data Word blocks (user defined addresses). The following figures delineate the "active" and "inactive" areas by the non-shaded and shaded areas, respectively.

As shown, the ACE stores the Command Word from each message received, in the fourth location within the message descriptor (in the stack) for the respective message. The T/R* bit, sub-address field, and (optionally) broadcast/own address, index into the active area Lookup Table, to locate the data block pointer for the current message. The PC Card RT memory management logic then accesses the data block pointer to locate the starting address of the Data Word block for the current message. The maximum size for a RT Data Word block is 32 words.



Note: Lookup table is not used for mode commands when enchanced mode codes are enabled.

Figure 37. RT Memory Management: Single Message Mode

For a particular sub-address in the Single Message mode, there is overwriting of the contents of the data blocks for receive/broadcast sub-addresses – or over reading, for transmit sub-addresses. In the single message mode, it is possible to access multiple data blocks for the same sub address. This operation requires the intervention of the host processor to update the respective Lookup Table pointer.

To implement a data wraparound sub-address, as required by Notice 2 of MIL-STD-1553B, the Single Message scheme should be used for the wrap-around sub-address. Notice 2 recommends sub-address 30 as the wraparound sub-address.

CIRCULAR BUFFER MODE

Figure 38 illustrates the RT circular buffer memory management scheme. The circular buffer mode facilitates bulk data transfers. The size of the RT circular buffer, shown on the right side of the figure, is programmable from 128 to 8192 words (in even powers of 2) by the respective Sub-address Control Word. As in the single message mode, the host processor initially loads the individual Lookup Table entries. At the start of each message, the ACE stores the Lookup Table entry in the third position of the respective message block descriptor in the stack area of RAM, as in the Single Message mode. The ACE transfers Receive or Transmit Data Words to (from) the circular buffer, starting at the location referenced by the Lookup Table pointer.

At the end of a valid (or, optionally, invalid) message, the value of the Lookup Table entry is updated by the ACE to the location following the last address accessed for the current message. As a result, Data Words for the next message directed to the same Tx/RX(/Bcst) sub-address will be accessed from the next contiguous block of address locations within the circular buffer. As a recommended option, the Lookup Table pointers may be programmed to **not** update following an invalid receive (or broadcast) message. This method insures that only valid data is stored in the circular buffer, and any retried messages will overwrite the faulty attempts. This eliminates processing overhead for the RT's host processor. When the pointer reaches the lower boundary of the circular buffer (located at 128-, 256-, . . . 8192-word boundaries in the BU-65550 address space), the pointer moves to the top boundary of the circular buffer, as seen in Figure 38 shows.

Implementing Bulk Data Transfers: The use of the Circular Buffer scheme is ideal for bulk data transfers; that is, multiple messages to/from the same sub-address. The recommendation for such applications is to enable the circular buffer interrupt request. By so doing, the routine transfer of multiple messages to the selected sub-address, **including errors and retries**, is transparent to the RT's host processor. By strategically initializing the sub-addresses' Lookup Table pointer prior to the start of the bulk transfer buffer, the BU-65550 may be configured to issue an interrupt request only after it has received the anticipated number of valid Data Words to the designated sub-address.

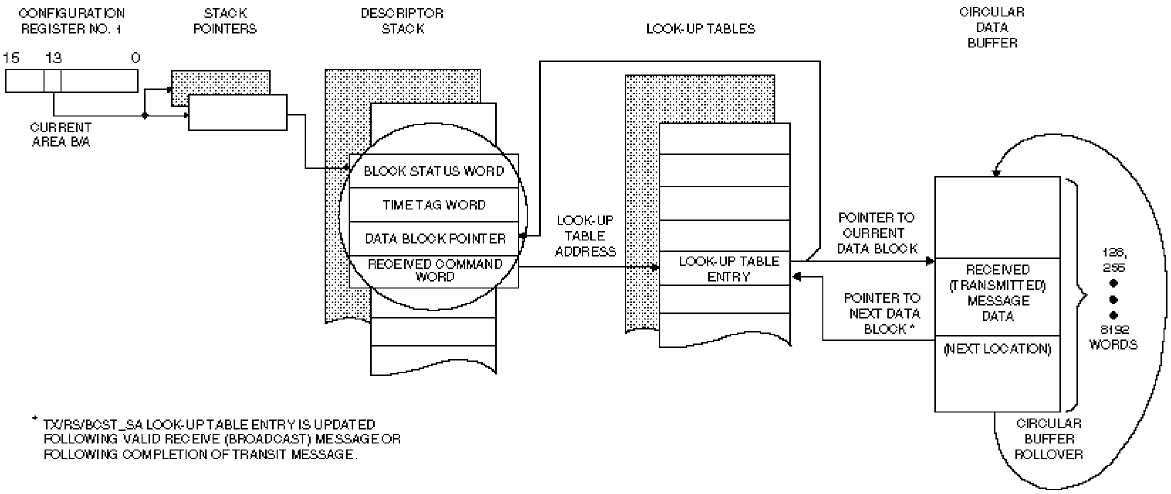

CONFIGURATION REGISTER NO. 1
15
13
0
CURRENT AREA B/A
STACK POINTERS
DESCRIPTOR STACK
BLOCK STATUS WORD
TIME TAG WORD
DATA BLOCK POINTER
RECEIVED COMMAND WORD
LOOK-UP TABLE ADDRESS
LOOK-UP TABLES
LOOK-UP TABLE ENTRY
POINTER TO CURRENT DATA BLOCK
POINTER TO NEXT DATA BLOCK *
CIRCULAR DATA BUFFER
RECEIVED (TRANSMITTED) MESSAGE DATA
(NEXT LOCATION)
128, 256 • • • 8192 WORDS
CIRCULAR BUFFER ROLLOVER
* TX/RS/BCST_SA LOOK-UP TABLE ENTRY IS UPDATED FOLLOWING VALID RECEIVE (BROADCAST) MESSAGE OR FOLLOWING COMPLETION OF TRANSIT MESSAGE.

Figure 38. RT Memory Management: Circular Buffered Mode

SUB-ADDRESS DOUBLE BUFFERING MODE

For receive (and broadcast) sub-addresses, the BU-65552 RT offers a third memory management option, Sub-address Double Buffering. Sub-address double buffering provides a means of ensuring data consistency. Figure 39 illustrates the RT Sub-address Double Buffering scheme. Like the Single Message and Circular Buffer modes, the Double Buffering mode may be selected on a sub-address basis by means of the Sub-address Control Word. The purpose of the Double Buffering mode is to provide the host processor a convenient means of accessing the most recent, valid data received to a given sub-address. This serves to ensure the highest possible degree of data consistency by allocating **two** 32-bit Data Word blocks for each individual receive (and/or broadcast) sub-address.

At a given point in time, one of the two blocks will be designated as the "active" 1553 data block while the other will be designated as the "inactive" block. The Data Words from the next receive message to that sub-address will be stored in the "active" block. Upon completion of a valid message, if Sub-address Double Buffering is enabled, the BU-65552 will automatically switch the "active" and "inactive" blocks for the respective sub-address. The ACE accomplishes this by toggling bit 5 of the sub-addresses' Lookup Table Pointer and rewriting the pointer. As a result, the most recent valid block of received Data Words will always be readily accessible to the host processor. As a means of ensuring data consistency, the host processor is able to reliably access the most recent valid, received Data Word block by performing the following sequence:

1) Disable the double buffering for the respective sub-address by accessing the Sub-address Control Word. That is, temporarily switch the sub-addresses memory management scheme to the Single Message mode.

2) Read the current value of the receive (or broadcast) sub-address Lookup Table pointer. This points to the current "active" Data Word block. By inverting bit 5 of this pointer value, it is possible to locate the start of the "inactive" Data Word block. This block will contain the Data Words received during the most recent valid message to the sub-address.

3) Read out the words from the "inactive" (most recent) Data Word Block.

4) Re-enable the Double Buffering mode for the respective sub-address by accessing the Sub-address Control Word.

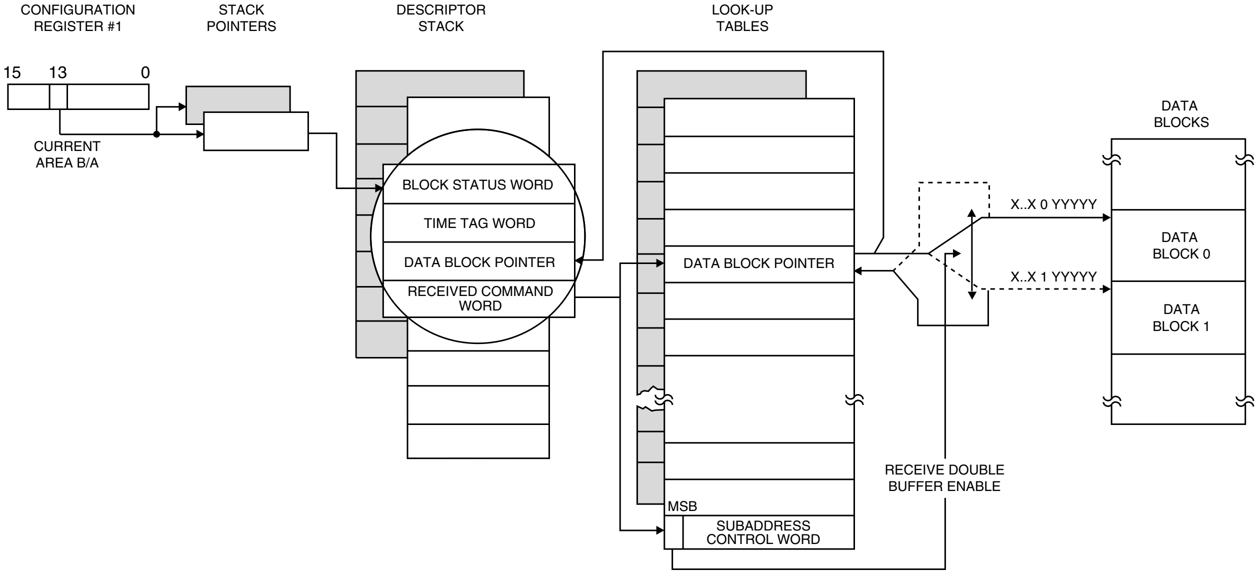


Figure 39. RT Memory Management: Sub-Address Double Buffering Mode

RT INTERRUPTS

As in BC mode, the BU-65552 RT provides many maskable interrupts. RT interrupt conditions include End of (every) Message, Message Error, Selected Sub-address (Sub-address Control Word) Interrupt, Circular Buffer Rollover, Selected Mode Code Interrupt, and Stack Rollover.

DESCRIPTOR STACK

At the beginning and end of each message, the BU-65552 RT stores a four-word message descriptor in the active area stack. The RT descriptor stack size is programmable, with choices of 256, 512, 1024, and 2048 words. The three preceding figures show the four words: Block Status Word, Time Tag Word, Data Block Pointer, and the 1553 received Command Word. The RT Block Status Word includes indications of message in-progress or message complete, bus channel, RT-to-RT transfer and RT-to-RT transfer errors, message format error, loop test (self-test) failure, circular buffer rollover, illegal command, and other error conditions.

Table 32 shows the bit mapping of the RT Block Status Word.

As in BC mode, the Time Tag Word stores the current contents of the BU-65552's read/write Time Tag Register. The resolution of the Time Tag Register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. Incrementing of the Time Tag counter may be from an internal or external clock source, or via software command.

The ACE stores the contents of the accessed Lookup Table location for the current message, indicating the starting location of the Data Word block, as the Data Block Pointer. This serves as a convenience in locating stored message data blocks. The ACE stores the full 16-bit 1553 Command Word in the fourth location of the RT message descriptor.

RT COMMAND ILLEGALIZATION

The PC Card provides an internal mechanism for RT command illegalization. The illegalization scheme uses a 256-word area in the PC Card address space. A benefit of this feature is the reduction of printed circuit board requirements, by eliminating the need for an external PROM, PLD, or RAM device that does the illegalizing function. The PC Card’s illegalization scheme provides maximum flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/R* bit, sub-address, and word count/mode code to be illegalized.

Another advantage of the RAM-based illegalization technique is that it provides for a high degree of self-test ability.

ADDRESSING THE ILLEGALIZATION TABLE

Table 42 illustrates the addressing scheme of the illegalization RAM. As shown in Table 39, the base address of the illegalizing RAM is word address 0300 (hex) in the shared RAM. The ACE formulates the index into the Illegalizing Table based on the values of BROADCAST/OWN ADDRESS, T/R* bit, Sub-address, and the MSB of the Word Count/Mode Code field (WC/MC4) of the current Command Word.

Broadcast_own = 128 if not a broad cast message, 0 if message is broadcast

T/R* = 64 if message is transmit, 0 if message is receive

SA = the sub-address of the message * 2

WC4 = bit 5 of the command word

Table location = 0x0300 + Broadcast_own + T/R* + SA +WC4

The internal RAM has 256 words reserved for command illegalization. Broadcast commands may be illegalized separately from non-broadcast receive commands and mode commands.

Commands may be illegalized down to the word count level. For example, a one-word receive command to sub-address 1 may be legal, while a two-word receive command to sub-address 1 may be made illegal.

The first 64 words of the Illegalization Table refer to broadcast receive commands (two words per sub-address). The next 64 words refer to broadcast transmit commands. Since non-mode code broadcast transmit commands are by definition invalid, this section of the table (except for sub-addresses 0 and 31) does **not** need to be initialized by the user. The next 64 words correspond to non-broadcast receive commands. The final 64 words refer to non-broadcast transmit commands. Messages with Word Count/ Mode Code (WC/MC) fields between 0 and 15 may be illegalized by setting the corresponding data bits for the respective even-numbered address locations in the illegalization table. Likewise, messages with WC/MC fields between 16 and 31 may be illegalized by setting the corresponding data bits for the respective odd-numbered address locations in the illegalization table.

The following should be noted with regards to command illegalization:

1) To illegalize a particular word count for a given broadcast/own address-T/R* sub-address, the appropriate bit position in the respective illegalization word should be set to logic 1. A bit value of logic 0 designates the respective Command Word as a legal command. The BUS-65552 will respond to an illegalized non-broadcast command with the Message Error bit set in its RT Status Word.

2) For sub-addresses 00001 through 11110, the ”WC/MC” field specifies the Word Count field of the respective Command Word. For sub-addresses 00000 and 11111, the ”WC/MC” field specifies the Mode Code field of the respective Command Word.

Since non-mode code broadcast transmit messages are not defined by MIL-STD-1553B, the 60 words in the illegalization RAM, addresses 0342 through 037D, corresponding to these commands do not need to be initialized. The PC Card will **not** respond to a non-mode code broadcast transmit command, but will automatically set the Message Error bit in its internal Status Register, regardless of whether or not corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, the PC Card will respond with its Message Error bit set.

Table 42. Illegalizing RAM Address Definition

BIT	DESCRIPTION
15(MSB)	0
14	0
13	0
12	0
11	0
10	0
9	1
8	1
7	BROADCAST*/ OWN ADDRESS
6	T/R*
5	SA4
4	SA3
3	SA2
2	SA1
1	SA0
0(LSB)	WC4/MC4

PROGRAMMABLE BUSY

As a means of providing compliance with Notice 2 of MIL-STD-1553B, the PC Card RT provides a software controllable means for setting the Busy Status Word bit as a function of sub-address. By means of a Busy Lookup Table in the PC Card address space, it is possible to set the Busy bit based on command broadcast/own address, T/R* bit, and sub-address. Another programmable option, allows received Data Words to be either stored or not stored for messages, when the Busy bit is set.

OTHER RT FUNCTIONS

The PC Card allows the RT Address to be programmed by the host processor. This enables the cards' RT address to be dynamically changed without having to set jumpers or switches. Also, there are options for the RT FLAG Status Word bit to be set under software control or automatically following a failure of the loop back self-test.

Other software controllable RT options include:

- Software programmable RT Status and RT BIT words
- Automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command
- Capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands
- Options regarding Data Word transfers for the Busy and/or Message Error (Illegal) Status Word bits and for handling of 1553A and reserved mode codes.

Monitor (MT) Architecture

The PC Card provides three bus monitor (MT) modes:

1) Word Monitor mode.

2) Selective Message Monitor mode.

3) Simultaneous Remote Terminal / Selective Message Monitor mode.

The strong recommendation for new applications is the use of the Selective Message Monitor, rather than the Word Monitor. Besides providing monitor filtering based on RT Address, T/R* bit, and Sub-address, the Message Monitor eliminates the need to determine the start and end of messages by software. The development of such software tends to be a tedious task. Moreover, at run time, it tends to entail a high degree of CPU overhead.

WORD MONITOR

In the Word Monitor mode, the PC Card monitors both 1553 buses. After initializing the Word Monitor and putting it on-line the BU-65552 stores all Command, Status, and Data Words received from both buses. For each word received from either bus, the PC Card stores a pair of words in RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or "Tag" word. The ID Word contains information relating to bus channel, sync type, word validity, and inter-word time gaps. The PC Card stores data and ID words in a circular buffer in the shared RAM address space.

WORD MONITOR MEMORY MAP

A typical word monitor memory map is illustrated in Table 43. The example assumes a 64K address space for the Enhanced Mini-ACE's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

The current Monitor address is maintained by means of a counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 or 0104, the initial pointer value stored in this shared RAM location will be overwritten by the monitored data and ID Words. When the internal counter reaches an address of FFFF (or 0FFF, for an Enhanced Mini-ACE with 4K RAM), the counter rolls over to 0000.

Table 43. Typical Word Monitor Memory Map

ADDRESS (HEX)	DESCRIPTION
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification Word
0004	Third Received 1553 Word
0005	Third Identification Word
• • •	• • •
0100	Stack Pointer (Fixed Location – gets overwritten)
• • • FFFF	• • Received 1553 Words and Identification Word •

MONITOR TRIGGER WORD

There is a Trigger Word Register that provides additional flexibility for the Word Monitor mode. The PC Card stores the value of the 16-bit Trigger Word in the MT Trigger Word Register. The contents of this register represent the value of the Trigger Command Word. The PC Card has programmable options to start or stop the Word Monitor, and/or to issue an interrupt request following receipt of the Trigger Command Word from the 1553 bus.

SELECTIVE MESSAGE MONITOR MODE

The PC Card Selective Message Monitor provides features to greatly reduce the software and processing burden of the host CPU. The Selective Message Monitor implements selective monitoring of messages from a dual 1553 bus, with the monitor filtering based on the RT Address, T/R* bit, and Sub-address fields of received 1553 Command Words. The Selective Message Monitor mode greatly simplifies the host processor software by distinguishing between Command and Status Words. The Selective Message Monitor maintains two stacks in the PC Card RAM: a Command Stack and a Data Stack.

SIMULTANEOUS RT/ MESSAGE MONITOR MODE

The Selective Message Monitor may function as a purely passive monitor or may be programmed to function as a simultaneous RT/Monitor. The RT/Monitor mode provides complete Remote Terminal (RT) operation for the PC Card’s strapped RT address and bus monitor capability for the other 30 nonbroadcast RT addresses. This allows the PC Card to simultaneously operate as a full function RT and "snoop" on all or a subset of the bus activity involving the other RTs on a bus. This type of operation is sometimes needed to implement a backup bus controller. The combined RT/Selective Monitor maintains three stack areas in the PC Card address space: a RT Command Stack, a Monitor Command Stack, and a Monitor Data Stack. The pointers for the various stacks have fixed locations in the PC Card address space.

SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

Table 44 illustrates a typical memory map for the ACE in the Selective Message Monitor mode. This mode of operation defines several fixed locations in the RAM. These locations allocate in a manner that is compatible with the combined RT/Selective Message Monitor mode. The fixed memory map consists of two Monitor Command Stack Pointers (location 102h and 106h), two Monitor Data Stack Pointers (locations 103h and 107h), and a Selective Message Monitor Lookup Table (0280-02FFh) based on RT Address, T/R*, and sub-address. Assume a Monitor Command Stack size of 1K words, and a Monitor Data Stack size of 2K words.

Refer to Figure 40 for an illustration of the Selective Message Monitor operation. Upon receipt of a valid Command Word, the PC Card will reference the Selective Monitor Lookup Table (a fixed block of addresses) to check for the condition (disabled/enabled) of the current command. If disabled, the PC Card will ignore (and not store) the current message; if enabled, the PC Card will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

Similar to RT mode, The ACE stores a Block Status Word, 16-bit Time Tag Word, and Data Block Pointer in the Message Descriptor, along with the received 1553 Command Word following reception of the Command Word. The ACE writes the Block Status and Time Tag Words at both the start and end of the message. The Monitor Block Status Word contains indications of message in-progress or message complete, bus channel, Monitor Data Stack Rollover, RT-to-RT transfer and RT-to-RT transfer errors, message format error, and other error conditions.

Table 35 shows the Message Monitor Block Status Word. The Data Block Pointer references the first word stored in the Monitor Data Stack (the first word following the Command Word) for the current message. The PC Card will then proceed to store the subsequent words from the message (possible second Command Word, Data Word(s), Status Word(s) into consecutive locations in the Monitor Data Stack.

The size of the Monitor Command Stack is programmable to 256, 1K, 4K, or 16K words. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K, or 64K words.

Monitor interrupts may be enabled for Monitor Command Stack Rollover, Monitor Data Stack Rollover, and/or End-of-Message conditions. In addition, in the Word Monitor mode there may be an interrupt enabled for a Monitor Trigger condition.

Table 44. Typical Selective Message Monitor Map (shown for 12K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack A (fixed location)
0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0BFF	Monitor Command Stack B
0C00-0FFF	Not Used
1000-1FFF	Monitor Data Stack A
2000-2FFF	Monitor Data Stack B

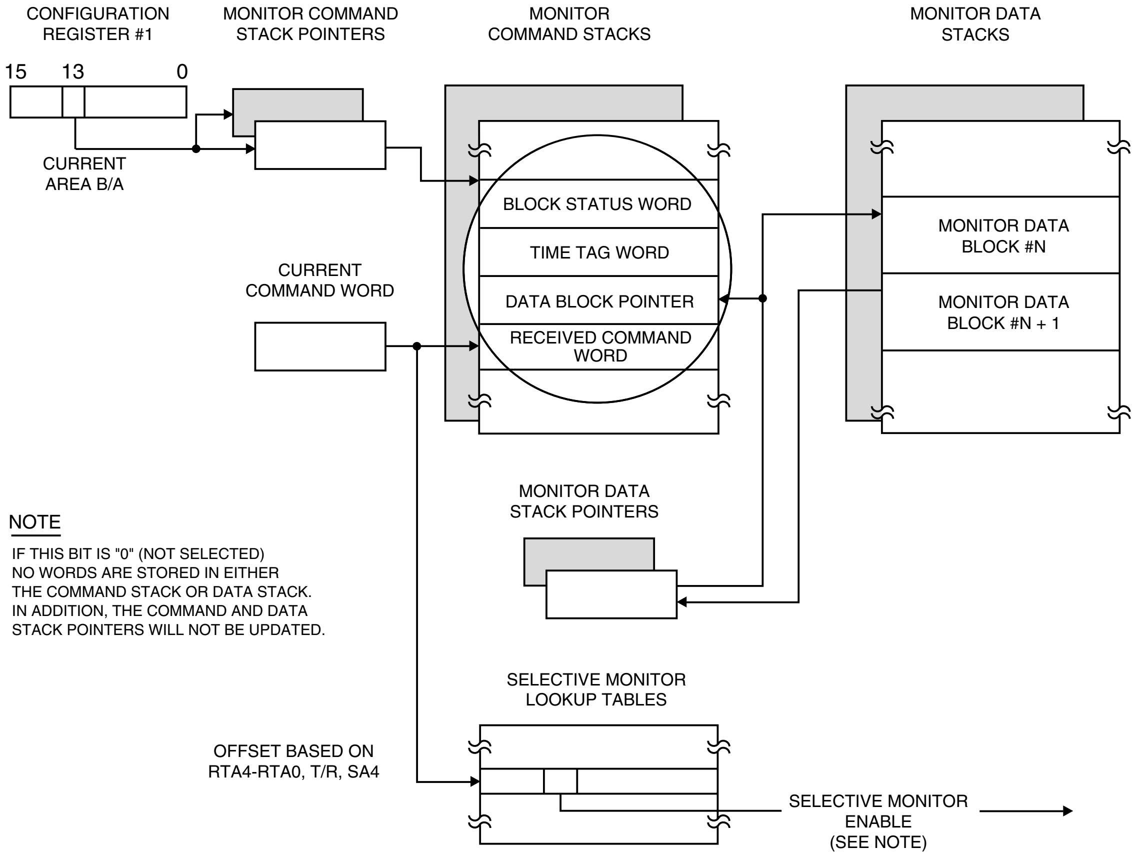

CONFIGURATION REGISTER #1
15
13
0
CURRENT AREA B/A
MONITOR COMMAND STACK POINTERS
MONITOR COMMAND STACKS
BLOCK STATUS WORD
TIME TAG WORD
DATA BLOCK POINTER
RECEIVED COMMAND WORD
MONITOR DATA STACKS
MONITOR DATA BLOCK #N
MONITOR DATA BLOCK #N + 1
CURRENT COMMAND WORD
MONITOR DATA STACK POINTERS
NOTE
IF THIS BIT IS "0" (NOT SELECTED) NO WORDS ARE STORED IN EITHER THE COMMAND STACK OR DATA STACK. IN ADDITION, THE COMMAND AND DATA STACK POINTERS WILL NOT BE UPDATED.
SELECTIVE MONITOR LOOKUP TABLES
OFFSET BASED ON RTA4-RTA0, T/R, SA4
SELECTIVE MONITOR ENABLE (SEE NOTE)

Figure 40. Selective Message Monitor Memory Management

HARDWARE SPECIFICATIONS

Table 45. BU-65553 Hardware Specifications

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
+5 V Supply Voltage	-0.3		7.0	V
RECEIVER				
Threshold Voltage, Transformer-Coupled, Measured on Stub	0.200		0.860	VP-P
TRANSMITTER				
Differential Output Voltage	18	20	27	VP-P
Transformer Coupled, Measured on Stub				
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
• + 5 V	4.5		5.5	V
Current Drain @ + 5.0 V				
• Idle			180	mA
• 25% Duty Cycle			296	mA
• 50% Duty Cycle			412	mA
• 100% Duty Cycle			645	mA
(see note 3)				
1553 MESSAGE TIMING				
RT Response Time	4		7	µsec
BC Intermessage Gap (See Note 1)		9.5		µsec
BC/RT/MT Response Timeout	17.5	18.5	19.5	µsec
(18.5 µsec nom., See Note 2)				
Transmitter Watchdog Timeout		668		µsec
THERMAL				
BU-65553				
Operating Temperature	0		+55	°C
Storage Temperature	-40		+85	°C
PHYSICAL CHARACTERISTICS				
Standard Type II PCMCIA	3.370 x 2.126 x 0.197			In
	(85.6 x 54.0 x 5.0)			(mm)
Weight	2.8			oz
	(80)			(gm)

NOTES:

(1) Typical value for minimum intermessage gap time. Under software control, may be lengthened (to 65,535 ms minus message time), in increments of 1 ms.

(2) Software programmable (4 options). Includes RT-to-RT Timeout (Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status).

(3) 100% Duty Cycle at MAX Transmit Amplitude [27 V PP].

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