English Language Test Description

Contract Number: N00244-09-C-0054

For

Unit Under Test

UUT Nomenclature: Power Supply CCA UUT Part Number: 6227570 UUT Reference Designator: DDM A3

From

Assault Amphibious Vehicle AN/PSM-115

ATE (Automated Test Equipment) SYSTEM

AN/USM-657B(V)2 Third Echelon Test System (TETS)
AN/USM-717(V)2 Virtual Instrument Portable Equipment Repair / Tester (VIPER/T)

Developed by

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Prepared By	Signature	Date Prepared	Date Submitted
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Approved By	Signature	Date Received	Date Approved

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ELTD REVISION SUMMARY

Revision Number	Date	Reason	Approved By – Date Approved
-	05/19/2010	ORIGINAL ISSUE	

1.	Intr	oduction	5
	1.1.	Scope	5
	1.2.	Purpose	5
	1.3.		
2.	Eng	lish Language Test Description (ELTD)	6
SA	FE T	O TURN ON TESTS	6
	Step 1	ITA Identification	6
	Step 2	UUT Identification (J1-Z to J2-22)	7
	Step 3	UUT Identification (J2-10/GND)	9
	Step 4	UUT Identification (J1-g to J2-4)	11
	Step 5	UUT Input Power Safe-to-Turn-On	13
UN	NPOW	TERED TESTS	15
	Step 6	T1-Center Tap to GND Resistance Test	15
	Step 7	+5V Output to GND Resistance Test	17
		+18V Output to GND Resistance Test	
	-	+12V Output to GND Resistance Test	
		O -3.6V Output to GND Resistance Test	
	Step 1	1 +250V Output to GND Resistance Test	25
	Step 12	2 R5 Resistance Test	27
		WER UP	
UU	J T PO	WER UP TESTS	29
		3 +28VDC Power On Test	
		E 1 REGULATED VOLTAGE TESTS	
		O1 +18V Regulated Output Test	
	Step 10	02 +5V Regulated Output Test	33
	-	03 +12V Regulated Output Test	
		04 +18V Regulated Output Test (at +24V in)	
		E 2 SWITCHING REGULATOR TESTS	
	Step 20	O1 +250V Regulated Output Test	39
		02 -3.6V Regulated Output Test	
	-	03 +250V Regulated Output Test (at +24V in)	
		04 Over-Current Regulation Test	
M	ODUL	E 3 ENGINE SPEED/WARNING CANCEL TESTS	47
	-	O1 Engine Speed Amplitude Test	
		O2 Engine Speed Voltage-Min Test	
		O3 Engine Speed Pulse-Width Test	
		04 Warning Cancel Test	
		E 4 CONTINUITY TESTS	
		O1 J1-W to J2-29 Continuity Test	
	-	O2 J1-V to J2-31 Continuity Test	
	-	O3 J1-U to J2-33 Continuity Test	
	-	04 J1-T to J2-35 Continuity Test	
	-	05 J1-G to J2-6 Continuity Test	
	-	06 J1-F to J2-5 Continuity Test	
	Step 40	07 J1-E to J2-19 Continuity Test	67

ELTD-05005104-VIPER/T ELTD-05005204-Retrofit	Rev -	05/19/2010
Step 408 J1-D to J2-21 Continuity	7 Test	69
Step 409 J1-C to J2-23 Continuity		
Step 410 J1-B to J2-24 Continuity		
Step 411 J1-A to J2-26 Continuity	Test	75
Step 412 J1-X to J2-27 Continuity	Test	77
Step 413 J1-j to J2-30 Continuity	Test	79
Step 414 J1-i to J2-34 Continuity	Test	81
Step 415 J1-a to J2-20 Continuity	Test	83
Step 416 J2-32 to GND Continuity		
FUNCTIONAL FLOW CHART (F	FFC)	87

1. Introduction

The Unit Under Test (UUT) for this English Language Test Description (ELTD) is the Power Supply Circuit Card Assembly (CCA), Part Number 6227570. The CCA is reference designator A3 in the Driver's Display Module Line Replaceable Unit (LRU) part number 5429249. The LRU resides in the Assault Amphibious Vehicle (AAV) Weapon System.

1.1. Scope

An ELTD is a detailed supplementary document consisting of textual test descriptions with graphical representation of signal interconnectivity and a functional flow chart.

1.2. Purpose

The purpose of this document is to provide English language test descriptions for the TP_AAV_DDM_A3 test program, to a level of detail used for maintenance purposes. The TP_AAV_DDM_A3 test program makes up part of the AN/PSM-115 Application Program Set (APS).

1.3. Content Arrangement

The document is laid out in the sequence the Test Program Set (TPS) would be executed when a 95 "Run All Mods" is entered in the main menu. A paragraph at the beginning of each module will describe the test description for that module. Each step will contain a description for that particular test followed by a graphical representation of the connections made from the receiver, through the Interface Test Adapter (ITA) and cables W8/W9 to the Power Supply CCA. A Functional Flow Chart resides at the end of the document.

2. English Language Test Description (ELTD)

WEAPON SYSTEM: Assault Amphibious Vehicle (AAV)

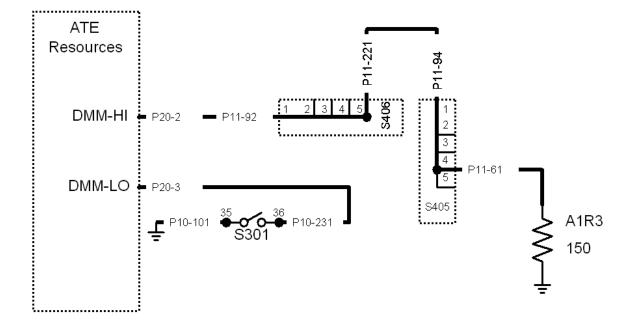
UNIT UNDER TEST: 6227570

TEST PROGRAM SET: TP_AAV_DDM_A3

SAFE TO TURN ON TESTS

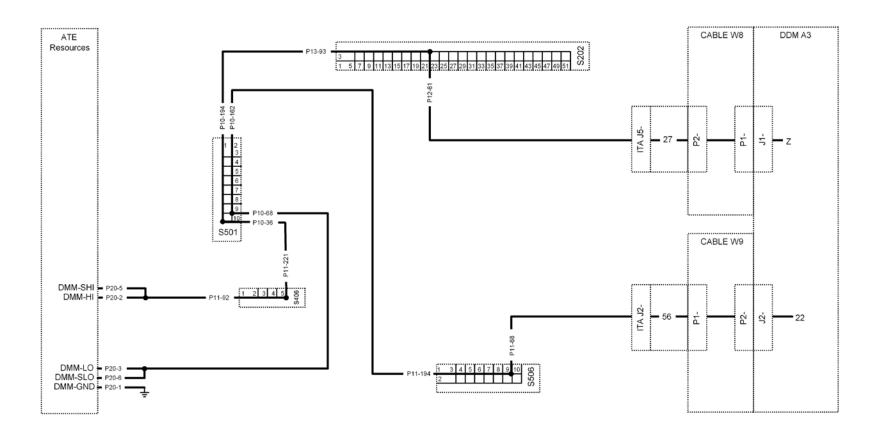
Step 1 ITA Identification

Test step 1 verifies the correct ITA is installed by using the DMM to measure the resistance of ITA A1R3. The resistance should be from 149 ohms to 155 ohms.



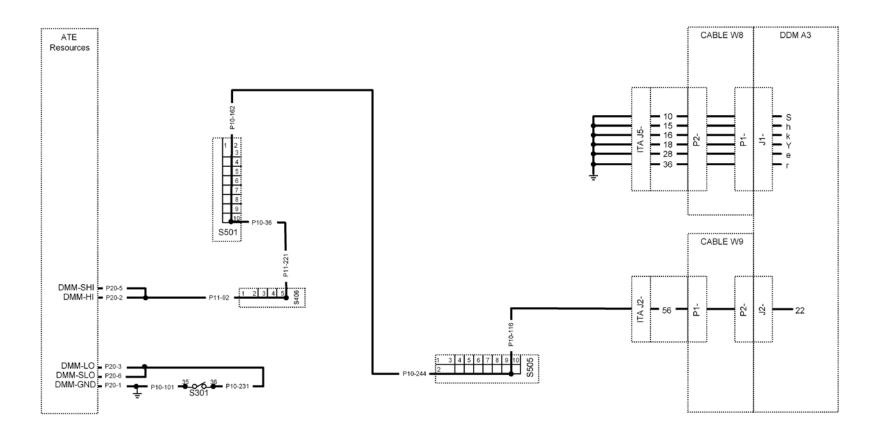
Step 2 UUT Identification (J1-Z to J2-22)

This step verifies continuity between UUT feed-through connectors J1-Z and J2-22 and is used in conjunction with STEPS 3 and 4 to determine that the UUT is a Power Supply CCA. The DMM is used to verify less than 10 ohms resistance across J1-Z and J2-22.



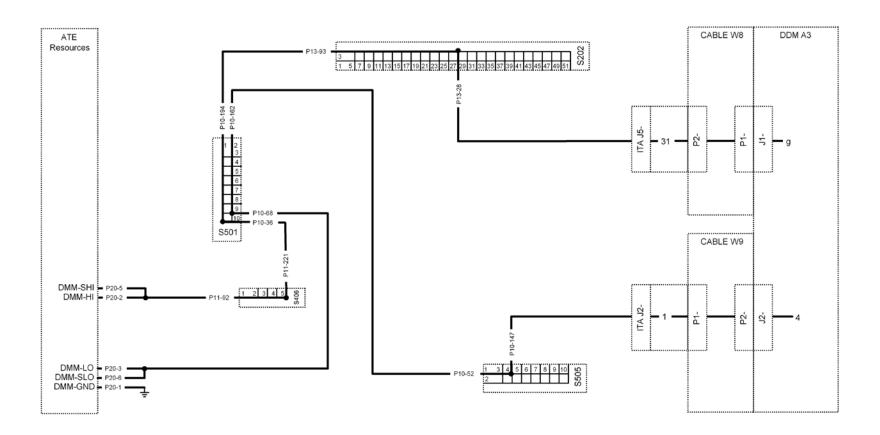
Step 3 UUT Identification (J2-10/GND)

This step verifies continuity of the UUT jumper between J2-10 and GND, and is used in conjunction with STEPS 2 and 4 to determine that the UUT is a Power Supply CCA. The DMM is used to verify less than 10 ohms resistance across J2-10 and UUT GND.



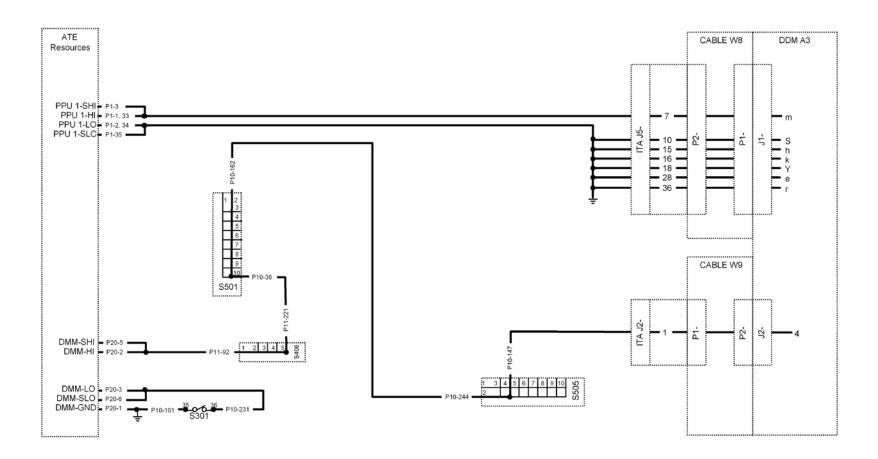
Step 4 UUT Identification (J1-g to J2-4)

This step is used in conjunction with STEPS 2 and 3 to determine that the UUT is a Power Supply CCA and then to determine which of the two Part Numbers supported (6227570 or 5429442) by the TPS it is. The DMM is used to verify greater than 1800 ohms resistance across J1-g and J2-4. A reading of nominally 2kohm (resistance of R3) identifies the UUT part number as 5429442. Otherwise, an open circuit identifies the UUT part number as 6227570. Part number 549442 is no longer required to be supported by this test program. However, it has been left unchanged for simplicity in the re-host effort and will still correctly identify the 6227570 UUT.



Step 5 UUT Input Power Safe-to-Turn-On

This step verifies the UUT +28V power input circuit is free of shorts that would constitute an Unsafe-to-Turn-On condition. DCPS (PPU) #1 is applied at J1-m/J1-r at a low voltage of 2 Vdc at 0.2 amps. The DMM is used to verify that the PPU did not sense an over-current condition by verifying greater than 1.9 Vdc at J2-4/GND.

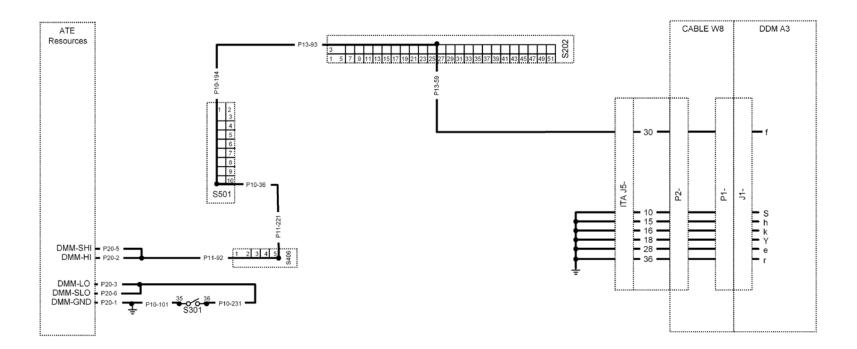


Rev -

UNPOWERED TESTS

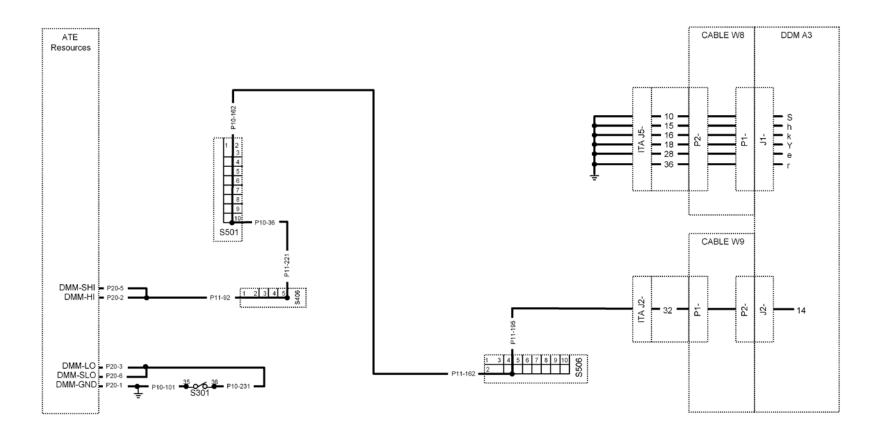
Step 6 T1-Center Tap to GND Resistance Test

This step verifies the isolation transformer T1 center-tap circuit resistance. The AN/USM-717 test program uses the DMM to verify 0.036 to 1.236 Mohms resistance across J1-f and GND. The AN/USM-657A/B test program uses the DMM to verify 0.9 to 1.1 Mohms resistance across J1-f and GND.



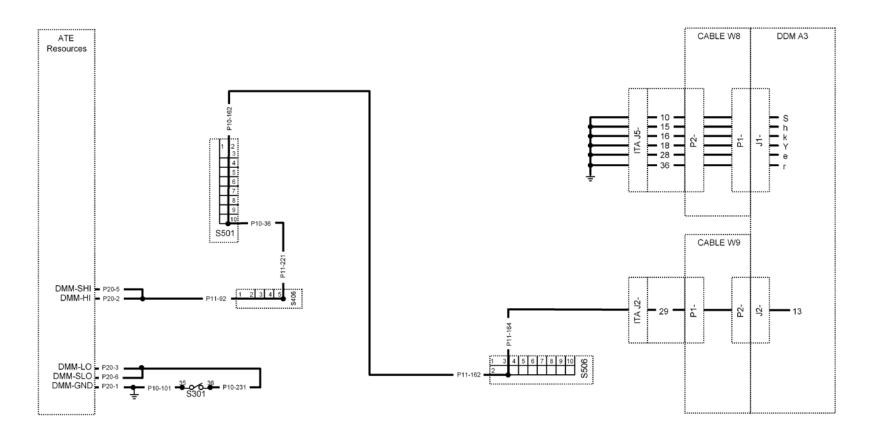
Step 7 +5V Output to GND Resistance Test

This step verifies the regulated +5V output circuit is free of shorts to ground. The DMM is used to verify greater than 1.0 Kohms resistance across J2-14 and GND.



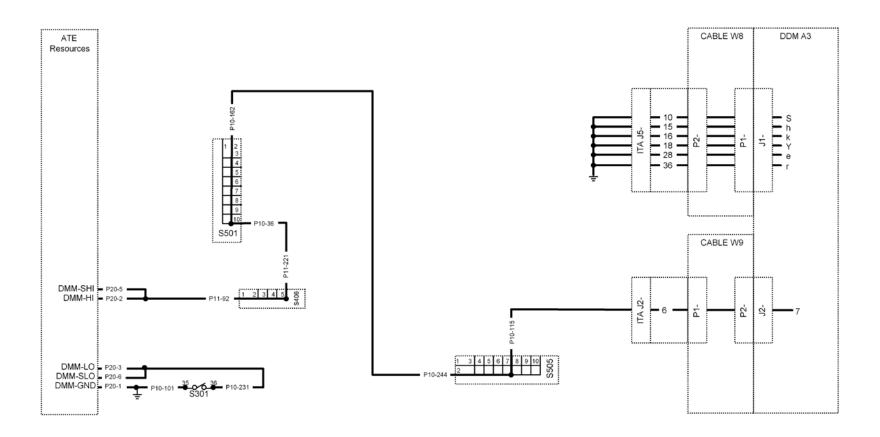
Step 8 +18V Output to GND Resistance Test

This step verifies the regulated +18V output circuit is free of shorts to ground. The DMM is used to verify greater than 1 Kohms resistance across J2-13 and GND.



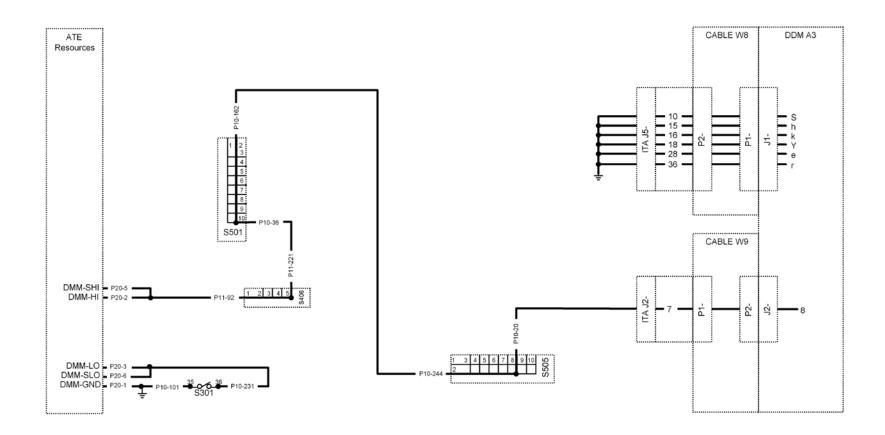
Step 9 +12V Output to GND Resistance Test

This step verifies the regulated +12V output circuit is free of shorts to ground as well as the 0.1% tolerance of resistors R20 and R21. The DMM is used to verify 12.0 Kohms +/-240 ohms resistance across J2-7 and GND.



Step 10 -3.6V Output to GND Resistance Test

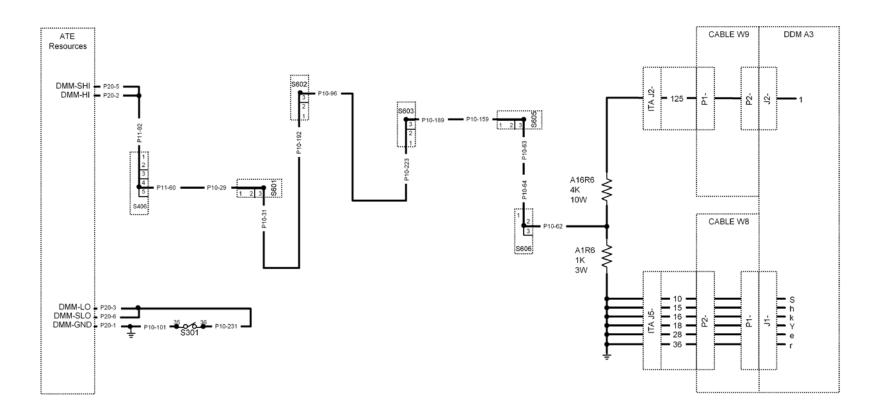
This step verifies the regulated -3.6V output circuit is free of shorts to ground. The DMM is used to verify greater than 10.0 Kohms resistance across J2-8 and GND.



Step 11 +250V Output to GND Resistance Test

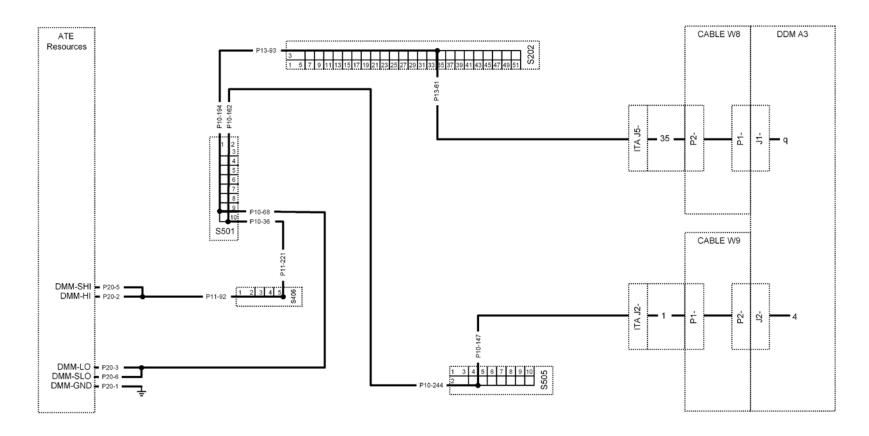
This step verifies the regulated +250V output circuit is free of shorts to ground. The DMM is used to verify greater than 900 ohms resistance across J2-1 and GND. A short on J2-1 will cause ITA resistor 1A16R6 (4 Kohms, 10 W) to be in parallel with 1A1R6 (1 Kohms, 3W), resulting in a reading of approximately 800 ohms.

Rev -



Step 12 R5 Resistance Test

This step verifies the 1% tolerance of resistor R5. The DMM is used to verify 2.0 ± 0.1 Kohms resistance across J2-4 and J1-q.



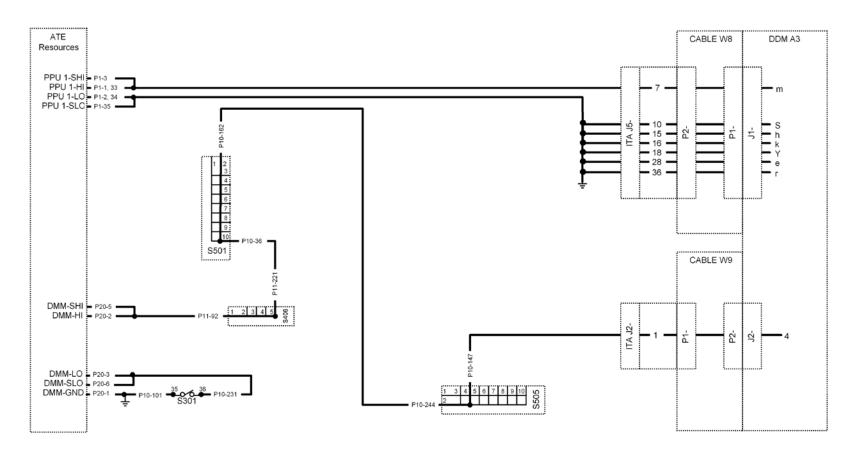
UUT POWER UP

+28 Vdc at 2.0A with a tolerance of ± 0.5 Vdc is required to power the UUT when output loads are connected. The power is removed prior to running test module 4.

UUT POWER UP TESTS

Step 13 +28VDC Power On Test

This step applies UUT +28V power and verifies the UUT +28V power input circuit is free of shorts that were not detected by the Safe-to-Turn-On Test. DCPS (PPU) #1 is applied at J1-m/J1-r at a current limit of 1.0 amp. Only the +250V output at J2-1 is loaded for this test. The DMM is used to verify that the PPU did not sense an over-current condition by verifying 28.0 +/-0.5VDC at J2-4/GND.



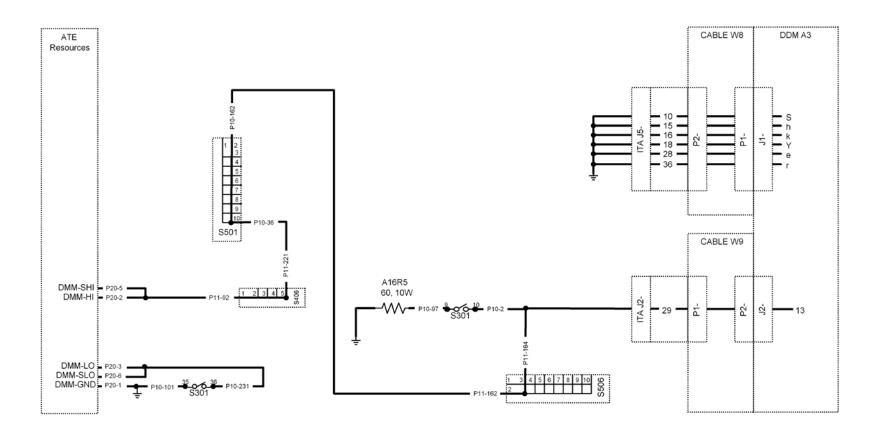
MODULE 1 REGULATED VOLTAGE TESTS

Module 1 verifies the following regulated outputs under the specified load conditions:

+18VDC: 60 ohm load +5VDC: 18 ohm load +12VDC: 120 ohm load

Step 101 +18V Regulated Output Test

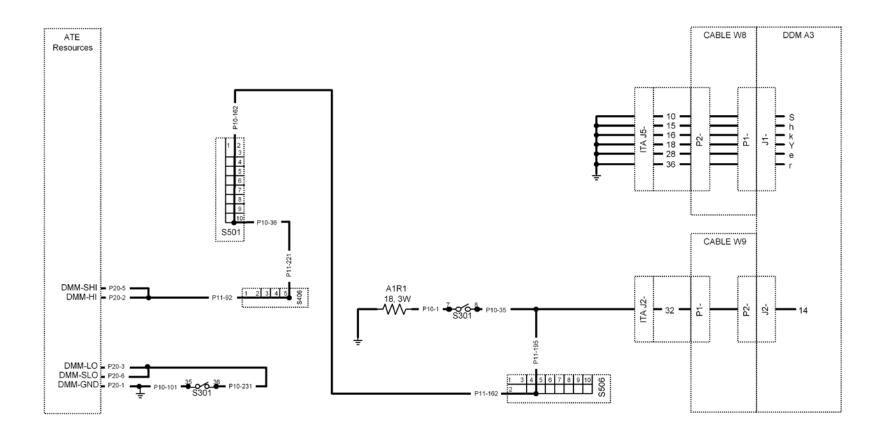
This step verifies the regulated +18V output under specified load conditions at J2-13/GND. UUT +28V power is applied using DCPS (PPU) #1 at J1-m/J1-r the specified current limit of 2 amps. With a 60.0 ohm ($\pm 5\%$) load connected at J2-13, the +18V regulated output is verified to be +18.0 ± 0.6 VDC using the DMM.



Rev -

Step 102 +5V Regulated Output Test

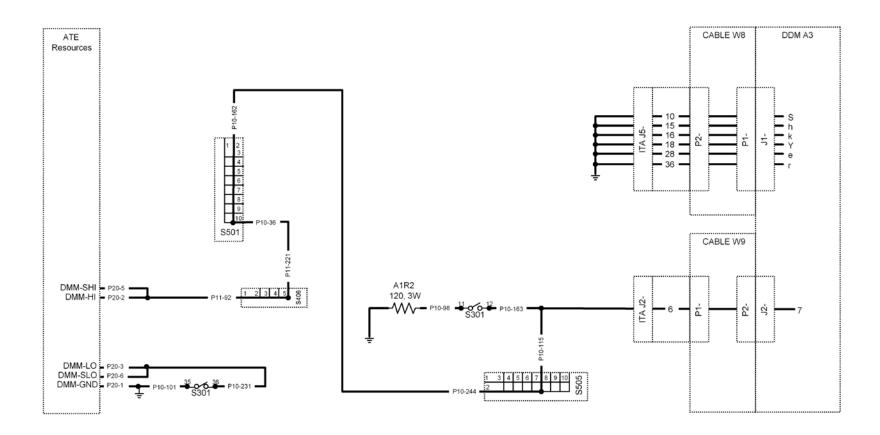
This step verifies the regulated +5V output under specified load conditions at J2-14/GND. With an 18.0 ohm ($\pm 1\%$) load connected at J2-14, the +5V regulated output is verified to be +5.0 ± 0.2 VDC using the DMM.



Rev -

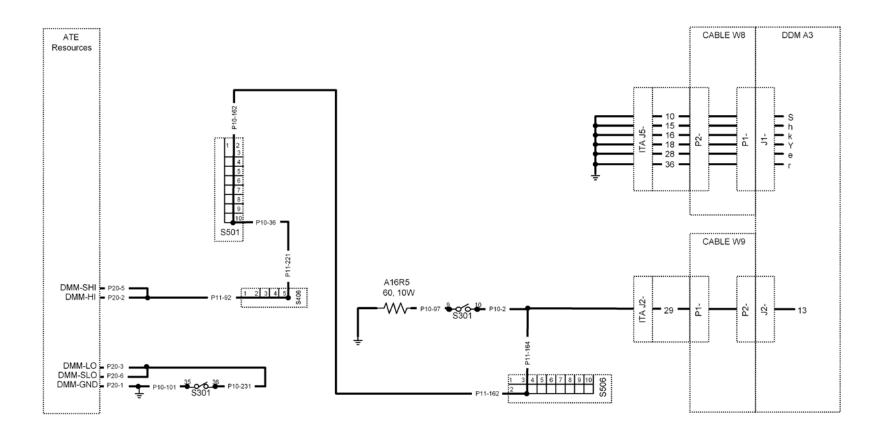
Step 103 +12V Regulated Output Test

This step verifies the regulated +12V output under specified load conditions at J2-7/GND. With a 120.0 ohm ($\pm 5\%$) load connected at J2-7, the +12V regulated output is then verified to be +12.0 ± 0.05 VDC using the DMM.



Step 104 +18V Regulated Output Test (at +24V in)

This step verifies the regulated +18V output under specified load conditions at J2-13/GND. UUT +28V power is applied using DCPS (PPU) #1 at J1-m/J1-r the specified current limit of 2 amps, but lowered to +24V. With a 60.0 ohm ($\pm 5\%$) load connected at J2-13, the +18V regulated output is verified to be +18.0 ± 0.6 VDC using the DMM.



MODULE 2 SWITCHING REGULATOR TESTS

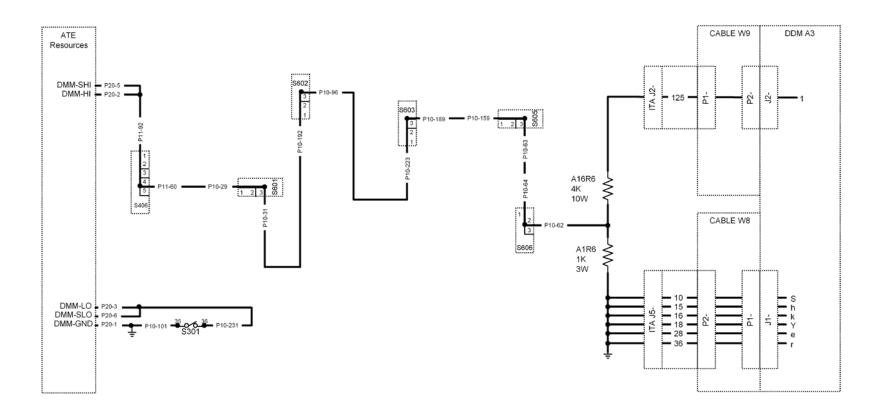
Module 2 verifies the following regulated outputs of the switching regulator circuit under the specified load conditions:

+250VDC: 5.0K ohm load

-3.6VDC: No load

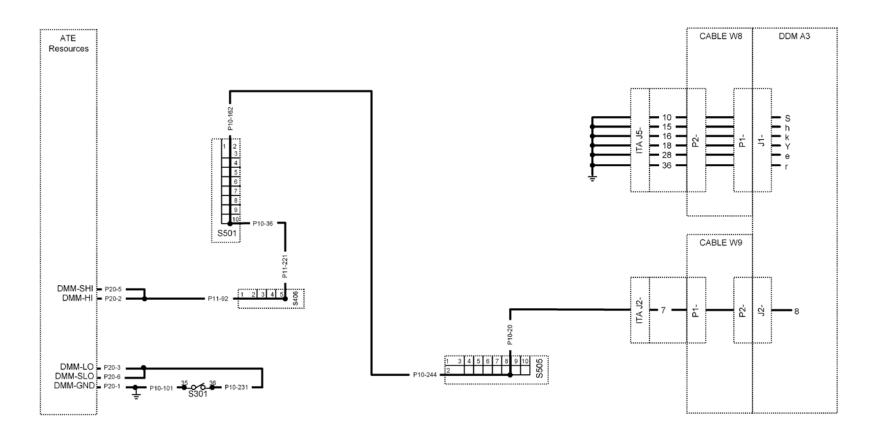
Step 201 +250V Regulated Output Test

This step verifies the regulated +250V output under specified load conditions at J2-1/GND. With a 5.0K ohm ($\pm 2\%$) load connected at J2-1, the +250V regulated output is then verified to be +250.0V $\pm 5\%$ using the DMM. Since 250V exceeds the maximum voltage rating of the tester LF Switching, the output is applied thru load resistor/voltage-divider (5:1) network made up of ITA resistors 1A16R6 and 1A1R6, which results in a nominal value of 50VDC (+/-2.5V).



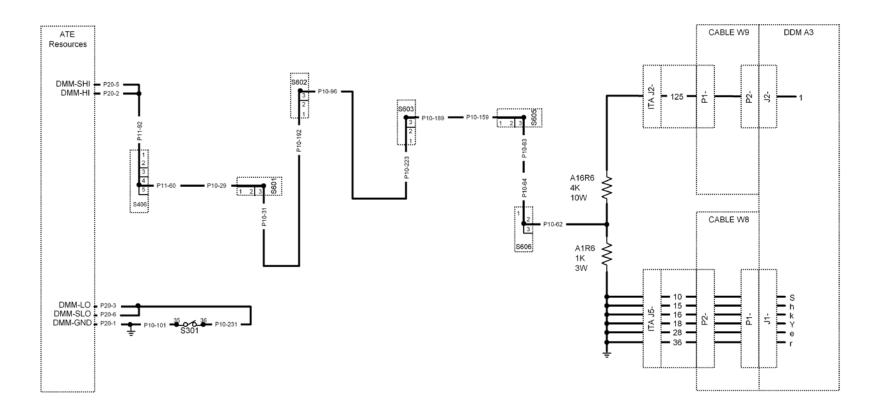
Step 202 -3.6V Regulated Output Test

This step verifies the regulated -3.6V output at J2-5/GND is within the specified tolerance of 10% using the DMM.



Step 203 +250V Regulated Output Test (at +24V in)

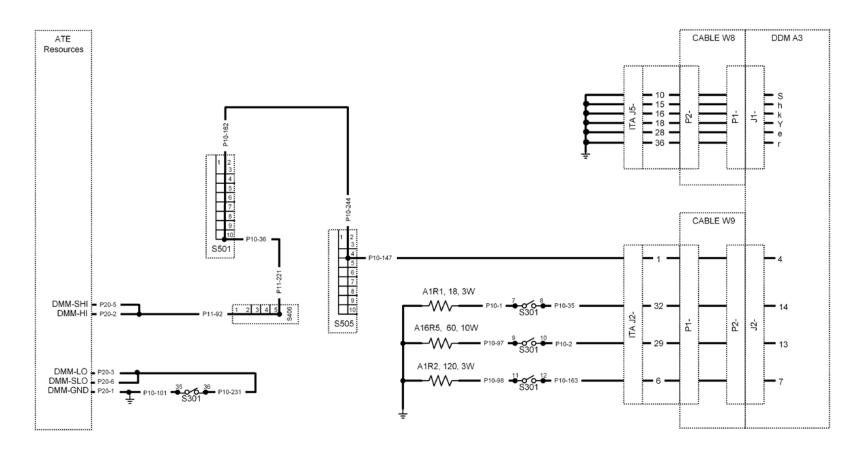
This step verifies the regulated +250V output under specified load conditions at J2-1/GND with the input power reduced from +28V to +24V. With a 5.0K ohm ($\pm2\%$) load connected at J2-1, the +250V regulated output is then verified to be $+250.0\text{V} \pm 5\%$ using the DMM. Since 250V exceeds the maximum voltage rating of the tester LF Switching, the output is applied thru load resistor/voltage-divider (5:1) network made up of ITA resistors 1A16R6 and 1A1R6, which results in a nominal value of 50VDC (+/-2.5V).



Rev -

Step 204 Over-Current Regulation Test

This step verifies the over-current regulation functionality of the switching regulator circuitry by reducing the input voltage to +16V while monitoring the DC supply current, ensuring it never exceeds 1.5 amps. This measurement will be accomplished by setting the PPU current limit to 1.5A and monitoring the input voltage. A failure will cause the PPU to fault, causing the voltage to go to 0V. All specified regulator output loads are connected during this test.

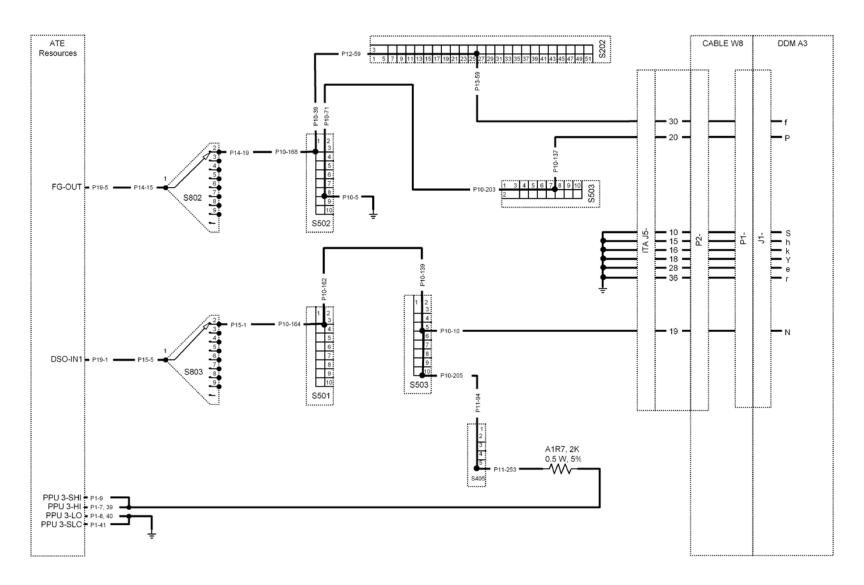


MODULE 3 ENGINE SPEED/WARNING CANCEL TESTS

Module 3 verifies the functionality of the Engine Speed and Warning Cancel line.

Step 301 Engine Speed Amplitude Test

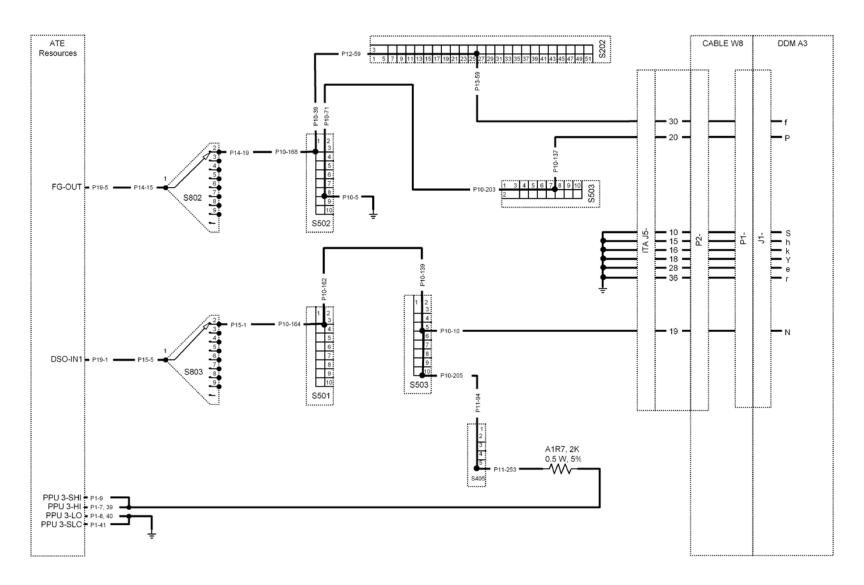
This step verifies the functionality of the Engine Speed circuit built around the zero-crossing detector U1. The Function Generator is used to apply a 20Hz sine wave at 2 Vpp (required to exceed U1 input threshold) across T1 primary input at J1-f/J1-P. Because of the 50-ohm input impedance of the Function Generator only 1 Vpp is programmed, but during execution this voltage is doubled before it is applied. With a +28V pull-up applied at the open-collector (Q1) output J1-N via a 2Kohm (+/-5%), the digitizing oscilloscope is used to verify greater than 27 Vpp pulse amplitude at J1-N.



Step 302 Engine Speed Voltage-Min Test

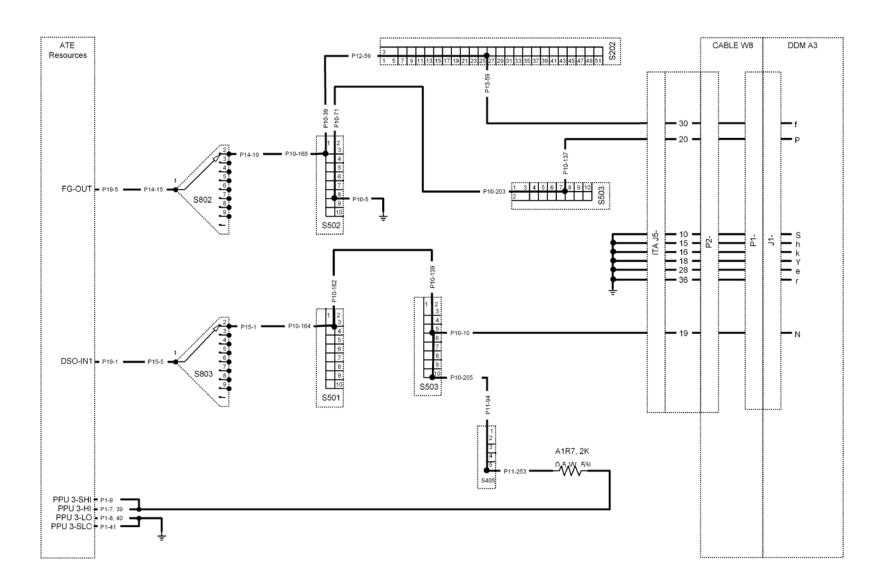
This step verifies the output pulse of the Engine Speed circuit at J1-N transitions to a low level. The Function Generator is used to apply a 20Hz sine wave at 2 Vpp (required to exceed U1 input threshold) across T1 primary input at J1-f/J1-P. Because of the 50-ohm input impedance of the Function Generator only 1 Vpp is programmed, but during execution this voltage is doubled before it is applied. With a +28V pull-up applied at the open-collector (Q1) output J1-N via a 2Kohm (+/-5%), the digitizing oscilloscope is used to verify a Voltage-Peak minimum of 1.0 V or less at J1-N.

Rev -



Step 303 Engine Speed Pulse-Width Test

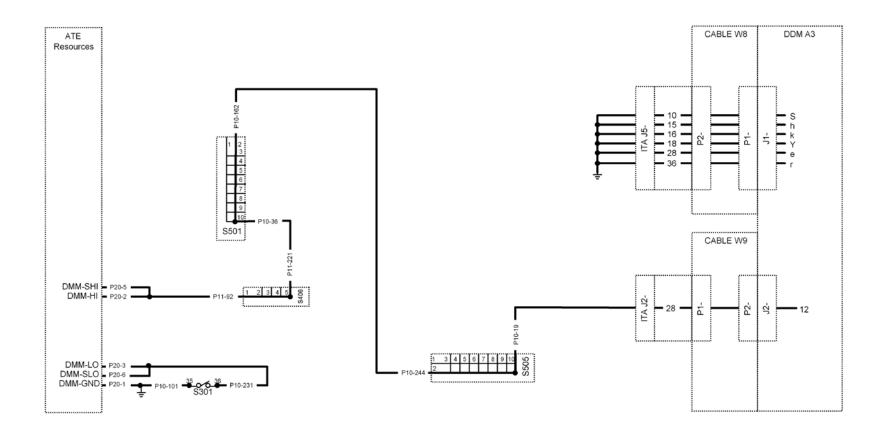
This step verifies the output pulse-width of the Engine Speed circuit at J1-N is 6.5mSec (R22/C22 RC time-constant) ±1.6mSec (the cumulative 25% tolerance of the values of R22 and C22). The Function Generator is used to apply a 20Hz sine wave at 2 Vpp (required to exceed U1 input threshold) across T1 primary input at J1-f/J1-P. Because of the 50-ohm input impedance of the Function Generator only 1 Vpp is programmed, but during execution this voltage is doubled before it is applied. With a +28V pull-up applied at the open-collector (Q1) output J1-N via a 2Kohm (+/-5%), the digitizing oscilloscope is used to verify a negative pulse-width of 4.9 mSec to 8.1 mSec at J1-N.



Rev -

Step 304 Warning Cancel Test

This step verifies the functionality of the Warning Cancel circuit not already tested (VR4, C4, and R7). With +28V power applied at J1-m and the Warning Cancel input at J1-q open, the voltage at J2-12 is verified to be nominally 19.8V (28V [in] - 8.2V [VR4 drop]), using the DMM. The reading should be between 15.85 and 23.75 Vdc.

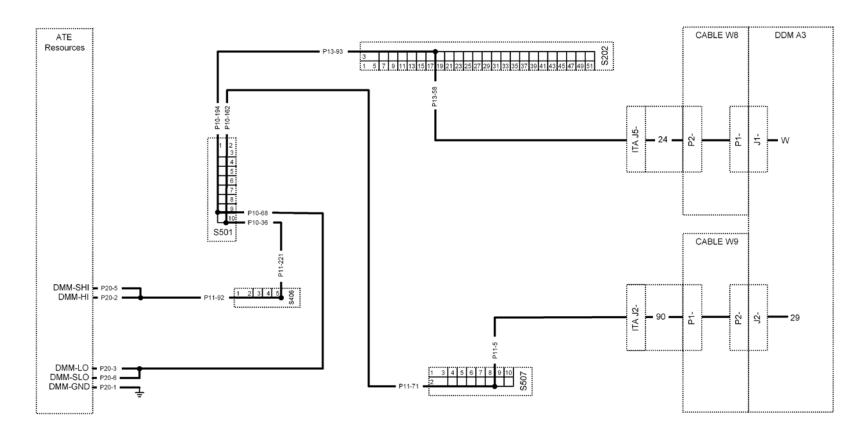


MODULE 4 CONTINUITY TESTS

Module 4 verifies continuity through the J1 to J2 feed-through lines.

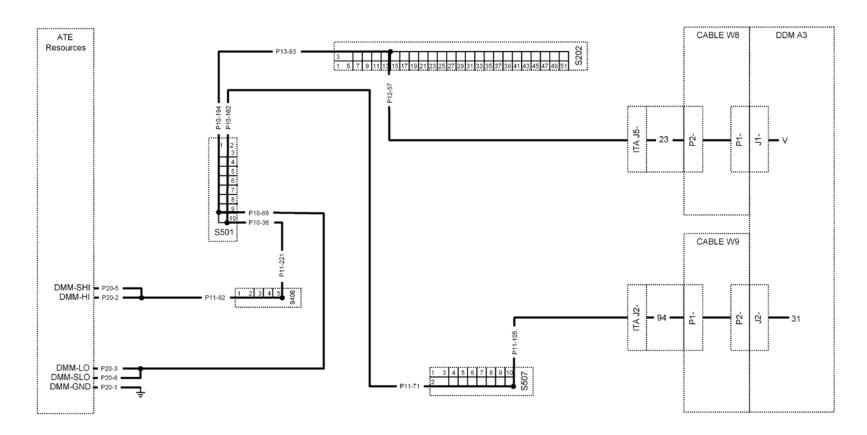
Step 401 J1-W to J2-29 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-W to J2-29 feed-through path.



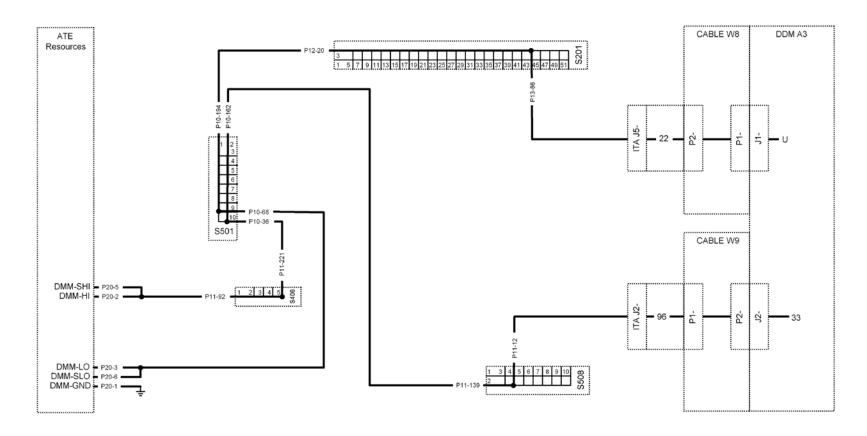
Step 402 J1-V to J2-31 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-V to J2-31 feed-through path.



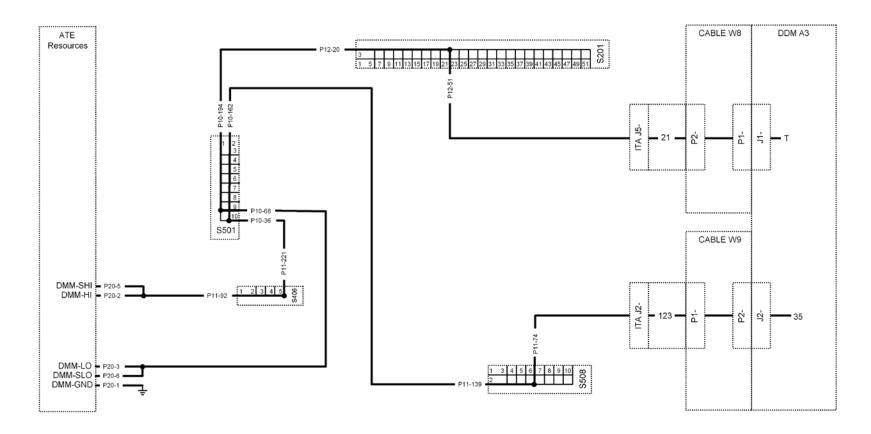
Step 403 J1-U to J2-33 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-U to J2-33 feed-through path.



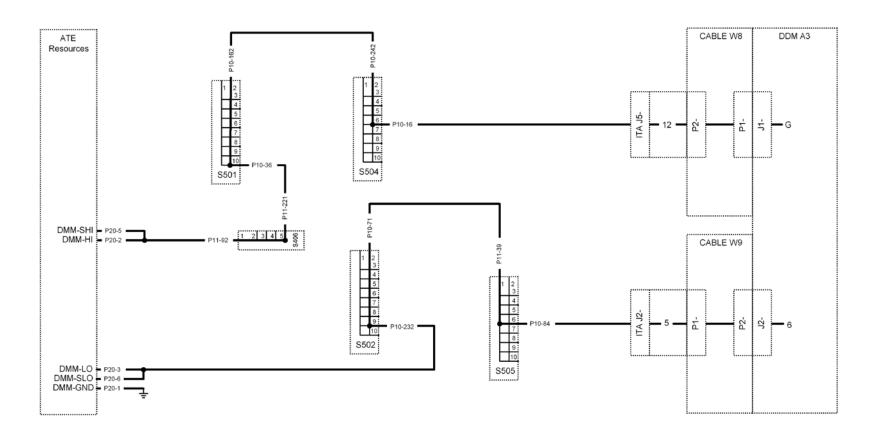
Step 404 J1-T to J2-35 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-T to J2-35 feed-through path.



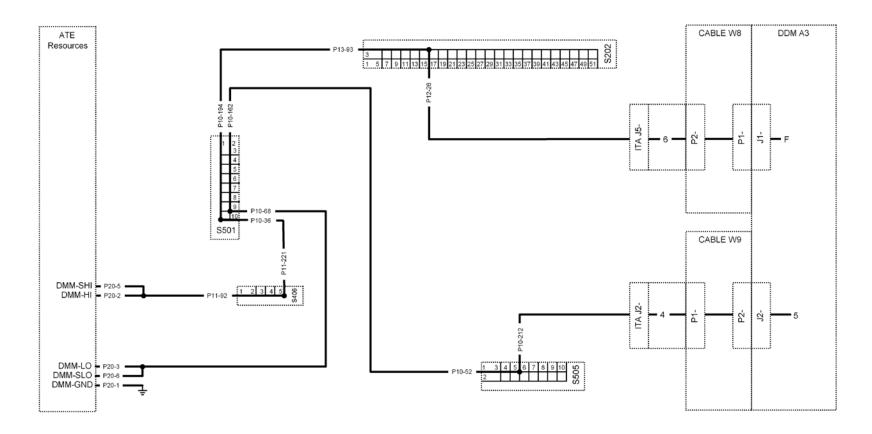
Step 405 J1-G to J2-6 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-G to J2-6 feed-through path.



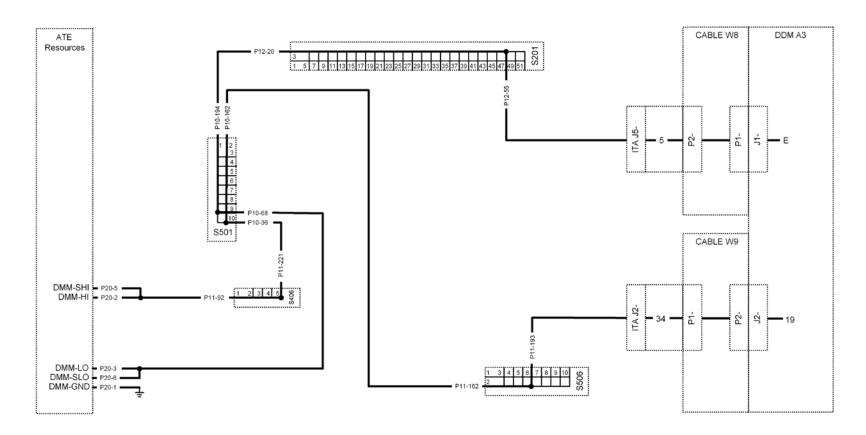
Step 406 J1-F to J2-5 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-F to J2-5 feed-through path.



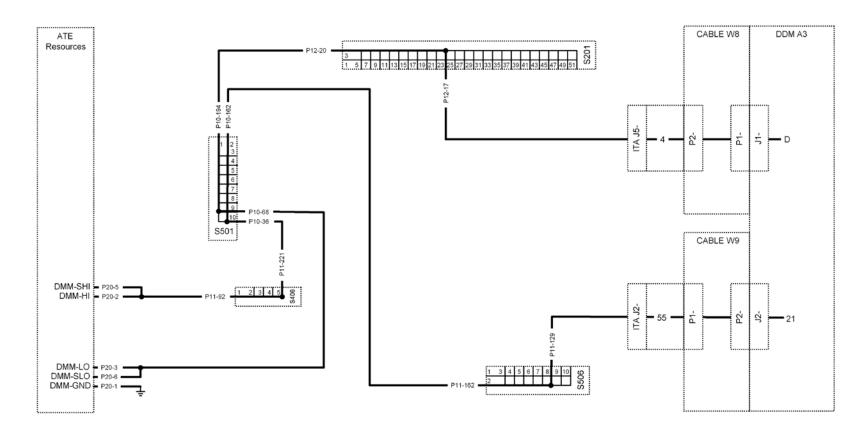
Step 407 J1-E to J2-19 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-E to J2-19 feed-through path.



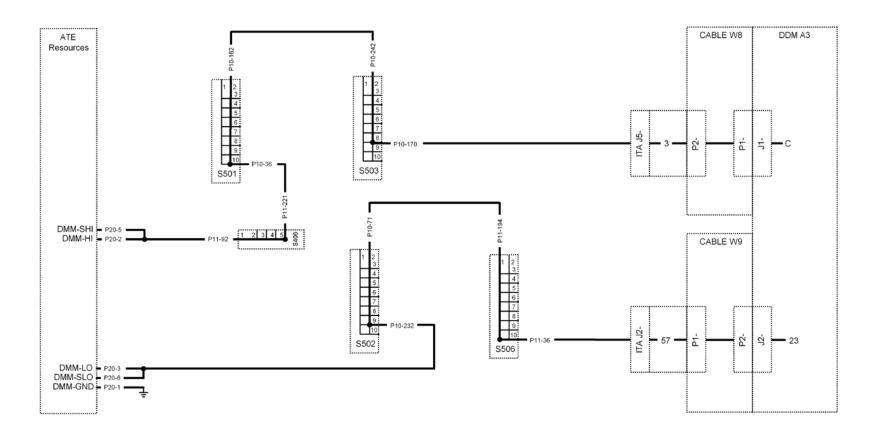
Step 408 J1-D to J2-21 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-D to J2-21 feed-through path.



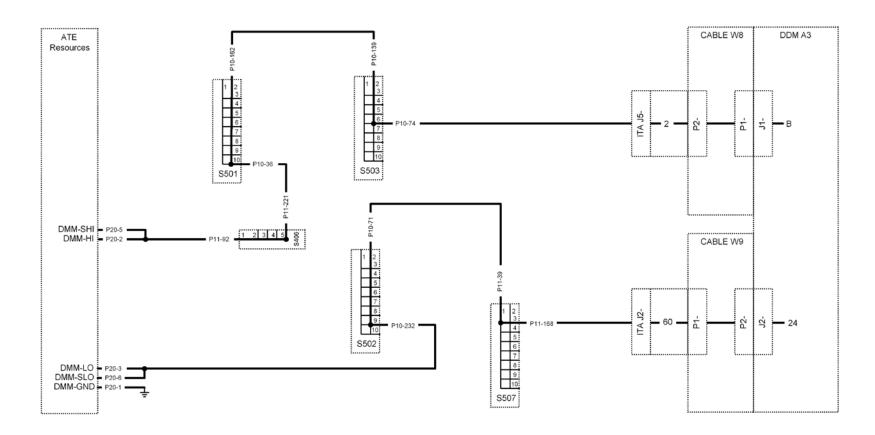
Step 409 J1-C to J2-23 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-C to J2-23 feed-through path.



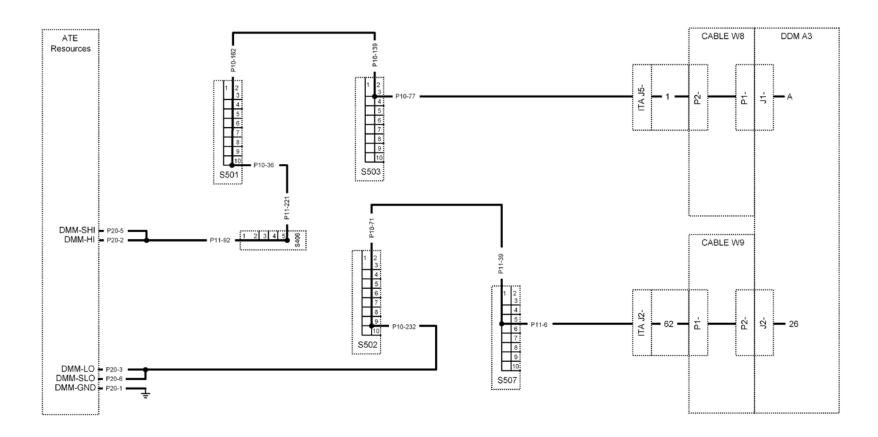
Step 410 J1-B to J2-24 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-B to J2-24 feed-through path.



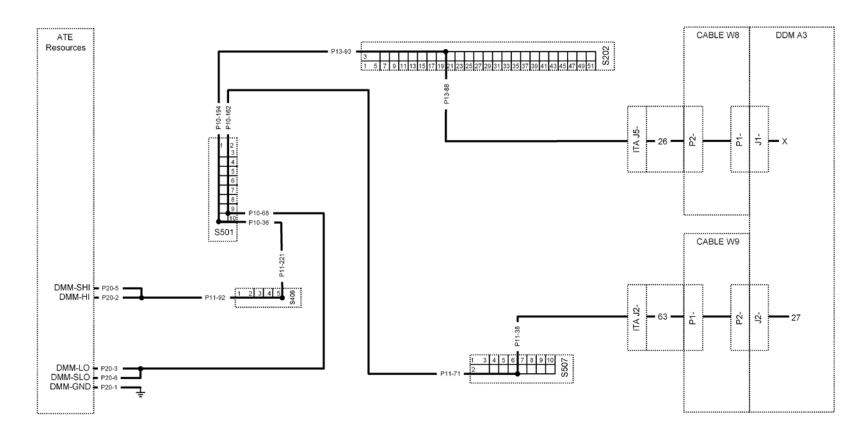
Step 411 J1-A to J2-26 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-A to J2-26 feed-through path.



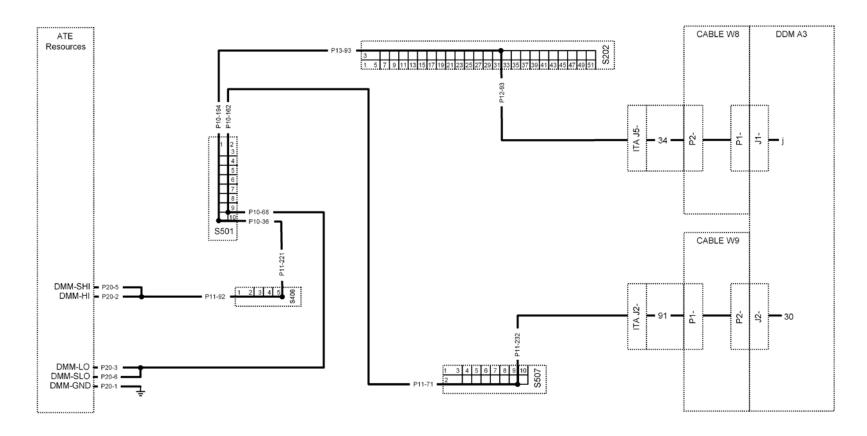
Step 412 J1-X to J2-27 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-X to J2-27 feed-through path.



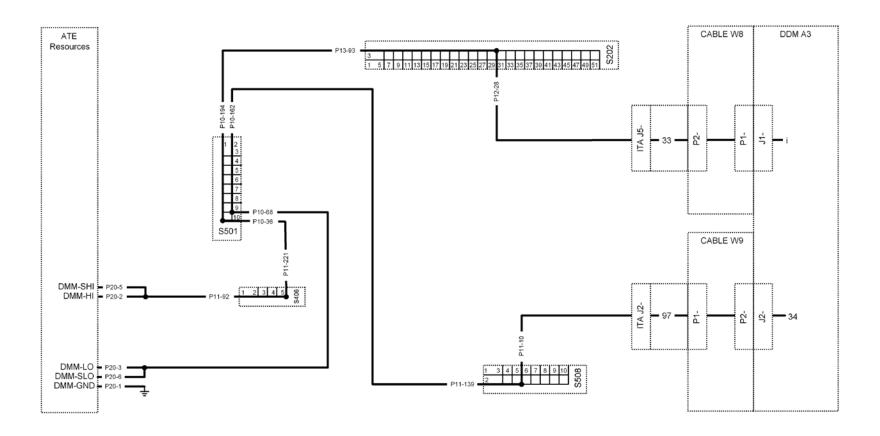
Step 413 J1-j to J2-30 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-j to J2-30 feed-through path.



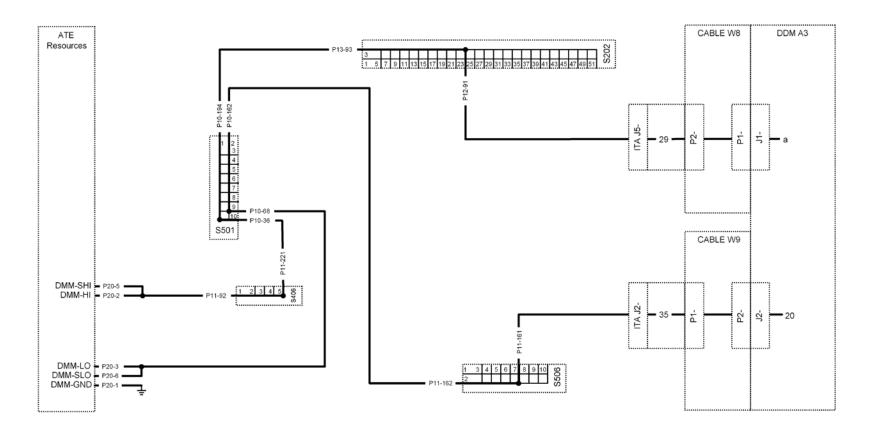
Step 414 J1-i to J2-34 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-i to J2-34 feed-through path.



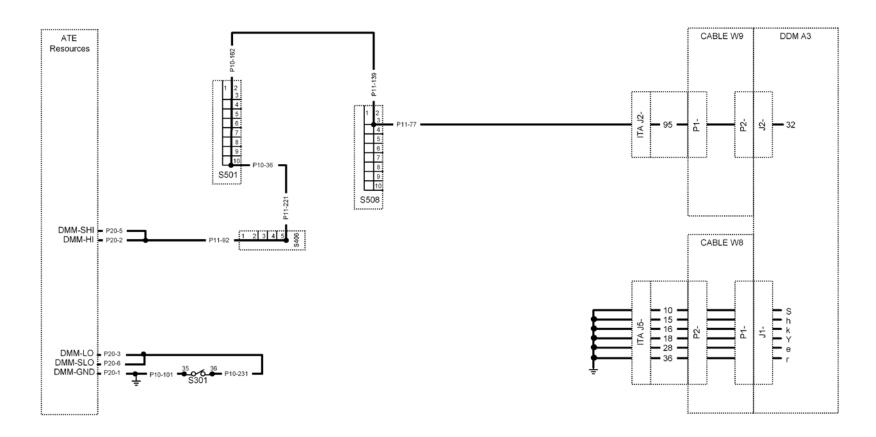
Step 415 J1-a to J2-20 Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J1-a to J2-20 feed-through path.

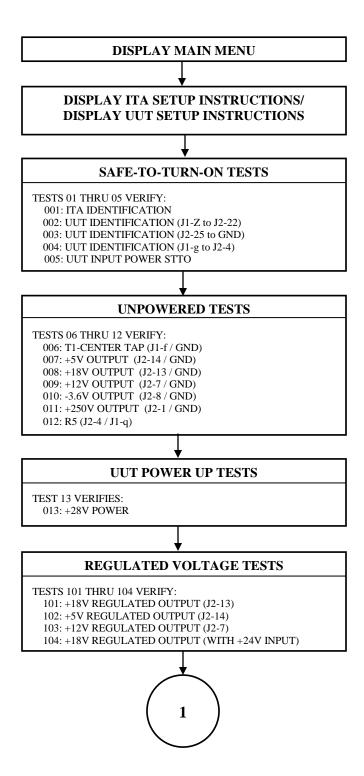


Step 416 J2-32 to GND Continuity Test

This step utilizes the DMM to verify the path resistance is less than 10 ohms (allowed for ITA/Test Cable path resistance) across the J2-32 to J1-k (GND) feed-through path.



FUNCTIONAL FLOW CHART (FFC)





SWITCHING REGULATOR TESTS

TESTS 201 THRU 204 VERIFY:

201: +250V OUTPUT (J2-1)

202: -3.6V OUTPUT (J2-8)

203: +250V OUTPUT (WITH +24V INPUT) 204: OVER-CURRENT REGULATION

ENGINE SPEED / WARNING CANCEL TESTS

TESTS 301 THRU 304 VERIFY:

301: ENGINE SPEED Amplitude

302: ENGINE SPEED Voltage-Min

303: ENGINE SPEED Pulse-Width

304: WARNING CANCEL

CONTINUITY TESTS

TESTS 401 THRU 416 VERIFY:

401: J1-W to J2-29

402: J1-V to J2-31

403: J1-U to J2-33 404: J1-T to J2-35

405: J1-G to J2-6

406: J1-F to J2-5 407: J1-E to J2-19

408: J1-D to J2-21

409: J1-C to J2-23

410: J1-B to J2-24

411: J1-A to J2-26

412: J1-X to J2-27

413: J1-j to J2-30

414: J1-i to J2-34

415: J1-a to J2-20

416: J2-32 to GND (VERIFIES J1-k to J2-32)

DISPLAY CLOSEOUT INSTRUCTIONS

DISPLAY MAIN MENU