English Language Test Description

Contract Number: N00244-09-C-0054

For

Unit Under Test

UUT Nomenclature: Power Amplifier CCA
UUT Part Number: 2618547-1
UUT Reference Designator: ICS A5

From

Assault Amphibious Vehicle
AN/PSM-115

ATE (Automated Test Equipment) SYSTEM

AN/USM-657B(V)2 Third Echelon Test System (TETS)
AN/USM-717(V)2 Virtual Instrument Portable Equipment Repair / Tester (VIPER/T)

Developed by

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Prepared By	Signature	Date Prepared	Date Submitted
Tom Biggs		05/25/2010	

Approved By	Signature	Date Received	Date Approved

ELTD REVISION SUMMARY

Revision Number	Date	Reason	Approved By – Date Approved
-	05/25/2010	ORIGINAL ISSUE	

1. Introduction

The Unit Under Test (UUT) for this English Language Test Description (ELTD) is the Power Amplifier Circuit Card Assembly (CCA), Part Number 2618547-1. The CCA is reference designator A5 in the Intercommunication Set (ICS) Line Replaceable Unit (LRU) part number AN/MIQ-1(V)3. The LRU resides in the Assault Amphibious Vehicle (AAV) Weapon System.

1.1. Scope

An ELTD is a detailed supplementary document consisting of textual test descriptions with graphical representation of signal interconnectivity and a functional flow chart.

1.2. Purpose

The purpose of this document is to provide English language test descriptions for the TP_AAV_ICS_A5 test program, to a level of detail used for maintenance purposes. The TP_AAV_ICS_A5 test program makes up part of the AN/PSM-115 Application Program Set (APS).

1.3. Content Arrangement

The document is laid out in the sequence the Test Program Set (TPS) would be executed when a 95 “Run All Mods” is entered in the main menu. A paragraph at the beginning of each module will describe the test description for that module. Each step will contain a description for that particular test followed by a graphical representation of the connections made from the receiver, through the Interface Test Adapter (ITA) and cable W7 to the Power Amplifier CCA. A Functional Flow Chart resides at the end of the document.

2. English Language Test Description (ELTD)

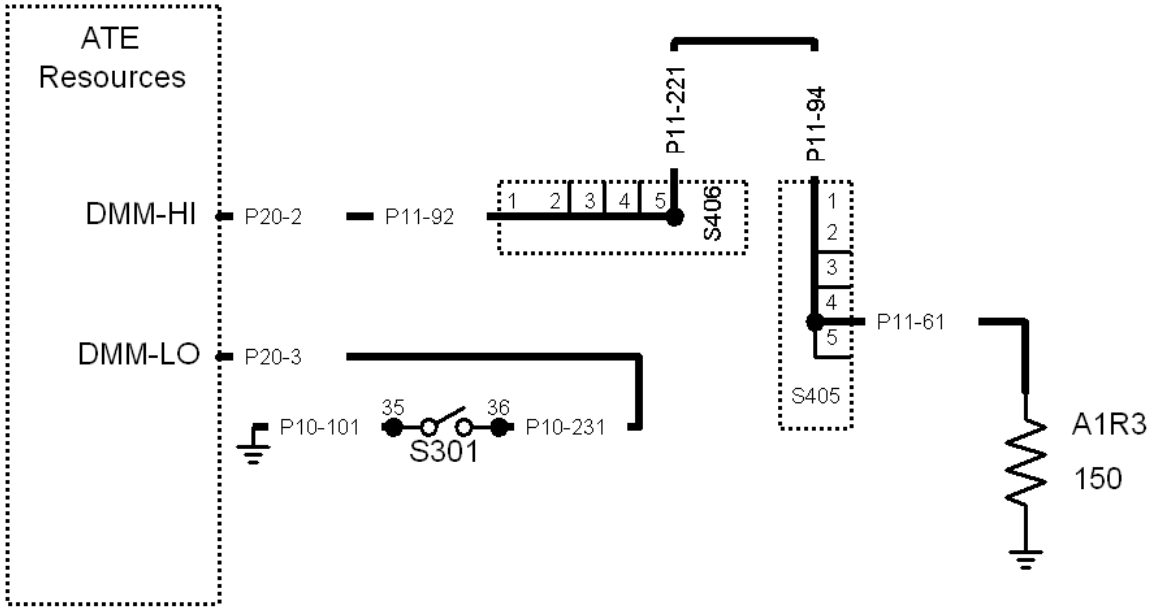
WEAPON SYSTEM: Assault Amphibious Vehicle (AAV)
UNIT UNDER TEST: 2618547-1
TEST PROGRAM SET: TP_AAV_ICS_A5

SAFE TO TURN ON TESTS

Step 1 ITA Identification

Test step 1 verifies the correct ITA is installed by using the DMM to measure the resistance of ITA A1R3. The resistance should be from 149 ohms to 155 ohms.

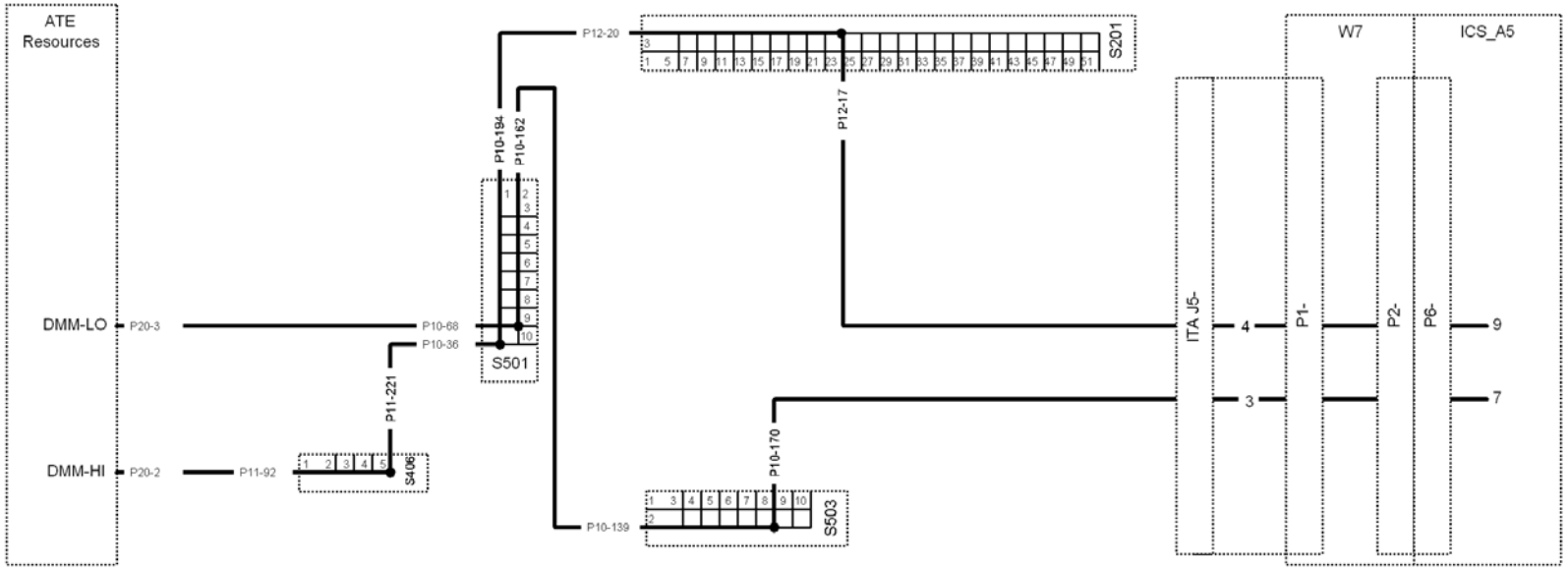
Connection Path as follows:



Step 2 UUT Identification (P6-9 to P6-7)

Test step 2 verifies the correct UUT is connected to the ITA by using the DMM to measure the resistance between P6-9 and P6-7. The resistance should be less than 10 ohms.

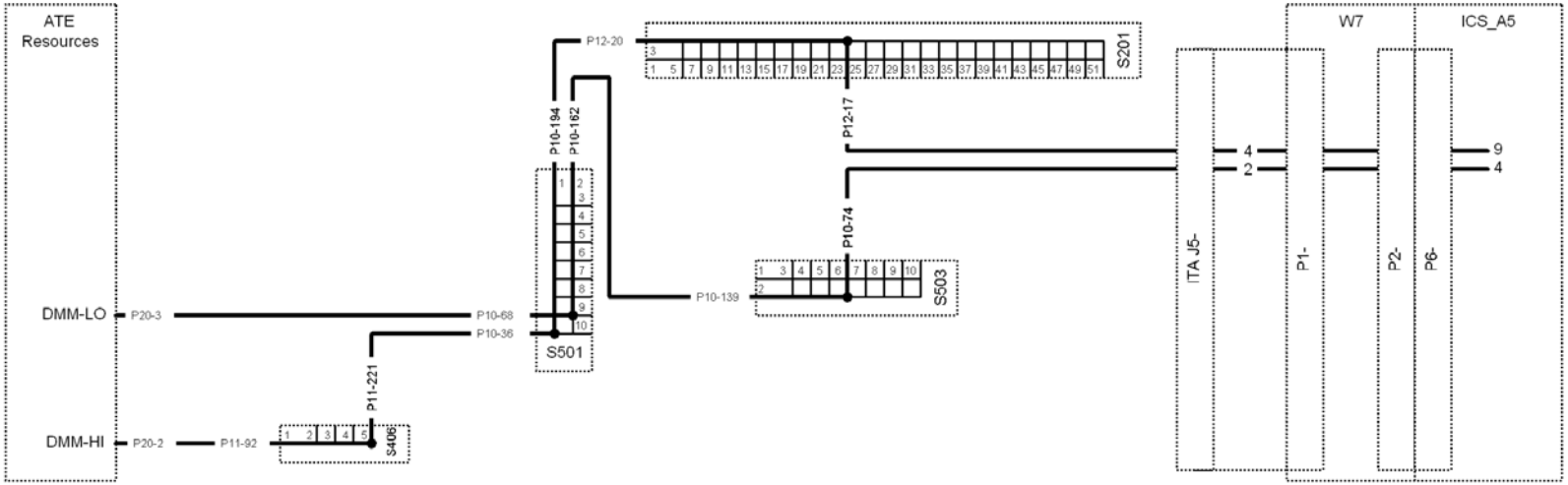
Connection Path as follows:


ATE
Resources
DMM-LO
P20-3
P10-68
P10-36
DMM-HI
P20-2
P11-92
P11-221
S406
P10-194
P10-162
S501
P12-20
S201
P12-17
P10-139
P10-170
S503
ITA J5-
4
3
W7
P1-
P2-
ICS_A5
P6-
9
7

Step 3 UUT Identification (P6-9 to P6-4)

Test step 3 verifies the correct UUT is connected to the ITA by using the DMM to measure the resistance between P6-9 and P6-4. The resistance should be less than 10 ohms.

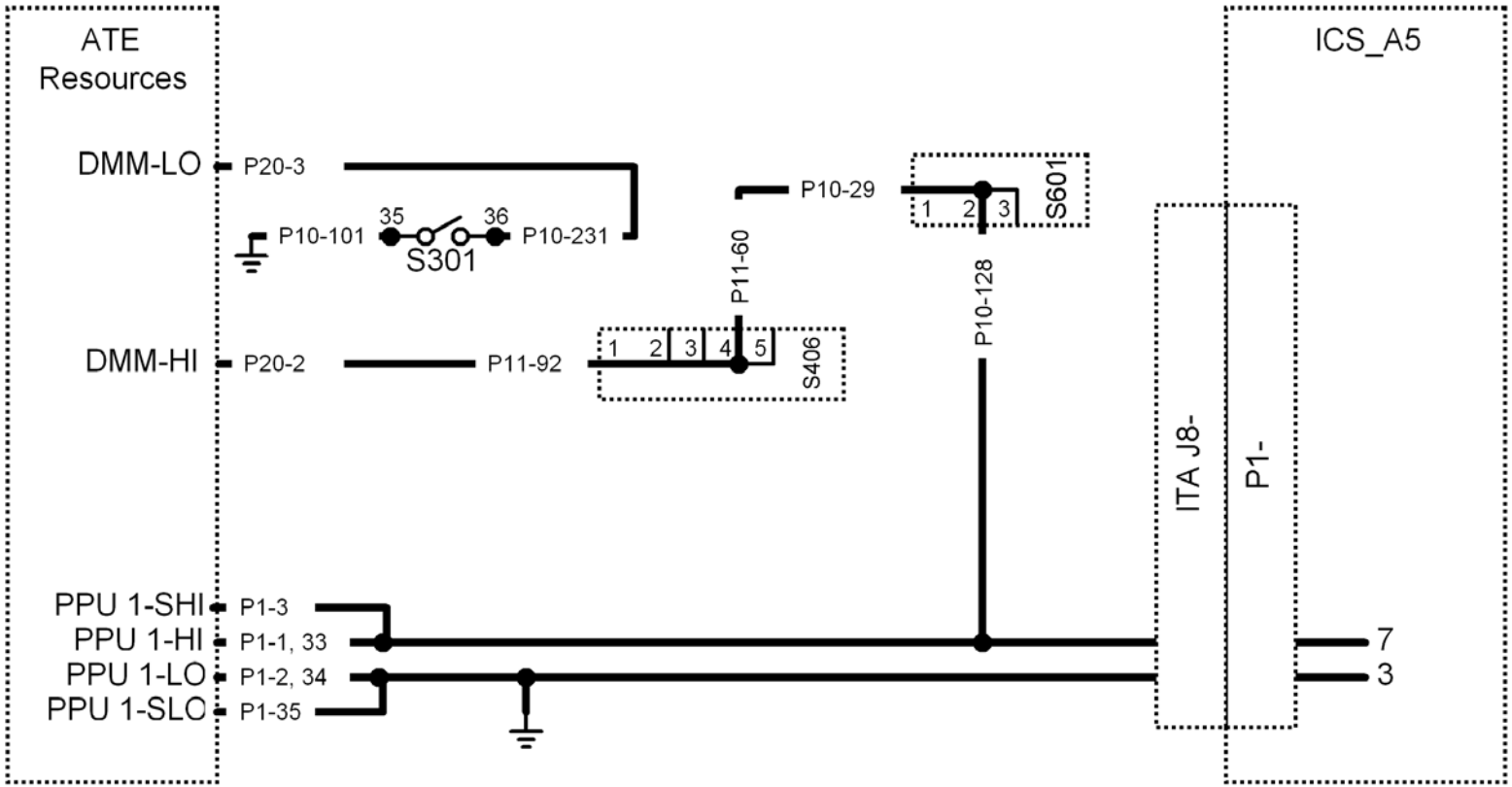
Connection Path as follows:


ATE Resources
DMM-LO
DMM-HI
P20-3
P20-2
P11-92
P11-221
S406
P10-68
P10-36
S501
P10-194
P10-162
P12-20
S201
P12-17
P10-74
P10-139
S503
ITA J5-
P1-
P2-
P6-
W7
ICS_A5

Step 4 +15 VDC Power STTO

Test step 4 verifies the +15 Vdc is safe to apply power by connecting PPU1 to the UUT but only applying +1.0 Vdc at 0.1 A. The DMM is used to measure the voltage from P1-7 to P1-3. The voltage should be between 750 mVdc and 1.1 Vdc. If an overload condition is present PPU1 will exceed its current limit and turn off before the measurement causing the test to fail.

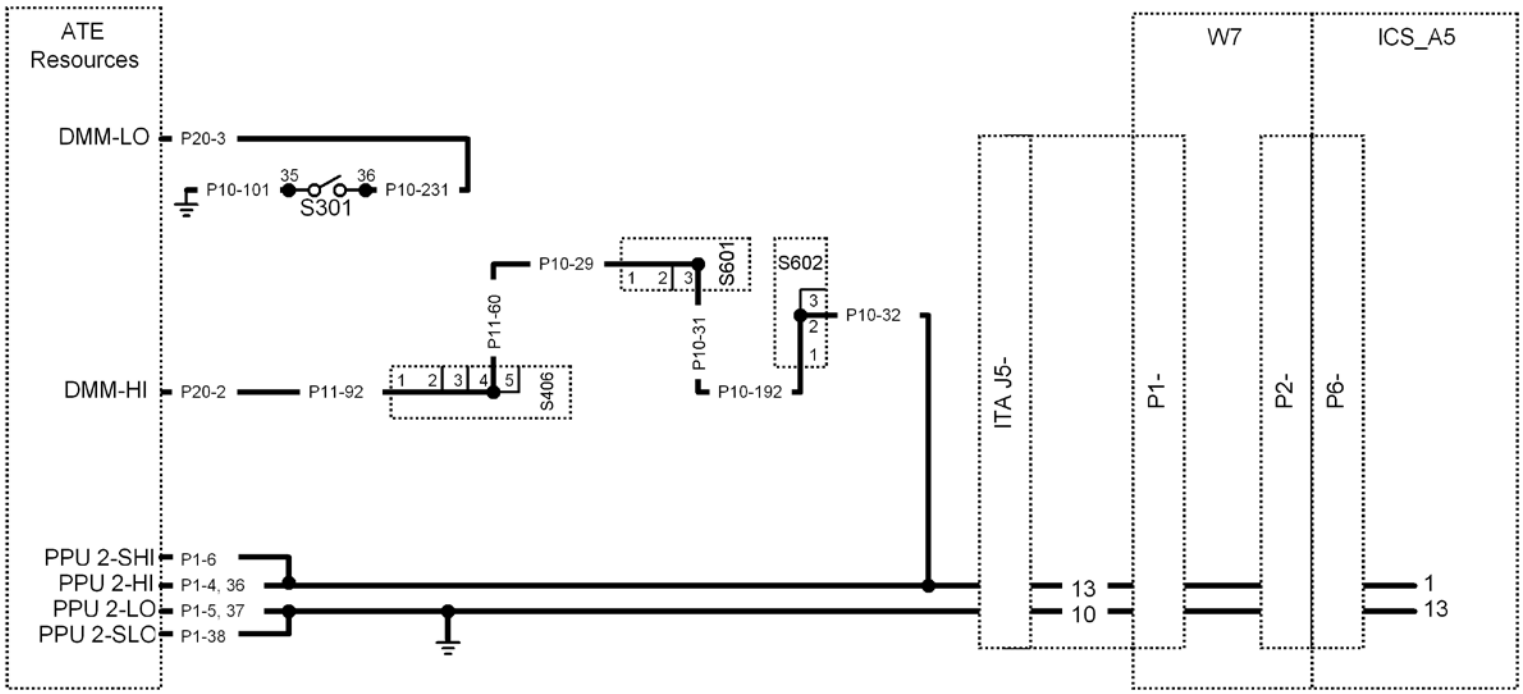
Connection Path as follows:


ATE
Resources
ICS_A5
DMM-LO
P20-3
P10-101
35
36
P10-231
S301
P10-29
S601
1 2 3
P11-60
P10-128
DMM-HI
P20-2
P11-92
1 2 3 4 5
S406
ITA J8-
P1-
PPU 1-SHI
P1-3
PPU 1-HI
P1-1, 33
PPU 1-LO
P1-2, 34
PPU 1-SLO
P1-35
7
3

Step 5 +24 VDC Power STTO

Test step 5 verifies the +24 Vdc is safe to apply power by connecting PPU2 to the UUT but only applying +1.0 Vdc at 0.1 A. The DMM is used to measure the voltage from P6-1 to P6-13. The voltage should be between 750 mVdc and 1.1 Vdc. If an overload condition is present PPU1 will exceed its current limit and turn off before the measurement causing the test to fail.

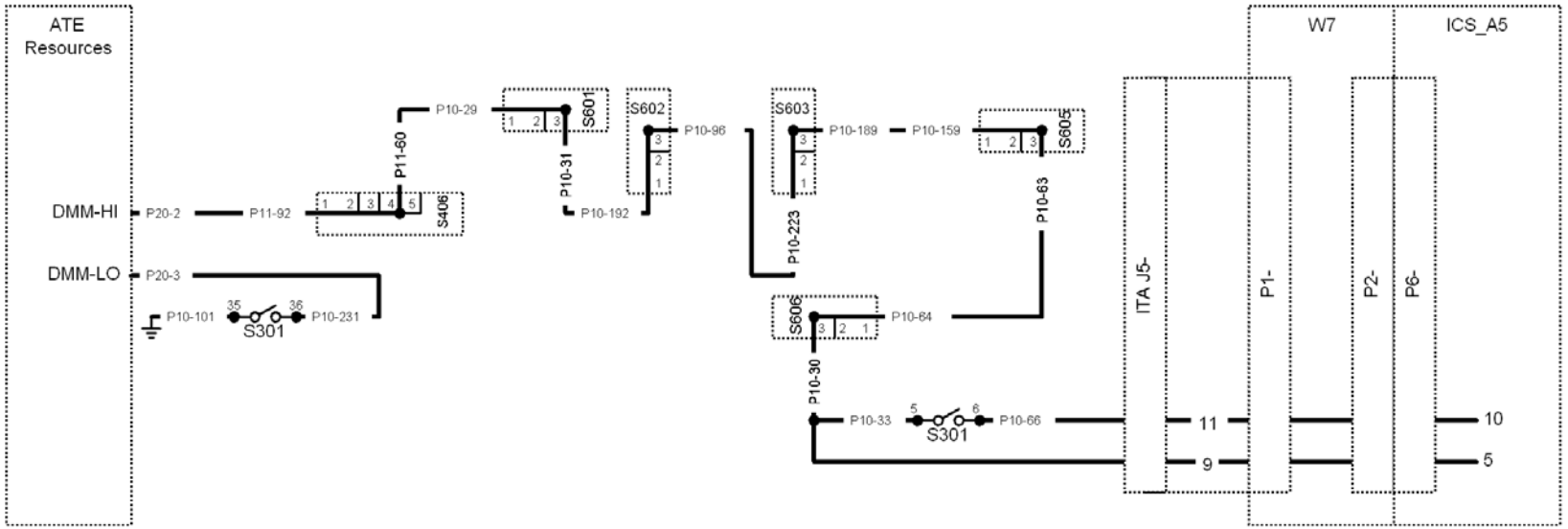
Connection Path as follows:


ATE
Resources
DMM-LO
P20-3
P10-101
35
36
P10-231
S301
P10-29
S601
1 2 3
S602
3
2
1
P10-32
P11-60
P10-31
DMM-HI
P20-2
P11-92
1 2 3 4 5
S406
P10-192
PPU 2-SHI
PPU 2-HI
PPU 2-LO
PPU 2-SLO
P1-6
P1-4, 36
P1-5, 37
P1-38
ITA J5-
W7
P1-
P2-
ICS_A5
P6-
13
10
1
13

Step 6 P6-5/10 -To- GND Test

Test step 6 verifies there is no short to ground on the OUTPUT and CONTROL lines. With P6-5 and P6-10 connected together, the DMM is used to measure the resistance between P6-5/10 and GND. The resistance should be greater than 10 ohms.

Connection Path as follows:


ATE Resources
DMM-HI
DMM-LO
P20-2
P20-3
P11-92
P10-101
P10-231
S301
S406
P11-60
P10-29
S601
P10-31
P10-192
S602
P10-96
S603
P10-189
P10-159
S605
P10-223
P10-63
S606
P10-64
P10-30
P10-33
P10-66
ITA J5-
W7
ICS_A5
P1-
P2-
P6-
11
9
10
5

UUT POWER UP

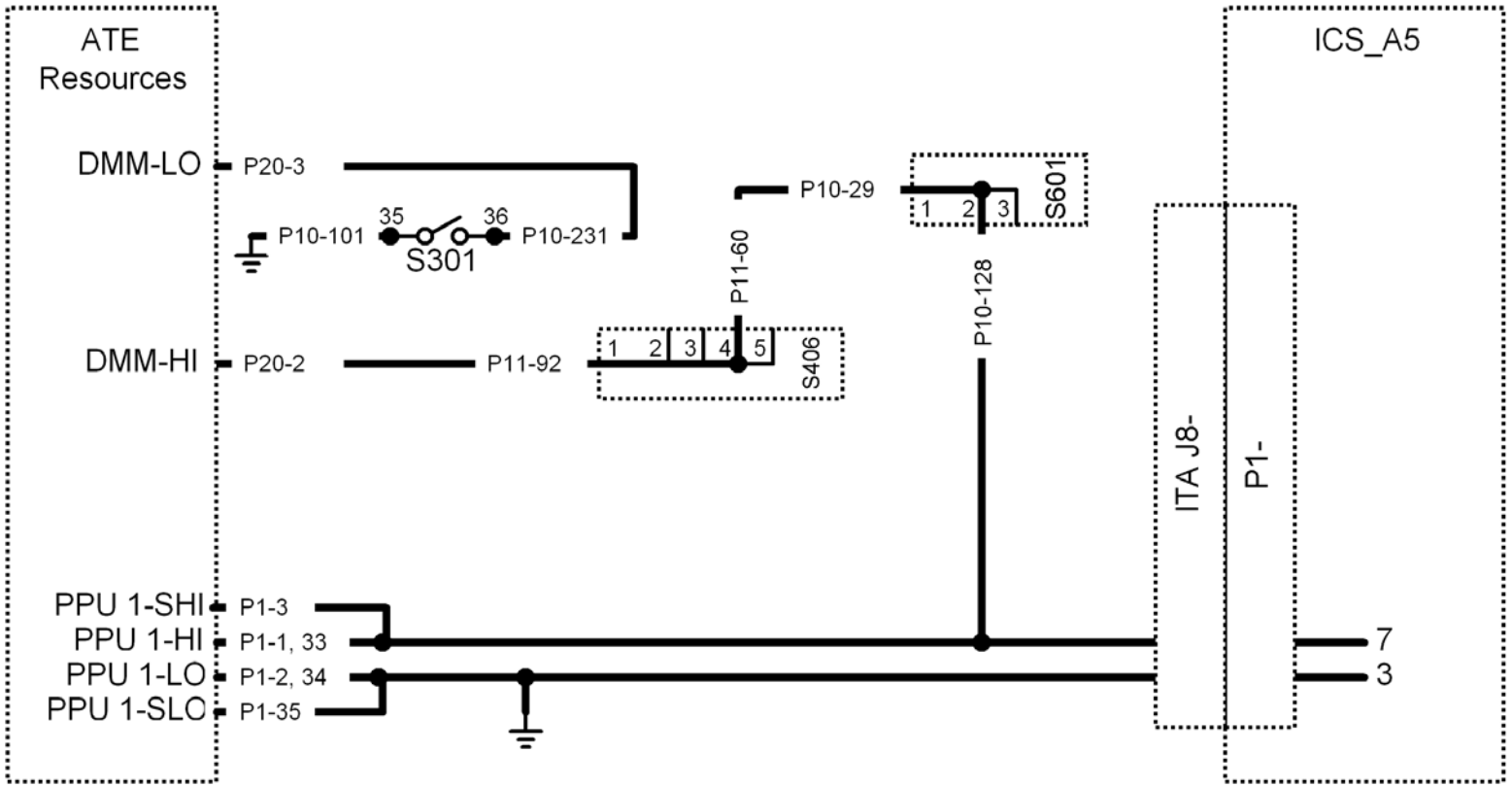
+15 Vdc at 0.5 A with a tolerance of ±0.25 Vdc and +24 Vdc at 2.0 A with a tolerance of 0.5 Vdc is required to power the UUT.

UUT POWER UP TESTS

Step 7 +15 VDC Power

Test step 7 verifies PPU1 can deliver +15 Vdc to the UUT by using the DMM to measure the voltage between P1-7 and P1-3. The voltage should be from 14.75 Vdc to 15.25 Vdc. PPU1 remains connected to the UUT for the remainder of testing.

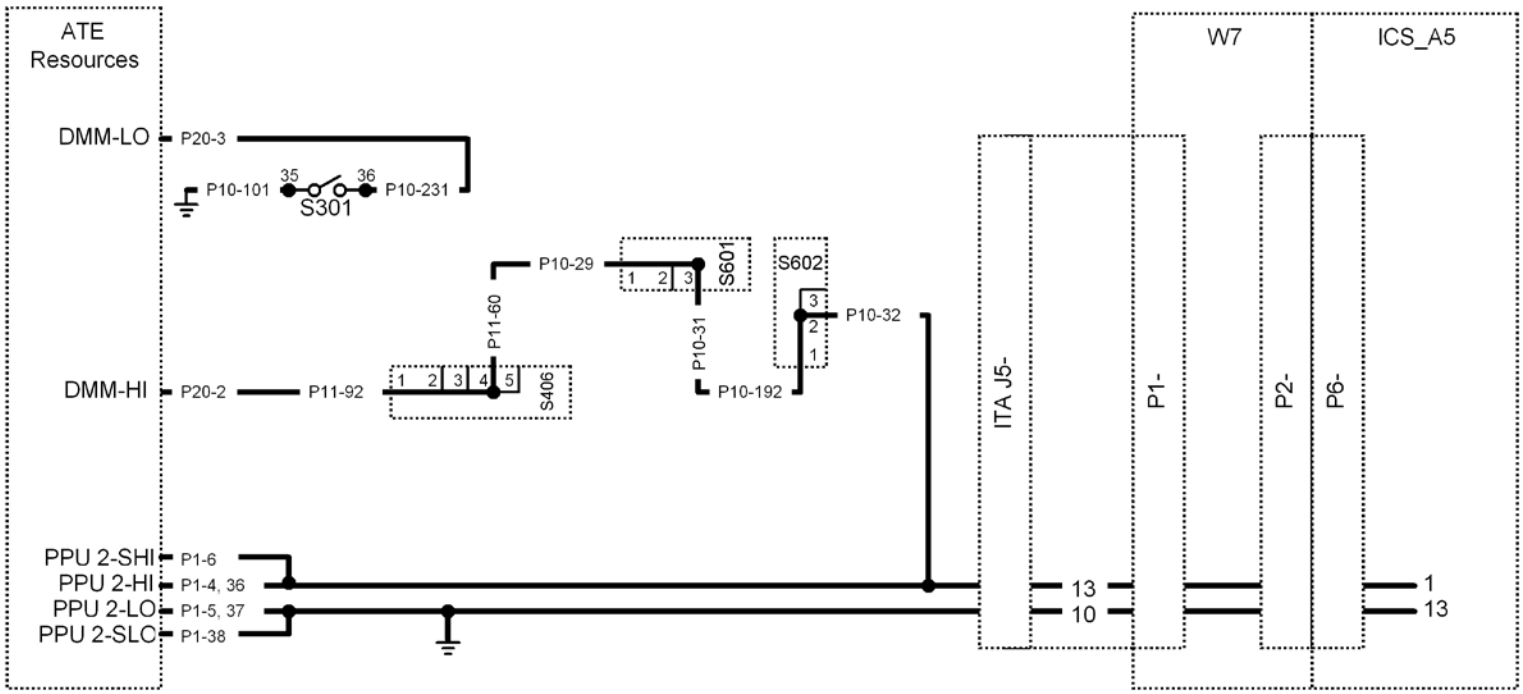
Connection Path as follows:


ATE
Resources
ICS_A5
DMM-LO
P20-3
P10-101
35
36
P10-231
S301
P10-29
1 2 3
S601
P11-60
P10-128
DMM-HI
P20-2
P11-92
1 2 3 4 5
S406
ITA J8-
P1-
PPU 1-SHI
P1-3
PPU 1-HI
P1-1, 33
PPU 1-LO
P1-2, 34
PPU 1-SLO
P1-35
7
3

Step 8 +24 VDC Power

Test step 8 verifies PPU2 can deliver +24 Vdc to the UUT by using the DMM to measure the voltage between P6-1 and P6-13. The voltage should be from 23.5 Vdc to 24.5 Vdc. Due to the 10 ohm load always connected at P6-5, PPU2 is removed following the test and re-applied when needed by test module 2. This is done to reduce possible damage to the UUT due to excessive heat generated by the dimmer circuit with the 10 ohm load connected.

Connection Path as follows:


ATE
Resources
DMM-LO
P20-3
P10-101
35
36
P10-231
S301
P10-29
S601
1 2 3
S602
3
2
1
P10-32
P11-60
P10-31
DMM-HI
P20-2
P11-92
1 2 3 4 5
S406
P10-192
PPU 2-SHI
PPU 2-HI
PPU 2-LO
PPU 2-SLO
P1-6
P1-4, 36
P1-5, 37
P1-38
ITA J5-
W7
P1-
P2-
ICS_A5
P6-
13
10
1
13

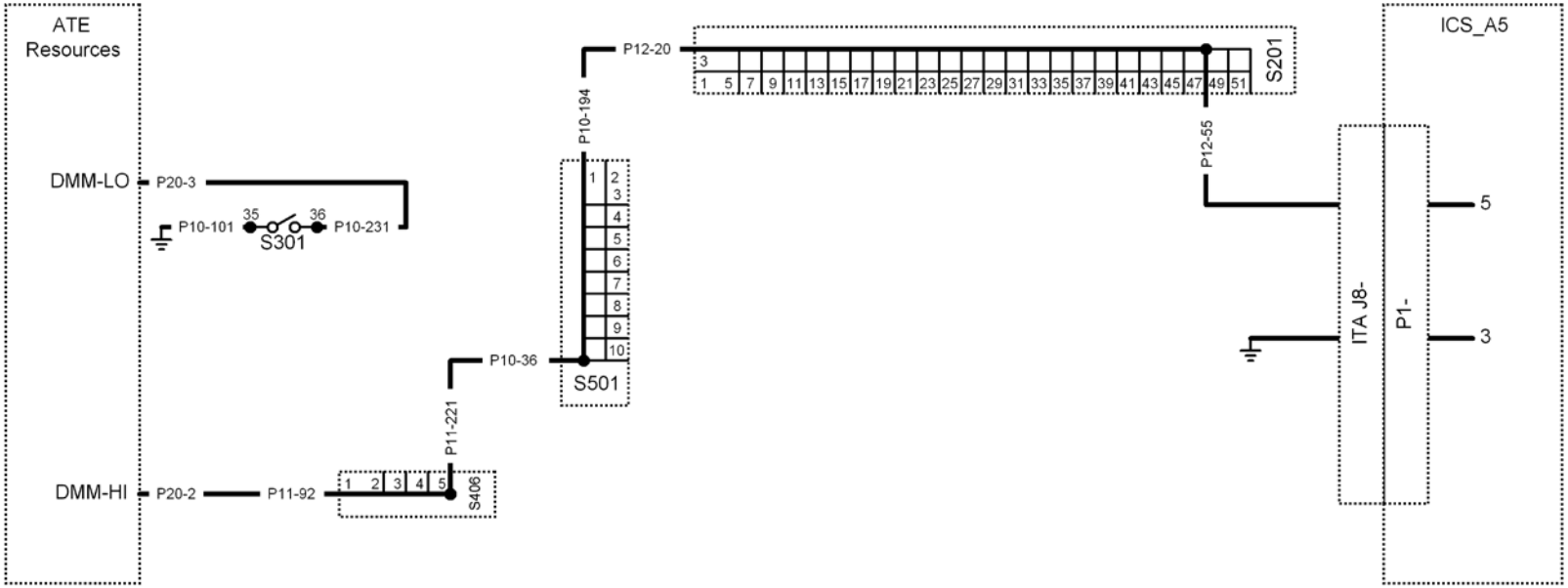
MODULE 1 POWER AMPLIFIER TESTS

Module 1 verifies the functionality of the audio power amplifier section of the UUT. The circuit gain is verified and the output signal distortion level is verified to be within the specified tolerance across the frequency range.

Step 101 C1 Short Test

Test step 101 verifies that coupling capacitor C1 is not short at the UUT AUDIO IN input by using the DMM to measure the voltage between P1-5 and P1-3. The voltage should be less than 0.5 Vdc.

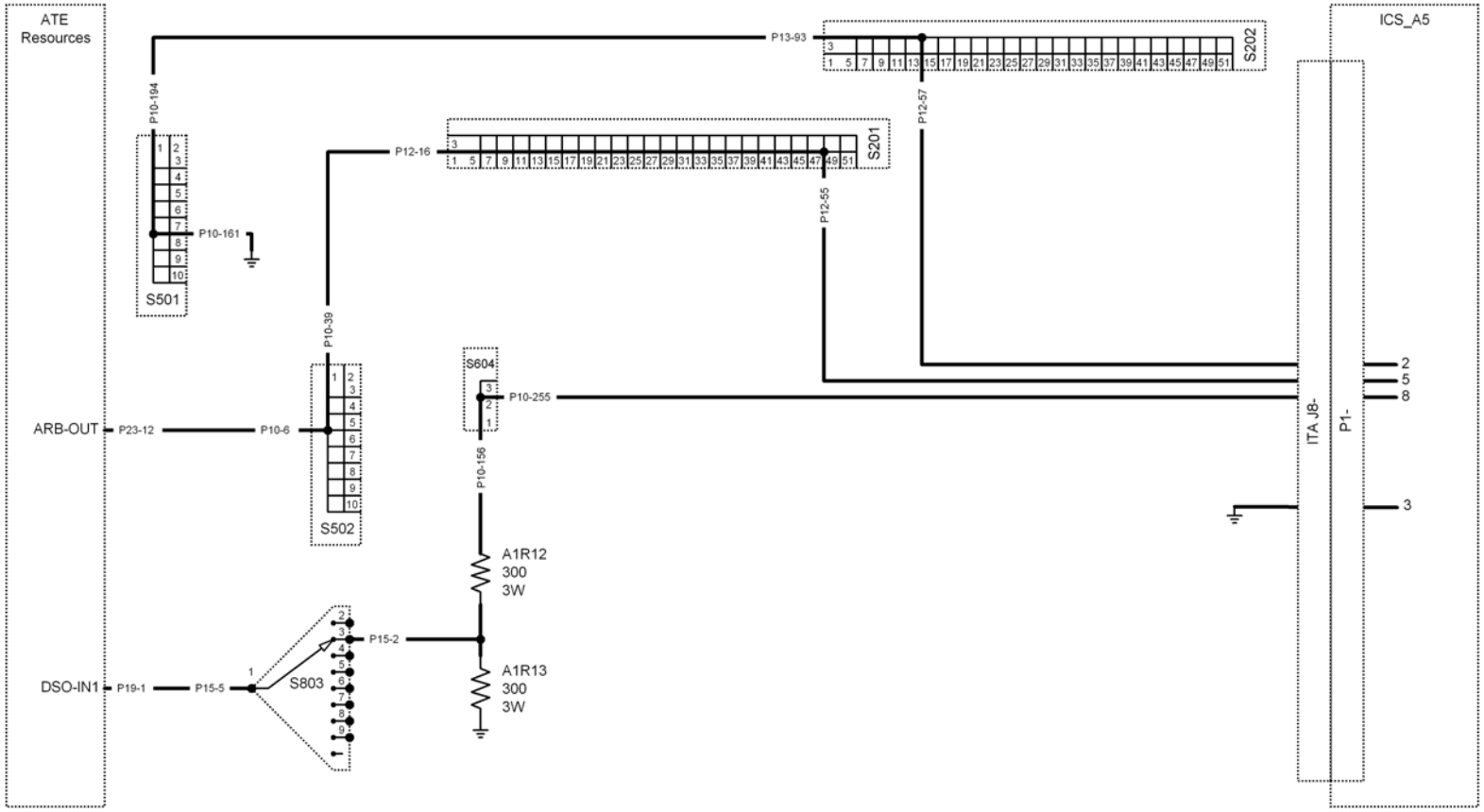
Connection Path as follows:


ATE
Resources
DMM-LO
P20-3
P10-101
35
36
P10-231
S301
DMM-HI
P20-2
P11-92
1 2 3 4 5
S406
P11-221
P10-36
P10-194
1 2
3
4
5
6
7
8
9
10
S501
P12-20
3
1 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49 51
S201
P12-55
ICS_A5
ITA J8-
P1-
5
3

Step 102 Amplifier Gain Test

Test step 102 verifies that the audio amplifier circuit is working correctly by using the ARB to apply a 4.0 Vpp, 1.0 KHz signal to P1-5 and using the DSO to measure the amplitude of the AC signal between P1-8 and P1-2. The amplitude should be greater than 45 Vpp. The actual reading will be one-half the UUT output level due to the effect of the ITA voltage divider made up of 1A1R12 and 1A1R13, which also serves as a 600 ohm load specified for the audio output. Resistors 1A1R12 and 1A1R13 are both 300 ohm 3 W.

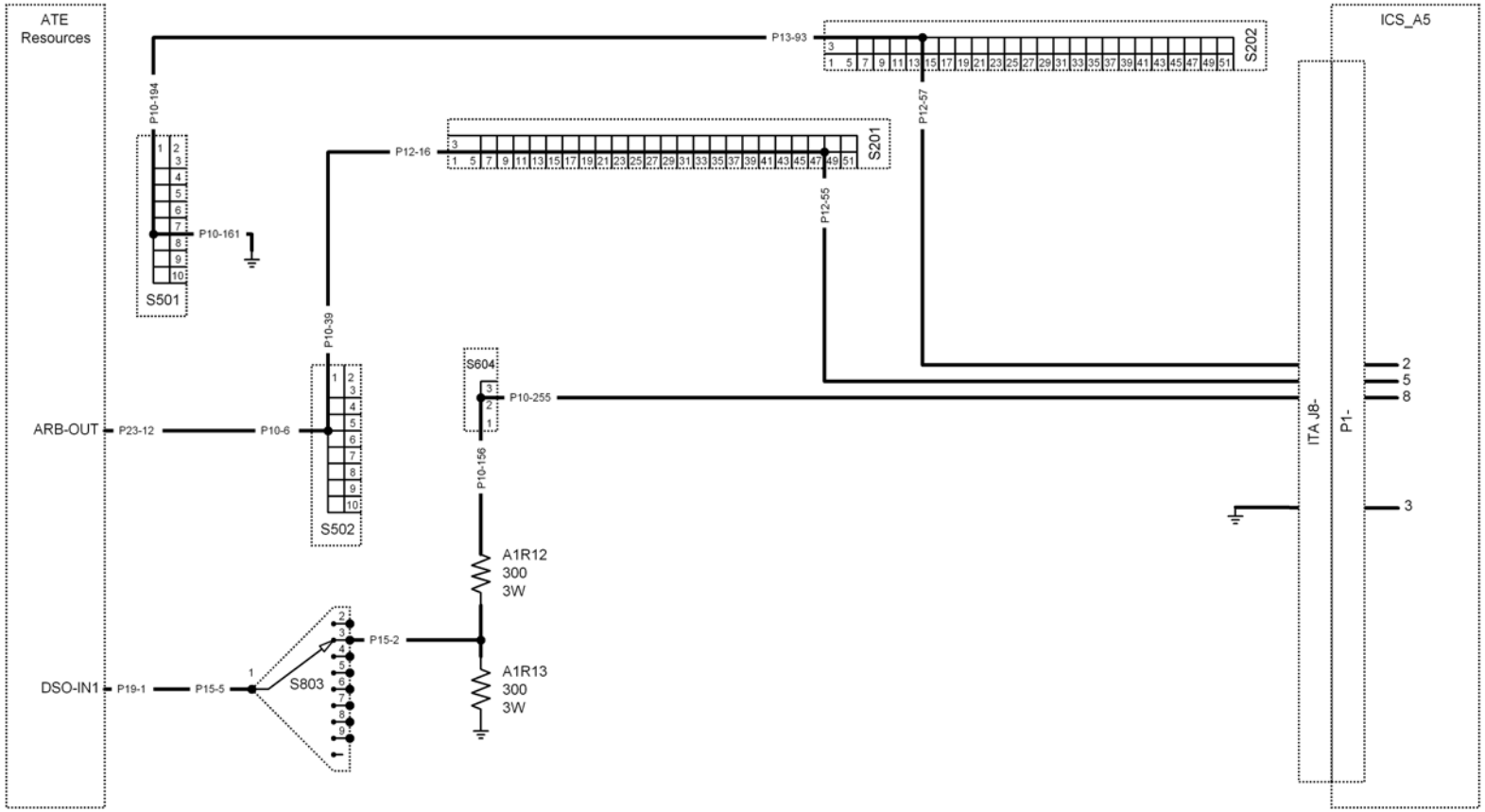
Connection Path as follows:


ATE
Resources
P13-93
S202
P12-57
P10-194
P12-16
S201
P12-55
P10-161
S501
P10-39
S604
P10-255
ARB-OUT
P23-12
P10-6
S502
P10-156
A1R12
300
3W
P15-2
A1R13
300
3W
DSO-IN1
P19-1
P15-5
S803
ICS_A5
ITA J8-
P1-
2
5
8
3

Step 103 1 KHz Distortion Test

Test step 103 verifies that the output of audio amplifier circuit is excessively distorted at its specified maximum output level of 40.5Vpp. Using the ARB to apply a 1.0 Vpp, 1.0 KHz signal to P1-5 and using the DSO to measure the amplitude of the AC signal between P1-8 and P1-2, the gain of the circuit is calculated. The amplitude of the input signal is then adjusted to achieve an output level of 40.5 +/-0.5Vpp. Distortion is measured by using the Digitizing Oscilloscope in waveform sampling mode to capture one complete cycle (1 KHz), sample 5000 voltage points and perform distortion analysis. The percentage distortion is calculated as the difference between the Voltage-PP of the signal versus the True-RMS voltage of an undistorted waveform of the same amplitude. The distortion should be less than 5%.

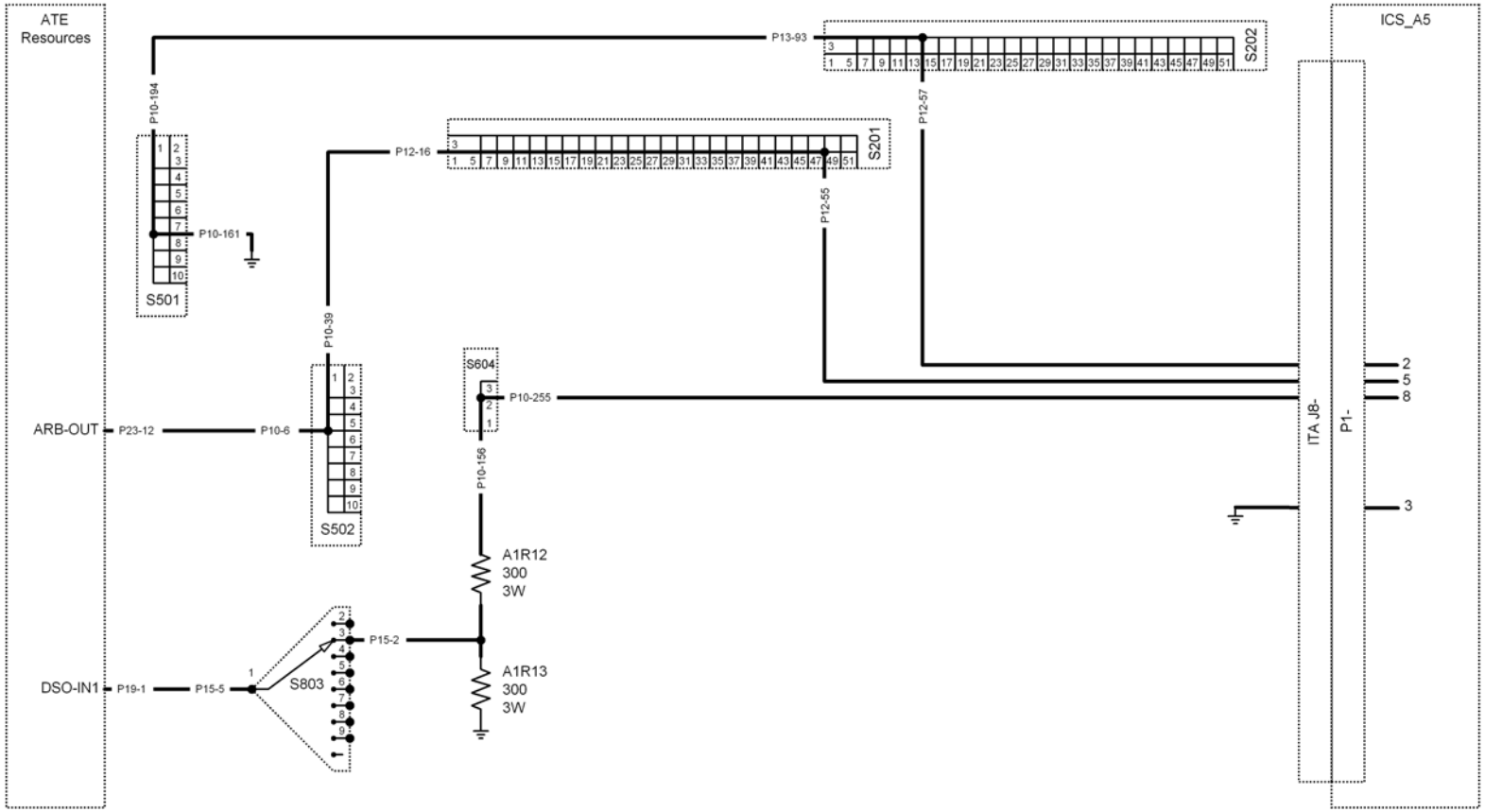
Connection Path as follows:


ATE
Resources
P13-93
S202
P12-57
P10-194
P12-16
S201
P12-55
P10-161
S501
P10-39
S604
P10-255
ARB-OUT
P23-12
P10-6
S502
P10-156
A1R12
300
3W
P15-2
A1R13
300
3W
DSO-IN1
P19-1
P15-5
S803
ICS_A5
ITA J8-
P1-
2
5
8
3

Step 104 450 Hz Distortion Test

Test step 104 verifies that the output of audio amplifier circuit is excessively distorted at its specified maximum output level of 40.5Vpp. Using the ARB to apply a 1.0 Vpp, 450 Hz signal to P1-5 and using the DSO to measure the amplitude of the AC signal between P1-8 and P1-2, the gain of the circuit is calculated. The amplitude of the input signal is then adjusted to achieve an output level of 40.5 +/-0.5Vpp. Distortion is measured by using the Digitizing Oscilloscope in waveform sampling mode to capture one complete cycle (450 Hz), sample 5555 voltage points and perform distortion analysis. The percentage distortion is calculated as the difference between the Voltage-PP of the signal versus the True-RMS voltage of an undistorted waveform of the same amplitude. The distortion should be less than 5%.

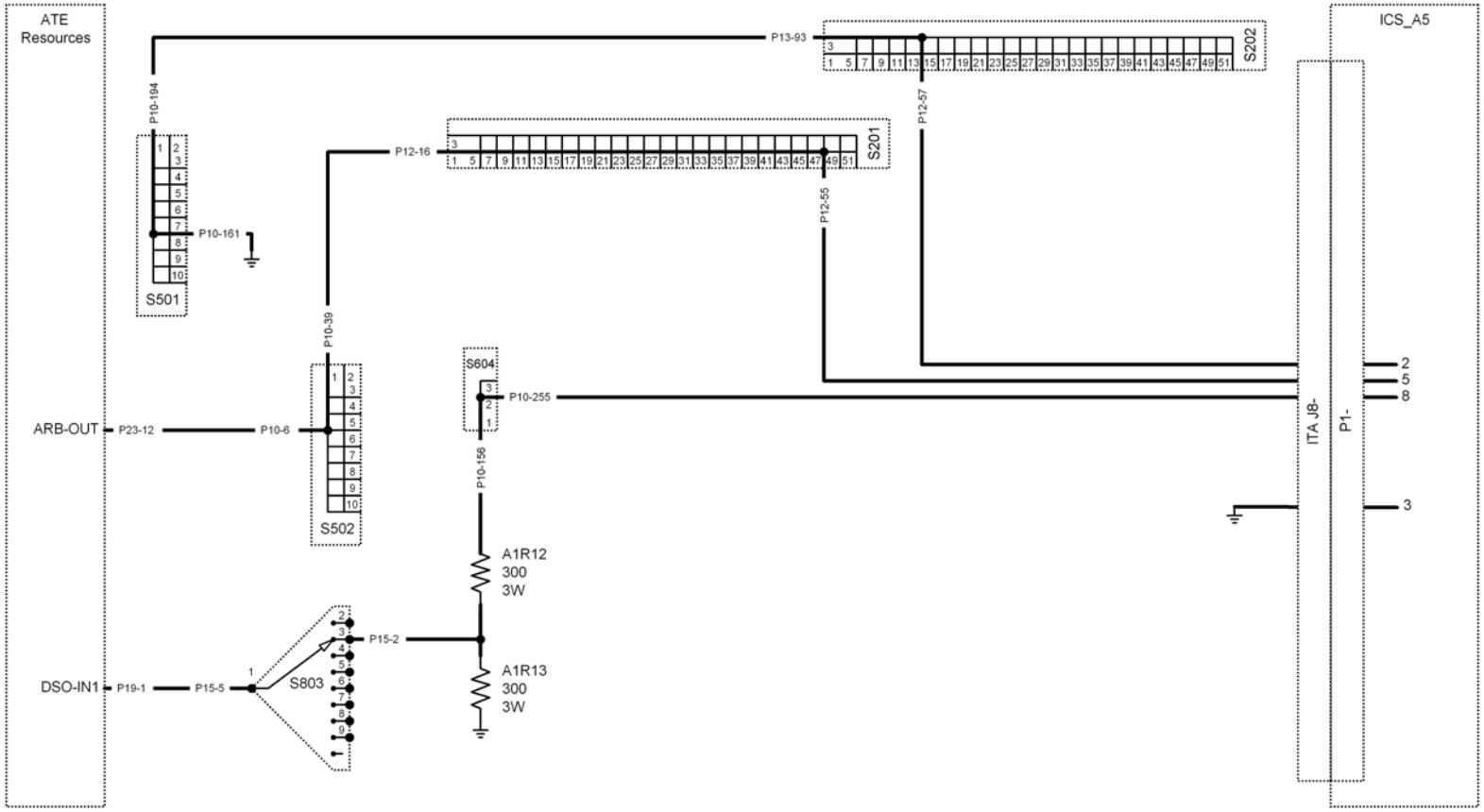
Connection Path as follows:


ATE
Resources
P13-93
S202
P12-57
P10-194
P12-16
S201
P12-55
P10-161
S501
P10-39
S604
P10-255
ARB-OUT
P23-12
P10-6
S502
P10-156
A1R12
300
3W
P15-2
A1R13
300
3W
DSO-IN1
P19-1
P15-5
S803
ICS_A5
ITA J8-
P1-
2
5
8
3

Step 105 1.5 KHz Distortion Test

Test step 105 verifies that the output of audio amplifier circuit is excessively distorted at its specified maximum output level of 40.5Vpp. Using the ARB to apply a 1.0 Vpp, 1.5 KHz signal to P1-5 and using the DSO to measure the amplitude of the AC signal between P1-8 and P1-2, the gain of the circuit is calculated. The amplitude of the input signal is then adjusted to achieve an output level of 40.5 +/-0.5Vpp. Distortion is measured by using the Digitizing Oscilloscope in waveform sampling mode to capture one complete cycle (1.5 KHz), sample 6666 voltage points and perform distortion analysis. The percentage distortion is calculated as the difference between the Voltage-PP of the signal versus the True-RMS voltage of an undistorted waveform of the same amplitude. The distortion should be less than 5%.

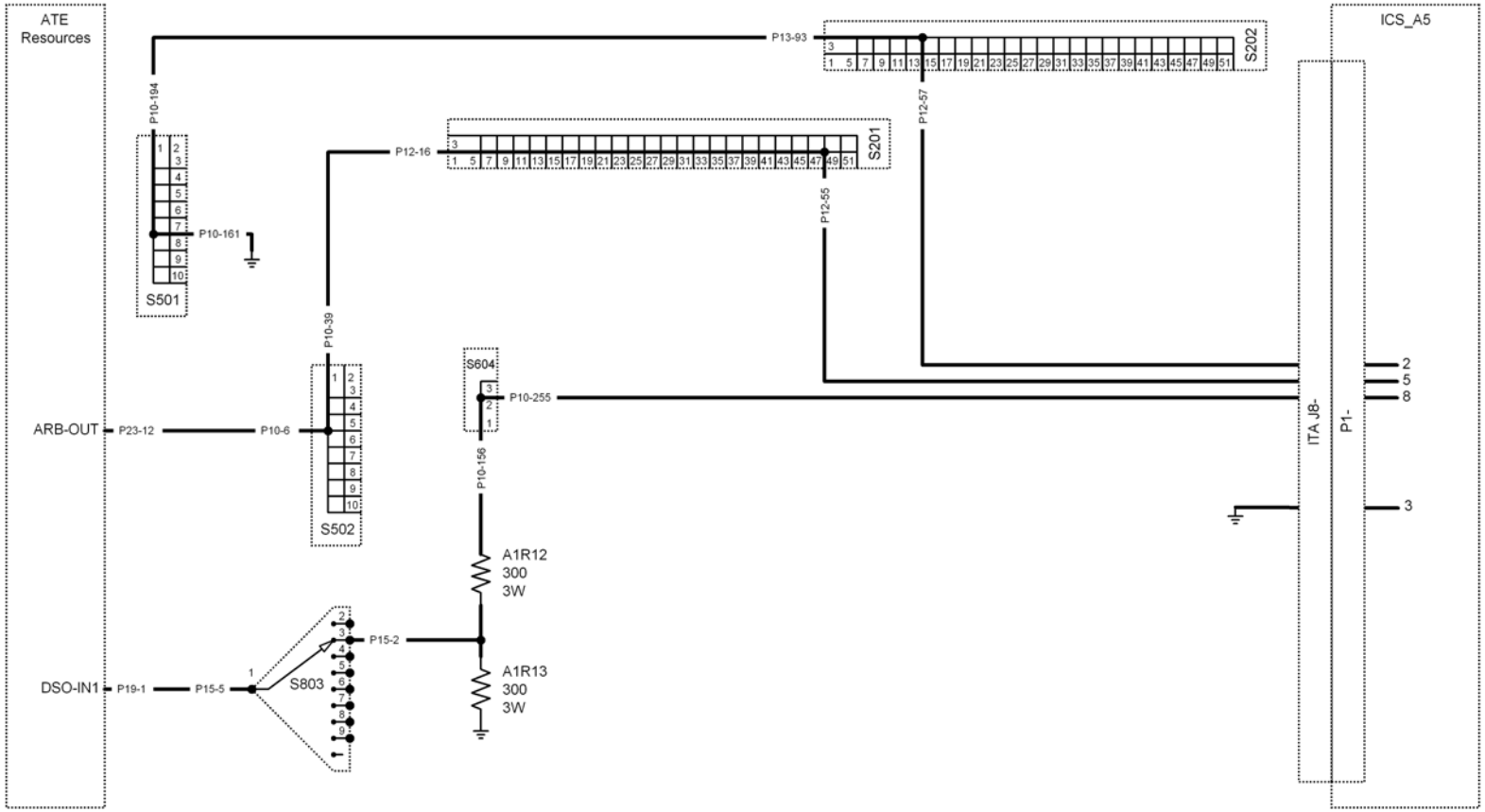
Connection Path as follows:


ATE
Resources
P13-93
S202
P12-57
ICS_A5
P10-194
P12-16
S201
P12-55
P10-161
S501
P10-39
S604
P10-255
ARB-OUT
P23-12
P10-6
S502
P10-156
ITA J8-
P1-
2
5
8
3
A1R12
300
3W
P15-2
A1R13
300
3W
DSO-IN1
P19-1
P15-5
S803

Step 106 2 KHz Distortion Test

Test step 106 verifies that the output of audio amplifier circuit is excessively distorted at its specified maximum output level of 40.5Vpp. Using the ARB to apply a 1.0 Vpp, 2.0 KHz signal to P1-5 and using the DSO to measure the amplitude of the AC signal between P1-8 and P1-2, the gain of the circuit is calculated. The amplitude of the input signal is then adjusted to achieve an output level of 40.5 +/-0.5Vpp. Distortion is measured by using the Digitizing Oscilloscope in waveform sampling mode to capture one complete cycle (2 KHz), sample 5000 voltage points and perform distortion analysis. The percentage distortion is calculated as the difference between the Voltage-PP of the signal versus the True-RMS voltage of an undistorted waveform of the same amplitude. The distortion should be less than 5%.

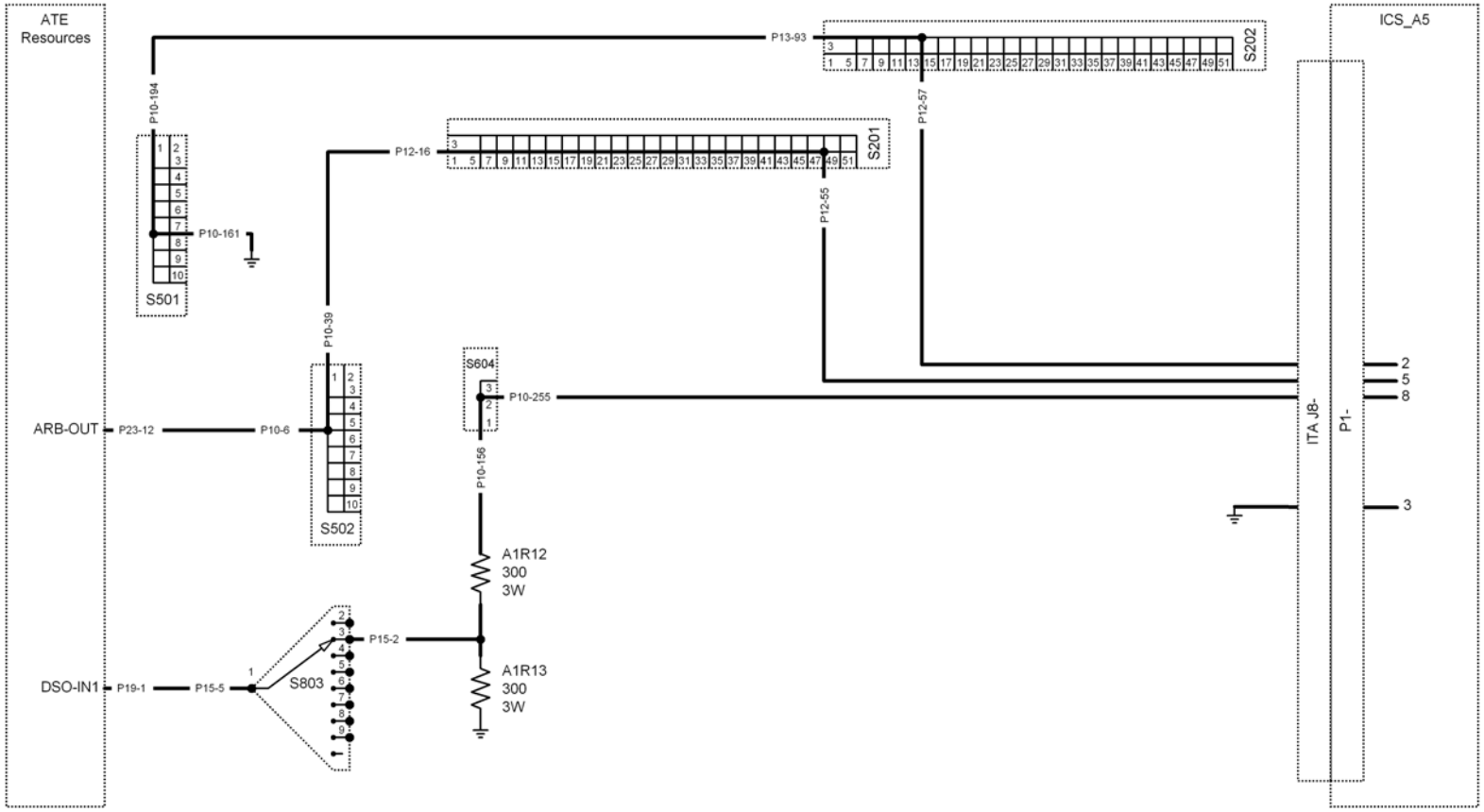
Connection Path as follows:


ATE
Resources
P13-93
S202
P12-57
P10-194
P12-16
S201
P12-55
P10-161
S501
P10-39
S604
P10-255
ARB-OUT
P23-12
P10-6
S502
P10-156
A1R12
300
3W
P15-2
A1R13
300
3W
DSO-IN1
P19-1
P15-5
S803
ICS_A5
ITA J8-
P1-
2
5
8
3

Step 107 2.5 KHz Distortion Test

Test step 107 verifies that the output of audio amplifier circuit is excessively distorted at its specified maximum output level of 40.5Vpp. Using the ARB to apply a 1.0 Vpp, 2.5 KHz signal to P1-5 and using the DSO to measure the amplitude of the AC signal between P1-8 and P1-2, the gain of the circuit is calculated. The amplitude of the input signal is then adjusted to achieve an output level of 40.5 +/-0.5Vpp. Distortion is measured by using the Digitizing Oscilloscope in waveform sampling mode to capture one complete cycle (2.5 KHz), sample 4000 voltage points and perform distortion analysis. The percentage distortion is calculated as the difference between the Voltage-PP of the signal versus the True-RMS voltage of an undistorted waveform of the same amplitude. The distortion should be less than 5%.

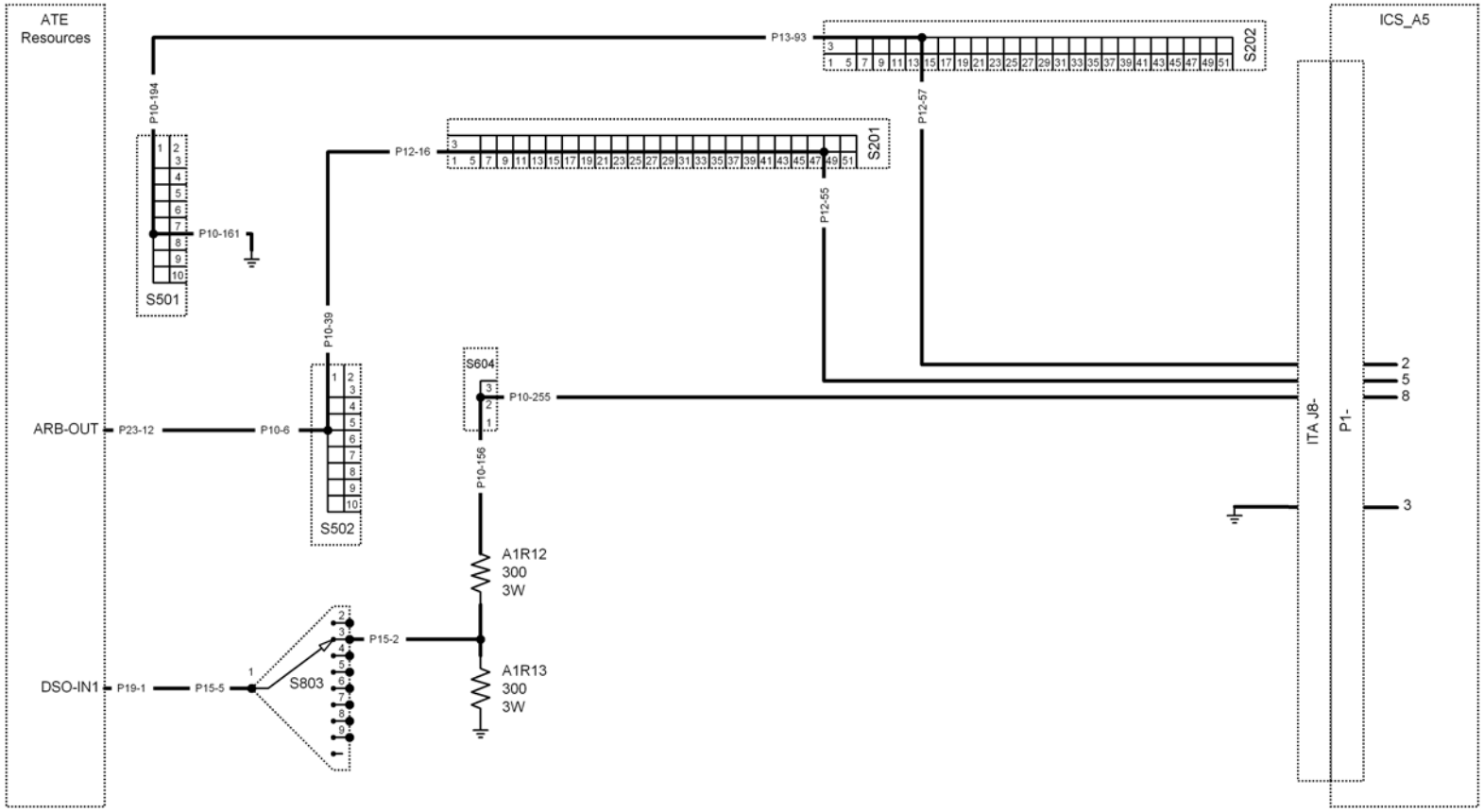
Connection Path as follows:


ATE
Resources
P13-93
S202
P12-57
P10-194
P12-16
S201
P12-55
P10-161
S501
P10-39
S604
P10-255
ARB-OUT
P23-12
P10-6
S502
P10-156
A1R12
300
3W
P15-2
A1R13
300
3W
DSO-IN1
P19-1
P15-5
S803
ICS_A5
ITA J8-
P1-
2
5
8
3

Step 108 2.95 KHz Distortion Test

Test step 108 verifies that the output of audio amplifier circuit is excessively distorted at its specified maximum output level of 40.5Vpp. Using the ARB to apply a 1.0 Vpp, 2.95 KHz signal to P1-5 and using the DSO to measure the amplitude of the AC signal between P1-8 and P1-2, the gain of the circuit is calculated. The amplitude of the input signal is then adjusted to achieve an output level of 40.5 +/-0.5Vpp. Distortion is measured by using the Digitizing Oscilloscope in waveform sampling mode to capture one complete cycle (2.95 KHz), sample 3389 voltage points and perform distortion analysis. The percentage distortion is calculated as the difference between the Voltage-PP of the signal versus the True-RMS voltage of an undistorted waveform of the same amplitude. The distortion should be less than 5%.

Connection Path as follows:


ATE
Resources
P13-93
S202
P12-57
P10-194
P12-16
S201
P12-55
P10-161
S501
P10-39
S604
P10-255
ARB-OUT
P23-12
P10-6
S502
P10-156
A1R12
300
3W
P15-2
A1R13
300
3W
DSO-IN1
P19-1
P15-5
S803
ICS_A5
ITA J8-
P1-
2
5
8
3

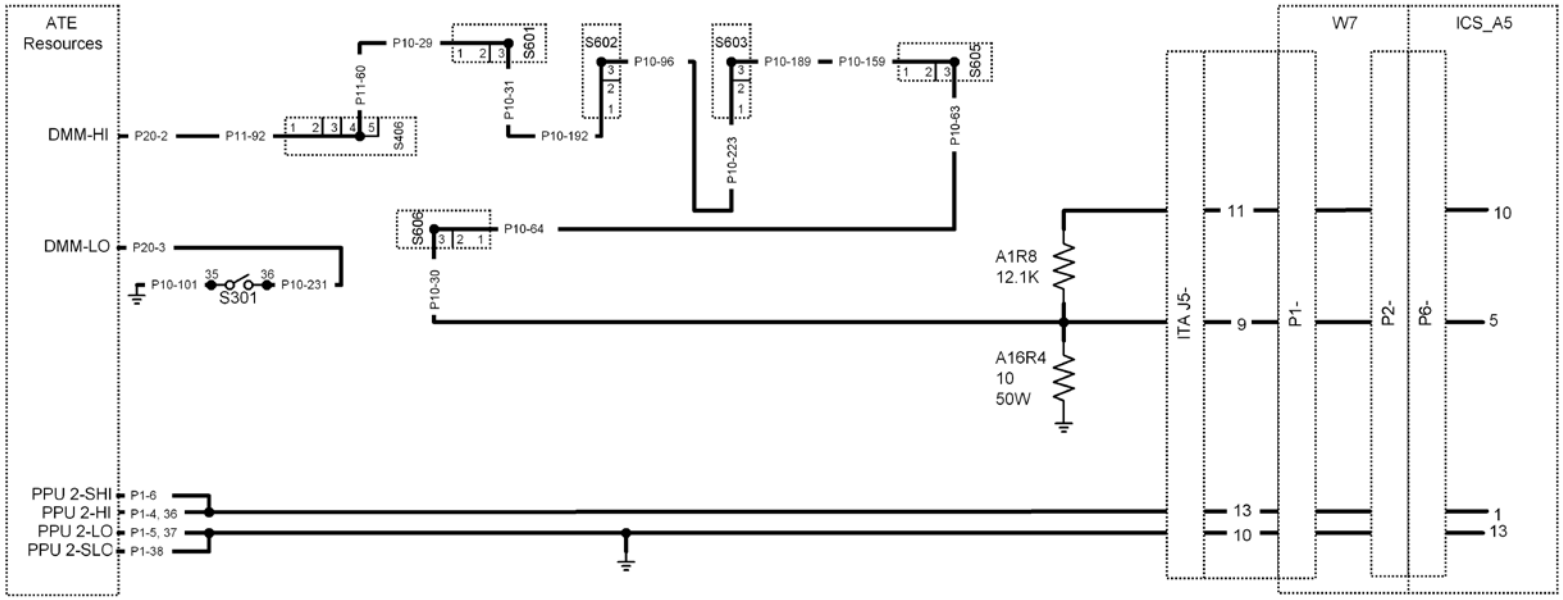
MODULE 2 DIMMER CONTROL TESTS

Module 2 verifies the lamp dimmer regulator circuit is functional at the specified minimum and maximum lamp voltage levels of 5.0 and 18.0 volts.

Step 201 +18 VDC Lamp Output Test

Test step 201 verifies that the maximum brightness setting of the dimmer regulator circuit is working correctly. The input voltage of +24 Vdc is applied to P6-1/GND using PPU2. With a 12.1 Kohm resistor (ITA A1R8) connected across P6-5 and P6-10 and a specified load of 50 ohms (50 W Resistor ITA A16R4) on the dimmer output of P6-5, the DMM is used to verify the voltage between P6-5 and P6-13 is 15.5 Vdc to 20.5 Vdc.

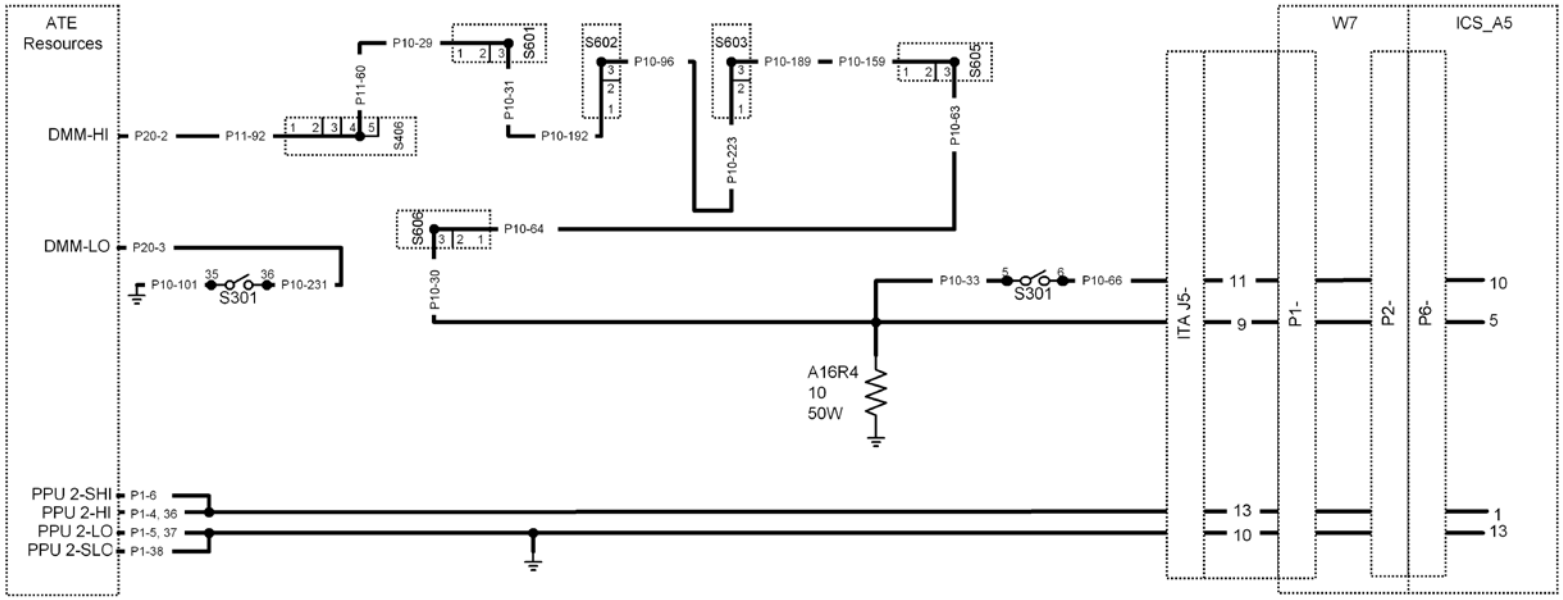
Connection Path as follows:


ATE Resources
DMM-HI
P20-2
P11-92
P11-60
S406
P10-29
S601
P10-31
P10-192
S602
P10-96
S603
P10-189
P10-159
S605
P10-63
P10-223
DMM-LO
P20-3
P10-101
S301
P10-231
S606
P10-64
P10-30
A1R8
12.1K
A16R4
10
50W
PPU 2-SHI
PPU 2-HI
PPU 2-LO
PPU 2-SLO
P1-6
P1-4, 36
P1-5, 37
P1-38
ITA J5-
W7
ICS_A5
P1-
P2-
P6-
11
9
13
10
10
5
1
13

Step 202 +5 VDC Lamp Output Test

Test step 202 verifies that the minimum brightness setting of the dimmer regulator circuit is working correctly. The input voltage of +24 Vdc is applied to P6-1/GND using PPU2. With P6-5 connected to P6-10 (using tester switching) and a specified load of 50 ohms (50 W Resistor ITA A16R4) on the dimmer output of P6-5, the DMM is used to verify the voltage between P6-5 and P6-13 is 4.0 Vdc to 6.0 Vdc.

Connection Path as follows:


ATE Resources
DMM-HI
P20-2
P11-92
P11-60
S406
P10-29
S601
P10-31
P10-192
S602
P10-96
S603
P10-189
P10-159
S605
P10-63
P10-223
DMM-LO
P20-3
P10-101
S301
P10-231
S606
P10-64
P10-30
P10-33
S301
P10-66
A16R4
10
50W
PPU 2-SHI
PPU 2-HI
PPU 2-LO
PPU 2-SLO
P1-6
P1-4, 36
P1-5, 37
P1-38
W7
ICS_A5
ITA J5-
P1-
P2-
P6-
11
9
13
10
10
5
1
13

FUNCTIONAL FLOW CHART (FFC)