

English Language Test Description

Contract Number: N00244-09-C-0054

For

Unit Under Test

UUT Nomenclature: DPCM CCA
UUT Part Number: 2618582-1
UUT Reference Designator: CON A6

From

Assault Amphibious Vehicle
AN/PSM-115

ATE (Automated Test Equipment) SYSTEM

AN/USM-657B(V)2 Third Echelon Test System (TETS)
AN/USM-717(V)2 Virtual Instrument Portable Equipment Repair / Tester (VIPER/T)

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1. Introduction

The Unit Under Test (UUT) for this English Language Test Description (ELTD) is the DPCM Circuit Card Assembly (CCA), Part Number 2618582-1. The CCA is reference designator CON A6 in the Controller C-10879/MSQ-115 Line Replaceable Unit (LRU) part number 2618506-1. The LRU resides in the Assault Amphibious Vehicle (AAV) Weapon System.

1.1. Scope

An ELTD is a detailed supplementary document consisting of textual test descriptions with graphical representation of signal interconnectivity and a functional flow chart.

1.2. Purpose

The purpose of this document is to provide English language test descriptions for the TP_AAV_CON_A6 test program, to a level of detail used for maintenance purposes. The TP_AAV_CON_A6 test program makes up part of the AN/PSM-115 Application Program Set (APS).

1.3. Content Arrangement

The document is laid out in the sequence the Test Program Set (TPS) would be executed when a 95 “Run All Mods” is entered in the main menu. A paragraph at the beginning of each module will describe the test description for that module. Each step will contain a description for that particular test followed by a graphical representation of the connections made from the receiver, through the Interface Test Adapter (ITA) and cable W10 to the DPCM CCA. A Functional Flow Chart resides at the end of the document.

2. English Language Test Description (ELTD)

WEAPON SYSTEM: Assault Amphibious Vehicle (AAV)

UNIT UNDER TEST: 2618582-1

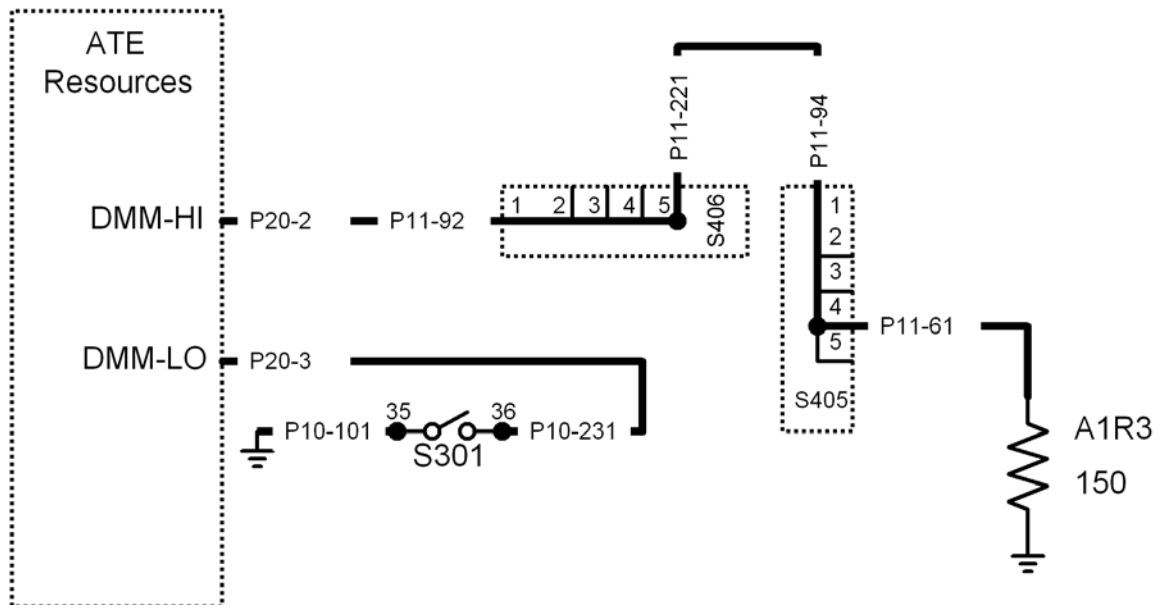
TEST PROGRAM SET: TP_AAV_CON_A6

SAFE TO TURN ON TESTS

Step 1 ITA Identification

Test step 1 verifies the correct ITA is installed by using the DMM to measure the resistance of ITA A1R3. The resistance should be from 149 ohms to 155 ohms.

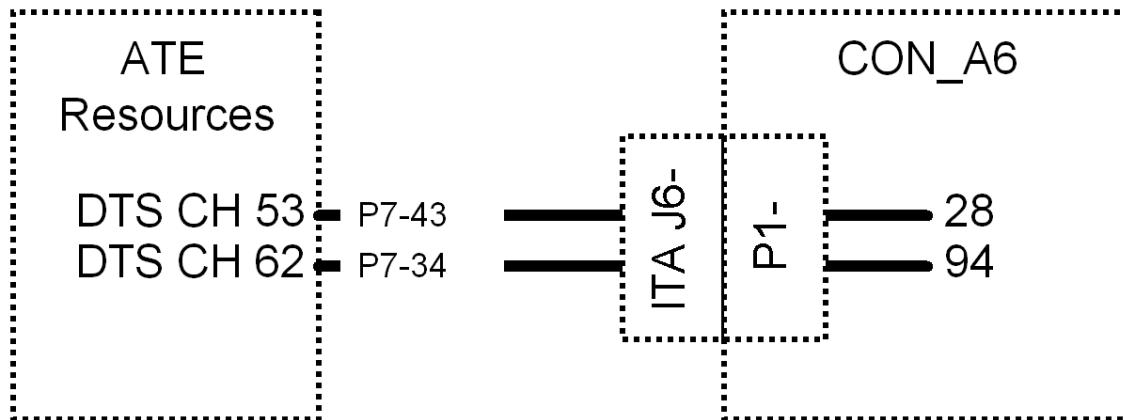
Connection Path as follows:



Step 2 UUT Identification

Test step 2 verifies the correct UUT is connected to the ITA by setting the DTS active load pull-ups to 5V by applying 1mA to P1-28 and P1-94. Each digital channel should be less than 2 Vdc.

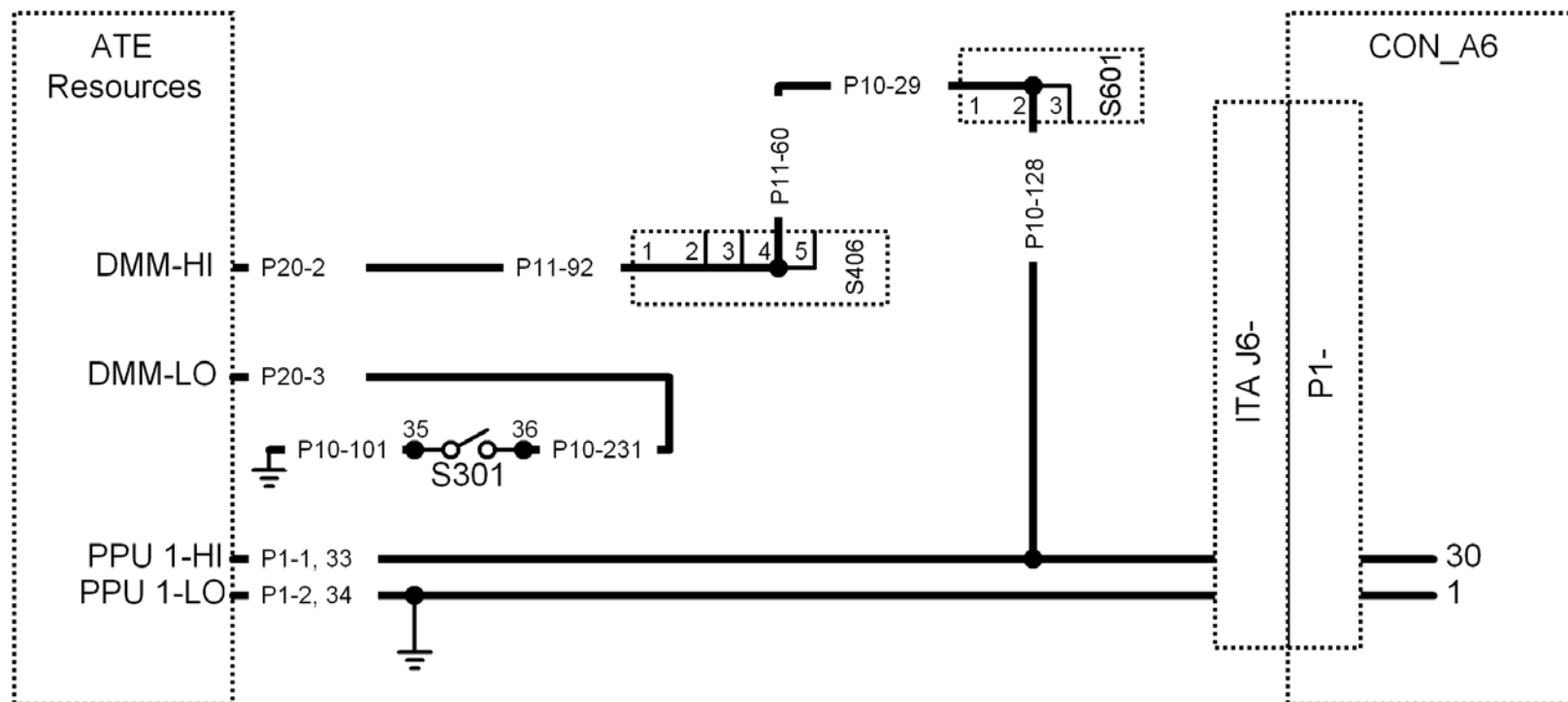
Connection Path as follows:



Step 3 UUT Input Power Safe-to-Turn-On

Test step 3 verifies the +5 Vdc is safe to apply power by connecting PPU1 to the UUT but only applying +1.0 Vdc at 0.1 A. The DMM is used to measure the voltage from P1-30 to GND. The voltage should be from 0.75 Vdc to 1.1 Vdc. If an overload condition is present PPU1 will exceed its current limit and turn off before the measurement causing the test to fail.

Connection Path as follows:



UUT POWER UP

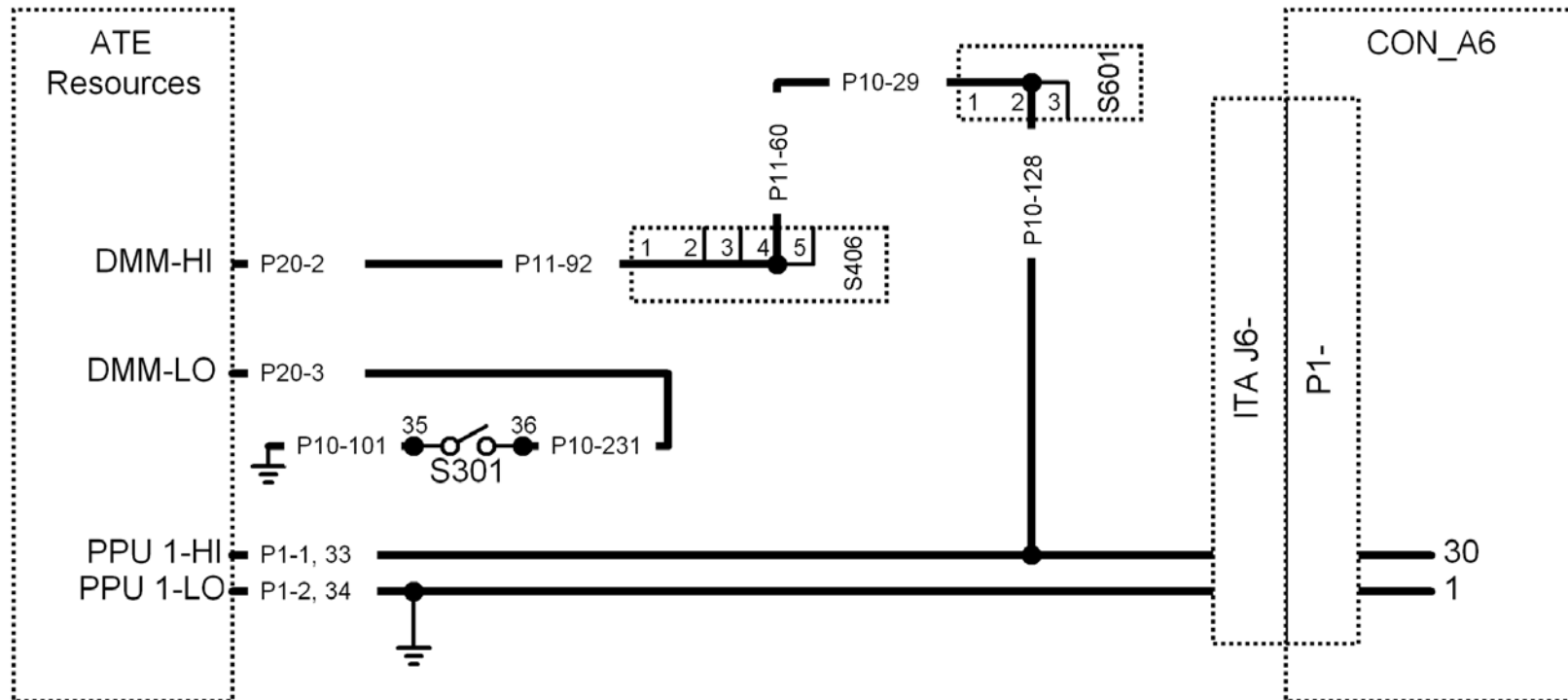
+5 Vdc at 2.0 A with a tolerance of ± 0.8 Vdc is required to power the UUT.

UUT POWER UP TESTS

Step 4 +5VDC Power-On Test

Test step 4 verifies PPU1 can deliver +5 Vdc to the UUT by using the DMM to measure the voltage between P1-30 and GND. The voltage should be from 4.2 Vdc to 5.8 Vdc. PPU1 remains connected to the UUT for the remainder of testing.

Connection Path as follows:



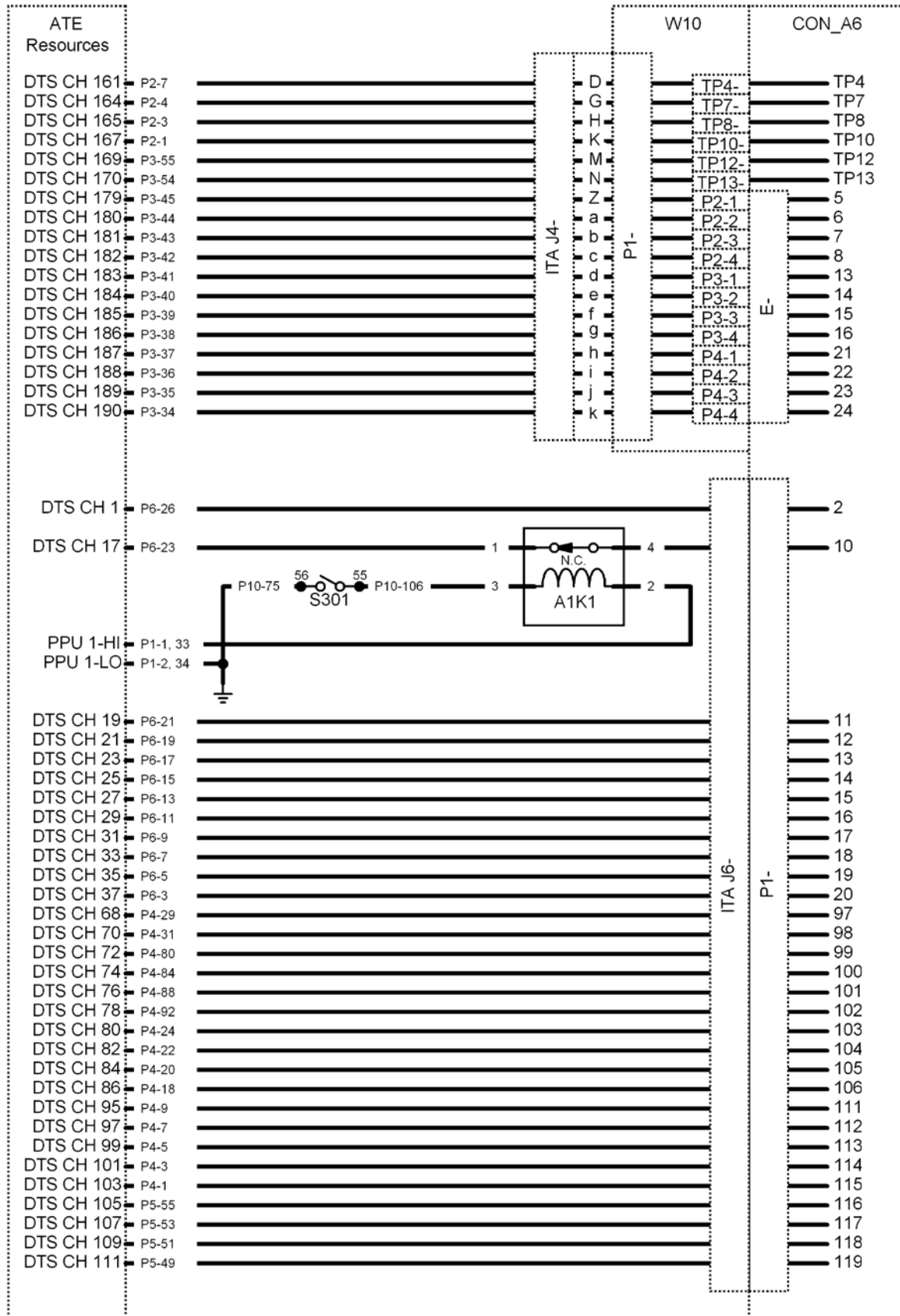
MODULE 1 LASAR DIGITAL TEST

Module 1 verifies the functionality of 99.58% of the UUT circuitry including U26 PROM data, but not the Vcc filter capacitors, the Y1 oscillator or the R8/R9 Tone Return voltage divider resistors. Test Step 101 is generated using a digital simulation and fault analysis tool called LASAR. The test data stored in these test files in conjunction with an external software diagnostic algorithm called M9-Series Diagnostics, will facilitate guided probe diagnostics seeded by fault dictionary diagnostics. LASAR processing generates detailed information about the quality of fault detection that is given by a particular test including a list of detected faults and statistics of percent detection. The CON_A6.DTB digital test binary pattern file created from the LASAR simulation is preceded by a manually-generated pattern file CON_A6_Init.DTB. This file initializes the U53 flip-flop and U15 binary counter to create a U26 PROM address of 1. Force/release statements are used to initialize U15 to the same state in the simulation at the pattern at which U53 becomes known as a result of input stimulus used in the simulation. The LASAR Judge listing states that the highest detecting pattern is about 8,000 out of 16,000. However, all 16,000 patterns are needed to test all PROM data locations of U26. PROM data elements are not fault-simulated.

Step 101 LASAR Digital Test

Test step 101 verifies the functionality of most of the UUT by connecting the input and output pins to digital channels and running the digital test file CON_A6.DTB. One connection made, DTS Channel 17 to P1-10, is connected via A1K1. This is a relay that is Normally Closed (N.C.) and provides a direct connection when A1K1 is not energized. The test should pass without any errors.

Connection Path as follows:



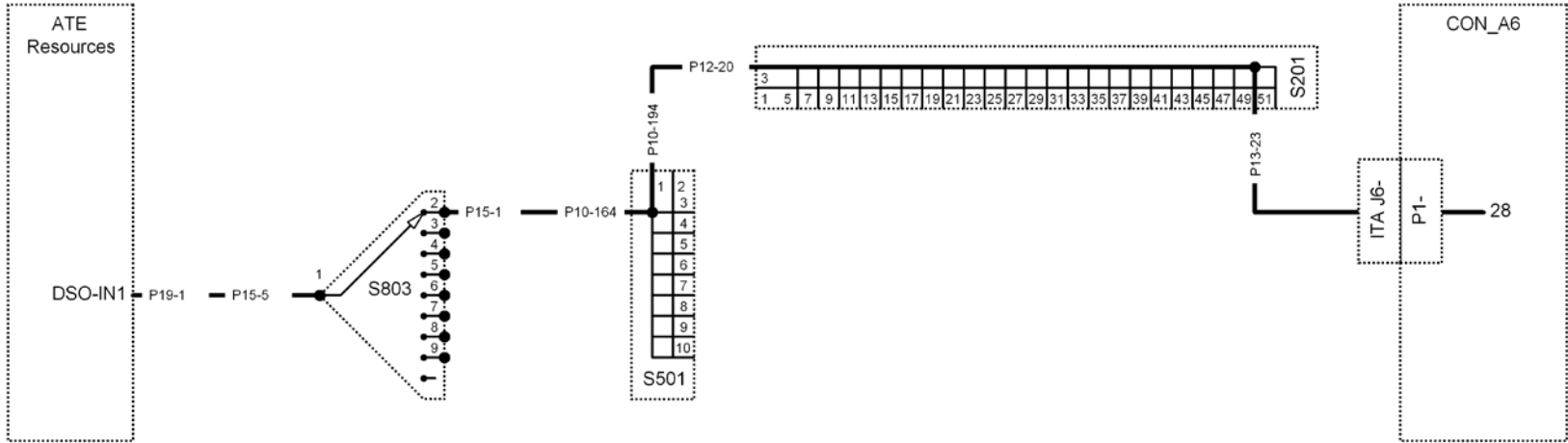
MODULE 2 OSCILLATOR AND TONE RETURN TESTS

Module 2 verifies the functionality of the Y1 oscillator and the R8/R9 Tone Return voltage divider resistors.

Step 201 Oscillator Amplitude Test

Test Step 201 verifies the P-P amplitude of the Y1 oscillator TTL output signal by using the DSO to measure the voltage peak-to-peak between P1-28 and GND. The voltage should be more than 0.035 Vpp.

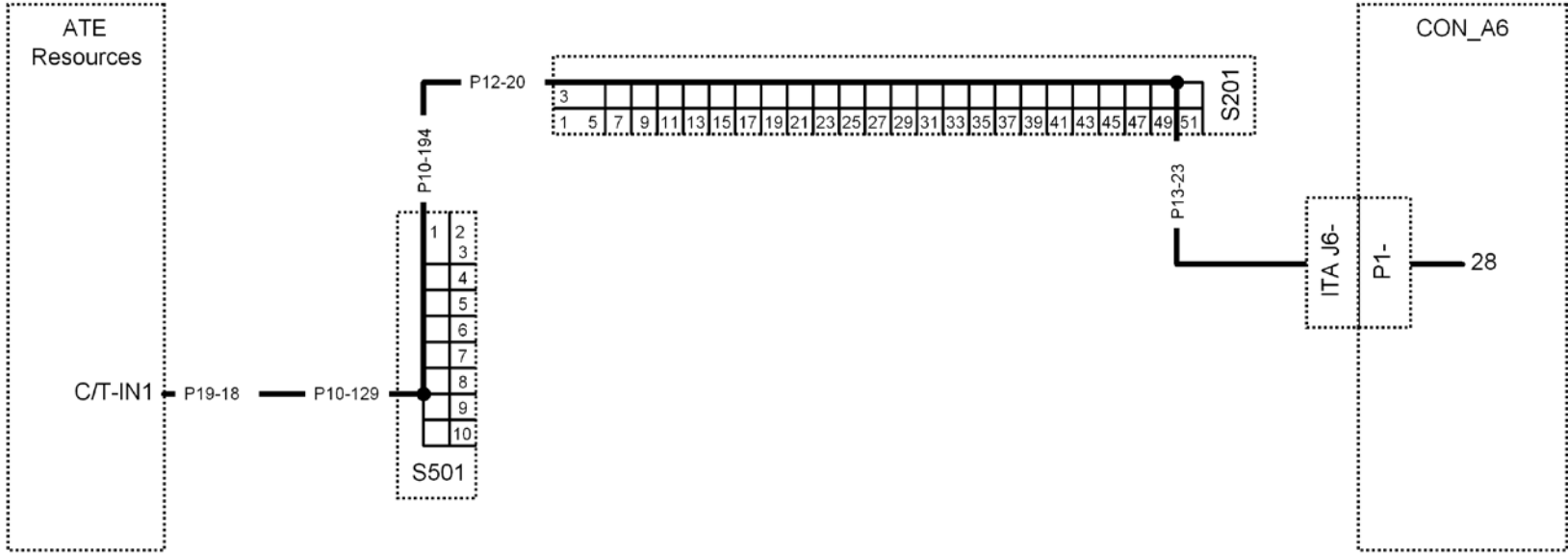
Connection Path as follows:



Step 202 Oscillator Frequency Test

Test Step 202 verifies the frequency of the Y1 oscillator 16.384 MHz output signal by using the C/T to measure the frequency between P1-28 and GND. The frequency should be between 16389980 Hz and 16378020 Hz.

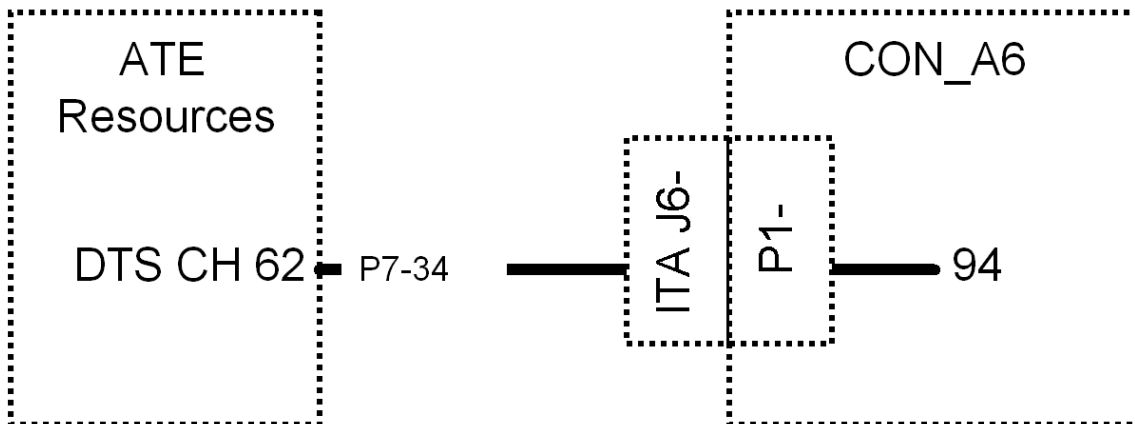
Connection Path as follows:



Step 203 Tone Return Output LO Test

Test Step 203 verifies that the 2.5 Vdc level on the Tone Return output is greater than 2Vdc by using ATLAS Digital. This is done by testing for a logical high with DTS channel 62 connected to P1-94 with the threshold set at 2.0 Vdc.

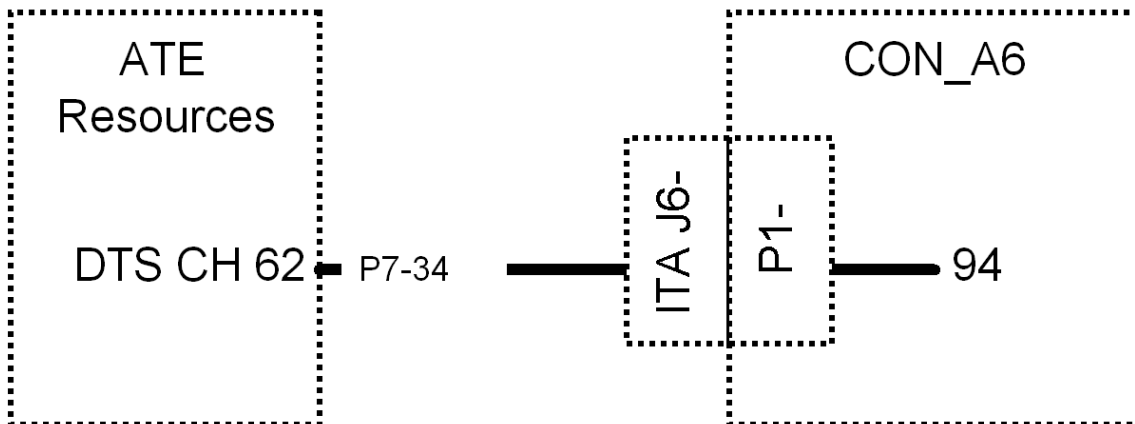
Connection Path as follows:



Step 204 Tone Return Output HI Test

Test Step 204 verifies that the 2.5 Vdc level on the Tone Return output is less than 3Vdc by using ATLAS Digital. This is done by testing for a logical low with DTS channel 62 connected to P1-94 with the threshold set at 3.0 Vdc.

Connection Path as follows:



FUNCTIONAL FLOW CHART (FCC)

