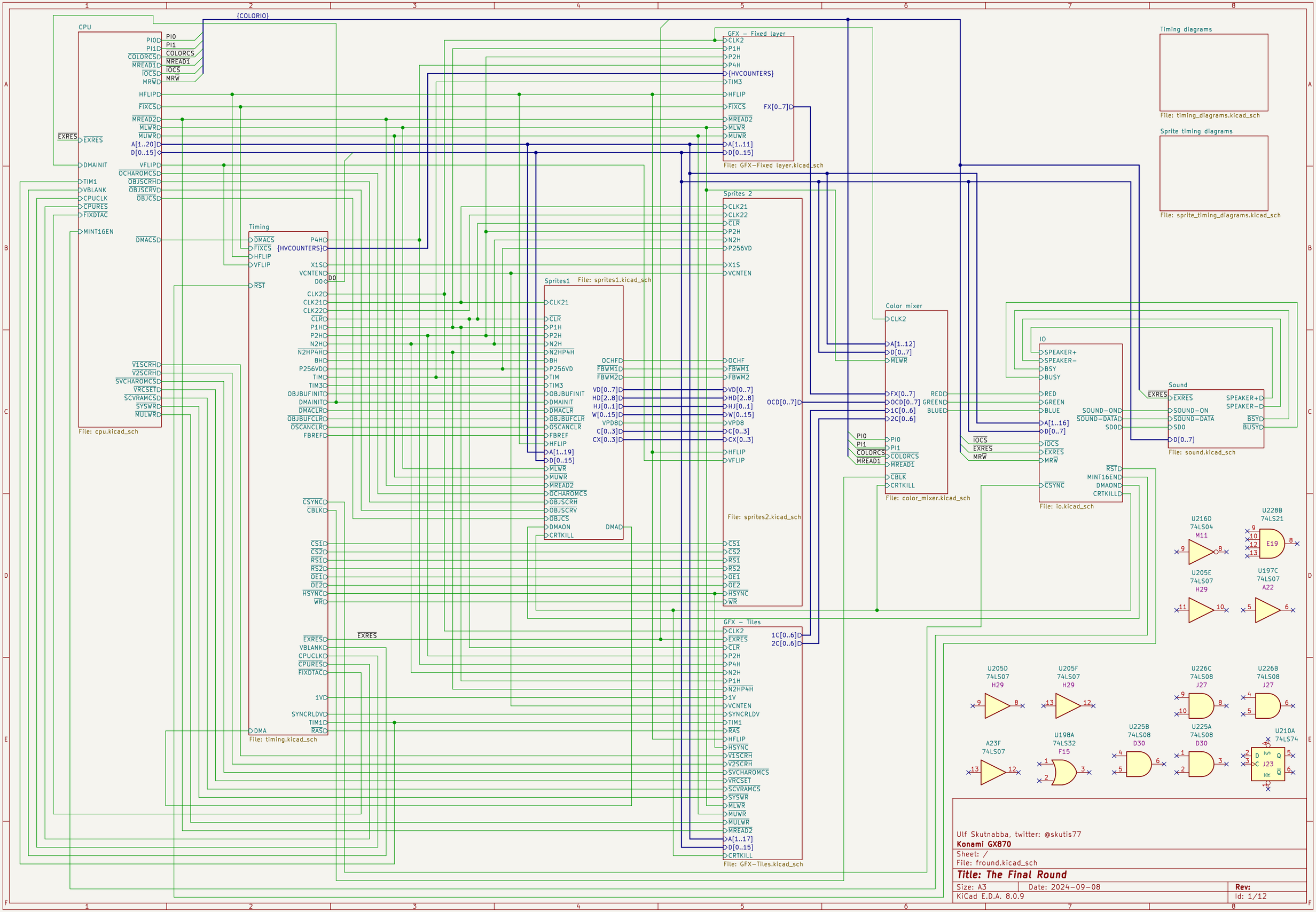
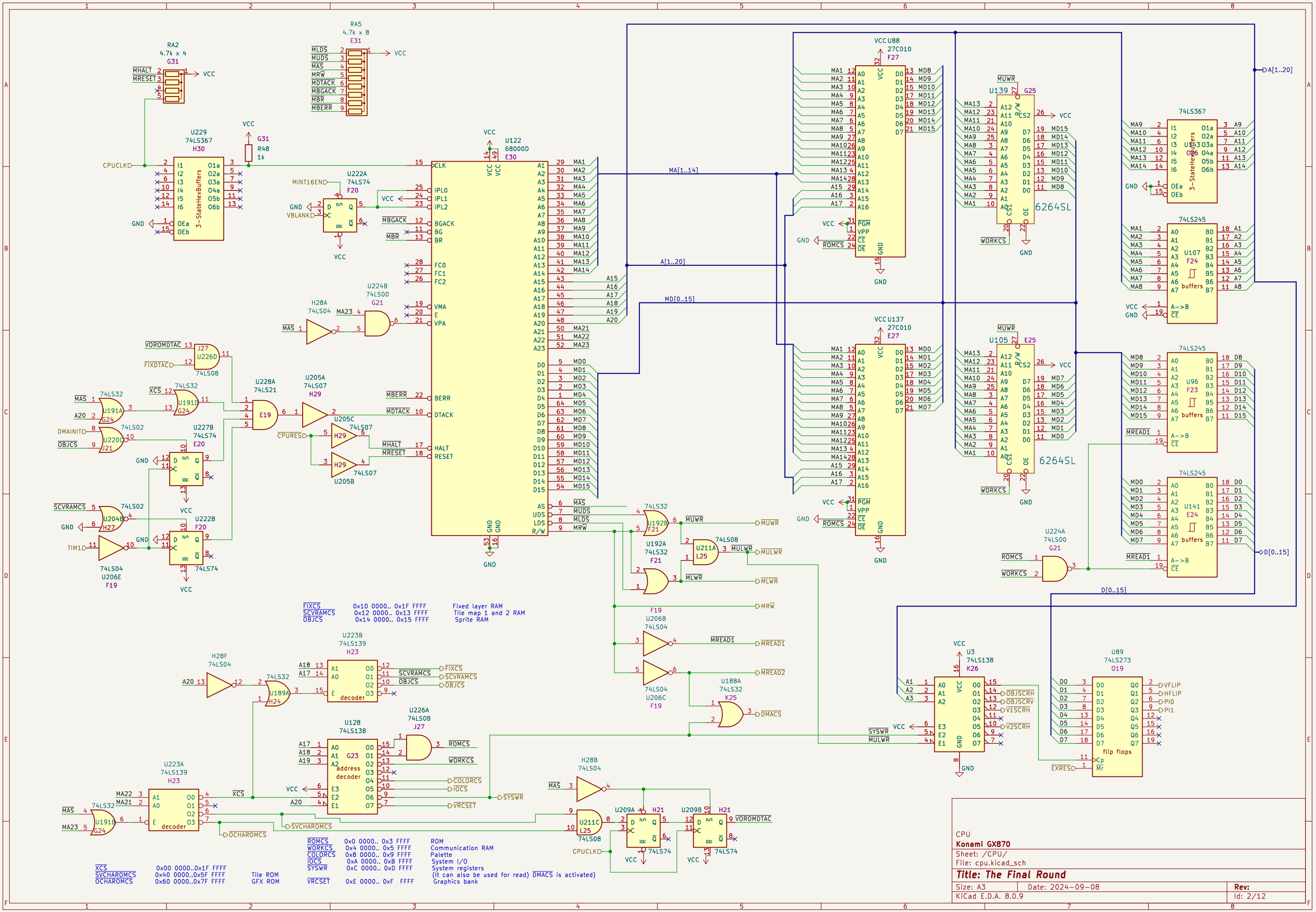
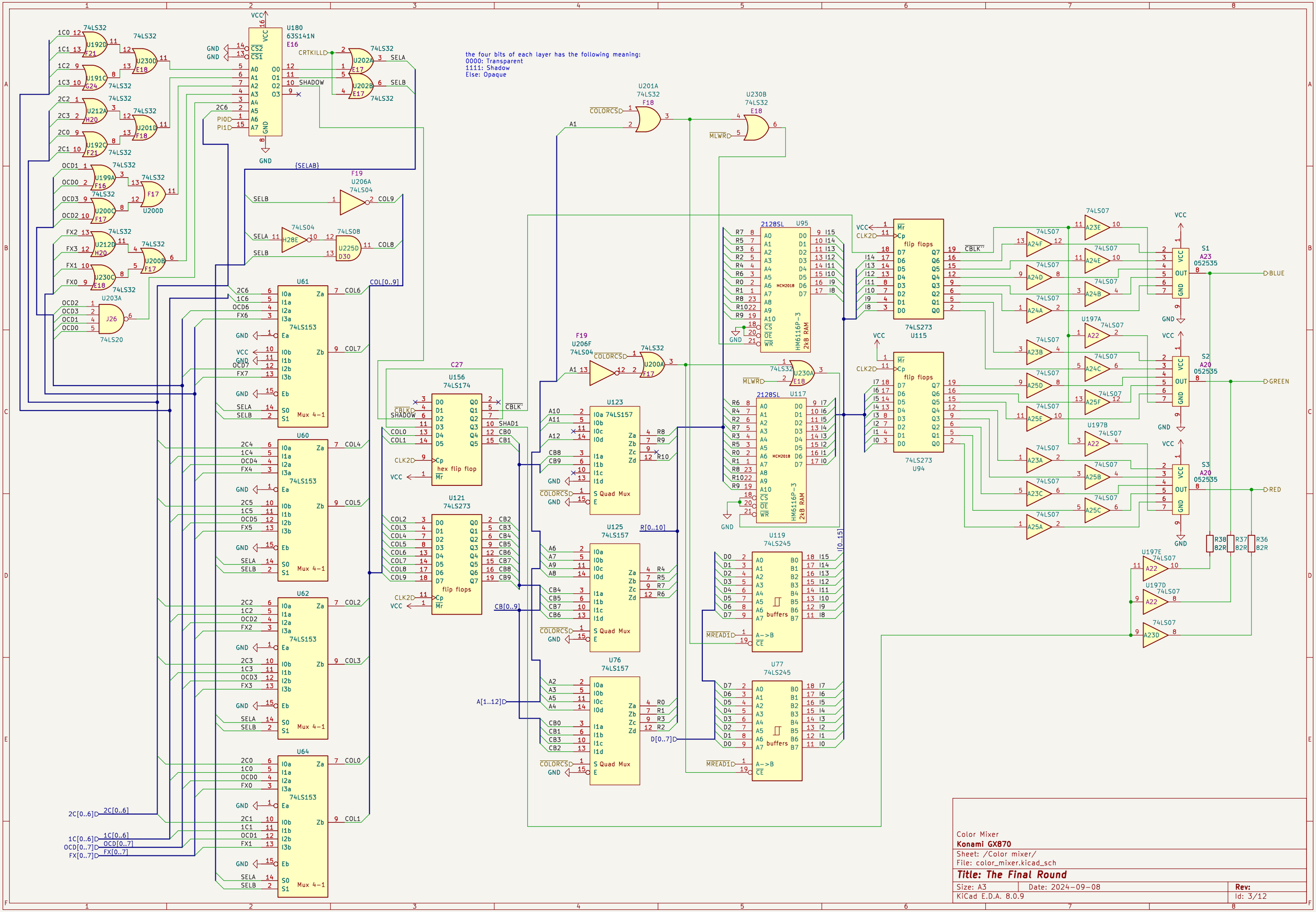

CPU
File: cpu.kicad_sch
Timing
File: timing.kicad_sch
Sprites1
File: sprites1.kicad_sch
Sprites 2
File: sprites2.kicad_sch
GFX – Fixed layer
File: GFX–Fixed layer.kicad_sch
GFX – Tiles
File: GFX–Tiles.kicad_sch
Color mixer
File: color_mixer.kicad_sch
IO
File: io.kicad_sch
Sound
File: sound.kicad_sch
Timing diagrams
File: timing_diagrams.kicad_sch
Sprite timing diagrams
File: sprite_timing_diagrams.kicad_sch
U216D 74LS04 M11
U228B 74LS21 E19
U205E 74LS07 H29
U197C 74LS07 A22
U205D 74LS07 H29
U205F 74LS07 H29
U226C 74LS08 J27
U226B 74LS08 J27
A23F 74LS07
U198A 74LS32 F15
U225B 74LS08 D30
U225A 74LS08 D30
U210A 74LS74 J23
Ulf Skutnabba, twitter: @skutis77
Konami GX870
Sheet: /
File: fround.kicad_sch
Title: The Final Round
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 1/12



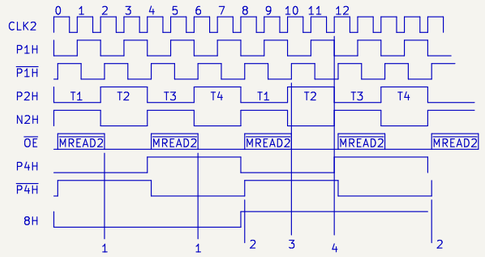

CPU
**Konami GX870**
Sheet: /CPU/
File: cpu.kicad_sch

***Title: The Final Round***

| | | |
|---|---|---|
| Size: A3 | Date: 2024-09-08 | Rev: |
| KiCad E.D.A. 8.0.9 | | Id: 2/12 |


the four bits of each layer has the following meaning:
0000: Transparent
1111: Shadow
Else: Opaque
U180
63S141N
E16
U61
74LS153
U60
74LS153
U62
74LS153
U64
74LS153
Mux 4-1
U156
74LS174
hex flip flop
U121
74LS273
flip flops
U123
74LS157
S Quad Mux
U125
74LS157
U76
74LS157
U95
2128SL
HM6116P-3
2kB RAM
U117
2128SL
U115
74LS273
U94
74LS273
U119
74LS245
U77
74LS245
buffers
U201A
74LS32
F18
U230B
74LS32
E18
U206A
74LS04
F19
U206F
74LS04
U200A
F17
U230A
E18
U197A
U197B
U197E
U197D
S1
A23
052535
S2
A20
052535
S3
A20
052535
BLUE
GREEN
RED
R38
82R
R37
82R
R36
82R
Color Mixer
Konami GX870
Sheet: /Color mixer/
File: color_mixer.kicad_sch
Title: The Final Round
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 3/12

CLK2: 6.1397MHz
1V: 8.00kHz
2V: 4.00kHz
4V: 2.000kHz
P1H: 3.0719MHz
P2H: 1.536MHz
P4H: 0.767971MHz
8H: 384.000kHz
16H: 192.000kHz




RAM Control

| Slot | Control |
|---|---|
| T1,T3 | CPU |
| T2,T4 | Video circuit |

| Time | |
|---|---|
| 1 | Data output from RAM to Video circuit |
| 2 | Data latched into first DFF's |
| 3 | Data latched into second DFF's. |
| 4 | Pixel data output to FX[0..7] |

The delay from the LSB (8H) of the RAM accessed by the video circuit is six pixels to output.

8-bits of data is latched every $\overline{P4H}$ cycle.
It is 2 pixels = 8bits / (4 bits / pixel).
The current pixel is multiplexed with $\overline{P1H}$ (also HFLIP).

B0 goes to pin 36 on timing circuit

Kolla 8V och 256H

When P2H is high I1 is selected.

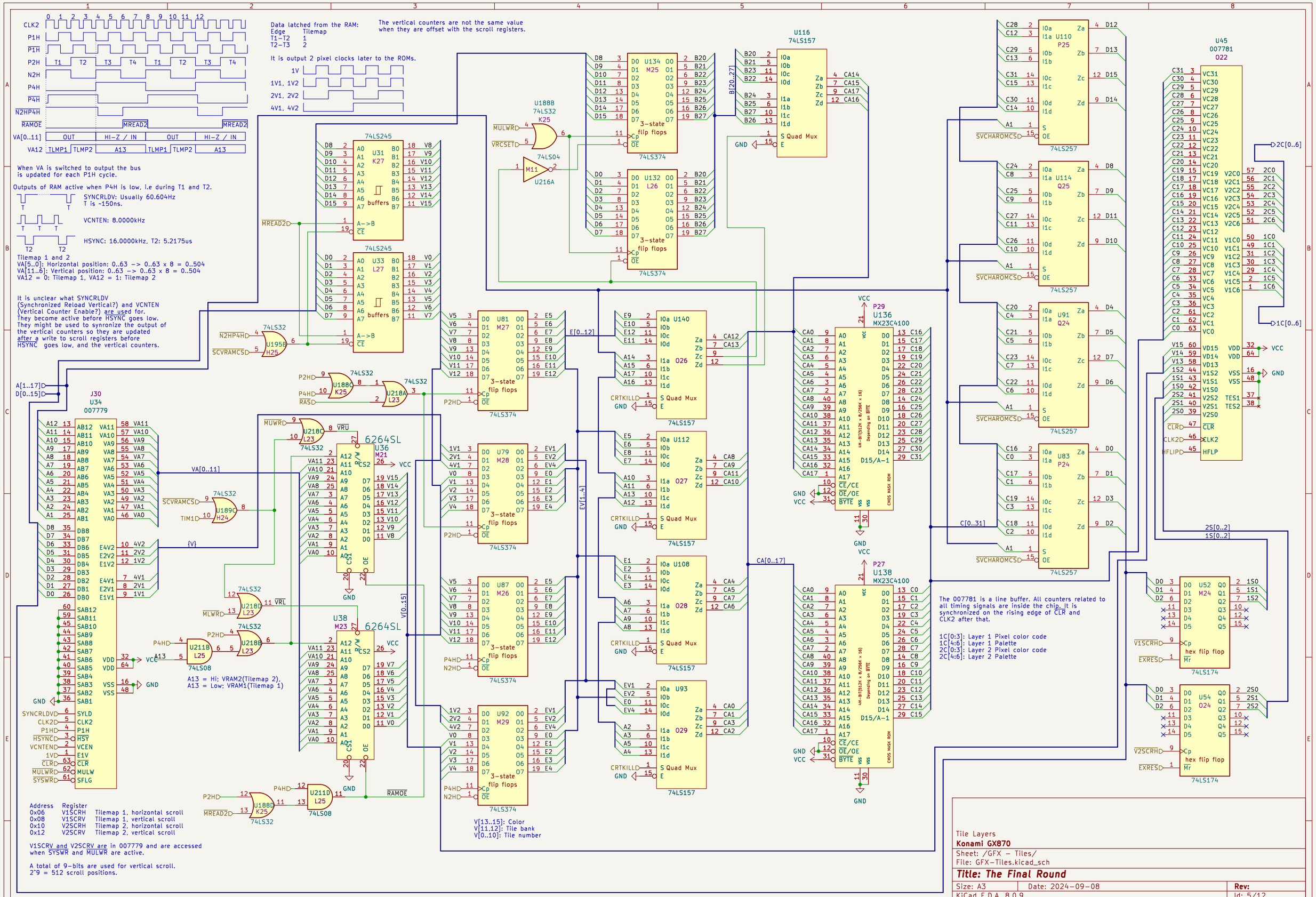
FXD[0..8]: Tile number
FXD[9..12]: Palette color
FXD[13]: HFLIP, not used on Final round
FXD[14]: VFLIP, not used on Final round

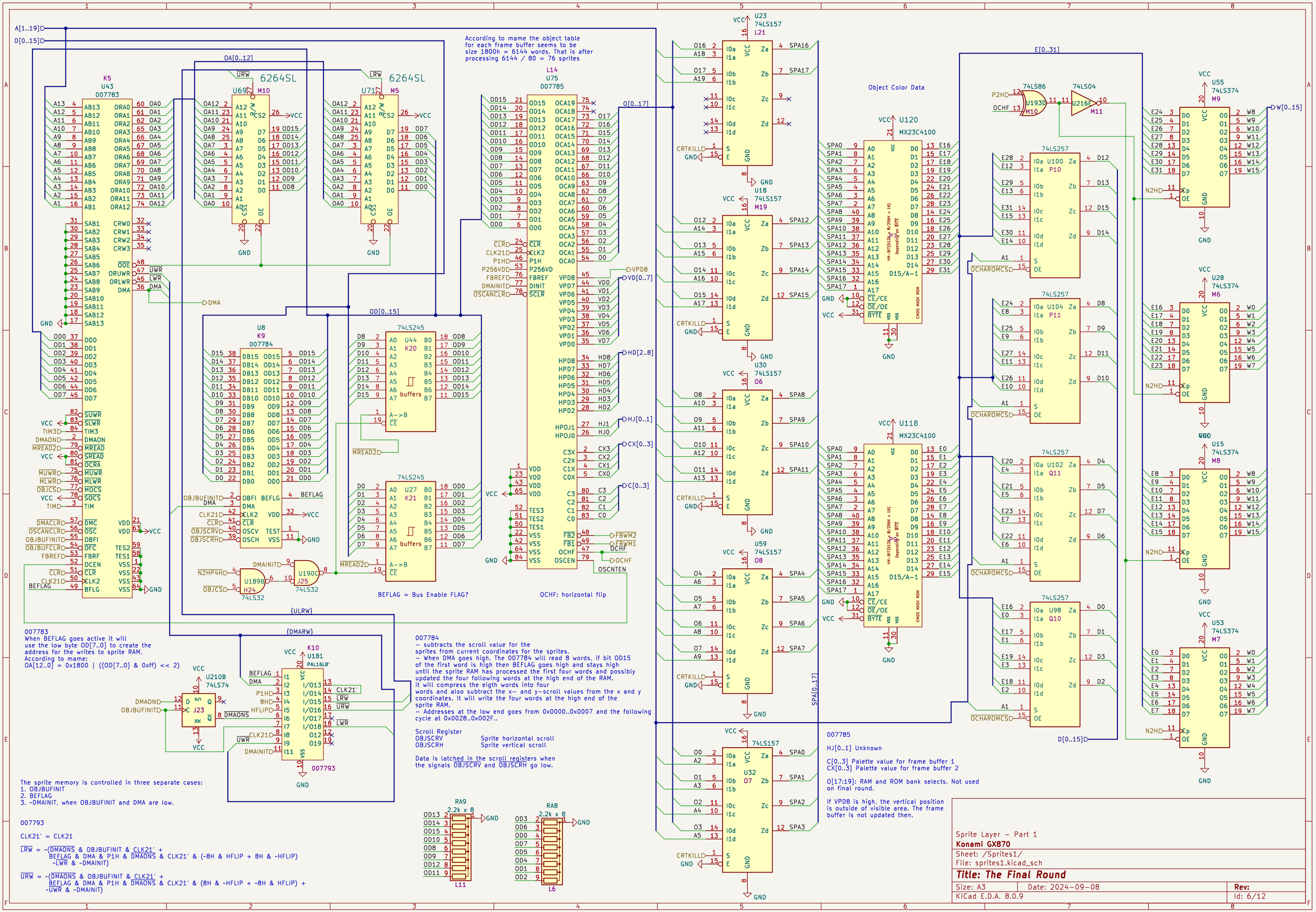
RAM
A[0..5] Horizontal position 0..511
A[6..10] Vertical position 0..255 in steps of 8
A[11.12] Tilemaps? Up to 4.

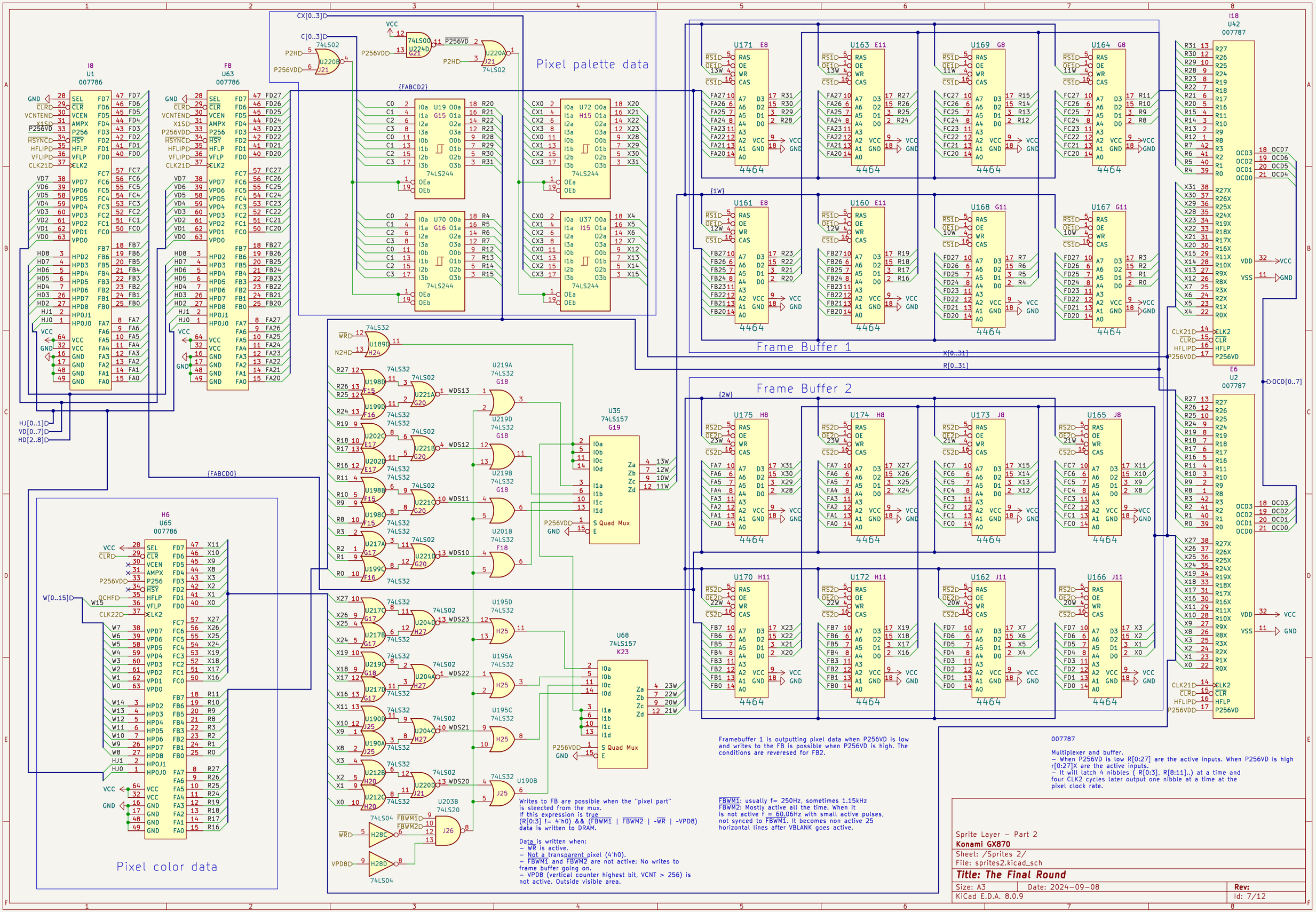
Fixed Layer
**Konami GX870**
Sheet: /GFX - Fixed layer/
File: GFX-Fixed layer.kicad_sch

***Title: The Final Round***

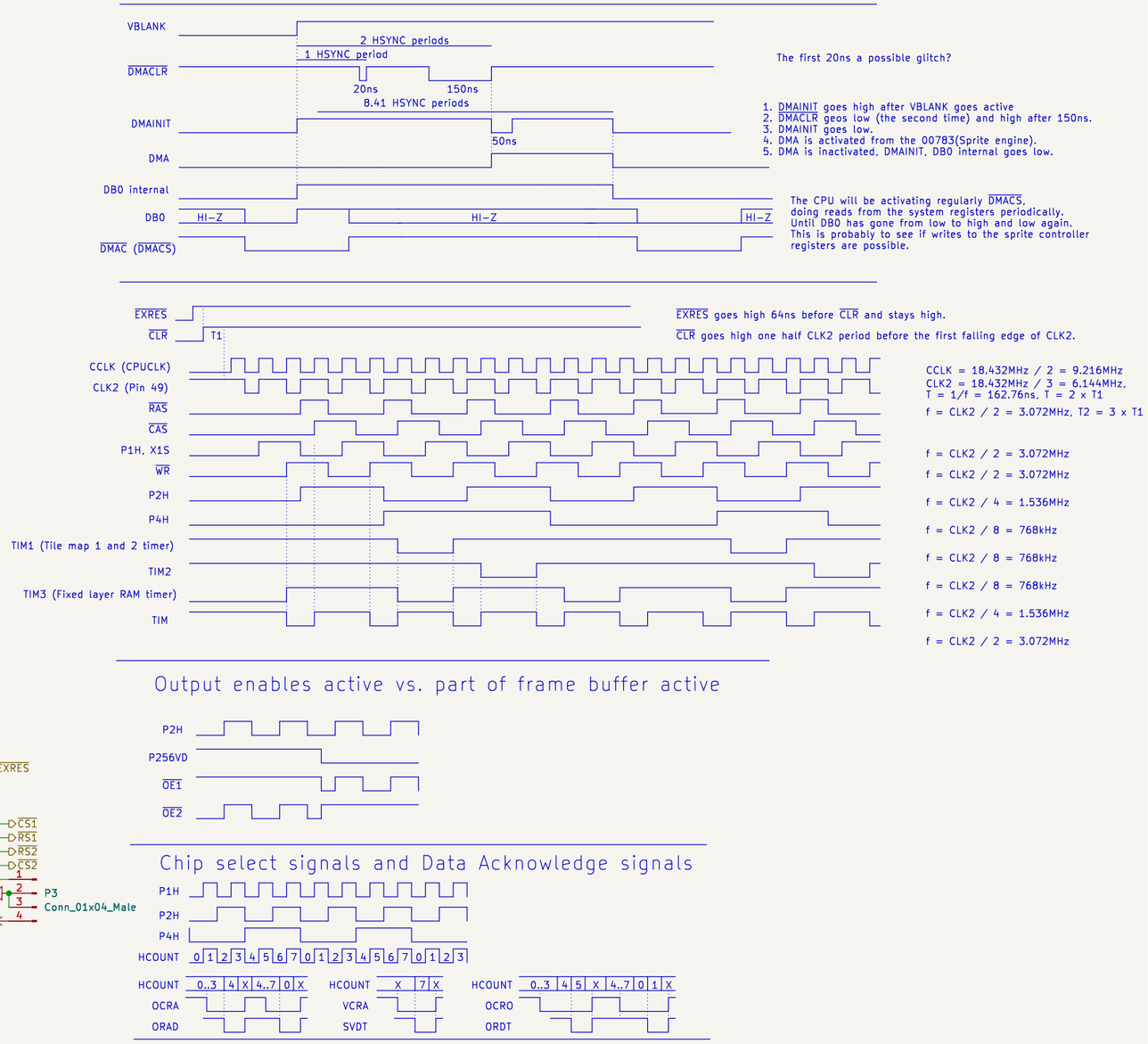
| Size: A3 | Date: 2024-09-08 | **Rev:** |
|---|---|---|
| KiCad E.D.A. 8.0.9 | | Id: 4/12 |


CLK2
P1H
P2H
N2H
P4H
N2HP4H
RAMOE
VA[0..11]
VA12
OUT
HI-Z / IN
MREAD2
TLMP1
TLMP2
A13
Data latched from the RAM:
Edge Tilemap
T1-T2 1
T2-T3 2
It is output 2 pixel clocks later to the ROMs.
1V
1V1, 1V2
2V1, 2V2
4V1, 4V2
The vertical counters are not the same value when they are offset with the scroll registers.
When VA is switched to output the bus is updated for each P1H cycle.
Outputs of RAM active when P4H is low, i.e during T1 and T2.
SYNCRLDV: Usually 60.604Hz T is ~150ns.
VCNTEN: 8.0000kHz
HSYNC: 16.0000kHz, T2: 5.2175us
Tilemap 1 and 2
VA[5..0]: Horizontal position: 0..63 -> 0..63 x 8 = 0..504
VA[11..6]: Vertical position: 0..63 -> 0..63 x 8 = 0..504
VA12 = 0: Tilemap 1, VA12 = 1: Tilemap 2
It is unclear what SYNCRLDV (Synchronized Reload Vertical?) and VCNTEN (Vertical Counter Enable?) are used for. They become active before HSYNC goes low. They might be used to synronize the output of the vertical counters so they are updated after a write to scroll registers before HSYNC goes low, and the vertical counters.
74LS245
U31 K27
U33 L27
buffers
A->B
CE
74LS374
3-state flip flops
U116
74LS157
S Quad Mux
U188B
74LS32
K25
74LS04
U216A
U34
007779
6264SL
U36 M21
U38 M23
74LS08
74LS174
U45
007781
O22
P29
U136
MX23C4100
P27
U138
MX23C4100
14M-BIT(512K x 8/256K x 16)
Depending on BYTE
D15/A-1
CMOS MASK ROM
74LS257
U110 P25
U114 Q25
U91 Q24
U83 P24
U52 M24
U54 O24
U140 O26
U112 O27
U108 O28
U93 O29
U132 L26
U134 M25
U81 M27
U79 M28
U87 M26
U92 M29
A[1..17]
D[0..15]
VA[0..11]
{V}
V[0..15]
E[0..12]
EV[1..4]
CA[0..17]
B[20..27]
C[0..31]
2C[0..6]
1C[0..6]
2S[0..2]
1S[0..2]
VCC
GND
A13 = Hi; VRAM2(Tilemap 2).
A13 = Low; VRAM1(Tilemap 1)
Address Register
0x06 V1SCRH Tilemap 1, horizontal scroll
0x08 V1SCRV Tilemap 1, vertical scroll
0x10 V2SCRH Tilemap 2, horizontal scroll
0x12 V2SCRV Tilemap 2, vertical scroll
V1SCRV and V2SCRV are in 007779 and are accessed when SYSWR and MULWR are active.
A total of 9-bits are used for vertical scroll.
2^9 = 512 scroll positions.
V[13..15]: Color
V[11,12]: Tile bank
V[0..10]: Tile number
The 007781 is a line buffer. All counters related to all timing signals are inside the chip. It is synchronized on the rising edge of CLR and CLK2 after that.
1C[0:3]: Layer 1 Pixel color code
1C[4:6]: Layer 1 Palette
2C[0:3]: Layer 2 Pixel color code
2C[4:6]: Layer 2 Palette
Tile Layers
Konami GX870
Sheet: /GFX - Tiles/
File: GFX-Tiles.kicad_sch
Title: The Final Round
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 5/12


A[1..19]
D[0..15]
K5
U43
007783
6264SL
U69
M10
U71
M5
OA[0..12]
According to mame the object table
for each frame buffer seems to be
size 1800h = 6144 words. That is after
processing 6144 / 80 = 76 sprites
L14
U75
007785
U23
74LS157
L21
U18
M19
U30
O6
U59
O8
U32
O7
Object Color Data
U120
MX23C4100
U118
MX23C4100
E[0..31]
74LS86
U193D
M10
74LS04
U216E
M11
74LS257
U100
P10
U104
P11
U102
Q11
U98
Q10
U55
74LS374
M9
U28
M6
U15
M8
U53
M7
W[0..15]
D[0..15]
U8
K9
007784
74LS245
U44
K20
U27
K21
buffers
OD[0..15]
U189B
H24
74LS32
U190C
J25
74LS32
BEFLAG = Bus Enable FLAG?
OCHF: horizontal flip
{ULRW}
{DMARW}
K10
U181
PAL16L8'
007793
U210B
74LS74
J23
007783
When BEFLAG goes active it will
use the low byte OD[7..0] to create the
address for the writes to sprite RAM.
According to mame:
OA[12..0] = 0x1800 | ((OD[7..0] & 0xff) << 2)
007784
– subtracts the scroll value for the
sprites from current coordinates for the sprites.
– When DMA goes high. The 007784 will read 8 words, if bit OD15
of the first word is high then BEFLAG goes high and stays high
until the sprite RAM has processed the first four words and possibly
updated the four following words at the high end of the RAM.
it will compress the eigth words into four
words and also subtract the x– and y–scroll values from the x and y
coordinates. It will write the four words at the high end of the
sprite RAM.
– Addresses at the low end goes from 0x0000..0x0007 and the following
cycle at 0x0028..0x002F..
Scroll Register
OBJSCRV Sprite horizontal scroll
OBJSCRH Sprite vertical scroll
Data is latched in the scroll registers when
the signals OBJSCRV and OBJSCRH go low.
The sprite memory is controlled in three separate cases:
1. OBJBUFINIT
2. BEFLAG
3. ~DMAINIT, when OBJBUFINIT and DMA are low.
007793
CLK21′ = CLK21
LRW = ~(DMAONS & OBJBUFINIT & CLK21′ +
BEFLAG & DMA & P1H & DMAONS & CLK21′ & (~8H & HFLIP + 8H & ~HFLIP)
~LWR & ~DMAINIT)
URW = ~(DMAONS & OBJBUFINIT & CLK21′ +
BEFLAG & DMA & P1H & DMAONS & CLK21′ & (8H & ~HFLIP + ~8H & HFLIP) +
~UWR & ~DMAINIT)
RA9
2.2k x 8
L11
RA8
2.2k x 8
L6
007785
HJ[0..1] Unknown
C[0..3] Palette value for frame buffer 1
CX[0..3] Palette value for frame buffer 2
O[17:19]: RAM and ROM bank selects. Not used
on final round.
If VPD8 is high, the vertical position
is outside of visible area. The frame
buffer is not updated then.
Sprite Layer – Part 1
Konami GX870
Sheet: /Sprites1/
File: sprites1.kicad_sch
Title: The Final Round
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 6/12


Pixel palette data
Frame Buffer 1
Frame Buffer 2
Pixel color data
I8 U1 007786
F8 U63 007786
H6 U65 007786
I18 U42 007787
E6 U2 007787
U35 74LS157 G19
U68 74LS157 K23
Writes to FB are possible when the "pixel part" is sleected from the mux.
If this expression is true
(R[0:3] != 4'h0) && (FBWM1 | FBWM2 | ~WR | ~VPD8)
data is written to DRAM.
Data is written when:
– WR is active.
– Not a transparent pixel (4'h0).
– FBWM1 and FBWM2 are not active: No writes to frame buffer going on.
– VPD8 (vertical counter highest bit, VCNT > 256) is not active. Outside visible area.
Framebuffer 1 is outputting pixel data when P256VD is low and writes to the FB is possible when P256VD is high. The conditions are reveresed for FB2.
FBWM1: usually f= 250Hz, sometimes 1.15kHz
FBWM2: Mostly active all the time. When it is not active f = 60.06Hz with small active pulses, not synced to FBWM1. It becomes non active 25 horizontal lines after VBLANK goes active.
007787
Multiplexer and buffer.
– When P256VD is low R[0:27] are the active inputs. When P256VD is high r[0:27]X are the active inputs.
– It will latch 4 nibbles ( R[0:3], R[8:11]..) at a time and four CLK2 cycles later output one nibble at a time at the pixel clock rate.
Sprite Layer – Part 2
Konami GX870
Sheet: /Sprites 2/
File: sprites2.kicad_sch
Title: The Final Round
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 7/12

# DMA Synchronization

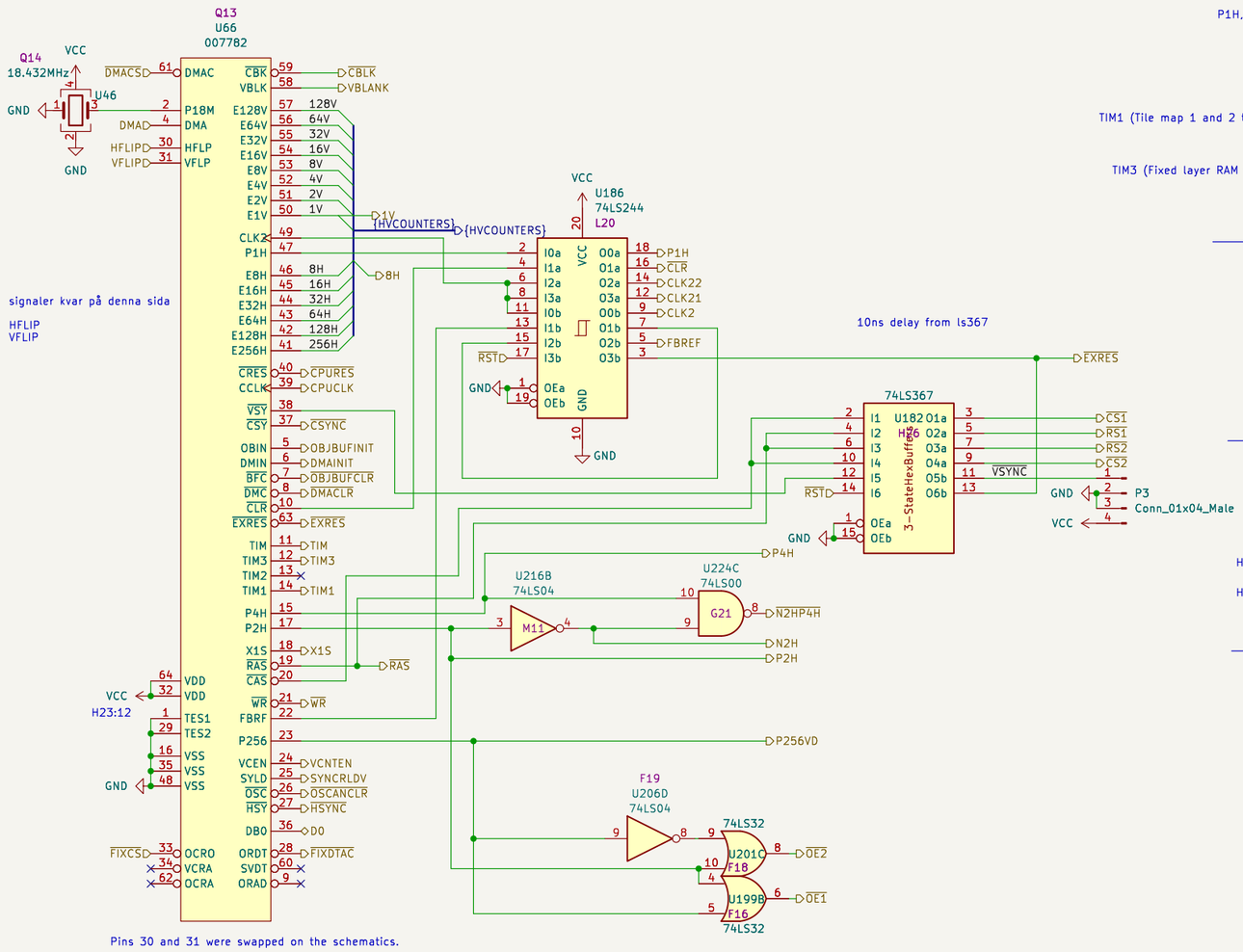



## Output enables active vs. part of frame buffer active

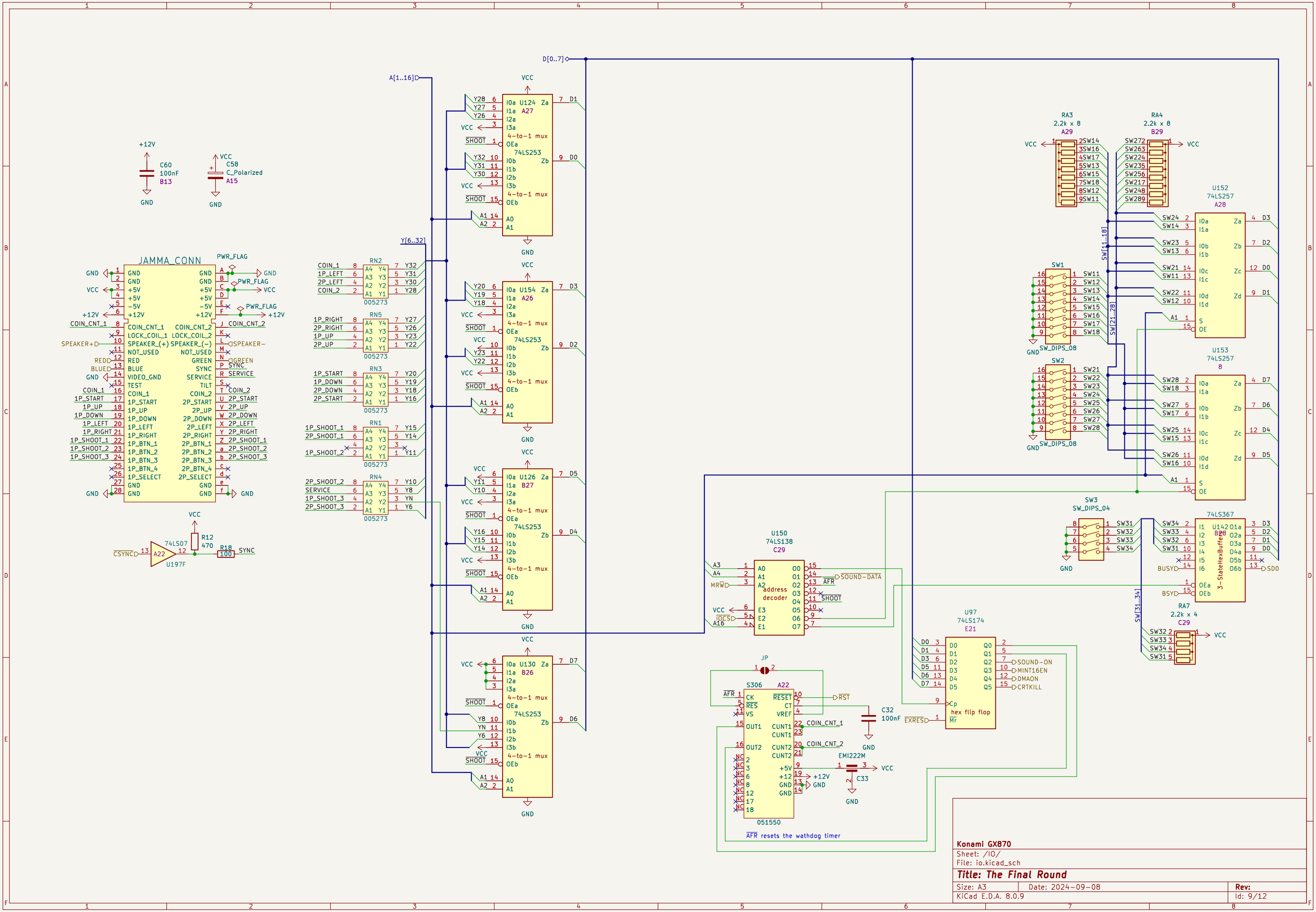


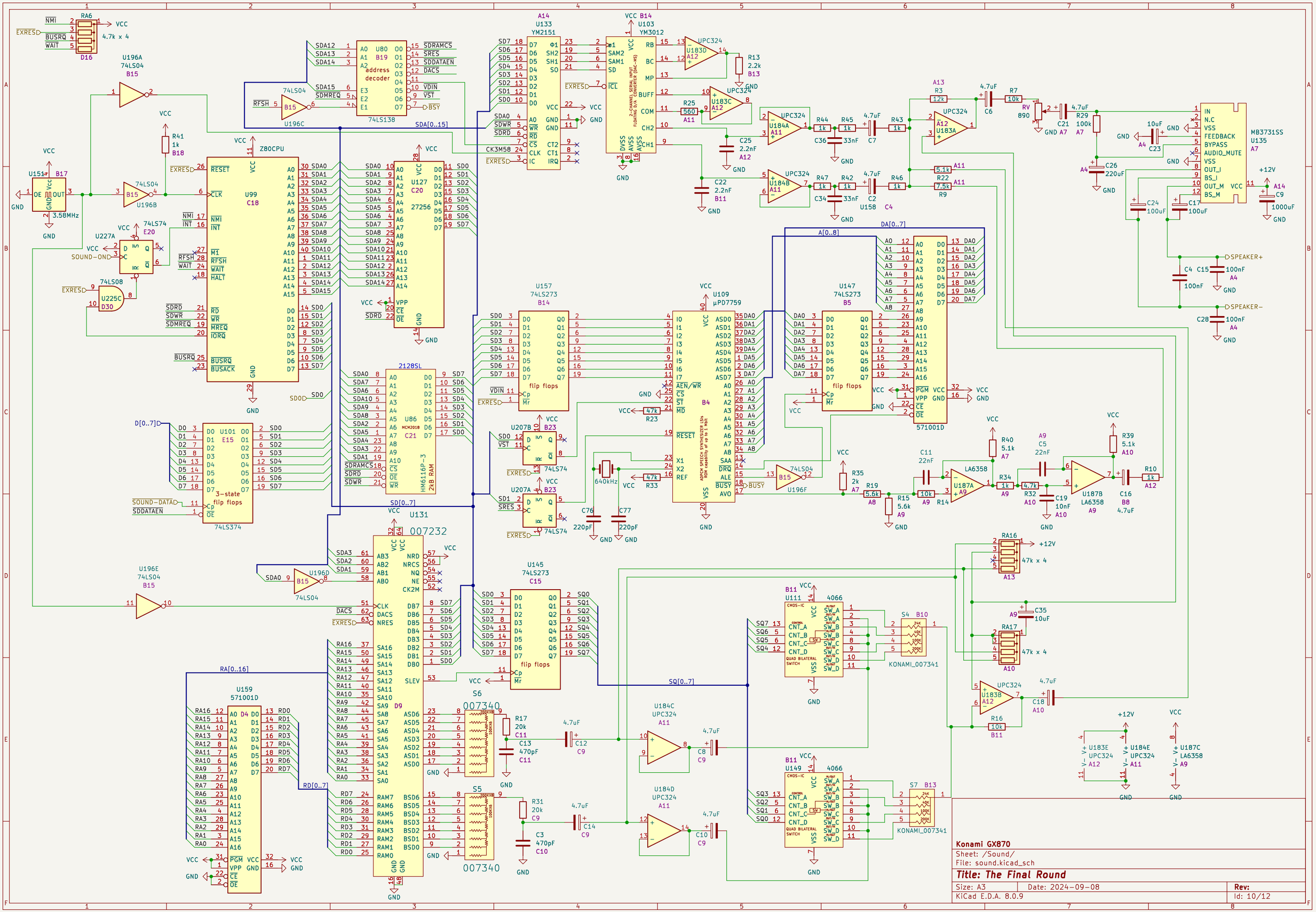

## Chip select signals and Data Acknowledge signals




| | | |
|---|---|---|
| Timing<br>**Konami GX870** | | |
| Sheet: /Timing/<br>File: timing.kicad_sch | | |
| ***Title: The Final Round*** | | |
| Size: A3 | Date: 2024-09-08 | **Rev:** |
| KiCad E.D.A. 8.0.9 | | Id: 8/12 |


JAMMA_CONN
PWR_FLAG
GND
VCC
+12V
C60
100nF
B13
C58
C_Polarized
A15
D[0..7]
A[1..16]
Y[6..32]
U124 Za
A27
74LS253
4-to-1 mux
U126 Za
B27
U154 Za
A26
U130 Za
B26
RN2
RN3
RN4
RN5
RN1
005273
SHOOT
COIN_1
1P_LEFT
2P_LEFT
COIN_2
1P_RIGHT
2P_RIGHT
1P_UP
2P_UP
1P_START
1P_DOWN
2P_DOWN
2P_START
1P_SHOOT_1
2P_SHOOT_1
1P_SHOOT_2
2P_SHOOT_2
SERVICE
1P_SHOOT_3
2P_SHOOT_3
SPEAKER+
SPEAKER-
REDD
BLUED
GREEN
SYNC
COIN_CNT_1
COIN_CNT_2
CSYNC
U197F
74LS07
R12
470
R18
100
U150
74LS138
C29
address decoder
MRW
IOCS
A16
SOUND-DATA
AFR
U97
74LS174
E21
hex flip flop
EXRES
SOUND-ON
MINT16EN
DMAON
CRTKILL
JP
S306
A22
051550
RESET
VREF
OUT1
OUT2
CUNT1
CUNT2
RST
C32
100nF
EMI222M
C33
AFR resets the wathdog timer
RA3
2.2k x 8
A29
RA4
2.2k x 8
B29
SW1
SW2
SW3
SW_DIPS_08
SW_DIPS_04
SW[11..18]
SW[21..28]
SW[31..34]
U152
74LS257
A28
U153
74LS257
B28
74LS367
U142
3-StateHexBuffer
BUSYD
BSYD
SDO
RA7
2.2k x 4
C29
Konami GX870
Sheet: /IO/
File: io.kicad_sch
Title: The Final Round
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 9/12




**Konami GX870**

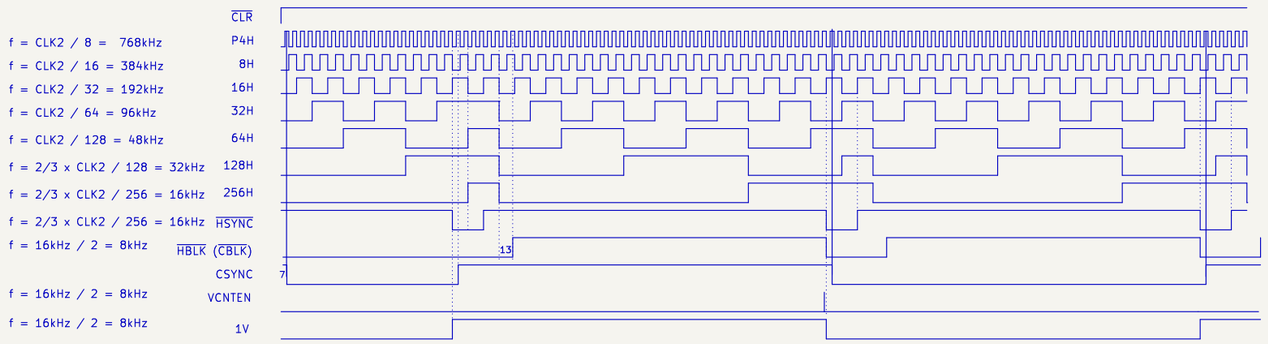
Sheet: /Sound/

File: sound.kicad_sch

**Title: The Final Round**

| Size: A3 | Date: 2024-09-08 | Rev: |
|---|---|---|
| KiCad E.D.A. 8.0.9 | | Id: 10/12 |

# Horizontal signals

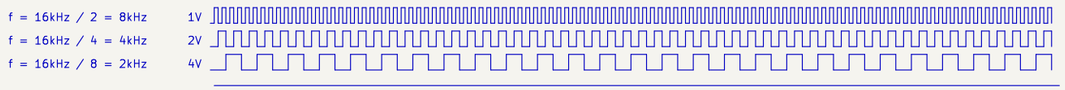


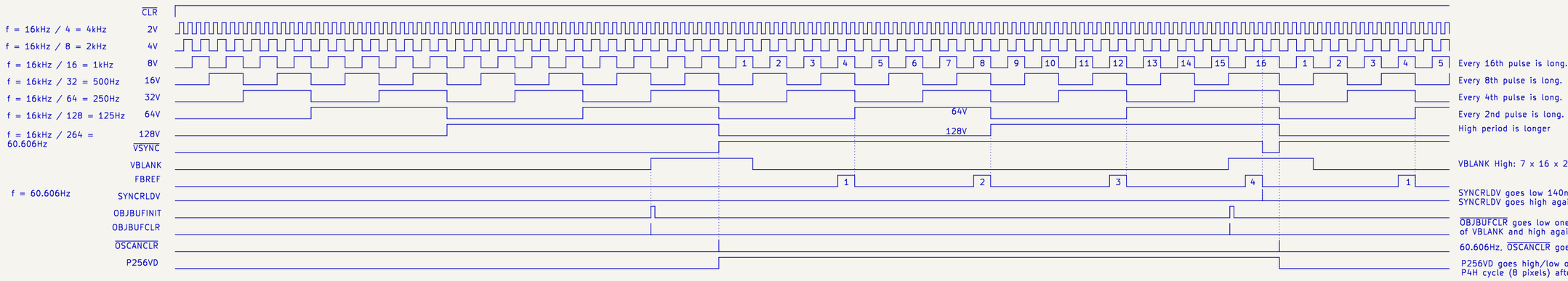

– The first VCNTEN is skipped after reset.
It goes low 140ns before HSYNC goes low,
and high again when HSYNC goes low.
VCNTEN is active right before every second falling edge of HSYNC.

– CPURES goes high, and stays high, on the seventh falling edge of HSYNC.

The first HSYNC is at HCOUNT 175 after reset.

# Vertical signals




FBREF is measured at pin 22. At U186:3 FBREF is delayed by 22ns going high and 12ns going low.

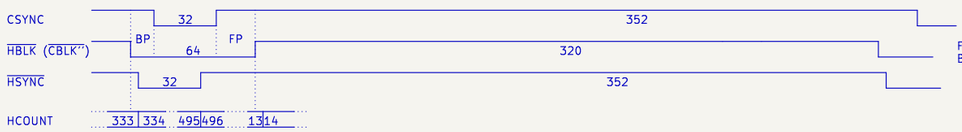
# Horizontal and vertical synch timing diagrams

Pixel clock CLK2 = 18.432MHz / 3 = 6.144MHz

Horizontal lines
HSYNC freq = 6.144MHz / 384 = 16kHz
HSYNC period = 1 / 16kHz = 62.5us
Pixels / line: 384
Active pixels: 320
Blank pixels: 64

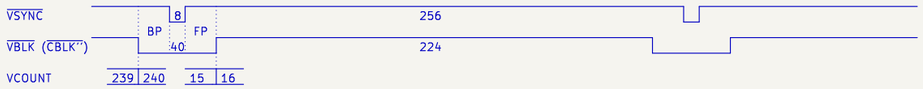
Vertical lines
VSYNC freq = 16kHz / 264 = 60.606060Hz
VSYNC period = 1 / f = 264 / 16kHz = 16.5ms
scanlines / frame: 264
Active lines: 224
Blank lines: 40

The numbers in the HSYNC and HBLK diagrams are HSYNC cycles.
All edges are synchronised to the rising edge of CLK2.




Front Porch (FP) 24 px,
Back Porch (BP) 8 px

The numbers in the VSYNC and VBLK diagrams are HSYNC cycles.
All edges are synchronised to the falling edge of HSYNC.

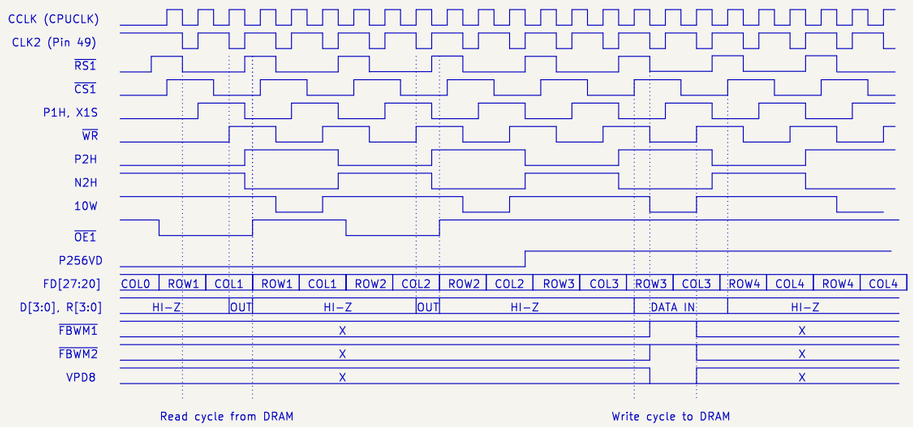



Front Porch (FP) and
Back Porch (BP) 16 HSYNC cycles.

HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]
VCOUNT is bits [128V, 64V, 32V, 16V, 8V, 4V, 2V, 1V]

CBLK'' is at the output of color mixer.

| | | |
|---|---|---|
| **Konami GX870** | | |
| Sheet: /Timing diagrams/ | | |
| File: timing_diagrams.kicad_sch | | |
| ***Title: The Final Round*** | | |
| Size: A3 | Date: 2024-09-08 | **Rev:** |
| KiCad E.D.A. 8.0.9 | | Id: 11/12 |




The same row and column addresses are repeated twice.
One for read cycle and the other for write cycles.

**Konami GX870**

Sheet: /Sprite timing diagrams/
File: sprite_timing_diagrams.kicad_sch

***Title: The Final Round***

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|---|---|---|
| Size: A3 | Date: 2024-09-08 | **Rev:** |
| KiCad E.D.A. 8.0.9 | | Id: 12/12 |