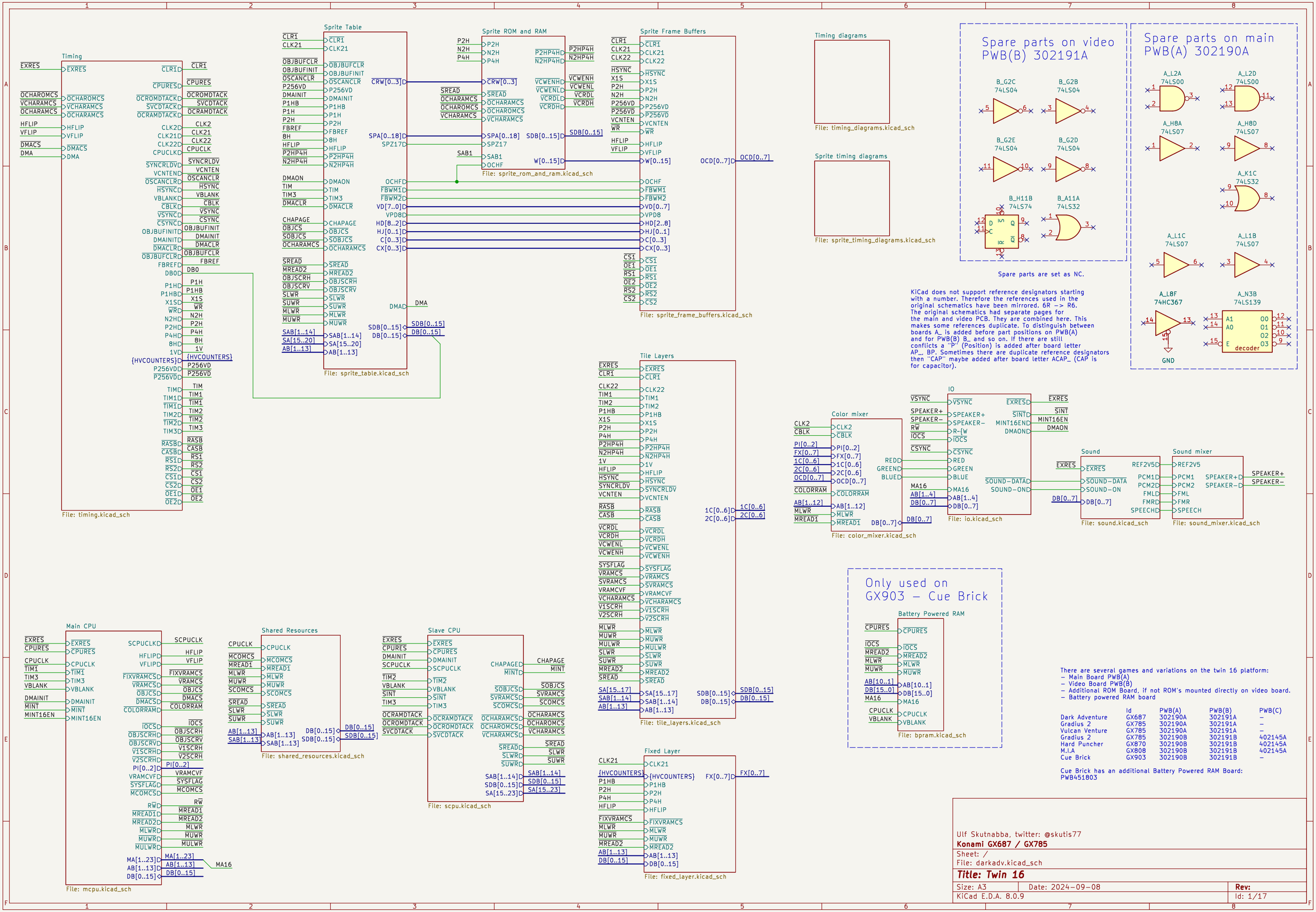
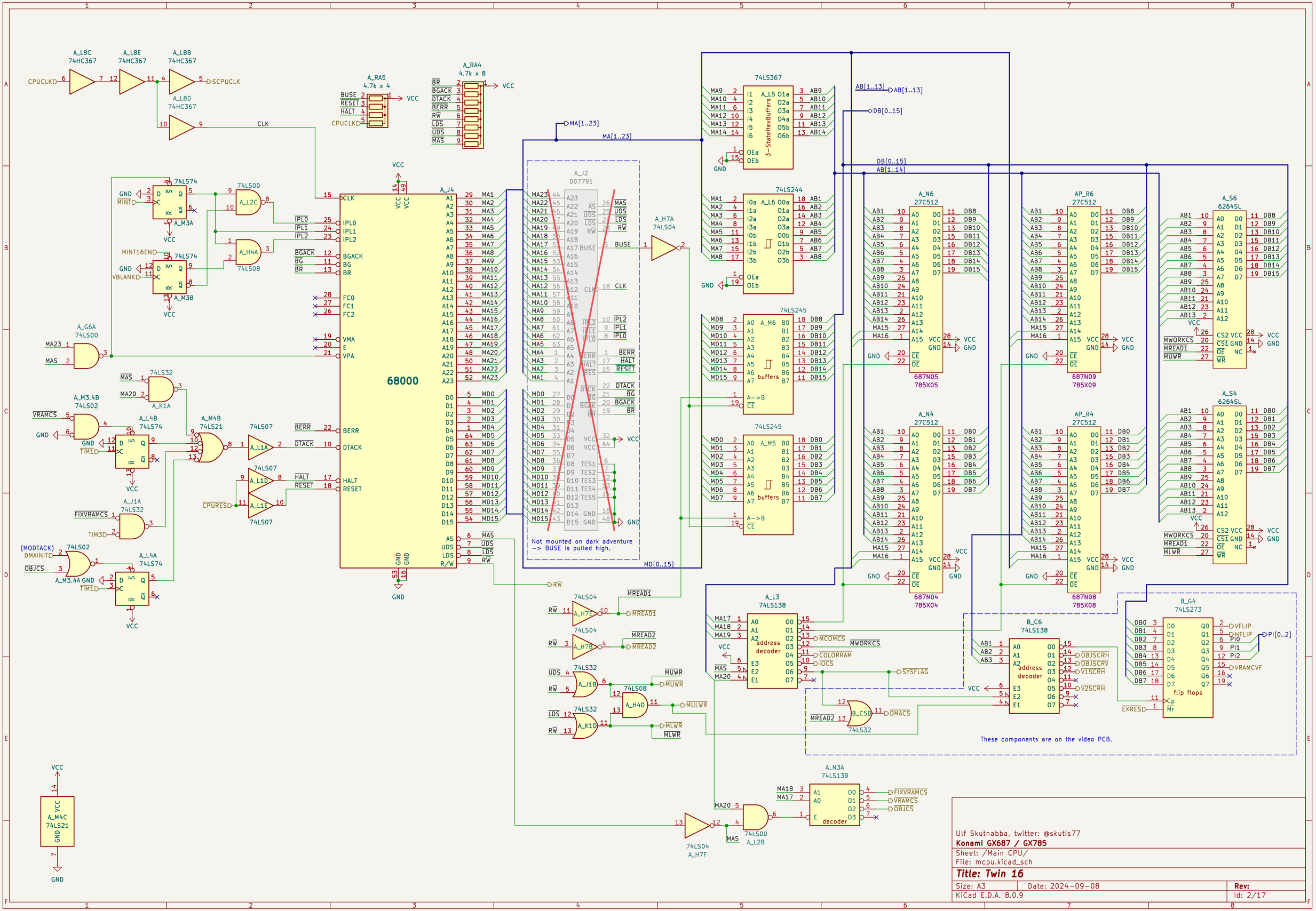
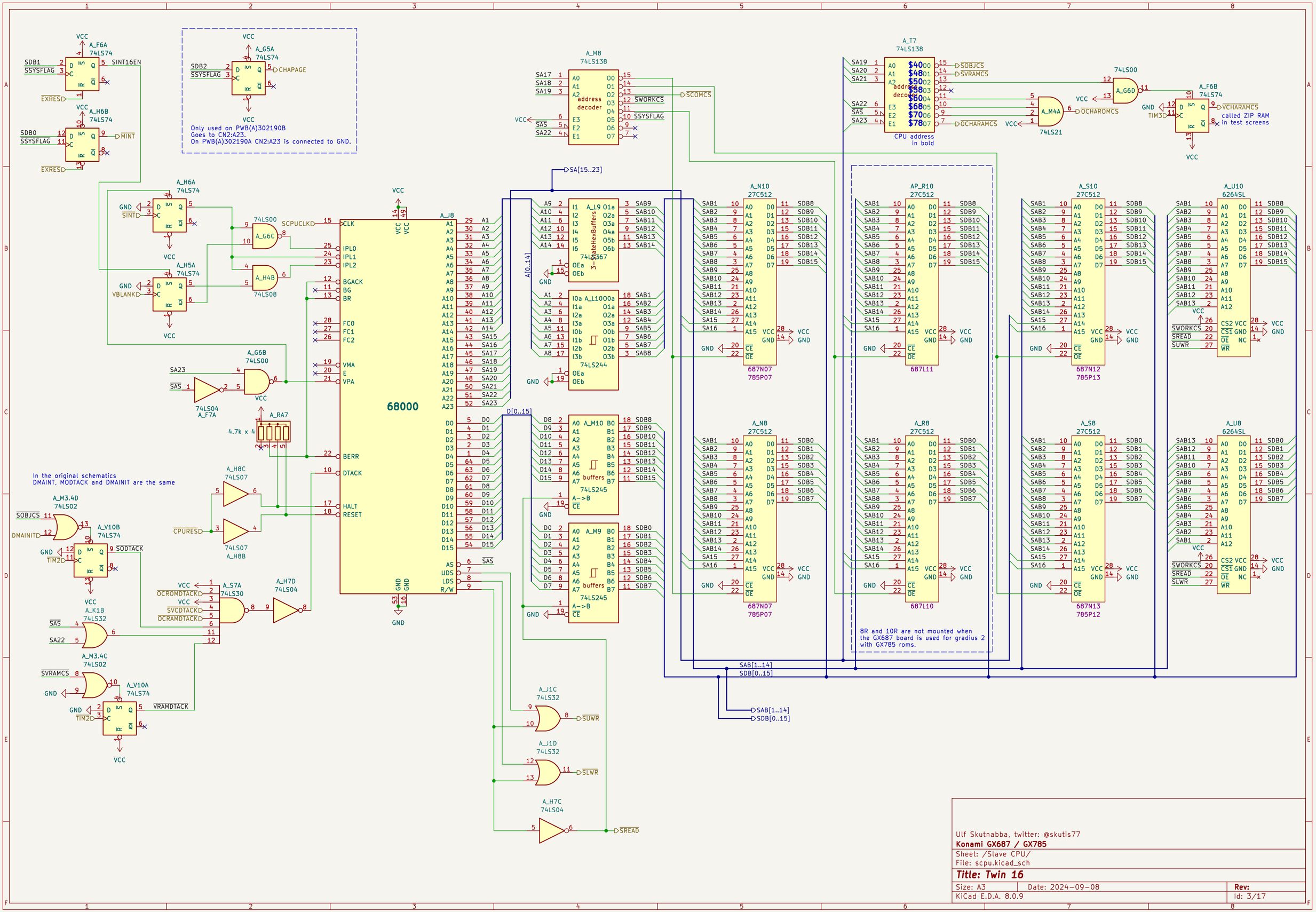

Timing
File: timing.kicad_sch
Sprite Table
File: sprite_table.kicad_sch
Sprite ROM and RAM
File: sprite_rom_and_ram.kicad_sch
Sprite Frame Buffers
File: sprite_frame_buffers.kicad_sch
Timing diagrams
File: timing_diagrams.kicad_sch
Sprite timing diagrams
File: sprite_timing_diagrams.kicad_sch
Spare parts on video PWB(B) 302191A
Spare parts on main PWB(A) 302190A
Spare parts are set as NC.
KiCad does not support reference designators starting with a number. Therefore the references used in the original schematics have been mirrored. 6R -> R6. The original schematics had separate pages for the main and video PCB. They are combined here. This makes some references duplicate. To distinguish between boards A_ is added before part positions on PWB(A) and for PWB(B) B_ and so on. If there are still conflicts a "P" (Position) is added after board letter AP_, BP. Sometimes there are duplicate reference designators then "CAP" maybe added after board letter ACAP_ (CAP is for capacitor).
Tile Layers
File: tile_layers.kicad_sch
Color mixer
File: color_mixer.kicad_sch
IO
File: io.kicad_sch
Sound
File: sound.kicad_sch
Sound mixer
File: sound_mixer.kicad_sch
Main CPU
File: mcpu.kicad_sch
Shared Resources
File: shared_resources.kicad_sch
Slave CPU
File: scpu.kicad_sch
Fixed Layer
File: fixed_layer.kicad_sch
Only used on GX903 – Cue Brick
Battery Powered RAM
File: bpram.kicad_sch
There are several games and variations on the twin 16 platform:
– Main Board PWB(A)
– Video Board PWB(B)
– Additional ROM Board, if not ROM's mounted directly on video board.
– Battery powered RAM board
Id PWB(A) PWB(B) PWB(C)
Dark Adventure GX687 302190A 302191A –
Gradius 2 GX785 302190A 302191A –
Vulcan Venture GX785 302190A 302191A –
Gradius 2 GX785 302190B 302191B 402145A
Hard Puncher GX870 302190B 302191B 402145A
M.I.A GX808 302190B 302191B 402145A
Cue Brick GX903 302190B 302191B –
Cue Brick has an additional Battery Powered RAM Board: PWB451803
Ulf Skutnabba, twitter: @skutis77
Konami GX687 / GX785
Sheet: /
File: darkadv.kicad_sch
Title: Twin 16
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 1/17


68000
A_J2
007791
Not mounted on dark adventure
-> BUSE is pulled high.
74LS367
74LS244
74LS245
74LS245
A_N6
27C512
687N05
785X05
A_N4
27C512
687N04
785X04
AP_R6
27C512
687N09
785X09
AP_R4
27C512
687N08
785X08
A_S6
6264SL
A_S4
6264SL
A_L3
74LS138
address
decoder
B_C6
74LS138
address
decoder
B_G4
74LS273
flip flops
These components are on the video PCB.
A_N3A
74LS139
decoder
A_M4C
74LS21
Ulf Skutnabba, twitter: @skutis77
Konami GX687 / GX785
Sheet: /Main CPU/
File: mcpu.kicad_sch
Title: Twin 16
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 2/17

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**Konami GX687 / GX785**

Sheet: /Slave CPU/

File: scpu.kicad_sch

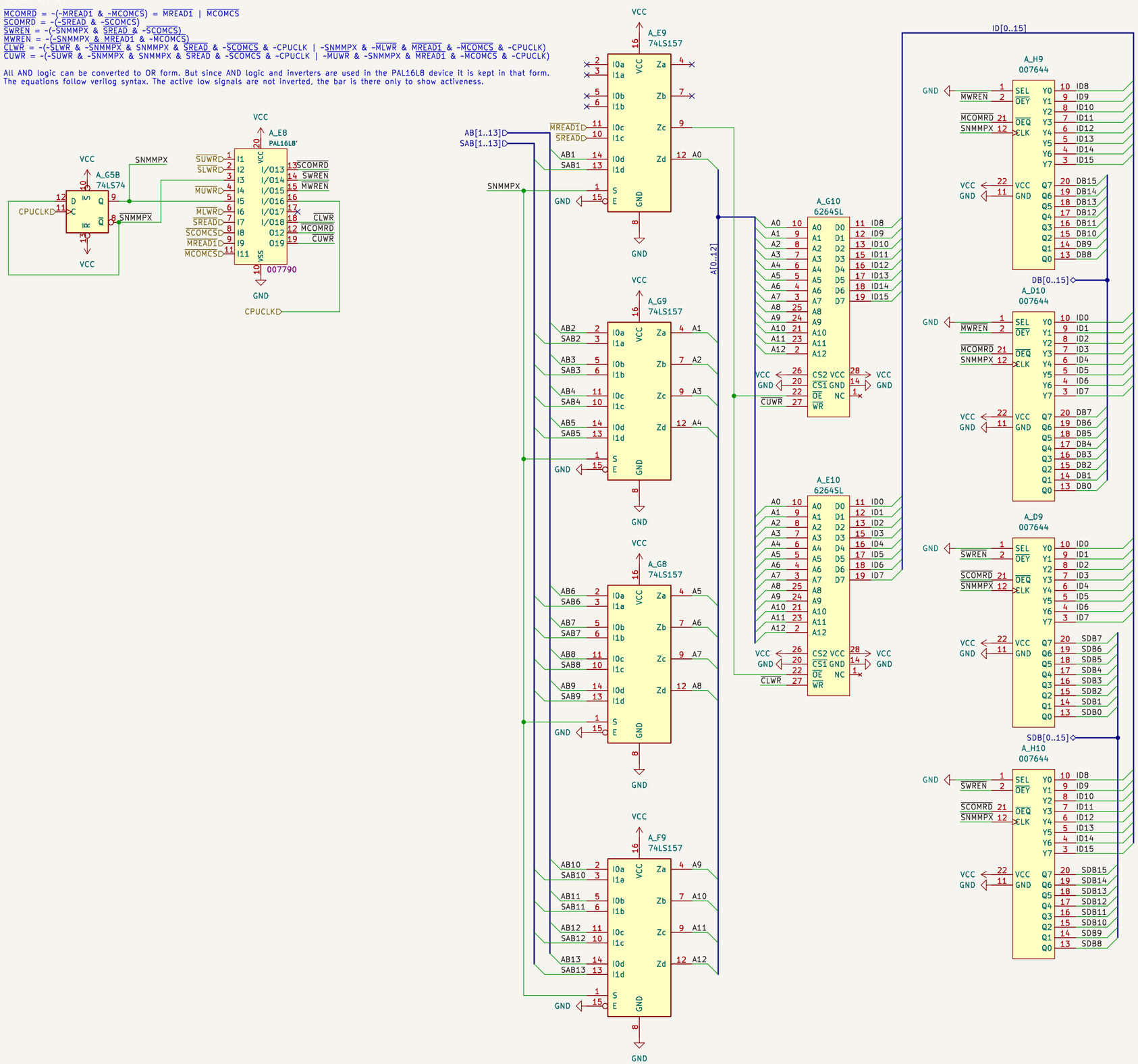
***Title: Twin 16***

| | | |
|---|---|---|
| Size: A3 | Date: 2024-09-08 | **Rev:** |
| KiCad E.D.A. 8.0.9 | | Id: 3/17 |

Konami 007790

$\overline{MCOMRD}$ = ~(~$\overline{MREAD1}$ & ~$\overline{MCOMCS}$) = $\overline{MREAD1}$ | $\overline{MCOMCS}$
$\overline{SCOMRD}$ = ~(~$\overline{SREAD}$ & ~$\overline{SCOMCS}$)
$\overline{SWREN}$ = ~(~$\overline{SNMMPX}$ & $\overline{SREAD}$ & ~$\overline{SCOMCS}$)
$\overline{MWREN}$ = ~(~$\overline{SNMMPX}$ & $\overline{MREAD1}$ & ~$\overline{MCOMCS}$)
$\overline{CLWR}$ = ~(~$\overline{SLWR}$ & ~$\overline{SNMMPX}$ & $\overline{SNMMPX}$ & $\overline{SREAD}$ & ~$\overline{SCOMCS}$ & ~CPUCLK | ~$\overline{SNMMPX}$ & ~$\overline{MLWR}$ & $\overline{MREAD1}$ & ~$\overline{MCOMCS}$ & ~CPUCLK)
$\overline{CUWR}$ = ~(~$\overline{SUWR}$ & ~$\overline{SNMMPX}$ & $\overline{SNMMPX}$ & $\overline{SREAD}$ & ~$\overline{SCOMCS}$ & ~CPUCLK | ~$\overline{MUWR}$ & ~$\overline{SNMMPX}$ & $\overline{MREAD1}$ & ~$\overline{MCOMCS}$ & ~CPUCLK)

All AND logic can be converted to OR form. But since AND logic and inverters are used in the PAL16L8 device it is kept in that form.
The equations follow verilog syntax. The active low signals are not inverted, the bar is there only to show activeness.




This is from jammarcade.net

Pin 1 = SEL – changes whether the Q outputs require a rising edge clock or not.
Pin 2 = OEY – Output enable for the Y outputs else they are inputs. Active LOW
Pin 21 = OEQ – Output enable for the Q (clocked) outputs else they are inputs. Active LOW
Pin 12 = CLK – Clock input

Pins 3–10 = Y outputs – normal outputs. If OEY is LOW these pins become outputs
mirroring the state of the Q input pins. SEL and CLK pins are not used in this mode.

Pins 13–20 = Q outputs – clocked outputs. If OEQ is LOW these pins become outputs.
If SEL is HIGH and CLK is HIGH these outputs will mirror the state of the Y inputs.
If SEL is LOW then the outputs will only change state on a rising edge CLK.

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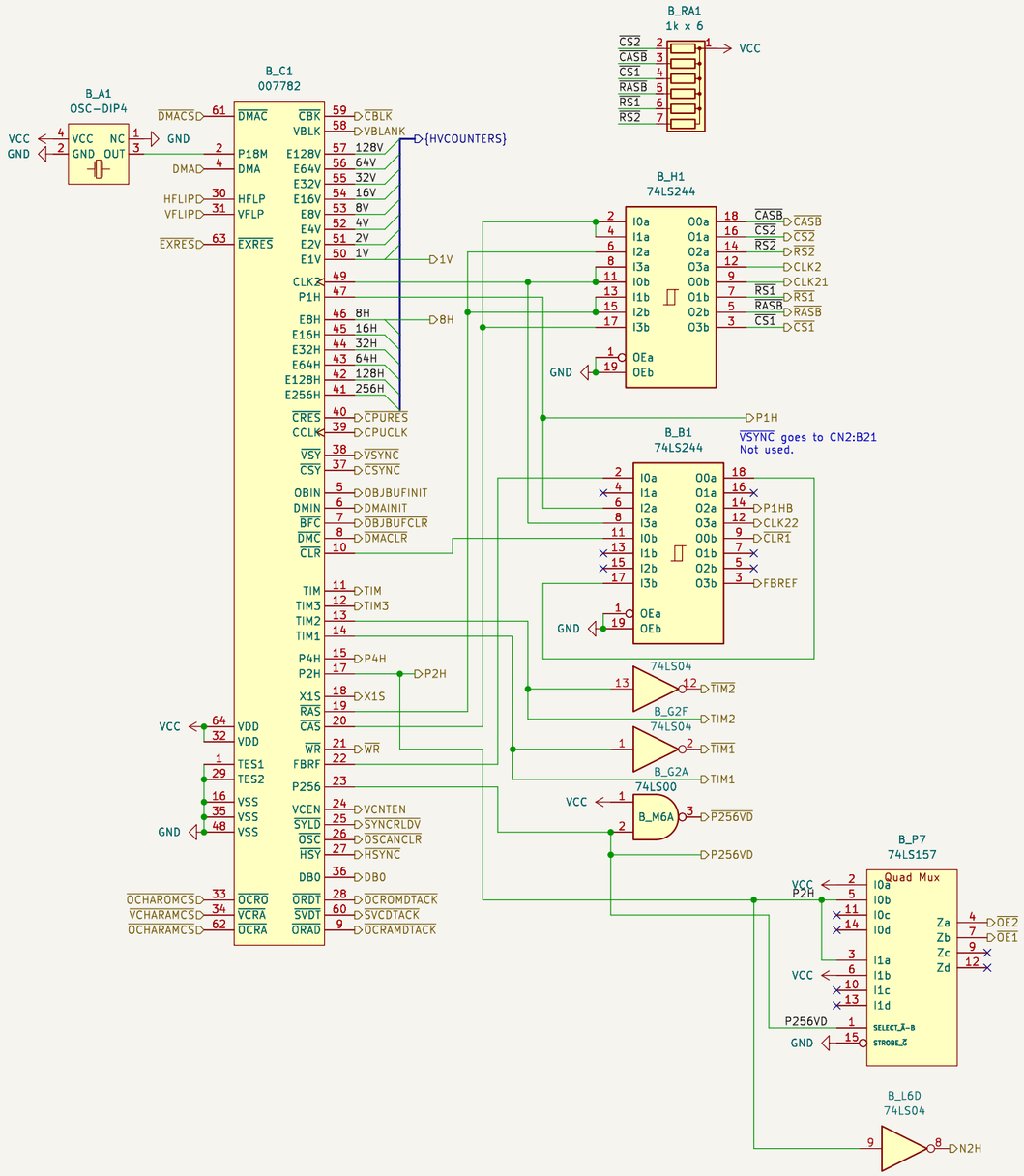
**Konami GX687 / GX785**

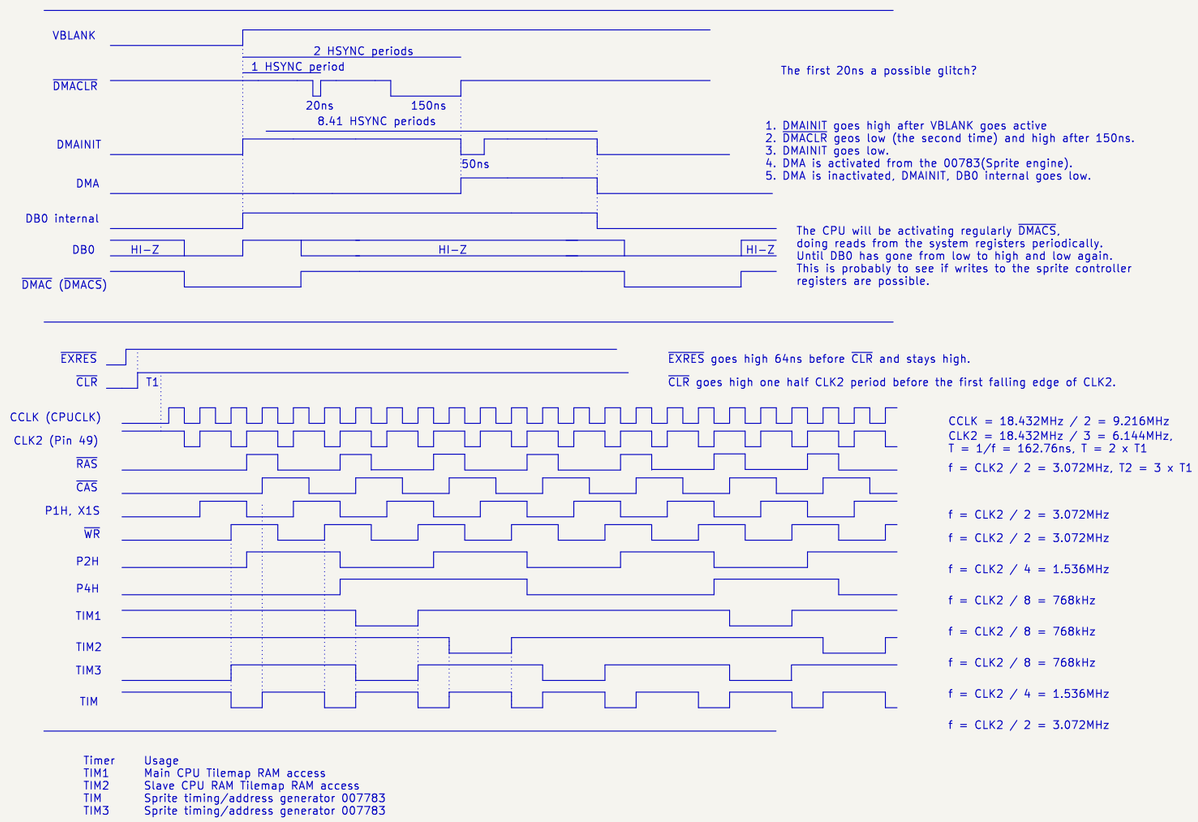
Sheet: /Shared Resources/
File: shared_resources.kicad_sch

***Title: Twin 16***

| Size: A3 | Date: 2024-09-08 | **Rev:** |
|---|---|---|
| KiCad E.D.A. 8.0.9 | | Id: 4/17 |

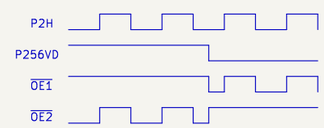



# DMA Synchronization

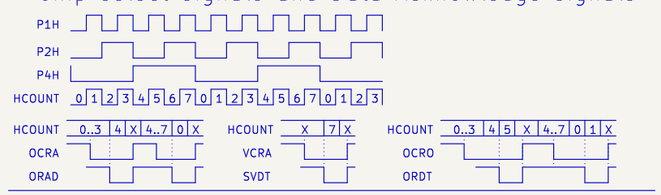



| Timer | Usage |
|---|---|
| TIM1 | Main CPU Tilemap RAM access |
| TIM2 | Slave CPU RAM Tilemap RAM access |
| TIM | Sprite timing/address generator 007783 |
| TIM3 | Sprite timing/address generator 007783 |

## Output enables active vs. part of frame buffer active




## Chip select signals and Data Acknowledge signals

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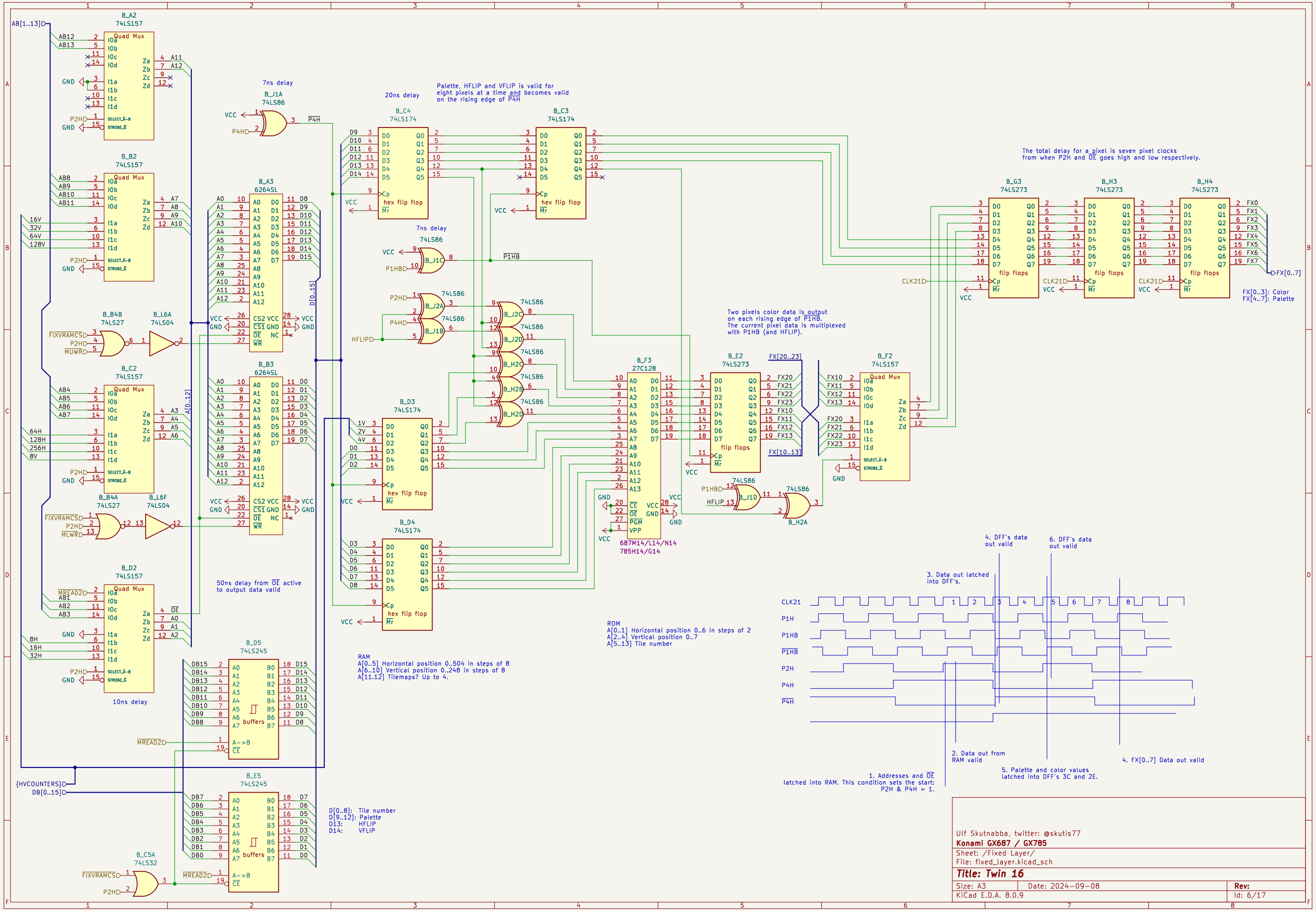
**Konami GX687 / GX785**

Sheet: /Timing/
File: timing.kicad_sch

***Title: Twin 16***

| Size: A3 | Date: 2024-09-08 | **Rev:** |
|---|---|---|
| KiCad E.D.A. 8.0.9 | | Id: 5/17 |


B_A2
74LS157
Quad Mux
B_B2
74LS157
B_A3
6264SL
B_B3
6264SL
B_B4B
74LS27
B_L6A
74LS04
B_C2
74LS157
B_B4A
74LS27
B_L6F
74LS04
B_D2
74LS157
B_D5
74LS245
B_E5
74LS245
B_C5A
74LS32
7ns delay
B_J1A
74LS86
20ns delay
B_C4
74LS174
B_C3
74LS174
hex flip flop
Palette, HFLIP and VFLIP is valid for eight pixels at a time and becomes valid on the rising edge of P4H
B_D3
74LS174
B_D4
74LS174
B_J2A
B_J1B
B_J2C
B_J2D
B_H2C
B_H2B
B_H2D
B_J1C
B_J1D
B_H2A
B_F3
27C128
687M14/L14/N14
785H14/G14
B_E2
74LS273
flip flops
B_F2
74LS157
B_G3
74LS273
B_H3
74LS273
B_H4
74LS273
The total delay for a pixel is seven pixel clocks from when P2H and OE goes high and low respectively.
FX[0..3]: Color
FX[4..7]: Palette
Two pixels color data is output on each rising edge of P1HB. The current pixel data is multiplexed with P1HB (and HFLIP).
50ns delay from OE active to output data valid
10ns delay
buffers
RAM
A[0..5] Horizontal position 0..504 in steps of 8
A[6..10] Vertical position 0..248 in steps of 8
A[11.12] Tilemaps? Up to 4.
ROM
A[0..1] Horizontal position 0..6 in steps of 2
A[2..4] Vertical position 0..7
A[5..13] Tile number
D[0..8]: Tile number
D[9..12]: Palette
D13: HFLIP
D14: VFLIP
1. Addresses and OE latched into RAM. This condition sets the start: P2H & P4H = 1.
2. Data out from RAM valid
3. Data out latched into DFF's.
4. DFF's data out valid
5. Palette and color values latched into DFF's 3C and 2E.
6. DFF's data out valid
4. FX[0..7] Data out valid
CLK21
P1H
P1HB
P2H
P4H
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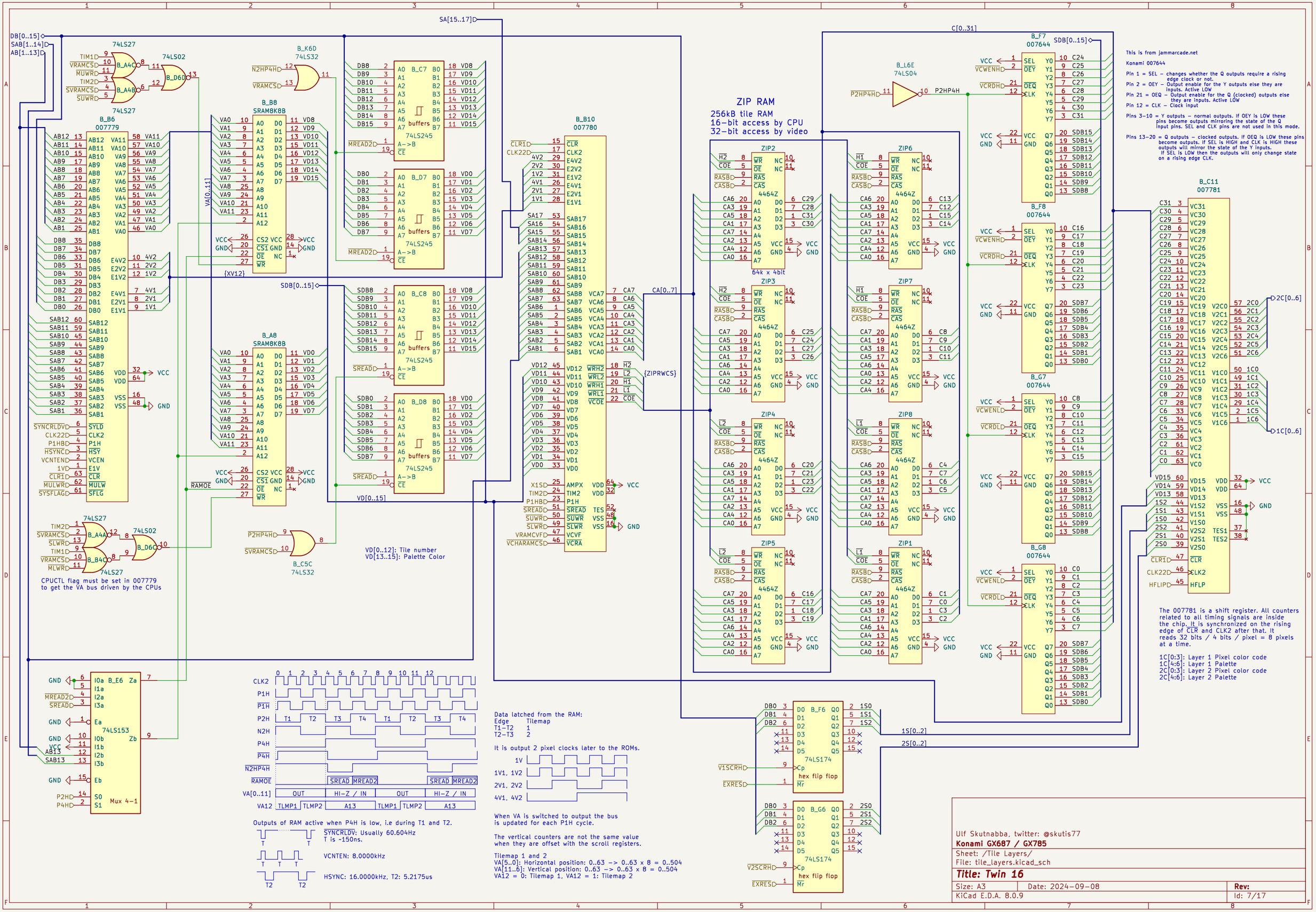
Konami GX687 / GX785
Sheet: /Fixed Layer/
File: fixed_layer.kicad_sch
Title: Twin 16
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 6/17


ZIP RAM
256kB tile RAM
16-bit access by CPU
32-bit access by video
This is from jammarcade.net
Konami 007644
Pin 1 = SEL – changes whether the Q outputs require a rising edge clock or not.
Pin 2 = OEY – Output enable for the Y outputs else they are inputs. Active LOW
Pin 21 = OEQ – Output enable for the Q (clocked) outputs else they are inputs. Active LOW
Pin 12 = CLK – Clock input
Pins 3–10 = Y outputs – normal outputs. If OEY is LOW these pins become outputs mirroring the state of the Q input pins. SEL and CLK pins are not used in this mode.
Pins 13–20 = Q outputs – clocked outputs. If OEQ is LOW these pins become outputs. If SEL is HIGH and CLK is HIGH these outputs will mirror the state of the Y inputs. If SEL is LOW then the outputs will only change state on a rising edge CLK.
CPUCTL flag must be set in 007779 to get the VA bus driven by the CPUs
VD[0..12]: Tile number
VD[13..15]: Palette Color
The 007781 is a shift register. All counters related to all timing signals are inside the chip. It is synchronized on the rising edge of CLR and CLK2 after that. It reads 32 bits / 4 bits / pixel = 8 pixels at a time.
1C[0:3]: Layer 1 Pixel color code
1C[4:6]: Layer 1 Palette
2C[0:3]: Layer 2 Pixel color code
2C[4:6]: Layer 2 Palette
Outputs of RAM active when P4H is low, i.e during T1 and T2.
SYNCRLDV: Usually 60.604Hz
T is ~150ns.
VCNTEN: 8.0000kHz
HSYNC: 16.0000kHz, T2: 5.2175us
Data latched from the RAM:
Edge Tilemap
T1–T2 1
T2–T3 2
It is output 2 pixel clocks later to the ROMs.
When VA is switched to output the bus is updated for each P1H cycle.
The vertical counters are not the same value when they are offset with the scroll registers.
Tilemap 1 and 2
VA[5..0]: Horizontal position: 0..63 –> 0..63 x 8 = 0..504
VA[11..6]: Vertical position: 0..63 –> 0..63 x 8 = 0..504
VA12 = 0: Tilemap 1, VA12 = 1: Tilemap 2
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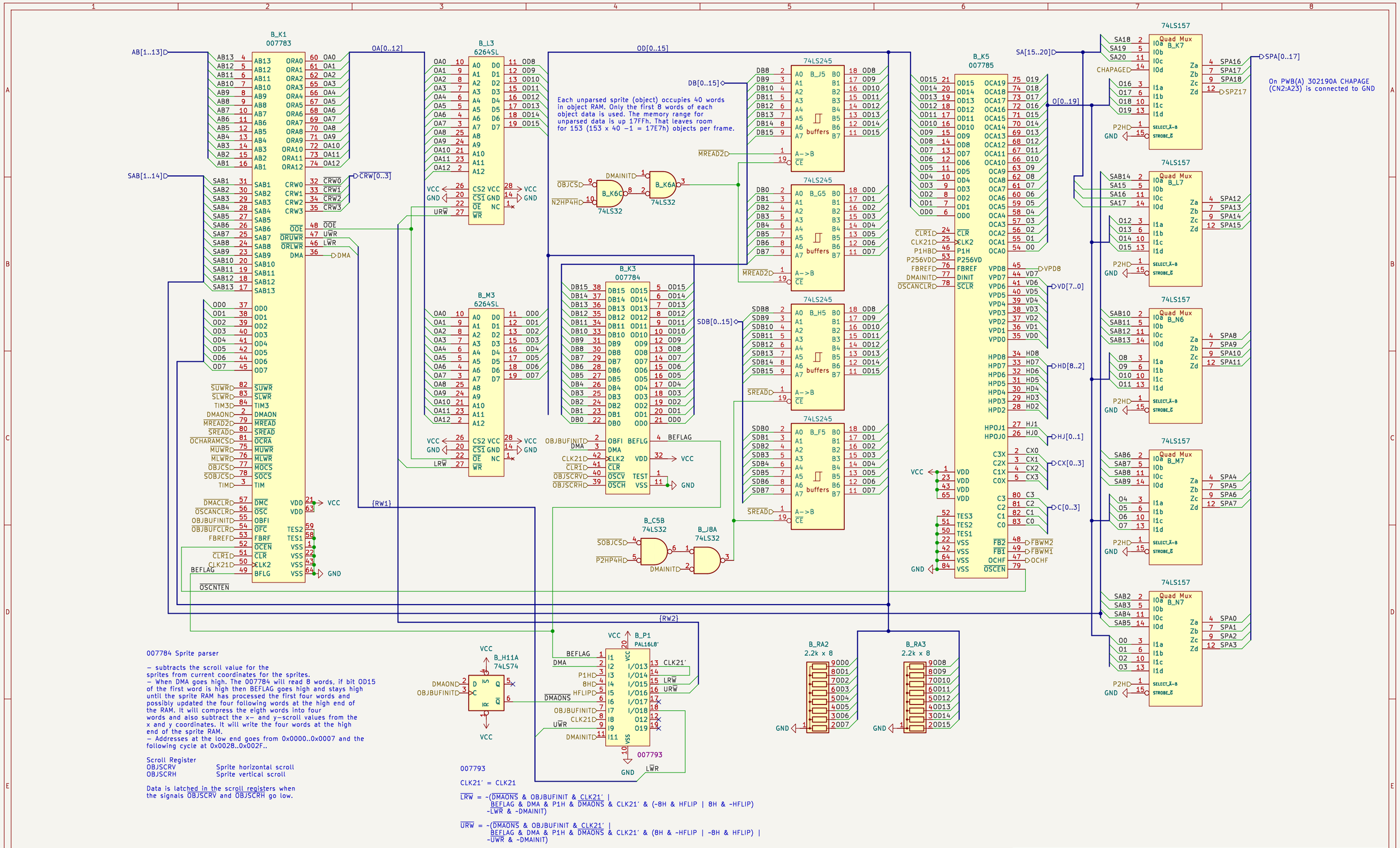
Konami GX687 / GX785
Sheet: /Tile Layers/
File: tile_layers.kicad_sch
Title: Twin 16
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 7/17

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**Konami GX687 / GX785**

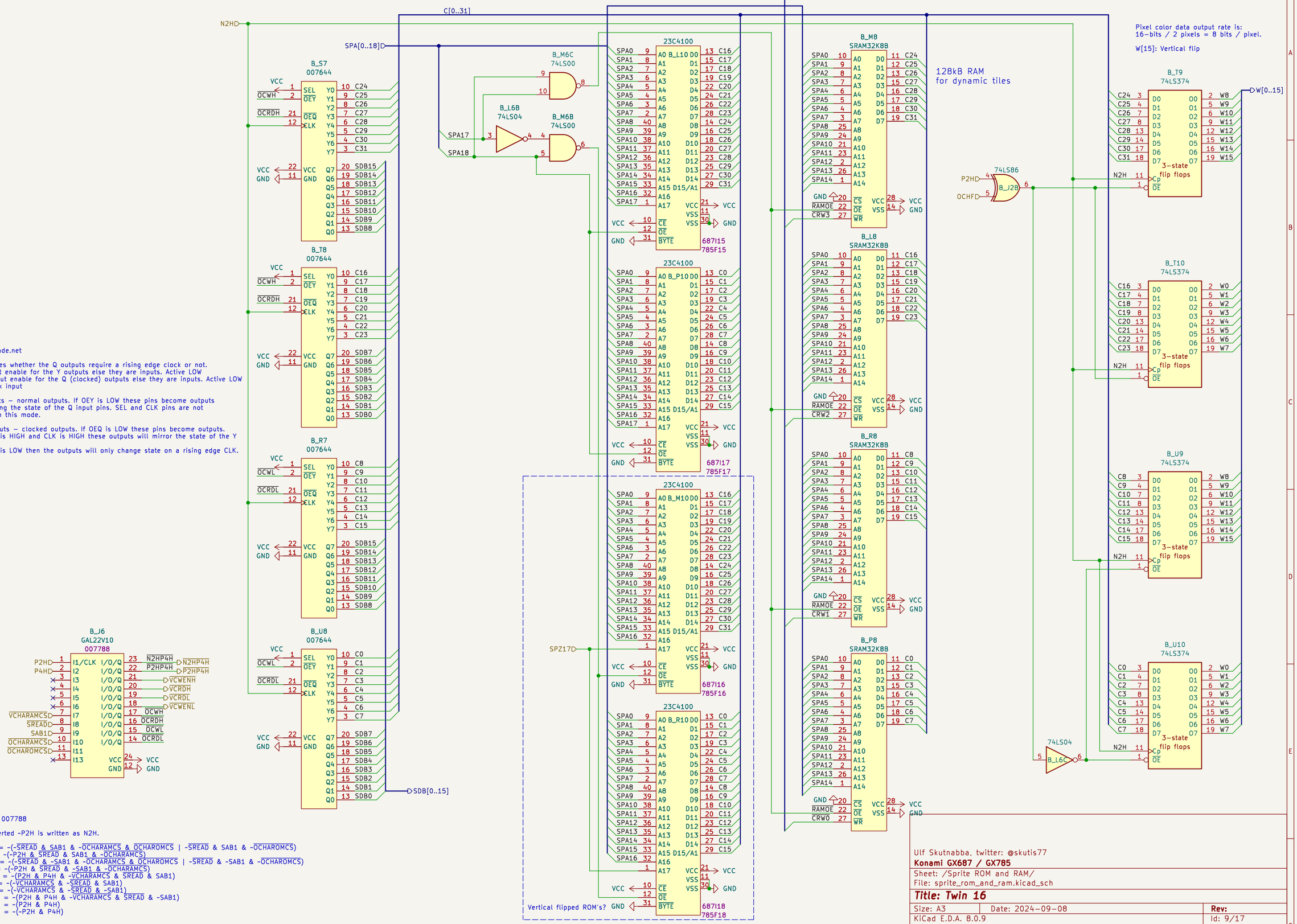
Sheet: /Sprite Table/

File: sprite_table.kicad_sch

***Title: Twin 16***

| Size: A3 | Date: 2024−09−08 | **Rev:** |
|---|---|---|
| KiCad E.D.A. 8.0.9 | | Id: 8/17 |

# Graphics Tile Data (ROM and RAM)




This is from jammarcade.net

Pin 1 = SEL – changes whether the Q outputs require a rising edge clock or not.
Pin 2 = OEY – Output enable for the Y outputs else they are inputs. Active LOW
Pin 21 = OEQ – Output enable for the Q (clocked) outputs else they are inputs. Active LOW
Pin 12 = CLK – Clock input

Pins 3–10 = Y outputs – normal outputs. If OEY is LOW these pins become outputs mirroring the state of the Q input pins. SEL and CLK pins are not used in this mode.

Pins 13–20 = Q outputs – clocked outputs. If OEQ is LOW these pins become outputs. If SEL is HIGH and CLK is HIGH these outputs will mirror the state of the Y inputs.
If SEL is LOW then the outputs will only change state on a rising edge CLK.

Konami 007788

The inverted ~P2H is written as N2H.

$\overline{\text{OCRDL}}$ = ~(~$\overline{\text{SREAD}}$ & SAB1 & ~$\overline{\text{OCHARAMCS}}$ & $\overline{\text{OCHAROMCS}}$ | ~$\overline{\text{SREAD}}$ & SAB1 & ~$\overline{\text{OCHAROMCS}}$)
$\overline{\text{OCWL}}$ = ~(~P2H & $\overline{\text{SREAD}}$ & SAB1 & ~$\overline{\text{OCHARAMCS}}$)
$\overline{\text{OCRDH}}$ = ~(~$\overline{\text{SREAD}}$ & ~SAB1 & ~$\overline{\text{OCHARAMCS}}$ & $\overline{\text{OCHAROMCS}}$ | ~$\overline{\text{SREAD}}$ & ~SAB1 & ~$\overline{\text{OCHAROMCS}}$)
$\overline{\text{OCWH}}$ = ~(~P2H & $\overline{\text{SREAD}}$ & ~SAB1 & ~$\overline{\text{OCHARAMCS}}$)
$\overline{\text{VCWENL}}$ = ~(P2H & P4H & ~$\overline{\text{VCHARAMCS}}$ & $\overline{\text{SREAD}}$ & SAB1)
$\overline{\text{VCRDL}}$ = ~(~$\overline{\text{VCHARAMCS}}$ & ~$\overline{\text{SREAD}}$ & SAB1)
$\overline{\text{VCRDH}}$ = ~(~$\overline{\text{VCHARAMCS}}$ & ~$\overline{\text{SREAD}}$ & ~SAB1)
$\overline{\text{VCWENH}}$ = ~(P2H & P4H & ~$\overline{\text{VCHARAMCS}}$ & $\overline{\text{SREAD}}$ & ~SAB1)
$\overline{\text{P2HP4H}}$ = ~(P2H & P4H)
$\overline{\text{N2HP4H}}$ = ~(~P2H & P4H)

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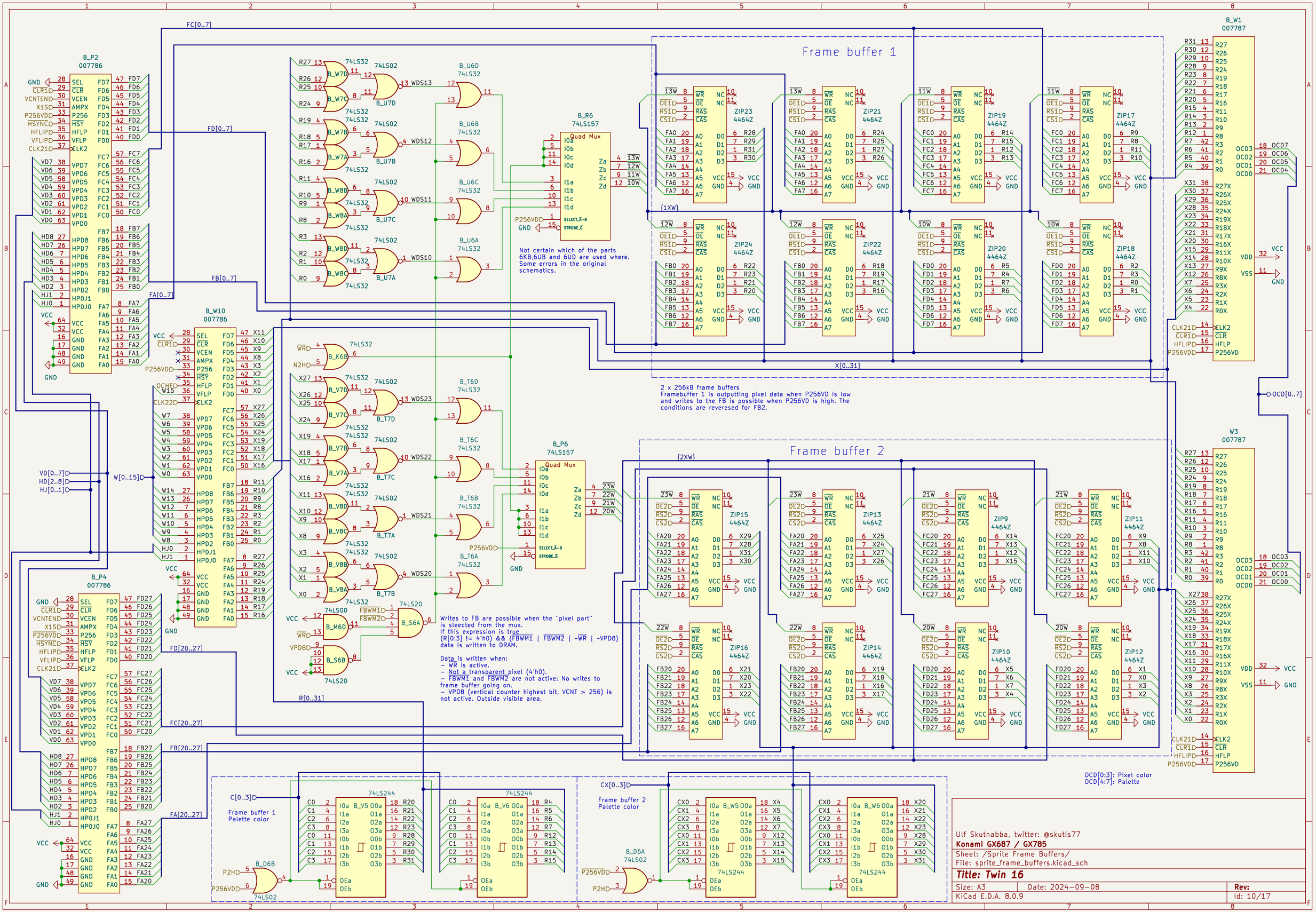
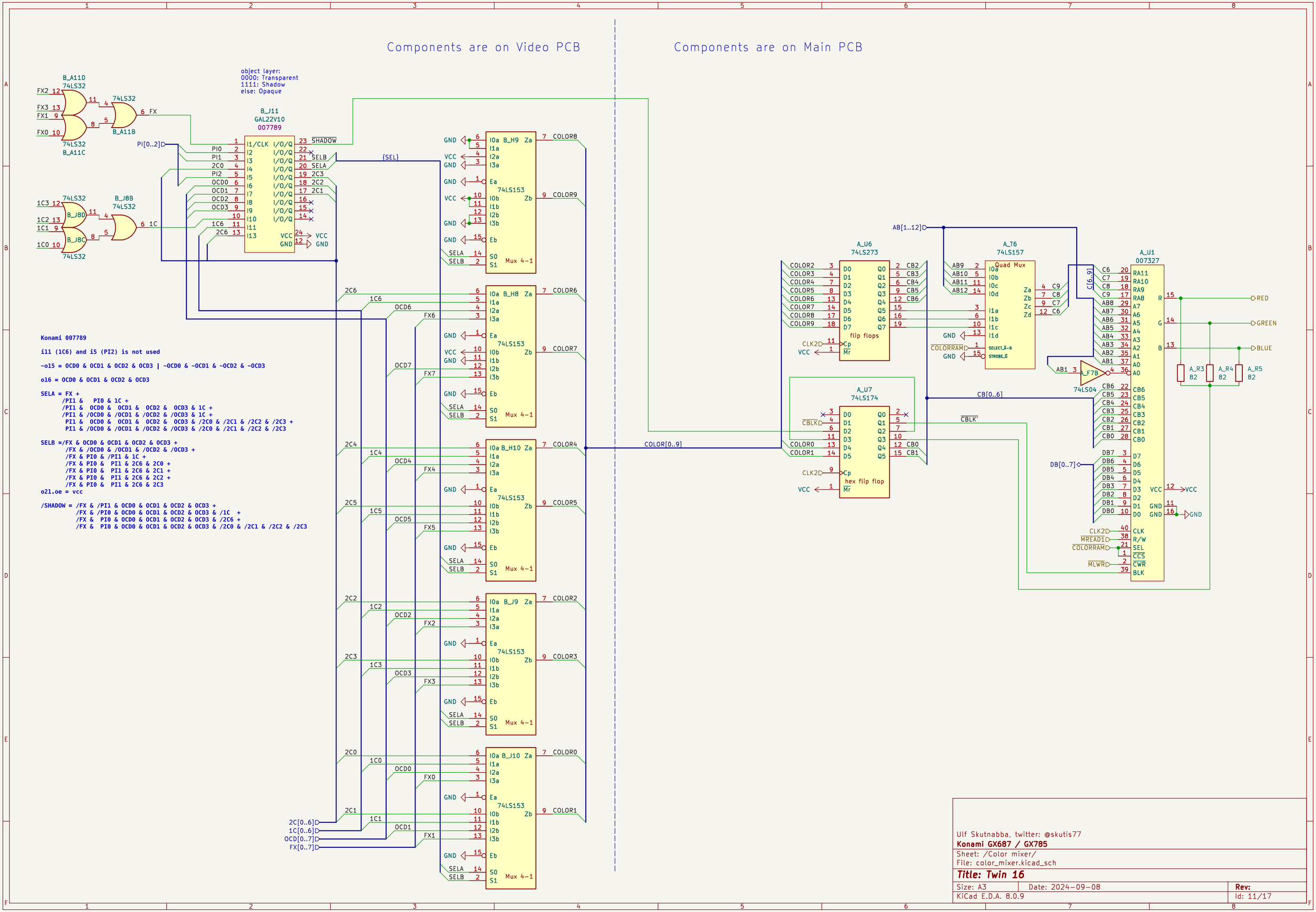
**Konami GX687 / GX785**

Sheet: /Sprite ROM and RAM/
File: sprite_rom_and_ram.kicad_sch

**Title: Twin 16**

| Size: A3 | Date: 2024-09-08 | Rev: |
|---|---|---|
| KiCad E.D.A. 8.0.9 | | Id: 9/17 |


Frame buffer 1
Frame buffer 2
B_P2 007786
B_W10 007786
B_P4 007786
B_W1 007787
W3 007787
B_R6 74LS157
B_P6 74LS157
Quad Mux
Not certain which of the parts 6KB,6UB and 6UD are used where. Some errors in the original schematics.
2 x 256kB frame buffers
Framebuffer 1 is outputting pixel data when P256VD is low and writes to the FB is possible when P256VD is high. The conditions are reveresed for FB2.
Writes to FB are possible when the "pixel part" is sleected from the mux.
If this expression is true
(R[0:3] != 4'h0) && (FBWM1 | FBWM2 | -WR | -VPD8)
data is written to DRAM.
Data is written when:
– WR is active.
– Not a transparent pixel (4'h0).
– FBWM1 and FBWM2 are not active: No writes to frame buffer going on.
– VPD8 (vertical counter highest bit, VCNT > 256) is not active. Outside visible area.
Frame buffer 1 Palette color
Frame buffer 2 Palette color
OCD[0:3]: Pixel color
OCD[4:7]: Palette
Ulf Skutnabba, twitter: @skutis77
Konami GX687 / GX785
Sheet: /Sprite Frame Buffers/
File: sprite_frame_buffers.kicad_sch
Title: Twin 16
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 10/17




Ulf Skutnabba, twitter: @skutis77

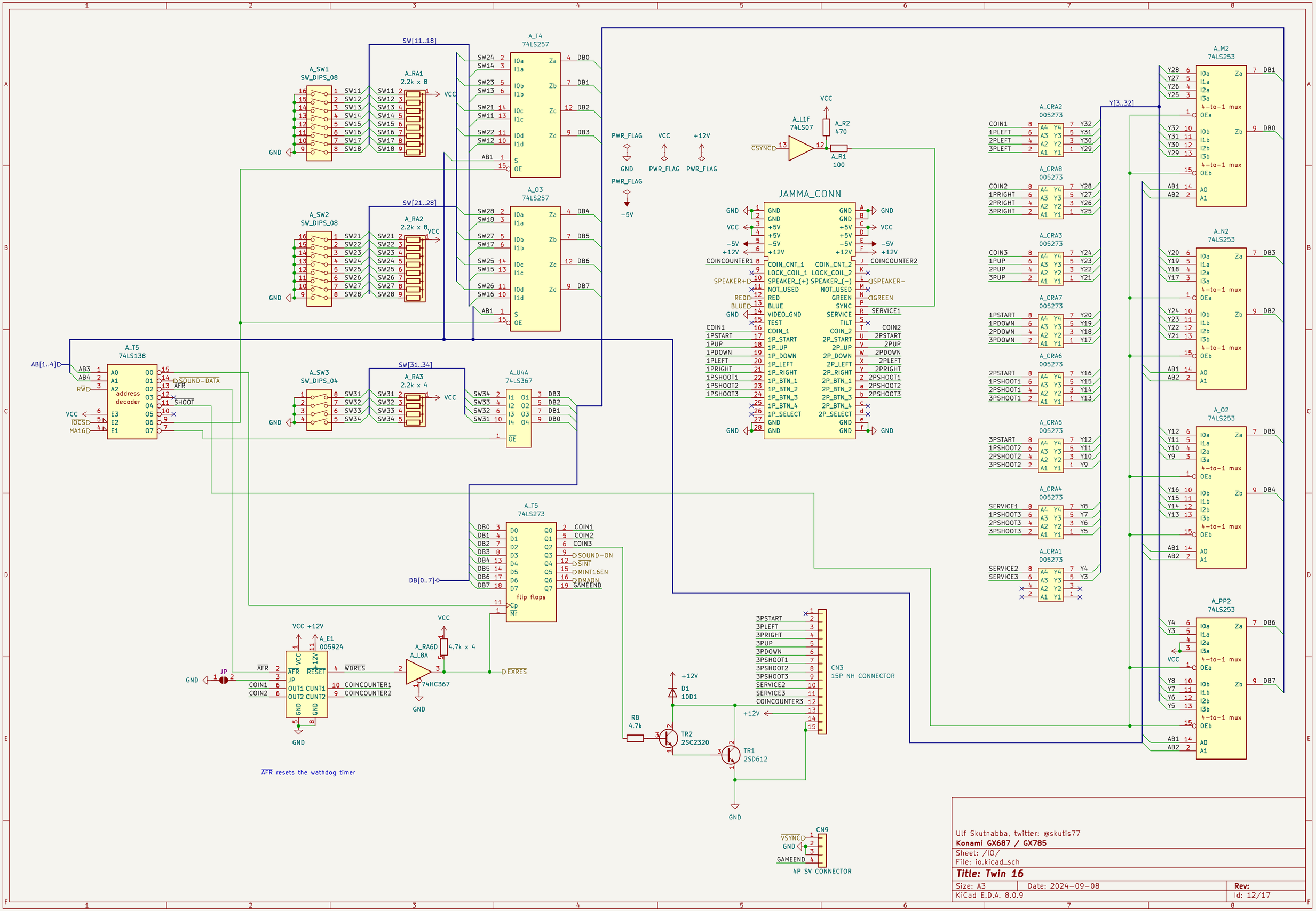
**Konami GX687 / GX785**

Sheet: /Color mixer/

File: color_mixer.kicad_sch

***Title: Twin 16***

| Size: A3 | Date: 2024-09-08 | Rev: |
|---|---|---|
| KiCad E.D.A. 8.0.9 | | Id: 11/17 |



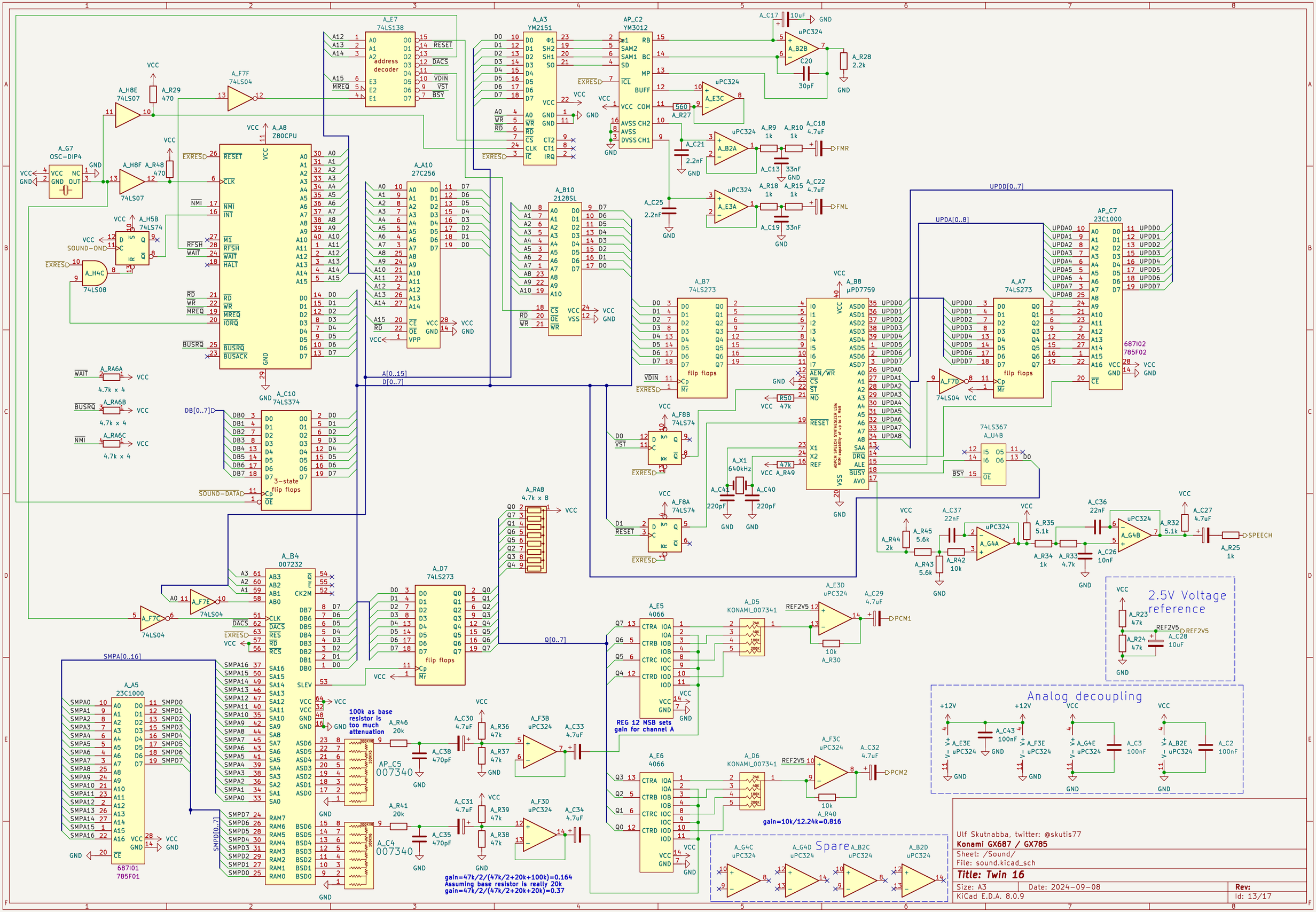

Ulf Skutnabba, twitter: @skutis77

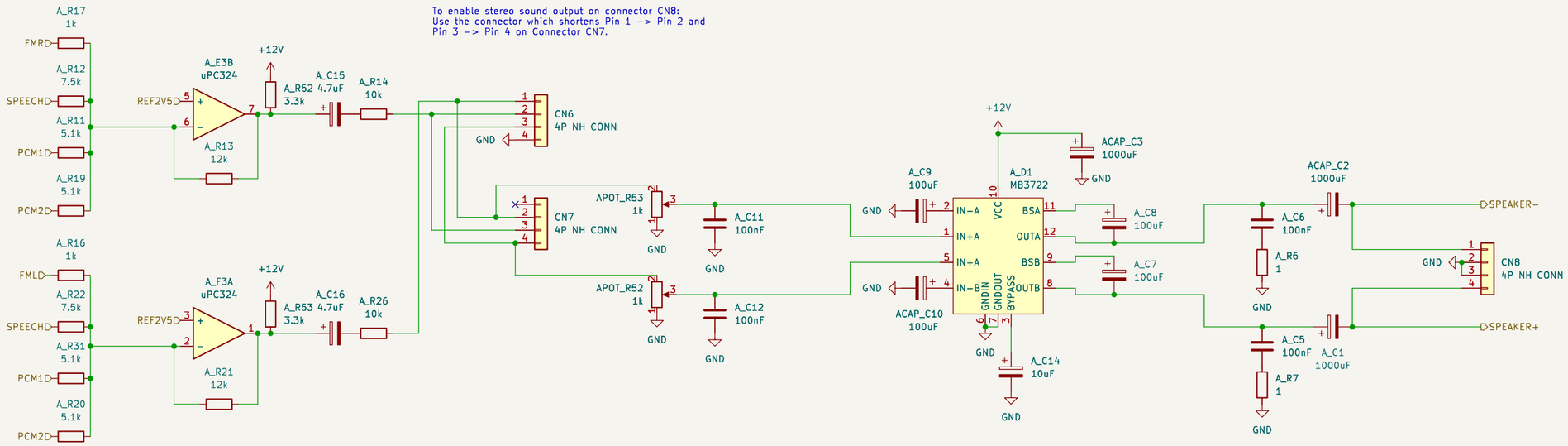
**Konami GX687 / GX785**

Sheet: /IO/
File: io.kicad_sch

***Title: Twin 16***

| | | |
|---|---|---|
| Size: A3 | Date: 2024-09-08 | **Rev:** |
| KiCad E.D.A. 8.0.9 | | Id: 12/17 |


A_E7
74LS138
address decoder
A_A3
YM2151
AP_C2
YM3012
A_F7F
74LS04
A_H8E
74LS07
A_R29
470
A_G7
OSC-DIP4
A_H8F
74LS07
A_R48
470
A_H5B
74LS74
A_H4C
74LS08
A_A8
Z80CPU
A_A10
27C256
A_B10
2128SL
A_B7
74LS273
flip flops
A_B8
µPD7759
ADPCM SPEECH SYNTHESIZER LSI
ROM capability of up to 1 Mbit
A_A7
74LS273
AP_C7
23C1000
687I02
785F02
A_C10
74LS374
3-state
flip flops
A_F8B
74LS74
A_F8A
74LS74
A_X1
640kHz
74LS367
A_U4B
A_RA6A
4.7k x 4
A_RA6B
4.7k x 4
A_RA6C
4.7k x 4
A_RA8
4.7k x 8
A_B4
007232
A_F7E
74LS04
A_F7C
74LS04
A_D7
74LS273
A_A5
23C1000
687I01
785F01
A_E5
4066
A_D5
KONAMI_007341
A_E6
4066
A_D6
KONAMI_007341
A_E3D
uPC324
A_F3B
uPC324
A_F3D
uPC324
A_F3C
uPC324
AP_C5
007340
A_C4
007340
100k as base resistor is too much attenuation
REG 12 MSB sets gain for channel A
gain=10k/12.24k=0.816
gain=47k/2/(47k/2+20k+100k)=0.164
Assuming base resistor is really 20k
gain=47k/2/(47k/2+20k+20k)=0.37
2.5V Voltage reference
Analog decoupling
Spare
A_G4C
uPC324
A_G4D
uPC324
A_B2C
uPC324
A_B2D
uPC324
A_B2B
uPC324
A_E3C
uPC324
A_B2A
uPC324
A_E3A
uPC324
A_G4A
uPC324
A_G4B
uPC324
A_E3E
uPC324
A_F3E
uPC324
A_G4E
uPC324
A_B2E
uPC324
A_F7D
74LS04
A_R28
2.2k
A_R27
560
A_R50
47k
A_R49
47k
A_R23
47k
A_R24
47k
A_R30
10k
A_R40
10k
A_R25
1k
A_R32
5.1k
A_R35
5.1k
A_R34
1k
A_R33
4.7k
A_R44
2k
A_R45
5.6k
A_R43
5.6k
A_R42
10k
A_R46
20k
A_R41
20k
A_R36
47k
A_R37
47k
A_R39
47k
A_R38
47k
A_R9
1k
A_R10
1k
A_R18
1k
A_R15
1k
A_C17
10uF
A_C20
30pF
A_C21
2.2nF
A_C25
2.2nF
A_C13
33nF
A_C19
33nF
A_C18
4.7uF
A_C22
4.7uF
A_C36
22nF
A_C37
22nF
A_C26
10nF
A_C27
4.7uF
A_C28
10uF
A_C29
4.7uF
A_C32
4.7uF
A_C33
4.7uF
A_C34
4.7uF
A_C30
4.7uF
A_C31
4.7uF
A_C38
470pF
A_C35
470pF
A_C41
220pF
A_C40
220pF
A_C43
100nF
A_C3
100nF
A_C2
100nF
A_C42
FMR
FML
PCM1
PCM2
SPEECH
REF2V5
UPDD[0..7]
UPDA[0..8]
A[0..15]
D[0..7]
DB[0..7]
SMPA[0..16]
SMPD[0..7]
Q[0..7]
Ulf Skutnabba, twitter: @skutis77
Konami GX687 / GX785
Sheet: /Sound/
File: sound.kicad_sch
Title: Twin 16
Size: A3
Date: 2024-09-08
KiCad E.D.A. 8.0.9
Rev:
Id: 13/17

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**Konami GX687 / GX785**

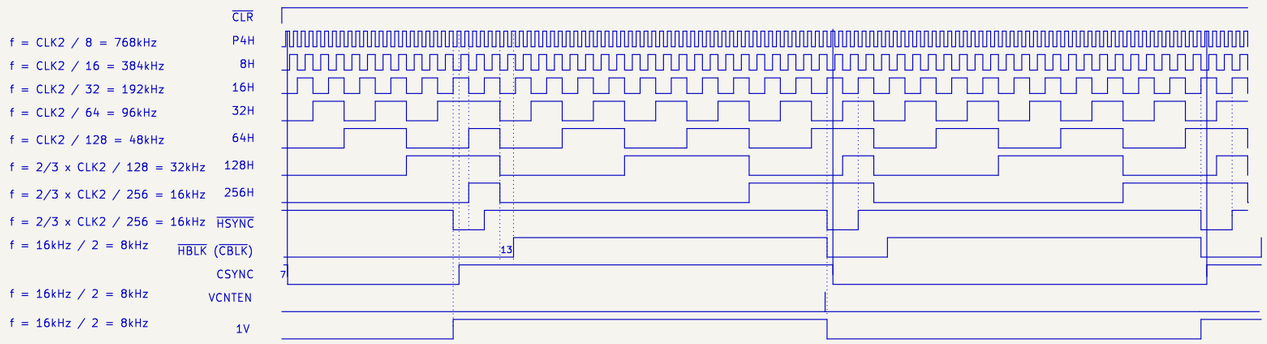
Sheet: /Sound mixer/

File: sound_mixer.kicad_sch

***Title: Twin 16***

| | | |
|---|---|---|
| Size: A3 | Date: 2024-09-08 | **Rev:** |
| KiCad E.D.A. 8.0.9 | | Id: 14/17 |

# Horizontal signals

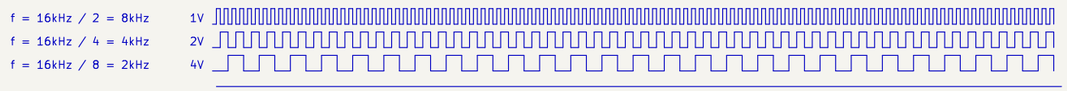


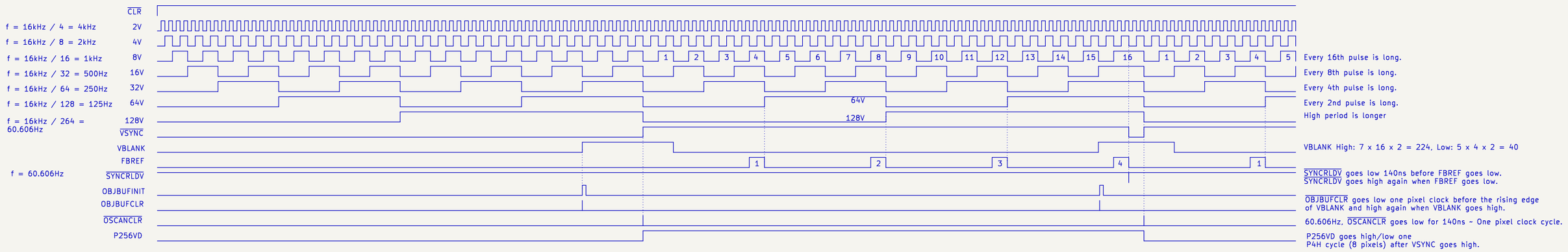

– The first VCNTEN is skipped after reset.
It goes low 140ns before HSYNC goes low,
and high again when HSYNC goes low.
VCNTEN is active right before every second falling edge of HSYNC.

– CPURES goes high, and stays high, on the seventh falling edge of HSYNC.

The first HSYNC is at HCOUNT 175 after reset.

# Vertical signals




FBREF is measured at pin 22. At U186:3 FBREF is delayed by 22ns going high and 12ns going low.

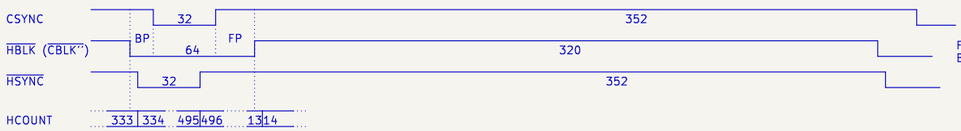
# Horizontal and vertical synch timing diagrams

Pixel clock CLK2 = 18.432MHz / 3 = 6.144MHz

Horizontal lines
HSYNC freq = 6.144MHz / 384 = 16kHz
HSYNC period = 1 / 16kHz = 62.5us
Pixels / line: 384
Active pixels: 320
Blank pixels: 64

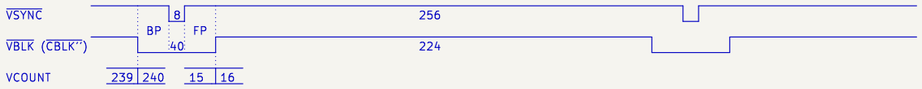
Vertical lines
VSYNC freq = 16kHz / 264 = 60.606060Hz
VSYNC period = 1 / f = 264 / 16kHz = 16.5ms
scanlines / frame: 264
Active lines: 224
Blank lines: 40

The numbers in the HSYNC and HBLK diagrams are HSYNC cycles.
All edges are synchronised to the rising edge of CLK2.




Front Porch (FP) 24 px,
Back Porch (BP) 8 px

The numbers in the VSYNC and VBLK diagrams are HSYNC cycles.
All edges are synchronised to the falling edge of HSYNC.




Front Porch (FP) and
Back Porch (BP) 16 HSYNC cycles.

HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]
VCOUNT is bits [128V, 64V, 32V, 16V, 8V, 4V, 2V, 1V]

CBLK'' is at the output of color mixer 007327.
CBLK' is shifted inside the 007327 one pixel clock.

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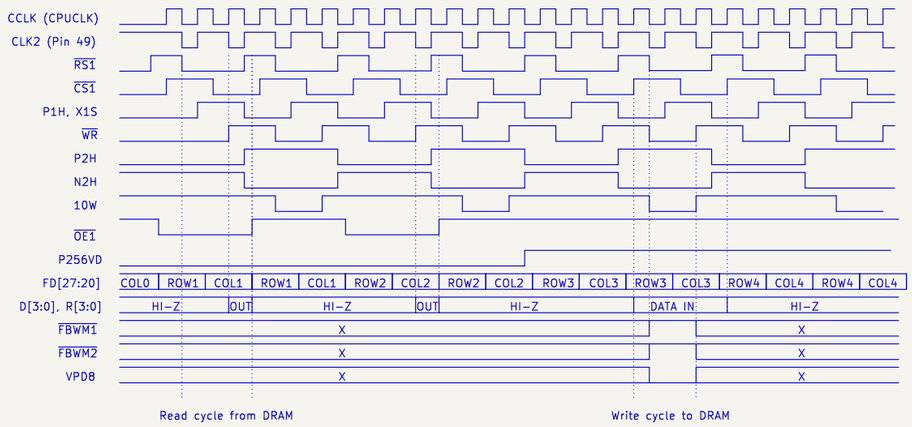
**Konami GX687 / GX785**

Sheet: /Timing diagrams/
File: timing_diagrams.kicad_sch

**Title: Twin 16**

| | | |
|---|---|---|
| Size: A3 | Date: 2024-09-08 | Rev: |
| KiCad E.D.A. 8.0.9 | | Id: 15/17 |




The same row and column addresses are repeated twice.
One for read cycle and the other for write cycles.

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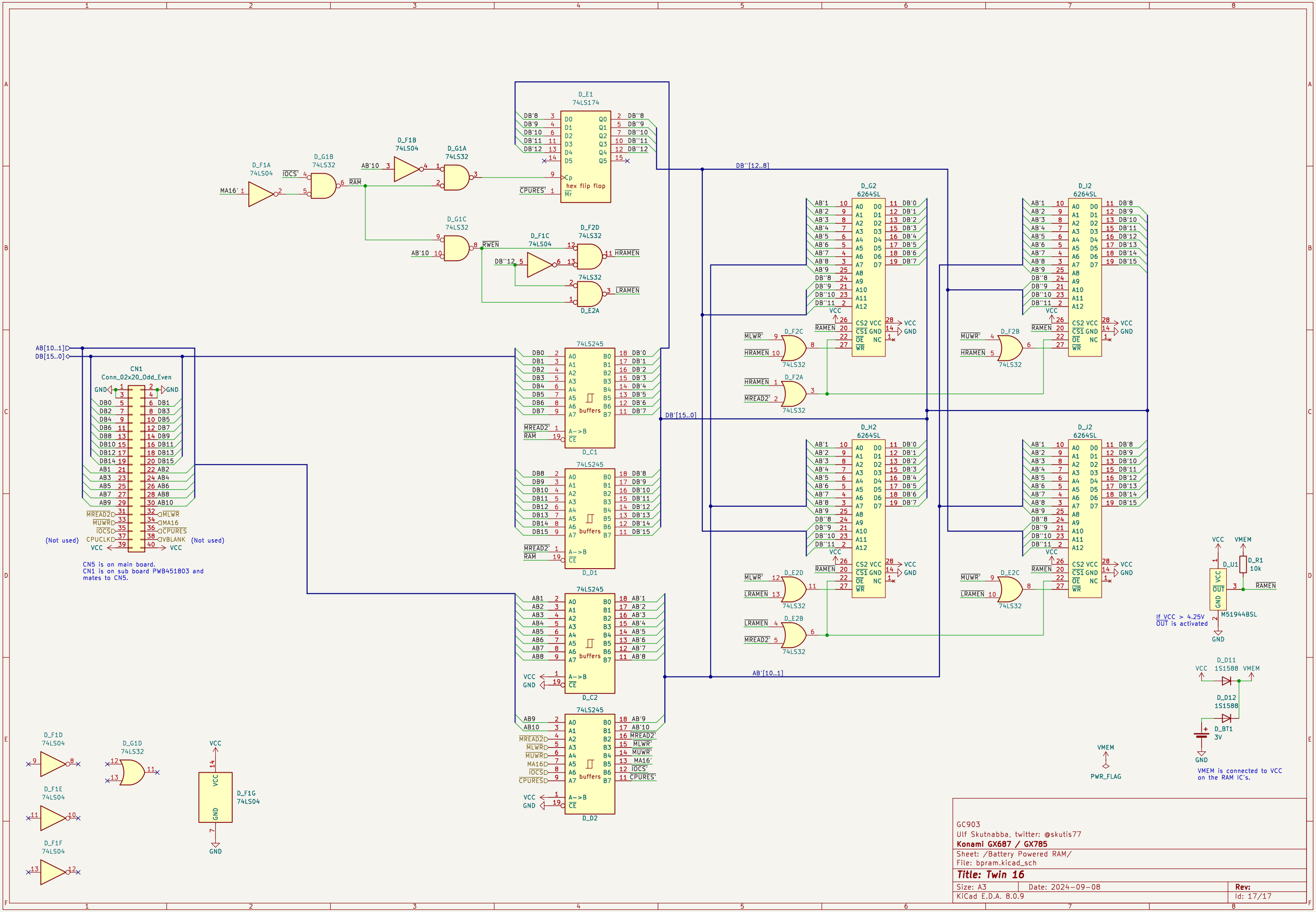
**Konami GX687 / GX785**

Sheet: /Sprite timing diagrams/
File: sprite_timing_diagrams.kicad_sch

***Title: Twin 16***

| | | |
|---|---|---|
| Size: A3 | Date: 2024-09-08 | **Rev:** |
| KiCad E.D.A. 8.0.9 | | Id: 16/17 |


D_E1
74LS174
D_F1A
74LS04
D_G1B
74LS32
D_F1B
74LS04
D_G1A
74LS32
D_G1C
74LS32
D_F1C
74LS04
D_F2D
74LS32
D_E2A
D_G2
6264SL
D_I2
6264SL
D_F2C
D_F2B
D_F2A
D_H2
6264SL
D_J2
6264SL
D_E2D
D_E2C
D_E2B
CN1
Conn_02x20_Odd_Even
CN5 is on main board.
CN1 is on sub board PWB451803 and
mates to CN5.
74LS245
D_C1
D_D1
D_C2
D_D2
D_F1D
74LS04
D_G1D
74LS32
D_F1E
74LS04
D_F1F
74LS04
D_F1G
74LS04
M51944BSL
If VCC > 4.25V
OUT is activated
D_D11
1S1588
D_D12
1S1588
D_BT1
3V
VMEM is connected to VCC
on the RAM IC's.
PWR_FLAG
GC903
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Konami GX687 / GX785
Sheet: /Battery Powered RAM/
File: bpram.kicad_sch
Title: Twin 16
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 17/17