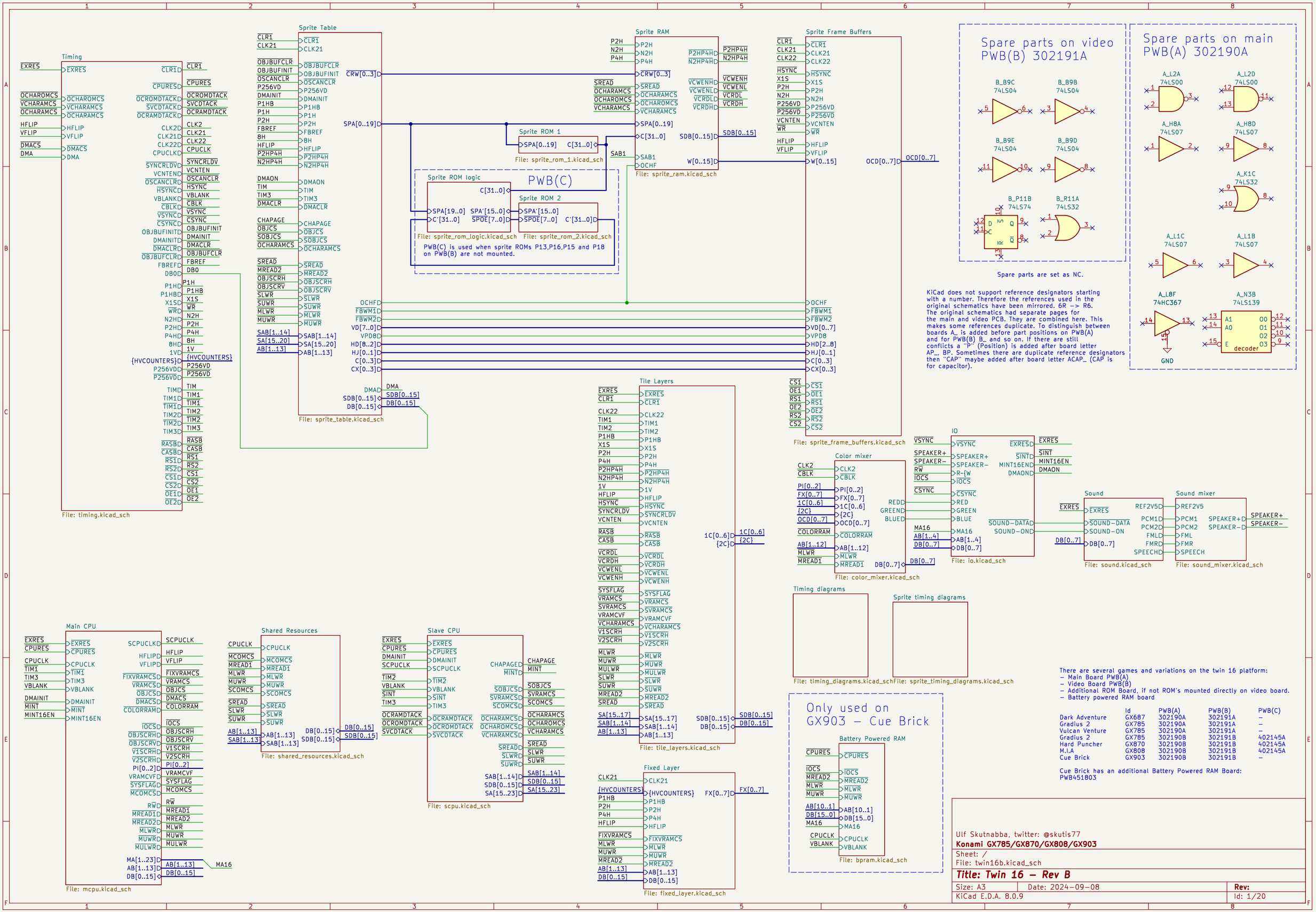
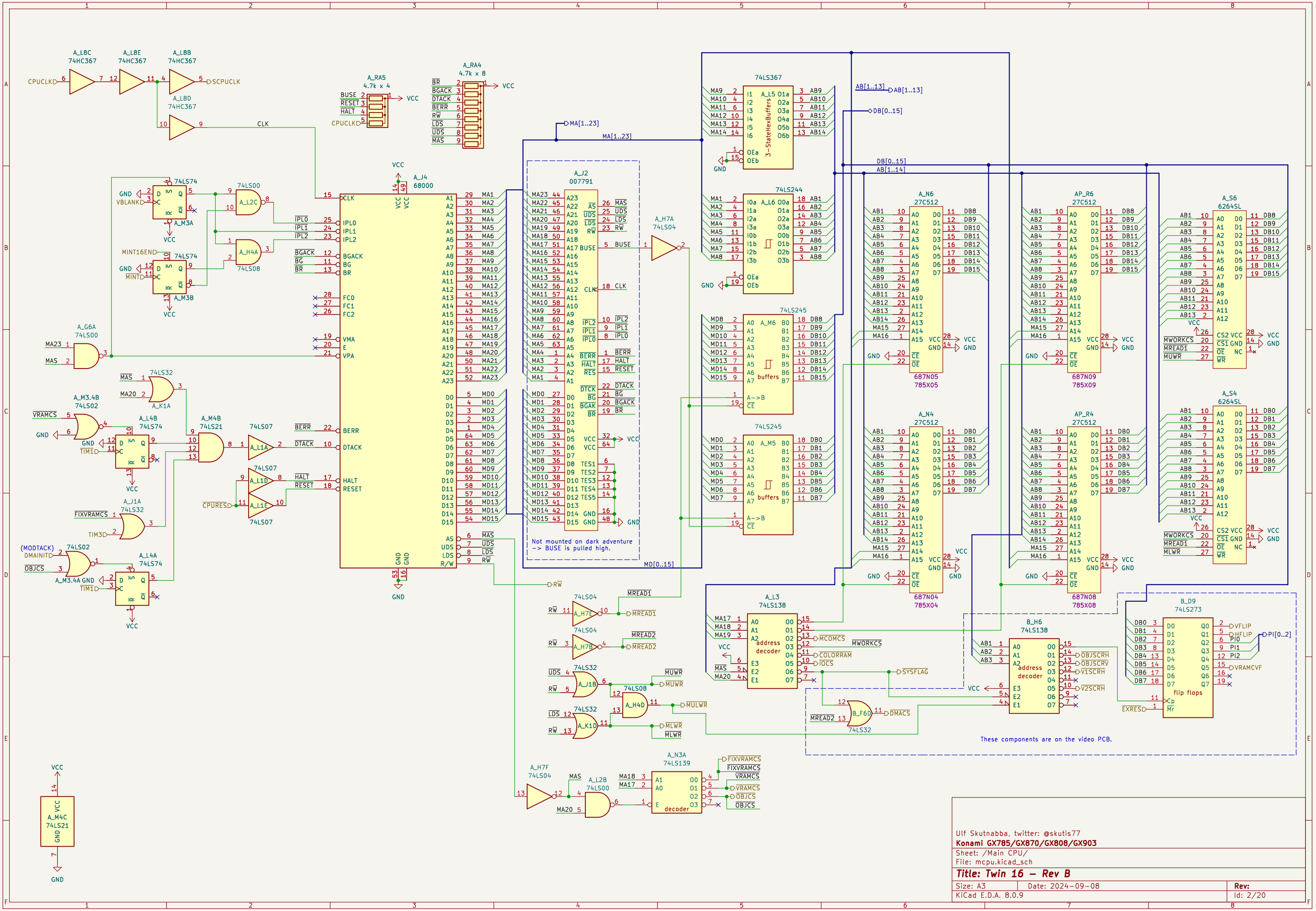

Timing
File: timing.kicad_sch
Sprite Table
File: sprite_table.kicad_sch
Sprite RAM
File: sprite_ram.kicad_sch
Sprite ROM 1
File: sprite_rom_1.kicad_sch
Sprite ROM logic
File: sprite_rom_logic.kicad_sch
Sprite ROM 2
File: sprite_rom_2.kicad_sch
PWB(C)
PWB(C) is used when sprite ROMs P13,P16,P15 and P18 on PWB(B) are not mounted.
Sprite Frame Buffers
File: sprite_frame_buffers.kicad_sch
Spare parts on video PWB(B) 302191A
Spare parts are set as NC.
Spare parts on main PWB(A) 302190A
KiCad does not support reference designators starting with a number. Therefore the references used in the original schematics have been mirrored. 6R -> R6. The original schematics had separate pages for the main and video PCB. They are combined here. This makes some references duplicate. To distinguish between boards A_ is added before part positions on PWB(A) and for PWB(B) B_ and so on. If there are still conflicts a "P" (Position) is added after board letter AP_, BP. Sometimes there are duplicate reference designators then "CAP" maybe added after board letter ACAP_ (CAP is for capacitor).
Tile Layers
File: tile_layers.kicad_sch
Color mixer
File: color_mixer.kicad_sch
IO
File: io.kicad_sch
Sound
File: sound.kicad_sch
Sound mixer
File: sound_mixer.kicad_sch
Timing diagrams
File: timing_diagrams.kicad_sch
Sprite timing diagrams
File: sprite_timing_diagrams.kicad_sch
Main CPU
File: mcpu.kicad_sch
Shared Resources
File: shared_resources.kicad_sch
Slave CPU
File: scpu.kicad_sch
Fixed Layer
File: fixed_layer.kicad_sch
Only used on GX903 – Cue Brick
Battery Powered RAM
File: bpram.kicad_sch
There are several games and variations on the twin 16 platform:
– Main Board PWB(A)
– Video Board PWB(B)
– Additional ROM Board, if not ROM's mounted directly on video board.
– Battery powered RAM board
Id PWB(A) PWB(B) PWB(C)
Dark Adventure GX687 302190A 302191A –
Gradius 2 GX785 302190A 302191A –
Vulcan Venture GX785 302190A 302191A –
Gradius 2 GX785 302190B 302191B 402145A
Hard Puncher GX870 302190B 302191B 402145A
M.I.A GX808 302190B 302191B 402145A
Cue Brick GX903 302190B 302191B –
Cue Brick has an additional Battery Powered RAM Board: PWB451803
Ulf Skutnabba, twitter: @skutis77
Konami GX785/GX870/GX808/GX903
Sheet: /
File: twin16b.kicad_sch
Title: Twin 16 – Rev B
Size: A3
Date: 2024-09-08
KiCad E.D.A. 8.0.9
Rev:
Id: 1/20



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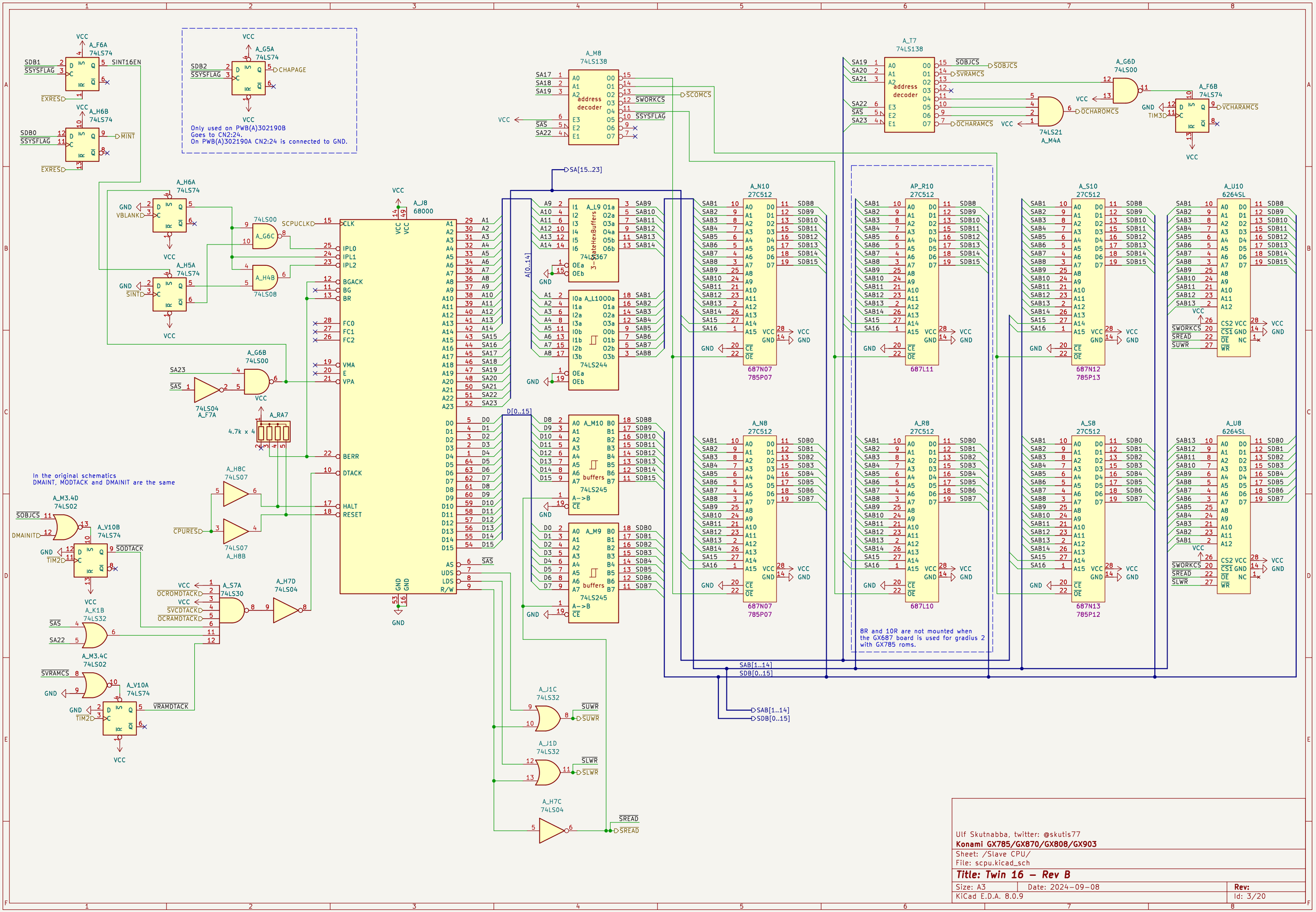
Konami GX785/GX870/GX808/GX903

Sheet: /Main CPU/

File: mcpu.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 2/20



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Konami GX785/GX870/GX808/GX903

Sheet: /Slave CPU/

File: scpu.kicad_sch

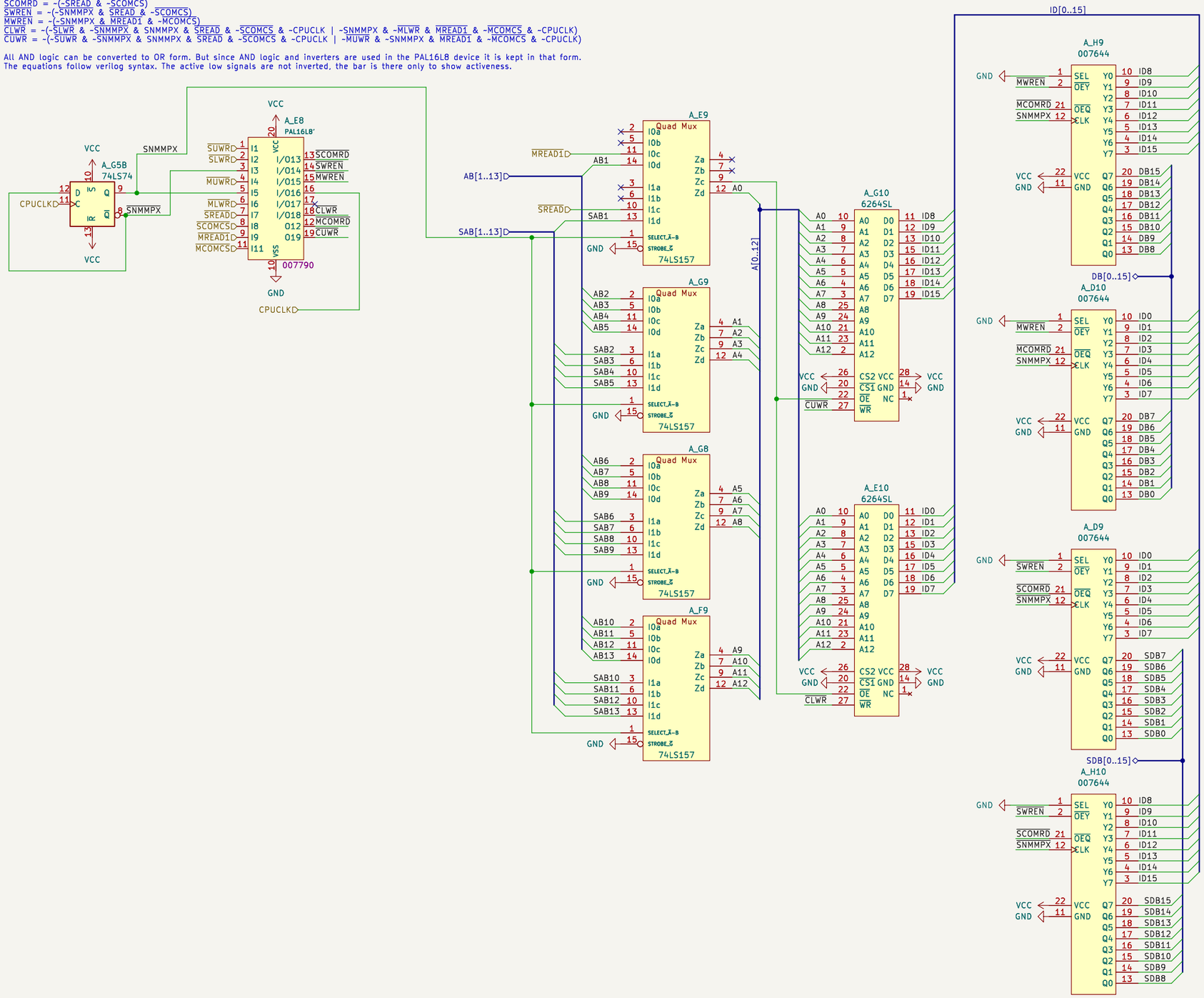
Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 3/20

Konami 007790

$\overline{MCOMRD}$ = ~($\overline{MREAD1}$ & ~$\overline{MCOMCS}$) = $\overline{MREAD1}$ | $\overline{MCOMCS}$
$\overline{SCOMRD}$ = ~($\overline{SREAD}$ & ~$\overline{SCOMCS}$)
$\overline{SWREN}$ = ~(~SNMMPX & $\overline{SREAD}$ & ~$\overline{SCOMCS}$)
$\overline{MWREN}$ = ~(~SNMMPX & $\overline{MREAD1}$ & ~$\overline{MCOMCS}$)
$\overline{CLWR}$ = ~(~$\overline{SLWR}$ & ~SNMMPX & SNMMPX & $\overline{SREAD}$ & ~$\overline{SCOMCS}$ & ~CPUCLK | ~SNMMPX & ~$\overline{MLWR}$ & $\overline{MREAD1}$ & ~$\overline{MCOMCS}$ & ~CPUCLK)
$\overline{CUWR}$ = ~(~$\overline{SUWR}$ & ~SNMMPX & SNMMPX & $\overline{SREAD}$ & ~$\overline{SCOMCS}$ & ~CPUCLK | ~$\overline{MUWR}$ & ~SNMMPX & $\overline{MREAD1}$ & ~$\overline{MCOMCS}$ & ~CPUCLK)

All AND logic can be converted to OR form. But since AND logic and inverters are used in the PAL16L8 device it is kept in that form.
The equations follow verilog syntax. The active low signals are not inverted, the bar is there only to show activeness.



This is from jammarcade.net

Pin 1 = SEL – changes whether the Q outputs require a rising edge clock or not.
Pin 2 = OEY – Output enable for the Y outputs else they are inputs. Active LOW
Pin 21 = OEQ – Output enable for the Q (clocked) outputs else they are inputs. Active LOW
Pin 12 = CLK – Clock input

Pins 3–10 = Y outputs – normal outputs. If OEY is LOW these pins become outputs
mirroring the state of the Q input pins. SEL and CLK pins are not used in this mode.

Pins 13–20 = Q outputs – clocked outputs. If OEQ is LOW these pins become outputs.
If SEL is HIGH and CLK is HIGH these outputs will mirror the state of the Y inputs.
If SEL is LOW then the outputs will only change state on a rising edge CLK.

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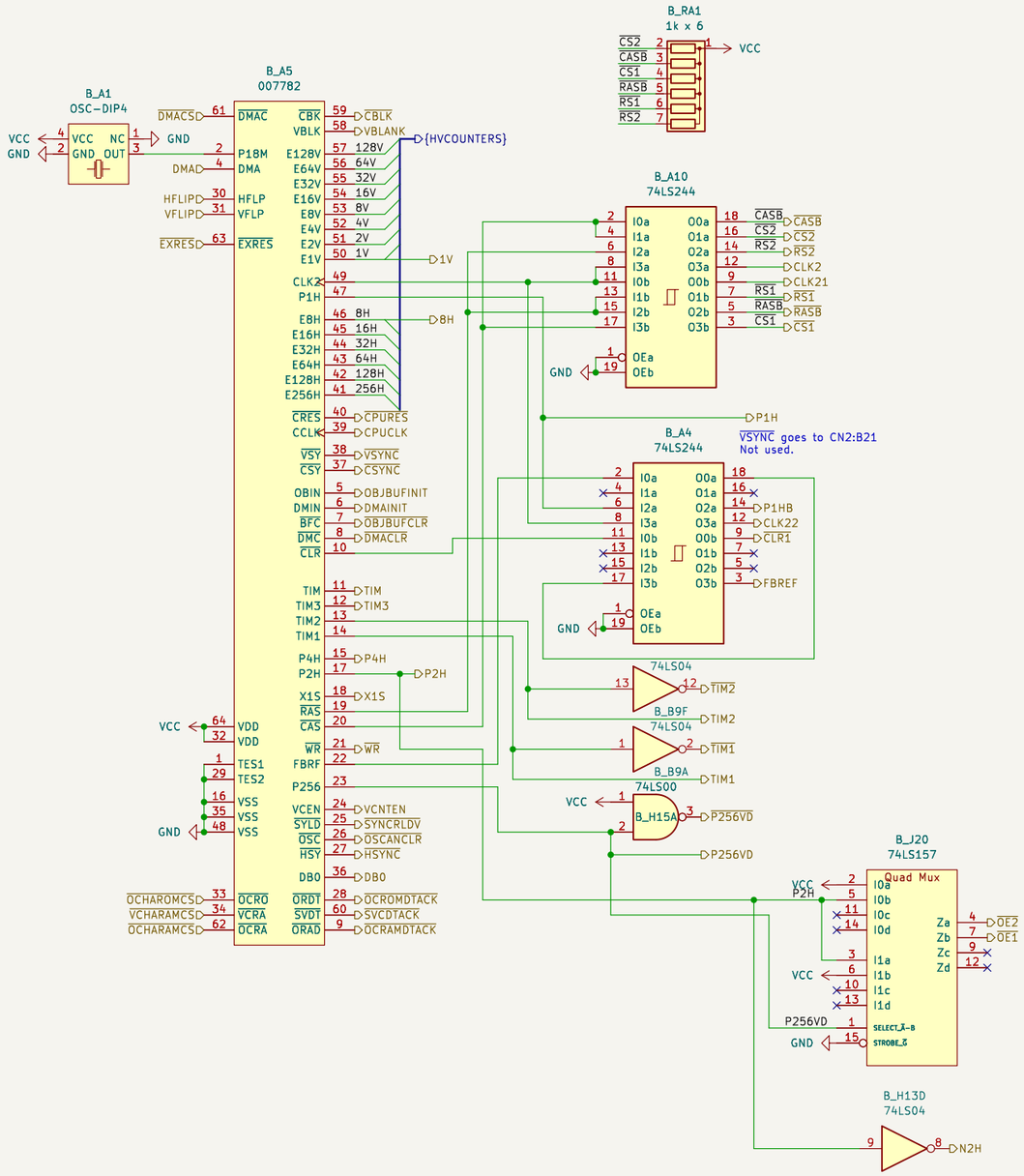
Konami GX785/GX870/GX808/GX903

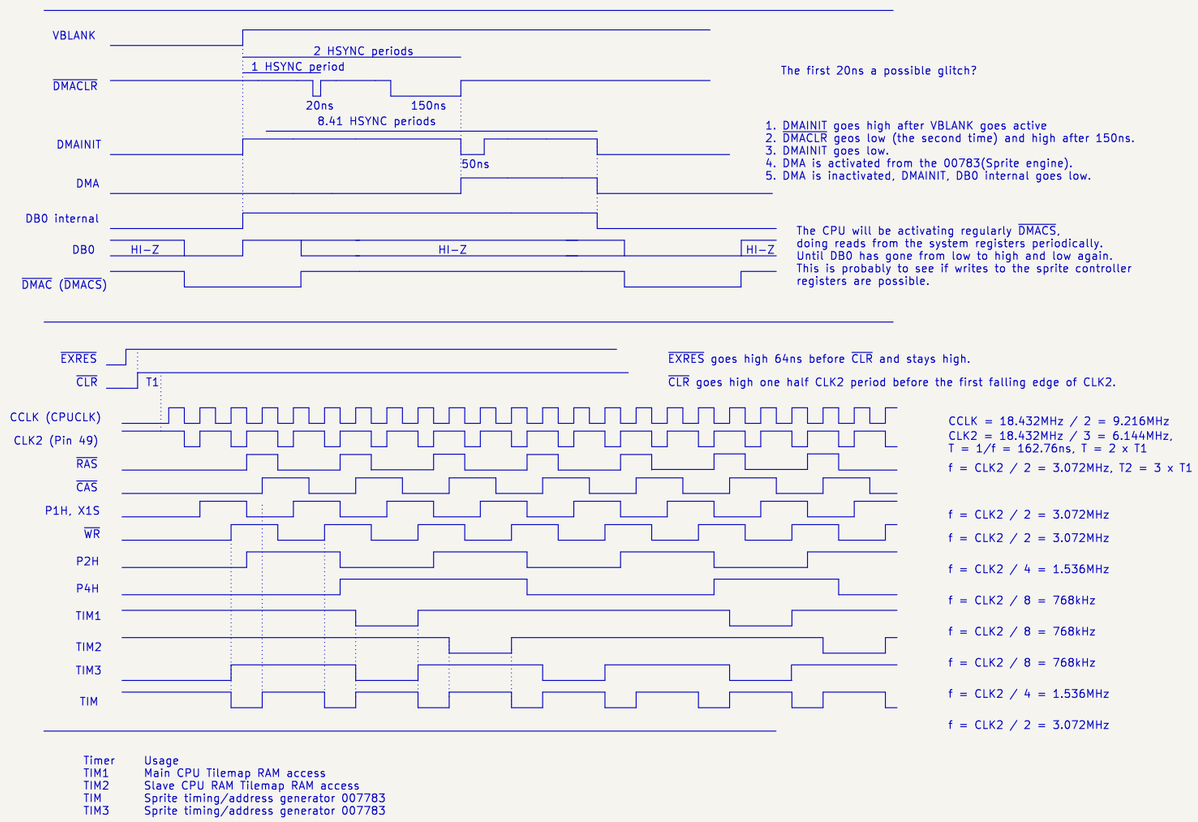
Sheet: /Shared Resources/
File: shared_resources.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 4/20

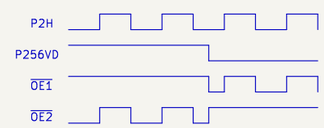


DMA Synchronization

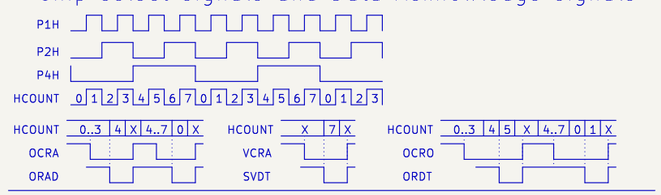


Timer	Usage
TIM1	Main CPU Tilemap RAM access
TIM2	Slave CPU RAM Tilemap RAM access
TIM	Sprite timing/address generator 007783
TIM3	Sprite timing/address generator 007783

Output enables active vs. part of frame buffer active



Chip select signals and Data Acknowledge signals



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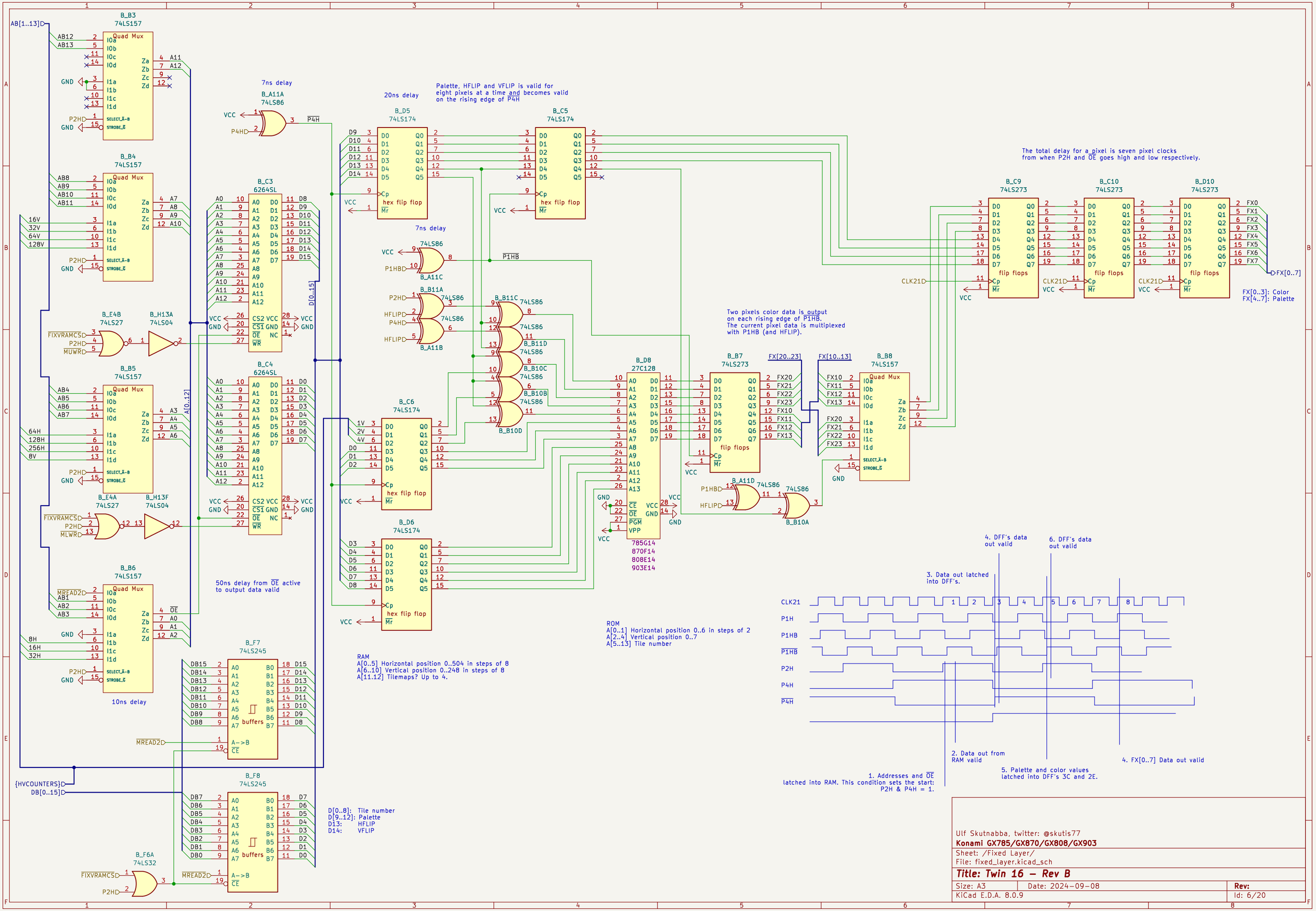
Konami GX785/GX870/GX808/GX903

Sheet: /Timing/
File: timing.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 5/20



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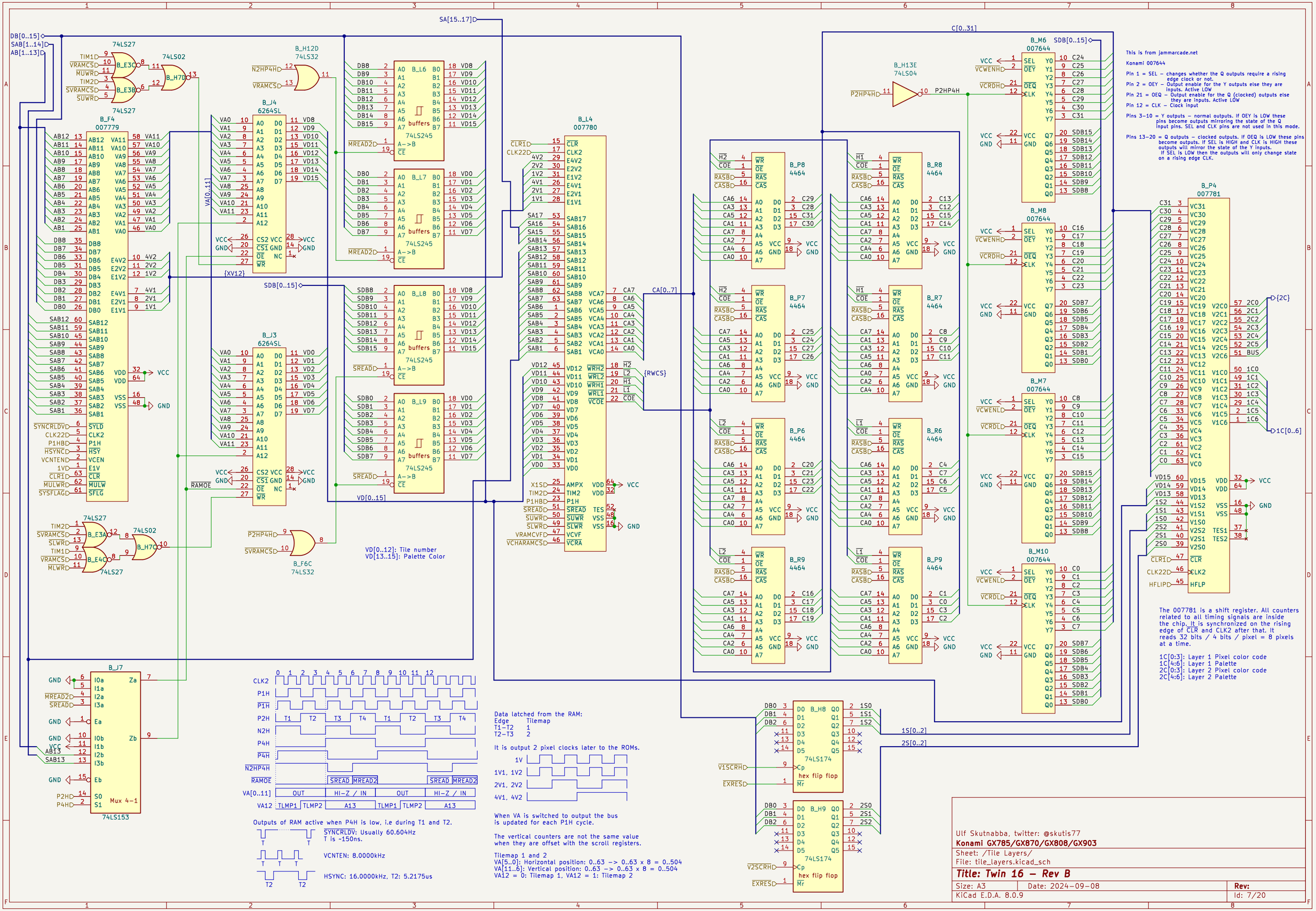
Konami GX785/GX870/GX808/GX903

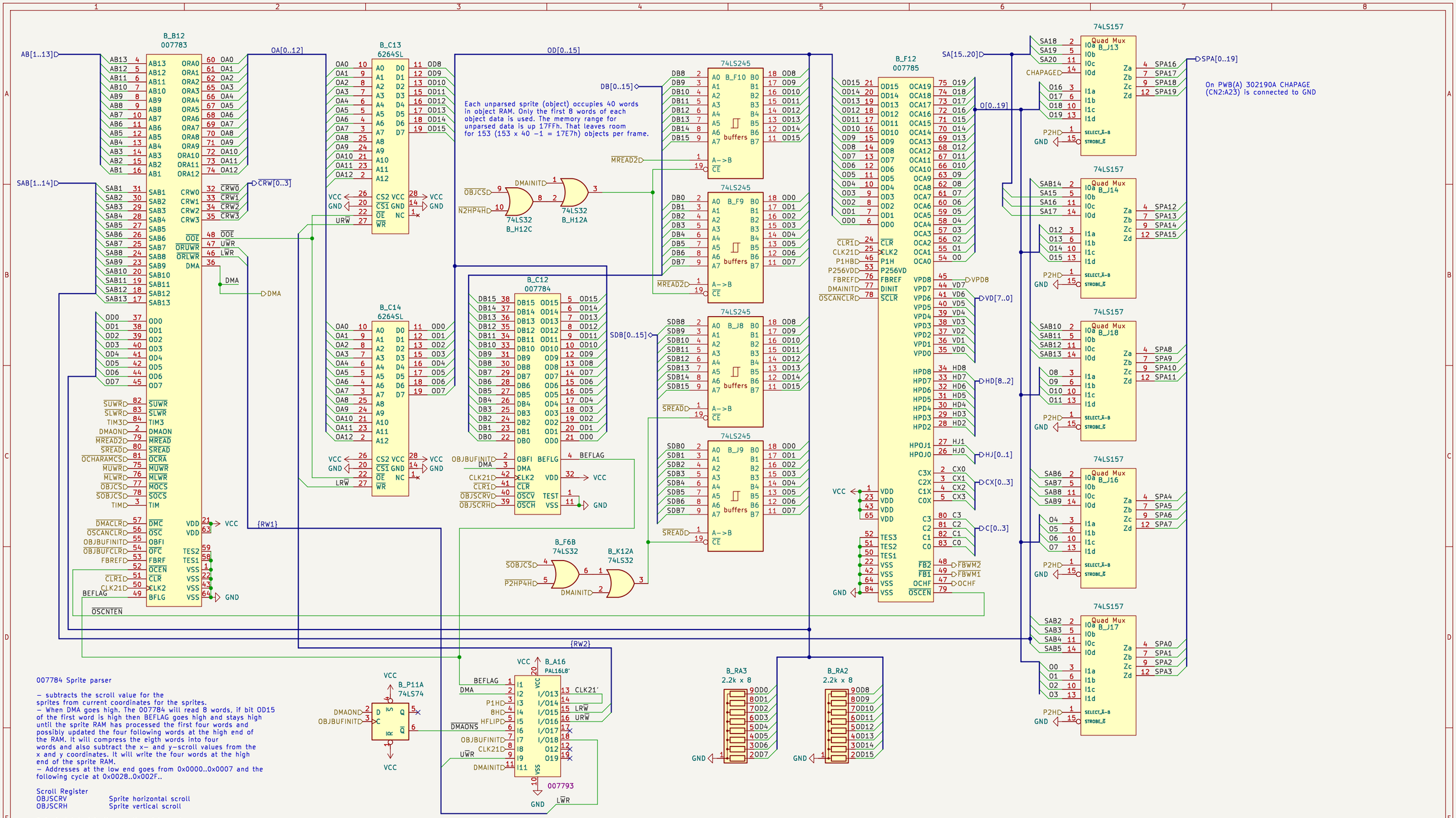
Sheet: /Fixed Layer/

File: fixed_layer.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	Rev:
KiCad E.D.A. 8.0.9		Id: 6/20


This is from jammarcade.net
Konami 007644
Pin 1 = SEL – changes whether the Q outputs require a rising edge clock or not.
Pin 2 = OEY – Output enable for the Y outputs else they are inputs. Active LOW
Pin 21 = OEQ – Output enable for the Q (clocked) outputs else they are inputs. Active LOW
Pin 12 = CLK – Clock input
Pins 3–10 = Y outputs – normal outputs. If OEY is LOW these pins become outputs mirroring the state of the Q input pins. SEL and CLK pins are not used in this mode.
Pins 13–20 = Q outputs – clocked outputs. If OEQ is LOW these pins become outputs. If SEL is HIGH and CLK is HIGH these outputs will mirror the state of the Y inputs. If SEL is LOW then the outputs will only change state on a rising edge CLK.
The 007781 is a shift register. All counters related to all timing signals are inside the chip. It is synchronized on the rising edge of CLR and CLK2 after that. It reads 32 bits / 4 bits / pixel = 8 pixels at a time.
1C[0:3]: Layer 1 Pixel color code
1C[4:6]: Layer 1 Palette
2C[0:3]: Layer 2 Pixel color code
2C[4:6]: Layer 2 Palette
VD[0..12]: Tile number
VD[13..15]: Palette Color
Data latched from the RAM:
Edge Tilemap
T1–T2 1
T2–T3 2
It is output 2 pixel clocks later to the ROMs.
When VA is switched to output the bus is updated for each P1H cycle.
The vertical counters are not the same value when they are offset with the scroll registers.
Tilemap 1 and 2
VA[5..0]: Horizontal position: 0..63 –> 0..63 x 8 = 0..504
VA[11..6]: Vertical position: 0..63 –> 0..63 x 8 = 0..504
VA12 = 0: Tilemap 1, VA12 = 1: Tilemap 2
Outputs of RAM active when P4H is low, i.e during T1 and T2.
SYNCRLDV: Usually 60.604Hz
T is ~150ns.
VCNTEN: 8.0000kHz
HSYNC: 16.0000kHz, T2: 5.2175us
Ulf Skutnabba, twitter: @skutis77
Konami GX785/GX870/GX808/GX903
Sheet: /Tile Layers/
File: tile_layers.kicad_sch
Title: Twin 16 – Rev B
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 7/20



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Konami GX785/GX870/GX808/GX903

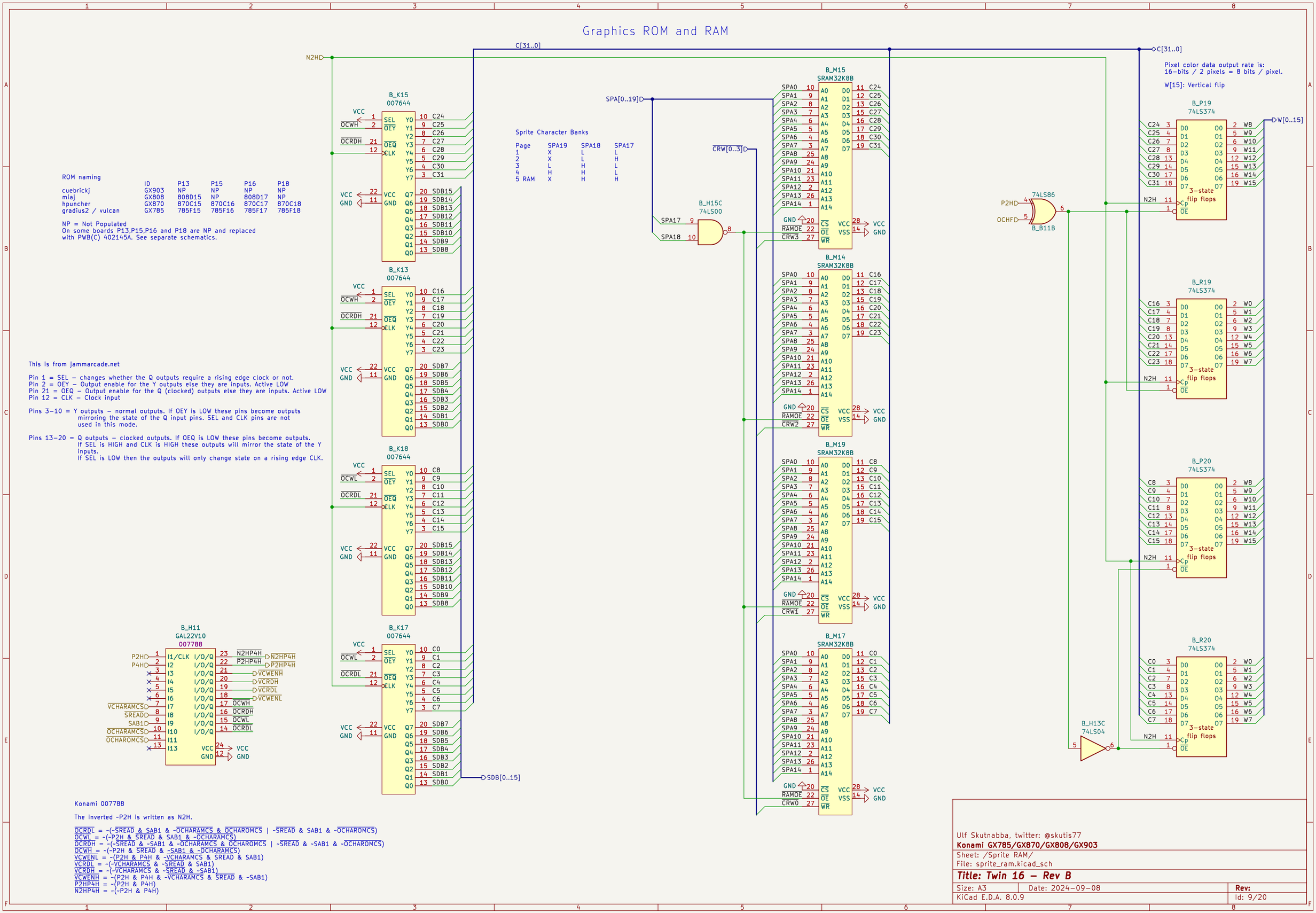
Sheet: /Sprite Table/

File: sprite_table.kicad_sch

Title: Twin 16 − Rev B

Size: A3	Date: 2024−09−08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 8/20

Graphics ROM and RAM



ROM naming

	ID	P13	P15	P16	P18
cuebrickj	GX903	NP	NP	NP	NP
miaj	GX808	808D15	NP	808D17	NP
hpuncher	GX870	870C15	870C16	870C17	870C18
gradius2 / vulcan	GX785	785F15	785F16	785F17	785F18

NP = Not Populated
On some boards P13,P15,P16 and P18 are NP and replaced with PWB(C) 402145A. See separate schematics.

Sprite Character Banks

Page	SPA19	SPA18	SPA17
1	X	L	L
2	X	L	H
3	L	H	L
4	H	H	L
5 RAM	X	H	H

Pixel color data output rate is:
16-bits / 2 pixels = 8 bits / pixel.

W[15]: Vertical flip

This is from jammarcade.net

Pin 1 = SEL – changes whether the Q outputs require a rising edge clock or not.
Pin 2 = OEY – Output enable for the Y outputs else they are inputs. Active LOW
Pin 21 = OEQ – Output enable for the Q (clocked) outputs else they are inputs. Active LOW
Pin 12 = CLK – Clock input

Pins 3–10 = Y outputs – normal outputs. If OEY is LOW these pins become outputs mirroring the state of the Q input pins. SEL and CLK pins are not used in this mode.

Pins 13–20 = Q outputs – clocked outputs. If OEQ is LOW these pins become outputs. If SEL is HIGH and CLK is HIGH these outputs will mirror the state of the Y inputs.
If SEL is LOW then the outputs will only change state on a rising edge CLK.

Konami 007788

The inverted ~P2H is written as N2H.

$\overline{OCRDL}$ = ~(~$\overline{SREAD}$ & SAB1 & ~$\overline{OCHARAMCS}$ & $\overline{OCHAROMCS}$ | ~$\overline{SREAD}$ & SAB1 & ~$\overline{OCHAROMCS}$)
$\overline{OCWL}$ = ~(~P2H & $\overline{SREAD}$ & SAB1 & ~$\overline{OCHARAMCS}$)
$\overline{OCRDH}$ = ~(~$\overline{SREAD}$ & ~SAB1 & ~$\overline{OCHARAMCS}$ & $\overline{OCHAROMCS}$ | ~$\overline{SREAD}$ & ~SAB1 & ~$\overline{OCHAROMCS}$)
$\overline{OCWH}$ = ~(~P2H & $\overline{SREAD}$ & ~SAB1 & ~$\overline{OCHARAMCS}$)
$\overline{VCWENL}$ = ~(P2H & P4H & ~$\overline{VCHARAMCS}$ & $\overline{SREAD}$ & SAB1)
$\overline{VCRDL}$ = ~(~$\overline{VCHARAMCS}$ & ~$\overline{SREAD}$ & SAB1)
$\overline{VCRDH}$ = ~(~$\overline{VCHARAMCS}$ & ~$\overline{SREAD}$ & ~SAB1)
$\overline{VCWENH}$ = ~(P2H & P4H & ~$\overline{VCHARAMCS}$ & $\overline{SREAD}$ & ~SAB1)
$\overline{P2HP4H}$ = ~(P2H & P4H)
$\overline{N2HP4H}$ = ~(~P2H & P4H)

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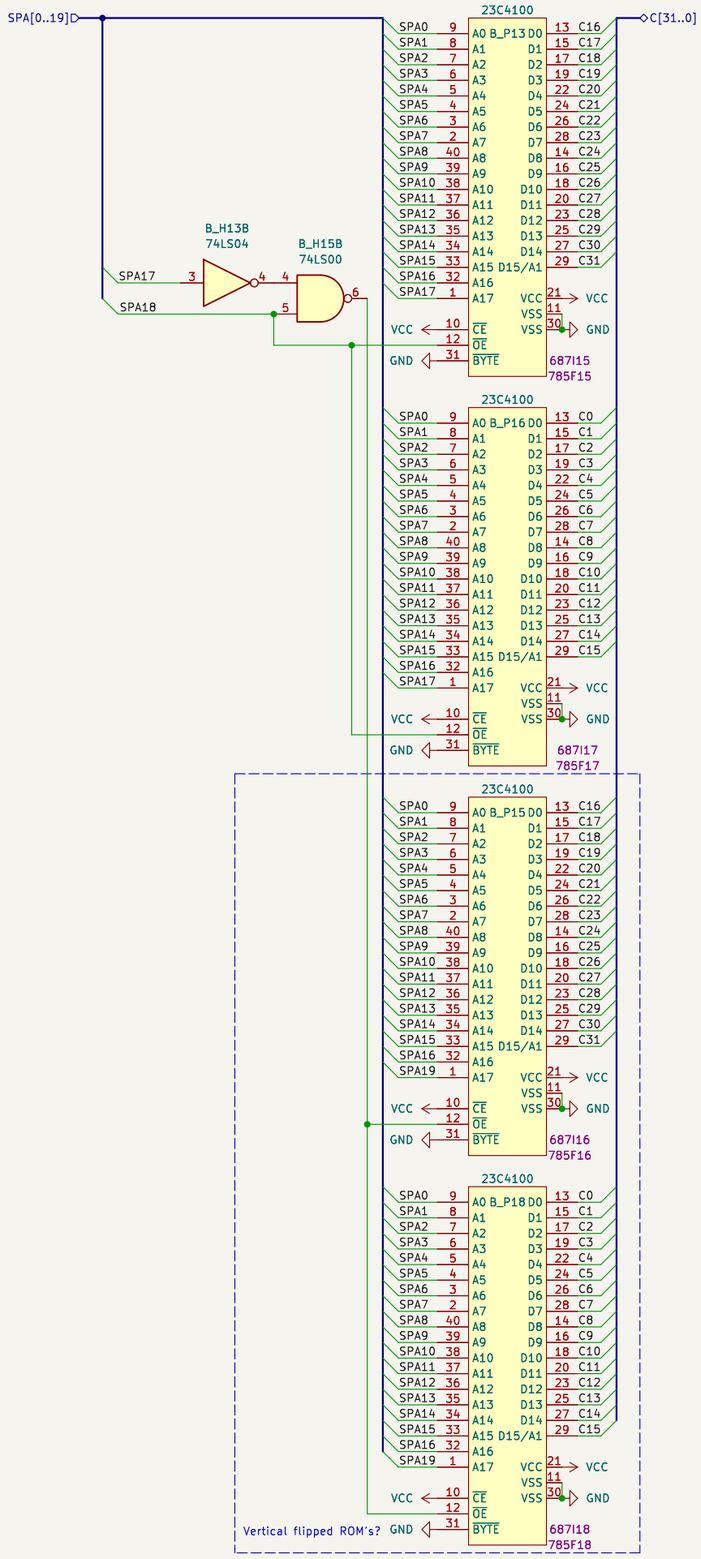
Konami GX785/GX870/GX808/GX903

Sheet: /Sprite RAM/
File: sprite_ram.kicad_sch

Title: Twin 16 – Rev B

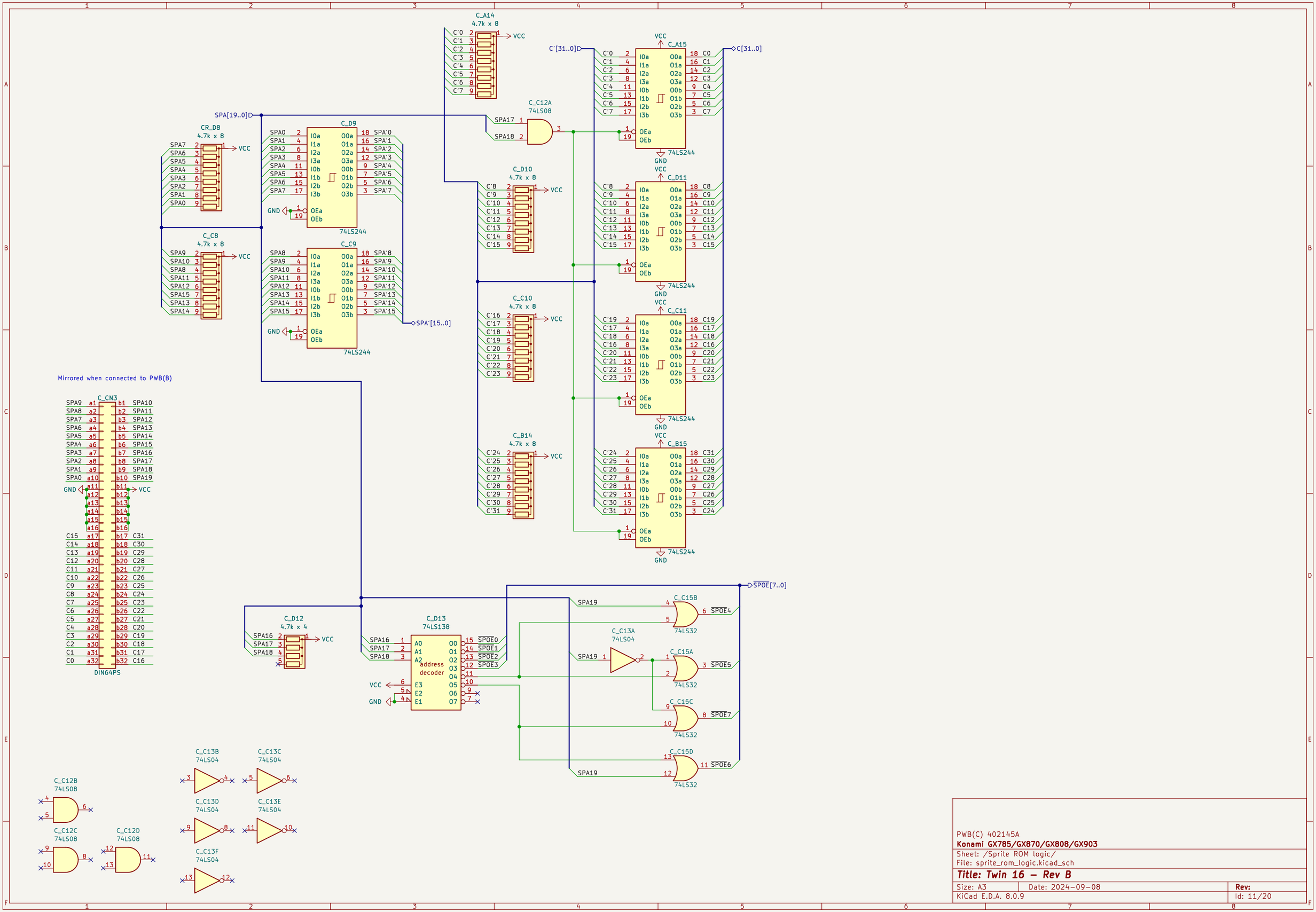
Size: A3	Date: 2024-09-08	Rev:
KiCad E.D.A. 8.0.9		Id: 9/20



Sheet: /Sprite ROM 1/
File: sprite_rom_1.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	Rev:
KiCad E.D.A. 8.0.9		Id: 10/20



PWB(C) 402145A

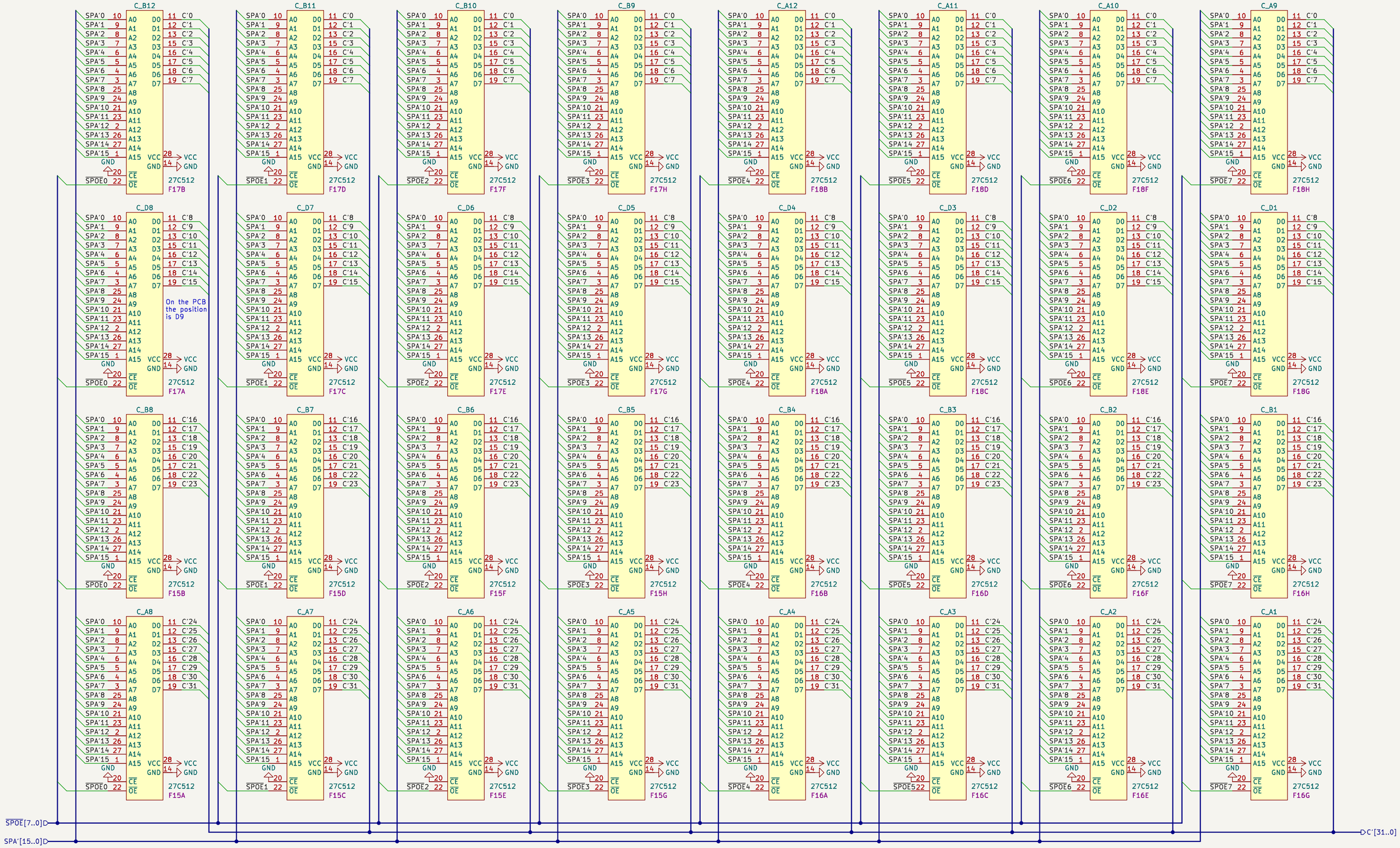
Konami GX785/GX870/GX808/GX903

Sheet: /Sprite ROM logic/

File: sprite_rom_logic.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 11/20



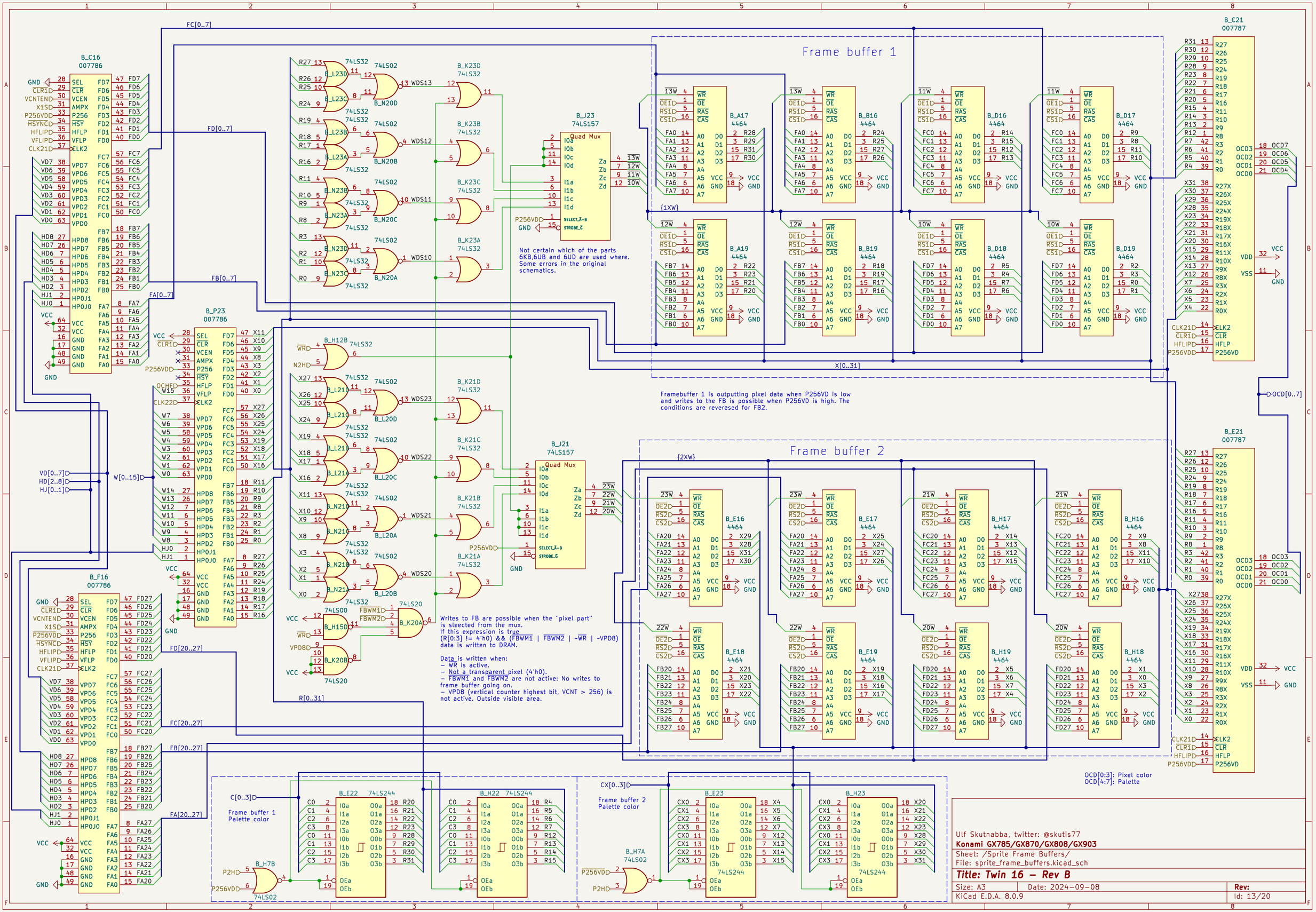
Konami GX785/GX870/GX808/GX903

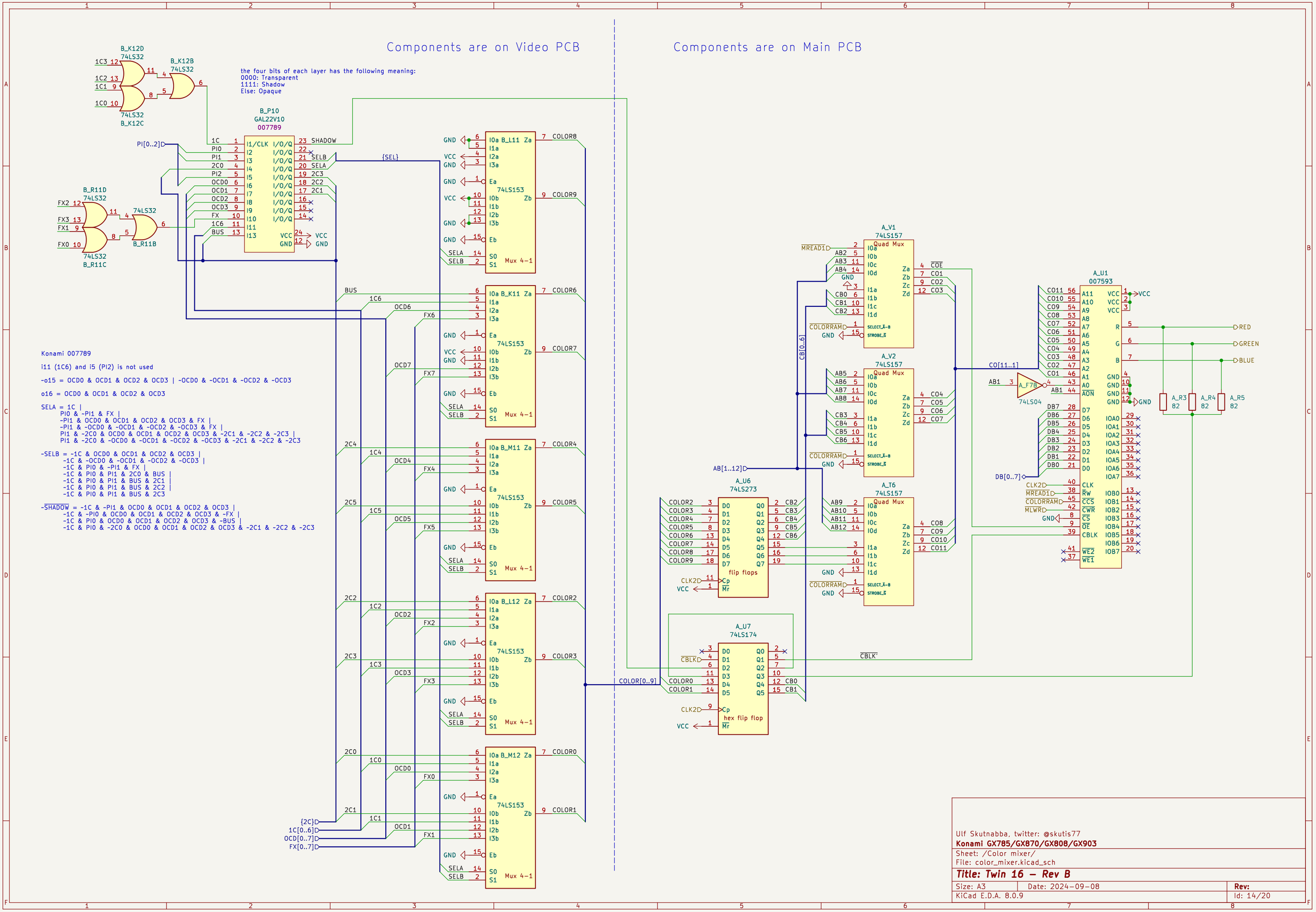
Sheet: /Sprite ROM 2/

File: sprite_rom_2.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 11/20


Frame buffer 1
Frame buffer 2
B_C16 007786
B_P23 007786
B_F16 007786
B_C21 007787
B_E21 007787
B_J23 74LS157
B_J21 74LS157
Quad Mux
B_A17 4464
B_A19 4464
B_B16 4464
B_B19 4464
B_D16 4464
B_D18 4464
B_D17 4464
B_D19 4464
B_E16 4464
B_E17 4464
B_E18 4464
B_E19 4464
B_H17 4464
B_H19 4464
B_H16 4464
B_H18 4464
B_E22 74LS244
B_H22 74LS244
B_E23 74LS244
B_H23 74LS244
B_H7A 74LS02
B_H7B 74LS02
B_H15D 74LS00
B_K20A 74LS20
B_K20B 74LS20
FC[0..7]
FD[0..7]
FB[0..7]
FA[0..7]
FD[20..27]
FC[20..27]
FB[20..27]
FA[20..27]
R[0..31]
X[0..31]
OCD[0..7]
VD[0..7]
HD[2..8]
HJ[0..1]
W[0..15]
C[0..3]
CX[0..3]
Frame buffer 1 Palette color
Frame buffer 2 Palette color
Not certain which of the parts 6KB,6UB and 6UD are used where. Some errors in the original schematics.
Framebuffer 1 is outputting pixel data when P256VD is low and writes to the FB is possible when P256VD is high. The conditions are reveresed for FB2.
Writes to FB are possible when the "pixel part" is sleected from the mux.
If this expression is true
(R[0:3] != 4'h0) && (FBWM1 | FBWM2 | -WR | -VPD8)
data is written to DRAM.
Data is written when:
– WR is active.
– Not a transparent pixel (4'h0).
– FBWM1 and FBWM2 are not active: No writes to frame buffer going on.
– VPD8 (vertical counter highest bit, VCNT > 256) is not active. Outside visible area.
OCD[0:3]: Pixel color
OCD[4:7]: Palette
Ulf Skutnabba, twitter: @skutis77
Konami GX785/GX870/GX808/GX903
Sheet: /Sprite Frame Buffers/
File: sprite_frame_buffers.kicad_sch
Title: Twin 16 – Rev B
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 13/20


Components are on Video PCB
Components are on Main PCB
the four bits of each layer has the following meaning:
0000: Transparent
1111: Shadow
Else: Opaque
B_K12D 74LS32
B_K12B 74LS32
B_K12C 74LS32
B_P10 GAL22V10 007789
B_R11D 74LS32
B_R11B 74LS32
B_R11C 74LS32
B_L11 74LS153 Mux 4-1
B_K11 74LS153 Mux 4-1
B_M11 74LS153 Mux 4-1
B_L12 74LS153 Mux 4-1
B_M12 74LS153 Mux 4-1
A_V1 74LS157 Quad Mux
A_V2 74LS157 Quad Mux
A_T6 74LS157 Quad Mux
A_U6 74LS273 flip flops
A_U7 74LS174 hex flip flop
A_U1 007593
A_F7B 74LS04
A_R3 82
A_R4 82
A_R5 82
Konami 007789
i11 (1C6) and i5 (PI2) is not used
~o15 = OCD0 & OCD1 & OCD2 & OCD3 | ~OCD0 & ~OCD1 & ~OCD2 & ~OCD3
o16 = OCD0 & OCD1 & OCD2 & OCD3
SELA = 1C |
PI0 & ~PI1 & FX |
~PI1 & OCD0 & OCD1 & OCD2 & OCD3 & FX |
~PI1 & ~OCD0 & ~OCD1 & ~OCD2 & ~OCD3 & FX |
PI1 & ~2C0 & OCD0 & OCD1 & OCD2 & OCD3 & ~2C1 & ~2C2 & ~2C3 |
PI1 & ~2C0 & ~OCD0 & ~OCD1 & ~OCD2 & ~OCD3 & ~2C1 & ~2C2 & ~2C3
~SELB = ~1C & OCD0 & OCD1 & OCD2 & OCD3 |
~1C & ~OCD0 & ~OCD1 & ~OCD2 & ~OCD3 |
~1C & PI0 & ~PI1 & FX |
~1C & PI0 & PI1 & 2C0 & BUS |
~1C & PI0 & PI1 & BUS & 2C1 |
~1C & PI0 & PI1 & BUS & 2C2 |
~1C & PI0 & PI1 & BUS & 2C3
~SHADOW = ~1C & ~PI1 & OCD0 & OCD1 & OCD2 & OCD3 |
~1C & ~PI0 & OCD0 & OCD1 & OCD2 & OCD3 & ~FX |
~1C & PI0 & OCD0 & OCD1 & OCD2 & OCD3 & ~BUS |
~1C & PI0 & ~2C0 & OCD0 & OCD1 & OCD2 & OCD3 & ~2C1 & ~2C2 & ~2C3
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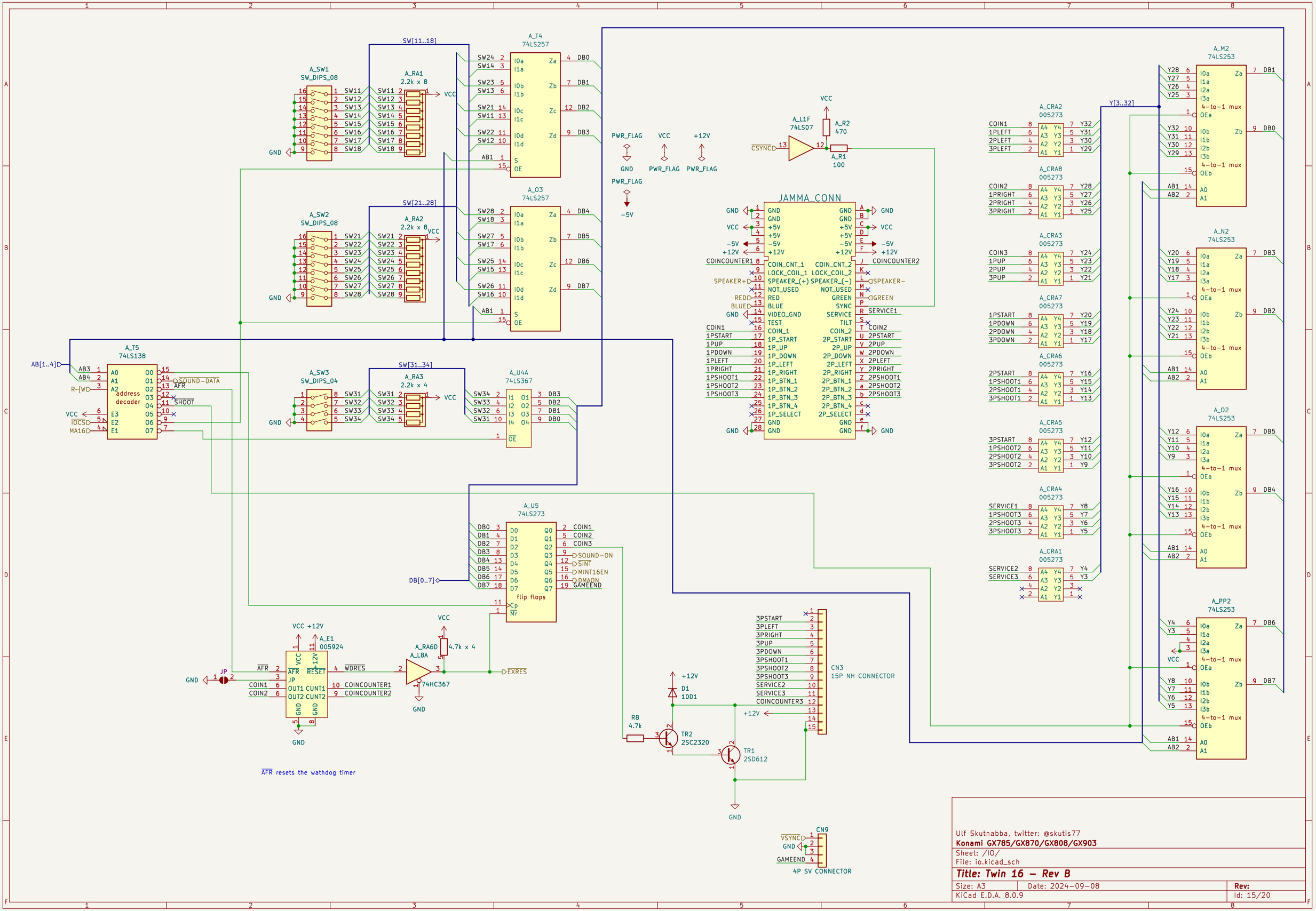
Konami GX785/GX870/GX808/GX903
Sheet: /Color mixer/
File: color_mixer.kicad_sch
Title: Twin 16 – Rev B
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 14/20



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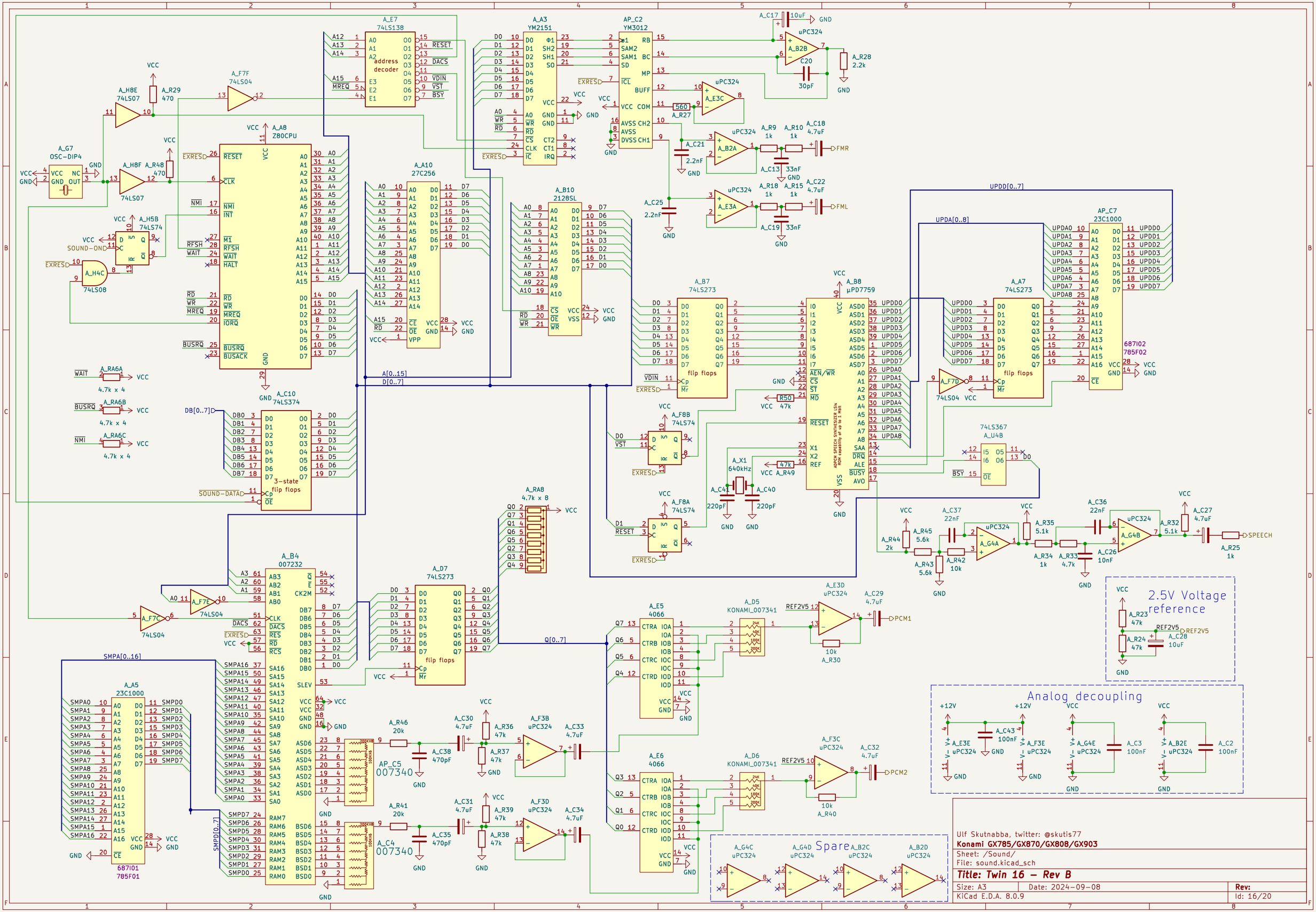
Sheet: /IO/

File: io.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 15/20



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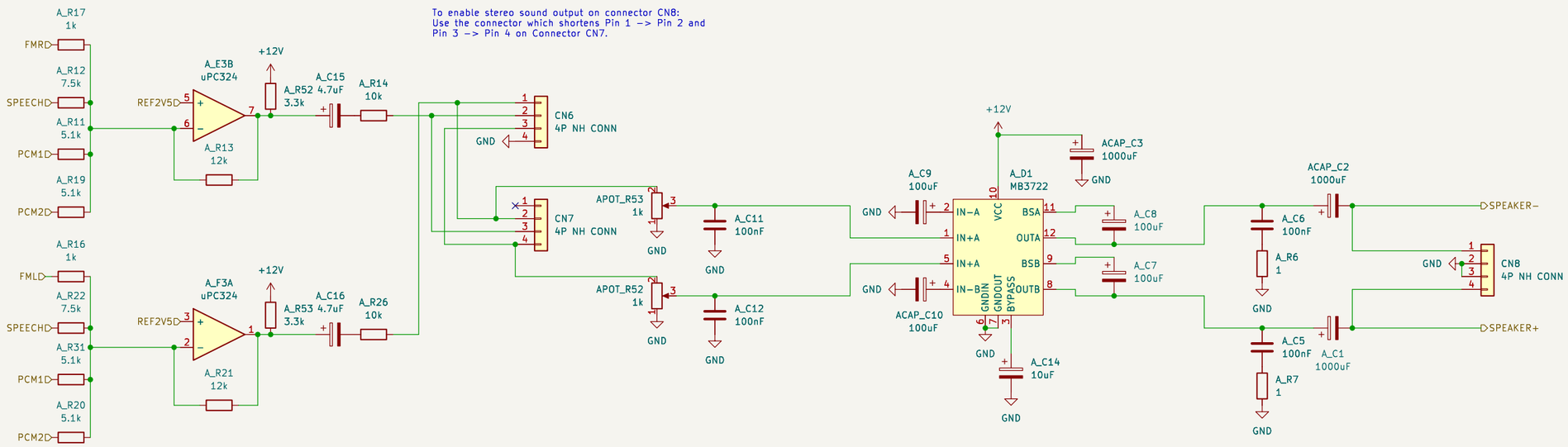
Sheet: /Sound/
File: sound.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	Rev:
KiCad E.D.A. 8.0.9		Id: 16/20



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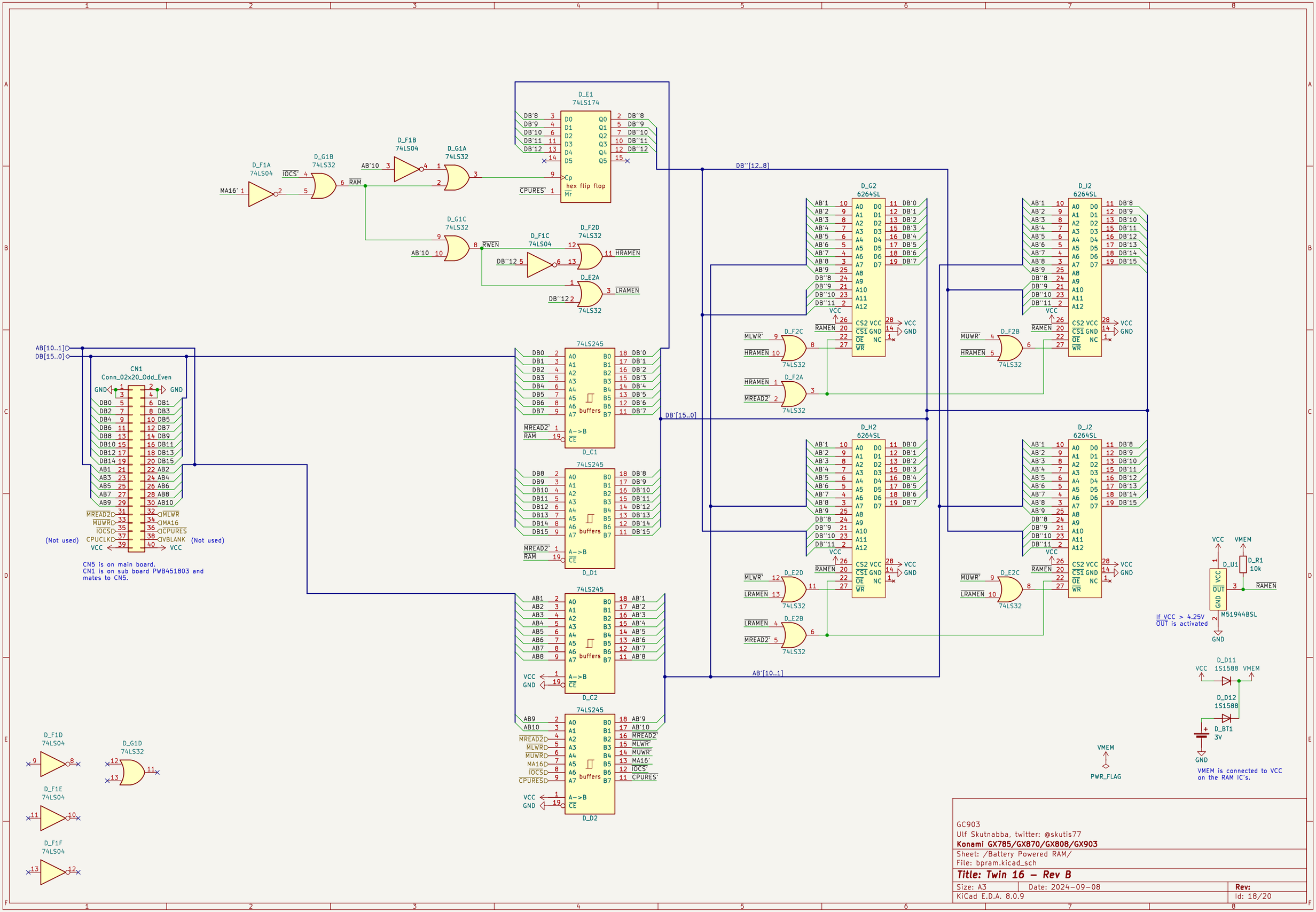
Sheet: /Sound mixer/

File: sound_mixer.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 17/20


D_E1
74LS174
D_F1A
74LS04
D_G1B
74LS32
D_F1B
74LS04
D_G1A
74LS32
D_G1C
74LS32
D_F1C
74LS04
D_F2D
74LS32
D_E2A
74LS32
MA16'
IOCS'
RAM
AB'10
RWEN
DB''12
HRAMEN
LRAMEN
CPURES'
DB''[12..8]
DB'[15..0]
AB'[10..1]
AB[10..1]
DB[15..0]
CN1
Conn_02x20_Odd_Even
(Not used)
CN5 is on main board.
CN1 is on sub board PWB451803 and
mates to CN5.
74LS245
buffers
D_C1
D_D1
D_C2
D_D2
D_G2
6264SL
D_I2
D_H2
D_J2
D_F2C
D_F2B
D_F2A
D_E2D
D_E2C
D_E2B
MLWR'
MUWR'
MREAD2'
D_F1D
D_G1D
D_F1E
D_F1F
VCC
VMEM
D_U1
D_R1
10k
M51944BSL
If VCC > 4.25V
OUT is activated
D_D11
1S1588
D_D12
1S1588
D_BT1
3V
PWR_FLAG
VMEM is connected to VCC
on the RAM IC's.
GC903
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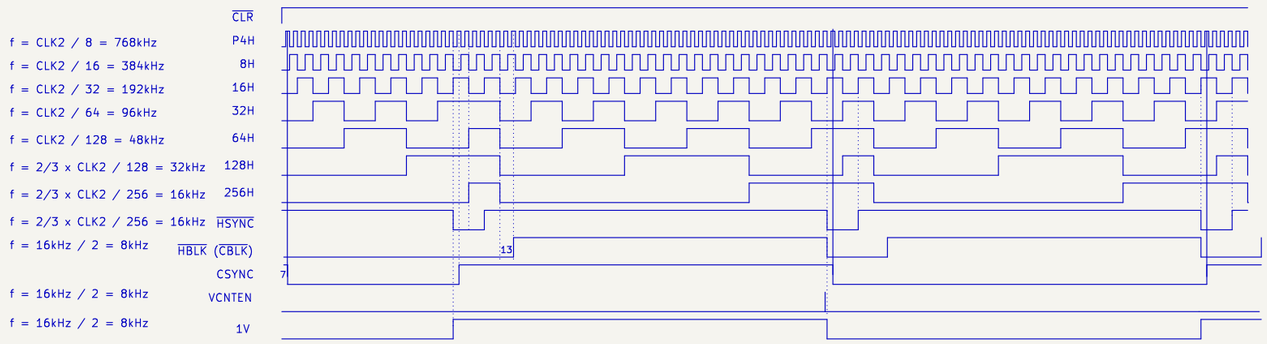
Sheet: /Battery Powered RAM/
File: bpram.kicad_sch
Title: Twin 16 – Rev B
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.9
Id: 18/20

Horizontal signals

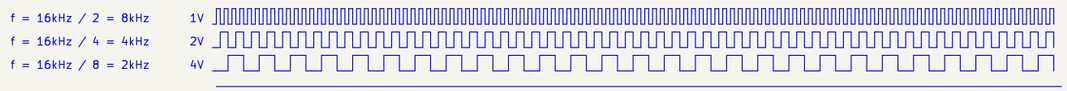


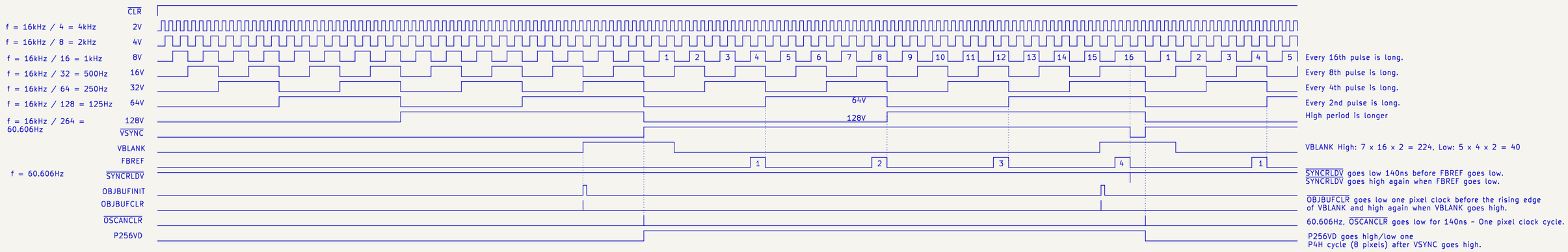
The first HSYNC is at HCOUNT 175 after reset.

– The first VCNTEN is skipped after reset.
It goes low 140ns before HSYNC goes low,
and high again when HSYNC goes low.
VCNTEN is active right before every second falling edge of HSYNC.

– CPURES goes high, and stays high, on the seventh falling edge of HSYNC.

Vertical signals





FBREF is measured at pin 22. At U186:3 FBREF is delayed by 22ns going high and 12ns going low.

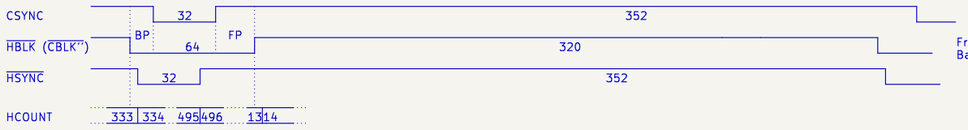
Horizontal and vertical synch timing diagrams

Pixel clock CLK2 = 18.432MHz / 3 = 6.144MHz

Horizontal lines
HSYNC freq = 6.144MHz / 384 = 16kHz
HSYNC period = 1 / 16kHz = 62.5us
Pixels / line: 384
Active pixels: 320
Blank pixels: 64

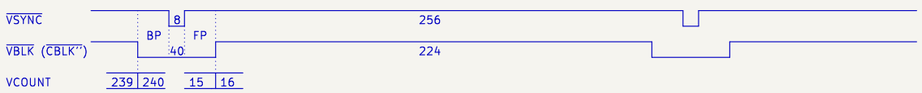
Vertical lines
VSYNC freq = 16kHz / 264 = 60.606060Hz
VSYNC period = 1 / f = 264 / 16kHz = 16.5ms
scanlines / frame: 264
Active lines: 224
Blank lines: 40

The numbers in the HSYNC and HBLK diagrams are HSYNC cycles.
All edges are synchronised to the rising edge of CLK2.



Front Porch (FP) 24 px,
Back Porch (BP) 8 px

The numbers in the VSYNC and VBLK diagrams are HSYNC cycles.
All edges are synchronised to the falling edge of HSYNC.



Front Porch (FP) and
Back Porch (BP) 16 HSYNC cycles.

CBLK'' is at the output of color mixer 007593.
CBLK' is shifted inside the 007593 one pixel clock.

HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]
VCOUNT is bits [128V, 64V, 32V, 16V, 8V, 4V, 2V, 1V]

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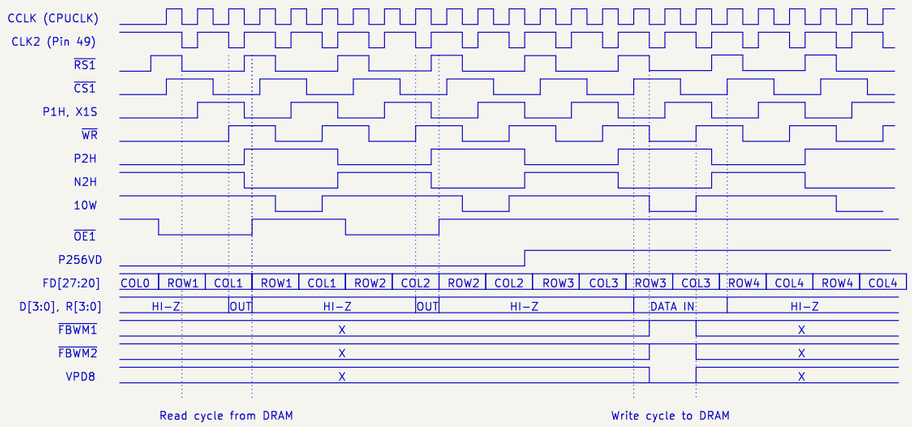
Sheet: /Timing diagrams/
File: timing_diagrams.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 19/20



The same row and column addresses are repeated twice.
One for read cycle and the other for write cycles.

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Sheet: /Sprite timing diagrams/
File: sprite_timing_diagrams.kicad_sch

Title: Twin 16 – Rev B

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.9		Id: 20/20