

Esperanza D. Triana
Ping Pong

JOTEGO

Sheet: /sound/
File: sound.sch

Title: Sound generator

Size: A4 Date: 2022-03-28
KiCad E.D.A. kicad 5.1.12-84ad8e8a8692ubuntu20.04.1

Rev: J. Tejada
Id: 2/11

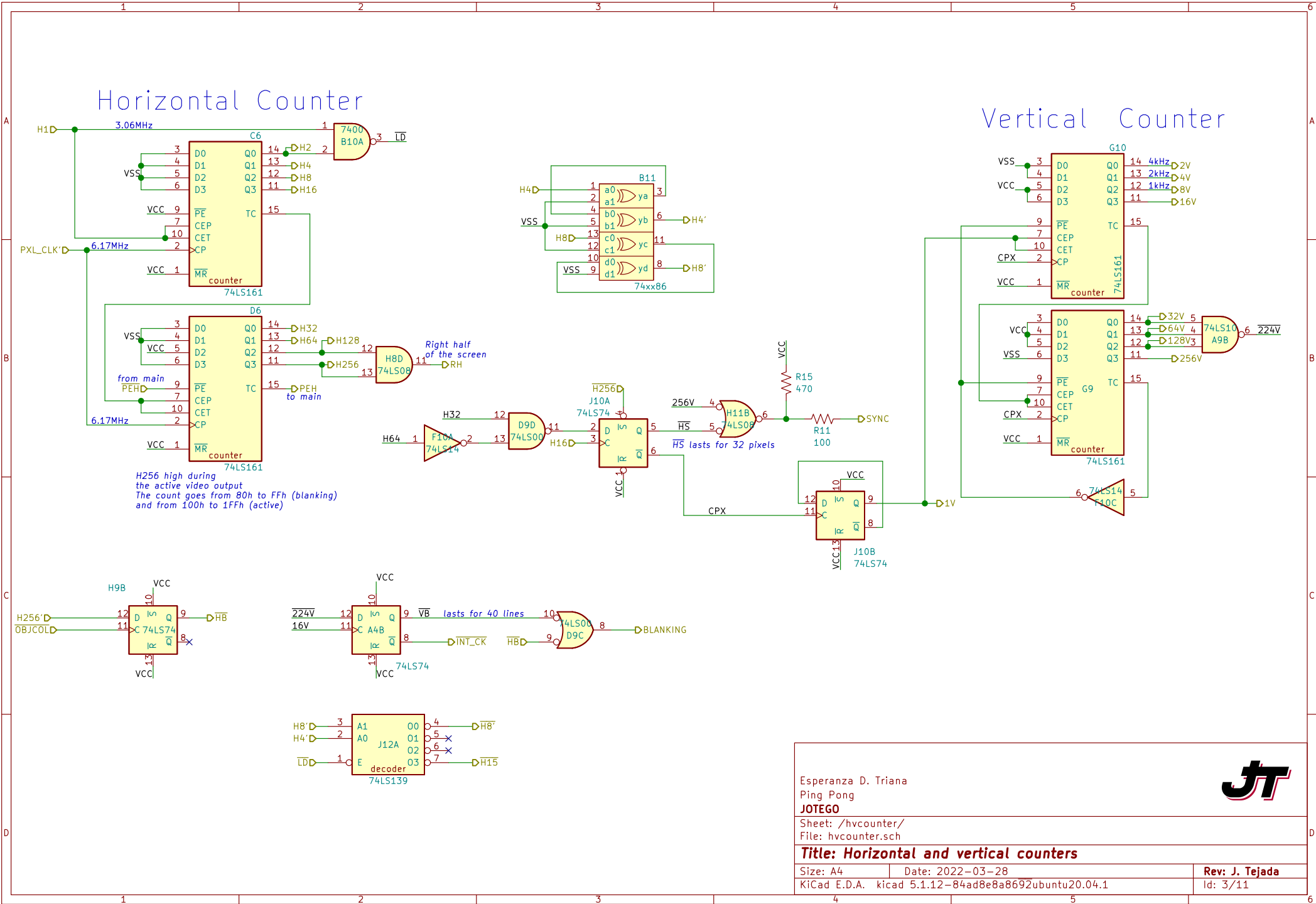
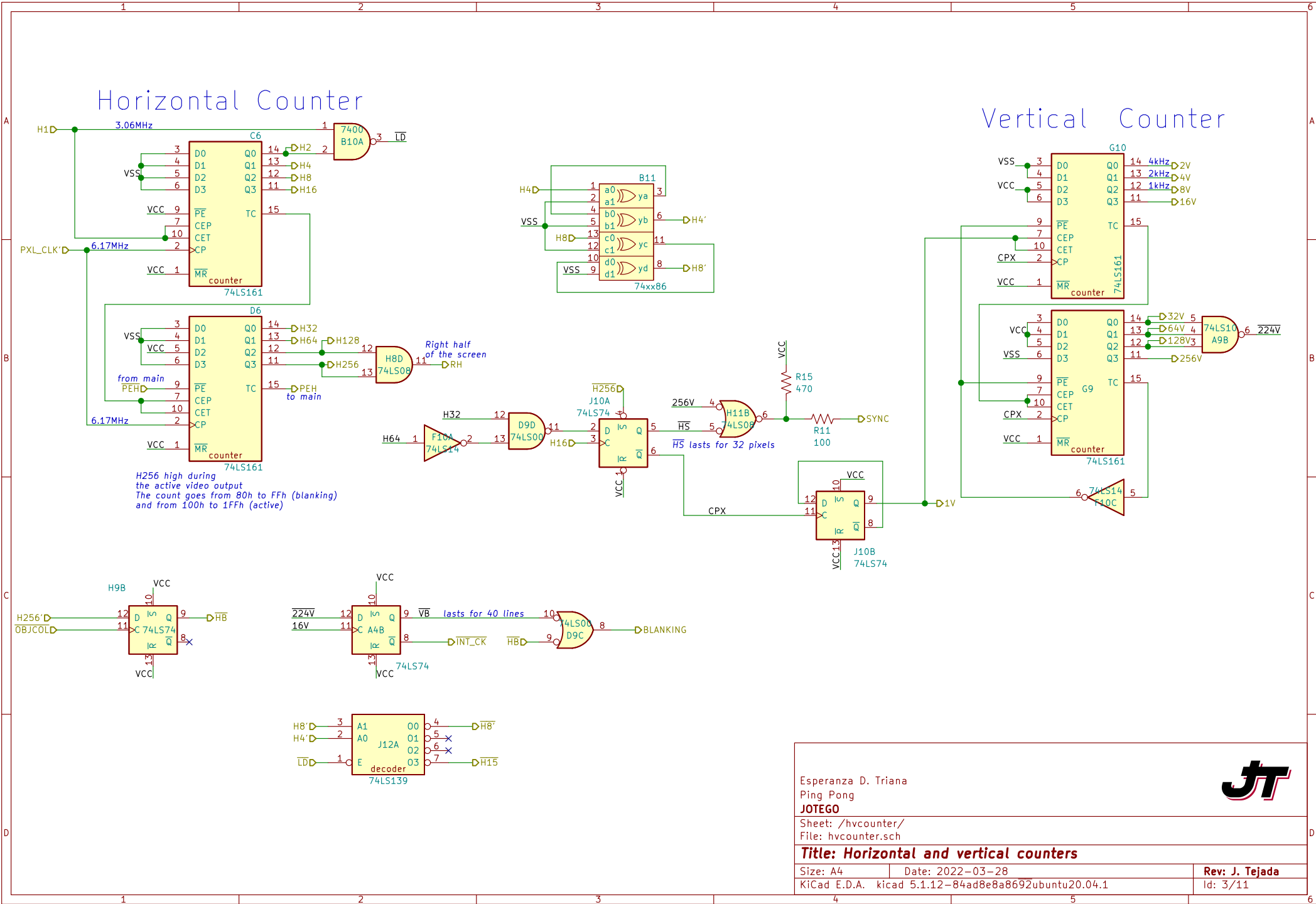
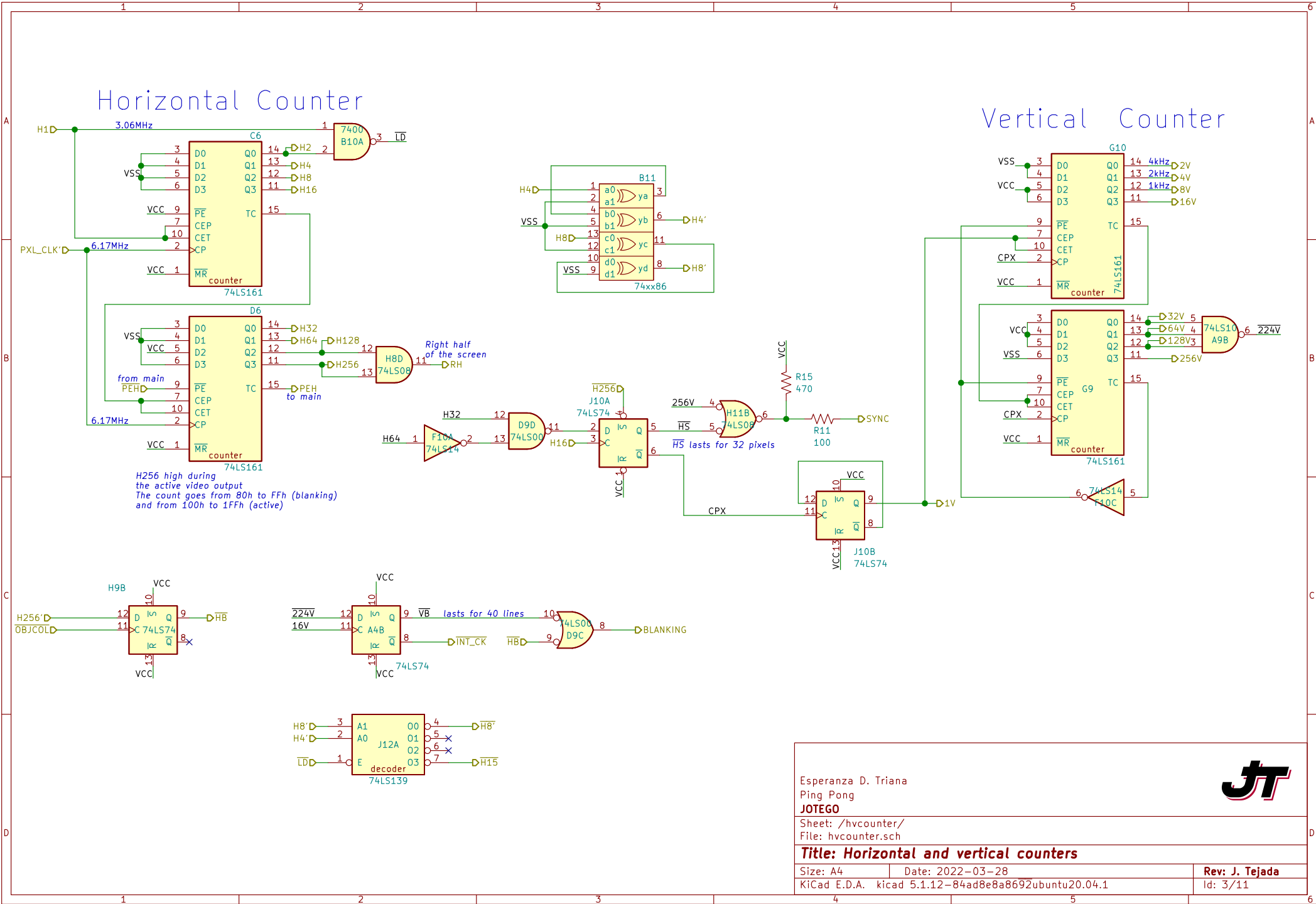


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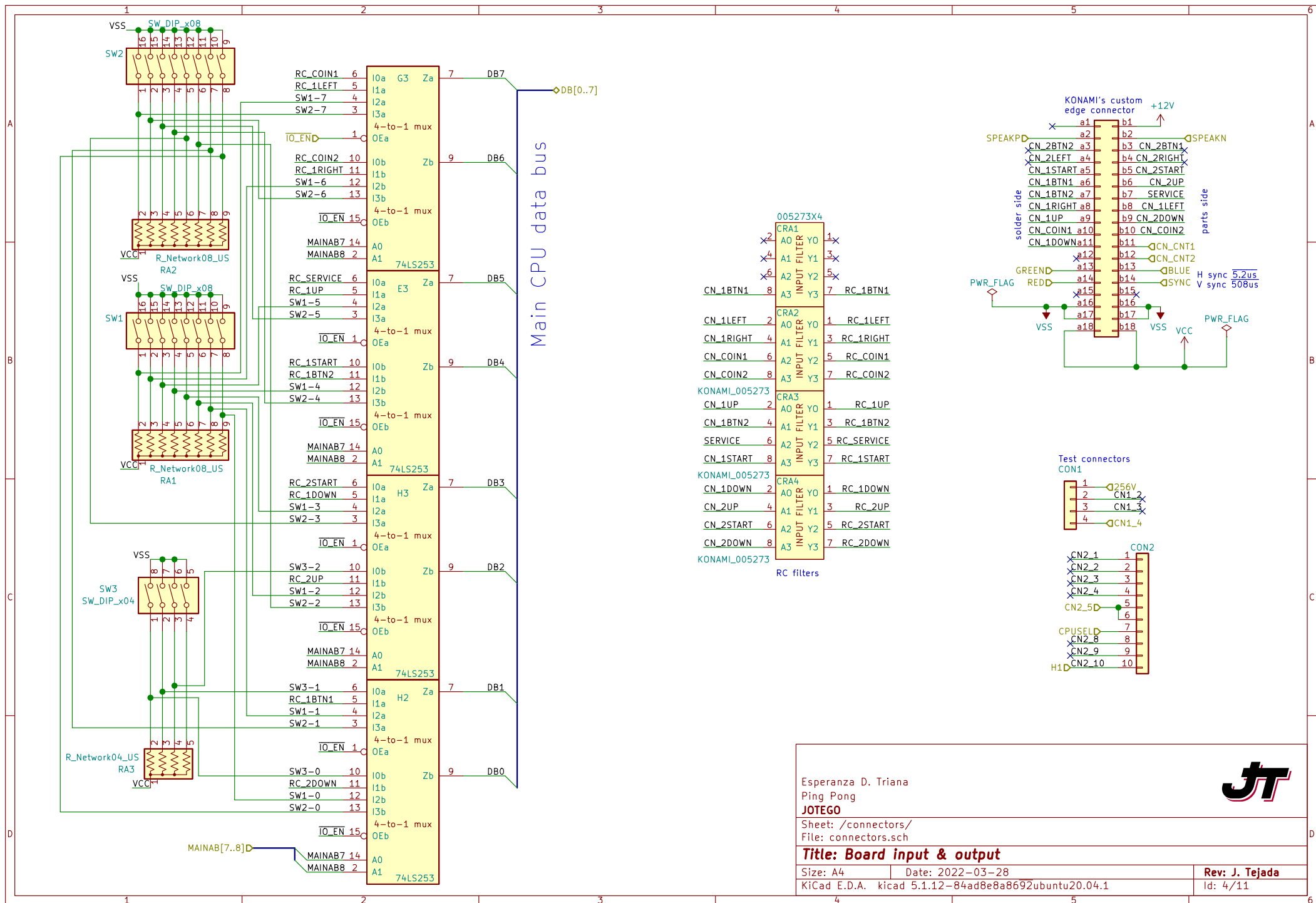
The diagram illustrates a video counter system for a Ping Pong game. It consists of several main components:

- Horizontal Counter:** A 74LS161 counter (C6) receiving a 3.06MHz clock (H1D) and a 6.17MHz clock (PXL_CLK'D). It outputs 16 horizontal sync signals (H2 to H16) and 16 horizontal data signals (H32 to H256). A 74LS08 (H8D) is used to generate the right half of the screen (RH) signal.
- Vertical Counter:** A 74LS161 counter (G10) receiving a 4kHz clock (D2V) and a 2kHz clock (D4V). It outputs 16 vertical sync signals (V2 to V16) and 16 vertical data signals (V32 to V256). A 74LS10 (A9B) is used to generate the 224V signal.
- Decoders:** A 74LS139 (J12A) decoder takes H8' and H4' as inputs and outputs H15 and H16. A 74LS74 (J10B) flip-flop is used to generate the 1V signal.
- Logic Gates and Flip-Flops:** Various logic gates (74LS00, 74LS04, 74LS08, 74LS10, 74LS14, 74LS161) and flip-flops (74LS74, 74LS161) are used to generate the final video signals (H15, H16, V15, V16) and the 224V signal.
- Timing and Control:** The system includes a 74LS00 (F10A) and a 74LS04 (H10A) to generate the 256V signal, which is used to control the horizontal counter. A 74LS08 (H11B) is used to generate the 256V signal, which is used to control the vertical counter.

The diagram is a detailed schematic showing the interconnection of these components, with labels for pins, signals, and components. It is a complex circuit designed to generate a video signal for a Ping Pong game.



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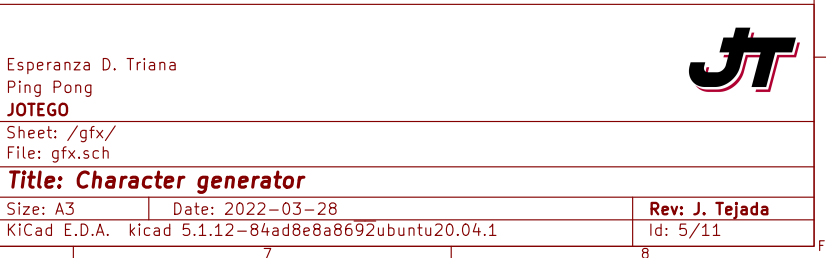
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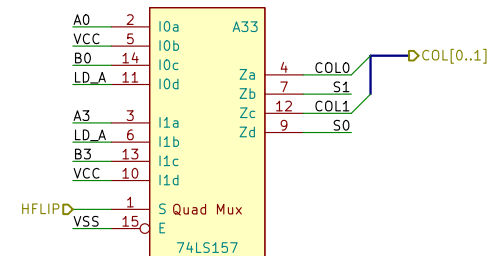
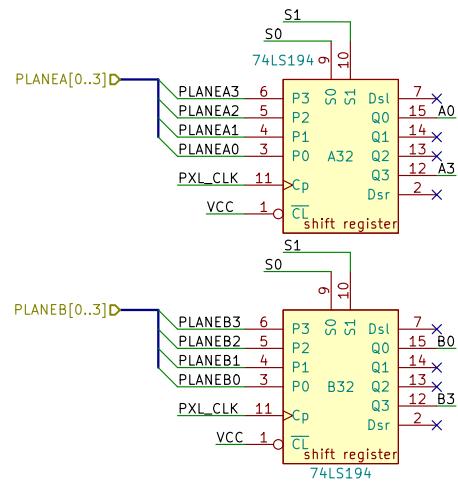
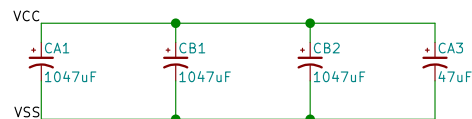
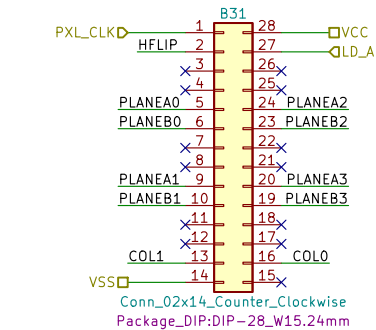
Title: Board input & output

Size: A4 Date: 2022-03-28
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*This is a small board soldered
to a DIP-28 footprint.
It appears twice in the design*

PWB-400322

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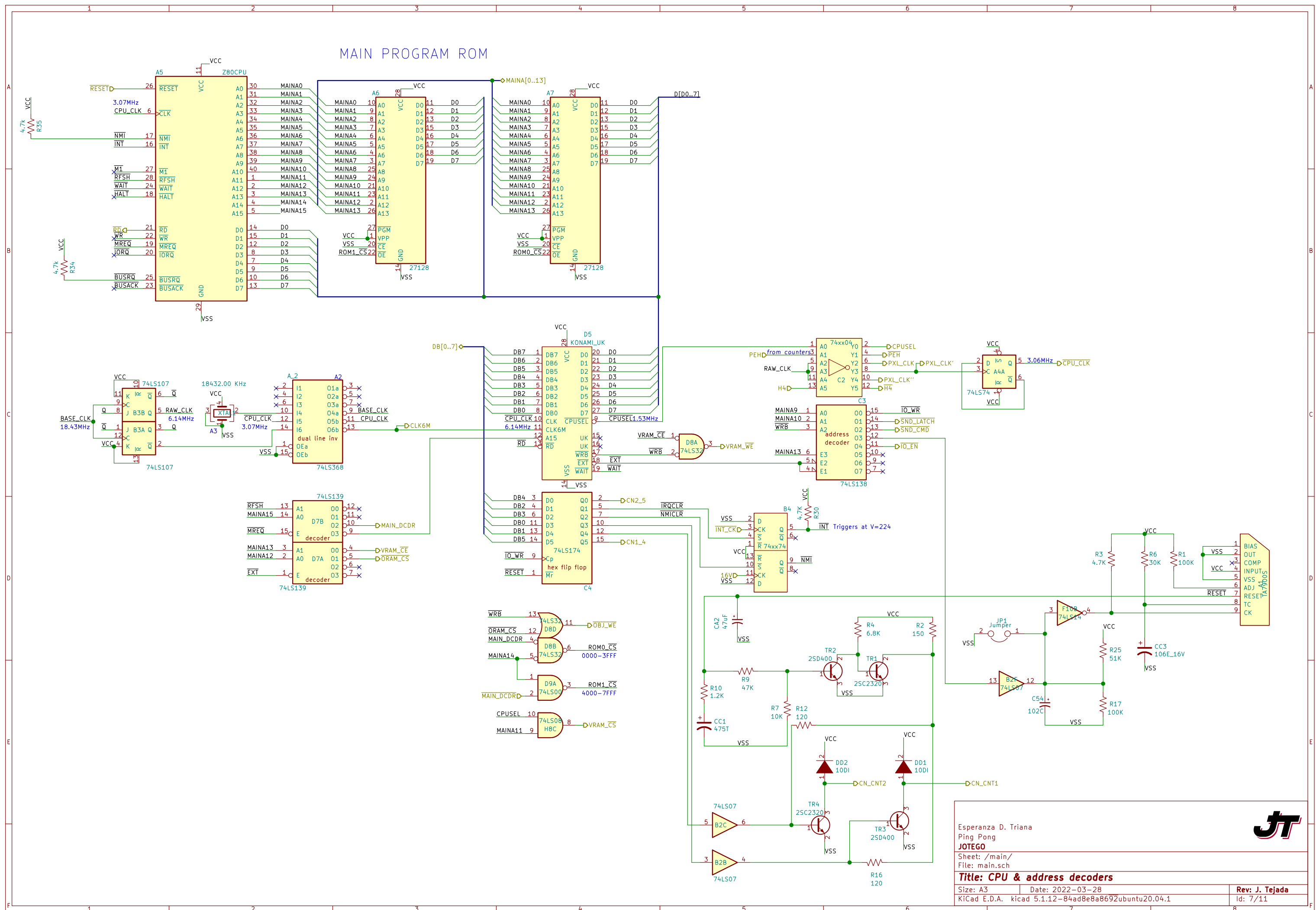


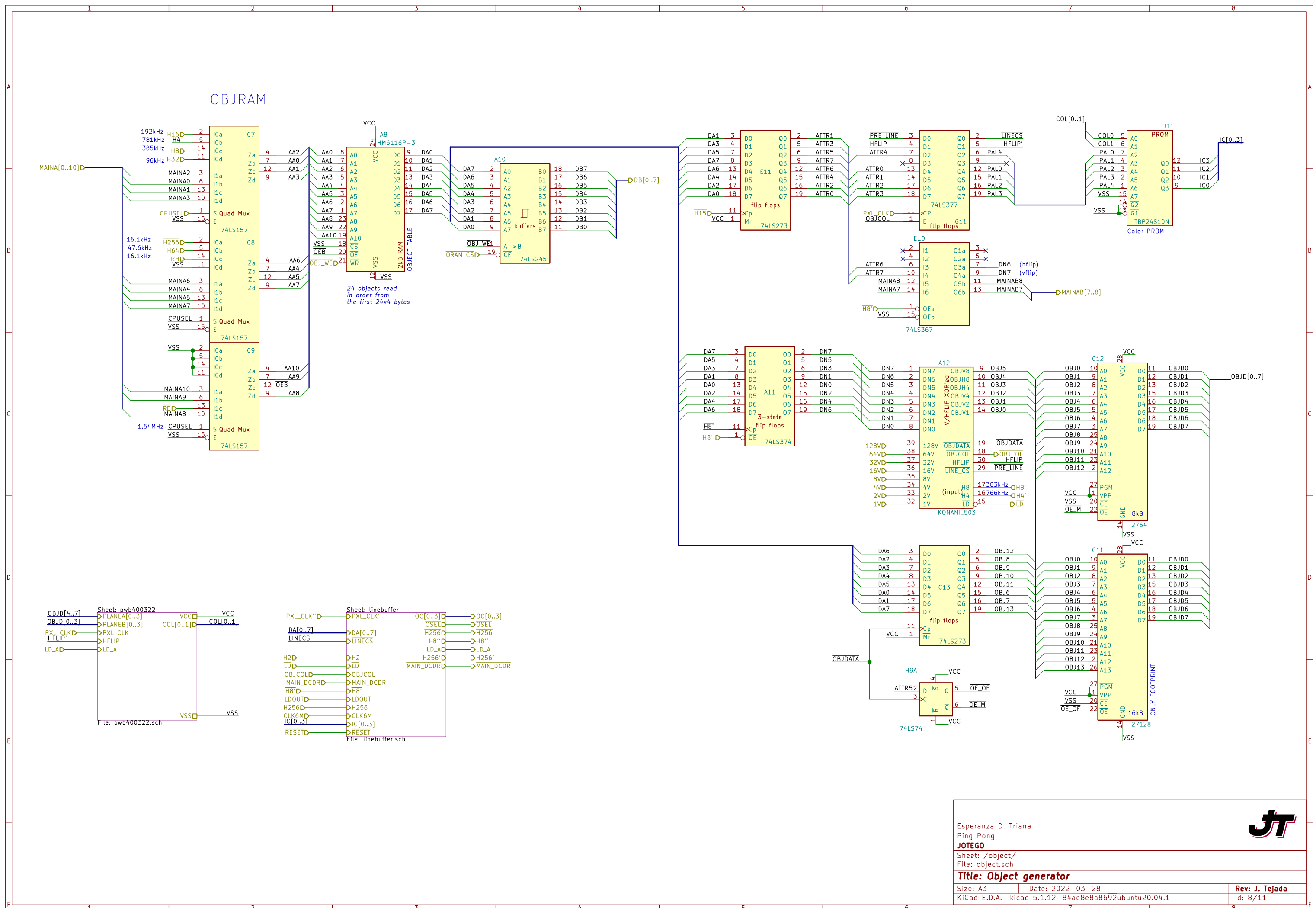
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File: pwb400322.sch

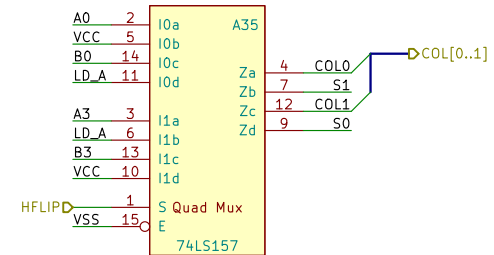
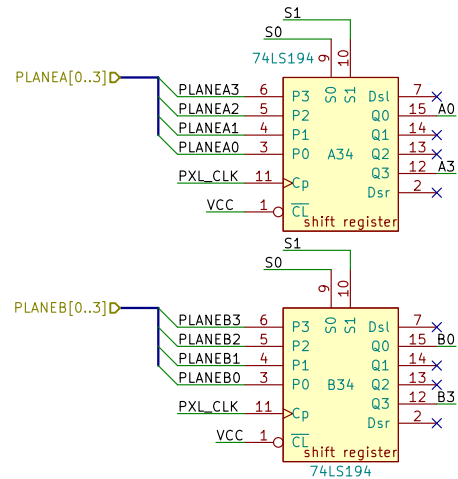
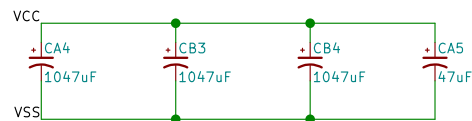
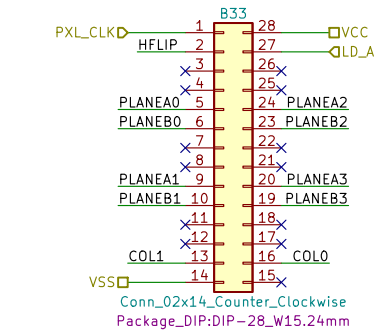
Title: Pixel shift register

Size: A4 Date: 2022-03-28
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PWB-400322

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Sheet: /object/pwb400322/
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Title: Double line buffer

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