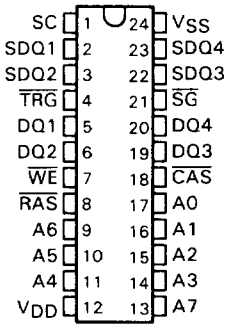
MAY 1988

- 65,536 × 4 Organization
- Dual-Port Accessibility — Four I/Os for Sequential Access, Four I/Os for Random Access
- One Serial Data Register Built into Each Serial I/O for Sequential-Access Applications
- Designed for Video and Non-Video Applications
- Fast Serial Ports . . . 20-MHz Shift Rate
- Mid-Scan Load — Serial Data Streams Uninterrupted by Register Reload
- $\overline{TRG}$ as Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Random-Access Port is Compatible with the SMJ4464, 64K × 4 DRAM
- Supported by TI's SMJ34061 Video System Controller and SMJ34010 Graphics System Processor (GSP)
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
- Maximum Access Time from $\overline{RAS}$ . . . 150 ns
- Minimum Cycle Time (Read or Write) . . . 260 ns
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Random-Access Outputs
- Common Random-Access I/O Capability with "Early Write" Feature
- Available Temperature Ranges with MIL-STD-883-C Class B High-Reliability Processing:
  —S . . . −55°C to 110°C
  —L . . . 0°C to 70°C

JD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Random-Access Data In/ Data Out/Write-Mask Bit
$\overline{RAS}$	Row-Address Strobe
SC	Serial Data Clock
SDQ1-SDQ4	Serial Data In/Data Out
$\overline{SG}$	Serial Enable
$\overline{TRG}$	Transfer Register/ Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{WE}$	Write-Mask Select/ Write Enable

- JEDEC Standardized Pinout
- High-Speed Page-Mode Operation for Faster Access
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh and Hidden Refresh Modes
- Low Power Dissipation
- 24-Pin, 400-Mil Dual-In-line Package

description

The SMJ4461 is a high-speed dual-ported 65,536 × 4 bit dynamic random-access memory with on-chip data registers. The two ports are the random-access port and the sequential-access port. The random-access port makes the memory appear to be organized as 65,536 words of four bits each, similar to the

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SMJ4464. The sequential-access port is interfaced to four internal 256-bit dynamic data registers which make the memory appear to be organized as 256 four-bit words of up to 256 bits each which are accessed serially.

The 256K Multiport Video RAM employs state-of-the-art scaled NMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

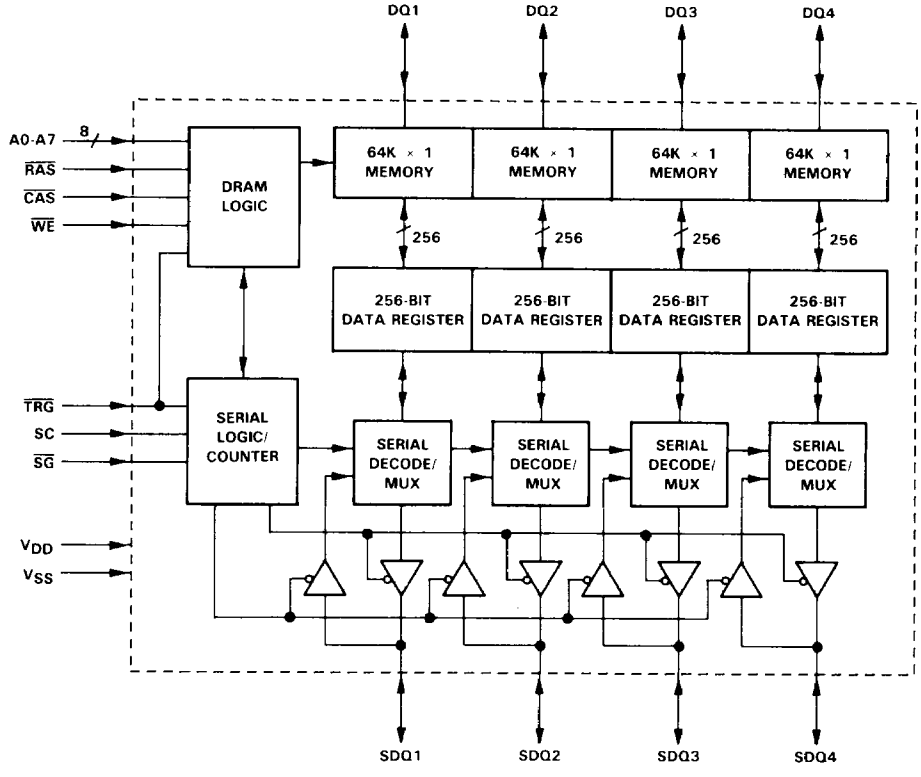
The SMJ4461 features full asynchronous dual-port accessibility except when transferring data between the data register and the random-access memory.

The refresh period is four milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the data register also refreshes that particular row. $\overline{CAS}$-before-$\overline{RAS}$ and hidden refresh modes are also available.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on-chip to simplify system design. All data outs are unlatched to allow greater system flexibility.

The 256K Multiport Video RAM is offered in a 24-pin dual-in-line ceramic package and is guaranteed for operation from −55°C to 110°C. Packages are designed for insertion in mounting-hole rows on 10,16-mm (400-mil) centers.

functional block diagram



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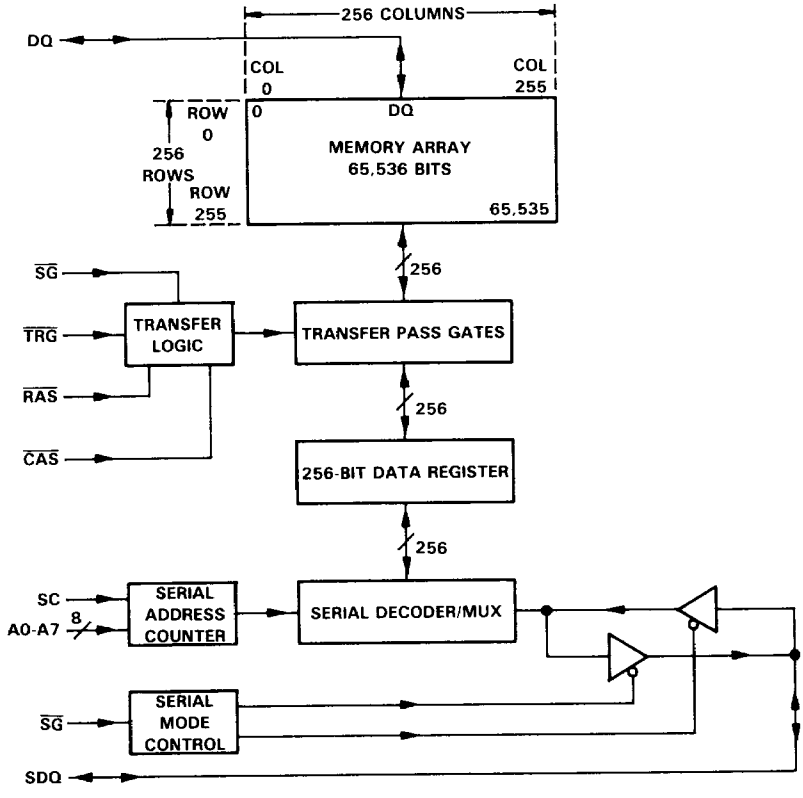
random port to serial port interface

The 256K Multiport Video RAM consists of a 64K × 4 DRAM port and a 256 × 4 serial port. Each of the four random (DRAM) I/Os is interfaced to a 256-bit data register, which can be loaded with 256 bits in parallel from any row in that I/O channel's memory and then read out sequentially, starting from one of 256 selectable locations along the data register. Conversely, each of the four data registers can be loaded serially with data from the serial input (SD) and subsequently transferred, 256 bits in parallel, into any row of memory for each respective DRAM I/O channel.

block diagram showing one random and serial interface



random-access address space to sequential-address space mapping

The 256 bits in each of the four data registers correspond to the 256 column locations of each of the four random I/Os. Data can be read out of the registers starting at any of the 256 data register bit locations.

This tap location is selected by addresses A7 through A0 on the falling edge of $\overline{CAS}$ during a transfer cycle between the memory array and the data registers. All registers are read out starting from the selected tap point proceeding from the least-significant bits to the most-significant bits. The four data registers are configured as circular data registers when reading their contents to the serial outputs. After the most-significant bit (bit 255) is read out of each register, the next bit read will be bit 00 (see explanation under section entitled "serial data input/output").

Note that if column address bits A7 through A0 equal 00 during the last memory-to-register transfer cycle, a total of 256 bits can be sequentially read out of each of the four data registers starting from bit position 00.

operation

random-access operation

transfer register select ($\overline{TRG}$)

The $\overline{TRG}$ selects either register transfer or random-access operation as $\overline{RAS}$ falls. To use the SMJ4461 in random-access mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. This causes the 256 storage elements of each data register to remain disconnected from the corresponding 256 bit lines of the memory array. If serial data is to be written in or read out of the data registers, the data registers must be disconnected from the bit lines. Holding TRG low as RAS falls enables the 256 switches that connect the data registers to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row.

random output enable ($\overline{TRG}$)

During random-access operations, $\overline{TRG}$ functions as an output enable for the random outputs after the read access times have been satisfied (if this is a read cycle). Whenever $\overline{TRG}$ is held high, the Q outputs will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q outputs, making it possible to connect the address lines to the data I/O lines — although use of this organization prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins to allow write data to be driven onto the pins after output read data has been externally latched.

address (A0 through A7)

Sixteen address bits are required to decode one of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip on the falling edge of $\overline{RAS}$. Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip on the falling edge of $\overline{CAS}$. All row and column addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$ respectively. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the device input and output buffers. $\overline{CAS}$ is also used to strobe the column address into the memory.

write-mask enable ($\overline{WE}$)

The $\overline{WE}$ pin selects the random-mode write-mask option. The SMJ4461 random port is equipped with two modes of write operations. If $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$ (during a random access operation), the write mask is enabled. Accordingly, a 4-bit binary code (the mask) is input to the device via the random D/Q pins and is also latched on the falling edge of $\overline{RAS}$. This binary pattern determines which of the four DRAM I/Os will will be written into on that access and which DRAM I/Os will not. Thus,

after $\overline{RAS}$ has latched the write mask on chip, input data is driven onto the DQ pins and is latched on the falling edge of the latter of $\overline{CAS}$ or $\overline{WE}$ (for early write operation, $\overline{WE}$ can remain low for the entire $\overline{RAS}$ low period). If a 0 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, then the write circuits for that particular I/O will be defeated and data will not be written to that I/O. If a 1 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, then the write circuits for that particular I/O will not be defeated and data will be written to that I/O. See the corresponding timing diagrams for details.

Important: The mask operation is selected only if $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{WE}$ is held high on the falling edge of $\overline{RAS}$, the mask is not enabled and the write operation is identical to standard × 4 DRAMs, with all four I/Os being written by the data appearing on the DQ pins when the latter of $\overline{WE}$ or $\overline{CAS}$ is brought low. Thus, if it is not desired to use the mask function, then a standard DRAM timing interface can be used.

WRITE MASK FUNCTION TABLE

$\overline{TRG}$	$\overline{WE}$	DQ1-DQ4	MODE
1	1	X	Write enabled at DQ1-DQ4
1	0	1	Write to DQ enabled
1	0	0	Write to DQ disabled

NOTE 1: The logic states in the table above are assumed valid on the falling edge of $\overline{RAS}$.

write enable ($\overline{WE}$)

The read or write mode is selected through the write-enable ($\overline{WE}$) input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle.

data I/O (DQ1-DQ4)

Memory data is written during a write or read-modify-write cycle. The falling edge of $\overline{WE}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed in by $\overline{WE}$ with data setup and hold times referenced to this signal. The three-state output buffers provide direct TTL compatibility (no pull-up resistors required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low.

Once the outputs are valid, they will remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high will return the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle. In a register-transfer operation (memory-to-register or register-to-memory), the outputs remain in the high-impedance state for the entire cycle, regardless of transitions on $\overline{CAS}$ or $\overline{TRG}$.

write mask bits (DQ1-DQ4)

When the write mask is enabled ($\overline{WE}$ low on the falling edge of $\overline{RAS}$), the write mask bits determine which DRAM I/Os are to be written and which of the DRAM I/Os will have their write operations internally defeated. The states of the write mask bits are latched on-chip on the falling edge of $\overline{RAS}$ and selectively control the internal write enable circuits of each corresponding DRAM I/O. If the write mask is not enabled ($\overline{WE}$ high on the falling edge of $\overline{RAS}$), then no write enable circuits will be defeated and data appearing at the DQ1-DQ4 pins on the falling edge of $\overline{RAS}$ will be ignored. See timing diagrams and the table under "write mask enable ($\overline{WE}$)" for details.

refresh

A refresh operation must be performed to each row at least once every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power. Note that the data registers are dynamic storage elements and that the data held in the registers will be lost unless SC is clocked two times or else the data is reloaded from the memory array. See specifications for maximum register retention times.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}). The external row address is ignored and the refresh address is generated internally.

column-address strobe ($\overline{CAS}$)

The $\overline{CAS}$ input latches the column addresses on-chip and also functions as an output enable for DQ1-DQ4.

power up

After power up, the power supply must remain at its steady-state value for one millisecond. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles and one memory-to-register transfer cycle with an SC cycle following the rising edge of $\overline{TRG}$ before proper device operation is achieved.

sequential-access operation

transfer register select ($\overline{TRG}$)

Memory operations involving parallel use (i.e., transfer from memory to data register or data register to memory) of the data register are invoked by bringing $\overline{TRG}$ low with the address lines A0-A7 before $\overline{RAS}$ falls. This enables the switches connecting the 256 elements of each data register to the 256 bit lines of each DRAM I/O. The states of $\overline{WE}$ and $\overline{SG}$, which are also latched on the falling edge of $\overline{RAS}$, determine whether the 256-bit data transfer will be from the memory array to the data registers or from the data registers to memory array, as well as determining if the SDQs are in read or write mode (see "transfer operation logic table").

Note that the state of $\overline{TRG}$ is latched on the falling edge of $\overline{RAS}$ just like a row address to select the mode of operation. During read or read-modify-write cycles, $\overline{TRG}$ functions as output enable after $\overline{CAS}$ falls.

transfer write enable ($\overline{WE}$)

In register transfer mode, $\overline{WE}$ determines whether a transfer will occur from the data registers to the memory array, or from the memory array to the data registers. To transfer data from the data registers to the memory array, $\overline{WE}$ and $\overline{SG}$ are held low as $\overline{RAS}$ falls. If $\overline{SG}$ were to be high during this transition, then no transfer of data from the data register to the memory array would occur, but the SDQs would be put into the write mode. This would allow serial data to be written into the register. To transfer from the memory array to the data registers, $\overline{WE}$ is held high and $\overline{SG}$ is a don't care as $\overline{RAS}$ falls. This cycle puts the SDQs into the read mode, thus allowing serial data to be read out of the data register. Note that $\overline{WE}$ and $\overline{SG}$ setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation (see "transfer operation logic" table).

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the data registers. (The states of A0-A7, $\overline{WE}$, $\overline{TRG}$, and $\overline{SG}$ are latched on the falling edge of $\overline{RAS}$).

register column address (A0 through A7)

To select one of the 256 positions along each of the four data registers from which the first serial data will be read out, or to which the first serial data will be written, the appropiate 8-bit column address (A0-A7) must be valid when $\overline{CAS}$ falls during the appropriate transfer cycle.

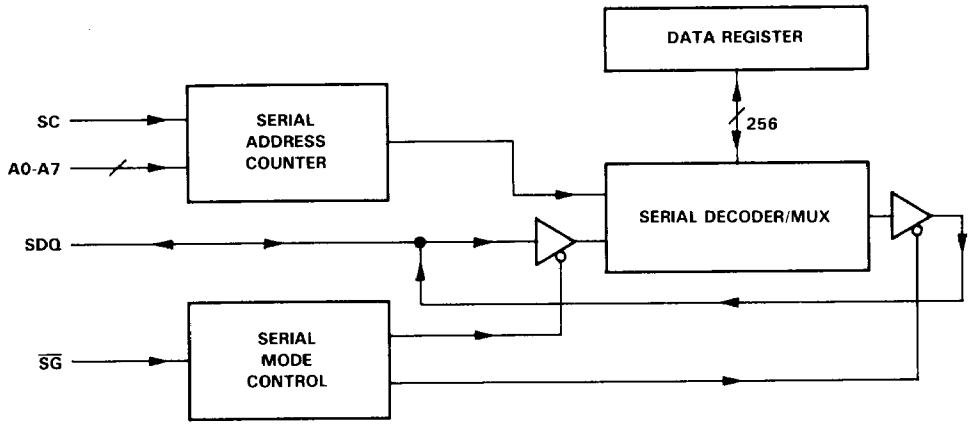
serial data clock (SC)

Data is written in or read out of the data registers on the rising edge of SC. This makes it possible to view the data registers as though they were made of 256 positive-edge-triggered D flip-flops connected D to Q (not to be confused with the DQ random I/O pins of the SMJ4461). The SMJ4461 is designed to work with a wide range duty cycle clock to simplify system design.

serial data input/output (SDQ1-SDQ4)

SD and SQ share a common I/O pin. Data is written in when $\overline{SG}$ is low during write mode and data is read out when $\overline{SG}$ is low during read mode (see "transfer operation logic table"). Note that when the serial address counter reaches its maximum value of 255, it is reset back to 00 with the next positive transition of SC. This allows data to be read out in a continuous loop.

block diagram of one serial I/O



serial enable ($\overline{SG}$)

The serial enable pin has two functions. First, it is used on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{WE}$ low. If $\overline{SG}$ is low during this transition, then a register-to-memory transfer will occur. On the other hand, if $\overline{SG}$ were to be high as $\overline{RAS}$ falls, then a write-mode control cycle will be performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing serial data to be written into the data register. Second, $\overline{SG}$ is used as a SDQ enable/disable. In the write mode, $\overline{SG}$ is used as an input enable. $\overline{SG}$ high disables the input, and $\overline{SG}$ low enables the input. To take the device out of the write mode and into the read mode, a memory-to-register transfer cycle must be performed. The read mode allows data to be read out of the data register. $\overline{SG}$ high disables the output and $\overline{SG}$ low enables the output. Note that the serial address counter will be incremented on each SC cycle regardless of the state of $\overline{SG}$.

TRANSFER OPERATION LOGIC TABLE

$\overline{TRG}$	$\overline{WE}$	$\overline{SG}$	MODE
0	0	0	Register-to-memory transfer
0	0	1	Write-mode enable
0	1	X	Memory-to-register transfer

NOTE 2: The logic states in the table above are assumed valid on the falling edge of $\overline{RAS}$.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 3) . . . . . −1.0 V to 7 V
Voltage range for V_{DD} supply with respect to V_{SS} . . . . . −1 V to 7 V
Voltage range for data out with respect to V_{SS} . . . . . −1 V to V_{DD} + 0.3 V
Short circuit output current per output . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating temperature range . . . . . −55°C to 110°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except SC	2.4		5.5	V
		SC	2.6		5.5	
V_{IL}	Low-level input voltage (see Note 4)		−1		0.8	V
T_A	Operating free-air temperature		−55			°C
T_C	Operating case temperature				110	°C

NOTE 4: The algebraic convention where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4461-15			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All outputs open			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V			±10	μA
I_{DD1}	Average operating current during read, write or transfer cycle (serial port in standby)	Mininum cycle time, No load on DQ and SDQ pins		50	80	mA
I_{DD2}	Standby current (total, both ports)	After 1 memory cycle, $\overline{RAS}$, $\overline{CAS}$, SC, and $\overline{SG}$ ≥ 2.4 V, No load on DQ and SDQ pins		15	20	mA
I_{DD3}	Average refresh current	Minimum cycle time, $\overline{RAS}$ ≤ 0.8 V, $\overline{CAS}$ ≥ 2.4 V, No load on DQ and SDQ pins		45	75	mA
I_{DD4}	Average page-mode current (serial port in standby)	Minimum cycle time, $\overline{RAS}$ ≤ 0.8 V, $\overline{CAS}$ cycling, No load on DQ and SDQ		35	60	mA
I_{DD5}	Average current with memory array in standby and register shifting	$t_{c(SC)}$ = MIN, $\overline{RAS}$ and $\overline{CAS}$ ≥ 2.4 V, No load on DQ and SDQ pins		70	80	mA
I_{DD6}	Worst case average current	Minimum cycle time on both ports, No load on DQ and SDQ pins		110	140	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance at 25°C with nominal supply voltage, f = 1 MHz

PARAMETER‡		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		4		pF
$C_{i(RC)}$	Input capacitance, strobe inputs		8		pF
$C_{i(WE)}$	Input capacitance, write enable input		8		pF
$C_{i(SC)}$	Input capacitance, serial clock		8		pF
$C_{i(SG)}$	Input capacitance, serial enable		4		pF
$C_{i(TRG)}$	Input capacitance, transfer register input		4		pF
C_o	Output capacitance		5		pF

‡Capacitance data collected for major design or process changes only.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (see Figure 1)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4461-15		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, t_{RLCL} ≥ MAX	t_{CAC}		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 80 pF, t_{RLCL} ≤ MAX	t_{RAC}		150	ns
$t_{a(TRG)}$	Access time of DQ from $\overline{TRG}$ low	C_L = 80 pF			45	ns
$t_{a(SC)}$	Access time of SQ from SC high	C_L = 80 pF			50	ns
$t_{a(SG)}$	Access time of SQ from $\overline{SG}$ low	C_L = 80 pF			40	ns
$t_{dis(CH)}$	Random-output disable time from $\overline{CAS}$ high	C_L = 80 pF	t_{OFF}	0	30	ns
$t_{dis(TRG)}$	Random-output disable time from $\overline{TRG}$ high	C_L = 80 pF		0	30	ns
$t_{dis(SG)}$	Serial-output disable time from $\overline{SG}$ high	C_L = 80 pF			30	ns

timing requirements over recommended supply voltage and operating free-air temperature ranges

		ALT.	SMJ4461-15		UNIT
		SYMBOL	MIN	MAX	
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{c(Trd)}$	Transfer read cycle time	t_{RC}	260		ns
$t_{c(TW)}$	Transfer write cycle time	t_{WC}	260		ns
$t_{c(P)}$	Page-mode read or write cycle time	t_{PC}	145		ns
$t_{c(rdWP)}$	Page-mode read-write/read-modify-write cycle time	t_{RWC}	230		ns
$t_{c(SC)}$	Serial clock cycle time	t_{SCC}	50	20,000	ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ duration (precharge time)	t_{CP}	60		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		ns
$t_{w(SCL)}$	Pulse duration, SC low		10		ns
$t_{w(SCH)}$	Pulse duration, SC high		10		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		45		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(RW)}$	$\overline{WE}$ setup time before $\overline{RAS}$ low with $\overline{TRG}$ low (register transfer cycles)		0		ns
$t_{su(DQ)}$	DQ setup time before $\overline{RAS}$ low with $\overline{TRG}$ high (random access, write mask select)		8		ns
$t_{su(D)}$	Data setup time	t_{DS}	5		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		ns
$t_{su(SD)}$	Serial data setup time before SC high		5		ns
$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low		0		ns
$t_{su(SG)}$	$\overline{SG}$ setup time before $\overline{RAS}$ low with $\overline{TRG}$ and $\overline{WE}$ low		0		ns
$t_{su(WM)}$	$\overline{WE}$ setup time before $\overline{RAS}$ low (write mask select)		0		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RW)}$	$\overline{WE}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ low (transfer cycles)		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		ns
$t_{h(WLD)}$	Data hold time after $\overline{WE}$ low	t_{DH}	45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns

Continued next page.

NOTES: 5. Timing measurements referenced to V_{IL} max and V_{IH} min.

6. System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage and operating free-air temperature ranges (continued)

			ALT. SYMBOL	SMJ4461-15 MIN	SMJ4461-15 MAX	UNIT
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low		t_{WCH}	45		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low		t_{WCR}	120		ns
$t_{h(WQE)}$	$\overline{TRG}$ hold time after $\overline{WE}$ low			40		ns
$t_{h(SD)}$	Serial data-in hold time after SC high			15		ns
$t_{h(SQ)}$	Serial data-out hold time after SC high□			6		ns
$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low			15		ns
$t_{h(DQ)}$	DQ hold time after $\overline{RAS}$ low with $\overline{TRG}$ high and $\overline{WE}$ low			15		ns
$t_{h(SG)}$	$\overline{SG}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ and $\overline{WE}$ low			15		ns
$t_{h(WM)}$	$\overline{WE}$ hold time after $\overline{RAS}$ low (write mask select)			15		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		t_{CSH}	150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		t_{CRP}	5		ns
t_{CLGH}	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high			80		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		t_{RSH}	75		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{WE}$ low (read-modify-write cycle only)¶		t_{CWD}	110		ns
t_{RLTH}	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (memory-to-register transfer cycle)	Early load#		25		ns
		Mid-line real-time load		100		
t_{RLSH}	Delay time, $\overline{RAS}$ low to the first positive transition of SC after $\overline{TRG}$ high (register transfer cycle)			125		ns
t_{THRL}	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low after a transfer cycle			100		ns
t_{CLSH}	Delay time, $\overline{CAS}$ low to the first positive transition of SC after $\overline{TRG}$ high (register transfer cycle)			50		ns
t_{SHRL}	Delay time, SC high to $\overline{RAS}$ low with $\overline{TRG}$ and $\overline{WE}$ low (register-to-memory transfer cycle)‖			50		ns
t_{SHTH}	Delay time, SC high to $\overline{TRG}$ high (memory-to-register transfer cycle)☆			15		ns

Continued next page.

NOTE 5: Timing measurements are referenced to V_{IL} max and V_{IH} min.

¶ $\overline{TRG}$ must disable the output buffers prior to applying data to the device.

$\overline{TRG}$ may be brought high early during a memory-to-register transfer cycle as long as the $th_{(TRG)}$, t_{SHTH}, and t_{RLSH} specifications are met.

‖ In a register-to-memory transfer cycle, the state of SC when $\overline{RAS}$ falls is a don't care condition. However, to guarantee proper sequencing of the internal clock circuitry there can be no positive transitions of SC for at least 40 ns prior to when $\overline{RAS}$ goes low. See the section entitled "sequential access operation" for a complete explanation of the transfer operation.

☆ In a memory-to-register transfer cycle, the state of SC when $\overline{TRG}$ rises is a don't care condition. However, to guarantee proper sequencing of the internal clock circuitry there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high. See the section entitled "sequential access operation" for a complete explanation of the transfer operation.

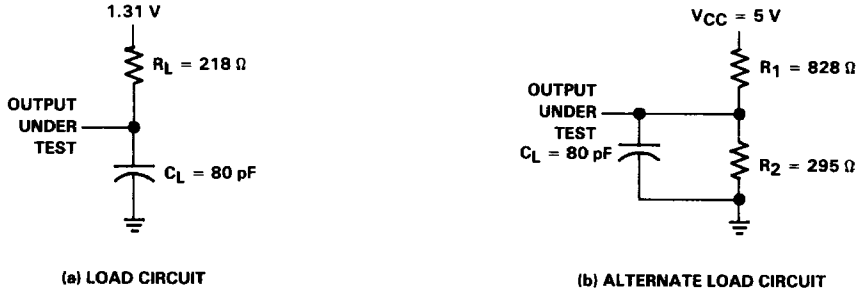
□ This parameter is guaranteed but not tested.

timing requirements over recommended supply voltage and operating free-air temperature ranges (concluded)

		ALT.	SMJ4461-15		UNIT
		SYMBOL	MIN	MAX	
t_{THSH}	Delay time, $\overline{TRG}$ high to SC high (memory-to-register transfer cycle)		20		ns
t_{THRH}	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (memory-to-register transfer cycle)		0		ns
t_{THCH}	Delay time, $\overline{TRG}$ high to $\overline{CAS}$ high (register transfer cycles)		0		ns
t_{CLTH}	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high (memory-to-register transfer cycle)		25		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee $\overline{RAS}$ access time)	t_{RCD}	25	75	ns
t_{CLGL}	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ low (maximum value specified to guarantee column access time)			30	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low (read-modify-write cycle only)	t_{RWD}	185		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	25		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	25		ns
t_{SGSC}	Delay time, $\overline{SG}$ low to SC high during serial data-in shift cycle		10		ns
t_{GHD}	Delay time, $\overline{TRG}$ high before data applied at DQ	t_{GDD}	30		ns
$t_{rf(MA)}$	Refresh time interval, memory array	t_{REF1}		4	ms
$t_{rf(SR)}$	Refresh time interval, shift register	t_{REF2}		20,000	ns

NOTE 5: Timing measurements are referenced to V_{IL} max and v_{IH} min.

PARAMETER MEASUREMENT INFORMATON



(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

FIGURE 1. LOAD CIRCUITS FOR TIMING PARAMETERS

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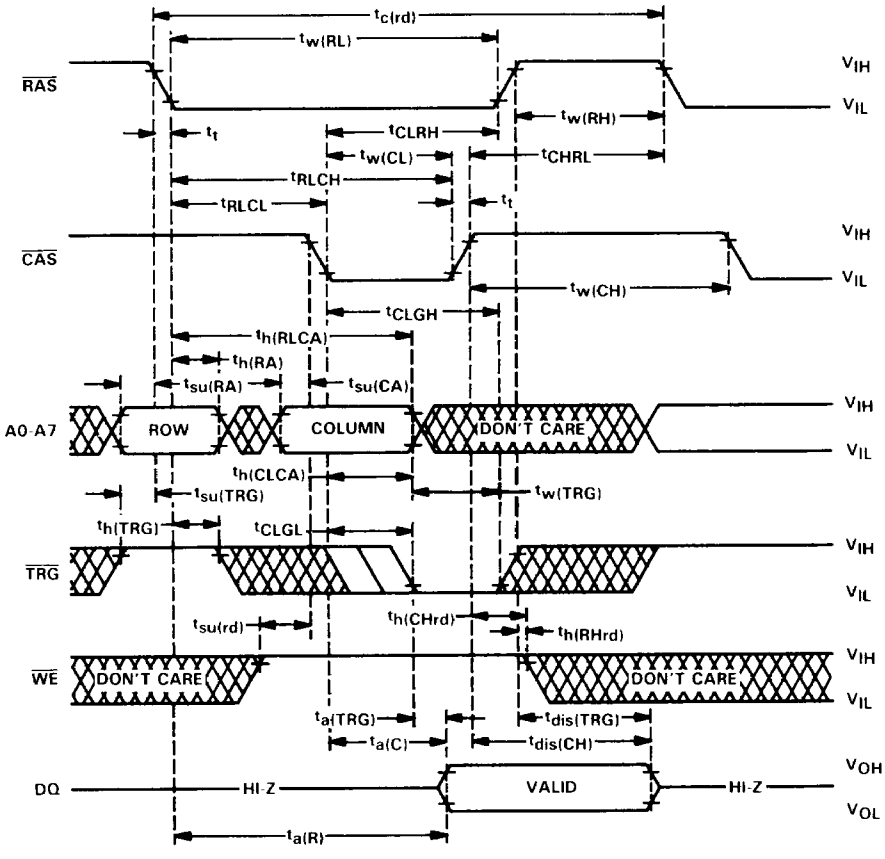
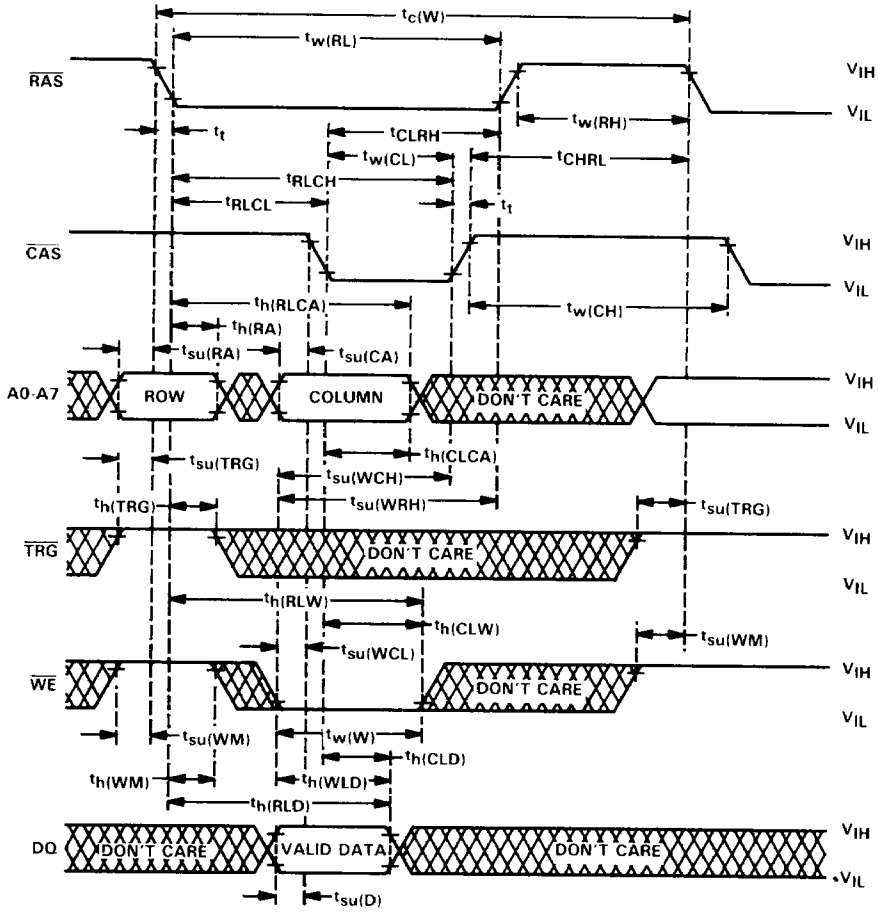
read cycle timing



early write cycle timing, write mask unselected



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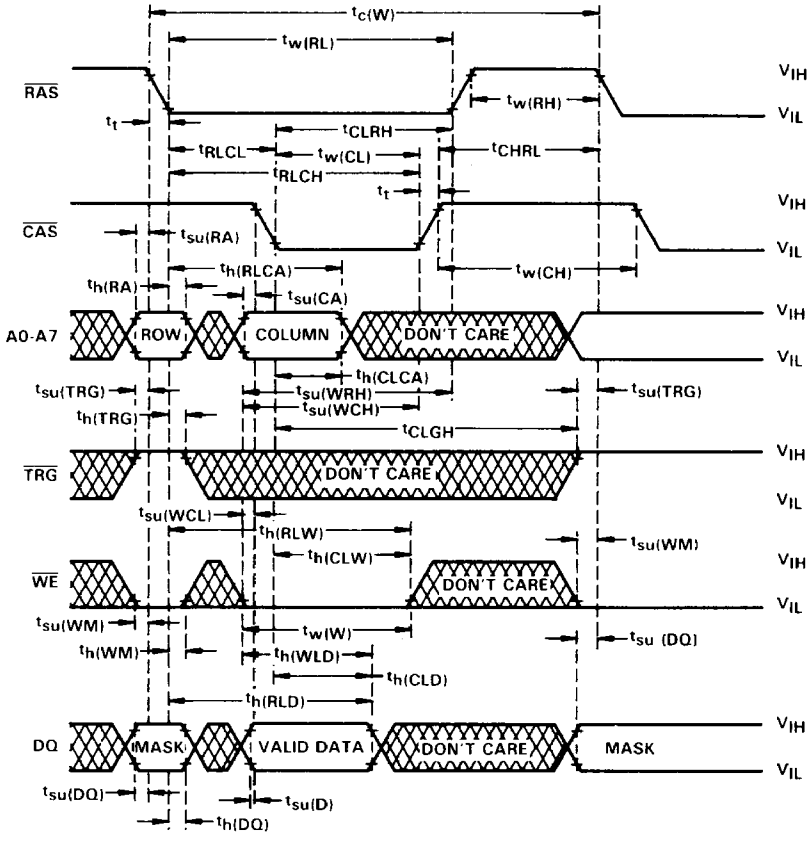
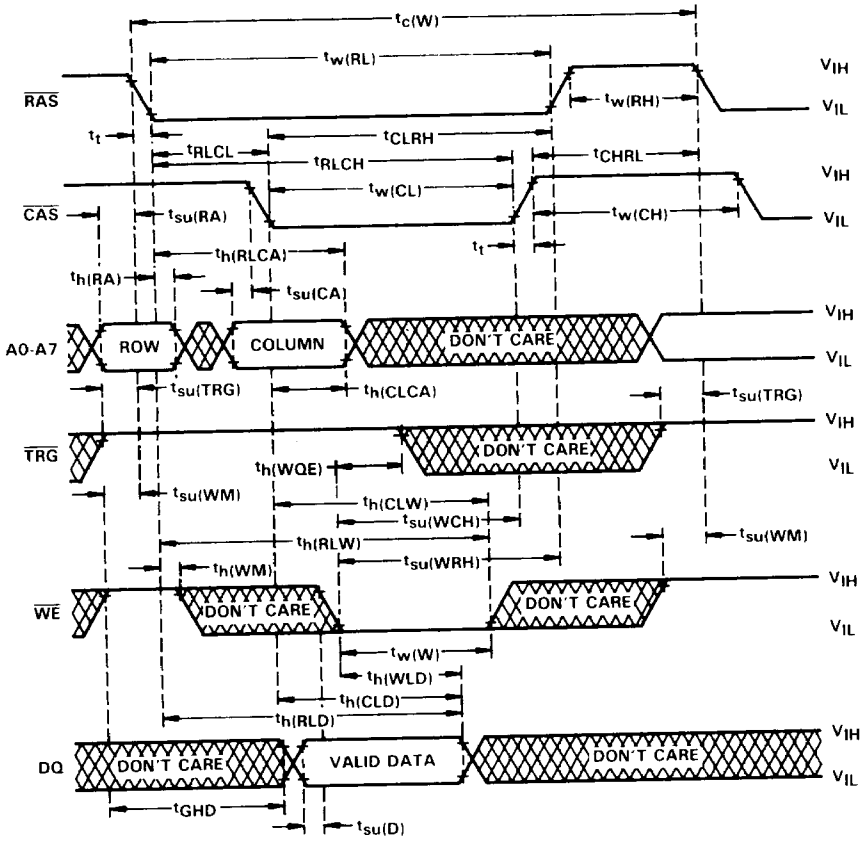
early write cycle timing, write mask selected



delayed write cycle timing, mask unselected



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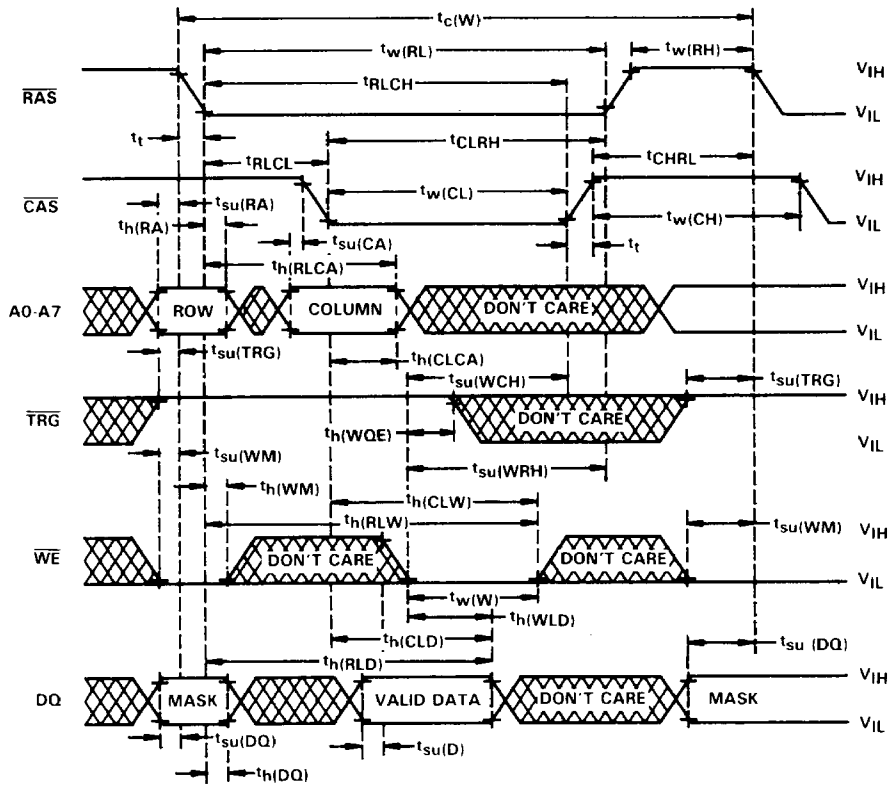
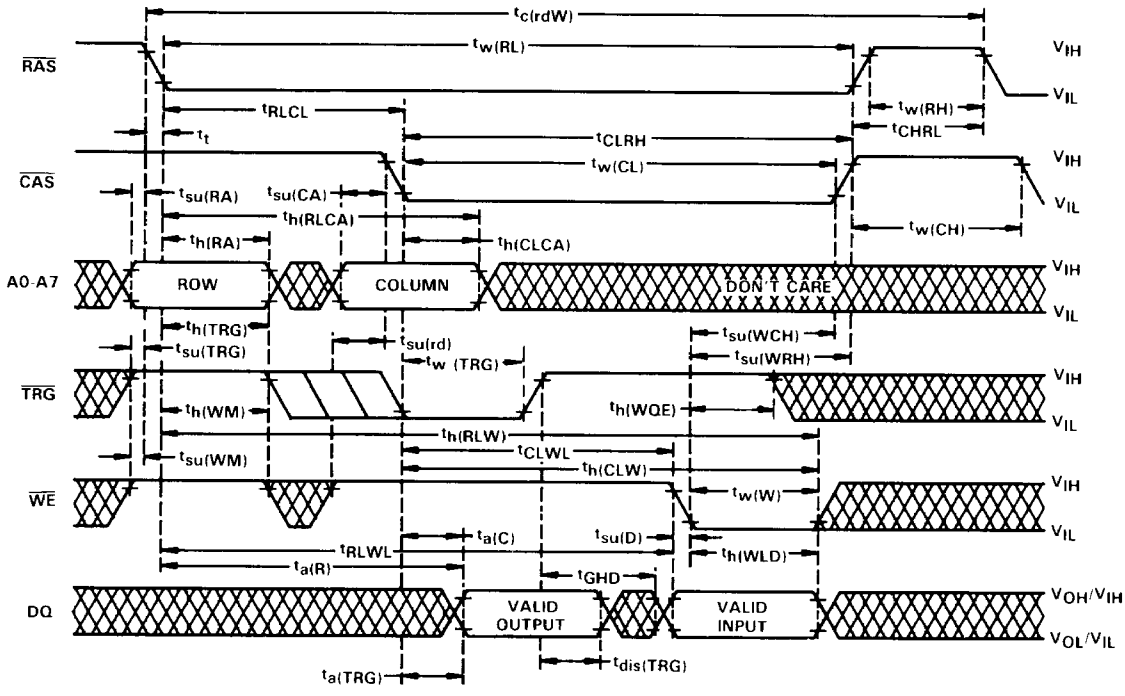
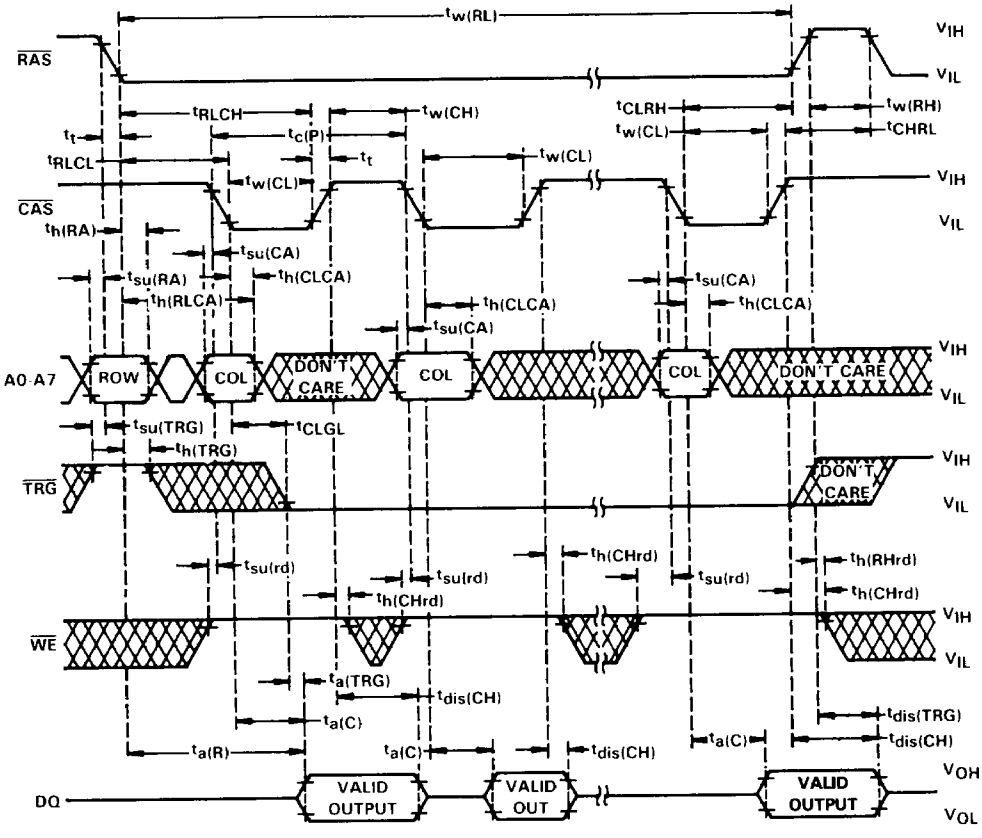
delayed write cycle timing, mask selected



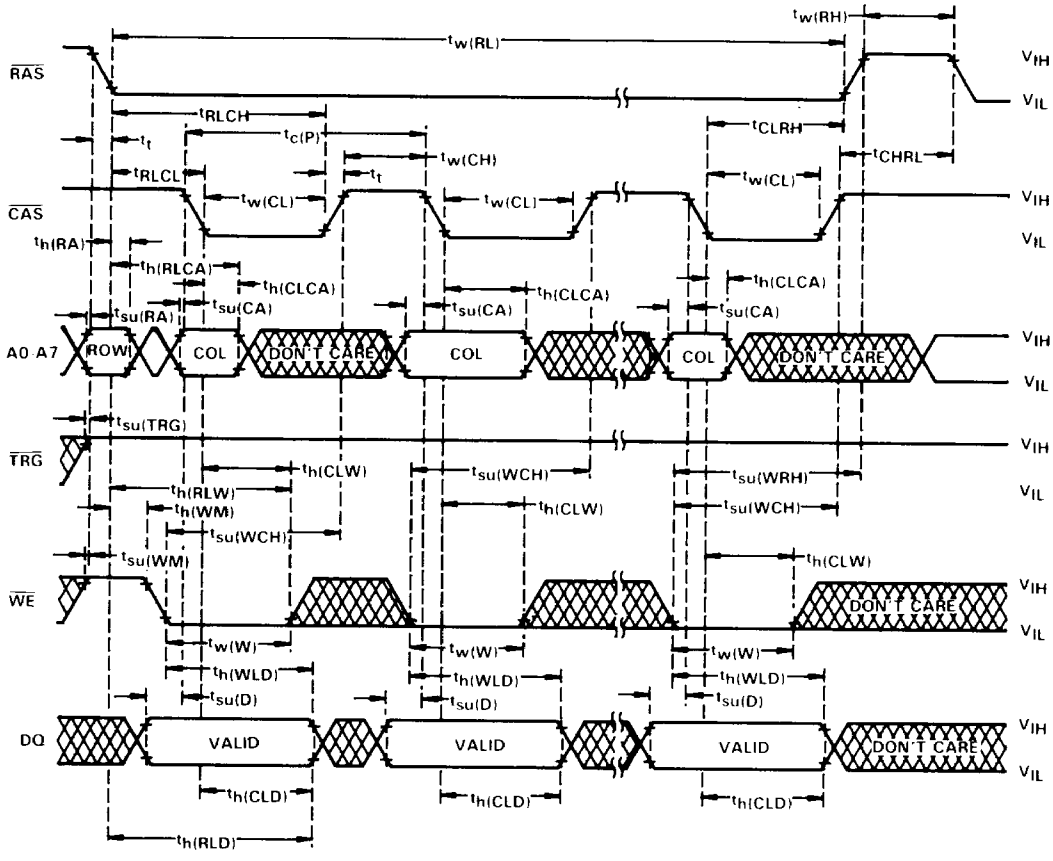
read-write/read-mofidy-write cycle timing



page-mode read cycle timing



page-mode write write cycle timing, write mask unselected



NOTE 7: Timing assumes use of the early write feature. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used to guarantee page-mode cycle time.

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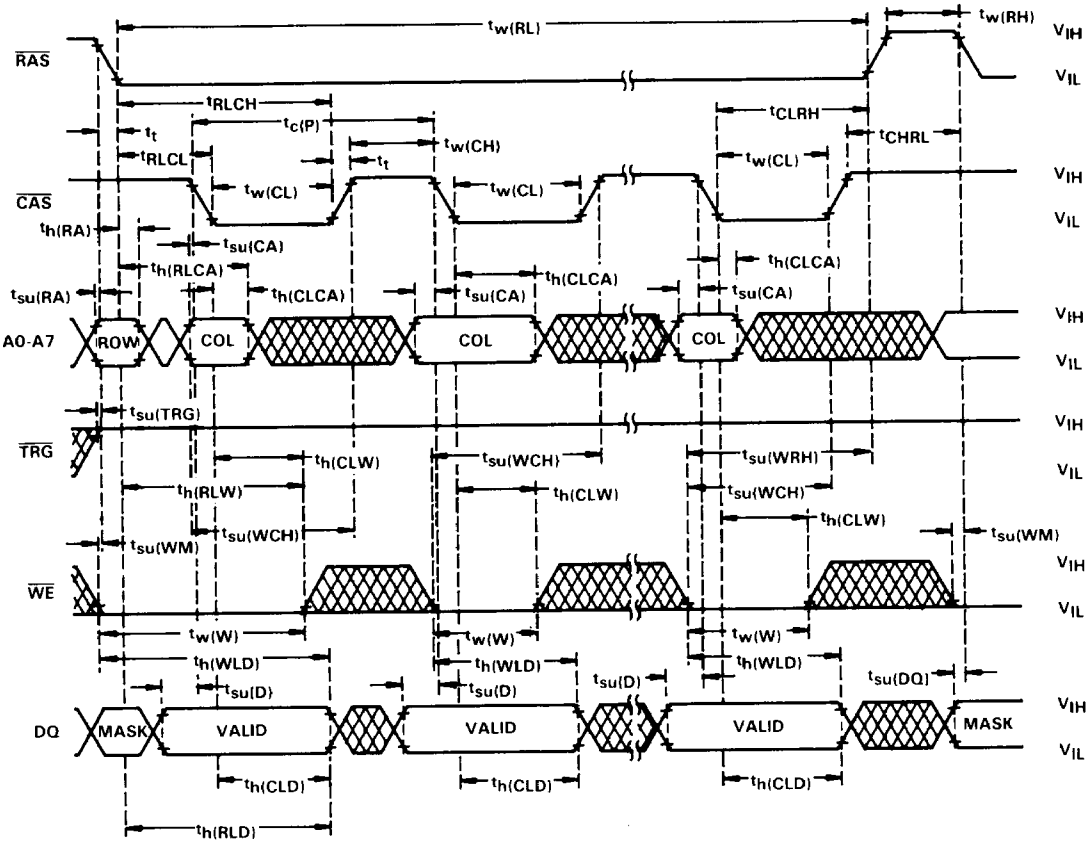
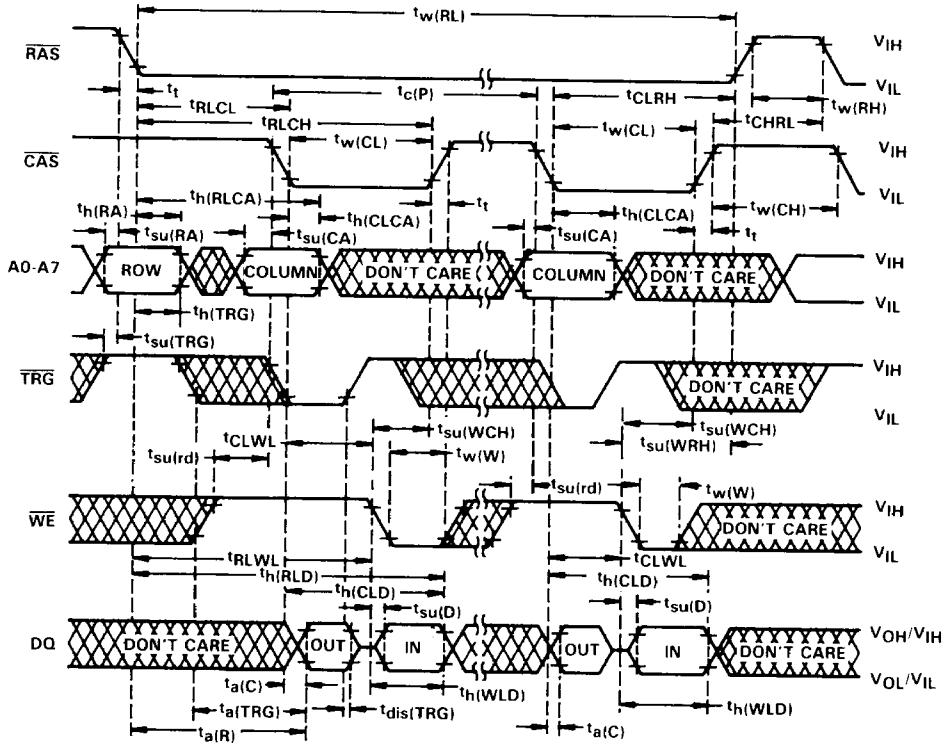
page-mode write cycle timing, write mask selected



NOTE 8: Timing assumes use of the early write feature. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used to guarantee page-mode cycle time. Timing also assumes that only those I/Os selected by DQ1-DQ4 on the falling edge of $\overline{RAS}$ are written during page-mode operation.

page-mode read-modify-write cycle timing



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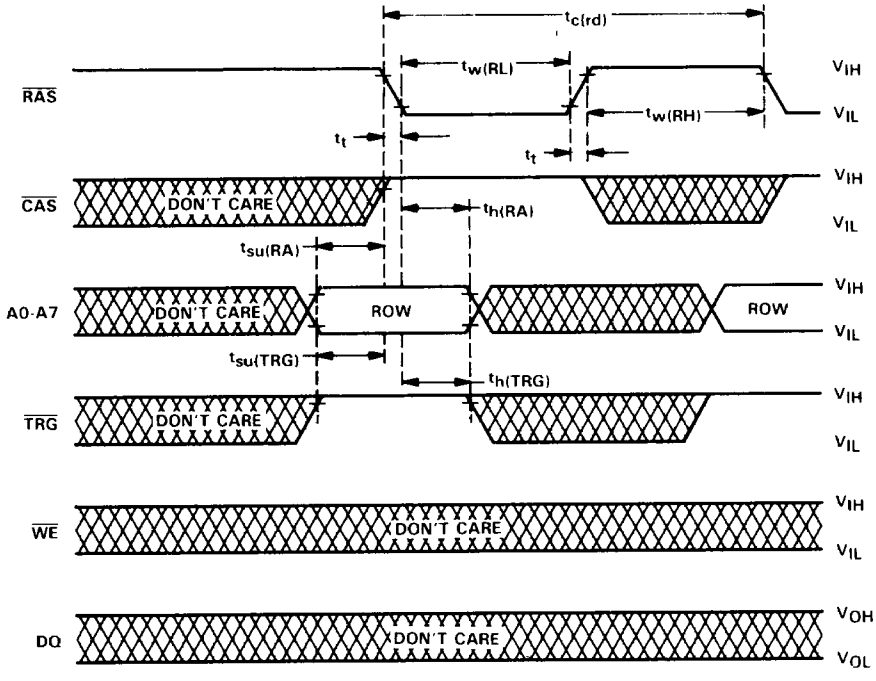
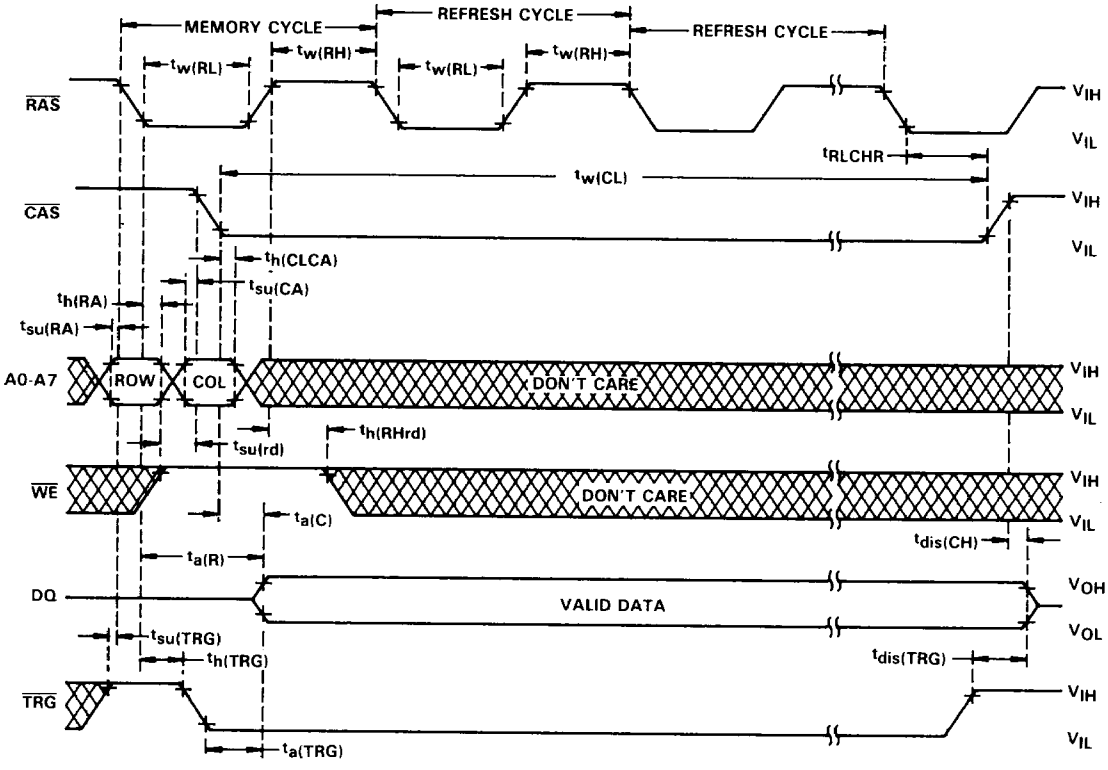
$\overline{\text{RAS}}$-only refresh timing



hidden refresh cycle timing



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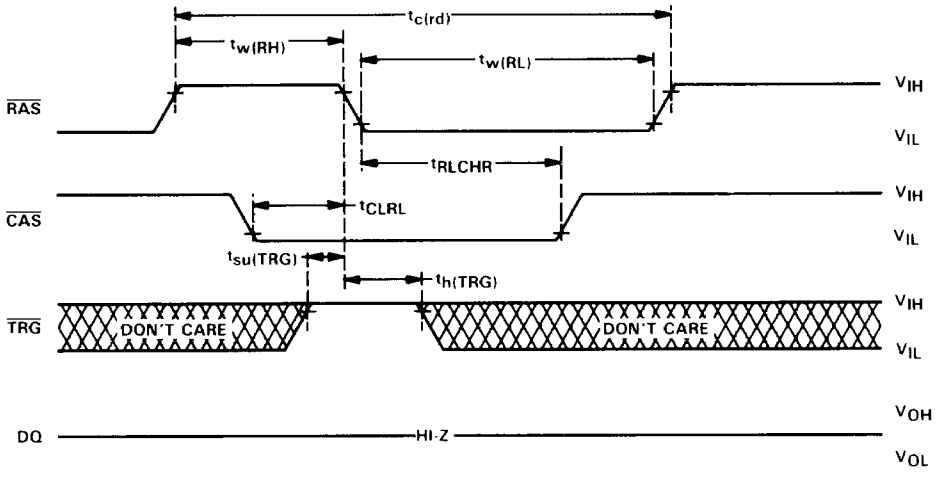
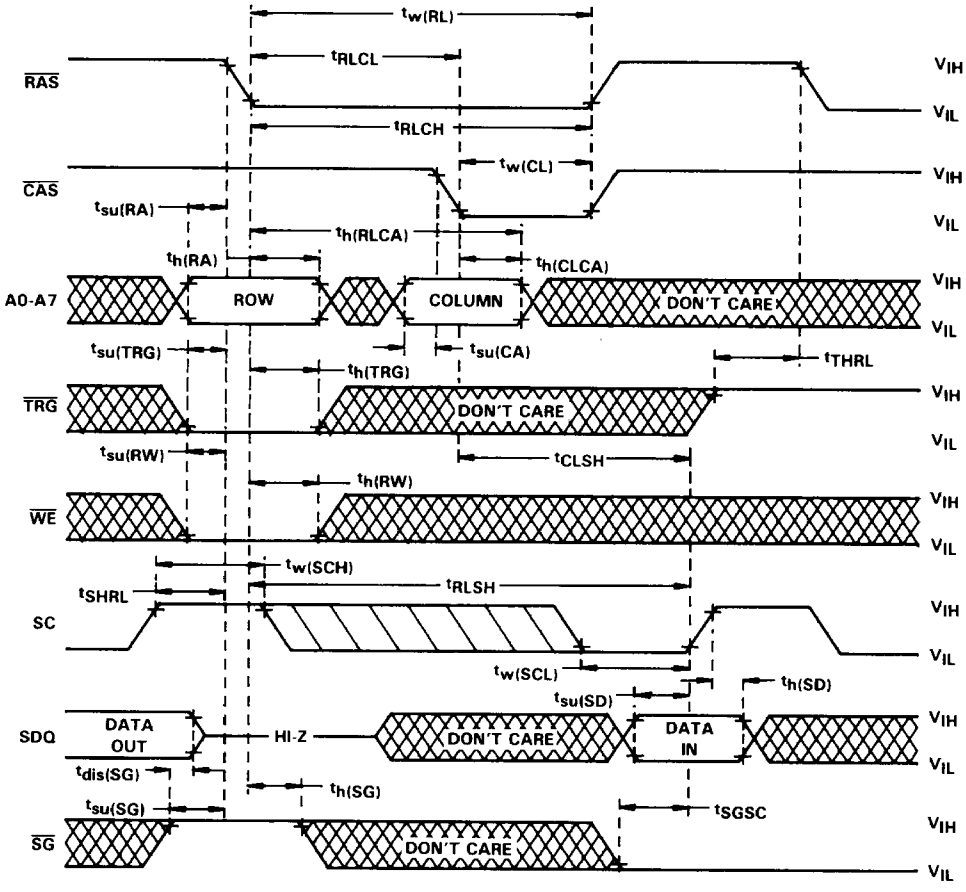
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh



write-mode control timing

The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 9. Random-mode (Q outputs) remain in 3-state for the entire write-mode control cycle.
10. $\overline{SG}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

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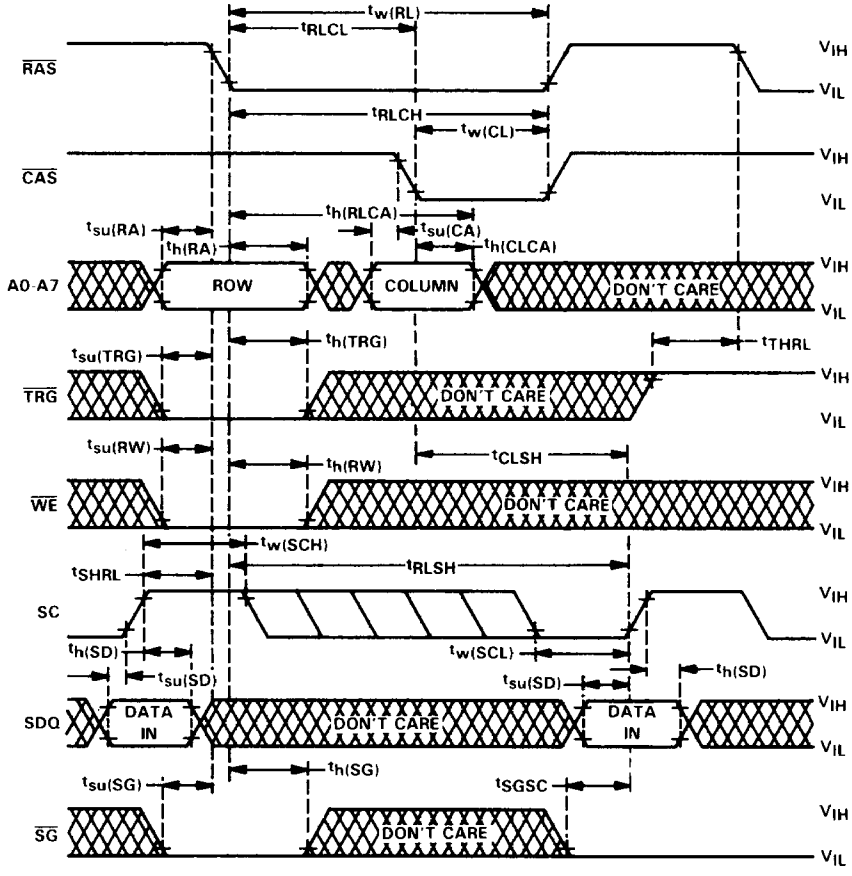
data-register-to-memory timing, serial input enabled

The data-register-to-memory cycle is used to transfer data from the data register to the memory array. Every one of the 256 locations in the data register is written into the 256 columns of the selected row. Note that the data that was in the data register may have arrived there either from a serial write in or from a parallel load of the data register from one of the memory array rows. The diagram below assumes that the device is presently in the serial-write mode (i.e., SD is enabled by a previous write-mode control cycle, thus allowing data to be written in).

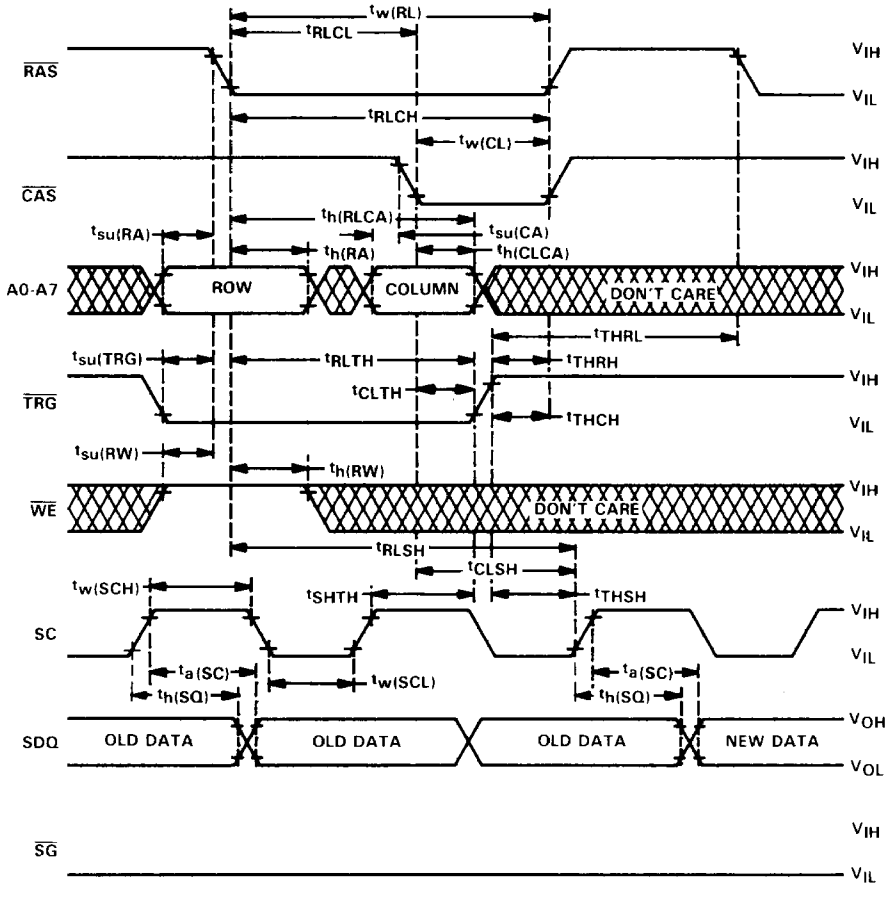


NOTES: 11. Random-mode (Q outputs) remain in 3-state for the entire data-register-to-memory transfer cycle.
12. $\overline{SG}$ must be high as $\overline{RAS}$ falls in order to perform a register-to-memory transfer.

memory-to-data-register timing

The memory-to-data-register cycle is used to load the data register in parallel from the memory array. Every one of the 256 locations in the data register are written into from the 256 columns of the selected row. Note that the data that is loaded into the data register may be either read out or written back into another row. This cycle puts the device into the serial read mode (i.e., the SQ is enabled, thus allowing data to be read out of the register).

Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.



NOTES: 13. Random-mode (Q outputs) remain in 3-state for the entire memory-to-data-register transfer cycle.
14. Column address must be supplied to load register start address on every transfer cycle.
15. The first positive transition of SC after $\overline{TRG}$ has gone high during a memory-to-register transfer cycle is used to read the first bit of new data.

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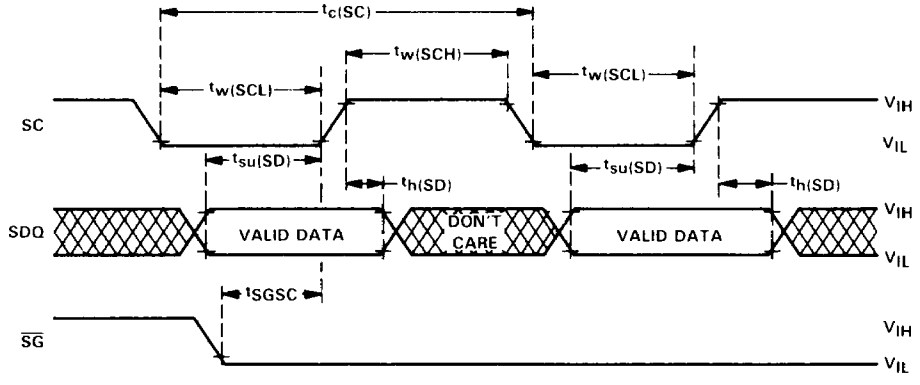
serial data-in timing

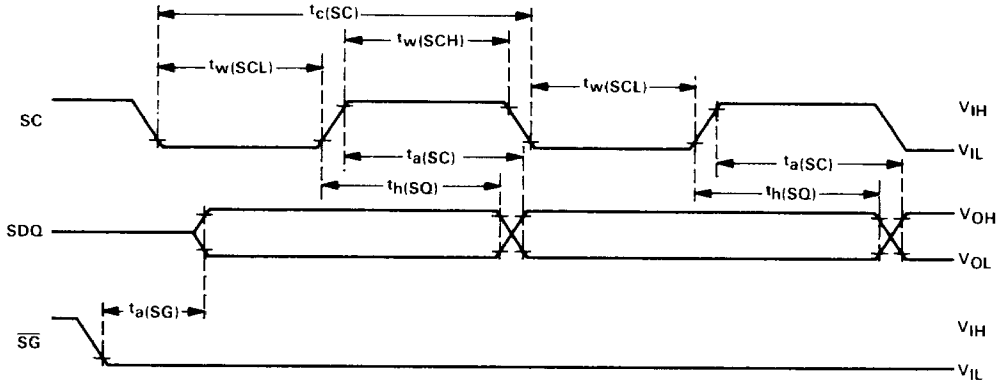
The serial data-in write cycle is used to write data into the data register. Before data can be written into the data register via SD, the device must be put into the write mode by performing a write-mode control cycle. Register-to-memory transfer cycles occurring between the write-mode control cycle and the subsequent writing in of data will not take the device out of the write mode. But a memory-to-register transfer cycle during that time will take the device out of the write mode and put it into the read mode, thus not allowing the writing in of data.



NOTE 16: While writing data into the data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-to-memory or memory-to-register data-transfer function.

serial-data-out timing

The serial data-out read cycle is used to read data out of the data register. Before data can be read out via SQ, the device must be put into the read mode by performing a memory-to-data-register transfer cycle. Register-to-memory transfer cycles occurring between the memory-to-register transfer cycle and the subsequent reading out of data will not take the device out of the read mode. But, a write-mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading out of data.



NOTE 17: While reading data out of the data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-to-memory or memory-to-register data-transfer operation.

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