ELC 363 - LABORATORY #4

ARM ALU

In this laboratory, a 64-bit ALU that you can use later to build one of the processors studied in ELC451 will be implemented and verified in Verilog® using an as high as possible level of abstraction design methodology.

The design approach should be bottoms-up and this implementation will not support overflow detection.

The function table of the ALU is as follows:

ALU control	Function
0000	AND
0001	OR
0010	add
0110	subtract
0111	Pass input b
1100	NOR

An additional requirement is that the ALU has an active high output that is asserted when the result is zero.

After you have designed the ALU, the next step is to write a test bench to verify the design. The minimum deliverables for this laboratory are the following:

a) All Verilog® code.

b) Waveforms that show that the ALU works for all functions.

A report with, at a minimum, all the items requested to be turned in is to be submitted by each team by the

due date discussed in class. All reports should be written in a word processor and similar productivity computer tools; no hand-written reports will be accepted.

GRADING RUBRIC: The total grade for this assignment will be 18 points normalized to 100% for your report. Parts (a) and (b) above will be worth 6 points each. The rest of your report will be worth 6 points, for a total of 18 points.

REPORT FORMAT: Free form, but it must be:

a. One report per team.

b. Have a cover sheet with identification: Title, Class, Your Name, etc.

c. COMPLETELY word-processed

d. Double spaced

e. 12 pt Times New Roman font

f. Fully justified (optional)

g. Outline of the body of the report: Introduction, Problem Description, Results, Discussion, and Conclusions.