DMA: Direct Memory Access

CPU → memory movment instructions

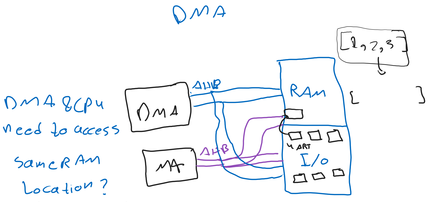
ex: uart → string [RAM]
peripheral memory

ex: usb to TTL : uart 250MHz → USB 1MHz

ex: DAC → Audio → GPIO
arr

Goal: to offload CPU from memory movment instructions

DMA

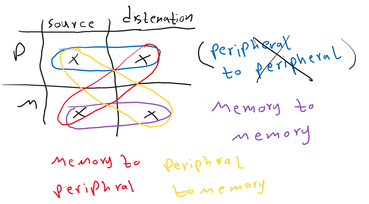


DMA & CPU need to access same RAM location?

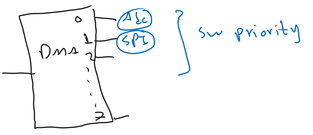
DMA → because CPU (fetch/decode/excute)

DMA peripheral

source → destination
* peripheral
* memory

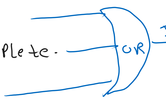


DMA → channels or streams



DMA flags:

TC : transmission complete.
HTC: Half transmission complete.
TE: transmission error



ISR per stream

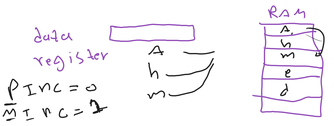
ISR{
if (TC==1)
{
}
elsif(HTC==1)
{
}

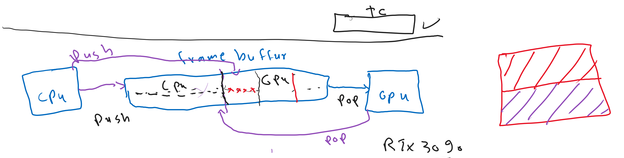
element size:
↳ 8-bit
↳ 16-bit
↳ 32-bit

Source element size	destination element size	
8-bit	8-bit	normal
8-bit 0x5A	16-bit 0x005A	un packing
16-bit 0x ~~5A~~ 4B 0x ~~0A~~ 5A	8-bit 0x 4B 0x5A	Packing

Block size
no of elements [4]
↳ Max → 2^{16} → 65535

Pointer Arthemitic





RTx 309.
8616A

12 frame

HTC ← Half transmission complete

double buffer → HTC
↳ double buffer mode.