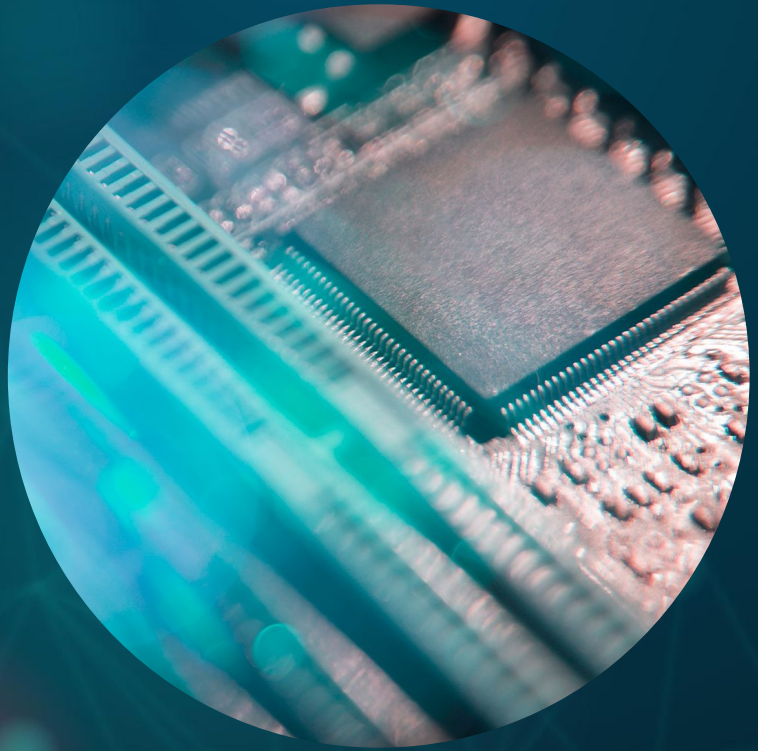
ARM Based Microcontroller

RCC

Lecture 2



Advanced RISC Machines

Clock 01

Reset Clock and Control

Clocks

The optimum clock source for a particular application is determined by a combination of factors including accuracy, cost, power consumption and environmental requirements. The following table summarizes the common oscillator types discussed, together with their strengths and weaknesses.

- Crystal Oscillator
- Ceramic Oscillator
- RC Oscillator

Clocks

Clock Source	Crystal Oscillator	Ceramic Oscillator	RC Oscillator
Accuracy	**Medium to High**	Medium	Very Low
Cost	High Cost	Lower Cost	**Lowest Cost**
Settling Time	**Very Low**	Medium	High
Temperature Immunity	**Insensitive to temperature**	**Insensitive to temperature**	Sensitive to temperature
Electromagnetic Interference	**Insensitive to EMI**	**Insensitive to EMI**	Sensitive to EMI
Vibration	sensitive to Vibration	sensitive to Vibration	**InSensitive to Vibration**

RCC Introduction

02

Reset Clock and Control

Reset and Clock Control (RCC)

The **RCC** peripheral is used to control the internal peripherals, as well as the reset signals and clock distribution. The RCC gets several internal (LSI, HSI and CSI) and external (LSE and HSE) clocks. They are used as clock sources for the hardware blocks, either directly or indirectly, via four PLL that allow to achieve high frequencies.

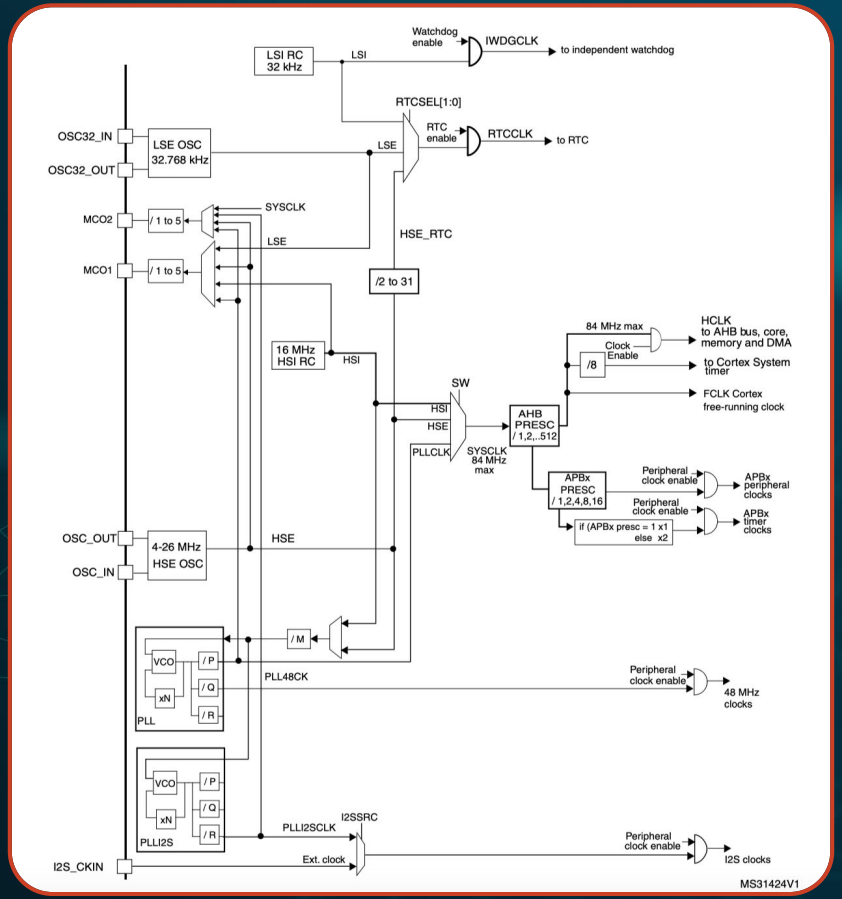
There are three clock sources can be used to drive the system clock (SYSCLK):

- **HSI** oscillator clock
- **HSE** oscillator clock
- **PLL** clock

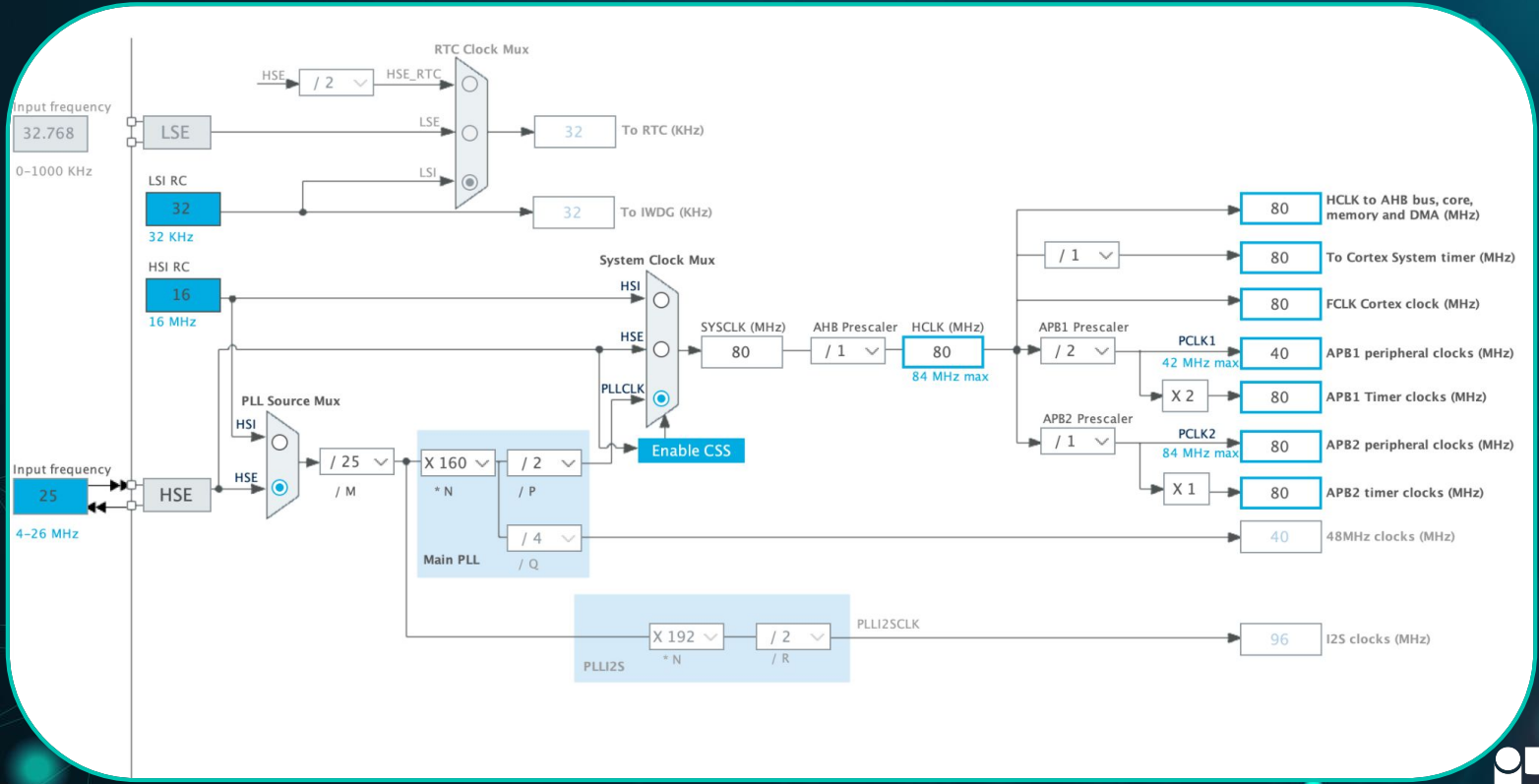
The devices have the following two secondary clock sources:

- 40 kHz low speed internal RC (LSI RC) which drives the independent watchdog and optionally the RTC used for Auto-wakeup from Stop/Standby mode.
- 32.768 kHz low speed external crystal (LSE crystal) which optionally drives the real time clock (RTCCLK)

Reset and Clock Control (RCC)



Reset and Clock Control (RCC)



STM32 Clocks 03

Reset Clock and Control

HOW DO WE DO IT?

HSE
High Speed External clock

HSI
High Speed Internal clock

LSE
Low Speed External clock

PLL
Phase Locked Loop Clock

Low Speed Internal clock
LSI

HSI

High Speed Internal clock (HSI):-

HSI is a high-speed internal clock, is generated from an internal RC oscillator, with a frequency of 16 MHz and low accuracy and can be used directly as a system clock or as PLL input. The HSI RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator however, even with calibration the frequency is less accurate than an external crystal oscillator or ceramic resonator.

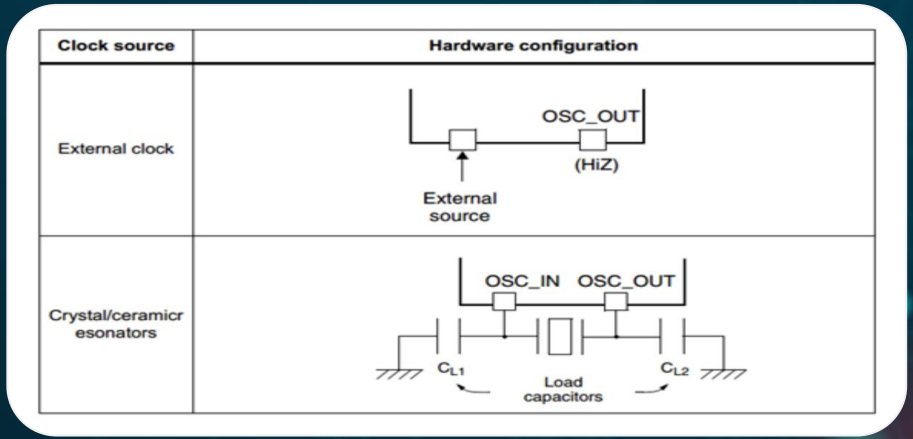
HSI is implemented using RC approach (Resistor and Capacitor)
We don't recommend using **HSI** as your clock source.

HSI

High Speed External clock (HSE):-

The high speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator
- HSE user external clock



Why HSE is better ?

They are more accurate over a wider temperature range, they have far less jitter (cycle by cycle timing precision) and in general are more accurate to within very good tolerances of the required frequency. If you then are multiplying this reference by many times to get the final clock speed in your processor, any error or inaccuracy of the clock source would be multiplied too, possible giving huge offsets in real vs intended frequencies and larger than acceptable clock jitter during time sensitive things such as high speed synchronous communications or asynchronous with timeouts.

External crystals (usually Quartz) or resonators (usually ceramic, have less awesome tolerances but are still better than internal RC oscillators) are quite cheap and can have very small footprints like the Murata Ceralock series ceramic resonators.

HSE

External source (HSE bypass):-
In this mode, an external clock source must be provided. It can have a frequency of up to 50 MHZ.
The external clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC_IN pin while the OSC_OUT pin should be left hi-Z.

External crystal/ceramic resonator (HSE crystal):-
The 4 to 26 MHz external oscillator has the advantage of producing a very accurate rate on the main clock.

PLL

PLL is a clock generation engine in the MCU which is used to generate the clock speed which is much higher than the internal **HSI** or external clock **HSE**. In MCU, most of the peripheral like USB,Ethernet PHY cannot work if you clock the MCU by low speed HSI or HSE. So, in those cases you can take the help of PLL.

Remember that in MCU PLL is not enabled by default, it must be configured before you use it.
The **PLL** configuration (selection of HSI oscillator or HSE oscillator
for PLL input clock, and multiplication factor) must be done before enabling the PLL. Once the PLL is enabled, these parameters cannot be changed.

Frequency doubling can be chosen as 2 to 16 times, but the maximum output frequency should not exceed 84MHz.

LSE

LSE clock:-

The LSE crystal is a 32.768 kHz Low Speed External crystal or ceramic resonator. It has the advantage providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

External source (LSE bypass):-
In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHZ.
The external clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC32_IN pin while the OSC32_OUT pin should be left Hi-Z.

LSI

LSI clock:-

The LSI RC acts as a low-power clock source that can be kept running in Stop and Standby mode for the independent watchdog (IWDG) and Auto-wakeup unit (AWU). The clock frequency is around 32 kHz.

System clock (SYSCLK) selection

After a system reset, the HSI oscillator is selected as system clock. When a clock source is used directly or through the PLL as the system clock, it is not possible to stop it.

A switch from one clock source to another occurs only if the target clock source is ready (clock stable after startup delay or PLL locked). If a clock source which is not yet ready is selected, the switch will occur when the clock source will be ready.

STM32 Buses 04

Reset Clock and Control

STM32 Buses

AHB

APB1

APB2

Overview

AHB stands for Advanced High-performance Bus and APB stands for Advanced Peripheral Bus. Both the Advanced High-performance Bus and the Advanced Peripheral Bus are part of the Advanced Microprocessor Bus Architecture (AMBA). Though both the AHB and the APB belong to AMBA, they differ in many ways.

When talking of the difference between the two, the AHB uses a full duplex parallel communication whereas the APB uses massive memory-I/O accesses.

Both the AHB and the APB are on chip Bus standards. The Advanced High-performance Bus is capable of waits, errors and bursts. The ADH, which is pipelined, mainly connects to memories.

Overview

When comparing the usage, the APB is simpler than the AHB. Unlike the AHB, there is no pipelining in APB. The APB is mainly proposed for connecting to simple peripherals. Looking at the AHB and the APB, it can be seen that the APB comes with a low power peripheral.

It can also be seen that Advanced Peripheral Bus is sometimes optimized for reduced interface complexity and minimal power consumption for supporting peripheral functions. This Bus can also be used in union with either
version of the system bus.

When looking at the features of AHB, it has a single edge clock protocol, several bus masters, split transactions, single-cycle bus master handover, burst transfers, large bus widths and non-tristate implementation.

Overview

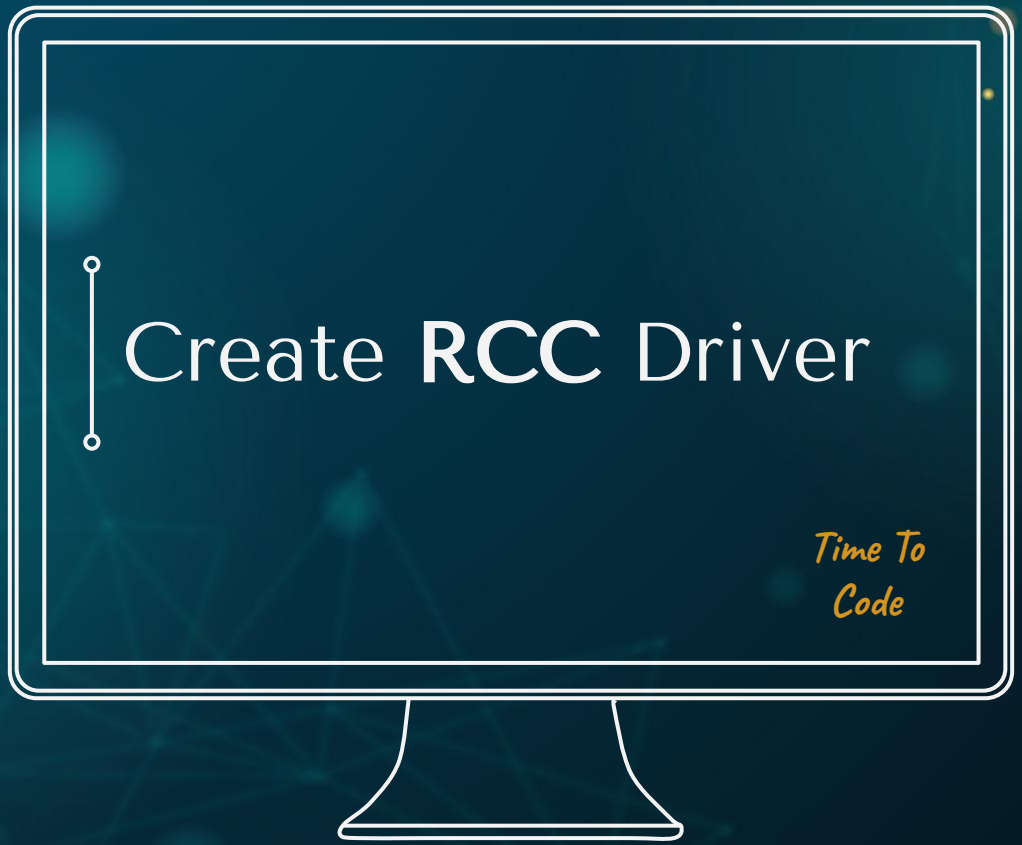
In AHB, the transaction consists of an address phase and a data phase. In case of AHB, there is only one Bus master at a time.
When compared to Advanced High-performance Bus, the Advanced Peripheral Bus is only used for low bandwidth control accesses. Though the APB has an address phase and data phase as like that of the AHB, it comes with a list of low complexity signal.

Summary

1. AHB stands for Advanced High-performance Bus and APB stands for Advanced Peripheral Bus.
2. When the AHB uses a full duplex parallel communication, the APB uses massive memory-I/O accesses.
3. The ADH, which is pipelined, mainly connects to memories. The APB is mainly proposed for connecting to simple peripherals.
4. When comparing the usage, the APB is simpler than the AHB.
5. Unlike the AHB, there is no pipelining in APB.
6. When compared to Advanced High-performance Bus, the Advanced Peripheral Bus is only used for low bandwidth control accesses.
7. Though the APB has an address phase and data phase as like that of the AHB, it comes with a list of low complexity signal.

STM32
Is AWESOME

Session LAb



THANKS!

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