# Jovan Stojkovic

## Curriculum Vitae

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### Research Interests

I have been working on novel hardware and software abstractions in data-center architectures. My focus is on cloud computing data platforms and deployment paradigms, such as microservices and serverless computing. I enjoy building systems and exploring ways to make them fast, reliable, and efficient in a holistic manner: from the hardware architecture up to the platform and application level.

## Education

August 2020 - University of Illinois at Urbana Champaign.

Present PhD in Computer Science

Advisor: Professor Josep Torrellas

**GPA**: 4.0/4

Passed Qualifying Exam: October 2021

2016 - 2020 School of Electrical Engineering, University of Belgrade, Serbia.

B.S. in Electrical and Computer Engineering

Awards: Best student of Computer Engineering and Information Theory Department for years:

2017, 2018, 2019 and 2020

**GPA**: 9.89/10

2012 – 2016 High School Bora Stankovic, Vranje, Serbia.

Applied Sciences and Mathematics

Award: Best student

**GPA**: 5/5

## Awards and Honors

- October 2022 Invitation to give a talk at the Workshop on the Future of Computer Architectures (FOCA), IBM Research, Yorktown Heights, NY.
- 2022-2023 **Student Travel Grants**, International Symposium on High-Performance Computer Architecture (HPCA'23), International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'23, '22), International Symp. on Microarchitecture (MICRO'22).
- April 2022 **Kenichi Miura Award Excellence in High Performance Computing**, Department of Computer Science, University of Illinois at Urbana-Champaign.
- April 2020 **Best Research Artifact Award**, International Conference on Information Processing on Sensor Networks (IPSN).
- 2017, 2018, Best Student of Computer Engineering and Information Theory Department Award,
  - 2019, 2020 School of Electrical Engineering, University of Belgrade.
- o July 2016 Bronze medal in 48th International Chemistry Olympiad, Tbilisi, Georgia.
- September II degree for research work in the field of Biology, XX Annual Bios Olympiad, St. Peters-2015 burg, Russia.
- o Stipend for Young Scientist/Researcher, from Serbian Ministry of Education, Science and Technological Development.

- O Numerous Gold, Silver and Bronze Awards at National Level Competitions in Physics, Chemistry, Biology and Mathematics.
- December Serbian Academy of Sciences and Arts Award for Results at International Olympiads.
- O December Serbian Chemistry Society Award. 2016
- July 2017 Dositeja Award from Young Talent Fund of the Republic of Serbia.
- o January 2015 St. Sava Award for the Best Student of Pcinja District.

## Publications

- **J. Stojkovic**, C. Liu, M. Shahbaz, J. Torrellas, " $\mu$ Manycore: A Cloud-Native CPU for Tail at Scale", *In Proceedings of the 50th International Symposium on Computer Architecture (ISCA)*, June, 2023.
- **J. Stojkovic**, T. Xu, H. Franke, J. Torrellas, "MXFaaS: Rethinking Resource Sharing in Serverless Environments for Parallelism and Efficiency", *In Proceedings of the 50th International Symposium on Computer Architecture (ISCA)*, June, 2023.
- **J. Stojkovic**, T. Xu, H. Franke, J. Torrellas, "SpecFaaS: Accelerating Function-as-a-Service Applications with Speculative Function Execution", *In Proceedings of the 29th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, February, 2023.
- **J. Stojkovic**, N. Mantri, D. Skarlatos, T. Xu, J. Torrellas, "Memory Efficient Hashed Page Tables", *In Proceedings of the 29th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, February, 2023.
- **J. Stojkovic**, D. Skarlatos, A. Kokolis, T. Xu, J. Torrellas, "Parallel Virtualized Memory Translation with Nested Elastic Cuckoo Page Tables", *In Proceedings of the 27th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March, 2022.*
- G. Lan, Z. Liu, Y. Zhang, T. Scargill, **J. Stojkovic**, C. Joe-Wong, M. Gorlatova, "Edge-assisted Collaborative Image Recognition for Mobile Augmented Reality", *ACM Transactions on Sensor Networks*, February, 2022.
- Z. Liu, G. Lan, **J. Stojkovic**, Y. Zhang, C. Joe-Wong, M. Gorlatova, "CollabAR: Edge-assisted Collaborative Image Recognition for Mobile Augmented Reality," *In Proceedings of the International Conference on Information Processing on Sensor Networks (IPSN)*, April, 2020.  **Best Research Artifact Award**
- **J. Stojkovic**, M. Misic, J. Protic, "Collaboration Network Analysis of Scientific Production at UB-SEE", *In 27th Telecommunications forum (TELFOR)*, November 2019.
- **J.Stojkovic**, D. Stojkovic, "Combined Infusions of Plants, Traditionally Used for Fever in Serbia, Inhibit the Growth of Pathogenic Bacteria", *In XX INTERNATIONAL BIOS Youth Olympics, Saint Petersburg, Russia*, September 2015.

## Workshops, Posters, Demo

- **J. Stojkovic**, C. Liu, M. Shahbaz, J. Torrellas, "Hardware Support for Efficient and Secure Resource Harvesting in the Cloud", *In 5th Young Architect Workshop (YArch'23) in conjunction with ASPLOS'23*, March 2023.
- **J. Stojkovic**, T. Xu, H. Franke, J. Torrellas, "Super Scalar Clouds", *In 7th Workshop on the Future of Computing Architecture (FOCA'22)*, November 2022.
- J. Stojkovic, J. Torrellas, "Nested Elastic Cuckoo Page Tables", NSF Arch-1 Workshop, March 2022.
- **J. Stojkovic**, Z. Liu, G. Lan, C. Joe-Wong, M. Gorlatova, "Demo: Edge-assisted Collaborative Image Recognition for Augmented Reality," *In ACM Conference on Embedded Networked Sensor Systems (SenSys)*, November 2019, https://www.youtube.com/watch?v=RFCxe9ZAVQw .

# Research Experience

o May – August Intern, Azure Systems Research, Microsoft Research, Advisors: Dr Inigo Goiri and Dr 2023 Chetan Bansal, Virtual Machine Overclocking in the Cloud, Redmond, WA.

- May August Intern, Hybrid Cloud, IBM Research, Advisor: Dr Hubertus Franke, Efficient and Performant 2022 Serverless Computing, Thomas J. Watson Research Center, NY.
- August 2020 Research Assistant at University of Illinois at Urbana-Champaign, Advisor: Professor Present Josep Torrellas, Rethinking Architecture and OS for Modern Virtualization Technologies.
- o May July **Duke ECE REU Program**, *Advisor : Professor Maria Gorlatova*, Edge Computing Platforms 2019 for the IoT and Collaborative AR.
- o School of Electrical Engineering, University of Belgrade, Advisor: Professor Marko Misic, Social and Collaboration Networks Analysis.

# Teaching Experience

2017 - 2020 Undergraduate Teaching Assistant.

School of Electrical Engineering, University of Belgrade

Courses: Computer Architecture, Computer Architecture and Organization, Object-oriented Programming, Operating Systems, Computer Networks, Probability and Statistics, Algorithms and Data Structures, Laboratory Exercises in Fundamentals of Electrical Engineering, Databases.

# Projects

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- o Hardware Support for Microservices in the Cloud (UIUC): Current processors are not designed for microservices, an emerging cloud-computing paradigm. Contrary to long-running monolithic applications, microservice environments execute short functions that only interact with one another via remote procedure calls and are subject to stringent tail-latency constraints. During the third year of my PhD, I designed 1) an architecture optimized for cloud-native environments that minimizes unnecessary architecture and removes contention hot-spots that degrade the tail latency ( $\mu$ Manycore, ISCA'23), and 2) a processor architecture that enables efficient and secure resource harvesting in the cloud ( $\mu$ Harvest, YArch'23).
- o **High-Performant Serverless Computing (UIUC and IBM)**: Current serverless workloads exhibit multiple levels of overheads, including cold start, virtualization, RPC, and the need to persist temporal outputs in remote storage. To make the matter worse, the overheads have significant cascading effects for applications that orchestrate multiple functions through control and data dependencies, which is a common practice in complex real-world applications. During the second and third year of my PhD, I redesigned serverless platforms by 1) applying data and control speculation techniques (SpecFaaS, HPCA'23), 2) creating a novel container abstraction that ensures high cpu, memory and I/O resource utilization while minimizing the response time (MXFaaS, ISCA'23), and 3) providing a systematic approach for mapping the unique characteristics of serverless workload to the design and organization of distributed caching scheme.
- Leveraging Parallelism in Virtualized Address Translation (UIUC): In spite of nearly twenty years since the inception of virtualization hardware, address translation still introduces substantial performance overhead in virtualized systems. A major reason why address translation has high overhead is because page tables are currently organized in a multi-level tree that is accessed in a sequential manner. This organization is called radix page tables. During my first year of PhD, I redesigned the virtual memory subsystem in virtualized environments to improve its 1) performance by exploiting available memory level parallelism (Nested ECPTs, ASPLOS'22) and 2) memory efficiency by breaking the hashed page table into multiple small allocation units while maintaining the same performance through carefully chosen design decisions (ME-HPTs, HPCA'23).
- Exploring the Design Space of Virtual Memory: Performance, Memory, Energy Efficiency, Security and Hardware Heterogeneity (UIUC): I did an extensive study of the virtual memory subsystem in virtualized environments and conducted sensitivity analyses on helper hardware structures. My results suggest that the current radix organization of page tables is not scalable with a large memory footprint workload. Moreover, I reproduced literature solutions to avoid hardware-based address translation and instead used compiler and runtime protection mechanisms. I also explored the virtual memory design for GPUs and available prefetching opportunities inherently exposed by the SIMT model of execution. Finally, I conducted a study on the security implications of different page table and TLB organizations with existing attack and defense schemes.
- Edge Computing Platform for Collaborative Augmented Reality (Duke): I built a platform that allows multiple users' related images, captured with Android phones running Google ARCore, to be processed jointly

on an edge server, improving user's quality of object recognition. Additionally, I improved performance by reusing cached results from the database. I also did comparative benchmarking of two image recognition tools (AWS Rekognition and Yolo) in terms of quality and time efficiency. I went further to explore possible trade-offs. The project was presented at Duke's REU Symposium and published at IPSN and SenSys.

o Compiler, Two-pass Assembler, Linker, Loader and Emulator (University of Belgrade and UIUC): I implemented front-end, middle-end and back-end components of compilers for the Micro Java and the Decaf programming language (strongly typed, object-oriented with polymorphism). The implementation includes several optimizations in LLVM: loop fusion, loop unrolling and graph coloring register allocation. I implemented a two-pass assembler with two-address instructions and syntax similar to x86 assembly, written in C++ with output file format based on the ELF file format. In addition, I wrote a linker, loader and interpretative emulator for a processor with Von Neumann architecture.

### Technical Skills

Programming languages: C, C++, Java, Python, Scala, Kotlin, Arduino, Assembly (x86 and ARM) Worked with FPGA, Arduino Uno, Raspberry Pi Created applications using JSF, Primefaces, Angular, JS, HTML/CSS

#### Miscellaneous

I speak Serbian, English and French. I have been playing tennis for fourteen years and I obtained license to coach children under the age of ten. During my primary education I played violin (for seven years) and was member of scouts. I was member of many non-governmental organizations such as Red Cross, Nexus and others. I love dogs and nature.