

Dielectric barriers for flexible CIGS solar modules

K. Herz^{a,*}, F. Kessler^a, R. Wächter^a, M. Powalla^a, J. Schneider^b, A. Schulz^b, U. Schumacher^b

^aZentrum für Sonnenenergie- und Wasserstoff-Forschung (ZSW), Hessbruehlstr. 21c, D-70565 Stuttgart, Germany

^bInstitut für Plasmaforschung (IPF) der Universität Stuttgart, Pfaffenwaldring 31, D-70569 Stuttgart, Germany

Abstract

Cu(In,Ga)Se₂ (CIGS)-based thin-film solar modules are commonly deposited on float glass substrates at temperatures of approximately 550°C. For the preparation of flexible and monolithically integrated solar modules on metal foils, the substrates first have to be coated by an electrically insulating barrier. In this study, dielectric barrier layers of Al₂O₃ and SiO_x were deposited on metal foils of Ti, Kovar[®] and ferritic Cr steel. The insulation properties were tested by sputtering small Mo contacts onto the barriers and measuring the resistance and breakdown voltages of the layers before and after CIGS deposition. Best insulating barriers could be achieved with 6-μm-thick combi layers of SiO_x (plasma CVD)/SiO_x (sol-gel) and SiO_x (plasma CVD)/Al₂O₃ (sputtered). These layers additionally act as diffusion barriers. Results of solar cell and module characterisation are presented to demonstrate the progress in barrier development. © 2002 Elsevier Science B.V. All rights reserved.

Keywords: Flexible solar modules; Cu(In,Ga)Se₂ (CIGS); Dielectric barrier; Electric insulation; Barrier resistance; Breakdown voltage

1. Introduction

Interesting and novel applications in photovoltaics are expected from thin and flexible solar modules, especially in the fields of space, aeronautic and mobile applications. Several efforts have been reported within the past years on the development of flexible and lightweight Cu(In,Ga)Se₂ (CIGS) modules [1–5], especially from the USA. Both the US and European activities were encouraged by relatively high small-area cell efficiencies obtained on polymer as well as on metallic substrates. An efficiency of $\eta = 12.8\%$ was reported [4] on a 20-μm thin polyimide film, and even 17.1% could be achieved on stainless steel substrates [1]. On bigger areas, a device with 8.4% efficiency from CIGS roll-coated onto a stainless steel substrate was realised [3].

Various materials, such as metals and polymers, were evaluated at ZSW to find appropriate foils fulfilling both technological and economic requirements. The

most interesting substrates are metal foils, since they can be coated in a roll-to-roll process at high temperatures of up to 600°C and under Se atmosphere [5]. However, the fabrication of monolithically integrated modules on electrically conducting substrates requires the deposition of a dielectric barrier [6]. The barrier has two functions: (a) to provide electrical insulation between the metal substrate and the monolithically interconnected solar cells; and (b) to reduce the diffusion of impurities from the metal substrate into the solar cells. To avoid short circuits and shunts between individual module cells, the barrier must guarantee good insulation and adhesion during all deposition steps, especially the high-temperature CIGS deposition. At ZSW, various barrier types, such as plasma-sprayed layers, high-temperature varnishes and enamel layers, were investigated. Beside such ‘thick’ barriers of >10 μm, ZSW and IPF also developed several thin dielectric barriers. The insulation properties are mainly influenced by the barrier thickness, the substrate type, the preparation techniques and the CIGS deposition process, as will be shown in this paper.

* Corresponding author. Tel.: +49-711-7870-216; fax: +49-711-7870-230.

E-mail address: konrad.herz@zsw-bw.de (K. Herz).

Table 1

Density, coefficient of thermal expansion (CTE), and surface roughness R_t of soda lime glass (SL) and metal foils

	SL	Ti	Kovar	Cr steel
Density (g/cm^3)	4.5	4.5	8.2	7.7
CTE (ppm/K)	$\cong 9$	8.6	5.9	10.5
R_t (nm)	10–15	1900	540	680

2. Experimental

2.1. Substrates and barrier layers

Sufficient adhesion of the barrier layers, Mo back contact layer, CIGS absorption layer, and ZnO window layer was found on metal substrates made of some ferritic stainless steels, Fe–Ni alloys, Ti, and Mo. In this study, we used 0.1–0.2-mm-thick metal foils of a ferritic Cr steel, Kovar[®], a Fe–Ni alloy and Ti. Table 1 presents some technical data for these substrates, such as density, coefficient of thermal expansion (CTE) and the maximum roughness R_t . For comparison, these data are also given for the standard substrate material, soda lime glass. All commercially available metal foils showed a relatively high maximum roughness of $R_t=500$ –1900 nm compared to glass substrates of $R_t=10$ –15 nm. The high roughness results from the rolling process and affects the insulation properties of the barrier layers. This was demonstrated in separate tests using polished substrates. For the tests described here, we consider only unpolished substrates.

On these substrates, insulating thick barriers of >10 μm , such as plasma-sprayed layers, high-temperature varnishes and enamel layers, were deposited (Fig. 1a–c). Due to their thickness, such barriers possess good electrical insulation, but often suffer from extreme surface roughness, cracks and reduced flexibility. These disadvantages could be overcome by thin barrier layers of <10 μm . As depicted in Table 2, thin films of Al_2O_3 and SiO_x were deposited onto metal foils of 10×10 cm^2 by different methods. The best success was attained by single- and multilayers prepared by RF-magnetron sputtering, sol–gel deposition, and plasma CVD techniques.

Metal foils of 10×10 cm^2 were sputter-coated at ZSW Stuttgart from an Al_2O_3 target with variations in sputter power (800–2000 W) and Argon pressure (3–7 μbar). For the preparation of double layers, the sputter process was interrupted by cleaning the sputtered surface of particles. The film thickness ranged from 1 to 3 μm .

Sol–gel deposition was carried out at Institut für neue Materialien (INM), Universität Saarbrücken, using a preparation process without special optimisation for the application described here. Metal foils of 10×10 cm^2 were dipped into a colloidal silica solution of Si-containing nanoparticles. A dense film of SiO_x was

formed by sintering the dipped foils at 500°C in air. The composition was close to stoichiometry ($x=2$). Beside single layers, double layers were also grown by repeating the whole process with a metal foil covered with a single layer. The film thickness was in the range of 3–7 μm .

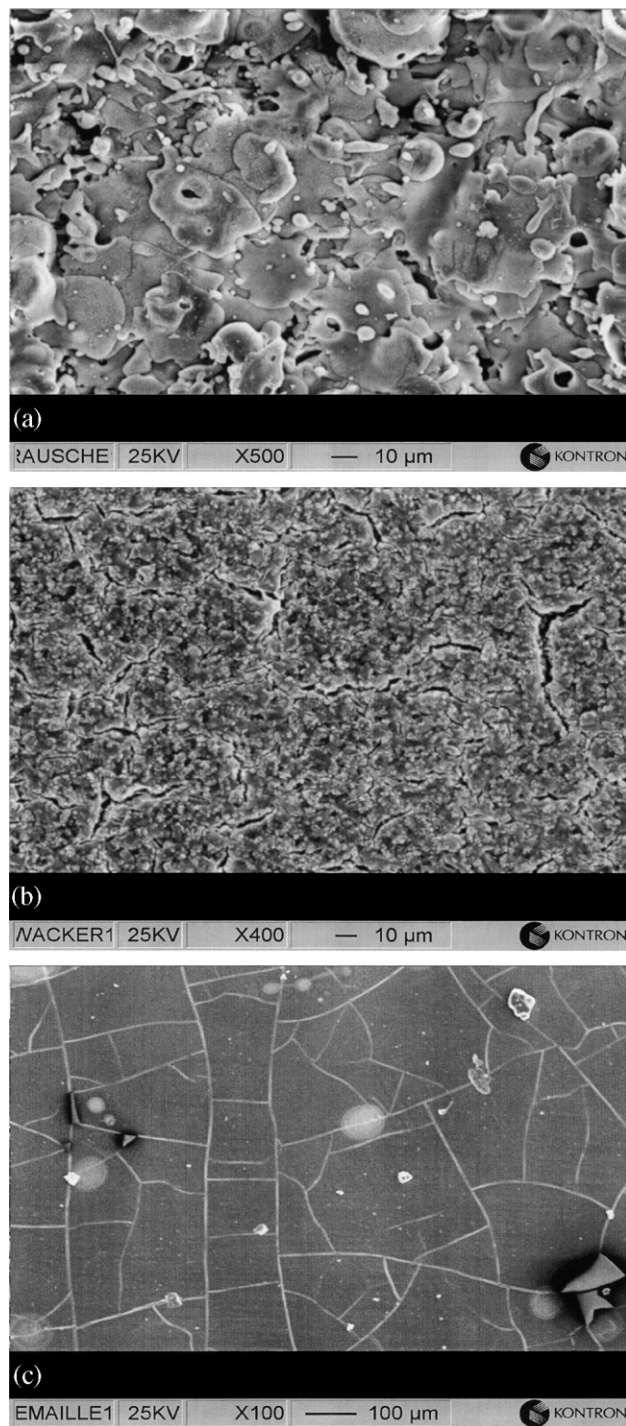


Fig. 1. (a) Plasma-sprayed layer on steel. (b) High-temperature varnish on Ti. (c) Enamel layer on Mo.

SiO_x layers were deposited on $10 \times 10\text{-cm}^2$ metal foils using low-pressure microwave plasma deposition with the Duo-Plasmatline [7]. Quartz-like SiO_x films with $x \cong 2$ have been deposited using oxygen and hexamethyldisiloxane (HMDSO) with an $[\text{O}]/[\text{HMDSO}]$ ratio of 10–20. Multilayers of up to $6\text{ }\mu\text{m}$ were prepared by interrupting the deposition process by one (double layer) or three (quad layer) intermediate cleaning processes.

For further improvements, combi layers of a $3\text{-}\mu\text{m}$ -thick SiO_x plasma CVD layer (quad) as the basic layer and sol-gel SiO_x or Al_2O_3 films (double) as a second layer were prepared with a total thickness of approximately $6\text{ }\mu\text{m}$.

2.2. Characterisation of barriers

The insulation resistance R_d and the breakdown voltage V_r of the barrier layers were tested to characterise the insulation properties. For this purpose, approximately 90 small Mo contacts of $2 \times 2\text{ mm}^2$ were sputtered through a Ti mask onto stripes of $25 \times 100\text{ mm}^2$ cut from the barrier-coated metal foils. The Mo contacts were sputtered using the standard sputter process for the CIGS cell preparation. The barrier resistance was determined by connecting a usual ohmmeter (test limit $40\text{ M}\Omega$) to the metal contacts on the dielectric barriers and the metal substrate. The breakdown voltage was tested by touching the Mo contacts on the barriers with a steel tip and increasing the voltage between tip and substrate until a breakdown occurred (applied limits, 300 V and 15 mA). To investigate the influence of temperature and of the CIGS deposition process, the electrical insulation of barriers was also tested after annealing at 500, 550 and 600°C , as well as after evaporating a standard CIGS layer on each Mo contact using the same Ti mask.

2.3. Cell and mini module preparation

Standard Mo/CIGS/CdS/ZnO test cells of 0.23 cm^2 were deposited on Ti, Kovar® and Cr steel stripes of $25 \times 100\text{ mm}^2$ using sputtered Mo back contacts of approximately $0.6\text{ }\mu\text{m}$ in thickness. The CIGS deposition was performed in our standard inline machine without any external Na doping. For the study of electrical insulation, monolithically integrated mini modules were prepared on metal foils of that size by a special mask technique without application of any pat-

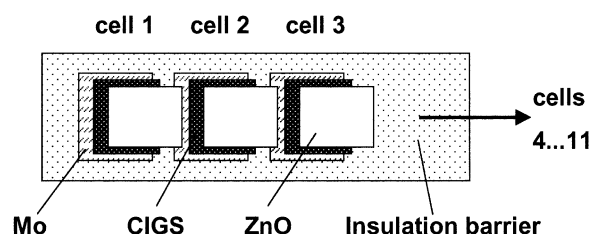


Fig. 2. Mini module preparation by mask technique.

terned process. The Mo back contact, CIGS layer and ZnO window layer were deposited by three different sized and overlapping steel and Ti masks (Fig. 2). Only the high-ohmic CdS film (50 nm) was deposited after CIGS preparation on the full area without masking. The width of CIGS and ZnO deposition was reduced compared to the Mo back contact. The active area of each module cell was 0.5 cm^2 . The remaining free edges on each side of the Mo contacts enabled measurement of the barrier resistance R_d after the CIGS deposition process, without damaging the CIGS layer. Moreover, the series resistances between each cell could be determined. Solar cells and mini modules were characterised by usual I - V measurements under AM1.5 equivalent illumination.

3. Results and discussion

3.1. Adhesion and morphology of barriers

Thin barrier layers usually have good adhesion to all the metal substrates investigated here. Only sol-gel SiO_x double layers often show cracks and delamination after tempering at $\geq 500^\circ\text{C}$. Occasionally, very fine cracks were observed in plasma CVD SiO_x layers on Kovar® in the as-grown state. The adhesion of Mo and CIGS on the barriers is usually sufficient to obtain satisfactory cell properties. Nevertheless, the mechanical stability is sometimes bad and these layers delaminate on touching. This was observed with Al_2O_3 barriers on Kovar® and SiO_x barriers (plasma CVD) on Cr steel. The reasons for delamination can be manifold, and have not been investigated in detail up to now. In contrast to plasma-deposited layers, sol-gel layers decrease the surface roughness by filling up scratches and small grooves. R_t values are decreased by a factor of up to four compared to the roughness of the metal substrates.

Table 2

Preparation of thin barrier layers on metal foils ($10 \times 10\text{ cm}^2$) of Ti, Kovar® and Cr steel

Barrier type	Thickness (μm)	Deposition process
Al_2O_3 single and double layers	1-3	RF magnetron sputtering
SiO_x single/double	3-7	Sol-gel deposition
SiO_x single/double/quad	1-6	Plasma CVD

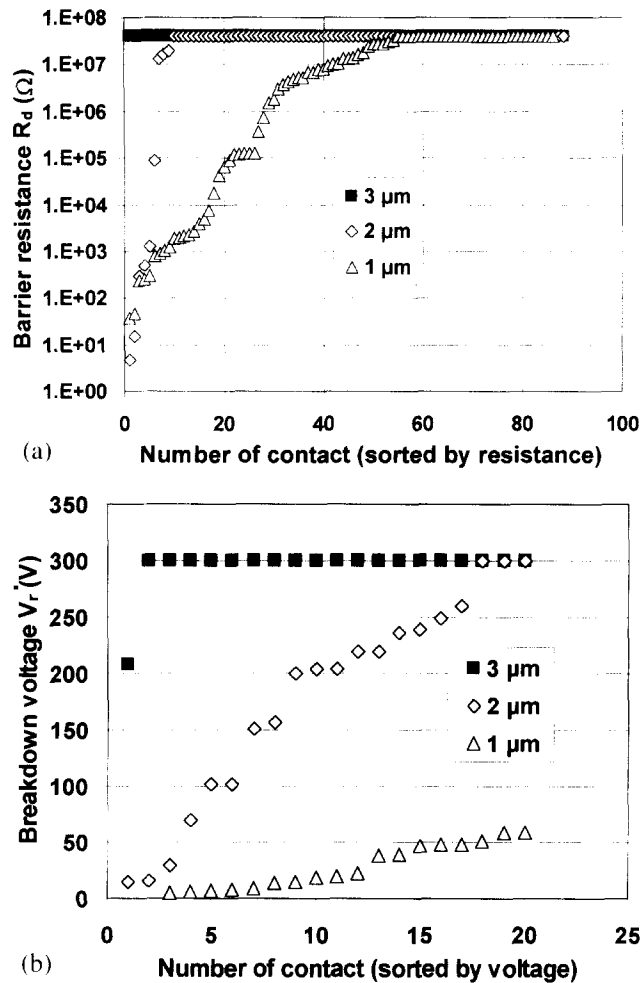


Fig. 3. (a) Barrier resistance of RF-sputtered Al_2O_3 layers on Kovar[®]. (b) Breakdown voltage of RF-sputtered Al_2O_3 layers on Kovar[®].

3.2. Insulation properties of barriers

Characteristic diagrams as shown in Fig. 3a,b for Al_2O_3 barriers on Kovar[®] substrates arise from sorting the barrier resistance values R_d and breakdown voltage data V_r by increasing values. The maximum possible values for R_d and V_r are the detection limit of the ohmmeter (40 M Ω) and the upper limit of the voltage generator for V_r (300 V), respectively. Values above these limits are represented by a horizontal line, as shown in Fig. 3a,b for the 3- μm barrier. For the 2- and 1- μm Al_2O_3 films, part of the values measured are below these upper limits, forming the 'lower-ohmic' and the 'lower-voltage' tail of the curves. The wider these tails and the lower their values, the worse is the insulation behaviour that is observed for the 1- μm Al_2O_3 barrier compared to the thicker ones. In particular, the breakdown voltages between 10 and 40 V are rather poor in contrast to the 3- μm barrier with a minimum value of 210 V.

Al_2O_3 barriers sputtered onto titanium yielded almost the same results, whereas the insulation properties on Cr steel were significantly worse [9], probably due to a greater mismatch of the thermal expansion coefficients of the barrier and substrate. Nevertheless, no cracks could be observed in the barrier layers. A preliminary ranking of the different barrier types was possible on the basis of such tests (Table 3). As just described, the insulation of 3- μm Al_2O_3 barriers is very good on Kovar[®], good on Ti and worse on Cr steel. SiO_x sol-gel layers are good on Cr steel and worse on Ti and Kovar[®]. Very good results for all metal foils were achieved with plasma CVD SiO_x barriers.

Severe degradation (decrease in R_d and V_r values) was observed with sol-gel-deposited SiO_x and sputtered Al_2O_3 layers when tempered at $\geq 500^\circ\text{C}$ for 30 min in vacuum. Better behaviour was observed with SiO_x quad barriers prepared by plasma CVD if they were at least approximately 3 μm thick. They could withstand temper processes in vacuum up to 550°C without significant degradation of the insulating properties ($R_d \geq 40 \text{ M}\Omega$, $V_r \geq 300 \text{ V}$). However, significant degradation was caused by CIGS deposition, proving that the combination of heat and the vapours of Se and metals stresses the barriers even more than heat alone.

One essential step forward could be attained by testing combi layers of a 3- μm -thick SiO_x plasma CVD layer as the basic layer and a sol-gel SiO_x or sputtered Al_2O_3 film of the same thickness as a second layer. A second layer formed by different nucleation and growth mechanisms probably decreases the pinhole density of the first layer. Test results of a 6- μm SiO_x (plasma CVD)/ SiO_x (sol-gel) combi layer on titanium are given in Fig. 4a,b. Barrier resistance was above 40 M Ω before deposition, and only two of approximately 90 values were found to be below this level after the deposition process. The same results apply for such barriers on Kovar[®] and Cr steel substrates. The breakdown voltages of such barriers on steel and Kovar[®] substrates were slightly reduced by CIGS deposition, but the remaining test values of $V_r > 60 \text{ V}$ would probably be sufficient for many applications.

Rather good results were achieved for 6- μm combi layers of the type $\text{SiO}_x/\text{Al}_2\text{O}_3$. In Fig. 5a,b, the barrier resistance values determined at the Mo back contacts ($6 \times 14 \text{ mm}^2$) of two mini modules (Cr steel and Kovar[®] substrate) are depicted before and after CIGS

Table 3
Qualitative assessment of insulation properties before heating

Barrier type	Ti	Kovar [®]	Cr steel
Al_2O_3 (double layer, 3 μm)	+	++	–
SiO_x sol-gel (single layer, 3 μm)	–	–	+
SiO_x plasma CVD (quad layer, 3 μm)	++	++	++

++ , very good; + , good; and – , worse.

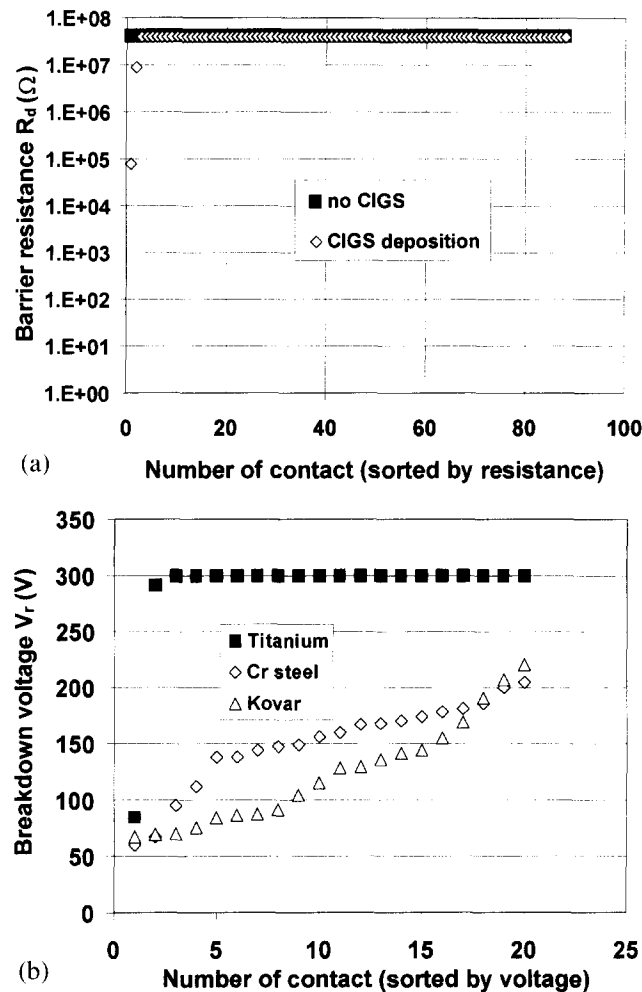


Fig. 4. (a) Barrier resistance of a 6- μm SiO_x combi layer (plasma CVD+sol-gel) on Ti before and after the CIGS deposition. (b) Breakdown voltage of a 6- μm SiO_x combi layer (plasma CVD+sol-gel) on Ti, Cr steel and Kovar[®] after the CIGS deposition.

deposition. Here, the values are not sorted by resistance, i.e. the numbers of contacts correspond to their real geometrical sequence. On Kovar[®], only the R_d value of contact number 2 (≥ 40 M Ω before CIGS deposition) was decreased to 15 k Ω , all others remain at ≥ 40 M Ω . On the steel substrate, R_d values of seven Mo contacts were decreased to values of > 1 M Ω . On Ti (not shown here), no decrease in R_d values was observed.

3.3. Solar cells and mini modules

On all metal substrates used, values for cell efficiency η of close to 11%, open circuit voltage V_{oc} of approximately 550 mV, short circuit current density j_{sc} of close to 30 mA/cm², and fill factors FF of up to 69% could be attained without Na doping (Table 4). The Al_2O_3 barriers used have no electrical function in this case, but act as a diffusion barrier [8] to reduce the diffusion of impurities from the metal substrates into the solar

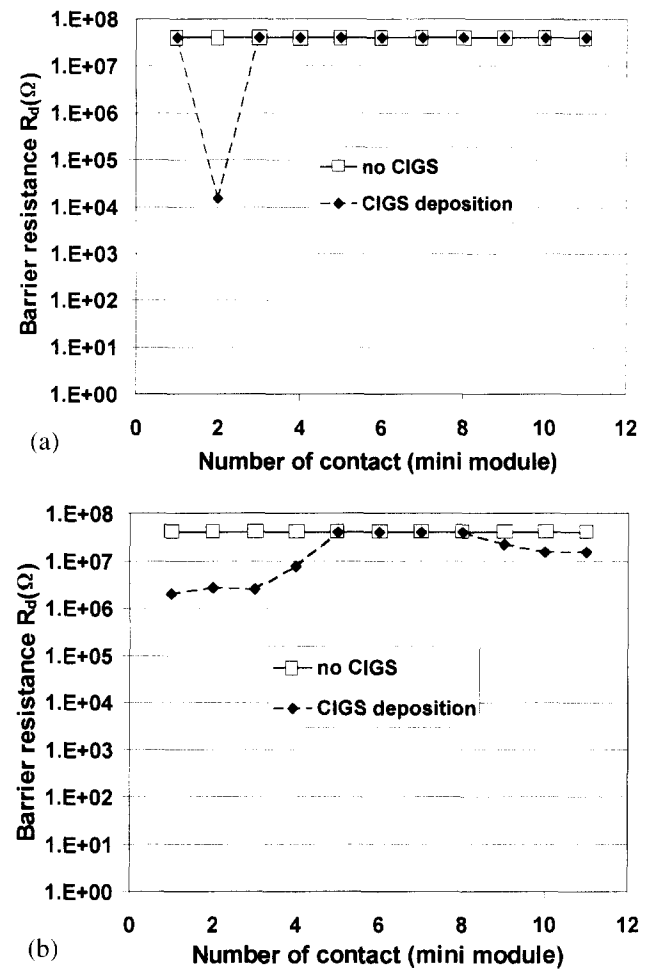


Fig. 5. (a) Barrier resistance before and after CIGS deposition: combi layer of 6- μm SiO_x (plasma CVD)/ Al_2O_3 (RF sputtered) on Kovar[®] substrate for mini module preparation. (b) Barrier resistance before and after CIGS deposition: combi layer of 6- μm SiO_x (plasma CVD)/ Al_2O_3 (RF sputtered) on Cr steel substrate for submodule preparation.

cells. Mini modules interconnecting 11 single cells of 0.5 cm² on these metal substrates showed V_{oc} of up to 5.4 V and j_{sc} of approximately 20 mA/cm². Mini modules suffered mainly from low fill factors, which seem to be a result of high series resistance and some shunt resistance caused by ZnO sputter arcs at the mask edges, but not insufficient insulation. The best mini module was attained on a steel substrate with 0.25-cm² cells after etching away the edges of ZnO. By interconnecting four such cells, open-circuit voltage V_{oc} = 2.15

Table 4
Solar cell properties on metal substrates using Al_2O_3 barriers

	Titanium	Kovar [®]	Cr steel
η (%)	10.8	10.7	10.9
V_{oc} (mV)	559	550	545
j_{sc} (mA/cm ²)	29.8	28.7	28.9
FF (%)	65.2	67.9	69.3

V, short-circuit current density $j_{sc}=26.5$ mA/cm², fill factor FF=42.0% and efficiency of $\eta=6.0\%$ were achieved. As single cells of mini modules generally show much better cell properties, we assume that significant further improvements will be possible in the near future. The probability of finding a defect within the insulation barrier, however, increases with the cell size. Therefore, the insulation for larger modules still has to be improved.

4. Conclusion

It is a great challenge to obtain perfect electrical insulation for the preparation of CIGS solar modules on metal substrates. High barrier resistance of ≥ 40 M Ω and breakdown voltage of ≥ 300 V could be achieved using dielectric combi layers (6 μ m thick) of two SiO_x films prepared by plasma CVD and sol–gel techniques, as well as combi layers of SiO_x (plasma CVD) and Al₂O₃ (RF sputtered). To minimise defects, such as pinholes and the inclusion of particles, the single layers were prepared with intermediate cleaning steps. The combination of two differently prepared layers obviously causes a further reduction in defects and stabilisation of the insulation properties. Results of *I*–*V* measurements on small cells and mini modules on metal substrates demonstrated the effectiveness of the barriers and the potential for further progress.

Acknowledgements

The authors acknowledge the support by the CIS group of ZSW and Dr Endress from INM, Universität Saarbrücken, for the preparation of sol–gel films. This work was supported by the European Commission under EC Contract No JOR-CT98-0304, the Ministerium für Wissenschaft, Forschung und Kunst Baden-Württemberg (MWK BW) and the ‘Stiftung Energieforschung Baden-Württemberg’.

References

- [1] M. Contreras, B. Egas, K. Ramanathan, J. Hiltner, F. Hasoon, R. Noufi, *Prog. Photovoltaics* 7 (1999) 311.
- [2] B.M. Basol, V.K. Kapur, C.R. Leidholm, A. Halani, *Sol. Energy Mater. Sol. Cells* 43 (1996) 93.
- [3] J. Britt, S. Wiedemann, R. Wendt, S. Albright, Technical Report NREL/SR-520-26840, 1999.
- [4] A.N. Tiwari, M. Krejci, F.J. Haug, H. Zogg, *Prog. Photovoltaics: Res. Appl.* 7 (1999) 393.
- [5] F. Kessler, K. Herz, E. Groß, M. Powalla, K.-M. Baumgärtner, A. Schulz, J. Herrero, *Proceedings of the 16th European Photovoltaic Solar Energy Conference, Glasgow, 2000*, p. 317.
- [6] M.A. Martinez, C. Guillen, A. Morales, J. Herrero, *Proceedings of the 16th European Photovoltaic Solar Energy Conference, Glasgow, 2000*, p. 879.
- [7] W. Petasch, E. Räuchle, H. Muegge, K. Muegge, *Surf. Coat. Technol.* 93 (1997) 112.
- [8] M. Hartmann, M. Schmidt, A. Jasenek, H.-W. Schock, F. Kessler, K. Herz, M. Powalla. In: *Proceedings of the 28th IEEE Photovoltaic Specialists Conference, 2000* p. 638.
- [9] R. Wächter, F. Kessler, K. Herz, M. Powalla, *Proceedings 10 Bundesdeutsche Fachtagung Plasmatechnologie, 2001*, p. 39.