고려대학교
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COSE321 Computer Systems Design

Lecture 6. Timers

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Timers

http://a-towntales.blogspot.kr/2011/09/dreaded-alarm-clock.html
http://www.ikea.com/us/en/catalog/products/50187566/

Timers in Zynq-7000

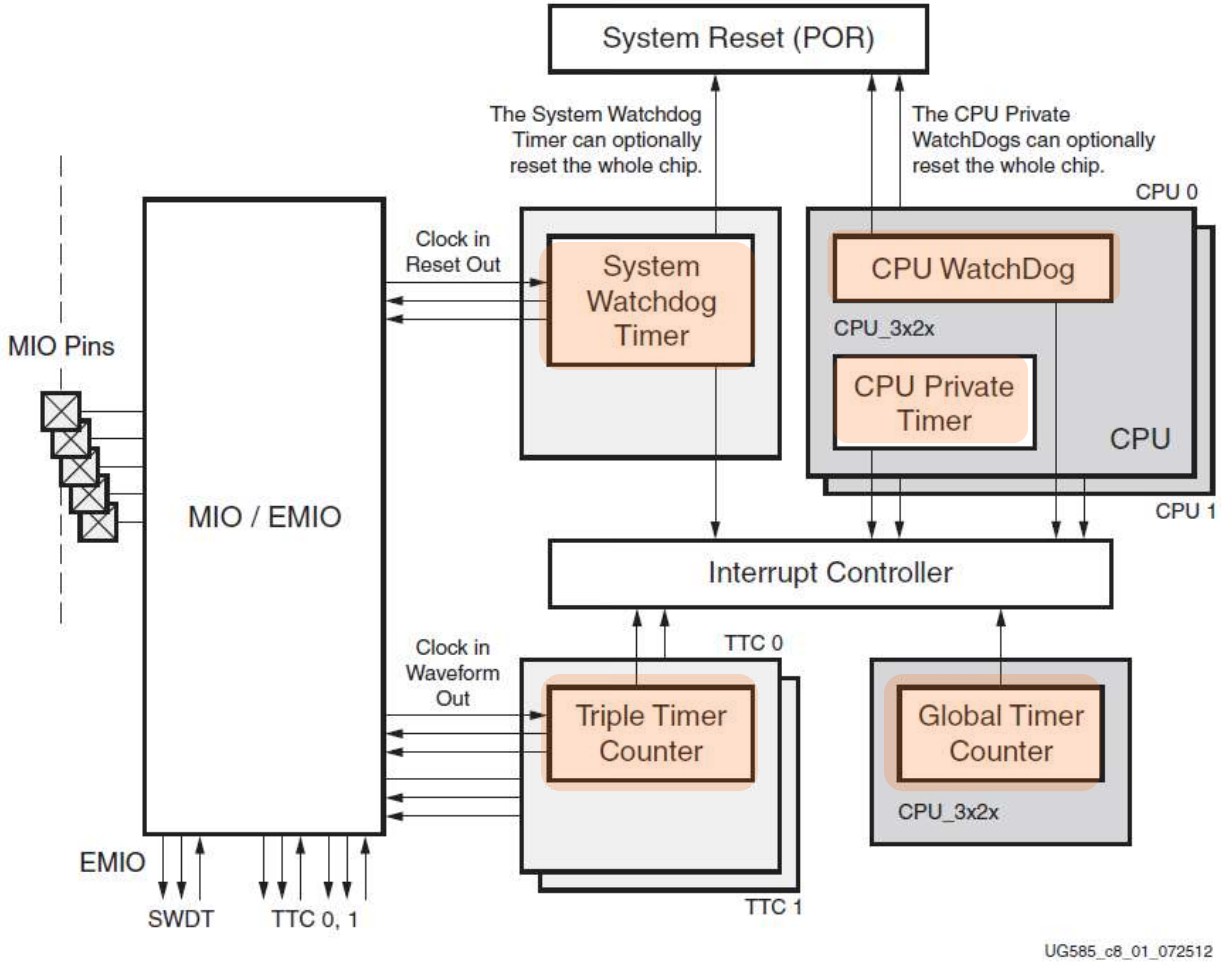


Figure 8-1: **System View**

Private Timer

- 32-bit decrementing counter
- Generate an interrupt when the counter reaches 0
- Single-shot or auto-reload configurable
- Configurable initial value
- Use PERIPHCLK

Base: 0xF8F0_0600 in Zynq

Table 4-1 Timer and watchdog registers

Offset	Type	Reset Value	Function
0x00	RW	0x00000000	*Private Timer Load Register*
0x04	RW	0x00000000	*Private Timer Counter Register*
0x08	RW	0x00000000	*Private Timer Control Register* on page 4-4
0x0C	RW	0x00000000	*Private Timer Interrupt Status Register* on page 4-4

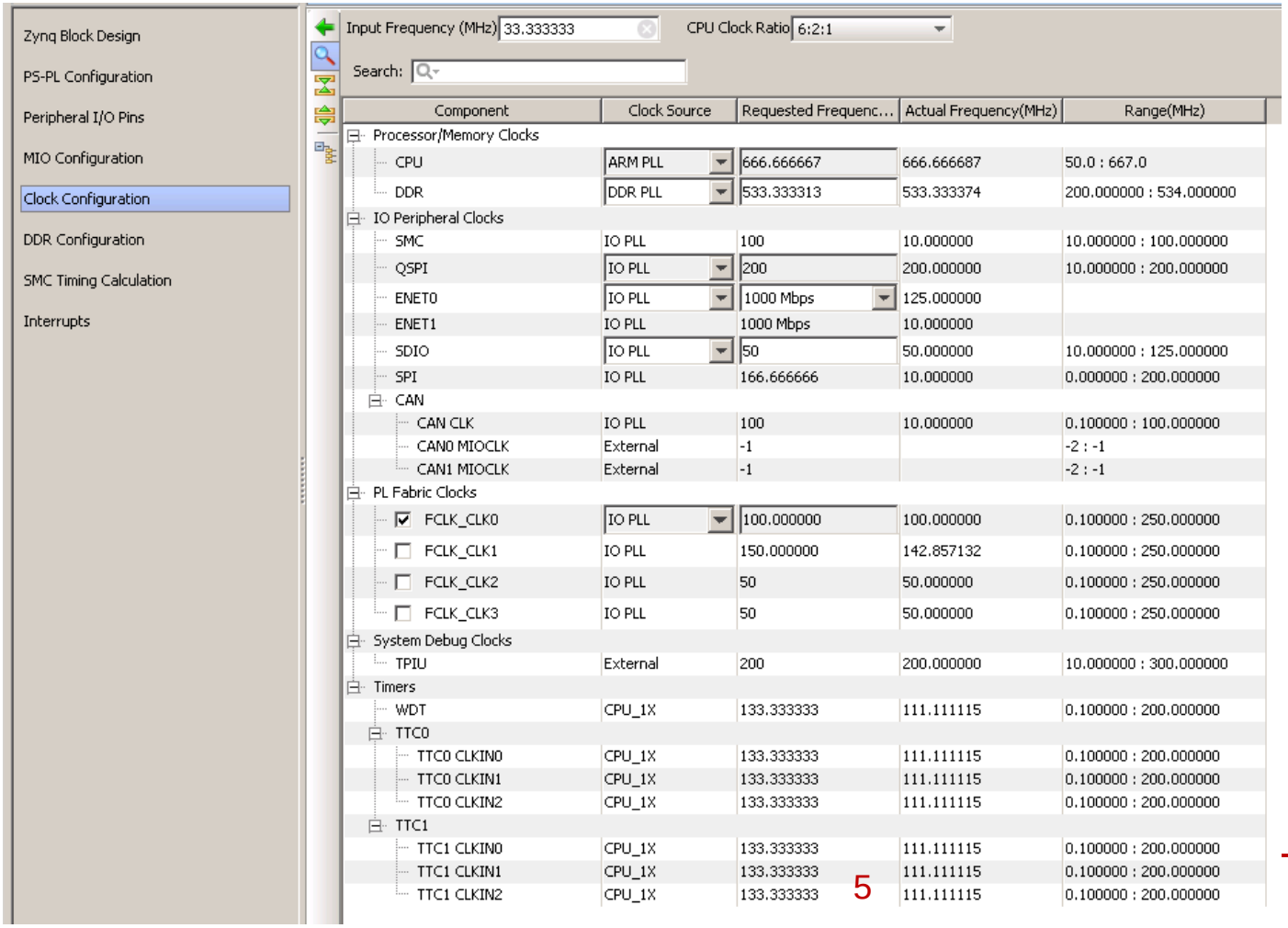
Source: Cortex A9 MPCore Technical Reference Manual

Clocks

8.2.1 Clocking

Source: Zynq-7000 AP SoC Technical Reference Manual

All private timers and watchdog timers are always clocked at 1/2 of the CPU frequency (CPU_3x2x).



Component	Clock Source	Requested Frequenc...	Actual Frequency(MHz)	Range(MHz)
Processor/Memory Clocks				
CPU	ARM PLL	666.666667	666.666687	50.0 : 667.0
DDR	DDR PLL	533.333313	533.333374	200.000000 : 534.000000
IO Peripheral Clocks				
SMC	IO PLL	100	10.000000	10.000000 : 100.000000
QSPI	IO PLL	200	200.000000	10.000000 : 200.000000
ENET0	IO PLL	1000 Mbps	125.000000	
ENET1	IO PLL	1000 Mbps	10.000000	
SDIO	IO PLL	50	50.000000	10.000000 : 125.000000
SPI	IO PLL	166.666666	10.000000	0.000000 : 200.000000
CAN				
CAN CLK	IO PLL	100	10.000000	0.100000 : 100.000000
CAN0 MIOCLK	External	-1		-2 : -1
CAN1 MIOCLK	External	-1		-2 : -1
PL Fabric Clocks				
FCLK_CLK0	IO PLL	100.000000	100.000000	0.100000 : 250.000000
FCLK_CLK1	IO PLL	150.000000	142.857132	0.100000 : 250.000000
FCLK_CLK2	IO PLL	50	50.000000	0.100000 : 250.000000
FCLK_CLK3	IO PLL	50	50.000000	0.100000 : 250.000000
System Debug Clocks				
TPIU	External	200	200.000000	10.000000 : 300.000000
Timers				
WDT	CPU_1X	133.333333	111.111115	0.100000 : 200.000000
TTC0				
TTC0 CLKIN0	CPU_1X	133.333333	111.111115	0.100000 : 200.000000
TTC0 CLKIN1	CPU_1X	133.333333	111.111115	0.100000 : 200.000000
TTC0 CLKIN2	CPU_1X	133.333333	111.111115	0.100000 : 200.000000
TTC1				
TTC1 CLKIN0	CPU_1X	133.333333	111.111115	0.100000 : 200.000000
TTC1 CLKIN1	CPU_1X	133.333333	111.111115	0.100000 : 200.000000
TTC1 CLKIN2	CPU_1X	133.333333	111.111115	0.100000 : 200.000000

So, private timer clock is 333MHz

Load Register & Counter Register

4.2.1 Private Timer Load Register

The Timer Load Register contains the value copied to the Timer Counter Register when it decrements down to zero with auto reload mode enabled. Writing to the Timer Load Register means that you also write to the Timer Counter Register.

4.2.2 Private Timer Counter Register

The Timer Counter Register is a decrementing counter.

The Timer Counter Register decrements if the timer is enabled using the timer enable bit in the Timer Control Register. If a Cortex-A9 processor timer is in debug state, the counter only decrements when the Cortex-A9 processor returns to non debug state.

When the Timer Counter Register reaches zero and auto reload mode is enabled, it reloads the value in the Timer Load Register and then decrements from that value. If auto reload mode is not enabled, the Timer Counter Register decrements down to zero and stops.

Control Register

Figure 4-1 shows the Private Timer Control Register bit assignments.

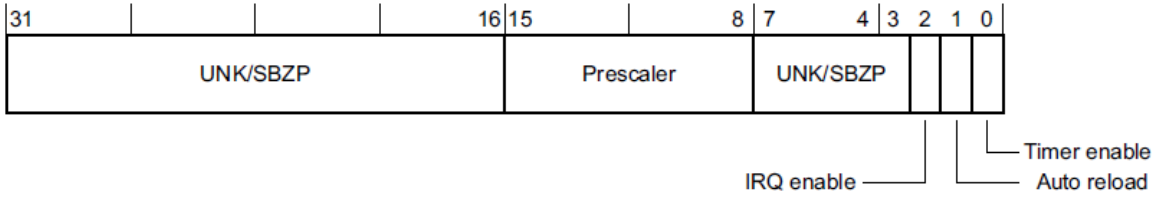


Figure 4-1 Private Timer Control Register bit assignments

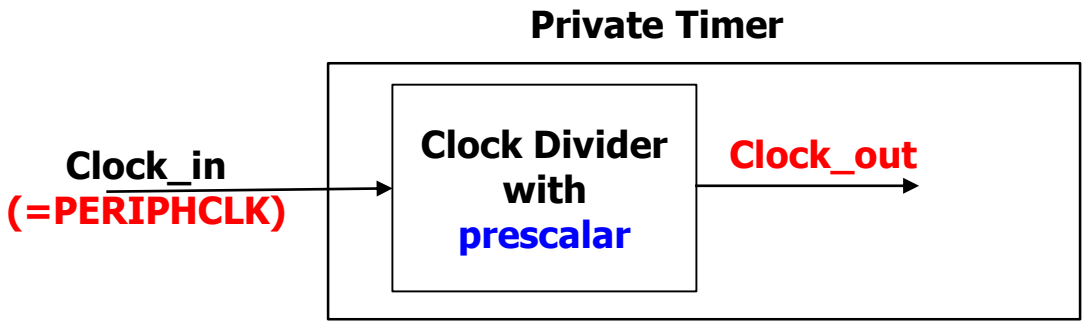
Table 4-2 shows the Private Timer Control Register bit assignments.

Table 4-2 Private Timer Control Register bit assignments

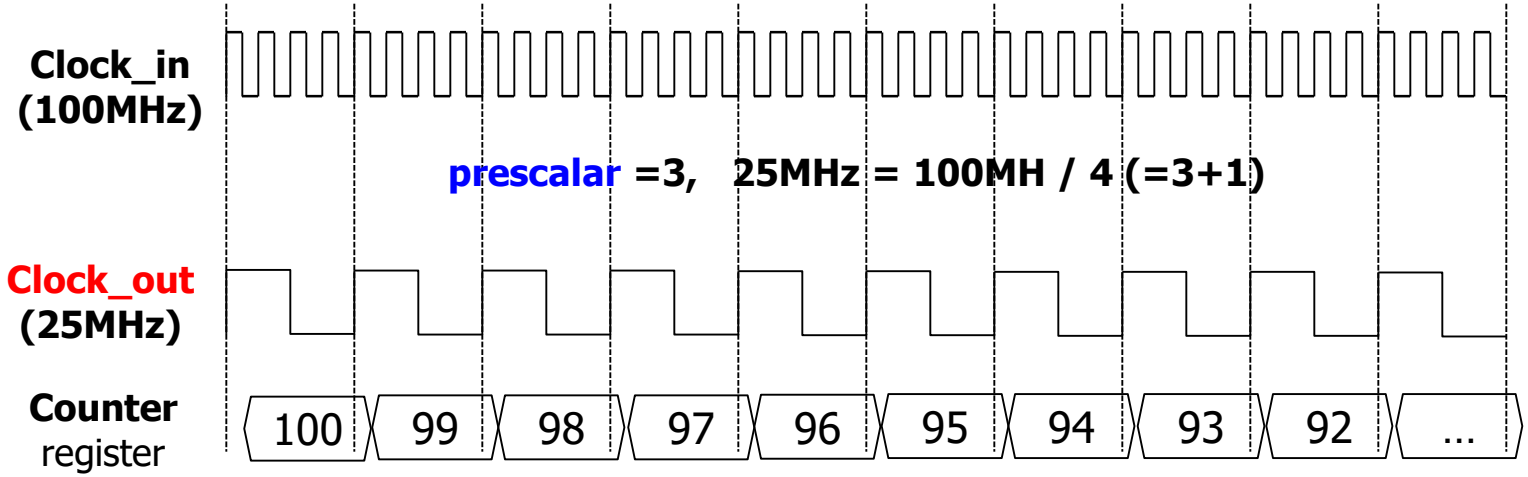
Bits	Name	Function	
[31:16]	-	UNK/SBZP.	
[15:8]	Prescaler	The prescaler modifies the clock period for the decrementing event for the Counter Register. See *Calculating timer intervals* on page 4-2 for the equation.	
[7:3]	-	UNK/SBZP.	
[2]	IRQ Enable	If set, the interrupt ID 29 is set as pending in the Interrupt Distributor when the event flag is set in the Timer Status Register.	
[1]	Auto reload	**0**	Single shot mode.Counter decrements down to zero, sets the event flag and stops.
		1	Auto-reload mode.Each time the Counter Register reaches zero, it is reloaded with the value contained in the Timer Load Register.
[0]	Timer Enable	Timer enable:	
		0	Timer is disabled and the counter does not decrement. All registers can still be read and written
		1	Timer is enabled and the counter decrements normally.

The timer is incremented every prescaler value+1. For example, if the prescaler has a value of five then the global timer is incremented every six clock cycles. **PERIPHCLK** is the reference clock for this.

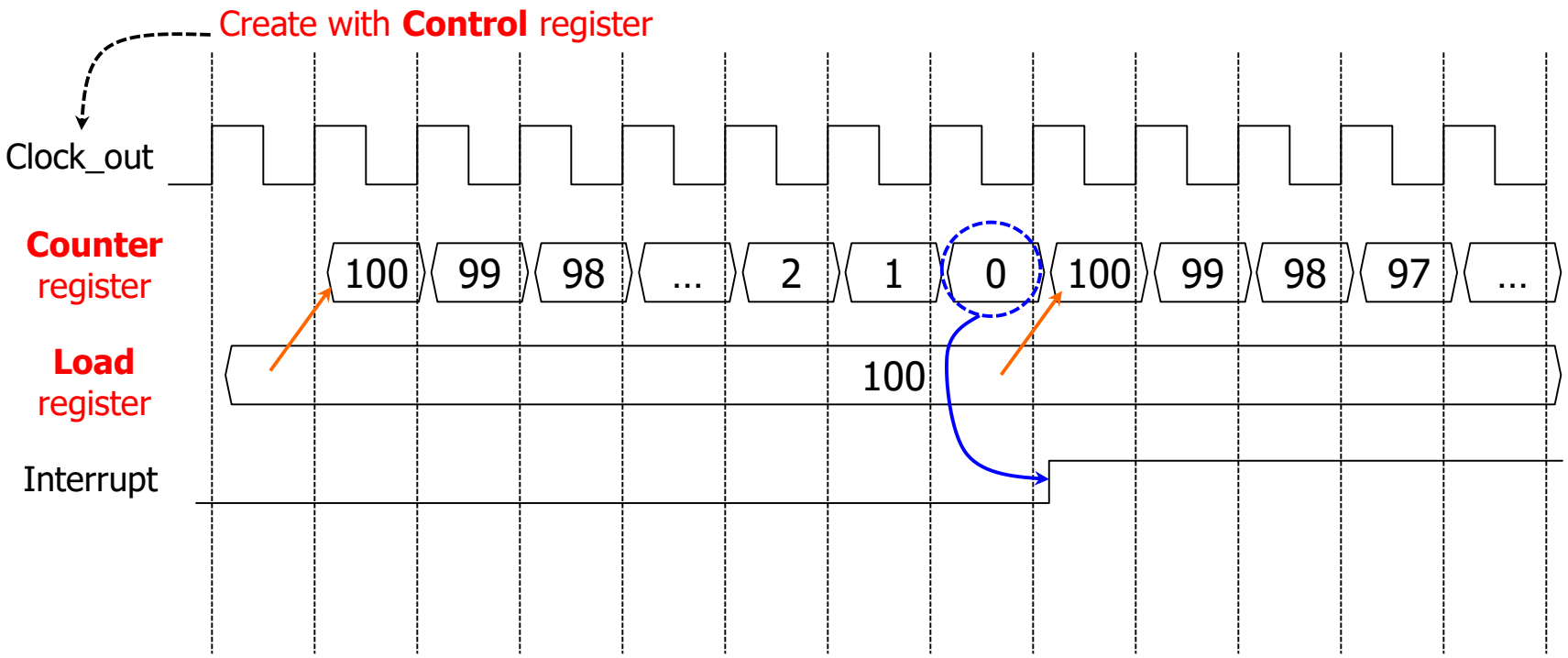
Timer Clock



$$\text{Clock\_out} = \frac{\text{Clock\_in}}{\text{prescalar} + 1}$$



Hardware Operation Example



Timer Interval

4.1.1 Calculating timer intervals

The timer interval is calculated using the following equation:

$$\left(\frac{(\text{PRESCALER\_value}+1) \times (\text{Load\_value}+1)}{\text{PERIPHCLK}}\right)$$

This equation can be used to calculate the period between two events generated by a timer or watchdog.

Interrupt Status Register

4.2.4 Private Timer Interrupt Status Register

Figure 4-2 on page 4-5 shows the Private Timer Interrupt Status Register bit assignment.

This is a banked register for all Cortex-A9 processors present.

The event flag is a sticky bit that is automatically set when the Counter Register reaches zero. If the timer interrupt is enabled, Interrupt ID 29 is set as pending in the Interrupt Distributor after the event flag is set. The event flag is cleared when written to 1.

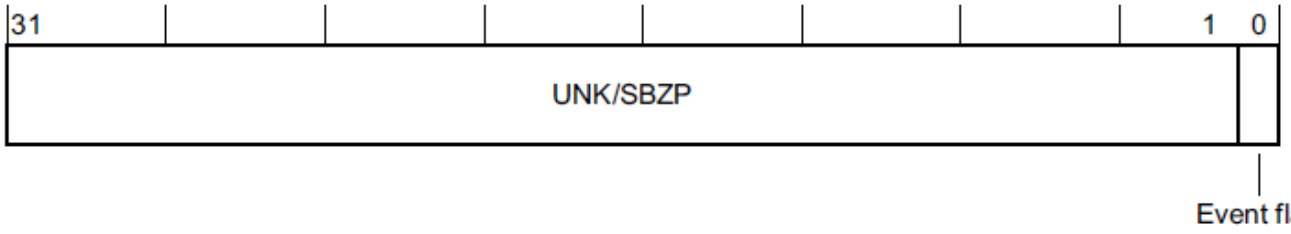


Figure 4-2 Private Timer Interrupt Status Register bit assignment

Base Addresses

4.4 CPU Private Bus Registers

The registers shown in Table 4-4 are only accessible by the CPU on the CPU private bus. The accelerator coherency port (ACP) cannot access any of the private CPU registers. The private CPU registers are used to control subsystems in the APU.

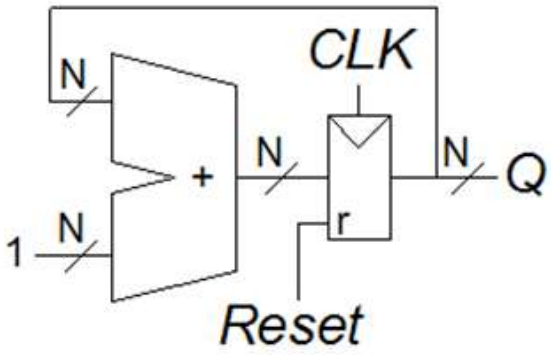
Table 4-4: **CPU Private Register Map**

Register Base Address	Description
F890_0000 to F89F_FFFF	Top-level interconnect configuration and Global Programmers View (GPV)
F8F0_0000 to F8F0_00FC	SCU control and status
F8F0_0100 to F8F0_01FF	Interrupt controller CPU
F8F0_0200 to F8F0_02FF	Global timer
F8F0_0600 to F8F0_06FF	Private timers and private watchdog timers
F8F0_1000 to F8F0_1FFF	Interrupt controller distributor
F8F0_2000 to F8F0_2FFF	L2-cache controller

Backup Slides

Counters

- An N-bit binary counter is a sequential arithmetic circuit with clock, reset, and an N-bit output
  - Increment output on each clock edge
  - Used to count cycles via numbers
    - For example: 000, 001, 010, 011, 100, 101, 110, 111, 000, 001…
  - Counters are used in many digital systems
    - Digital clock displays
    - Program counter (PC) register is used in computers to keep track of the current instruction CPU is executing



Private Timer & WDT

- 32-bit decrementing counter
- Generate an interrupt when the counter reaches 0
- Single-shot or auto-reload configurable
- Configurable initial value
- Use PERIPHCLK

Table 4-1 Timer and watchdog registers

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0x04	RW	0x00000000	*Private Timer Counter Register*
0x08	RW	0x00000000	*Private Timer Control Register* on page 4-4
0x0C	RW	0x00000000	*Private Timer Interrupt Status Register* on page 4-4
0x20	RW	0x00000000	*Watchdog Load Register* on page 4-5
0x24	RW	0x00000000	*Watchdog Counter Register* on page 4-5
0x28	RW	0x00000000	*Watchdog Control Register* on page 4-5
0x2C	RW	0x00000000	*Watchdog Interrupt Status Register* on page 4-6
0x30	RW	0x00000000	*Watchdog Reset Status Register* on page 4-7
0x34	WO	-	*Watchdog Disable Register* on page 4-7

Source: Cortex A9 MPCore Technical Reference Manual

PS Clock System Block Diagram

The major components of the clock subsystem are shown in Figure 25-1.

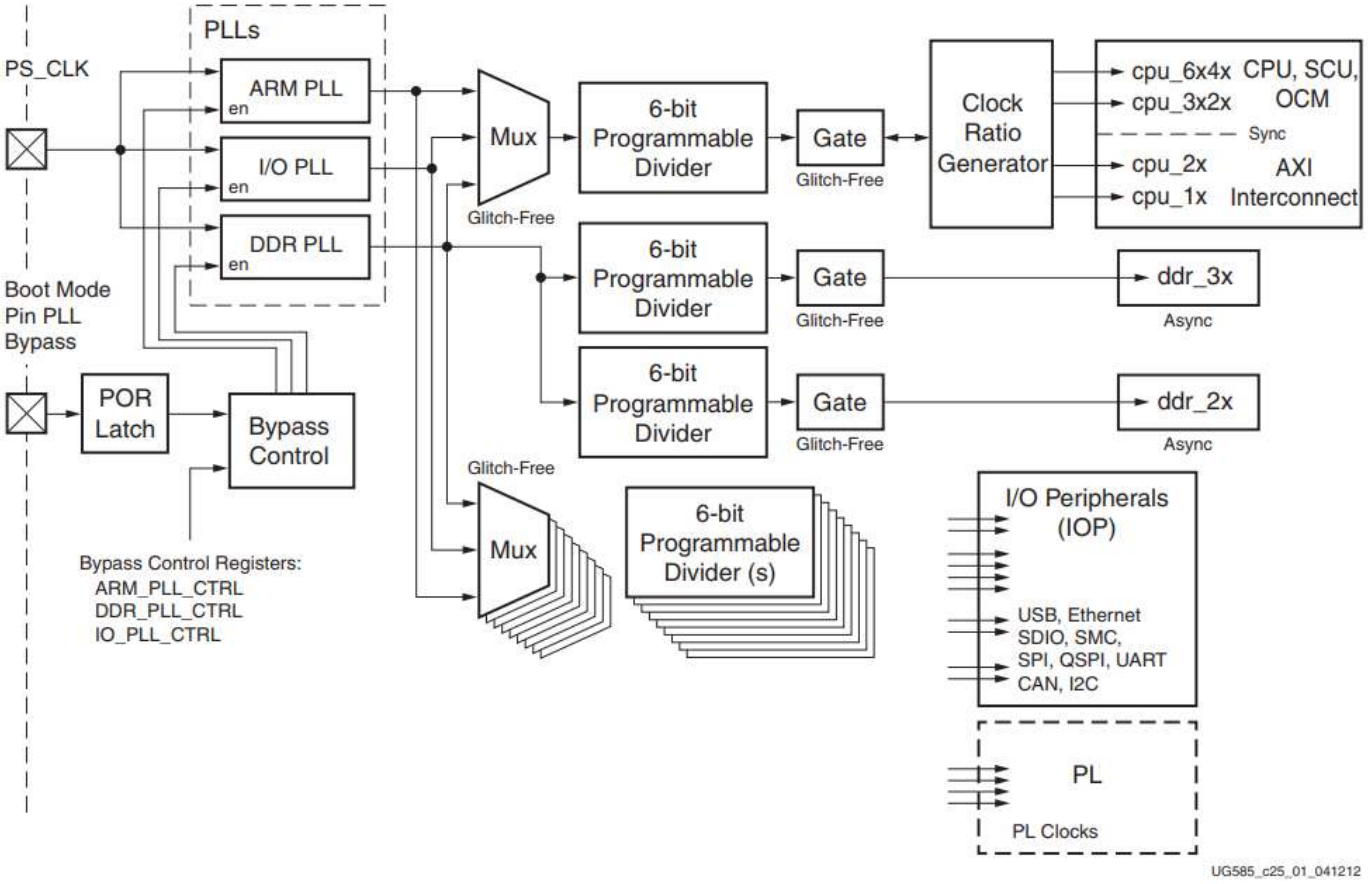

Figure 25-1: **PS Clock System Block Diagram**

Ratio Examples

Figure 25-3 shows the clock generation network in the CPU clock domains.

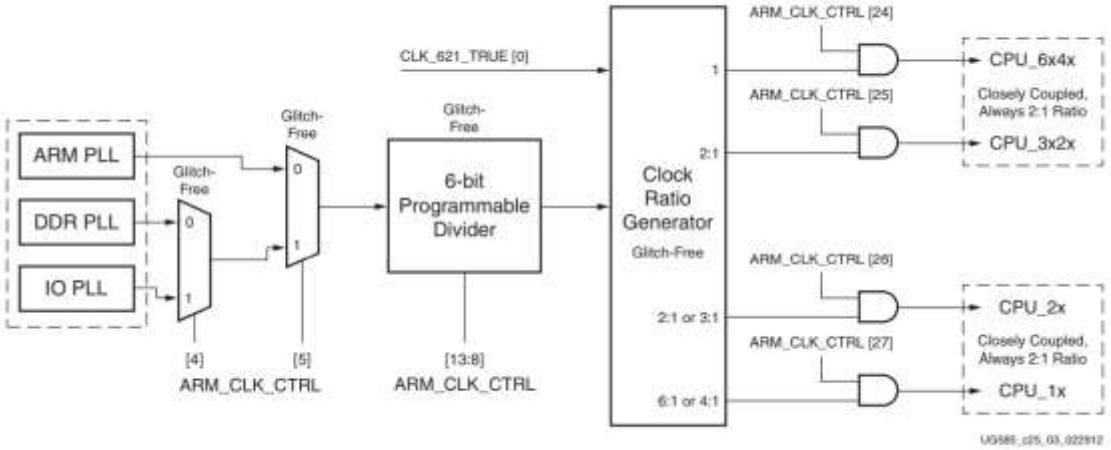

Figure 25-3: **CPU Clock Generation and Domains**

Ratio Examples

The CPU clock domain operates in two modes 6:2:1 and 4:2:1. Table 25-1 shows example frequencies for these modes and modules operating in each clock domain. (See the applicable Zynq-7000 AP SoC data sheet for the specific allowed frequencies for each clock.)

Table 25-1: **CPU Clock Frequency Ratio Examples**

CPU Clock	6:2:1	4:2:1	Clock Domain Modules
CPU_6x4x	800 MHz (6 times faster than CPU_1x)	600 MHz (4 times faster than CPU_1x)	CPU clock frequency, SCU, and OCM arbitration
CPU_3x2x	400 MHz (3 times faster than CPU_1x)	300 MHz (2 times faster than CPU_1x)	L2 cache memory, APU timers
CPU_2x	266 MHz (2 times faster than CPU_1x)	300 MHz (2 times faster than CPU_1x)	I/O peripherals, central interconnect, master interconnect, slave interconnect, and OCM RAM
CPU_1x	133 MHz	150 MHz	I/O peripherals AHB and APB interface busses

PERPHICLK

5.1 Clocks

The Cortex-A9 MPCore processor does not have any asynchronous interfaces. So, all the bus interfaces and the interrupt signals must be synchronous with reference to **CLK**.The Cortex-A9 MPCore processor has these functional clock inputs:

CLK

This is the main clock of the Cortex-A9 processor.

All Cortex-A9 processors in the Cortex-A9 MPCore processor and the SCU are clocked with a distributed version of CLK.

PERIPHCLK

The Interrupt Controller, global timer, private timers, and watchdogs are clocked with **PERIPHCLK**.

PERIPHCLK must be synchronous with **CLK**, and the **PERIPHCLK** clock period, N, must be configured as a multiple of the **CLK** clock period. This multiple N must be equal to, or greater than two.

PERIPHCLKEN

This is the clock enable signal for the Interrupt Controller and timers. The **PERIPHCLKEN** signal is generated at **CLK** clock speed. **PERIPHCLKEN** HIGH on a CLK rising edge indicates that there is a corresponding **PERIPHCLK** rising edge.

Figure 5-1 shows an example with the **PERIPHCLK** clock period N as three.

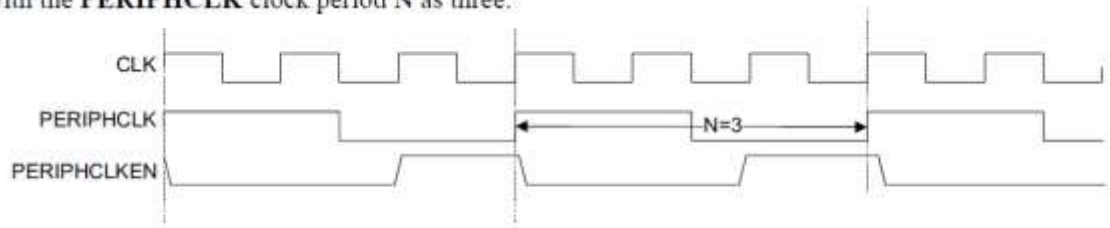

Figure 5-1 Three-to-one timing ratio

Timers in Cortex-A9 MPCore

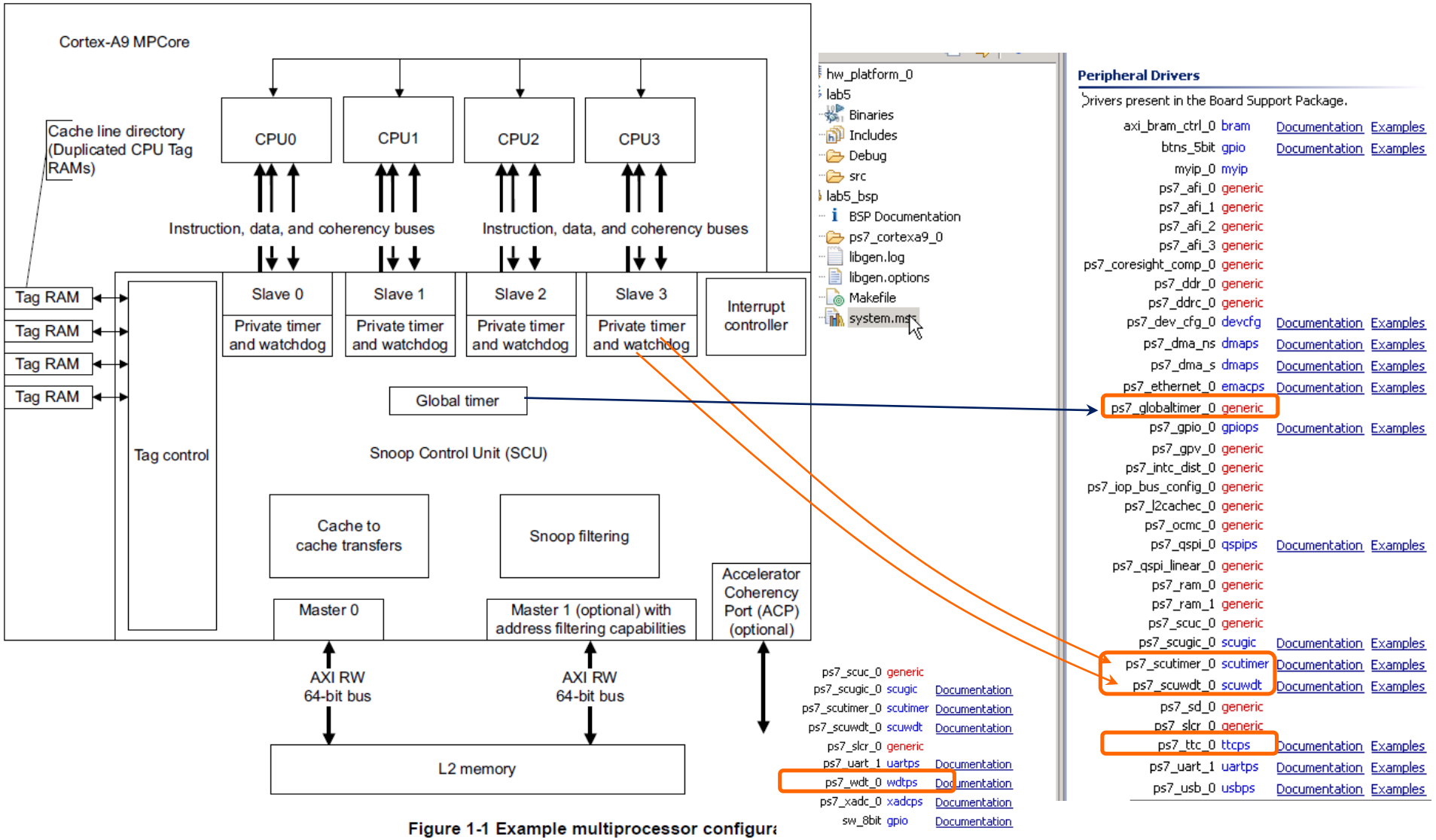

Figure 1-1 Example multiprocessor configura