Micro-M

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18-39263-3

Ques-1: Design of ALU

S_2	S_1	S_0	F with $C_{in}=0$	F with $C_{in}=1$	X_i (A_i)	Y_i (B_i)	Z_i (C_{in})
0	0	0	A − 1	0	A	1	0
0	0	0	Trans, A	1	A	1	1
0	0	1	A + B	0	A	B	0
0	0	1	A + B + 1	1	A	B	1
0	1	0	A − B − 1	0	A	$\bar{B}$	0
0	1	0	Trans, A − B	1	A	$\bar{B}$	1
0	1	1	Trans, A	0	A	0	0
0	1	1	A + 1	1	A	0	1
1	0	0	$\bar{A}$	X	A	1	0
1	0	1	A XOR B	X	A	B	0
1	1	0	A AND B	X	A + $\bar{B}$	$\bar{B}$	0
1	1	1	A OR B	X	A + B	0	0

K-map for X_i:

S_2S_1 \ S_0	0	1
00	A	A
01	A	A
11	A + $\bar{B}$	A + B
10	A	A

$X_i = A + S_2S_1\bar{S}_0\bar{B} + S_2S_1S_0B$

K-map for Y_i:

S_2S_1 \ S_0	0	1
00	1	B
01	$\bar{B}$	0
11	$\bar{B}$	0
10	1	B

$Y_i = \bar{S}_0\bar{B} + \bar{S}_1B$

K-map for Z_i:

S_2S_1 \ S_0C_{in}	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	0	0	0
10	0	0	0	0

$Z_i = \bar{S}_2C_{in}$

P.t.o

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ALU Design

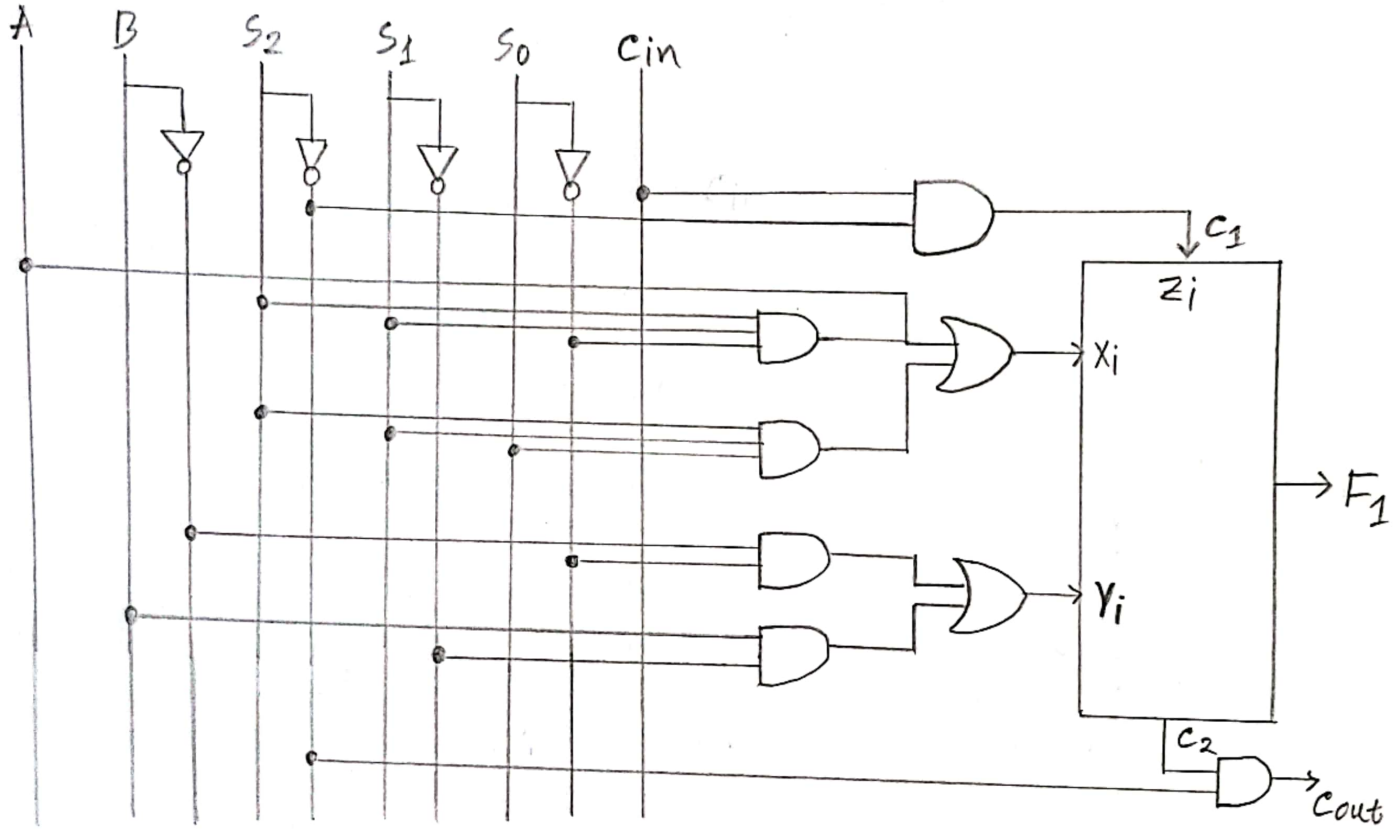

Figure: 1-bit ALU

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Ques:-2, Design of shifter:

H_2	H_1	H_0	Operations
0	0	0	1's to the output bus
0	0	1	Shift Left with $I_L = 0$
0	1	0	No shift
0	1	1	circulate Left with carry
1	0	0	0's to the output bus
1	0	1	——
1	1	0	circulate Right with carry
1	1	1	shift Right with $I_R = 0$

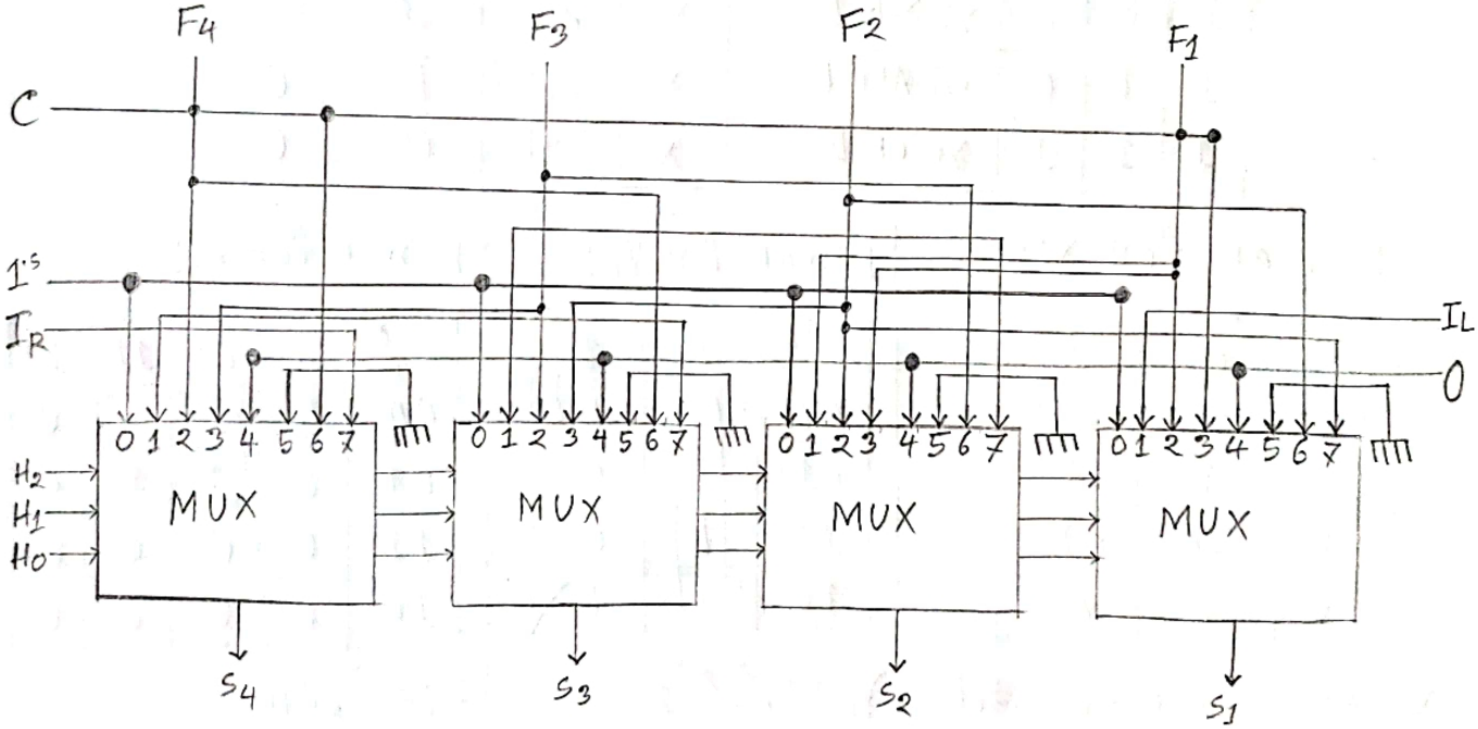

Figure: 4-bit shifter

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Ques:-3

ROM Address			X	S_2	S_1	S_0	Cin	L	y	z	w	Address			Select	
			1	2	3	4	5	6	7	8	9	10	11	12	13	14
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	1	1	0	0	0	1	0	1	0	0
1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0
1	1	0	0	1	0	0	0	1	0	0	0	1	1	1	0	0
1	1	1	0	0	1	1	1	1	0	1	0	0	0	0	0	0