Juechu (Joy) Dong

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EDUCATION

University of Michigan – Ann Arbor **Expected - May 2022**

Ann Arbor, MI

Computer Engineering, Bachelor of Science

GPA: 4.00/4.00

Coursework: Data Structures and Algorithm (A) Digital Integrated Circuits EECS312 (A) Computer Architecture EECS470 (A) Compilers (A+) Operation System (in progress) cuda Programming (in progress)

University of Michigan-Shanghai Jiao Tong University Joint Institute (UM-SJTU JI) **Expected - Aug. 2022**

Shanghai, China

Electrical and Computer Engineering (**ECE**), Bachelor of Science

GPA: 3.82/4.00

RESEARCH EXPERIENCE

Crossbar For Programmable Fully Homomorphic Encryption Accelerator @UMich **Sept. 2021-Present**

Monitored by: Dr. Ronald Dreslinski

- Design extremely high bandwidth, statically scheduled crossbar for FHE accelerator F1 (MICRO 2021) with strict power and area restrictions

A Federated Genomic Analysis System Based on Open-enclave & SGX @UMich **May 2021-Present**

Monitored by: Dr. Satish Narayanasamy

- Solve privacy concerns in genomic data sharing without accuracy penalty from metadata studies or performance penalty from homomorphic encryption
- Build a centralized system that collects genomic data from host institutions and analyze them on central server enclave without leaking raw or intermediate data

Fully-Autonomous SoC Synthesis, Explore CS Research Program @UMich **Jan. 2021-May 2021**

Monitored by: Dr. Ronald Dreslinski

- Build an intent solver that translates high-level user intent into hardware specifications and to satisfy user constraints, in particular, determines appropriate acceleration blocks for user python code
- Attend weekly meetings with Dr. Dreslinski to develop basic research skills in experiment setup and to learn how to narrow down research interests and identify a new research topic

TEACHING EXPERIENCE

Instructional Aid for Computer Architecture Course (EECS470)

University of Michigan, Ann Arbor MI **Sept. 2021-Present**

- Hold lab sessions regarding out of order processor design topics including branch prediction, scheduling, cache, pipeline etc. and Verilog
- Develop exam questions and answer questions regarding OoO processor topics

SELECTED HONORS

Dean's List University of Michigan Apr. 2020

SKILLS

Language

- **Chinese** (Native, Mandarin) **English** (Fluent)
- **Proficient in**: C/C++ (System)Verilog