A Selectorless RRAM with Record Memory Window and Nonlinearity Based on Trap Filled Limit Mechanism

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***Abstract*— Implementation of a crossbar array of selectorless resistive random access memory (RRAM) devices requires a high nonlinearity (NL) in low resistance state (LRS) currents to avoid the sneak path leakages. In this work, a process dependent nonlinearity in the low resistance state of $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) based RRAM devices is studied. We present a device with a record high NL of ~95.5 in LRS currents (I_{LRS}) along with a memory window (MW) of ~164. We report a very high slope of ~16 mV/dec in the nonlinear region of I_{LRS}. Further, we extract the material parameter like trap level, trap density etc. using previously developed space charge limited current (SCLC) based analytical model.**

Keywords-; selectorless RRAM, nonlinearity, space charge limited current, resistive switching, PCMO

I. INTRODUCTION

Resistive random access memories (RRAM) are promising due to its fast switching, endurance, retention, $4F^2$ cell size [1-2]. However, the sneak path current issue in memory crossbar array results into reduced readout margin, and increased power consumptions which limits the maximum crossbar array size. Several selector devices are being proposed to address these problems [3-4]. However, adding selector in series with RRAM increases the operating voltages [5] and structure complexities. Hence, selectorless RRAM with nonlinearity in LRS currents (I_{LRS}) are being proposed [1-2, 6-8]. However, the nonlinearity (NL) and memory window (MW) values of these devices are insufficient to realize a selectorless crossbar array.

In this paper, we propose a PCMO based selectorless RRAM device with a record NL of >95, MW of >160 along with a slope of ~16 mV/dec in I_{LRS}.

II. EXPERIMENT

A. Device Fabrication

The process flow for fabrication of devices in shown in Fig. 1 (a). First, Si <100> substrate was thermally oxidized to grow ~40 nm of SiO_2. The Pt bottom electrode of ~100 nm was then deposited on Si/SiO_2 substrate by using a 25 nm thick Ti layer as adhesion layer for Pt on SiO_2. $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) layer of ~65 nm is then deposited on $Si/SiO_2/Ti/Pt$ substrate by (a) pulsed laser deposition (PLD) & (b) sputtering at room temperature. The stacks were, thereafter, annealed in N_2 ambient for 30s. The schematic of the device is shown in Fig. 1 (b). The sample details are given in Table I.

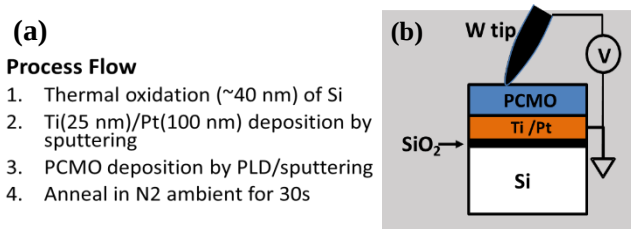

Figure 1. shows (a) the fabrication process flow & (b) the device schematic

TABLE I. SAMPLE DETAILS

Tool	Deposition Temperature	N2 Anneal Temperature	Sample ID
PLD	RT	650 °C	P650C
Sputter	RT	650 °C	S650C
Sputter	RT	750 °C	S750C

B. Electrical Characterization

Tungsten probe-tip of 3.5 µm was used as top electrode for electrical characterization [9]. The DC IV measurements were carried out using Agilent B1500a semiconductor device parameter analyzer.

III. RESULTS & DISCUSSION

The IV characteristics for three samples fabricated with different process and anneal conditions are shown in Fig. 2. Bipolar resistive switching was observed in all the three

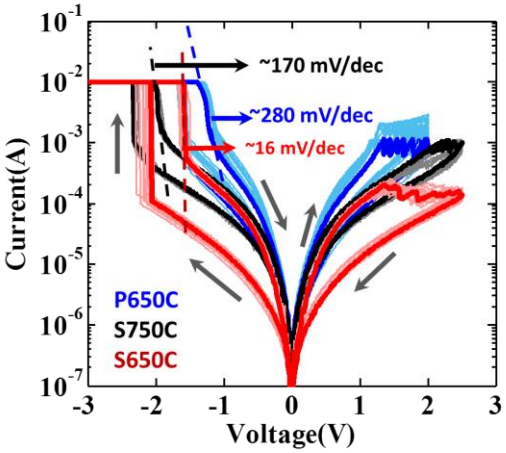

Figure 2. shows IV characteristics for P650C (blue), S750C (black) & S650C (red) for 20 cycles. Different nonlinearities (NL) and memory windows (MW) can be observed for 3 samples. A sharp nonlinearity (NL) with slope ~16 mV/dec is seen for sample S650C versus 170 mV/dec & 280 mV/dec for S750C & P650C, respectively.

samples. The set process i.e. switching from high resistance state (HRS) to low resistance state (LRS) takes place in negative polarity, whereas, switching from LRS to HRS takes place in positive polarity of voltage. We observe that the DC switching characteristics of three samples are different for similar bias voltages and current compliance. The differences in IV characteristics of three samples are compared in terms of nonlinearity and memory window in the following section.

A. *Nonlinearity (NL) in I_{LRS}*

We determine the NL in I_{LRS} as $\frac{I_{LRS(V_{read})}}{I_{LRS(V_{read})/2}}$, assuming V/2 biasing scheme. The read voltages (V_{read}) of -1.4 V, -2.1 V & -1.75 V were chosen for P650C, S750C & S650C samples, respectively, for determining the maximum NL in that particular sample. The S650C sample was found to show the highest NL of ~95.5 amongst the three samples. This NL is

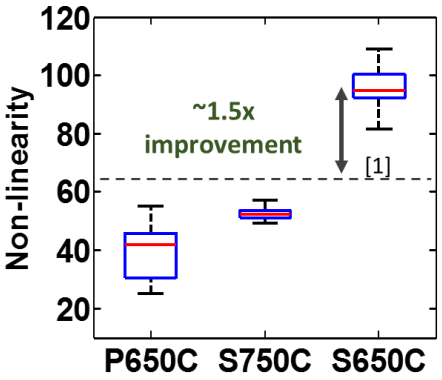

Figure 3. Shows the NL determined at V_{read} =-1.4 V, -2.1 V & -1.75 V for P650C, S750C & S650C, respectively, by V/2 read scheme. Sample S650C shows the highest NL of ~95.5 (median) followed by S750C & P650C with NLs of ~50 (median) & ~42 (median)

~1.5× better that the highest reported in [1], which makes the sample S650C a promising candidate for selectorless RRAM. The NL values for all the three samples are shown in Fig. 3.

Also, a record slope of ~ 16 mV/dec in I_{LRS} was obtained for S650C sample compared to slopes of 170 mV/dec & 280 mV/dec for S750C & P650C respectively.

B. *Memory Window (MW)*

The MW is determined as $\frac{I_{LRS(V_{read})}}{I_{HRS(V_{read})}}$. Again, the read voltages (V_{read}) of -1.4 V, -2.1 V & -1.75 V were chosen for P650C, S750C & S650C samples, respectively, for determining the maximum MW in that particular sample. A maximum MW of ~164 was found for S650C sample, which is ~4.5× higher than the MW window obtained for highest NL in [1]. The MW values for all the three samples are shown in Fig. 4.

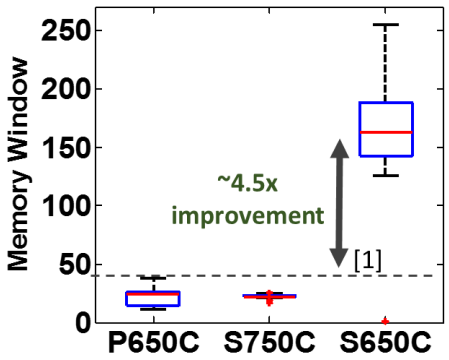

Figure 4. shows MWs for P650C, S750C & S650C determined at V_{read} =-1.4 V, -2.1 V & -1.75 V for P650C, S750C & S650C, respectively. Sample S650C shows the highest MW of ~164 (median).

IV. BENCHMARKING

To enable selectorless RRAM technology, an intrinsic NL in the IV characteristics of RRAM device is desired along with good MW. This would avoid sneak path leakages without the need of a selector device in series. Here, we compare the NL and MW for the various proposed selectorless RRAM technologies. It is found that the NL of ~95.5 and MW of ~164 for S650C sample is the best amongst the existing selectorless technologies. The comparison is shown in Fig. 5.

V. SPACE CHARGE LIMITED CURRENT (SCLC) BASED PARAMETER EXTRACTION

Fig. 6 shows the log-log plot of IV characteristic of S650C sample, showing space charge limited current (SCLC) signature. Four distinct regions, (i) Ohmic (α ~1) (ii) Trap SCLC, J_{trap} (α ~2) (iii) Trap-filled Limit (α >>2, V_{TFL}) (iv) Trap – free SCLC, $J_{trap\ free}$ (α ~2) were observed. This essentially indicates that the nonlinearity originates from the trap filled limit nonlinearity. For the first time, trap-filled limit phenomenon has been exploited to demonstrate a selectorless RRAM.

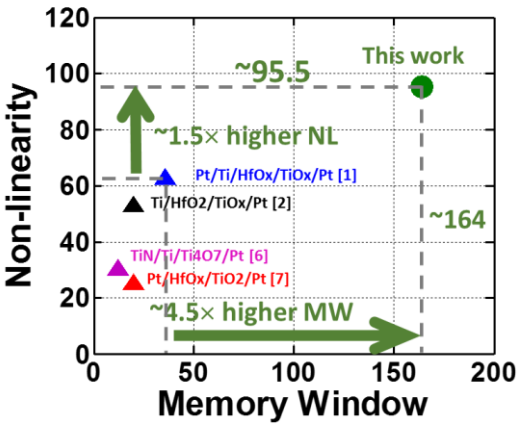

Figure 5. Comparison of NLs and MWs of various selectorless RRAMs demonstrated in literature with those obtained in S650C sample of this work. The NL obtained for S650C is ~1.5× higher than the highest reported NL, whereas the MW is ~4.5x higher than the highest reported MW for selectorless RRAM.

Recently, we have demonstrated a methodology to extract various materials parameters like trap concentration (N_T), trap energy level (E_T) compared to valence band energy (E_V), mobility (μ) etc. based on SCLC model for PCMO based RRAM [10]. Based on this, we obtained a trap energy level (E_T-E_V) of 0.183 eV using,

$$E_T - E_V = kTln\left(\frac{N_V}{\theta g N_{T-TFL}}\right), \text{where } \theta = \frac{J_{trap}}{J_{trap\ free}}$$

Also, a trap concentration of 9.35 x 10^{17}/cm^3 was calculated using,

$$V_{TFL} = \frac{qN_{T-TFL}L^2}{2\epsilon g}, \text{where } \varepsilon = 30 \text{ [10].}$$

The sharp NL in I_{LRS} is attributed to complete filling of traps known as trap filled limit (V_{TFL}) based on conventional Space Charge Limited Current model [11].

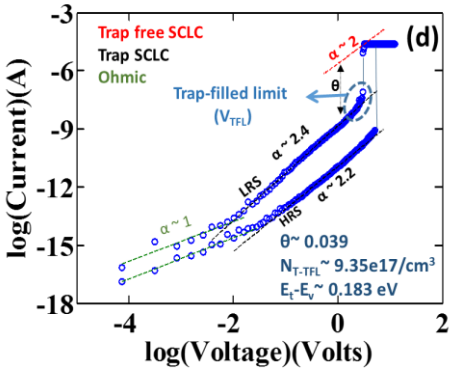

Figure 6. The loglog IV characteristic of S650C sample showing 4 distinct regimes based on exponent, α, of V i.e. I~$V^α$ (i) ohmic (α ~1) (ii) Trap SCLC (α ~2.4(LRS), α ~2.2(HRS)) (iii) Trap-filled Limit (α >>2) (iv) Trap – free SCLC (α ~2). These IV features are typical of SCLC mechanism. A trap density of 9.35 x 10^{17} /cm^3 and trap energy level of 0.183 eV was obtained for S650C sample.

VI. Conclusions

In this paper, we have studied the effect of deposition process (PLD & sputtering) & anneal temperature on NL & MW of IVs of PCMO based RRAM. We report a record high NL (~95) and MW (~164) for S650C sample. The NL & MW values obtained are the best till date. This makes the PCMO based RRAM devices a promising candidate for selectorless technology. We, further, report a sharp slope of ~16mV/dec in I_{LRS} of S650C sample. Also, the SCLC physics was used to obtain trap density and trap energy level in PCMO.

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