INDRANIL CHAKRABORTY
M.Tech Student, I.I.T Bombay Resume

Objective

Pursuing P.h.D

Personal Information

Permanent Address:	3, Meher Ali Mondal Street,Kolkata,West Bengal, India
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Research Interests

- **Transport Physics in Semiconductor devices:** Drift-Diffusion model, Space-Charge Limited Current transport model.
- **Physical Modelling of Semiconductor Devices:** Developing models to explain underlying physics in Semiconductor Devices.
- **Device Simulations:** Building novel device structures and characterizing it using TCAD simulations.
- **Memory Design:** Modeling of devices exhibiting resistive switching behavior in order to engineer materials to meet memory specification.

Academic Activities

Education

Master of Technology(M.Tech) 2014-present
Indian Institute of Technology, Bombay
Microelectronics & VLSI, Electrical Engineering Department

Cumulative GPA: **9.69 out of 10.0**
Class Position: **4th** out of 118 students in EE department(M.Tech)
M.Tech Thesis: Modelling of PCMO-based RRAM Devices
Thesis Advisor: Prof. Udayan Ganguly, IIT Bombay

Bachelor of Engineering(B.E) 2009-2013
Jadavpur University, Kolkata
Electronics & Telecommunications Engineering Department

Cumulative GPA: **9.21 out of 10.0**
Class Position: **12th** out of 60 students in ETCE department(B.E)
B.Tech Project: Tinyos 2.1x: A Beginner's Approach
Thesis Advisor: Prof. Mrinal Kanti Naskar, Jadavpur University

Qualifying Scores

- GRE: **331 (Quantitative-170, Verbal-161); AWA: 5.0/6.0**
- TOEFL:**113 (Reading-30, Listening-29, Speaking-26, Writing-28)**
- GATE: All India Rank **22** out of 2,16,237 students.
- WBJEE: Rank **98** out of 1,10,000 students

Teaching Experience

Microelectronics Simulations Laboratory(EE-735) Autumn'2015
Responsibilities: Prepared solutions to assignments, evaluated assignments and conducted viva-voce for students.

Digital Systems(EE-224) Spring'2014
Responsibilities: Hosted tutorial sessions for Undergraduate students, evaluated answer scripts and assignments.

Microprocessor Laboratory(EE-337) Autumn'2014
Responsibilities: Performed basic experiments using 8051 assembly language on Keil and Pt-51 Board, assisted Undergraduate students during lab sessions, developed documentation on lab experiments.

Major Research Projects

GRADUATE RESEARCH WORK

Topic: Physical Modelling of PCMO-based RRAM Devices
Advisor: Prof. Udayan Ganguly, IIT Bombay

Abstract: Resistance-RAM(RRAM) devices have been proposed as a new technology in the memory world. Many endeavors have been made to understand the current conduction mechanism and the underlying physics of such devices. In this work, we focus on analyzing experimental I-V characteristics of PCMO-based RRAM devices(Structure: W/PCMO/Pt on Si-SiO2 substrate) and developing a physical model to explain it based on Space-Charge-Limited-Current(SCLC) theory. We have developed methodology for extraction of different device parameters for both single and double trap levels and extracted trap parameters corresponding to experimental data, along with subsequent validation in Sentaurus TCAD. Our future goal is to engineer a material that can meet required memory specifications.

Publications:73rd Device Research Conference 2015[1]

Topic: Analysis of non-linearity in Selectorless RRAM devices
Advisor: Prof. Udayan Ganguly, IIT Bombay

Abstract: Resistive random access memories (RRAM) are promising due to its fast switching, endurance, retention, 4F2 cell size. However, the sneak path current issue in memory crossbar array results into reduced readout margin, and increased power consumptions which limits the maximum crossbar array size. Several selector devices are being proposed to address these problems. However, adding selector in series with RRAM increases the operating voltages and structure complexities. Hence, selector-less RRAM with non-linearity in LRS currents (ILRS) are being proposed. However, the non-linearity (NL) and memory window (MW) values of these devices are insufficient to realize a selector-less crossbar array. We have proposed a PCMO based RRAM device with a record NL of >160, MW of >160 along with a slope of 15 mV/dec in ILRS. The present challenge is to explain the physics causing such a sharp change in current.

Publications: Non-Volatile Memory Technology Symposium, 2015[2][4]

Topic: Analytical Solution of 1-D Poisson Equation for M-I-M Structures
Advisor: Prof. Udayan Ganguly, IIT Bombay

Abstract: M-I-M structures have widespread applications in RRAM technology due to its resistive switching behavior. In this work, I achieved derived a relationship between potential barrier and trap density, by solving the 1-D Poisson equation for M-I-M structure with a single,uniform trap distribution. The equation, thus derived, can be used to determine trap density from Current Density at low voltages.
Documentation: M.Tech Seminar Report, 2014

UNDERGRADUATE RESEARCH WORK

Topic: Cognitive Radio Networks
Advisor: Dr. Amitava Mukherjee, Senior Manager, IBM

Abstract:We propose a co-operative sensing framework, in conformation to the regulations stipulated by IEEE 802.22 WRAN standard. The objective of our work is to provide an efficient, yet, easily implementable spectrum discovery scheme following 802.22 standard. Through our work, we have shown that our proposed sensing framework achieves a lower probability of false detection and shows that the sensing procedure can be carried through less expensive receivers with lower sensitivity than those used in other traditional centralized sensing frameworks.

Publications: IEEE INDICON, 2014 [3]

List Of Publications

CONFERENCES:

[1] **I.Chakraborty**, A. K. Singh, P. Kumbhare, N. Panwar, and U. Ganguly. "Materials parameter extraction using analytical models in PCMO based RRAM." In *Device Research Conference (DRC), 2015 73rd Annual*, pp. 87-88. IEEE, 2015.

[2] P.Kumbhare,**I.Chakraborty**, A. K. Singh, N. Panwar, S. Chouhan, U. GangulyâĂIJA Selector-less RRAM with Record Memory Window and Non-linearity Based on Trap Filled Limit MechanismâĂİ,accepted in *Non-Volatile Memory Technology Symposium, 2015. NVMTS 2015.*,15th Annual.

[3] S.Biswas, and **I.Chakraborty**. "Cooperative sensing framework using IEEE 802.22-standard." In *India Conference (INDICON), 2014 Annual IEEE*, pp. 1-6. IEEE, 2014.

PATENT:

[4] P.Kumbhare, U. Ganguly,**I. Chakraborty**, A.K.Singh, “Selector-Less RRAM” (Patent Filed in Mumbai Patent Office, India)

Professional Experience

Internship May 2012- July 2012
Indian Statistical Institute, Kolkata
Bayesian and Interdisciplinary Research Unit

Title: **Resiliency of Wireless Sensor Networks**
Description: MATLAB analysis for Blom’s Scheme, a probabilistic key predistribution scheme for network size varying from 1000 to 100000 nodes and key length from 16-bit to 64-bit to assess the security of the network in the event of compromise of existing nodes.

Other Projects

- **Design of sub-100nm MOSFET:**
  o Designed a **sub-100nm** MOSFET using suitable process flow in **Sentaurus** with an effective Gate Length of **68nm** and oxide thickness of **1.5nm**, exhibiting a Ion/Ioff ratio of over $\sim \mathbf{80 \times 10^3}$ and threshold voltage of **0.2-0.4V**.
- **Design, Synthesis and Testing of an Expression Calculator**
  o Design, Synthesis and Testing of an Expression Calculator having two 32-bit operands and 1 binary operator using **VHDL**, tested on **DE0 Nano Board (Altera Cyclone IV EP4CE22F17C6N FPGA)** through **debouncer/synchronizer** implementation to interface with the keypad.
- **Design of Fully Differential Folded Cascode Opamp**
  o Designed a fully differential folded cascode opamp with Commonmode Feedback Circuit achieving a gain above **60 dB**, with a phase margin of **73-74^0**, a CMRR of **80-100 dB** in the input common mode range of **0.2V-1.1V**. Design also shows a differential slew rate of **289 mV/s** and unity gain frequency of **90 MHz.**

Major Academic Achievements

- Secured All India Rank**(AIR) 22** in GATE-2014, Electronics & Communication.
- Secured rank **98th** in Engineering in West Bengal Joint Entrance Examination 2009.
- Currently ranked **4th**(out of 118 students) in *Indian Institute of Technology, Bombay* M.Tech programme.
- Secured projected rank **32** (out of 661,042 students) in the Secondary Examination, 2007 (school-leaving) , with 95.4% marks.
- Secured **1st** position among 56 students in the course **Physics of Transistors(EE620).**

Relevant Courses

GRADUATE

Solid State Devices(AA), Physics of Transistors(AA), Nanoelectronics(AA), VLSI Technology(AA), Microelectronics Simulations Lab(AA)

UNDER-GRADUATE

IC Technology and Design(A), Material Science(A), Material Science Lab(S), Microelectronics & VLSI Lab(S)

Technical Skills

- **Equipment Exposure:** Proxima (Fast IV Measurement/ B1500)
- **Tools:** Sentaurus TCAD , MATLAB, Modelsim, Quartus, Multisim, NGSpice, Magic, CircuitMaker, Keil.
- **Languages:** VHDL, C, C++, 8085/ 8051(Assembly)
- **Hardware Exposure:** Altera Cyclone IV EP4CE22F17C6N FPGA, Atmel AT89c5131 based Pt-51 Board, Intel 8085 micro-processor chip, Intel 8051 micro-controller chip, DSP chip TMS 320

Personal Interests

- **Sports:** An avid football enthusiast, especially English Premier League.
- **Music:** An ardent follower of Indian Music, especially Hindustani Classical Music based on North Indian Ragas.