AGILEX™ 5 FPGA E-SERIES 065A PREMIUM DEVELOPMENT KIT (PRODUCTION)

REV	DATE	PAGES	DESCRIPTION
A1	05/30/2024	All	Initial Release
A2	09/23/2024	All 20	Update to Altera logo, and Altera copy right declaration Update CLK_SEL (U419) default state to Low status
A3	06/23/2025	13-16 8, 16, 19, 44	Update IO96B CDR assignment per A5ED065B pinout Clean up unused circuitry.
	09/17/2025	All	Dev Kit Production Version. Update Altera Schematic Template

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36	QSFP1		
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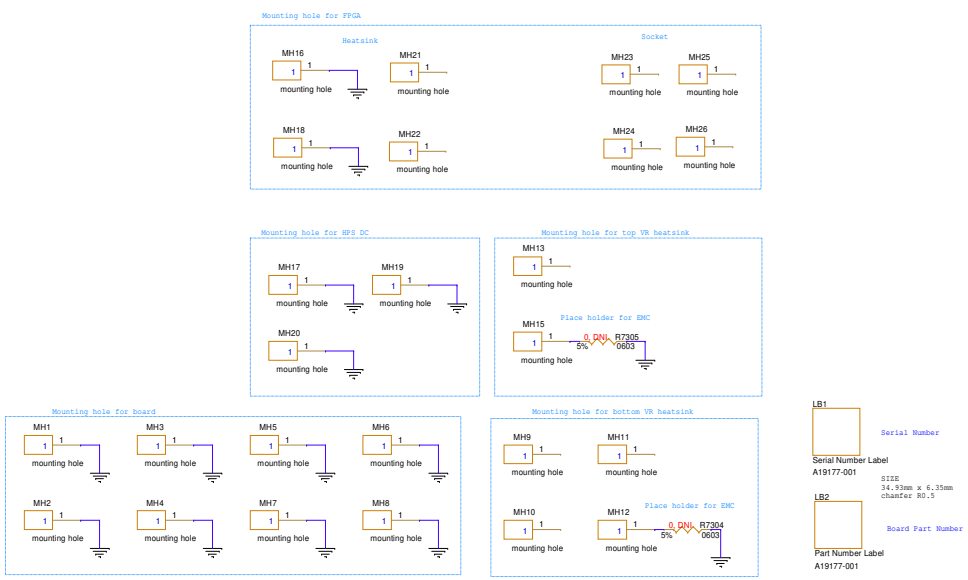
Board Name	Board OPN/ Board MMID	Device OPN/ Device MMID	TA/ PBA/ PB/ PCB MPN
Agilex TM 5 FPGA E-Series 065A Premium Development Kit (PRODUCTION)	DK-A5E065AB32AEA / 99D003	A5ED065AB32AE1V/ 99D56C	N83388-001/ N83389-101 N18468-003/ 100-0330713-A3



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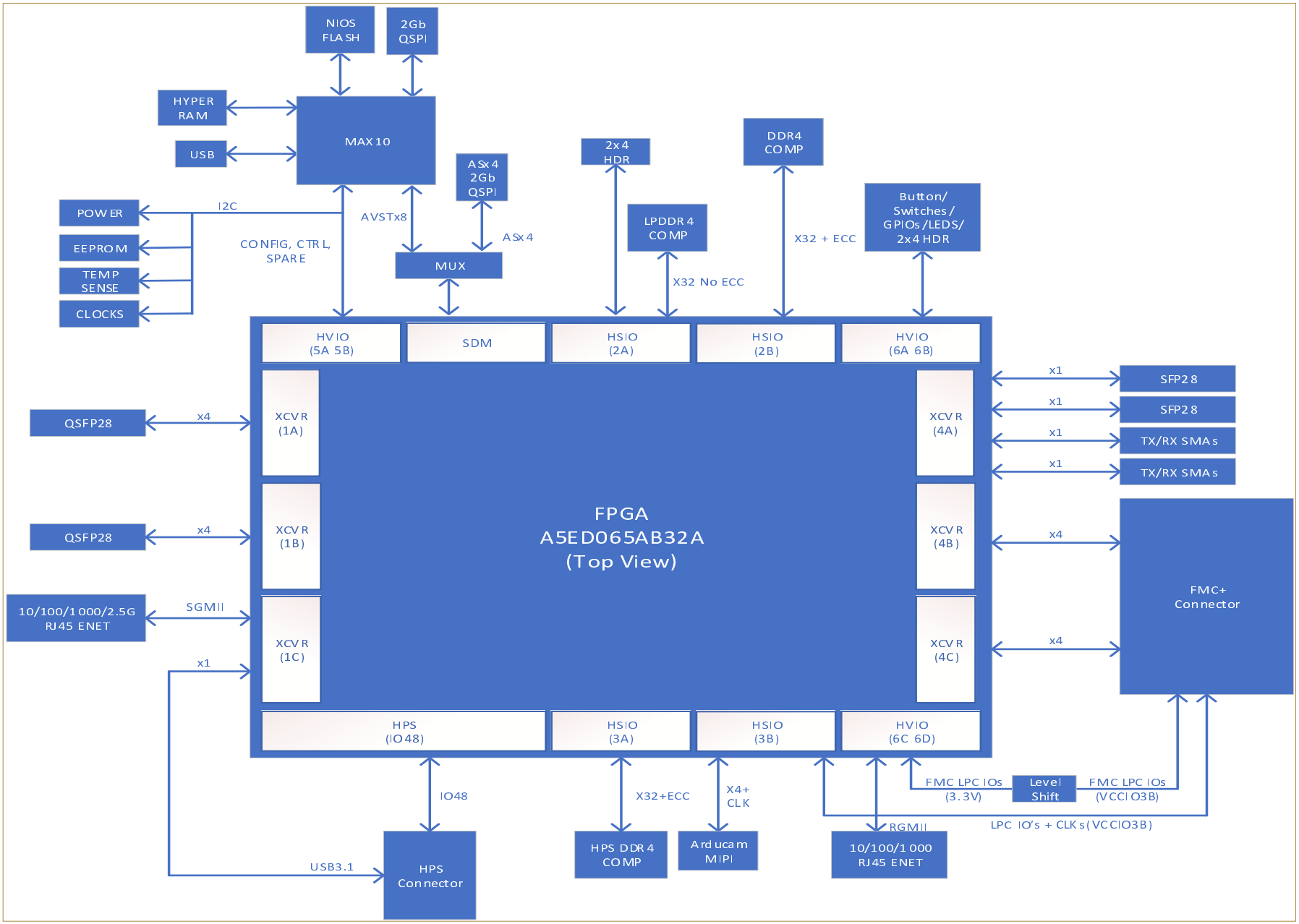

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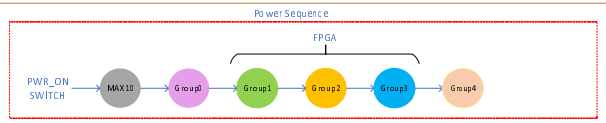
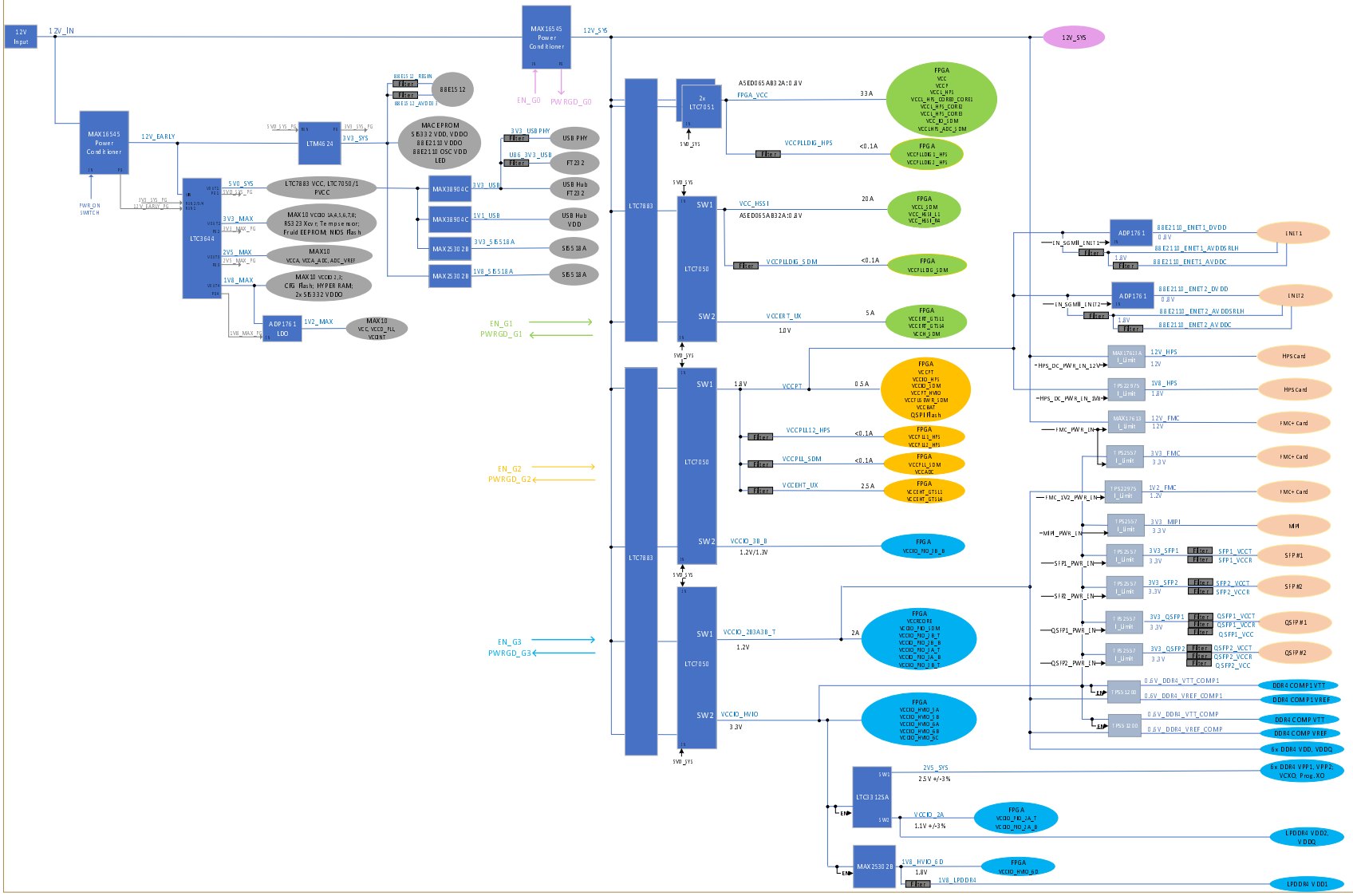
Recommendation:
Dev Kit power tree design are for reference.
Recommend customer to scale power solution based on design requirements





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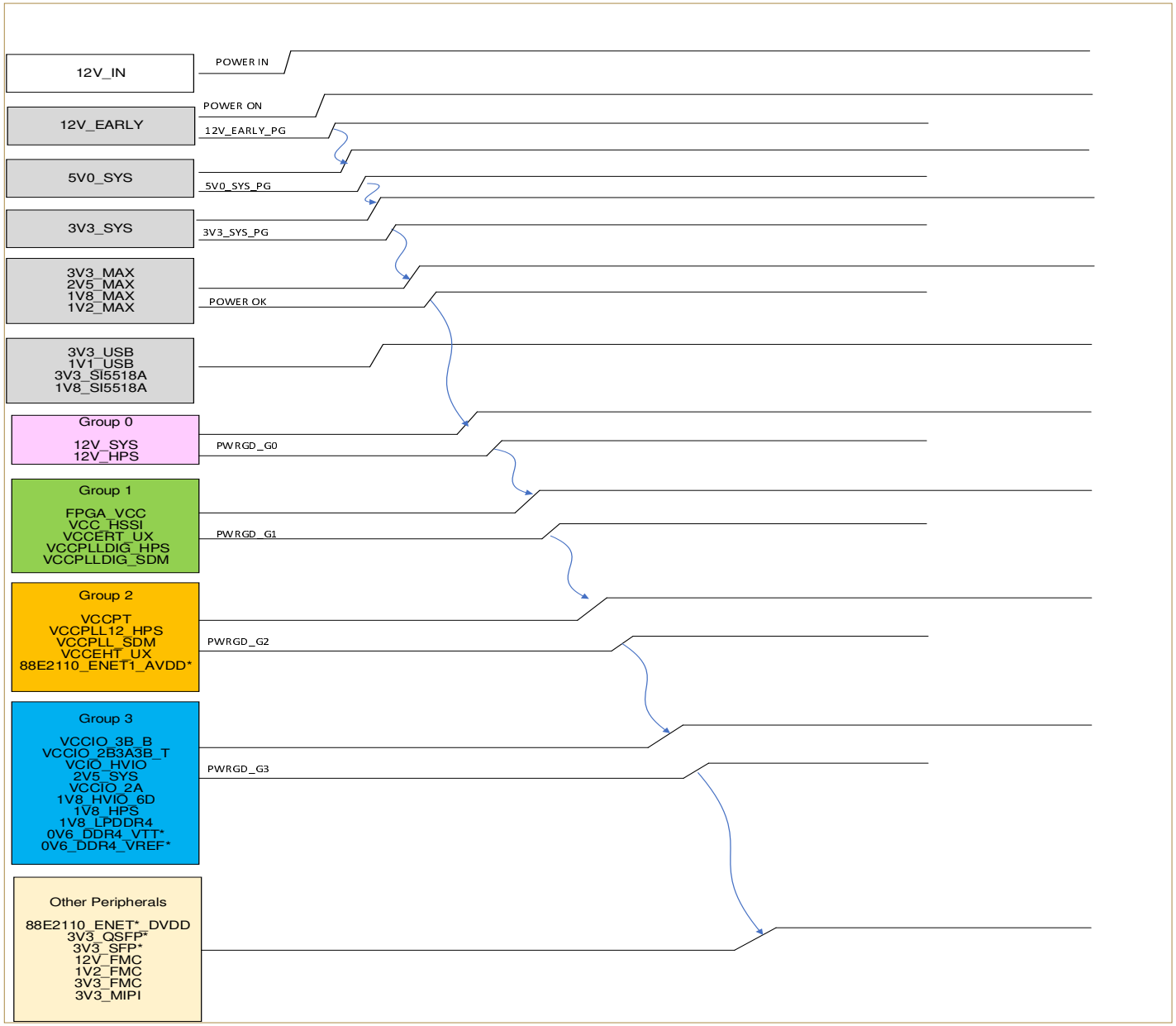

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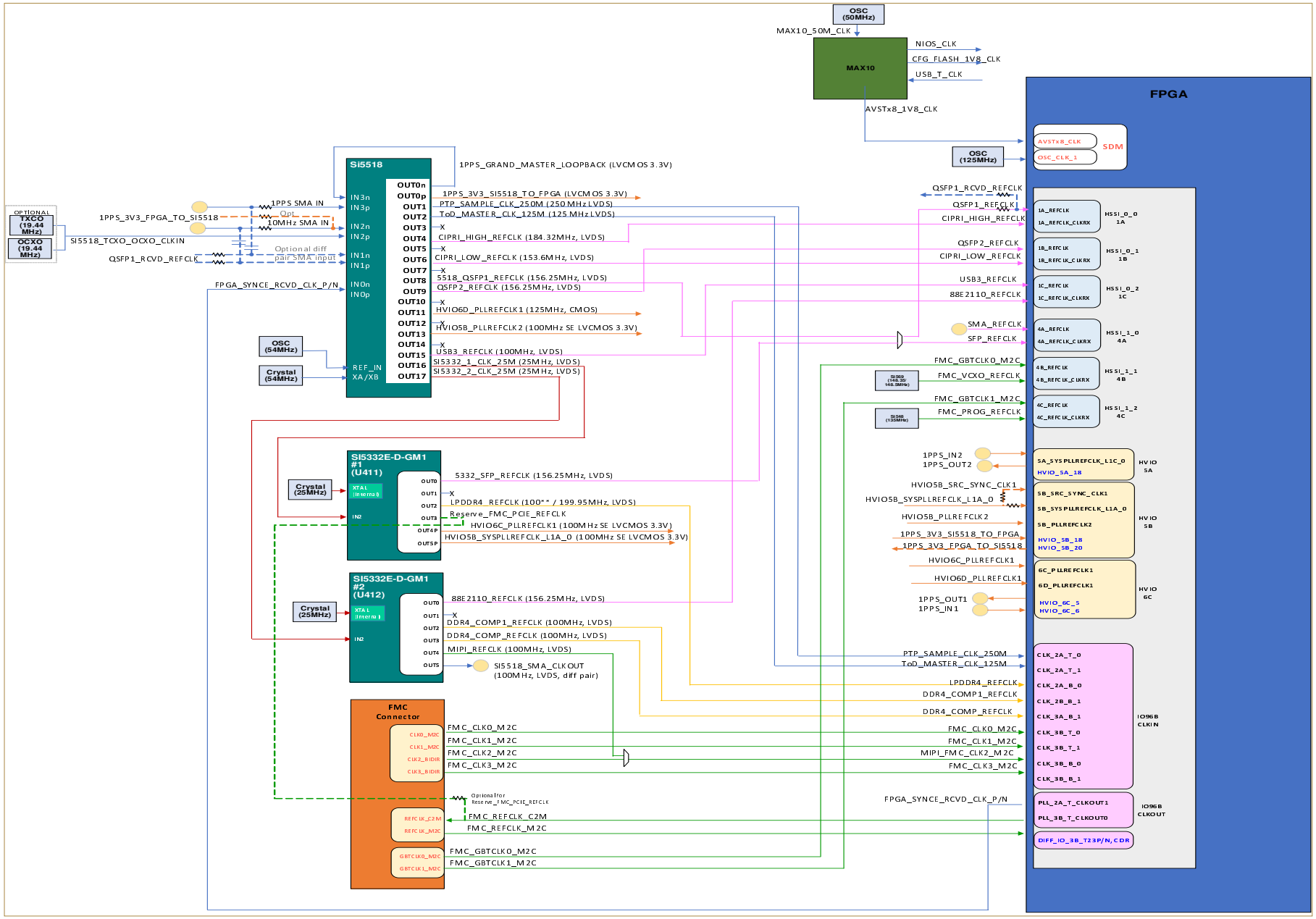

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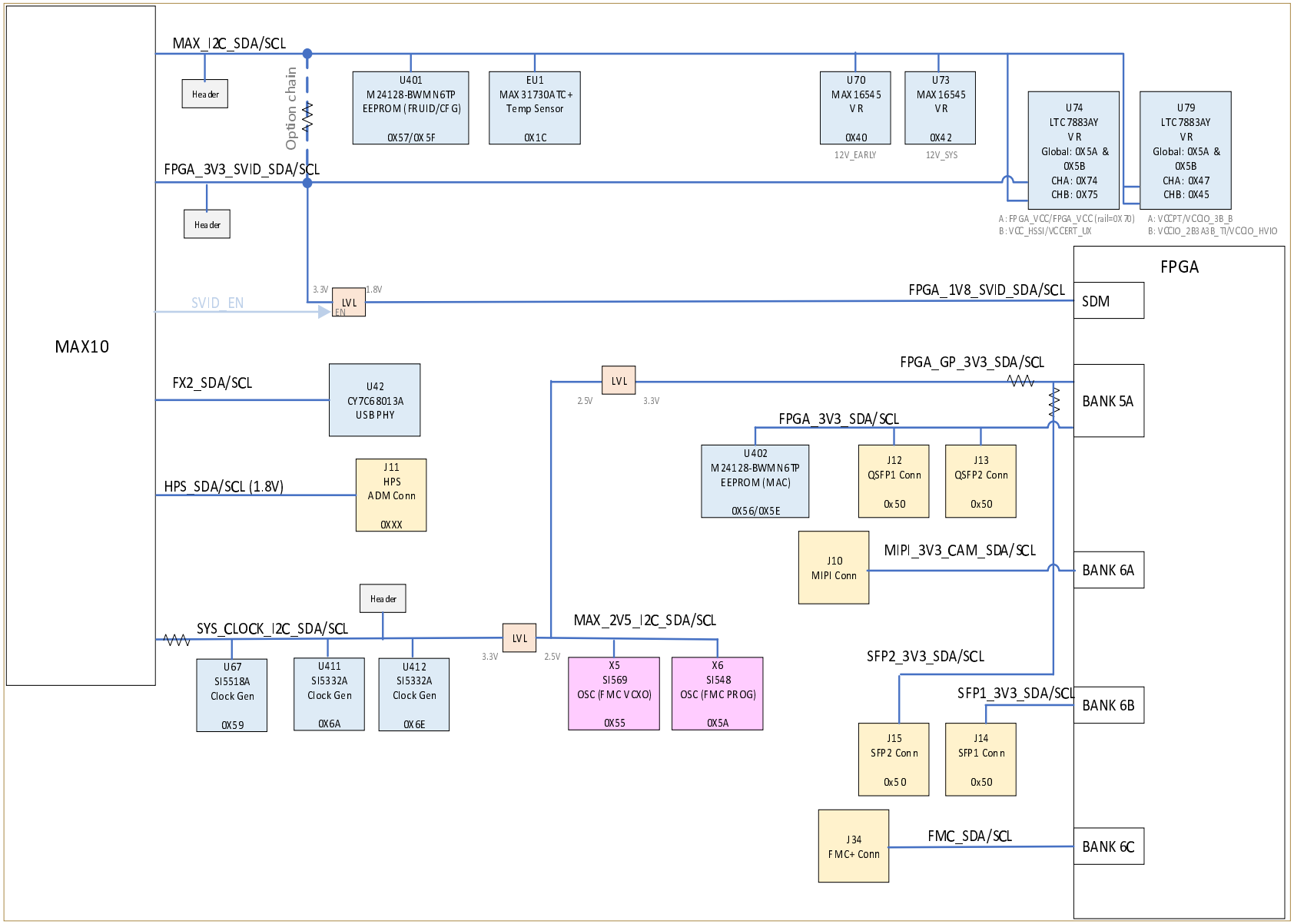

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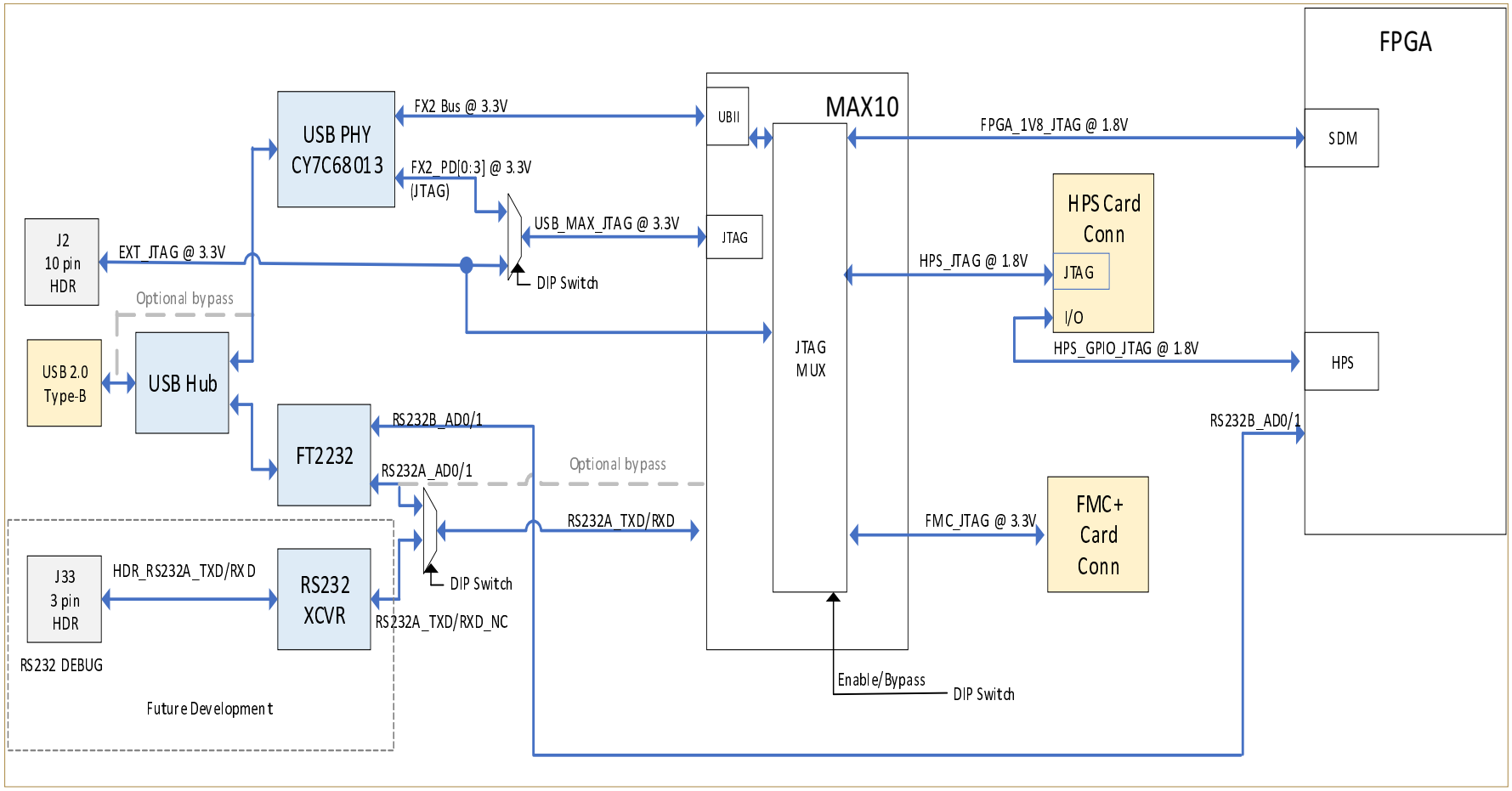

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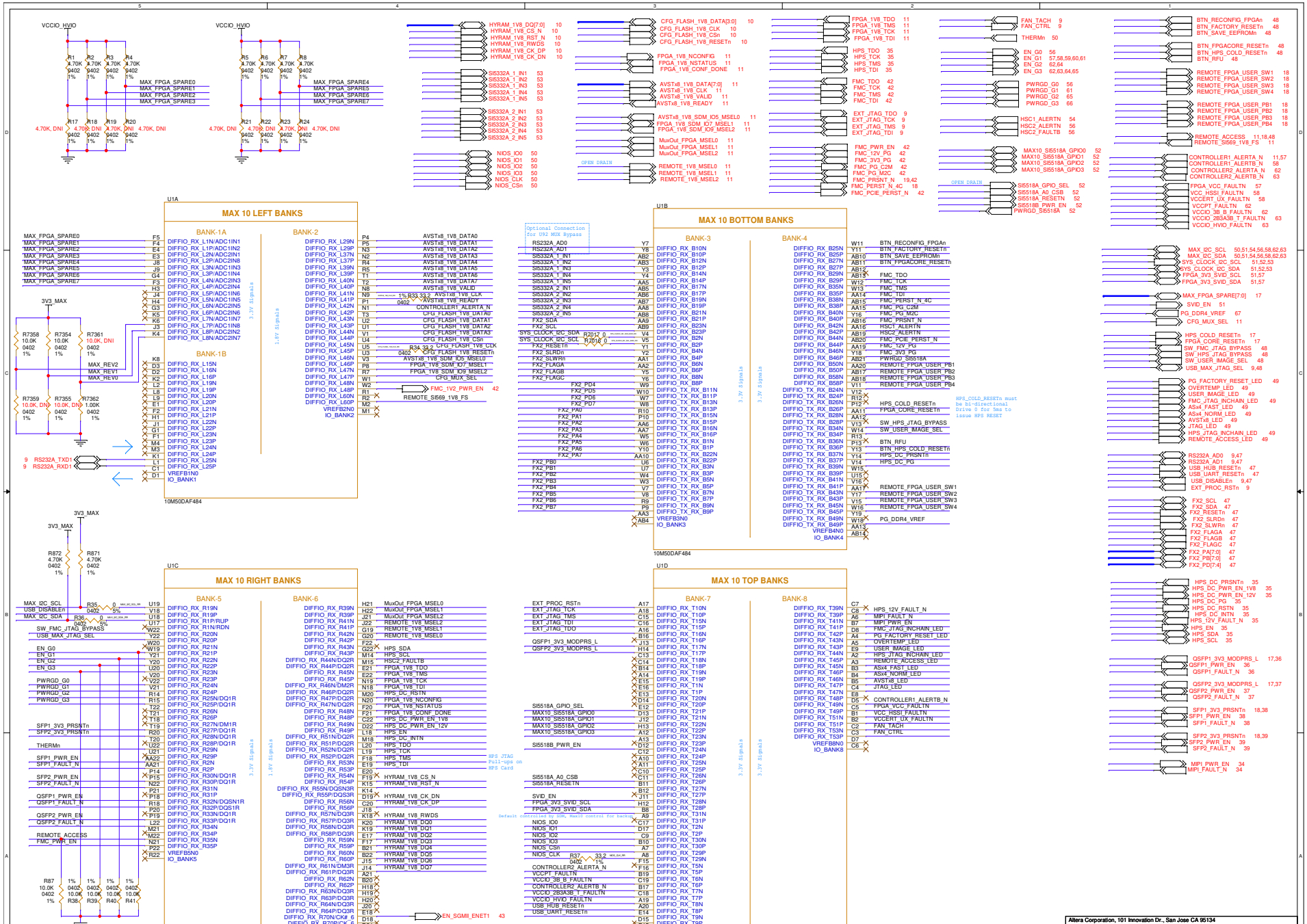

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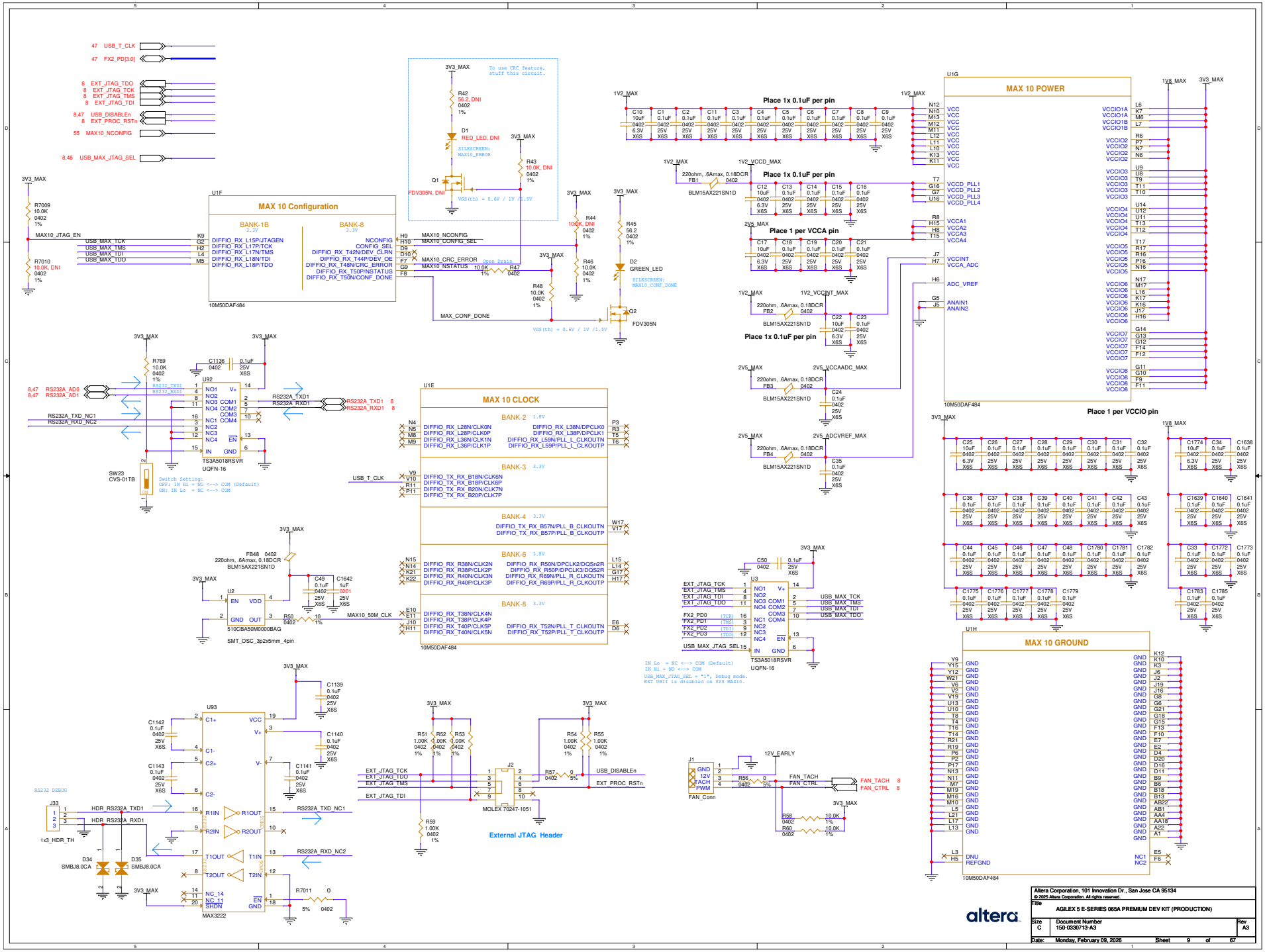

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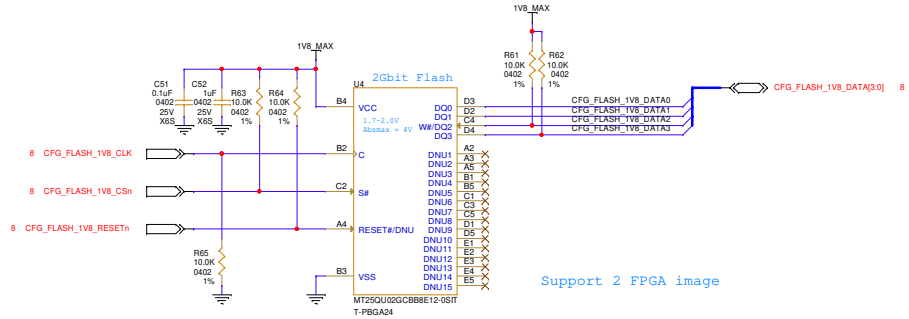
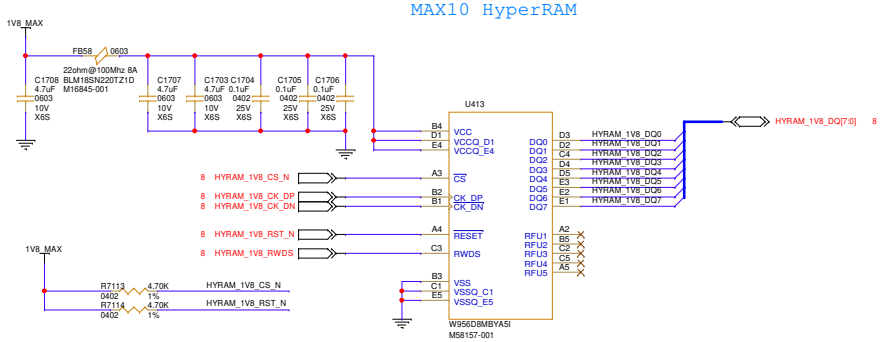
AVST CFG Flash



MAX10 HyperRAM



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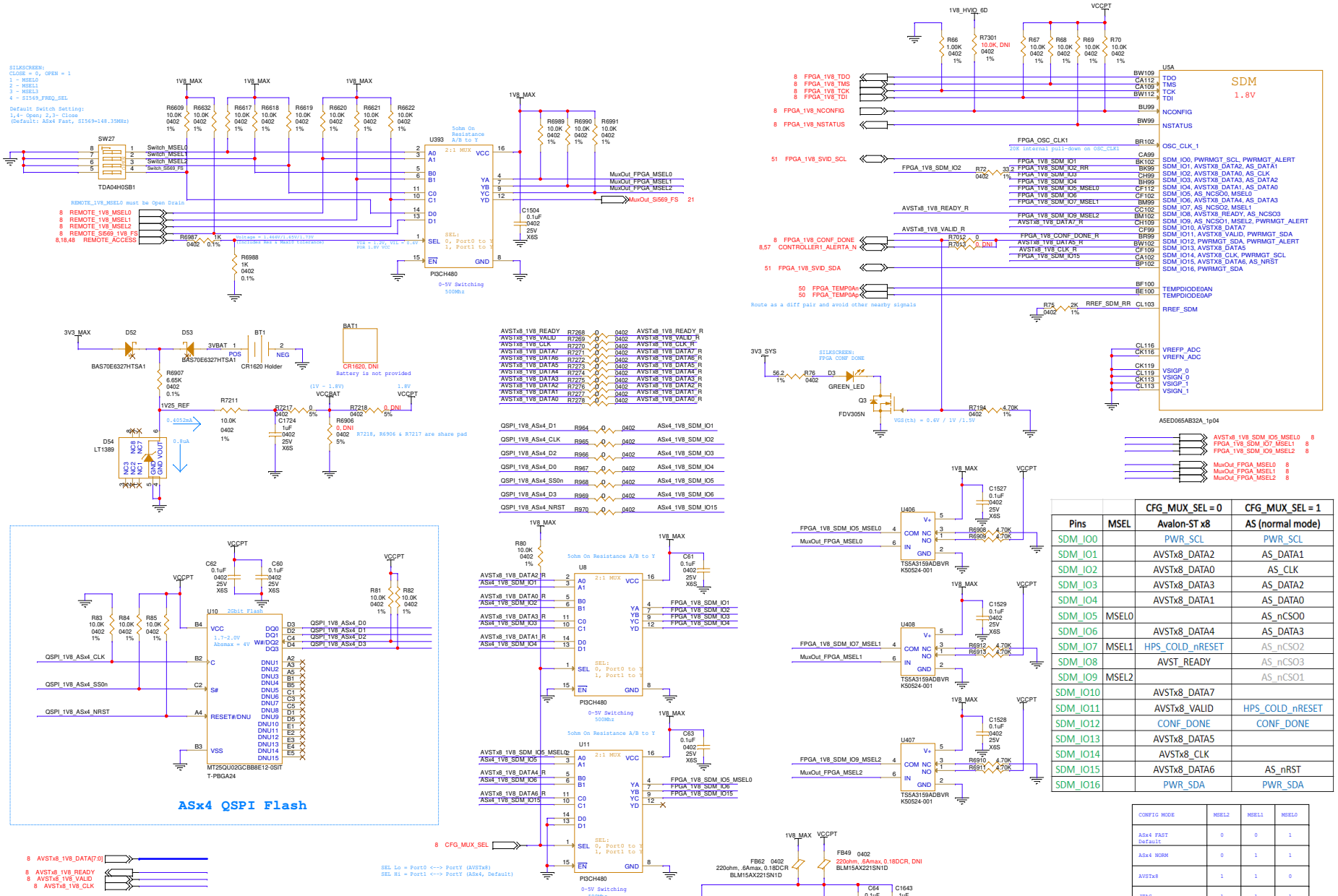
SDM CONFIGURATION



	CFG_MUX_SEL = 0	CFG_MUX_SEL = 1
Pins	Avalon-ST x8	AS (normal mode)
SDM_IO00	PWR_SCL	PWR_SCL
SDM_IO01	AVSTx8_DATA2	AS_DATA1
SDM_IO02	AVSTx8_DATA0	AS_CLK
SDM_IO03	AVSTx8_DATA3	AS_DATA2
SDM_IO04	AVSTx8_DATA1	AS_DATA0
SDM_IO05	MSEL0	AS_nCSO0
SDM_IO06	AVSTx8_DATA4	AS_DATA3
SDM_IO07	MSEL1	HPS_COLD_nRESET
SDM_IO08	AVST_READY	AS_nCSO2
SDM_IO09	MSEL2	AS_nCSO3
SDM_IO10	AVSTx8_DATA7	AS_nCSO1
SDM_IO11	AVSTx8_VALID	HPS_COLD_nRESET
SDM_IO12	CONF_DONE	CONF_DONE
SDM_IO13	AVSTx8_DATA5	
SDM_IO14	AVSTx8_CLK	
SDM_IO15	AVSTx8_DATA6	AS_nRST
SDM_IO16	PWR_SDA	PWR_SDA

CONFIG MODE	MSEL2	MSEL1	MSEL0
ASx4 FAST Default	0	0	1
ASx4 NORM	0	1	1
AVSTx8	1	1	0
JTAG	1	1	1

Note: MSEL0 is shared with QSPI_CSn which has a pull-up. MAX10 should make MSEL0 Open Drain.

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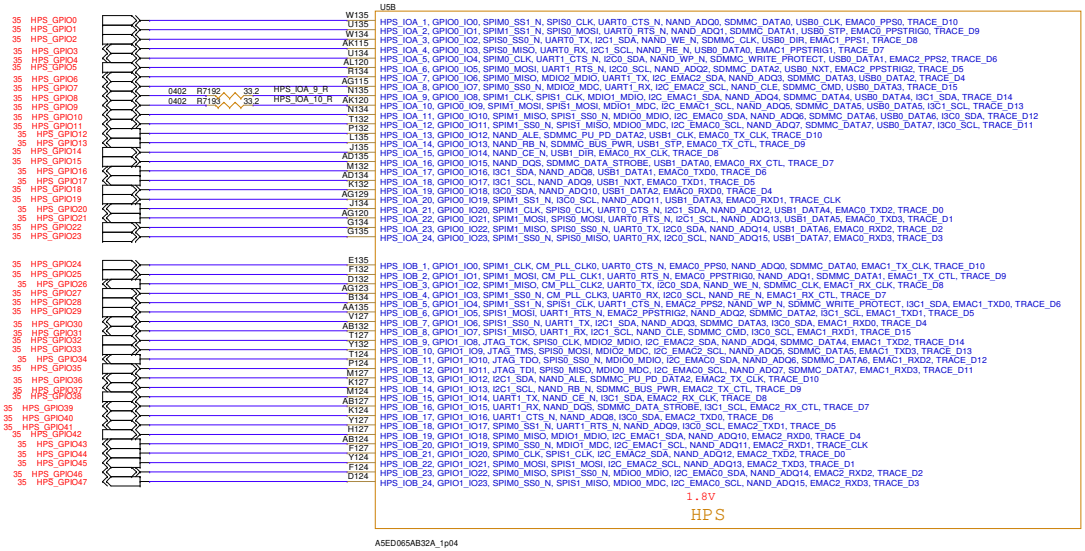
HPS BANK IO48



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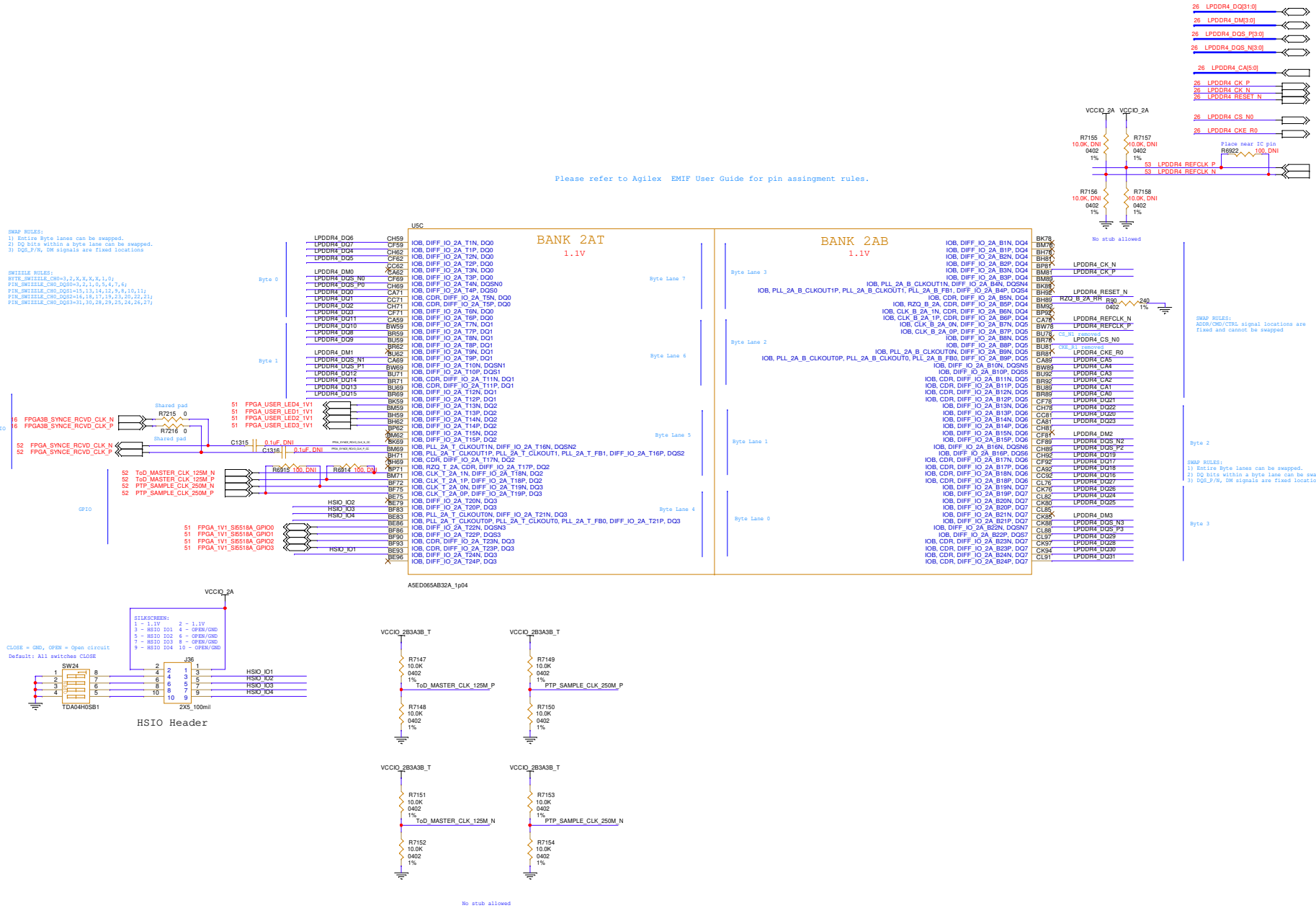
HSIO BANKS 2AL AND 2AR



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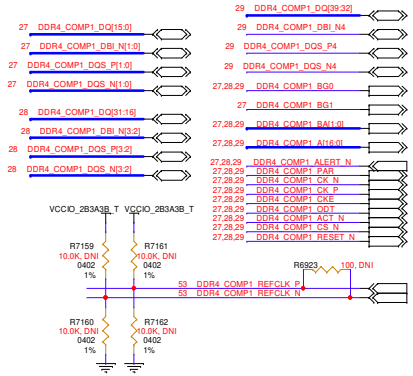
HSIO BANKS 2BL AND 2BR



Please refer to Agilex EMIF User Guide for pin assingment rules.

SWAP RULES:
1) Entire Byte lanes can be swapped.
2) DQ bits within a byte lane can be swapped.
3) DQS_P/N, DBI signals are fixed locations
4) ECC byte must be connected to Byte Lane 7.
5) For x16 device, DQ & DQS must be connected to one x16 device and placed on adjacent Byte Lane unless they are separated by ADD/CMD lane.

SWIZZLE RULES:
BYTE_SWIZZLE_CH0=0,X,X,X,1,2,3,ECC;
PIN_SWIZZLE_CH0_DQS0=3,1,7,5,0,4,6,2;
PIN_SWIZZLE_CH0_DQS1=11,9,15,13,12,14,8,10;
PIN_SWIZZLE_CH0_DQS2=17,21,19,23,16,22,18,20;
PIN_SWIZZLE_CH0_DQS3=29,31,27,25,30,26,24,28;
PIN_SWIZZLE_CH0_ECC=1,3,7,5,6,2,0,4;

U5D

BANK 2BT
1.2V

	DDR4_COMP1_DQ36	CC19	IOB, DIFF_IO_2B_T1N, DQ8
	DDR4_COMP1_DQ32	CF19	IOB, DIFF_IO_2B_T1P, DQ8
	DDR4_COMP1_DQ34	CH22	IOB, DIFF_IO_2B_T2N, DQ8
	DDR4_COMP1_DQ38	CF22	IOB, DIFF_IO_2B_T2P, DQ8
		CA22	IOB, DIFF_IO_2B_T3N, DQ8
ECC	DDR4_COMP1_DBI_N4	BC22	IOB, DIFF_IO_2B_T3P, DQ8
	DDR4_COMP1_DQS_N4	CC28	IOB, DIFF_IO_2B_T4N, DQSN8
	DDR4_COMP1_DQS_P4	CF28	IOB, DIFF_IO_2B_T4P, DQS8
	DDR4_COMP1_DQ37	CC31	IOB, CDR, DIFF_IO_2B_T5N, DQ8
	DDR4_COMP1_DQ39	CA31	IOB, CDR, DIFF_IO_2B_T5P, DQ8
	DDR4_COMP1_DQ35	CF31	IOB, DIFF_IO_2B_T6N, DQ8
	DDR4_COMP1_DQ33	CH31	IOB, DIFF_IO_2B_T6P, DQ8
	DDR4_COMP1_DQ28	CL6	IOB, DIFF_IO_2B_T7N, DQ9
	DDR4_COMP1_DQ24	CK8	IOB, DIFF_IO_2B_T7P, DQ9
	DDR4_COMP1_DQ26	CL8	IOB, DIFF_IO_2B_T8N, DQ9
	DDR4_COMP1_DQ30	CK11	IOB, DIFF_IO_2B_T8P, DQ9
		CL11	IOB, DIFF_IO_2B_T9N, DQ9
Byte 3	DDR4_COMP1_DBI_N3	CL14	IOB, DIFF_IO_2B_T9P, DQ9
	DDR4_COMP1_DQS_N3	CL17	IOB, DIFF_IO_2B_T10N, DQSN9
	DDR4_COMP1_DQS_P3	CK17	IOB, DIFF_IO_2B_T10P, DQS9
	DDR4_COMP1_DQ25	CK20	IOB, CDR, DIFF_IO_2B_T11N, DQ9
	DDR4_COMP1_DQ27	CL20	IOB, CDR, DIFF_IO_2B_T11P, DQ9
	DDR4_COMP1_DQ31	CK26	IOB, DIFF_IO_2B_T12N, DQ9
	DDR4_COMP1_DQ29	CL23	IOB, DIFF_IO_2B_T12P, DQ9
	DDR4_COMP1_DQ20	BF46	IOB, DIFF_IO_2B_T13N, DQ10
	DDR4_COMP1_DQ18	BE46	IOB, DIFF_IO_2B_T13P, DQ10
	DDR4_COMP1_DQ22	BE50	IOB, DIFF_IO_2B_T14N, DQ10
	DDR4_COMP1_DQ16	BF50	IOB, DIFF_IO_2B_T14P, DQ10
		BF53	IOB, DIFF_IO_2B_T15N, DQ10
Byte 2	DDR4_COMP1_DBI_N2	BF57	IOB, DIFF_IO_2B_T15P, DQ10
	DDR4_COMP1_DQS_N2	BE57	IOB, PLL_2B_T_CLKOUT1N, DIFF_IO_2B_T16N, DQSN10
	DDR4_COMP1_DQS_P2	BE61	IOB, PLL_2B_T_CLKOUT1P, PLL_2B_T_CLKOUT1, PLL_2B_T_FB1, DIFF_IO_2B_T16P, DQS10
	DDR4_COMP1_DQ23	BF64	IOB, CDR, DIFF_IO_2B_T17N, DQ10
	DDR4_COMP1_DQ19	BE64	IOB, RZQ_T_2B, CDR, DIFF_IO_2B_T17P, DQ10
	DDR4_COMP1_DQ21	BE68	IOB, CLK_T_2B_1N, DIFF_IO_2B_T18N, DQ10
	DDR4_COMP1_DQ17	BF68	IOB, CLK_T_2B_1P, DIFF_IO_2B_T18P, DQ10
	DDR4_COMP1_DQ10	BM38	IOB, CLK_T_2B_0N, DIFF_IO_2B_T19N, DQ11
	DDR4_COMP1_DQ8	BK38	IOB, CLK_T_2B_0P, DIFF_IO_2B_T19P, DQ11
	DDR4_COMP1_DQ14	BH41	IOB, DIFF_IO_2B_T20N, DQ11
	DDR4_COMP1_DQ12	BH38	IOB, DIFF_IO_2B_T20P, DQ11
		BM41	IOB, PLL_2B_T_CLKOUT0N, DIFF_IO_2B_T21N, DQ11
Byte 1	DDR4_COMP1_DBI_N1	BP41	IOB, PLL_2B_T_CLKOUT0P, PLL_2B_T_CLKOUT0, PLL_2B_T_FB0, DIFF_IO_2B_T21P, DQ11
	DDR4_COMP1_DQS_N1	BM49	IOB, DIFF_IO_2B_T22N, DQSN11
	DDR4_COMP1_DQS_P1	BK49	IOB, DIFF_IO_2B_T22P, DQS11
	DDR4_COMP1_DQ13	BH52	IOB, CDR, DIFF_IO_2B_T23N, DQ11
	DDR4_COMP1_DQ15	BH49	IOB, CDR, DIFF_IO_2B_T23P, DQ11
	DDR4_COMP1_DQ9	BP52	IOB, DIFF_IO_2B_T24N, DQ11
	DDR4_COMP1_DQ11	BM52	IOB, DIFF_IO_2B_T24P, DQ11

Byte Lane 7
Byte Lane 6
Byte Lane 5
Byte Lane 4

BANK 2BB
1.2V

		BW38	DDR4_COMP1_BG0
	IOB, DIFF_IO_2B_B1N, DQ12	CA38	DDR4_COMP1_BA1
	IOB, DIFF_IO_2B_B1P, DQ12	BU38	DDR4_COMP1_BA0
	IOB, DIFF_IO_2B_B2N, DQ12	BR38	DDR4_COMP1_ALERT_N
	IOB, DIFF_IO_2B_B2P, DQ12	BU41	DDR4_COMP1_A16
Byte Lane 3	IOB, DIFF_IO_2B_B3N, DQ12	BR41	DDR4_COMP1_A15
	IOB, DIFF_IO_2B_B3P, DQ12	CA49	DDR4_COMP1_A14
	IOB, PLL_2B_B_CLKOUT1N, DIFF_IO_2B_B4N, DQSN12	BW49	DDR4_COMP1_A13
	IOB, PLL_2B_B_CLKOUT1P, PLL_2B_B_CLKOUT1, PLL_2B_B_FB1, DIFF_IO_2B_B4P, DQS12	BU52	DDR4_COMP1_A12
	IOB, CDR, DIFF_IO_2B_B5N, DQ12	BR52	RZQ_B_2B_HR
	IOB, RZQ_B_2B, CDR, DIFF_IO_2B_B5P, DQ12	BU49	DDR4_COMP1_REFCLK_N
	IOB, CLK_B_2B_1N, CDR, DIFF_IO_2B_B6N, DQ12	BR49	DDR4_COMP1_REFCLK_P
	IOB, CLK_B_2B_1P, CDR, DIFF_IO_2B_B6P, DQ12	CF38	DDR4_COMP1_A11
	IOB, CLK_B_2B_0N, DIFF_IO_2B_B7N, DQ13	CH38	DDR4_COMP1_A10
	IOB, CLK_B_2B_0P, DIFF_IO_2B_B7P, DQ13	CA41	DDR4_COMP1_A9
	IOB, DIFF_IO_2B_B8N, DQ13	CC41	DDR4_COMP1_A8
	IOB, DIFF_IO_2B_B8P, DQ13	CF41	DDR4_COMP1_A7
	IOB, PLL_2B_B_CLKOUT0N, DIFF_IO_2B_B9N, DQ13	CH41	DDR4_COMP1_A6
Byte Lane 2	IOB, PLL_2B_B_CLKOUT0P, PLL_2B_B_CLKOUT0, PLL_2B_B_FB0, DIFF_IO_2B_B9P, DQ13	CH49	DDR4_COMP1_A5
	IOB, DIFF_IO_2B_B10N, DQSN13	CF49	DDR4_COMP1_A4
	IOB, DIFF_IO_2B_B10P, DQS13	CA52	DDR4_COMP1_A3
	IOB, CDR, DIFF_IO_2B_B11N, DQ13	CC52	DDR4_COMP1_A2
	IOB, CDR, DIFF_IO_2B_B11P, DQ13	CH52	DDR4_COMP1_A1
	IOB, CDR, DIFF_IO_2B_B12N, DQ13	CF52	DDR4_COMP1_A0
	IOB, CDR, DIFF_IO_2B_B12P, DQ13	CL38	DDR4_COMP1_PAR
	IOB, DIFF_IO_2B_B13N, DQ14	CK30	
	IOB, DIFF_IO_2B_B13P, DQ14	CL38	DDR4_COMP1_CK_N
	IOB, DIFF_IO_2B_B14N, DQ14	CK33	DDR4_COMP1_CK_P
	IOB, DIFF_IO_2B_B14P, DQ14	CL35	
	IOB, DIFF_IO_2B_B15N, DQ14	CK35	DDR4_COMP1_CKE
	IOB, DIFF_IO_2B_B15P, DQ14	CL39	
	IOB, DIFF_IO_2B_B16N, DQSN14	CK38	DDR4_COMP1_ODT
Byte Lane 1	IOB, DIFF_IO_2B_B16P, DQS14	CL45	DDR4_COMP1_ACT_N
	IOB, CDR, DIFF_IO_2B_B17N, DQ14	CK48	DDR4_COMP1_CS_N
	IOB, CDR, DIFF_IO_2B_B17P, DQ14	CK45	DDR4_COMP1_RESET_N
	IOB, CDR, DIFF_IO_2B_B18N, DQ14	CL42	DDR4_COMP1_BG1
	IOB, CDR, DIFF_IO_2B_B18P, DQ14	CK54	DDR4_COMP1_DQ2
	IOB, DIFF_IO_2B_B19N, DQ15	CL51	DDR4_COMP1_DQ6
	IOB, DIFF_IO_2B_B19P, DQ15	CL54	DDR4_COMP1_DQ4
	IOB, DIFF_IO_2B_B20N, DQ15	CK56	DDR4_COMP1_DQ0
	IOB, DIFF_IO_2B_B20P, DQ15	CL60	
	IOB, DIFF_IO_2B_B21N, DQ15	CL56	DDR4_COMP1_DBI_N0
Byte Lane 0	IOB, DIFF_IO_2B_B21P, DQ15	CL66	DDR4_COMP1_DQS_N0
	IOB, DIFF_IO_2B_B22N, DQSN15	CK63	DDR4_COMP1_DQS_P0
	IOB, DIFF_IO_2B_B22P, DQS15	CL73	DDR4_COMP1_DQ5
	IOB, CDR, DIFF_IO_2B_B23N, DQ15	CK73	DDR4_COMP1_DQ7
	IOB, CDR, DIFF_IO_2B_B23P, DQ15	CL70	DDR4_COMP1_DQ1
	IOB, CDR, DIFF_IO_2B_B24N, DQ15	CK66	DDR4_COMP1_DQ3
	IOB, CDR, DIFF_IO_2B_B24P, DQ15		

Byte Lane 3
Byte Lane 2
Byte Lane 1
Byte Lane 0

Place near RZQ pin
R91 240 0402 1%

SWAP RULES:
ADDR/CMD/CTRL signal locations are fixed and cannot be swapped

Byte 0

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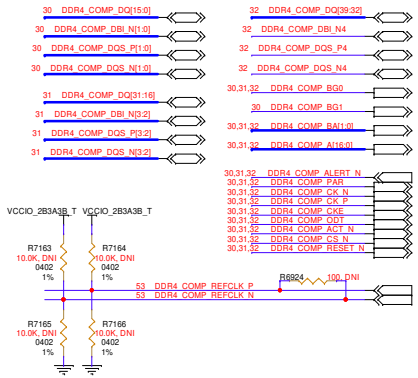
HSIO BANKS 3AL AND 3AR



Please refer to Agilex EMIF User Guide for pin assingment rules.

U5E

BANK 3AT
1.2V

	DDR4_COMP_DQ33	A91	IOB, DIFF_IO_3A_T1N, DQ16
	DDR4_COMP_DQ39	B88	IOB, DIFF_IO_3A_T1P, DQ16
	DDR4_COMP_DQ35	A94	IOB, DIFF_IO_3A_T2N, DQ16
	DDR4_COMP_DQ37	B91	IOB, DIFF_IO_3A_T2P, DQ16
		A97	IOB, DIFF_IO_3A_T3N, DQ16
ECC	DDR4_COMP_DBI_N4	B97	IOB, DIFF_IO_3A_T3P, DQ16, AVST_READY
	DDR4_COMP_DQS_N4	B101	IOB, DIFF_IO_3A_T4N, DQSN16
	DDR4_COMP_DQS_P4	A101	IOB, DIFF_IO_3A_T4P, DQS16
	DDR4_COMP_DQ36	A110	IOB, CDR, DIFF_IO_3A_T5N, DQ16
	DDR4_COMP_DQ32	B106	IOB, CDR, DIFF_IO_3A_T5P, DQ16
	DDR4_COMP_DQ38	B103	IOB, DIFF_IO_3A_T6N, DQ16
	DDR4_COMP_DQ34	A106	IOB, DIFF_IO_3A_T6P, DQ16
	DDR4_COMP_DQ29	D84	IOB, DIFF_IO_3A_T7N, DQ17, AVST_DATA10
	DDR4_COMP_DQ31	F84	IOB, DIFF_IO_3A_T7P, DQ17, AVST_DATA9
	DDR4_COMP_DQ27	M87	IOB, DIFF_IO_3A_T8N, DQ17, AVST_DATA8
	DDR4_COMP_DQ25	K87	IOB, DIFF_IO_3A_T8P, DQ17, AVST_VALID
		F87	IOB, DIFF_IO_3A_T9N, DQ17, AVST_DATA7
Byte 3	DDR4_COMP_DBI_N3	H87	IOB, DIFF_IO_3A_T9P, DQ17, AVST_DATA6
	DDR4_COMP_DQS_N3	D95	IOB, DIFF_IO_3A_T10N, DQSN17, AVST_DATA5
	DDR4_COMP_DQS_P3	F95	IOB, DIFF_IO_3A_T10P, DQS17, AVST_DATA4
	DDR4_COMP_DQ24	K98	IOB, CDR, DIFF_IO_3A_T11N, DQ17, AVST_DATA3
	DDR4_COMP_DQ28	M98	IOB, CDR, DIFF_IO_3A_T11P, DQ17, AVST_DATA2
	DDR4_COMP_DQ30	F98	IOB, DIFF_IO_3A_T12N, DQ17, AVST_DATA1
	DDR4_COMP_DQ26	H98	IOB, DIFF_IO_3A_T12P, DQ17, AVST_DATA0
	DDR4_COMP_DQ21	P84	IOB, DIFF_IO_3A_T13N, DQ18
	DDR4_COMP_DQ19	T84	IOB, DIFF_IO_3A_T13P, DQ18
	DDR4_COMP_DQ17	M84	IOB, DIFF_IO_3A_T14N, DQ18
	DDR4_COMP_DQ23	K84	IOB, DIFF_IO_3A_T14P, DQ18
		T87	IOB, DIFF_IO_3A_T15N, DQ18
Byte 2	DDR4_COMP_DBI_N2	V87	IOB, DIFF_IO_3A_T15P, DQ18
	DDR4_COMP_DQS_N2	M95	IOB, PLL_3A_T_CLKOUT1N, DIFF_IO_3A_T16N, DQSN18
	DDR4_COMP_DQS_P2	K95	IOB, PLL_3A_T_CLKOUT1P, PLL_3A_T_CLKOUT1, PLL_3A_T_FB1, DIFF_IO_3A_T16P, DQS18
	DDR4_COMP_DQ22	T95	IOB, CDR, DIFF_IO_3A_T17N, DQ18
	DDR4_COMP_DQ18	P95	IOB, RZQ_T_3A, CDR, DIFF_IO_3A_T17P, DQ18
	DDR4_COMP_DQ16	T98	IOB, CLK_T_3A_1N, DIFF_IO_3A_T18N, DQ18
	DDR4_COMP_DQ20	V98	IOB, CLK_T_3A_1P, DIFF_IO_3A_T18P, DQ18
	DDR4_COMP_DQ9	Y84	IOB, CLK_T_3A_0N, DIFF_IO_3A_T19N, DQ19
	DDR4_COMP_DQ13	Y87	IOB, CLK_T_3A_0P, DIFF_IO_3A_T19P, DQ19
	DDR4_COMP_DQ10	Y95	IOB, DIFF_IO_3A_T20N, DQ19
	DDR4_COMP_DQ14	Y98	IOB, DIFF_IO_3A_T20P, DQ19
		AC86	IOB, PLL_3A_T_CLKOUT0N, DIFF_IO_3A_T21N, DQ19
Byte 1	DDR4_COMP_DBI_N1	AC90	IOB, PLL_3A_T_CLKOUT0P, PLL_3A_T_CLKOUT0, PLL_3A_T_FB0, DIFF_IO_3A_T21P, DQ19
	DDR4_COMP_DQS_N1	AG93	IOB, DIFF_IO_3A_T22N, DQSN19, AVST_CLK
	DDR4_COMP_DQS_P1	AG90	IOB, DIFF_IO_3A_T22P, DQS19, AVST_DATA15
	DDR4_COMP_DQ11	AC96	IOB, CDR, DIFF_IO_3A_T23N, DQ19, AVST_DATA14
	DDR4_COMP_DQ8	AC100	IOB, CDR, DIFF_IO_3A_T23P, DQ19, AVST_DATA13
	DDR4_COMP_DQ15	AG104	IOB, DIFF_IO_3A_T24N, DQ19, AVST_DATA12
	DDR4_COMP_DQ12	AG100	IOB, DIFF_IO_3A_T24P, DQ19, AVST_DATA11

Byte Lane 7
Byte Lane 6
Byte Lane 5
Byte Lane 4

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BANK 3AB
1.2V

		AB105	IOB, DIFF_IO_3A_B1N, DQ20
		Y105	IOB, DIFF_IO_3A_B1P, DQ20
		AB108	IOB, DIFF_IO_3A_B2N, DQ20
		Y108	IOB, DIFF_IO_3A_B2P, DQ20
		AK104	IOB, DIFF_IO_3A_B3N, DQ20
Byte Lane 3		AK107	IOB, DIFF_IO_3A_B3P, DQ20
		AB114	IOB, PLL_3A_B_CLKOUT1N, DIFF_IO_3A_B4N, DQSN20
		Y114	IOB, PLL_3A_B_CLKOUT1P, PLL_3A_B_FB1, DIFF_IO_3A_B4P, DQS20
		AG111	IOB, CDR, DIFF_IO_3A_B5N, DQ20
		AK111	IOB, RZQ_B_3A, CDR, DIFF_IO_3A_B5P, DQ20
		Y117	IOB, CLK_B_3A_1N, CDR, DIFF_IO_3A_B6N, DQ20
		AB117	IOB, CLK_B_3A_1P, CDR, DIFF_IO_3A_B6P, DQ20
		K105	IOB, CLK_B_3A_0N, DIFF_IO_3A_B7N, DQ21
		M105	IOB, CLK_B_3A_0P, DIFF_IO_3A_B7P, DQ21
		P105	IOB, DIFF_IO_3A_B8N, DQ21
Byte Lane 2		T105	IOB, DIFF_IO_3A_B8P, DQ21
		T108	IOB, PLL_3A_B_CLKOUT0N, DIFF_IO_3A_B9N, DQ21
		V108	IOB, PLL_3A_B_CLKOUT0P, PLL_3A_B_CLKOUT0, PLL_3A_B_FB0, DIFF_IO_3A_B9P, DQ21
		K114	IOB, DIFF_IO_3A_B10N, DQSN21
		M114	IOB, DIFF_IO_3A_B10P, DQS21
		T117	IOB, CDR, DIFF_IO_3A_B11N, DQ21
		V117	IOB, CDR, DIFF_IO_3A_B11P, DQ21
		P114	IOB, CDR, DIFF_IO_3A_B12N, DQ21
		T114	IOB, CDR, DIFF_IO_3A_B12P, DQ21
		K108	IOB, DIFF_IO_3A_B13N, DQ22
		M108	IOB, DIFF_IO_3A_B13P, DQ22
		F108	IOB, DIFF_IO_3A_B14N, DQ22
		H108	IOB, DIFF_IO_3A_B14P, DQ22
		D105	IOB, DIFF_IO_3A_B15N, DQ22
Byte Lane 1		F109	IOB, DIFF_IO_3A_B15P, DQ22
		D114	IOB, DIFF_IO_3A_B16N, DQSN22
		F114	IOB, DIFF_IO_3A_B16P, DQS22
		M117	IOB, CDR, DIFF_IO_3A_B17N, DQ22
		K117	IOB, CDR, DIFF_IO_3A_B17P, DQ22
		H117	IOB, CDR, DIFF_IO_3A_B18N, DQ22
		F117	IOB, CDR, DIFF_IO_3A_B18P, DQ22
		A113	IOB, DIFF_IO_3A_B19N, DQ23
		B113	IOB, DIFF_IO_3A_B19P, DQ23
		A116	IOB, DIFF_IO_3A_B20N, DQ23
		B116	IOB, DIFF_IO_3A_B20P, DQ23
		A122	IOB, DIFF_IO_3A_B21N, DQ23
Byte Lane 0		B119	IOB, DIFF_IO_3A_B21P, DQ23
		A125	IOB, DIFF_IO_3A_B22N, DQSN23
		B122	IOB, DIFF_IO_3A_B22P, DQS23
		A130	IOB, CDR, DIFF_IO_3A_B23N, DQ23
		B130	IOB, CDR, DIFF_IO_3A_B23P, DQ23
		A128	IOB, CDR, DIFF_IO_3A_B24N, DQ23
		B128	IOB, CDR, DIFF_IO_3A_B24P, DQ23

DDR4_COMP_BG0	
DDR4_COMP_BA1	
DDR4_COMP_BA0	
DDR4_COMP_ALERT_N	
DDR4_COMP_A15	
DDR4_COMP_A14	
DDR4_COMP_A13	
DDR4_COMP_A12	
RZQ_B_3A_RR	
DDR4_COMP_REFCLK_N	
DDR4_COMP_REFCLK_P	
DDR4_COMP_A11	
DDR4_COMP_A10	
DDR4_COMP_A9	
DDR4_COMP_A8	
DDR4_COMP_A7	
DDR4_COMP_A6	
DDR4_COMP_A5	
DDR4_COMP_A4	
DDR4_COMP_A3	
DDR4_COMP_A2	
DDR4_COMP_A1	
DDR4_COMP_A0	
DDR4_COMP_PAR	
DDR4_COMP_CK_N	
DDR4_COMP_CK_P	
DDR4_COMP_CKE	
DDR4_COMP_ODT	
DDR4_COMP_ACT_N	
DDR4_COMP_CS_N	
DDR4_COMP_RESET_N	
DDR4_COMP_BG1	
DDR4_COMP_DQ7	
DDR4_COMP_DQ5	
DDR4_COMP_DQ3	
DDR4_COMP_DQ1	
DDR4_COMP_DBI_N0	
DDR4_COMP_DQS_N0	
DDR4_COMP_DQS_P0	
DDR4_COMP_DQ4	
DDR4_COMP_DQ6	
DDR4_COMP_DQ2	
DDR4_COMP_DQ0	

R92 240 0402 1%

Place near REQ pin

SWAP RULES:
1) Entire Byte lanes can be swapped.
2) DQ bits within a byte lane can be swapped.
3) DQS_P/N, DBI signals are fixed locations
4) ECC byte must be connected to Byte Lane 7.
5) For x16 device, DQ0 & DQ1 must be connected to one x16 device and placed on adjacent Byte Lane unless they are separated by ADD/CMD lane.

SWIZZLE RULES:
BYTE_SWIZZLE_CH0=0,X,X,X,1,2,3,ECC;
PIN_SWIZZLE_CH0_DQS0=0,2,6,4,1,3,5,7;
PIN_SWIZZLE_CH0_DQS1=12,15,8,11,14,10,13,9;
PIN_SWIZZLE_CH0_DQS2=20,16,18,22,23,17,19,21;
PIN_SWIZZLE_CH0_DQS3=26,30,28,24,25,27,31,29;
PIN_SWIZZLE_CH0_ECC=2,6,0,4,5,3,7,1;

SWAP RULES:
ADDR/CMD/CTRL signal locations are fixed and cannot be swapped

Byte 0

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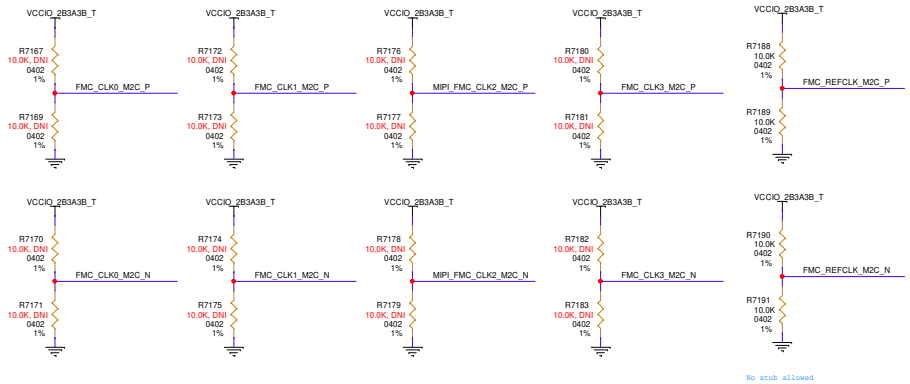
Pin placement restriction for MIPI & LVDS mixing with LVCMOS:

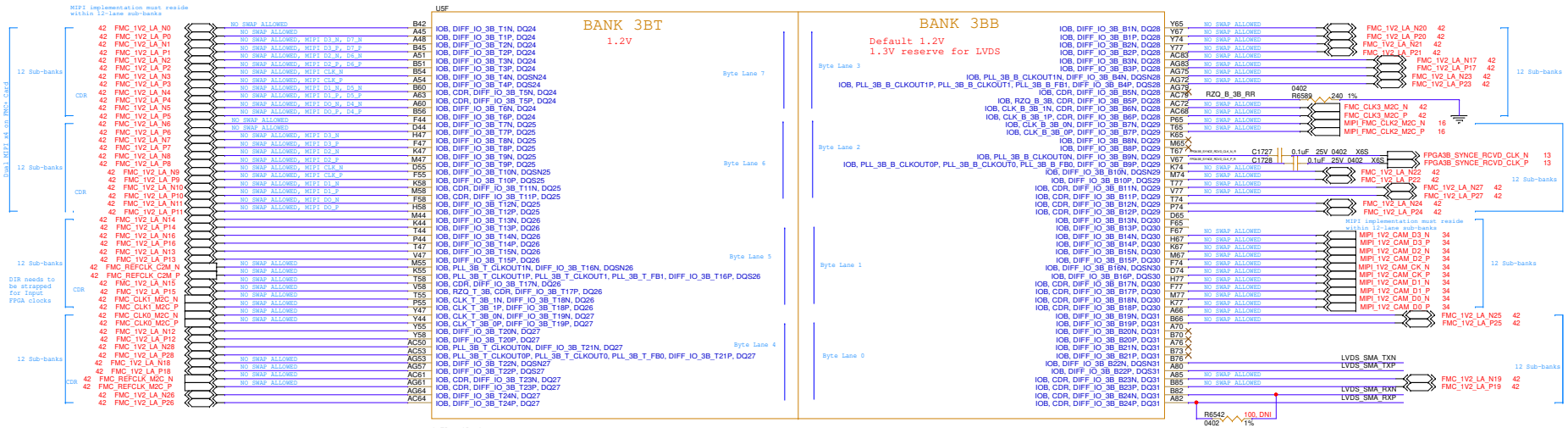
IO Lane Used for MIPI	Width	Restricted Pin Used As LVCMOS	
		Pin Index	Pin Number
IO Lane 1	1 data + 1 clock	P26	V77
	2 data + 1 clock	P26	V77
	4 data + 1 clock	P26 , P10	V77, B66
IO Lane 6	1 data + 1 clock	P75 , P87	K58, B60
	2 data + 1 clock	P87	B60
	4 data + 1 clock	P87, P70 , P82	B60, K44, D44
IO Lane 7	1 data + 1 clock	P86 ; P2 from Bank 3A	A63, B130
	2 data + 1 clock	P77 ; P2 from Bank 3A	D55, B130
	4 data + 1 clock	P77, P83,P94 ; P2 from Bank 3A	D55, F44, A45, B130
IO Lane 6 and 7	8 data + 1 clock	P70, P82, P83, P89 ,P94	K44, D44,F44,B54,A45

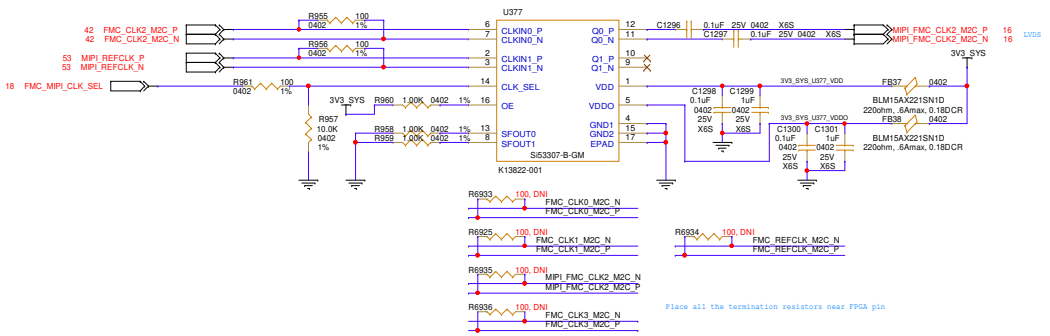
IO Lane Used for LVDS	Function	Restricted Pin Used As LVCMOS	
		Pin Index	Pin Number
IO Lane 0	LVDS_SMA_RX	P3	A85
	LVDS_SMA_TX	-	-
IO Lane 2	FPGA3B_SYNCE_RCVD_CLK	-	-
	MIPI_FMC_CLK2_M2C	P43	AC83
IO Lane 3	FMC_CLK3_M2C	P38, P41	AC79 (RZQ), AG75
IO Lane 4	FMC_REFCLK_M2C	P40, P48	AG72, AC64
	FMC_CLK0_M2C	P57, P67	Y55, T47
IO Lane 5	FMC_CLK1_M2C	P62	V58
	FMC_REFCLK_C2M	P74	M58

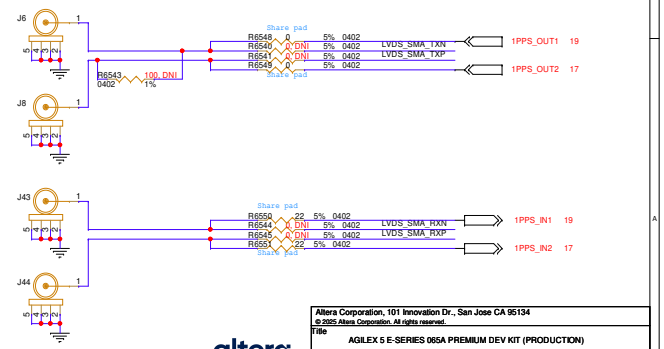
NOTES: Please check the detail restriction guide from IO Pinout Guideline Document if any of the FMC_1V2_LA_* to be used as LVDS.

HSIO BANKS 3BL AND 3BR









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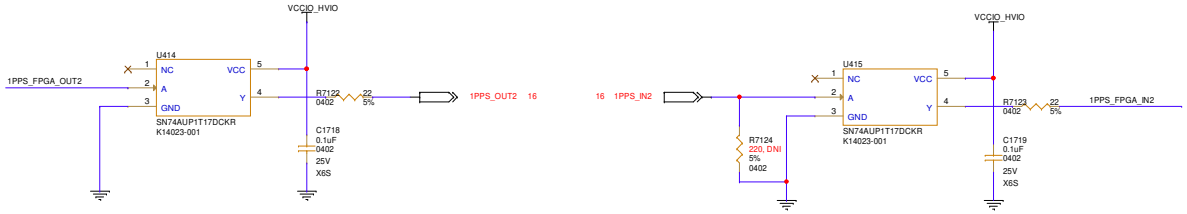
HVIO BANKS 5A AND 5B



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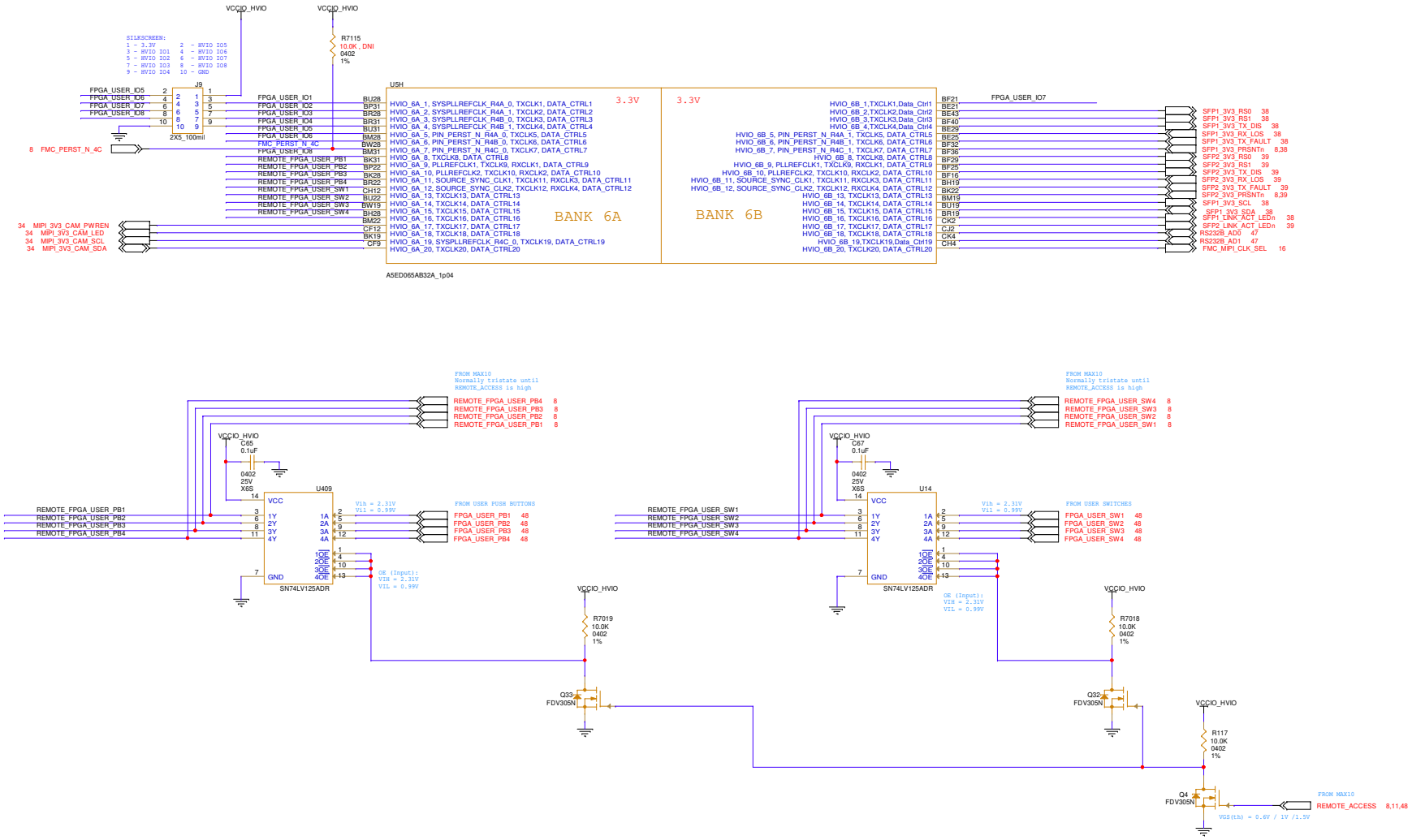
HVIO BANKS 6A AND 6B



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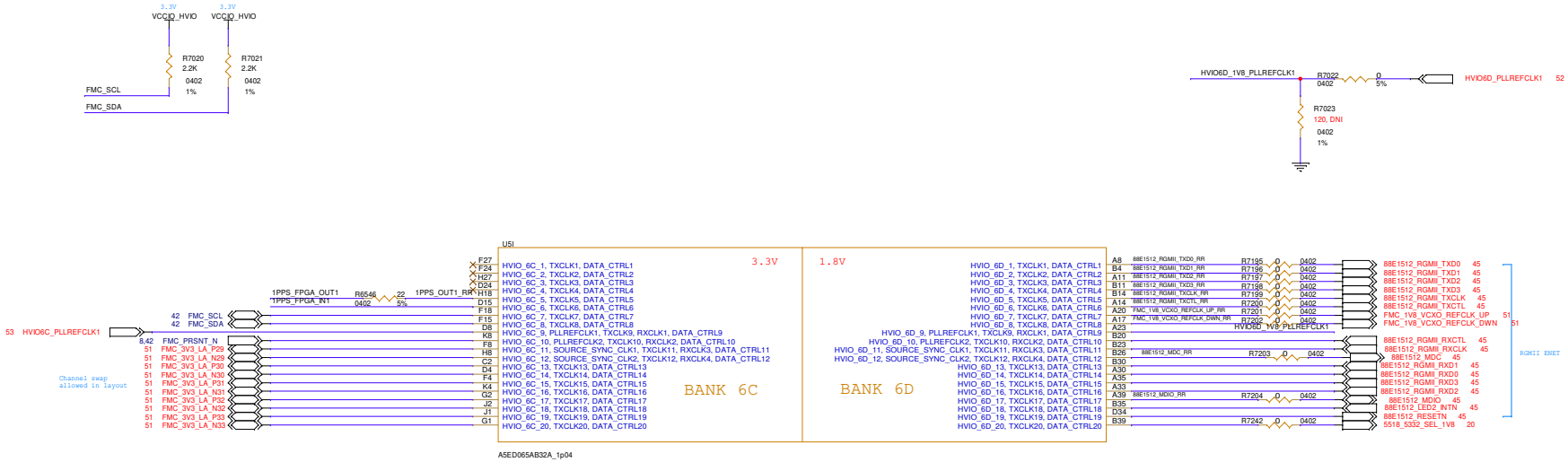
HVIO BANKS 6C AND 6D



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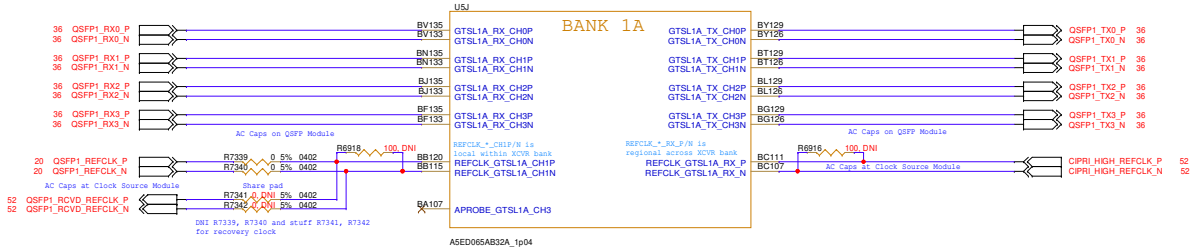
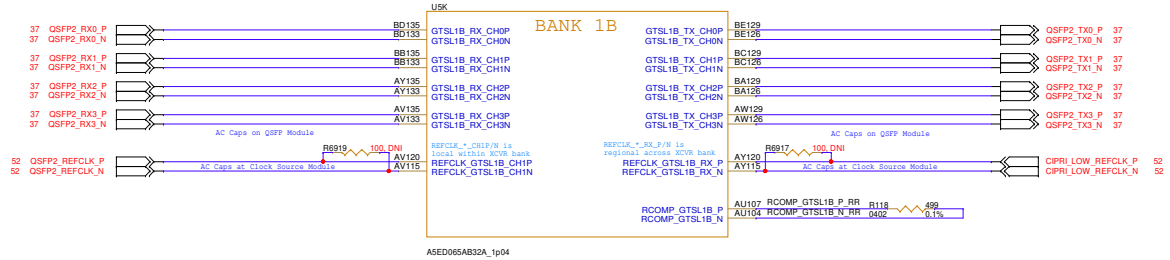
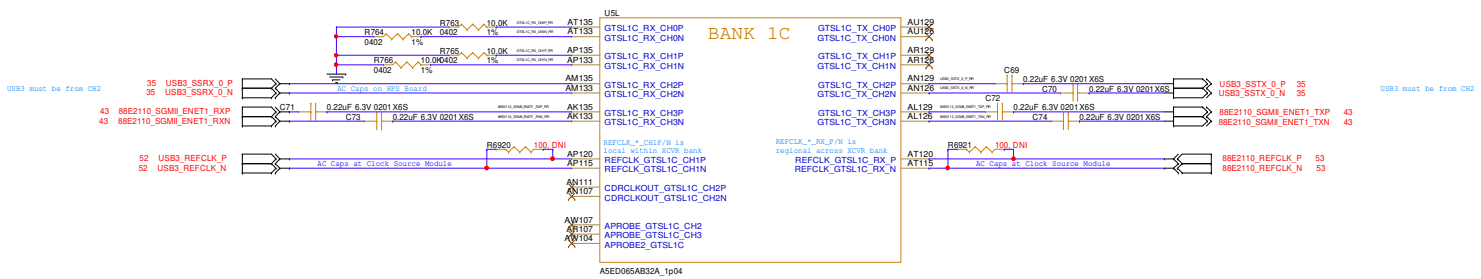
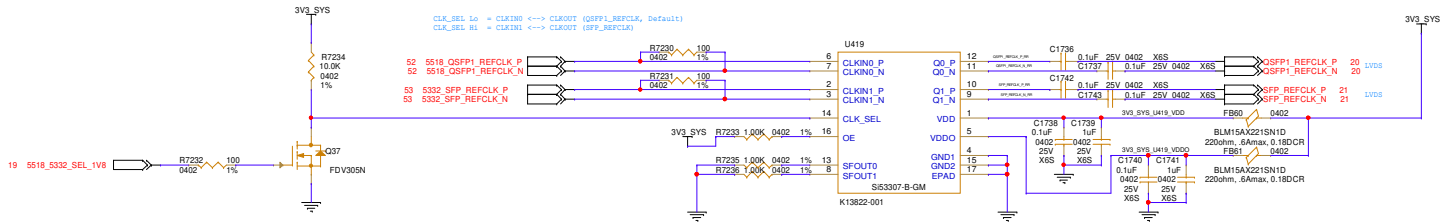
XCVR BANKS 1A, 1B, 1C









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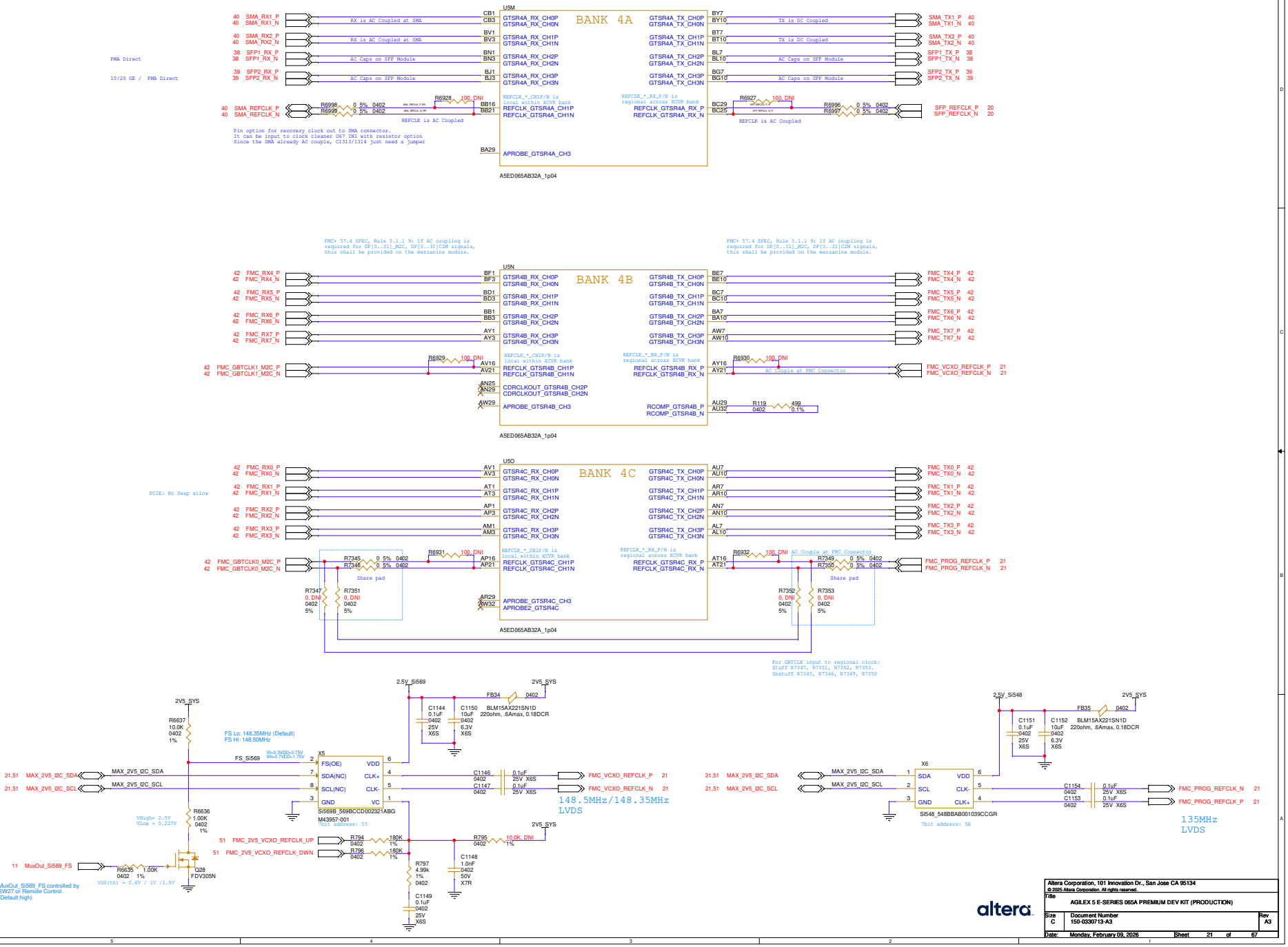
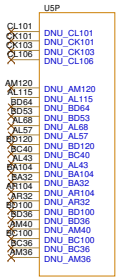
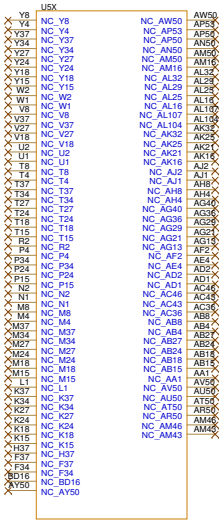
XCVR BANKS 4A, 4B, 4C



DNU & NC PINS





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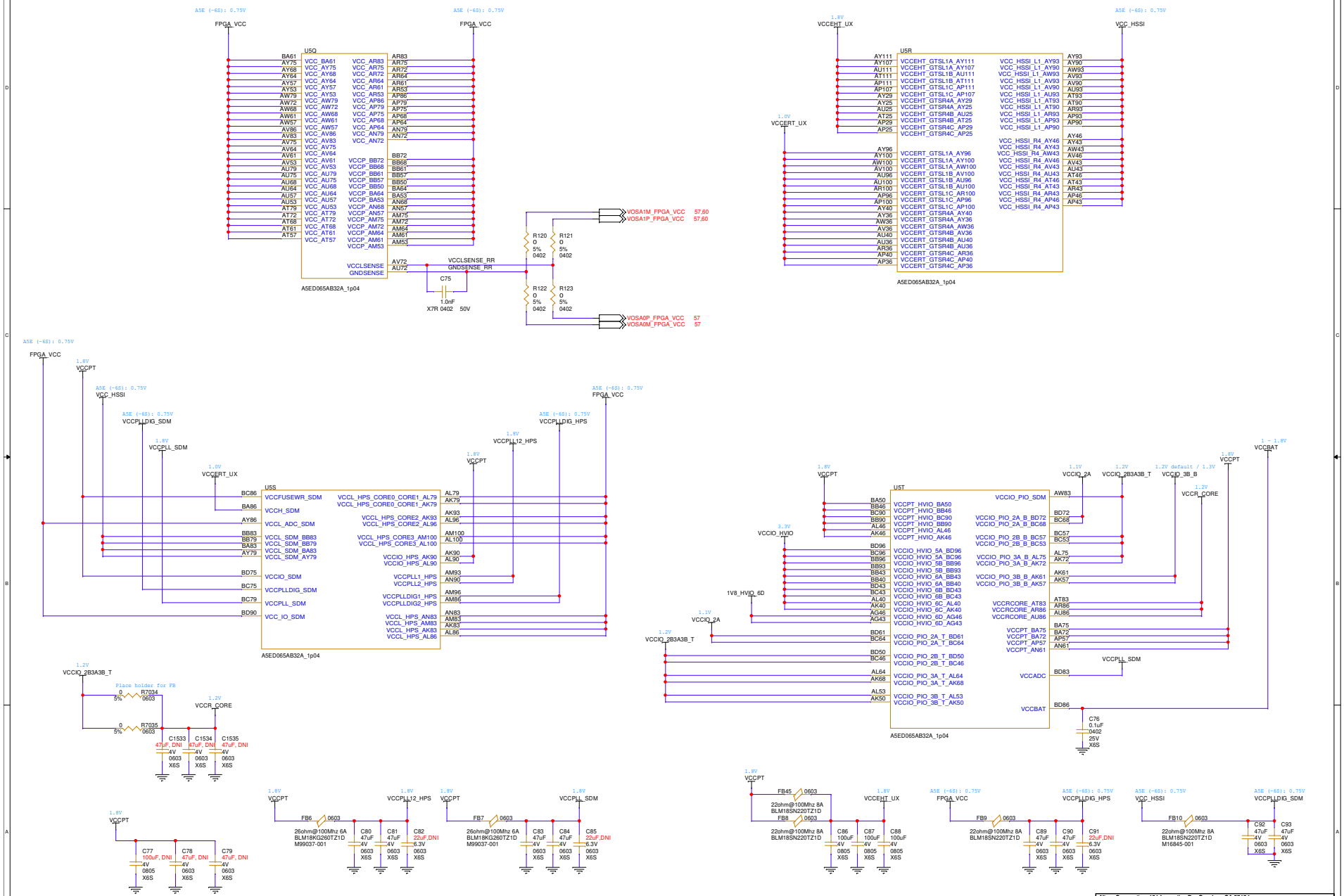
FPGA POWER



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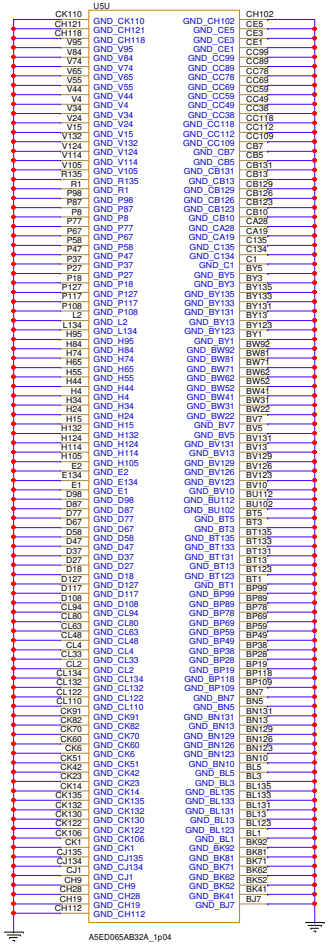
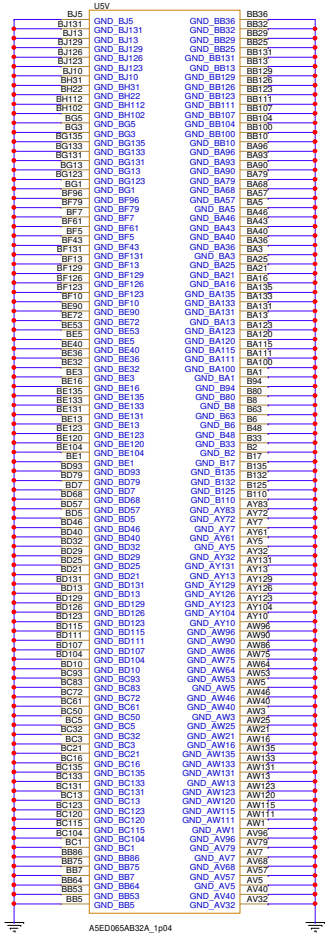
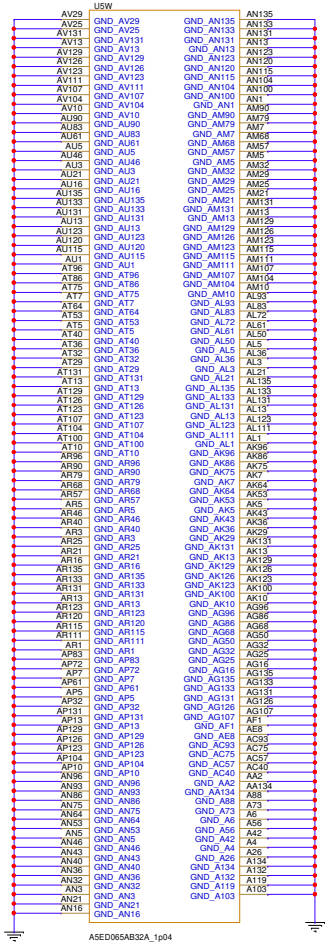
FPGA GND







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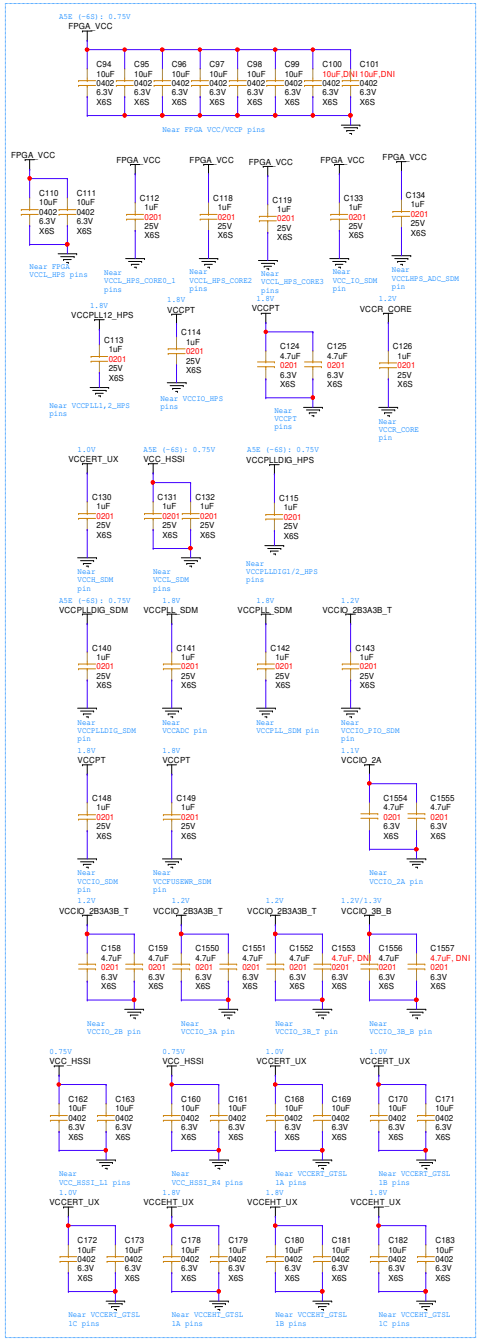
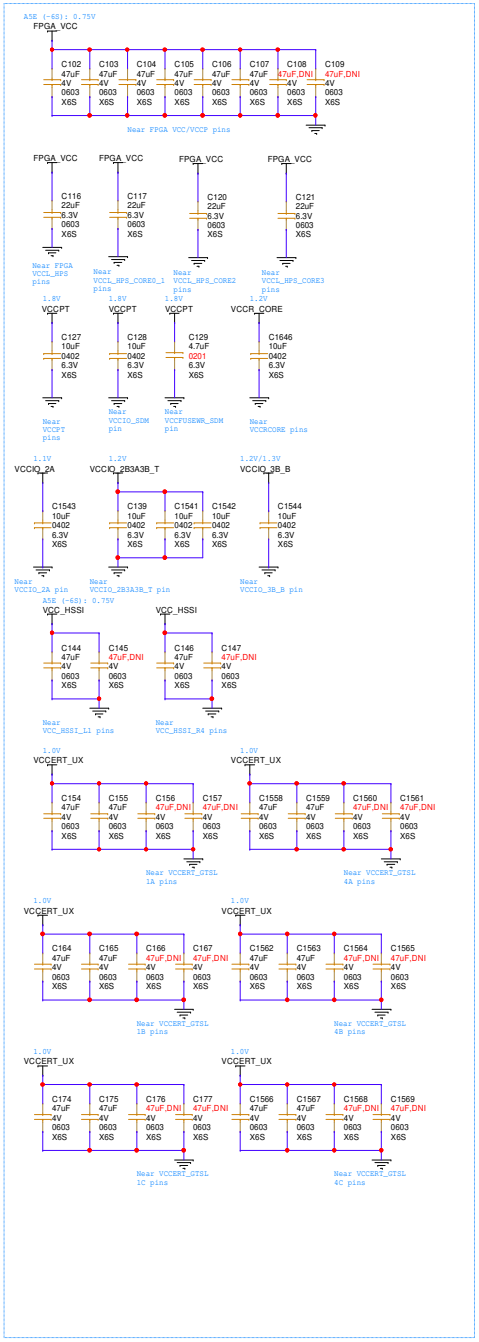
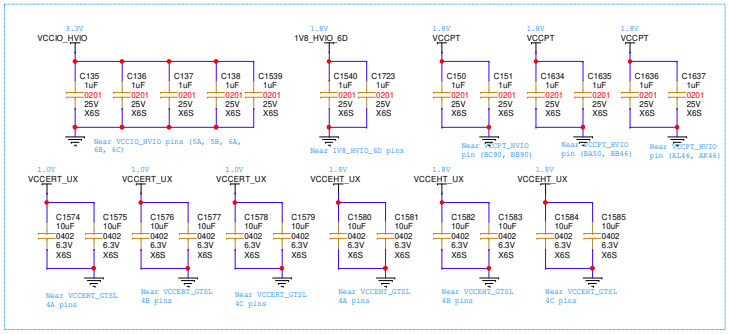
Place bottom FPGA cavity



Place top FPGA periphery



Place bottom FPGA cavity



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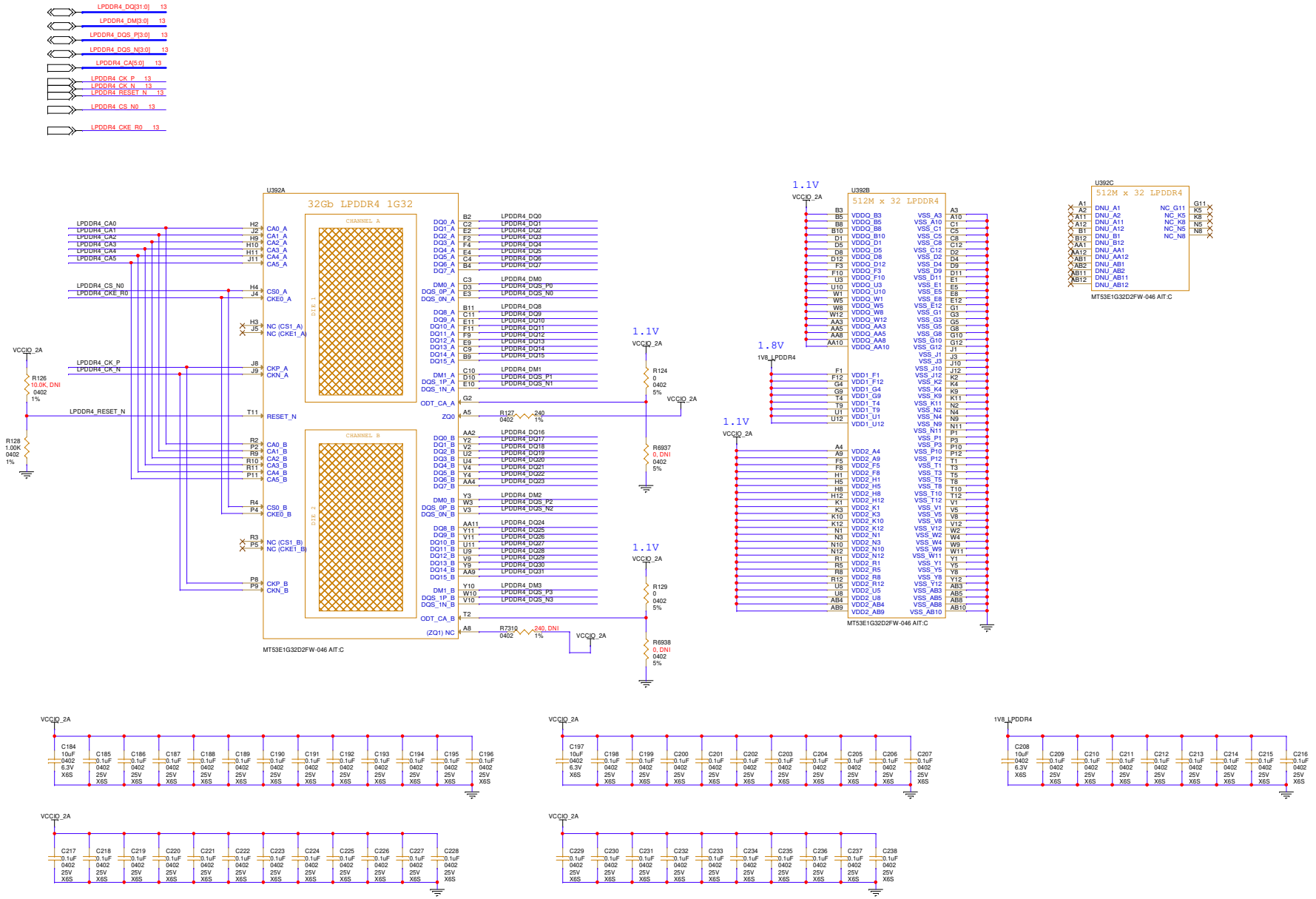
32-BIT LPDDR4



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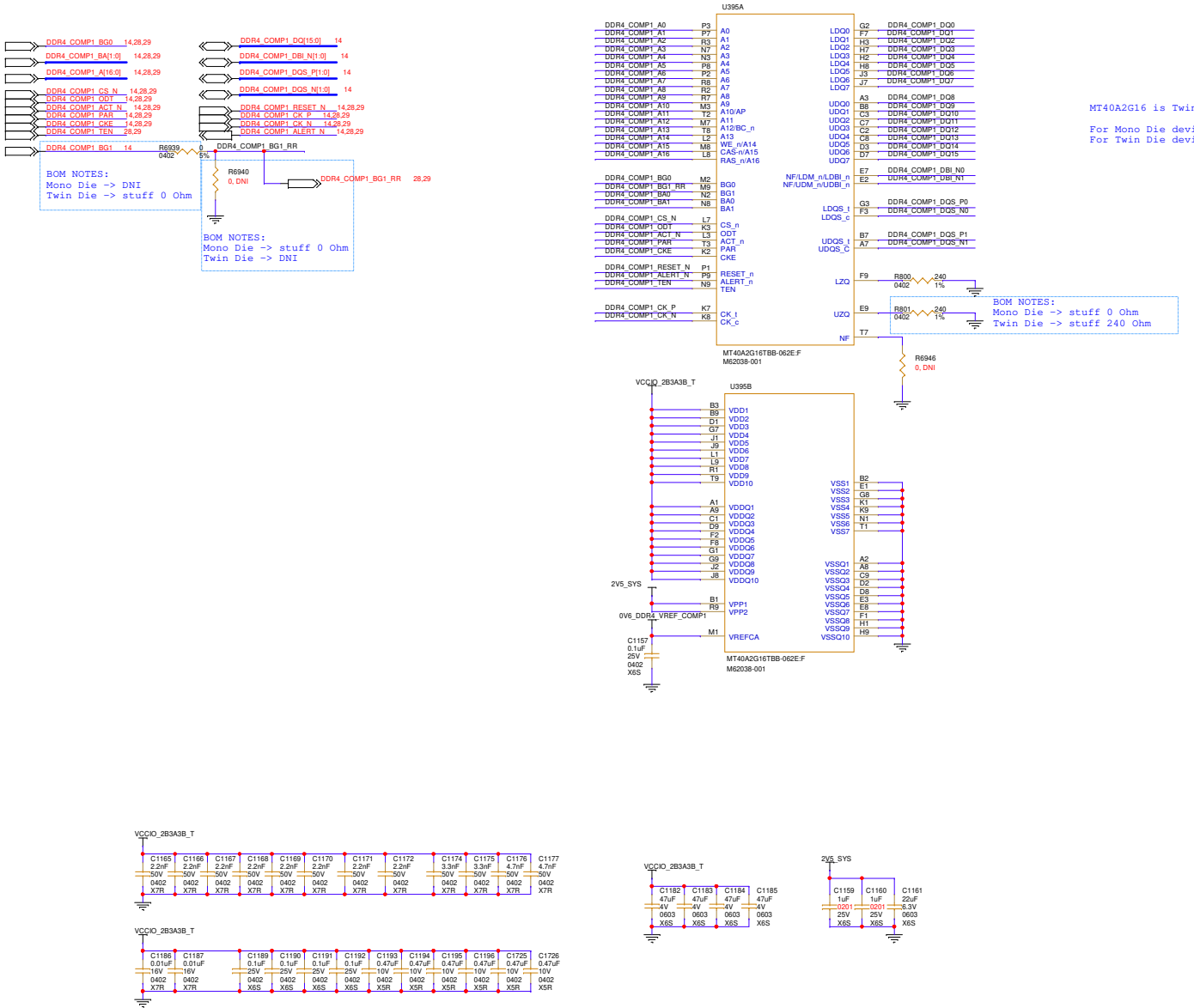
8GB DDR4 COMP1 BYTE 0-1



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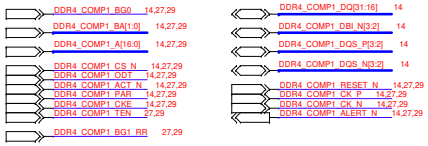
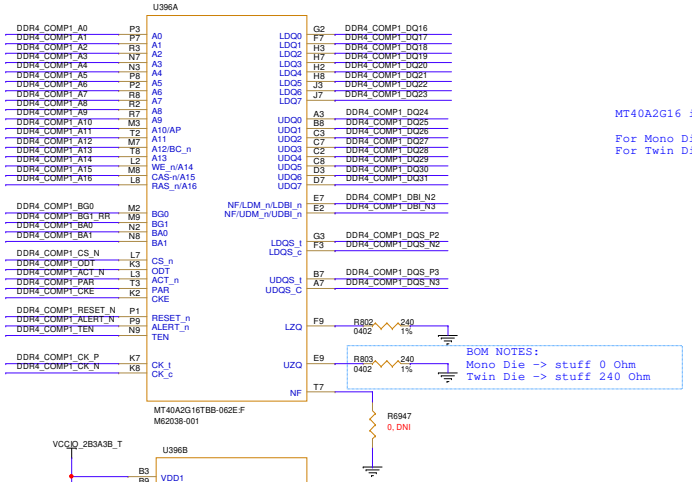
8GB DDR4 COMP1 BYTE 2-3

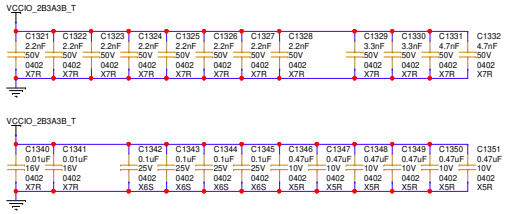


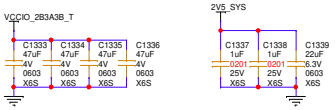


MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)

For Mono Die device, Pin E9 = GND; M9 = GND
For Twin Die device, Pin E9 = UZQ; M9 = BG1.

BOM NOTES:
Mono Die -> stuff 0 Ohm
Twin Die -> stuff 240 Ohm





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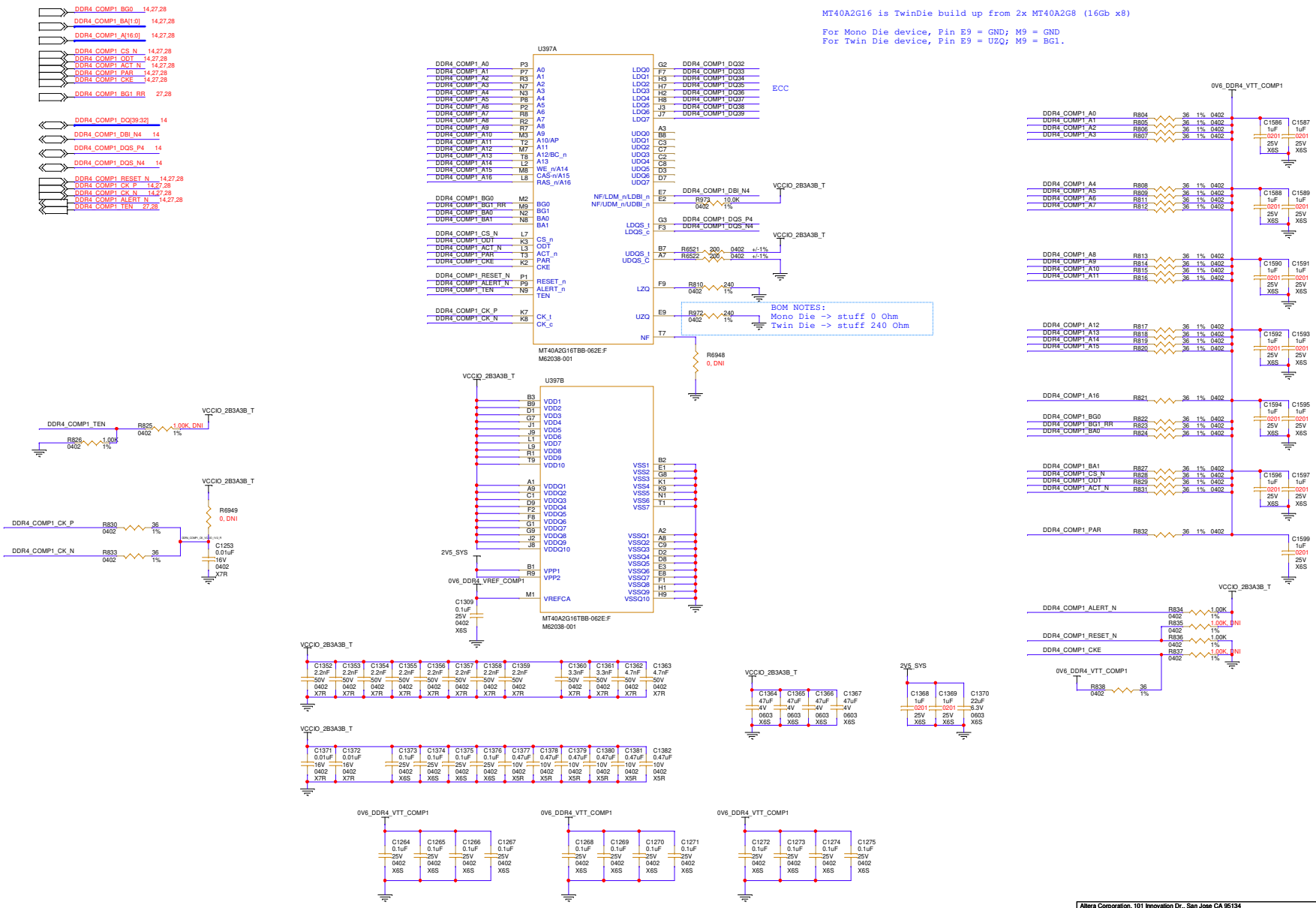
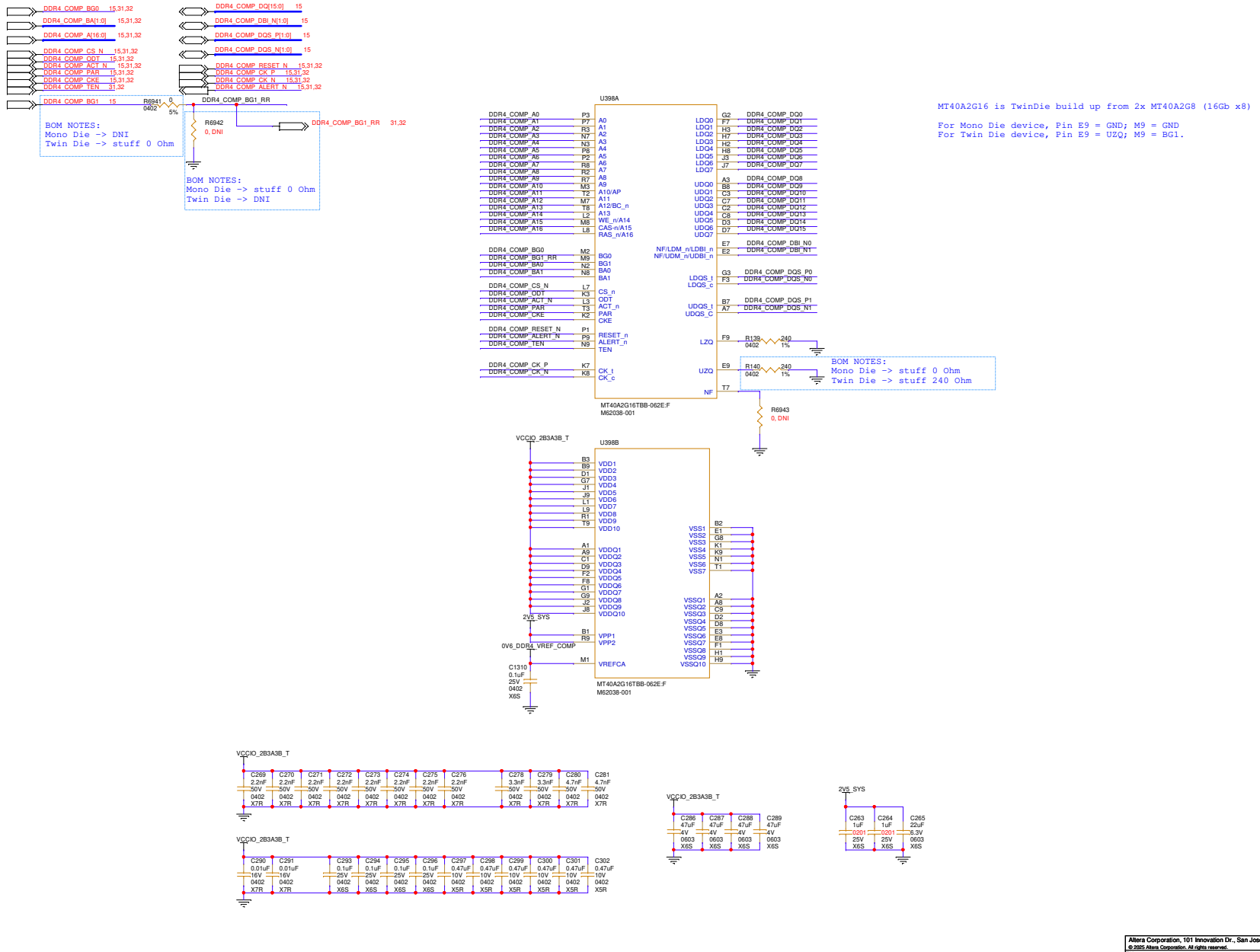
8GB DDR4 COMP1 BYTE ECC



HPS 8GB DDR4 COMPONENT BYTE 0-1



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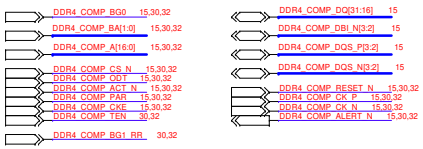
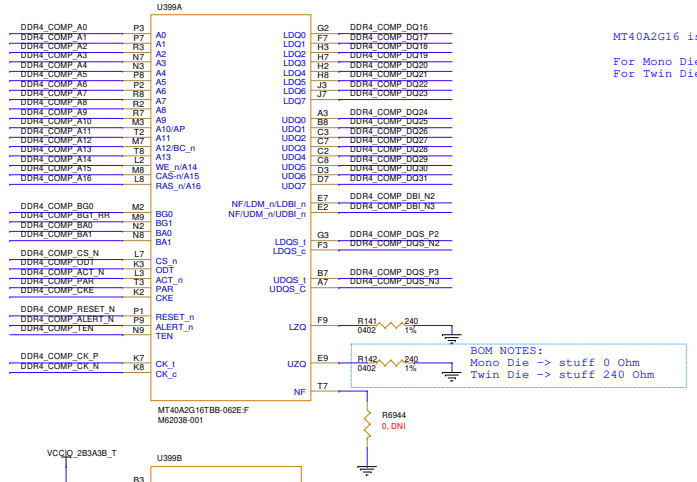
HPS 8GB DDR4 COMPONENT BYTE 2-3





MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)

For Mono Die device, Pin E9 = GND; M9 = GND
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BOM NOTES:
Mono Die -> stuff 0 Ohm
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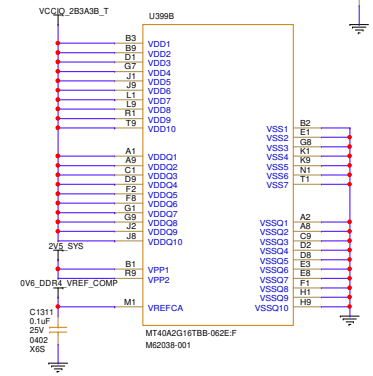

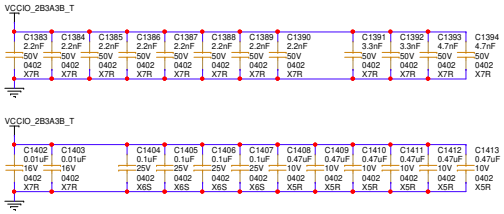

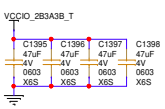

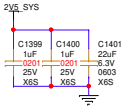

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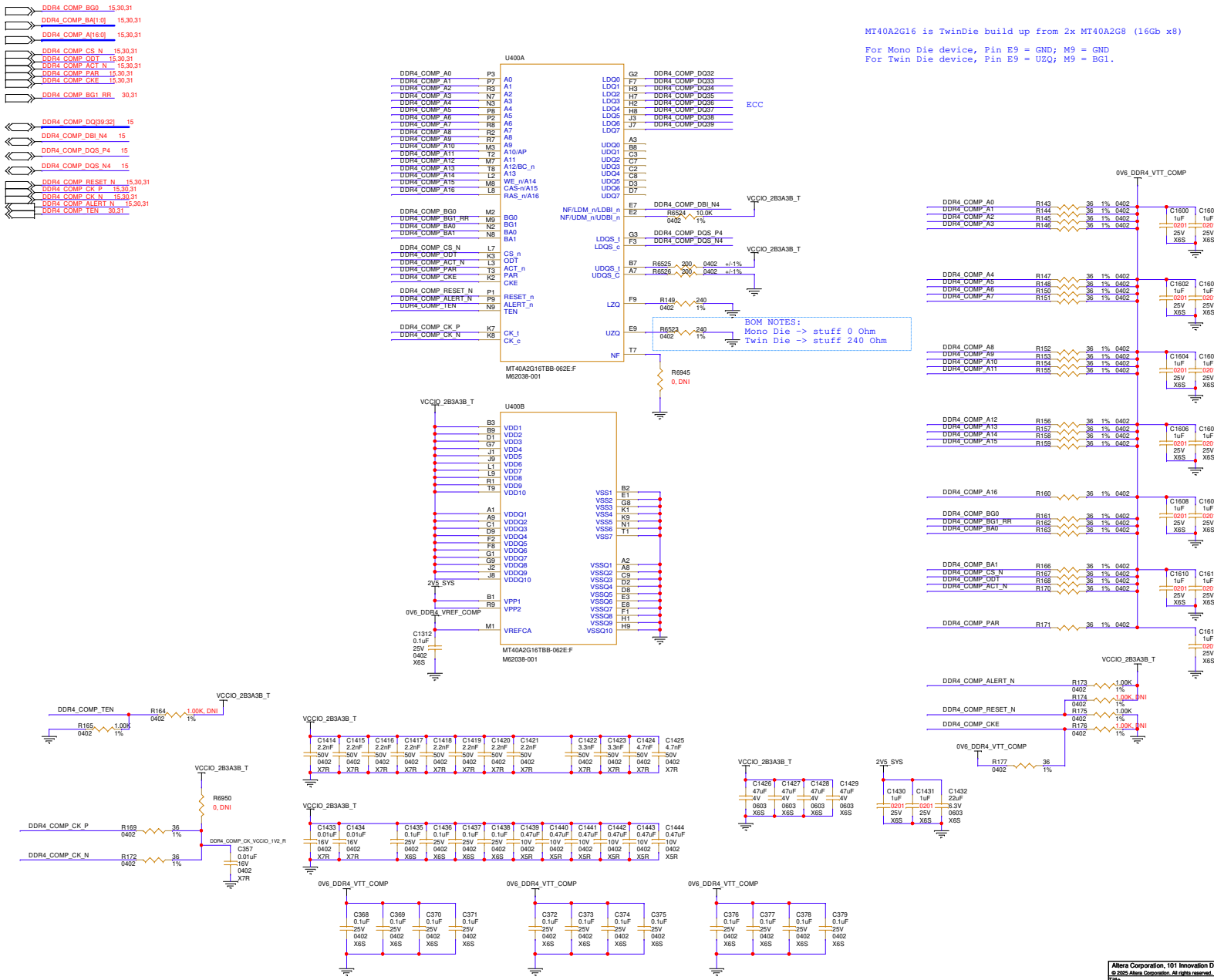
HPS 8GB DDR4 COMPONENT BYTE ECC



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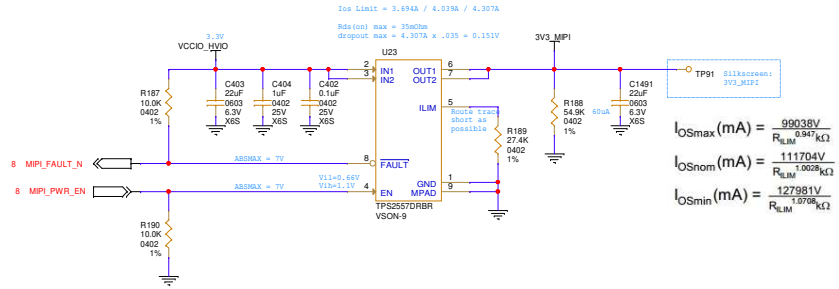
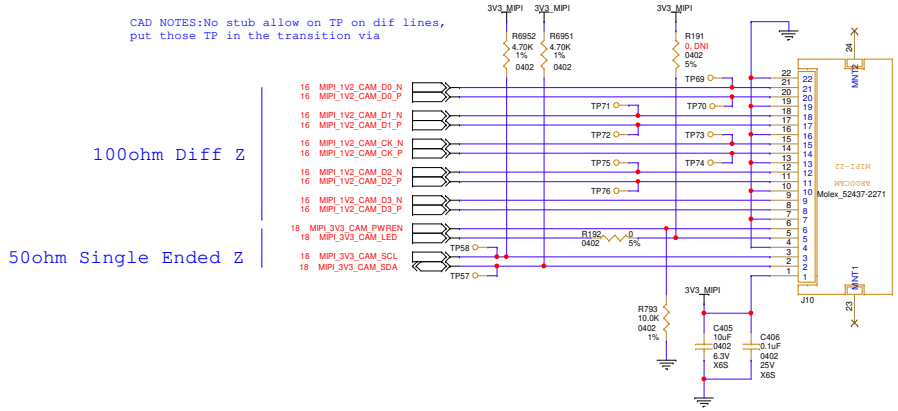


$$I_{OSmax}(mA) = \frac{99038V}{R_{ILIM}^{0.947}k\Omega}$$

$$I_{OSnom}(mA) = \frac{111704V}{R_{ILIM}^{1.0028}k\Omega}$$

$$I_{OSmin}(mA) = \frac{127981V}{R_{ILIM}^{1.0708}k\Omega}$$

CAD NOTES:No stub allow on TP on dif lines,
put those TP in the transition via



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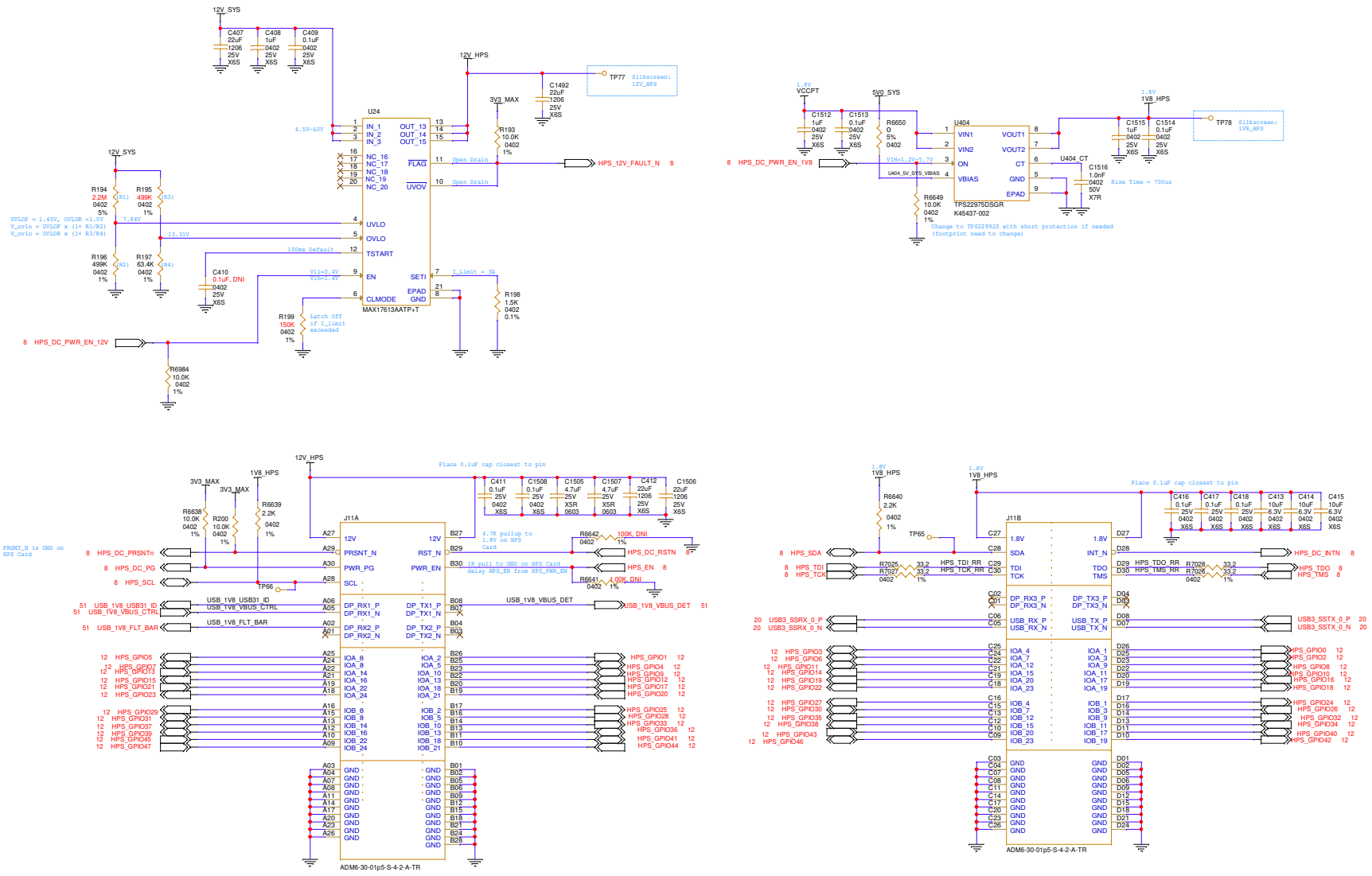

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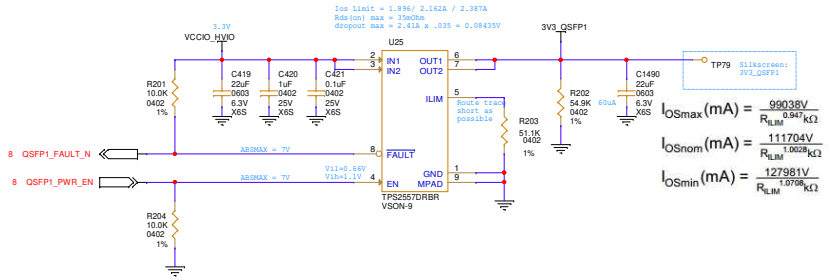
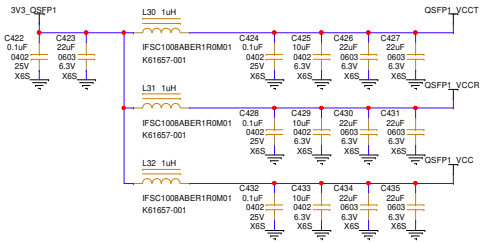


NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

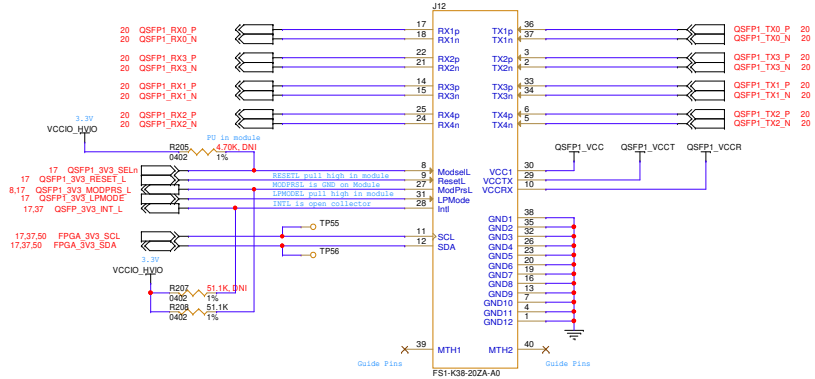
NOTE 2: QSFP 100-ohm termination is implemented via the FPGA on-chip termination.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

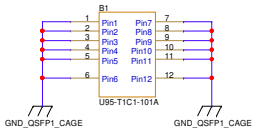
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



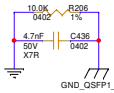
Place close to QSFP Connector

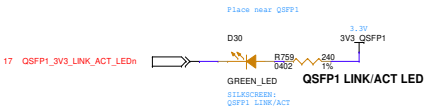


Amphenol FS1-K38-20ZA-A0



Amphenol U95-T1C1-101A





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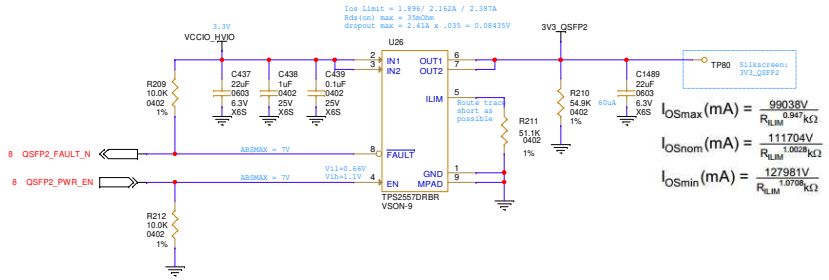

$$I_{OSmax}(mA) = \frac{99038V}{R_{ILIM}^{0.947}k\Omega}$$

$$I_{OSnom}(mA) = \frac{111704V}{R_{ILIM}^{1.0028}k\Omega}$$

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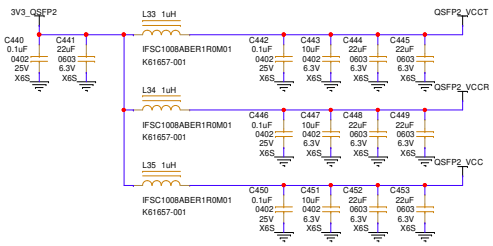
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

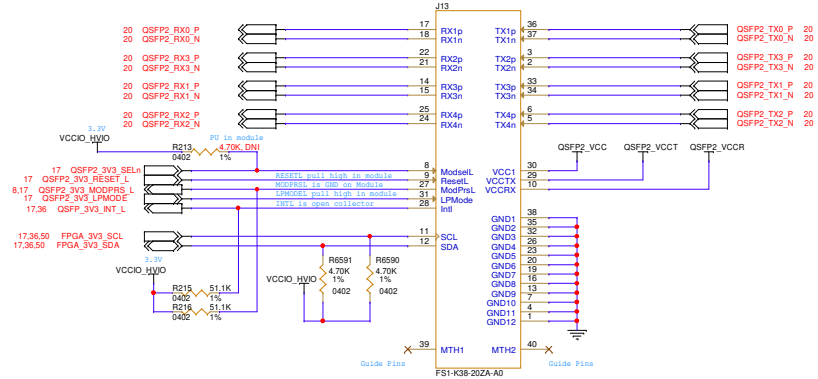
NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

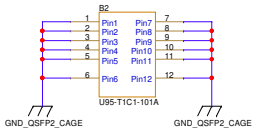
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



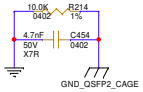
Place close to zQSFP Connector

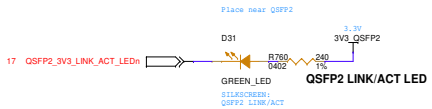


Amphenol FS1-K38-20ZA-A0



Amphenol U95-T1C1-101A





QSFP2 LINK/ACT LED

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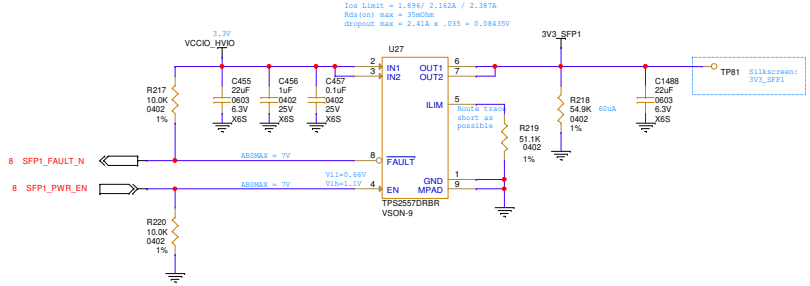
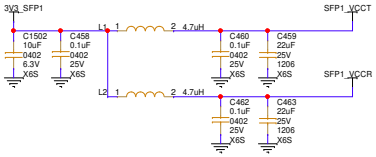
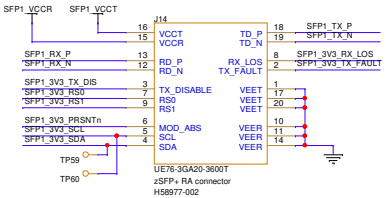


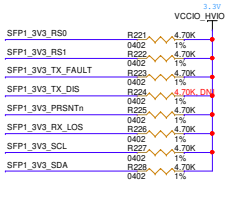
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

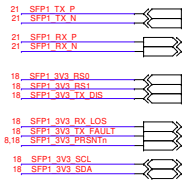
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

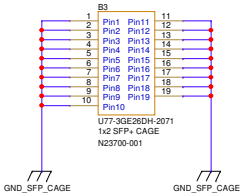
NOTE 3: DC blocking capacitors are in the module for RX and TX.







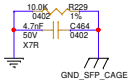


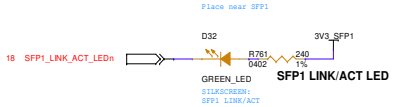


Optical (SFP+) Transceiver Cage 1x2

SFP modules have RS1 connected to GND.
If using SFP+ Rate Select pin are defined as:
RS1=0 -> TX datarates <= 4.25GB/s
RS1=1 -> TX datarates > 4.25GB/s

RS0=0 -> RX datarates <= 4.25GB/s
RS0=1 -> RX datarates > 4.25GB/s





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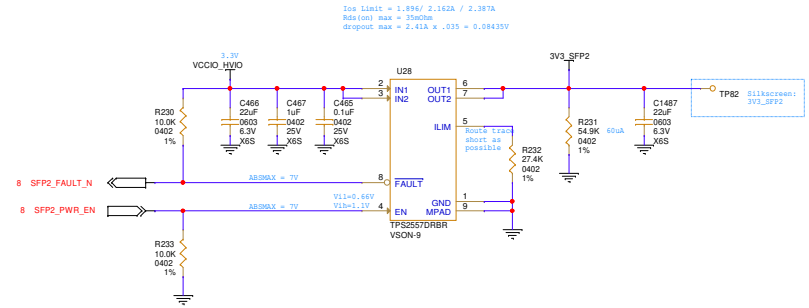
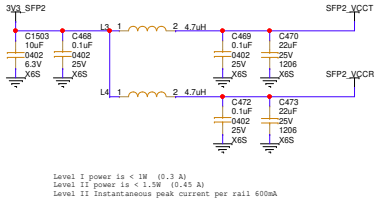
Size C	Document Number 150-0330713-A3	Rev A3
Date: Monday, February 09, 2026	Sheet 38 of 67	

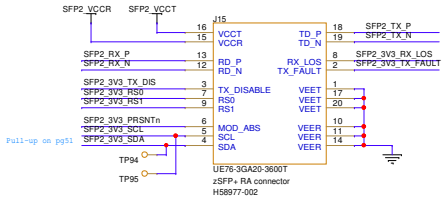


NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

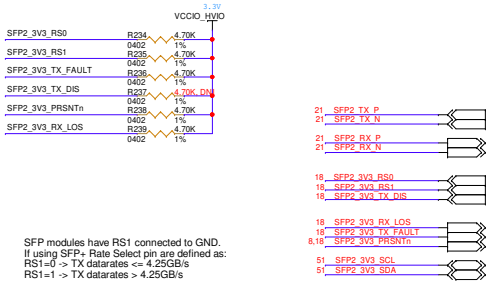
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

NOTE 3: DC blocking capacitors are in the module for RX and TX.



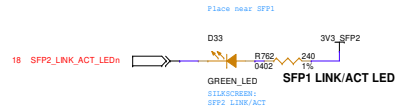


Optical (SFP+) Connector, case in page 38 B3



SFP modules have RS1 connected to GND.
If using SFP+ Rate Select pin are defined as:
RS1=0 -> TX datarates <= 4.25GB/s
RS1=1 -> TX datarates > 4.25GB/s

RS0=0 -> RX datarates <= 4.25GB/s
RS0=1 -> RX datarates > 4.25GB/s



SFP1 LINK/ACT LED

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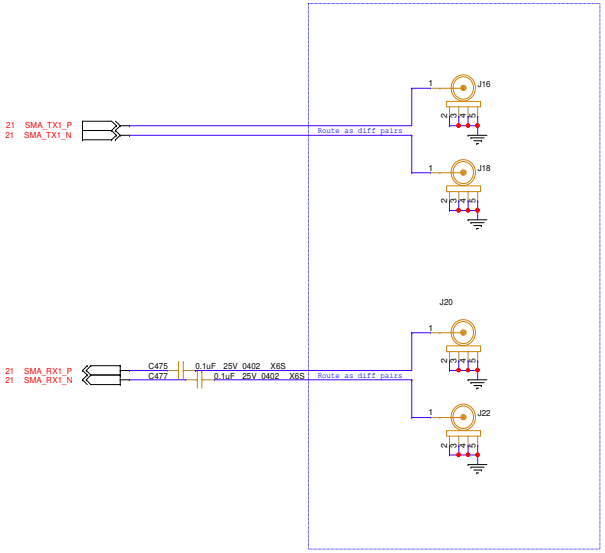
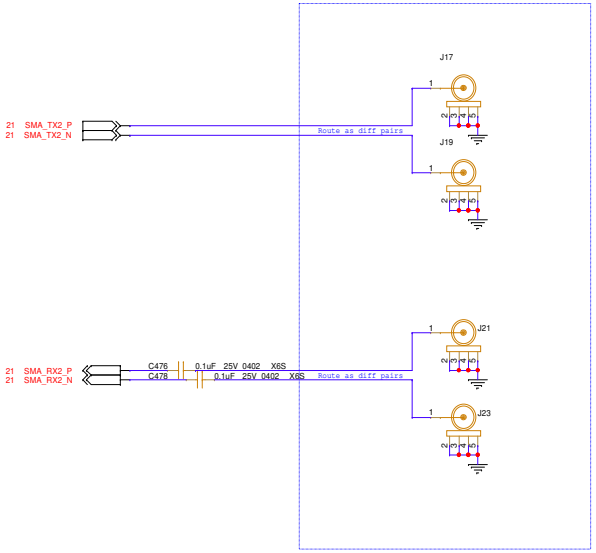
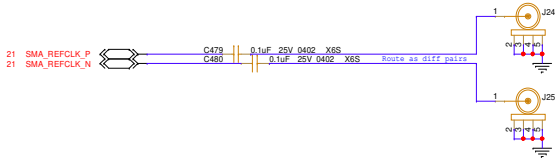
SMA TX/RX 1



SMA TX/RX 2



SMA XCVR REFCLK IN



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FMC+ Connector (Vita 57.4) Complete Pin Table

FMC Connector (Vita 57.1) Complete Pin Table

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

FMC+ Voltage Specification

Voltage Supply	Allowable Voltage Range	No Pins	Max Amps	Tolerance	Max Capacitive Load
VADJ	0 – 3.3V	4	4	+/- 5%	1000 uF
VIO_B_M2C	0 – VADJ	2	1.15	+/- 5%	500 uF
VREF_A_M2C	0 – VADJ	1	1mA	+/- 2%	10 uF
VREF_B_M2C	0 – VIO_B_M2C	1	1mA	+/- 2%	10 uF
3P3VAUX	3.3V	1	20mA	+/- 5%	150 uF
3P3V	3.3V	5	3	+/- 5%	1000 uF
12P0V	12V	5	1	+/- 5%	1000 uF

Supported FMC Cards:

1. FMC+ PCIe Gen4 x16 RootPort Card (HighTech Global)
** Note: Only support PCIe Gen4 x4 **
2. FMC+ HDMI 2.1 Card Rev9 (Bitec)
3. FMC+ DP 1.4 Rev12 (Bitec)

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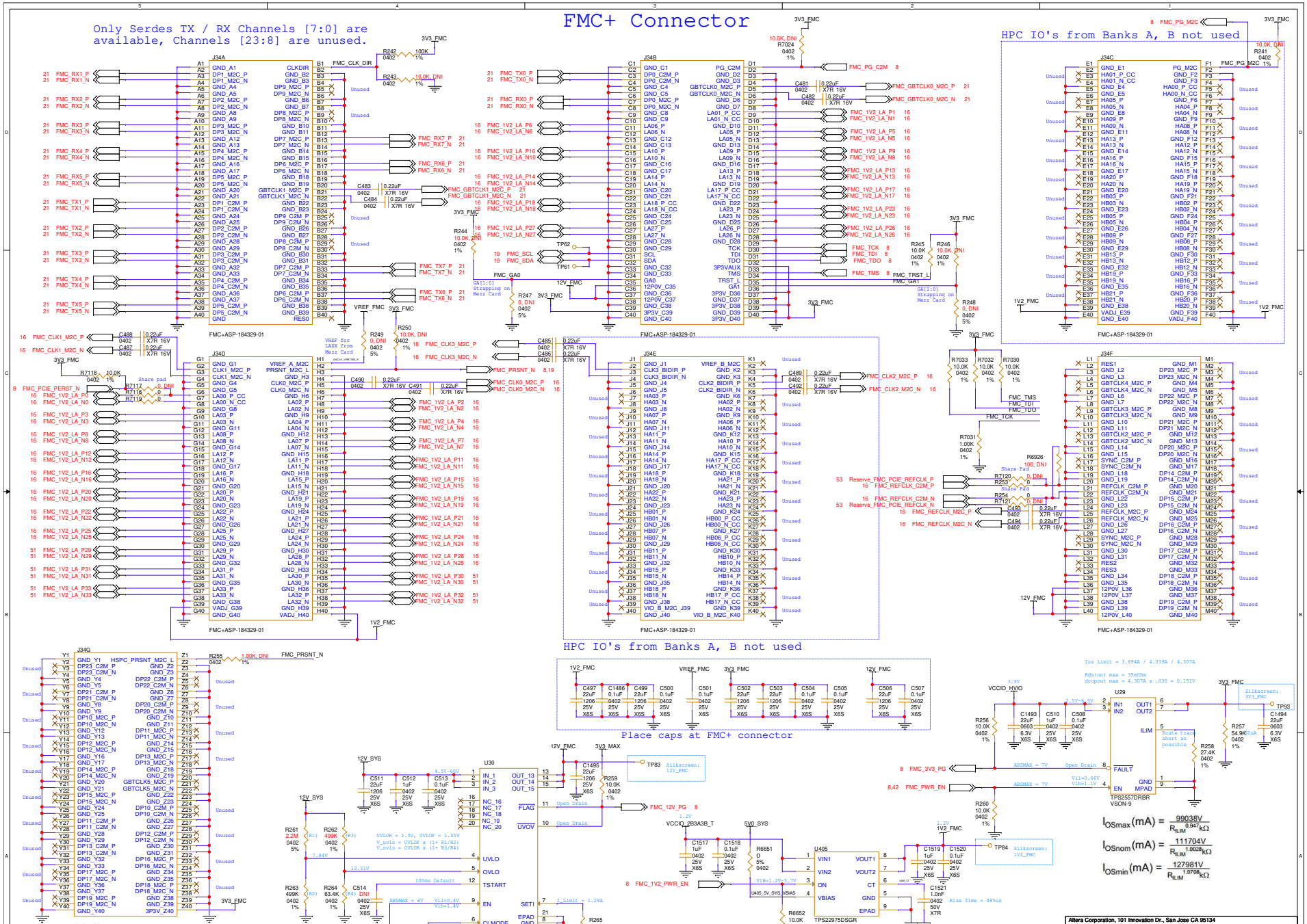
FMC+ Connector

Only Serdes TX / RX Channels [7:0] are available, Channels [23:8] are unused.



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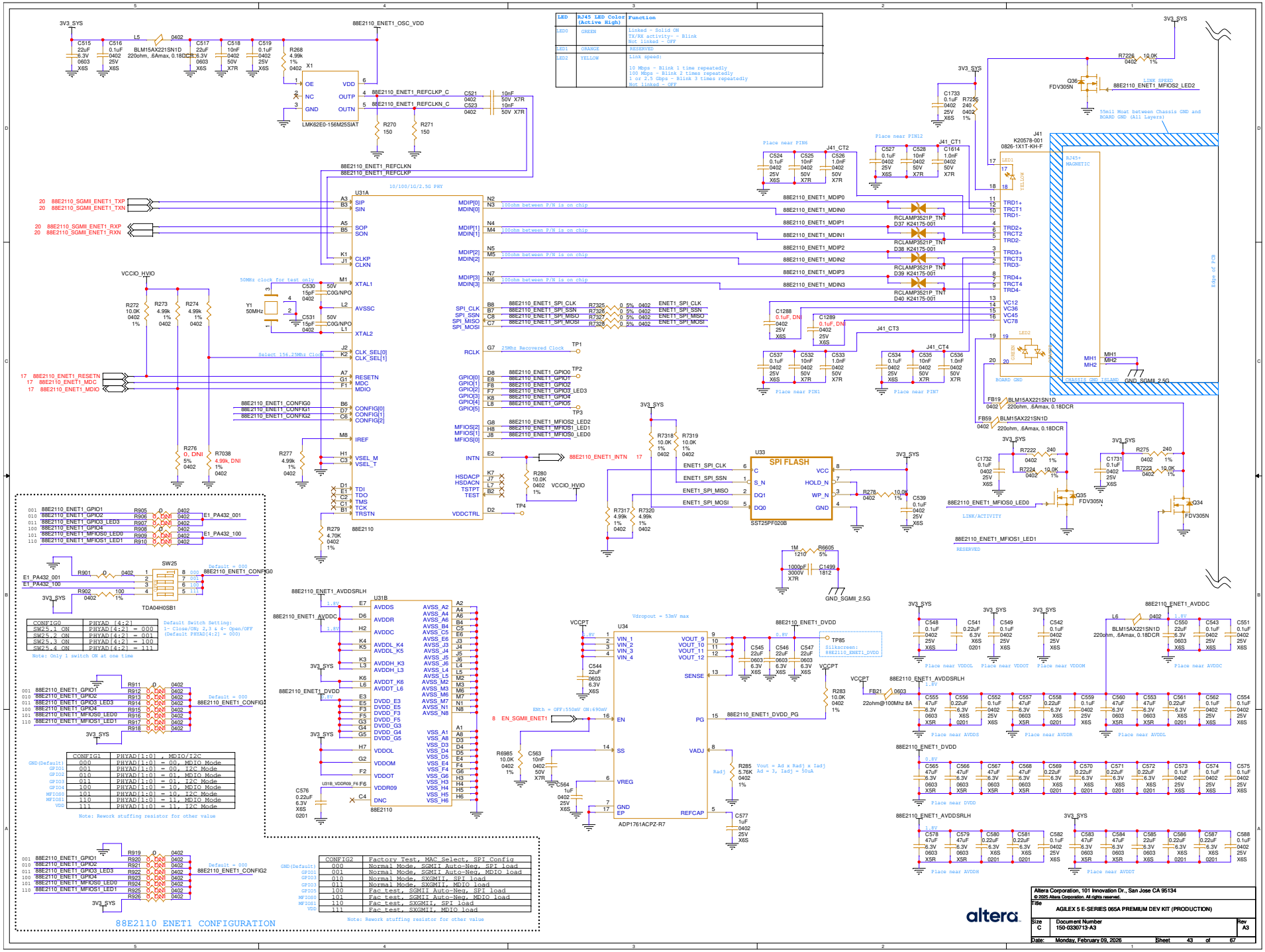
88E2110 ENET1 CONFIGURATION
U31A
U31B
U33
SPI FLASH
SST25PF020B
U34
ADP1761ACPZ-R7
LMK82E0-156M25SIAT
BLM15AX221SN1D
220ohm, .6Amax, 0.18DCR
RCLAMP3521P_TNT
K24175-001
K20578-001
0826-1X1T-KH-F
RJ45+ MAGNETIC
Edge of PCB
BOARD GND
CHASSIS GND ISLAND
GND_SGMII_2.5G
55mil Moat between Chassis GND and BOARD GND (All Layers)
10/100/1G/2.5G PHY
100ohm between P/N is on chip
50MHz clock for test only
Select 156.25Mhz Clock
25MHz Recovered Clock
Vdropout = 53mV max
ENth = OFF:550mV ON:690mV
Vout = Ad x Radj x Iadj
Ad = 3, Iadj = 50uA
Default Switch Setting:
1- Close/ON; 2,3 & 4- Open/OFF
(Default PHYAD[4:2] = 000)
Note: Only 1 switch ON at one time
Note: Rework stuffing resistor for other value
Factory Test, MAC Select, SPI Config
Normal Mode, SGMII Auto-Neg, SPI load
Normal Mode, SGMII Auto-Neg, MDIO load
Normal Mode, SXGMII, SPI load
Normal Mode, SXGMII, MDIO load
Fac test, SGMII Auto-Neg, SPI load
Fac test, SGMII Auto-Neg, MDIO load
Fac test, SXGMII, SPI load
Fac test, SXGMII, MDIO load
LINK SPEED
LINK/ACTIVITY
RESERVED
Place near VDDOL
Place near VDDOT
Place near VDDOM
Place near AVDDC
Place near AVDDS
Place near AVDDR
Place near AVDDL
Place near DVDD
Place near AVDDH
Place near AVDDT
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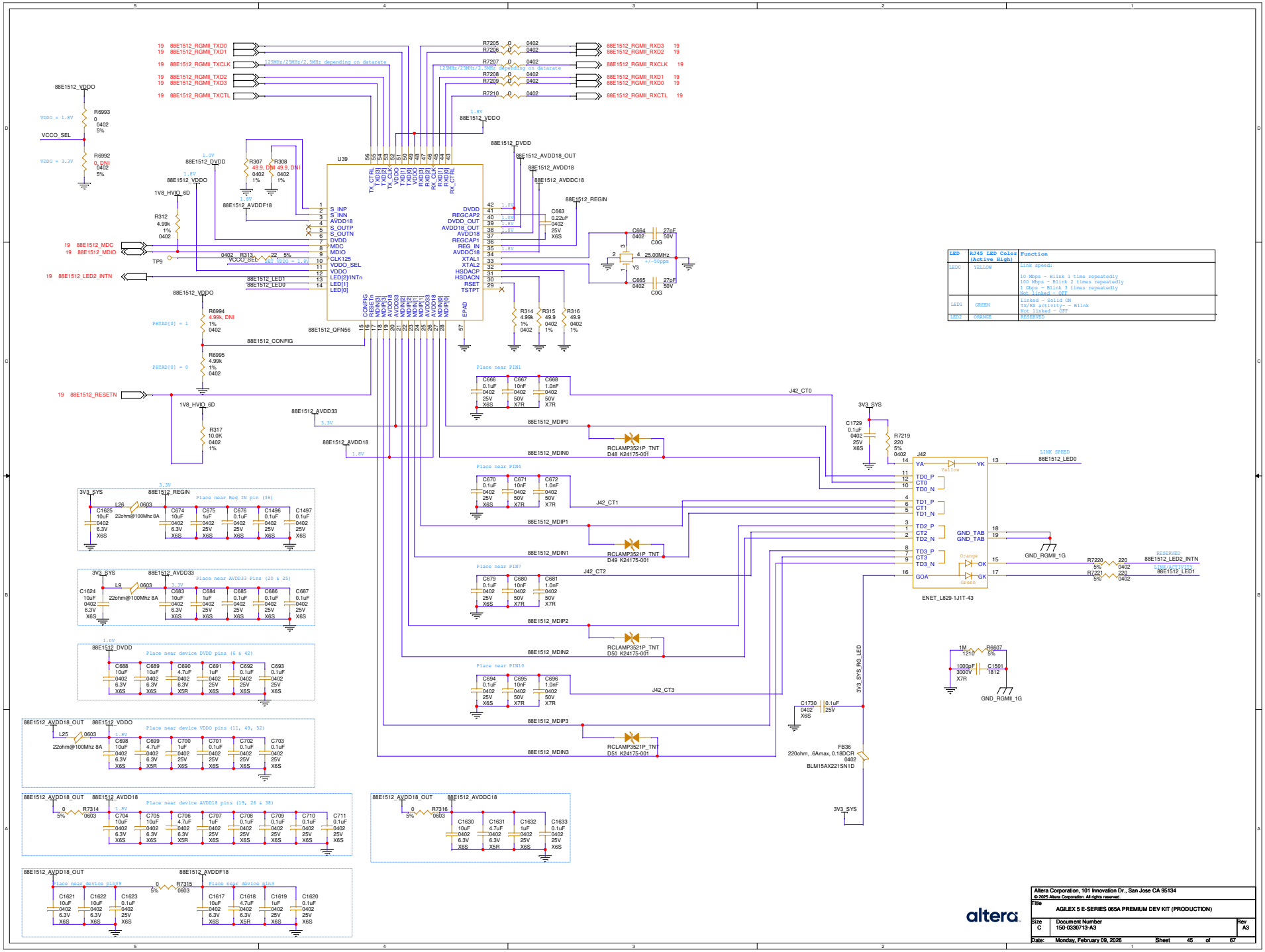

LED	RJ45 LED Color (Active High)	Function
LED0	YELLOW	Link speed: 10 Mbps - Blink 1 time repeatedly 100 Mbps - Blink 2 times repeatedly 1 Gbps - Blink 3 times repeatedly Not linked - OFF
LED1	GREEN	Linked - Solid ON TX/RX activity- - Blink Not linked - OFF
LED2	ORANGE	RESERVED

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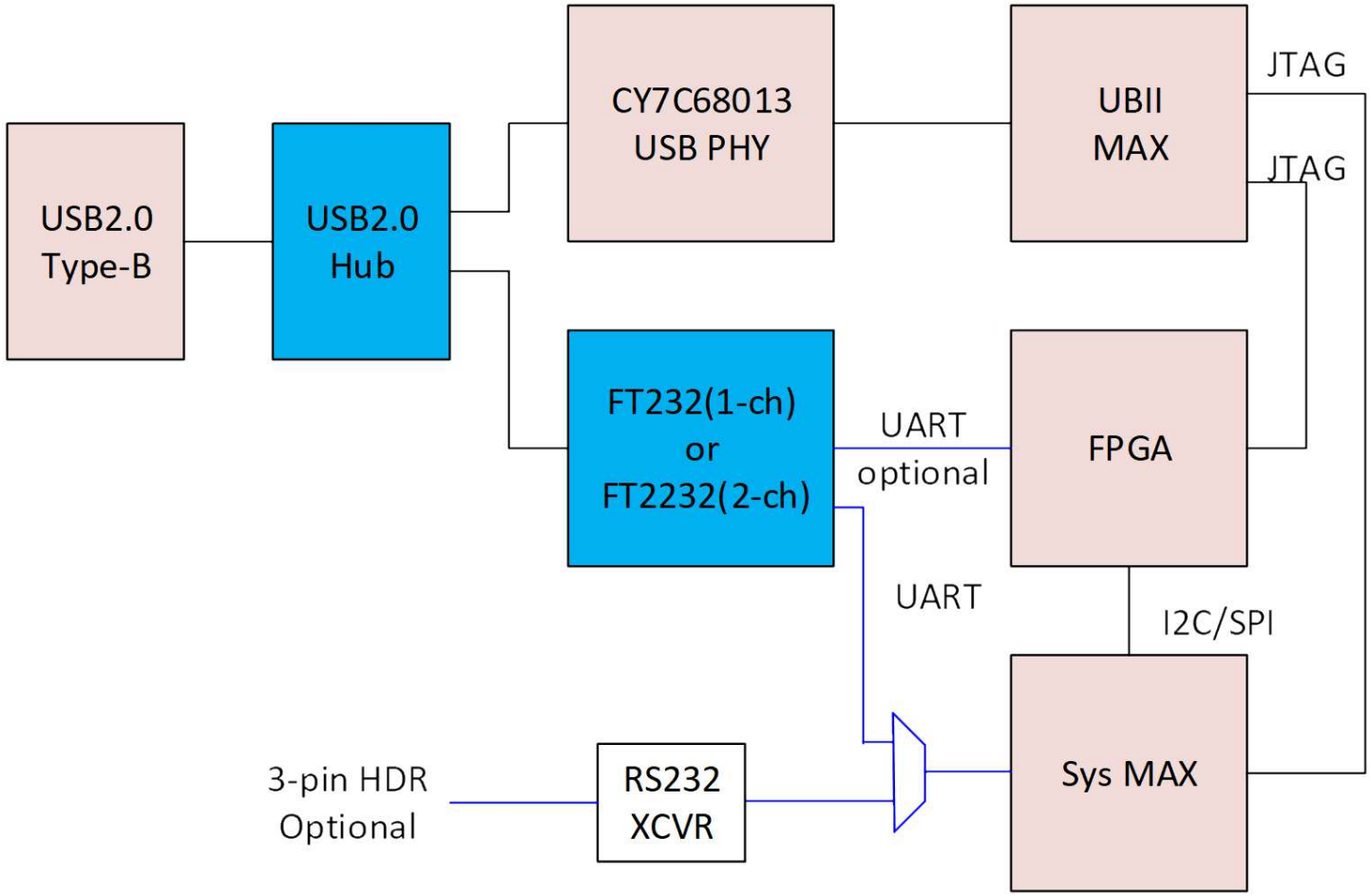

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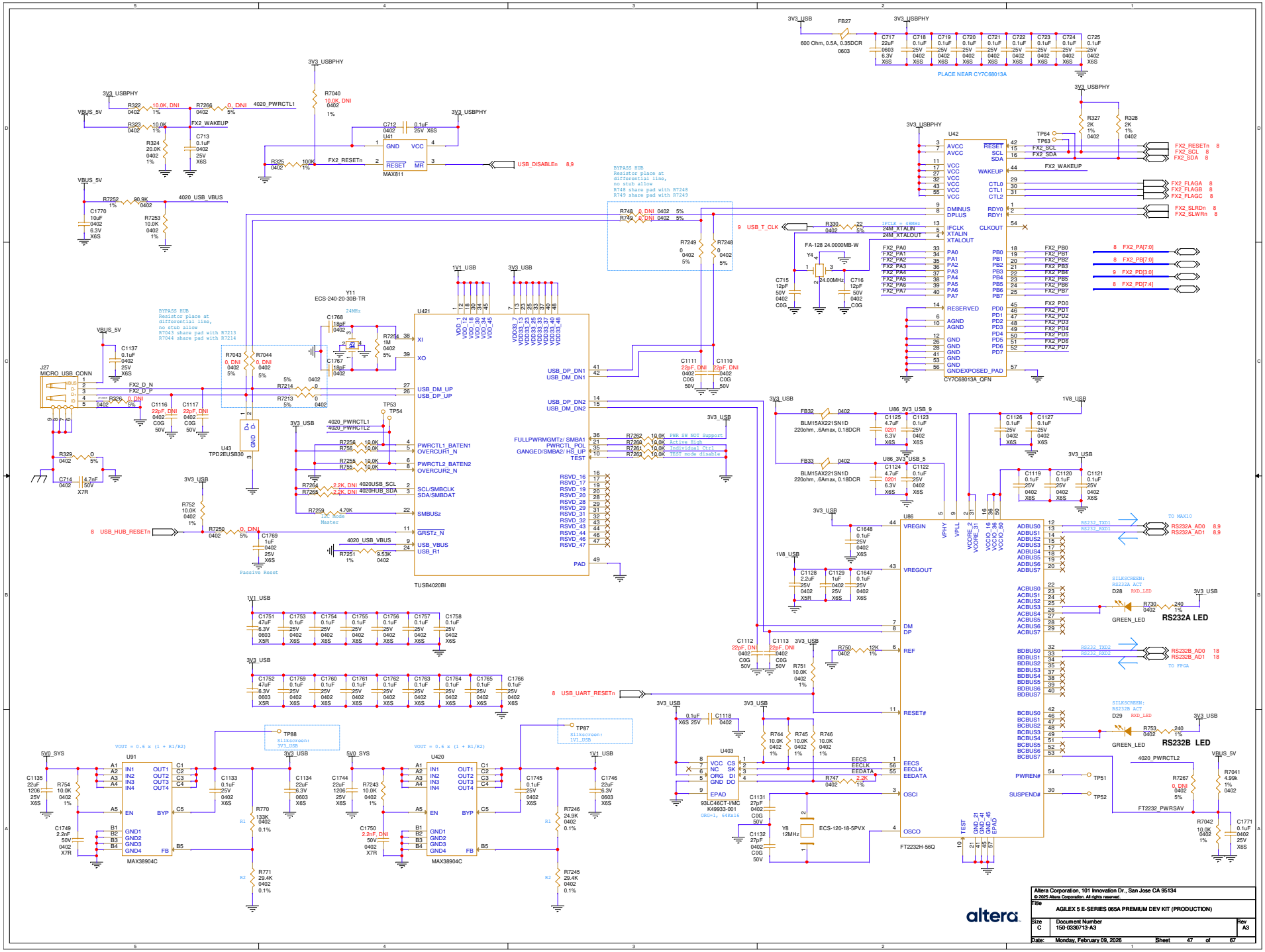
U42
CY7C68013A_QFN
U421
TUSB4020BI
U86
FT2232H-56Q
U91
MAX38904C
U420
MAX38904C
U41
MAX811
U43
TPD2EUSB30
J27
MICRO_USB_CONN
Y11
ECS-240-20-30B-TR
Y4
FA-128 24.0000MB-W
Y8
ECS-120-18-5PVX
U403
93LC46CT-I/MC
K49933-001
RS232A LED
RS232B LED
PLACE NEAR CY7C68013A
BYPASS HUB
Resistor place at differential line, no stub allow
R748 share pad with R7248
R749 share pad with R7249
R7043 share pad with R7213
R7044 share pad with R7214
Passive Reset
VOUT = 0.6 x (1 + R1/R2)
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Title
AGILEX 5 E-SERIES 065A PREMIUM DEV KIT (PROCTION)
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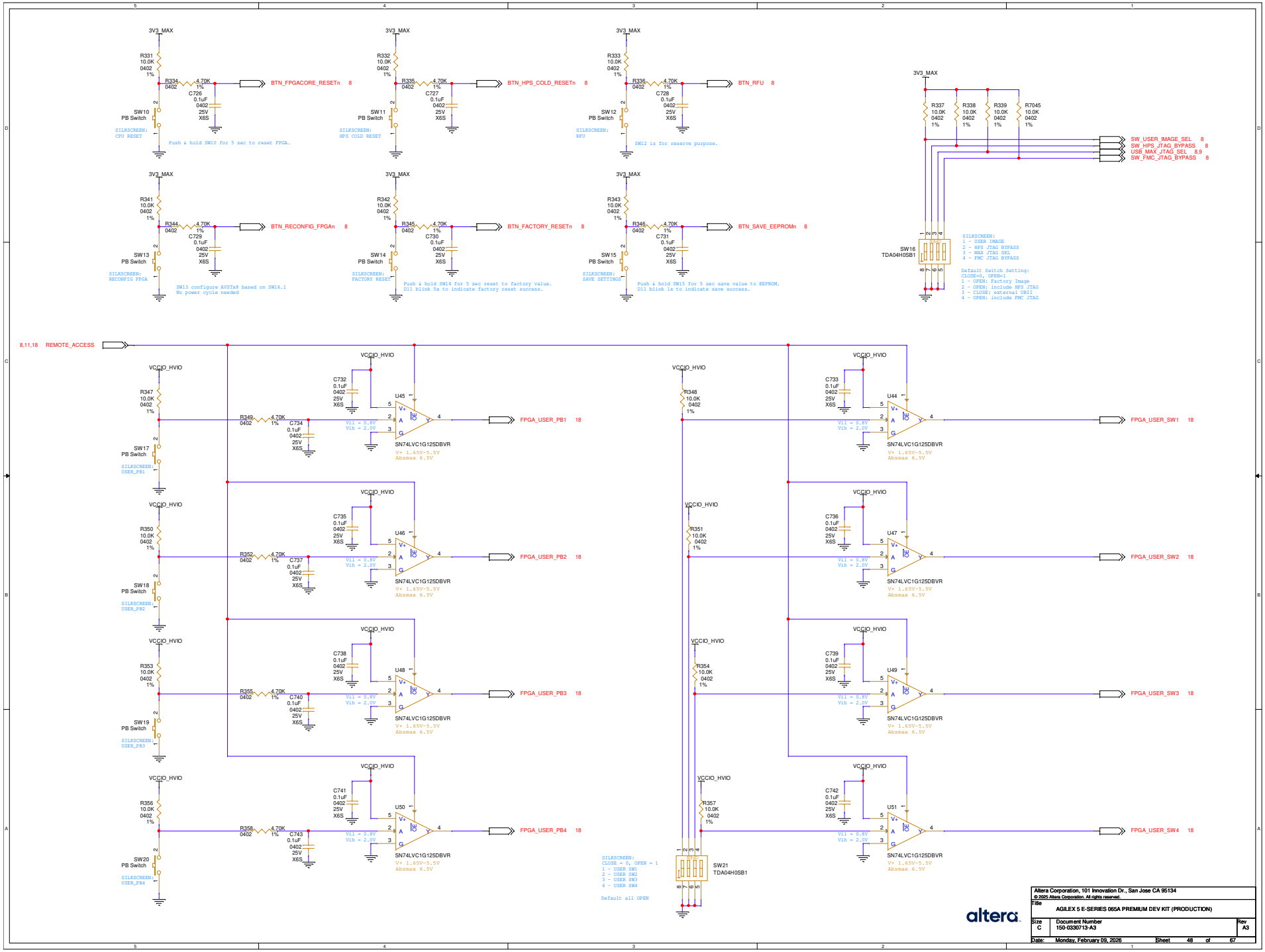
3V3_MAX
R331 10.0K 0402 1%
R334 0402 4.70K 1%
C726 0.1uF 0402 25V X6S
SW10 PB Switch
SILKSCREEN: CPU RESET
Push & hold SW10 for 5 sec to reset FPGA.
BTN_FPGACORE_RESETn 8
R332 10.0K 0402 1%
R335 0402 4.70K 1%
C727 0.1uF 0402 25V X6S
SW11 PB Switch
SILKSCREEN: HPS COLD RESET
BTN_HPS_COLD_RESETn 8
R333 10.0K 0402 1%
R336 0402 4.70K 1%
C728 0.1uF 0402 25V X6S
SW12 PB Switch
SILKSCREEN: RFU
SW12 is for reserve purpose.
BTN_RFU 8
R337 10.0K 0402 1%
R338 10.0K 0402 1%
R339 10.0K 0402 1%
R7045 10.0K 0402 1%
SW_USER_IMAGE_SEL 8
SW_HPS_JTAG_BYPASS 8
USB_MAX_JTAG_SEL 8,9
SW_FMC_JTAG_BYPASS 8
SW16 TDA04H0SB1
SILKSCREEN:
1 - USER IMAGE
2 - HPS JTAG BYPASS
3 - MAX JTAG SEL
4 - FMC JTAG BYPASS
Default Switch Setting:
CLOSE=0, OPEN=1
1 - OPEN: Factory Image
2 - OPEN: include HPS JTAG
3 - CLOSE: external UBII
4 - OPEN: include FMC JTAG
R341 10.0K 0402 1%
R344 0402 4.70K 1%
C729 0.1uF 0402 25V X6S
SW13 PB Switch
SILKSCREEN: RECONFIG FPGA
SW13 configure AVSTx8 based on SW16.1
No power cycle needed
BTN_RECONFIG_FPGAn 8
R342 10.0K 0402 1%
R345 0402 4.70K 1%
C730 0.1uF 0402 25V X6S
SW14 PB Switch
SILKSCREEN: FACTORY RESET
Push & hold SW14 for 5 sec reset to factory value.
D11 blink 5x to indicate factory reset success.
BTN_FACTORY_RESETn 8
R343 10.0K 0402 1%
R346 0402 4.70K 1%
C731 0.1uF 0402 25V X6S
SW15 PB Switch
SILKSCREEN: SAVE SETTINGS
Push & hold SW15 for 5 sec save value to EEPROM.
D11 blink 1x to indicate save success.
BTN_SAVE_EEPROMn 8
8,11,18 REMOTE_ACCESS
VCCIO_HVIO
R347 10.0K 0402 1%
R349 0402 4.70K 1%
C732 0.1uF 0402 25V X6S
C734 0.1uF 0402 25V X6S
U45
SW17 PB Switch
SILKSCREEN: USER_PB1
FPGA_USER_PB1 18
R350 10.0K 0402 1%
R352 0402 4.70K 1%
C735 0.1uF 0402 25V X6S
C737 0.1uF 0402 25V X6S
U46
SW18 PB Switch
SILKSCREEN: USER_PB2
FPGA_USER_PB2 18
R353 10.0K 0402 1%
R355 0402 4.70K 1%
C738 0.1uF 0402 25V X6S
C740 0.1uF 0402 25V X6S
U48
SW19 PB Switch
SILKSCREEN: USER_PB3
FPGA_USER_PB3 18
R356 10.0K 0402 1%
R358 0402 4.70K 1%
C741 0.1uF 0402 25V X6S
C743 0.1uF 0402 25V X6S
U50
SW20 PB Switch
SILKSCREEN: USER_PB4
FPGA_USER_PB4 18
Vil = 0.8V
Vih = 2.0V
SN74LVC1G125DBVR
V+ 1.65V-5.5V
Absmax 6.5V
R348 10.0K 0402 1%
C733 0.1uF 0402 25V X6S
U44
FPGA_USER_SW1 18
R351 10.0K 0402 1%
C736 0.1uF 0402 25V X6S
U47
FPGA_USER_SW2 18
R354 10.0K 0402 1%
C739 0.1uF 0402 25V X6S
U49
FPGA_USER_SW3 18
R357 10.0K 0402 1%
C742 0.1uF 0402 25V X6S
U51
FPGA_USER_SW4 18
SW21 TDA04H0SB1
SILKSCREEN:
CLOSE = 0, OPEN = 1
1 - USER SW1
2 - USER SW2
3 - USER SW3
4 - USER SW4
Default all OPEN
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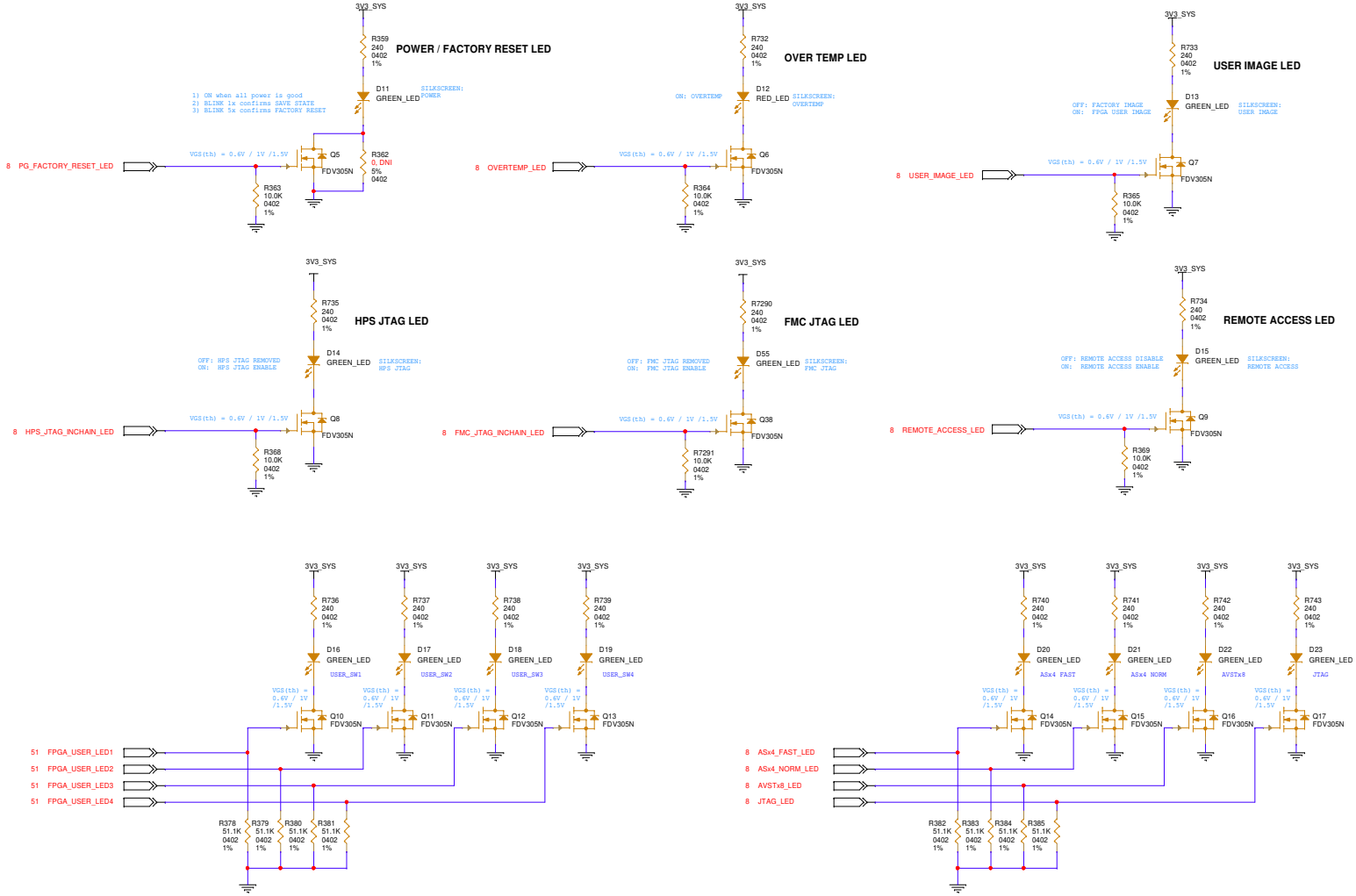

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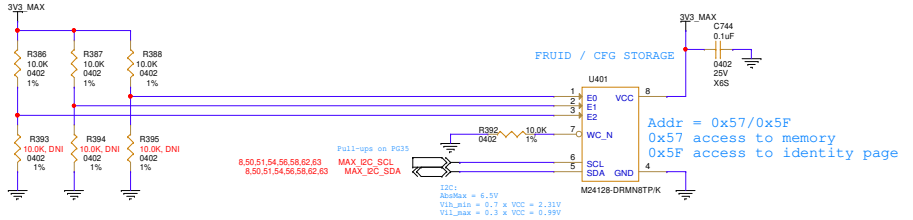

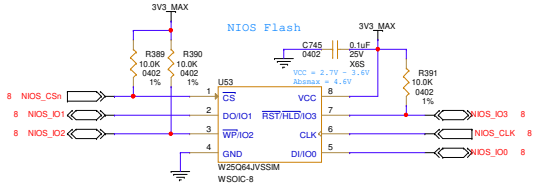

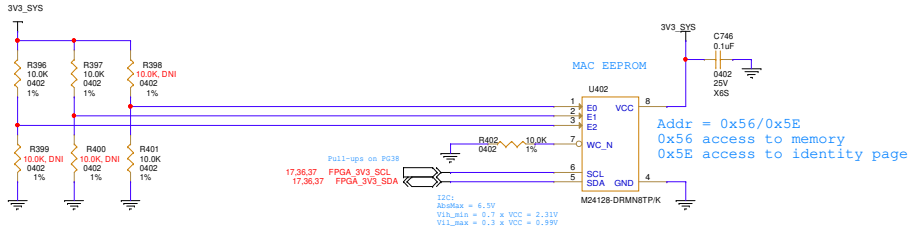

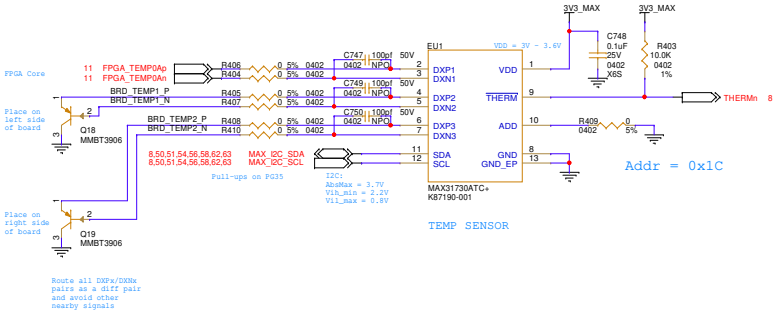

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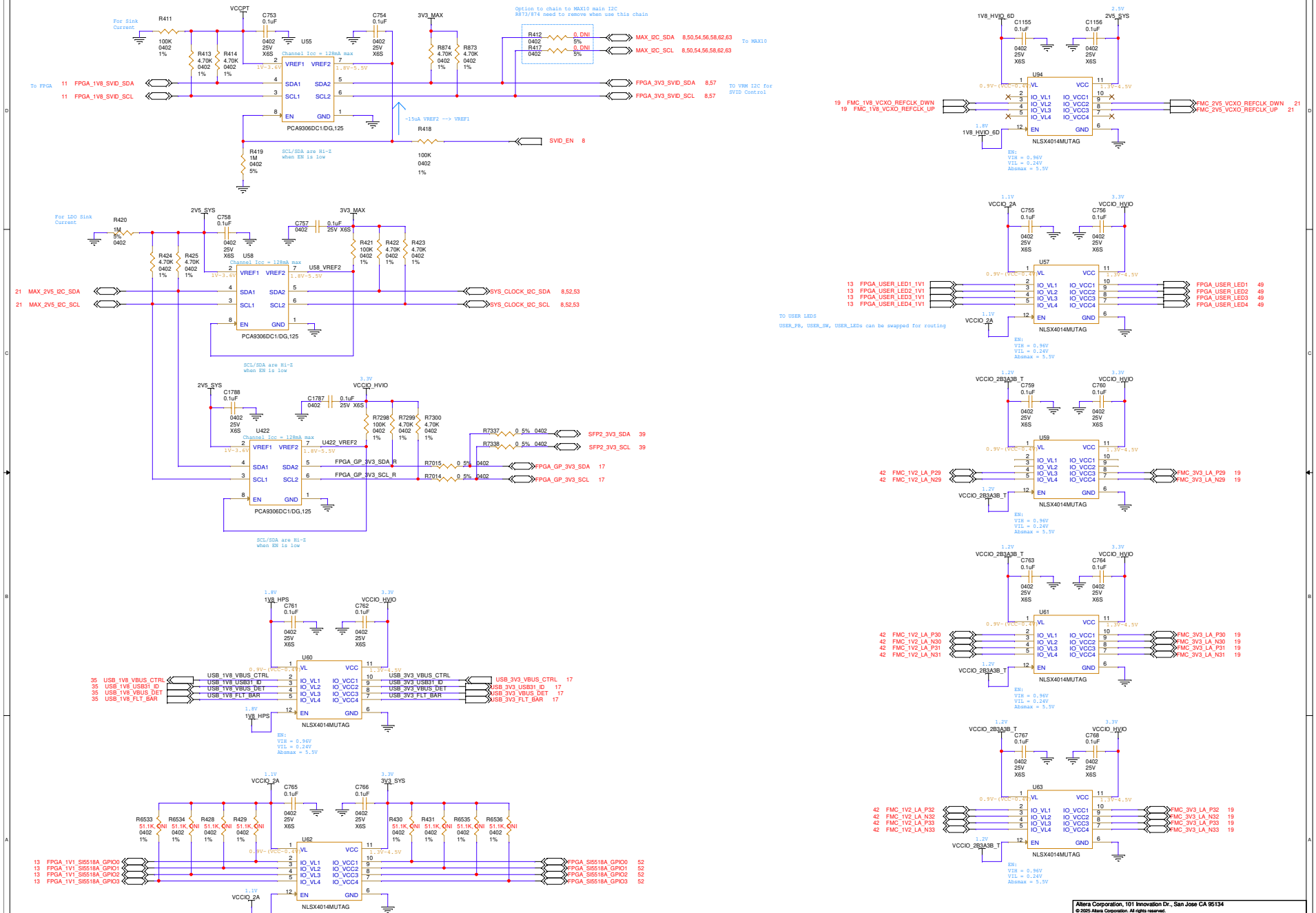

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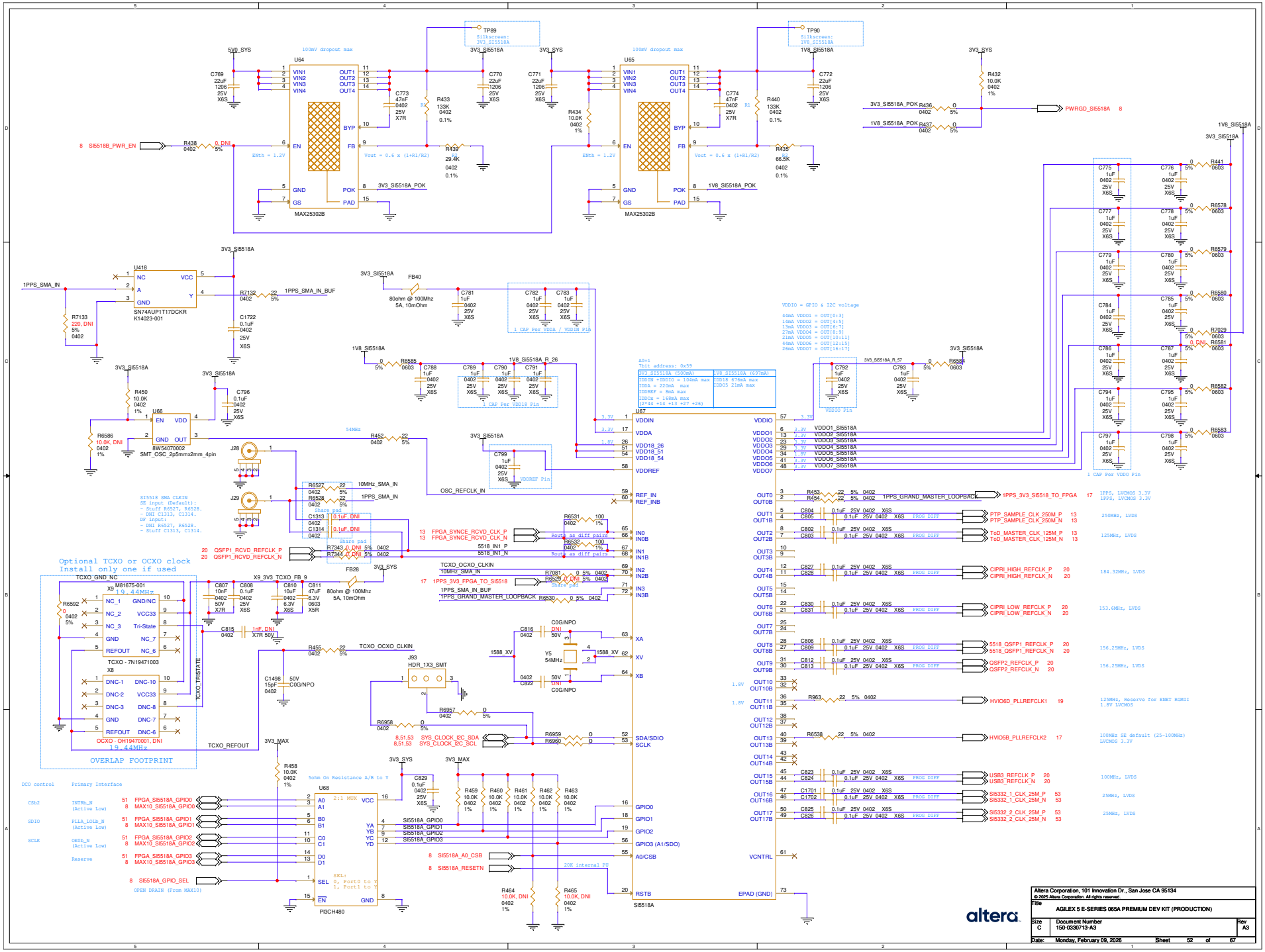
U64
MAX25302B
U65
MAX25302B
U418
SN74AUP1T17DCKR
K14023-001
U66
8WS4070002
SMT_OSC_2p5mmx2mm_4pin
U67
SI5518A
U68
PI3CH480
J28
J29
J93
HDR_1X3_SMT
X9
M81675-001
TCXO - 7N19471003
X8
OCXO - OH19470001, DNI
19.44MHz
OVERLAP FOOTPRINT
Optional TCXO or OCXO clock
Install only one if used
TP89
Silkscreen:
3V3_SI5518A
TP90
Silkscreen:
1V8_SI5518A
PWRGD_SI5518A
1PPS_SMA_IN
1PPS_SMA_IN_BUF
SI5518B_PWR_EN
3V3_SI5518A_POK
1V8_SI5518A_POK
OSC_REFCLK_IN
10MHz_SMA_IN
1PPS_SMA_IN
FPGA_SYNCE_RCVD_CLK_P
FPGA_SYNCE_RCVD_CLK_N
QSFP1_RCVD_REFCLK_P
QSFP1_RCVD_REFCLK_N
1PPS_3V3_FPGA_TO_SI5518
1PPS_GRAND_MASTER_LOOPBACK
TCXO_OCXO_CLKIN
TCXO_REFOUT
TCXO_TRISTATE
SYS_CLOCK_I2C_SDA
SYS_CLOCK_I2C_SCL
SI5518A_GPIO0
SI5518A_GPIO1
SI5518A_GPIO2
SI5518A_GPIO3
SI5518A_A0_CSB
SI5518A_RESETN
SI5518A_GPIO_SEL
FPGA_SI5518A_GPIO0
MAX10_SI5518A_GPIO0
FPGA_SI5518A_GPIO1
MAX10_SI5518A_GPIO1
FPGA_SI5518A_GPIO2
MAX10_SI5518A_GPIO2
FPGA_SI5518A_GPIO3
MAX10_SI5518A_GPIO3
HVIO6D_PLLREFCLK1
HVIO5B_PLLREFCLK2
1PPS_3V3_SI5518_TO_FPGA
PTP_SAMPLE_CLK_250M_P
PTP_SAMPLE_CLK_250M_N
ToD_MASTER_CLK_125M_P
ToD_MASTER_CLK_125M_N
CIPRI_HIGH_REFCLK_P
CIPRI_HIGH_REFCLK_N
CIPRI_LOW_REFCLK_P
CIPRI_LOW_REFCLK_N
SI518_QSFP1_REFCLK_P
SI518_QSFP1_REFCLK_N
QSFP2_REFCLK_P
QSFP2_REFCLK_N
USB3_REFCLK_P
USB3_REFCLK_N
SI5332_1_CLK_25M_P
SI5332_1_CLK_25M_N
SI5332_2_CLK_25M_P
SI5332_2_CLK_25M_N
VDDIO = GPIO & I2C voltage
1 CAP Per VDDA / VDDIN Pin
1 CAP Per VDD18 Pin
1 CAP Per VDDO Pin
VDDREF Pin
VDDIO Pin
Share pad
Route as diff pairs
PROG DIFF
OPEN DRAIN (From MAX10)
20K internal PU
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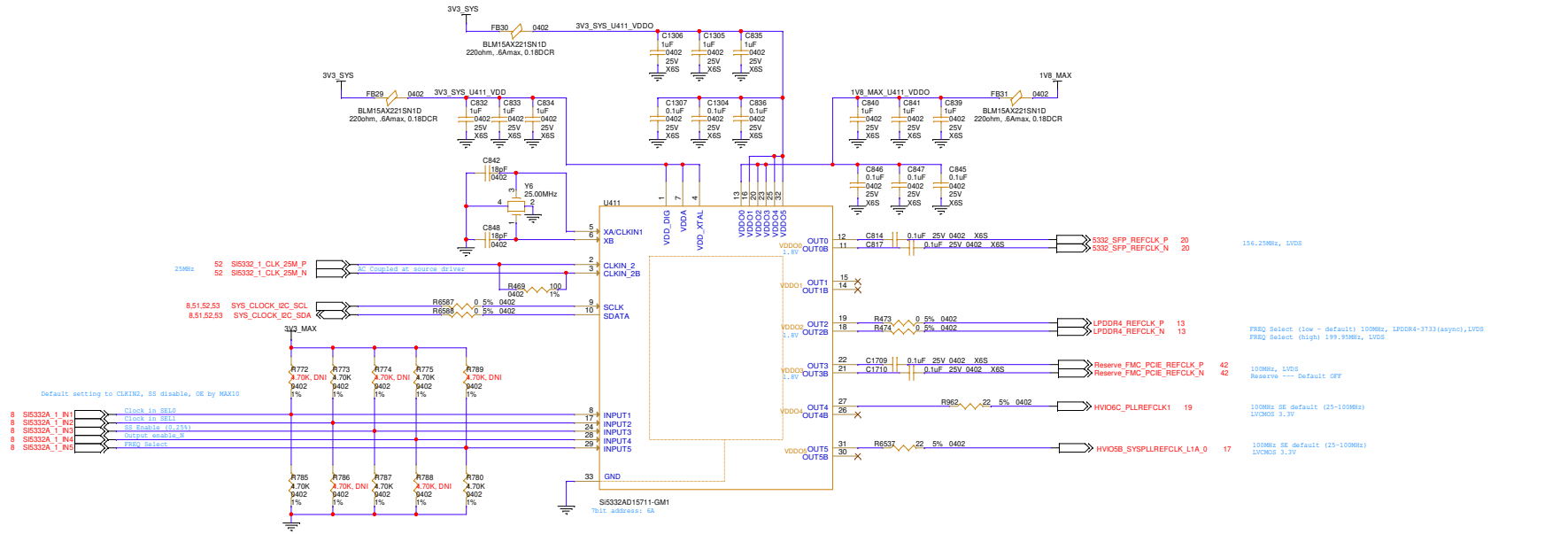

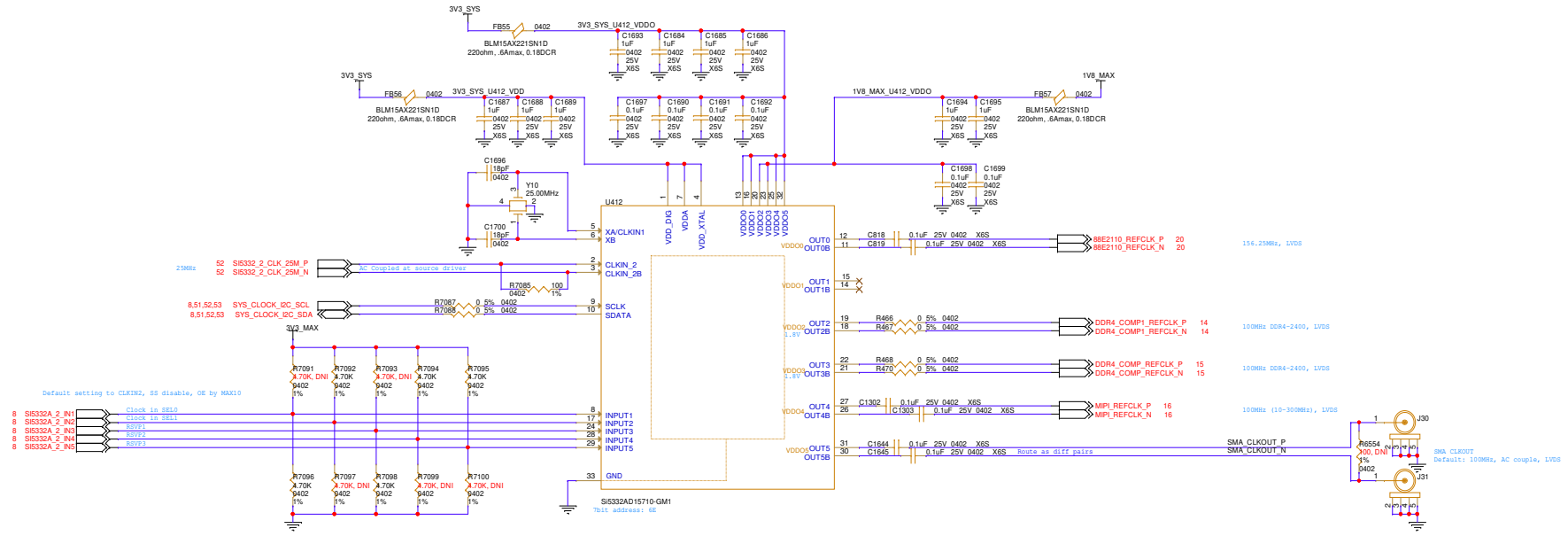

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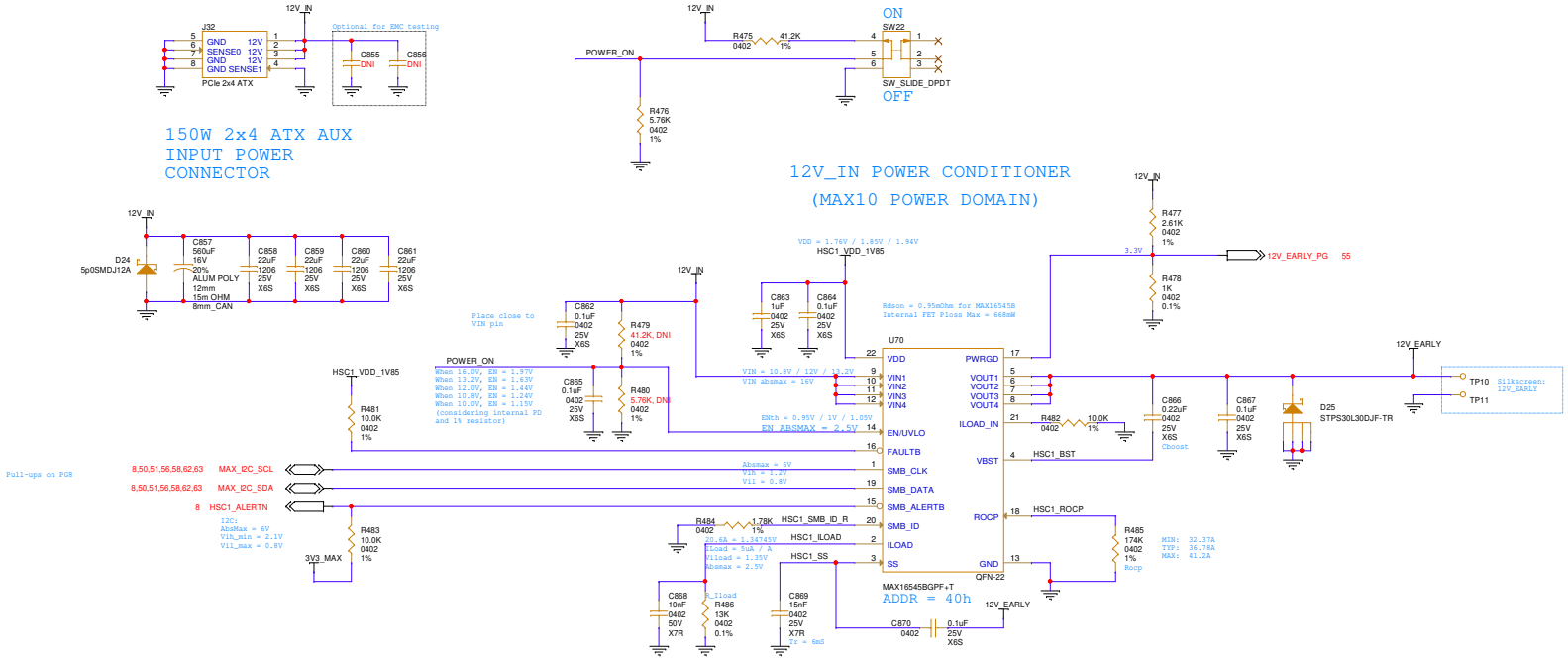
Power On Switch



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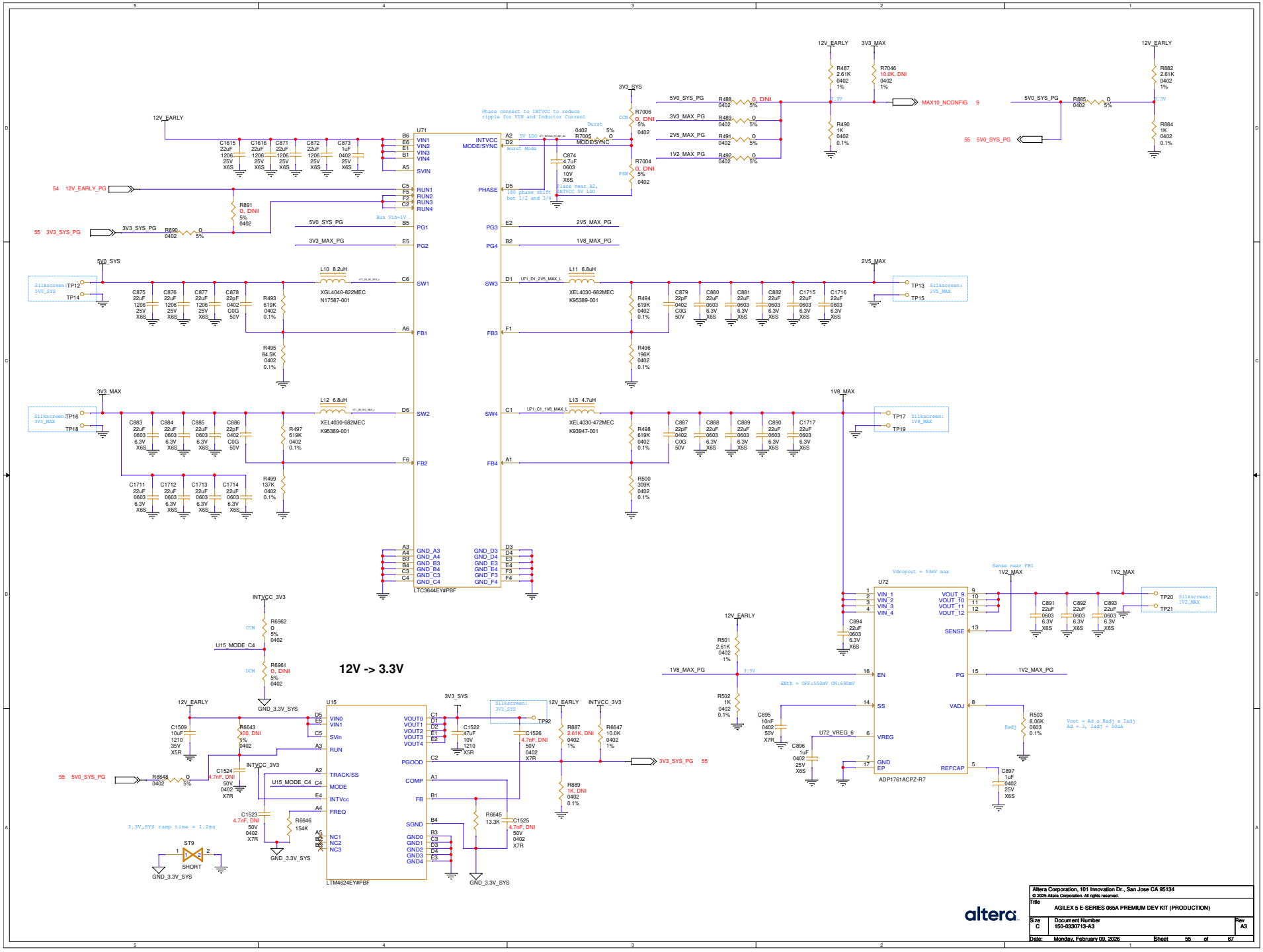

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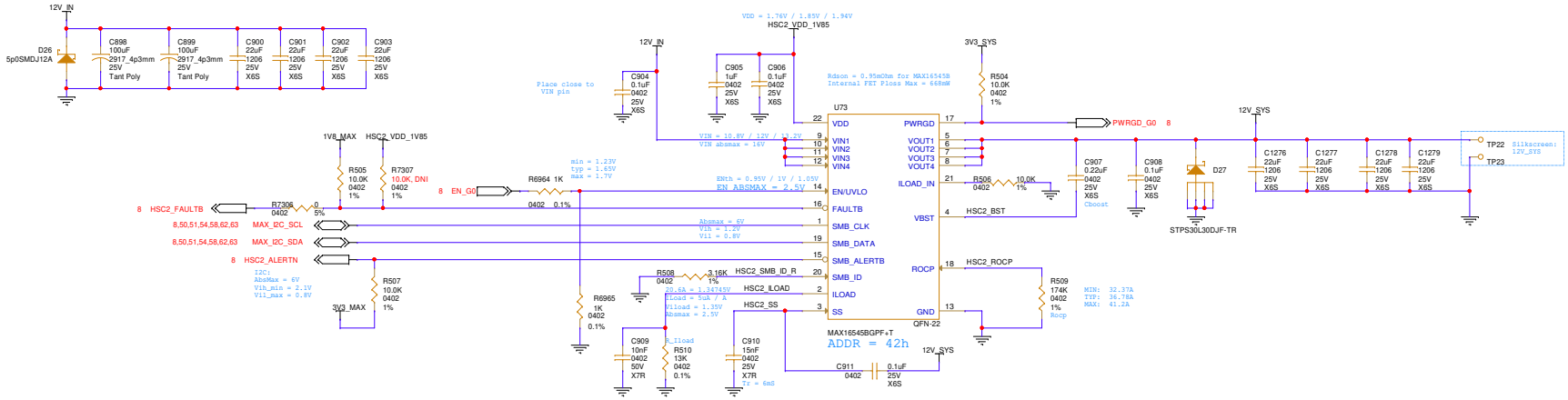

12V_SYS POWER CONDITIONER
(FPGA POWER DOMAIN)

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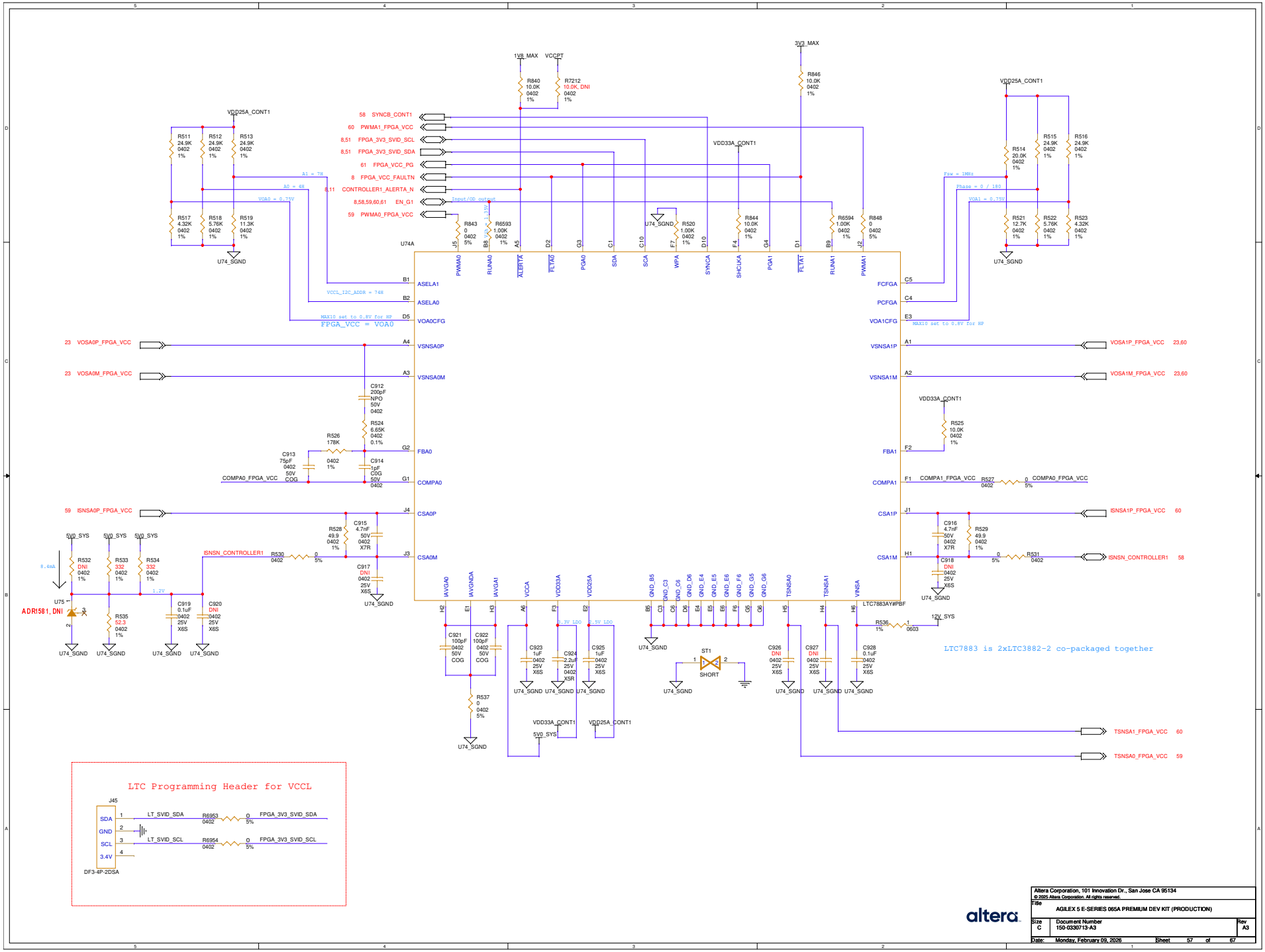

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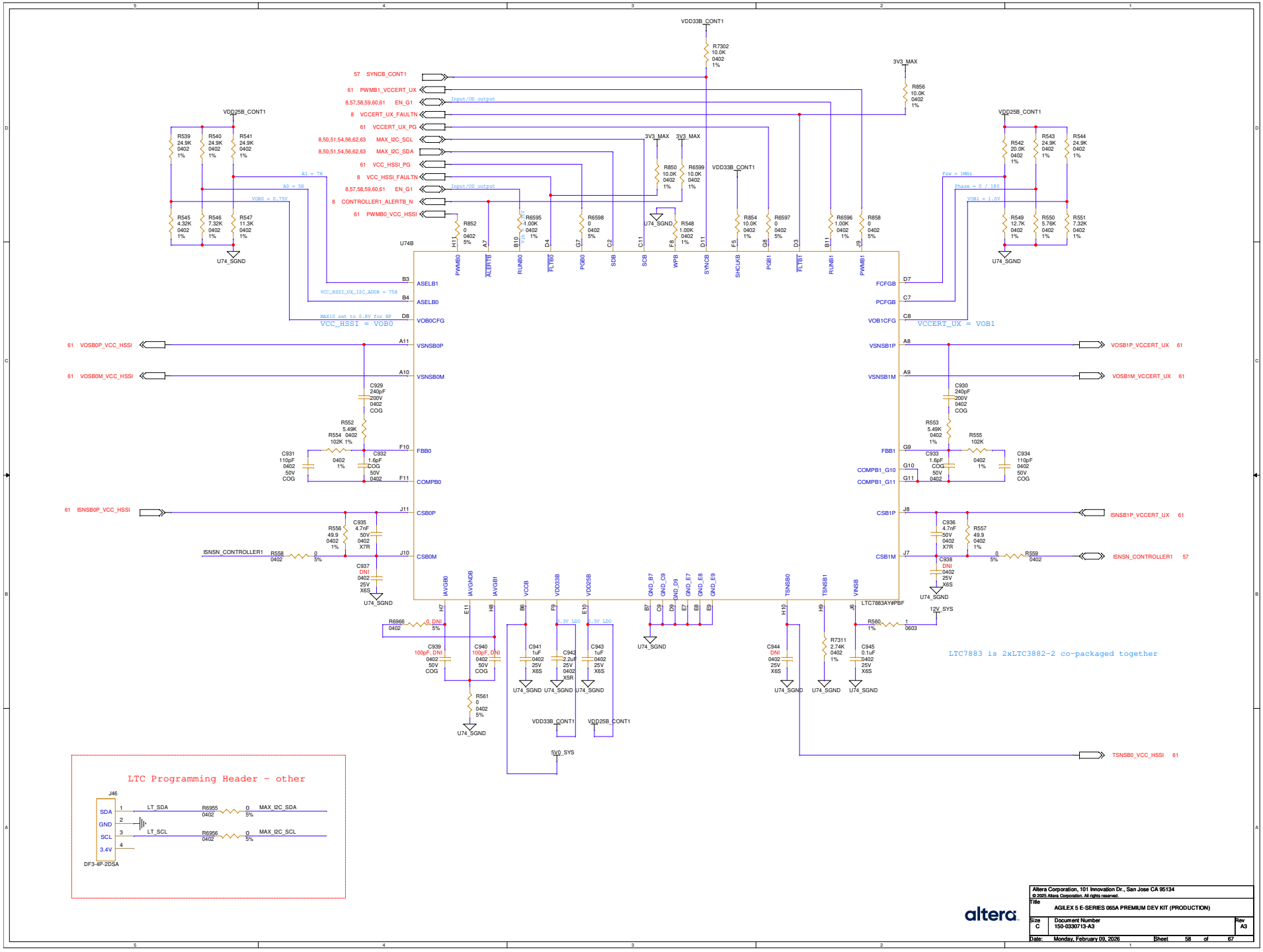

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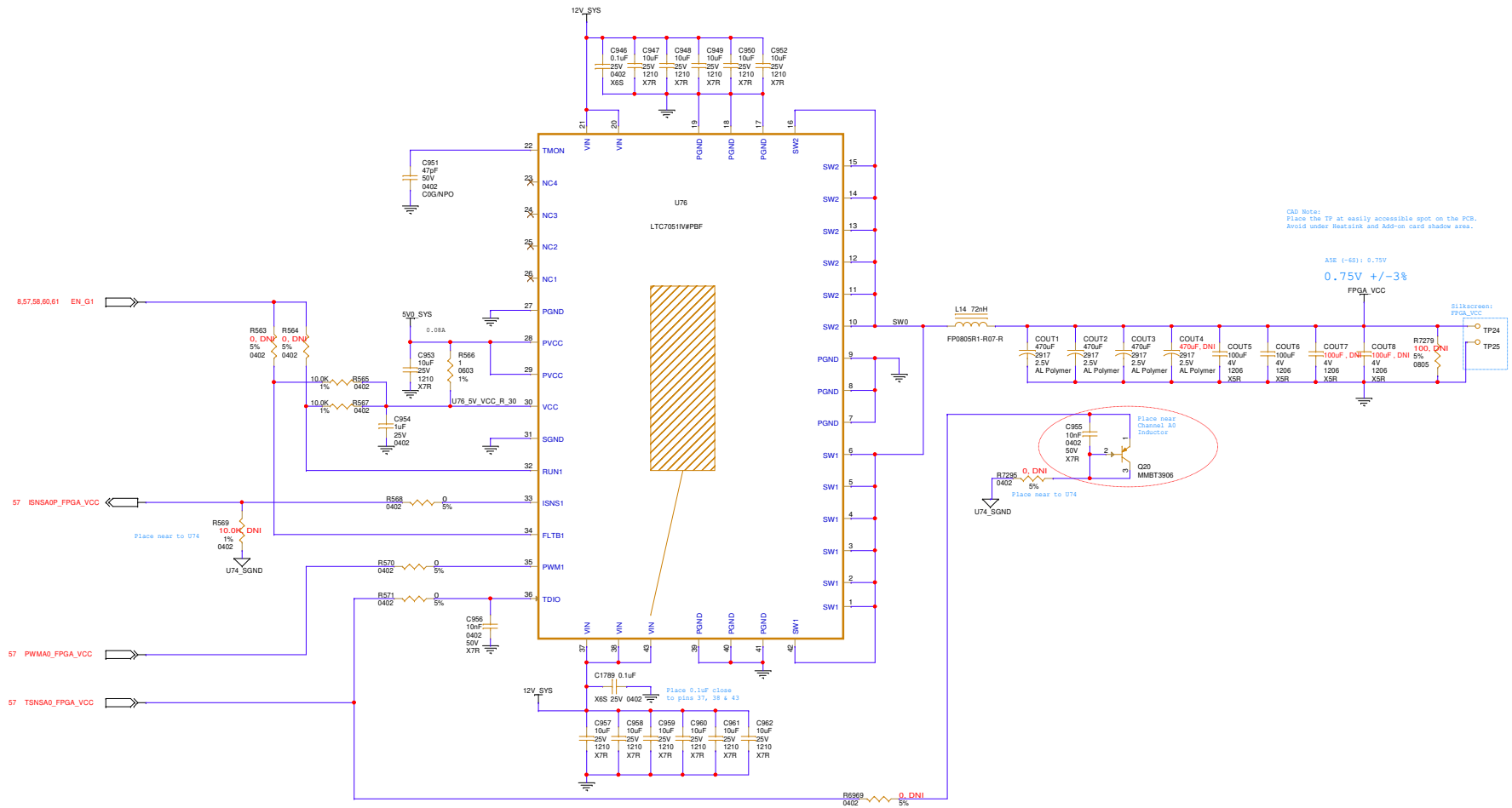

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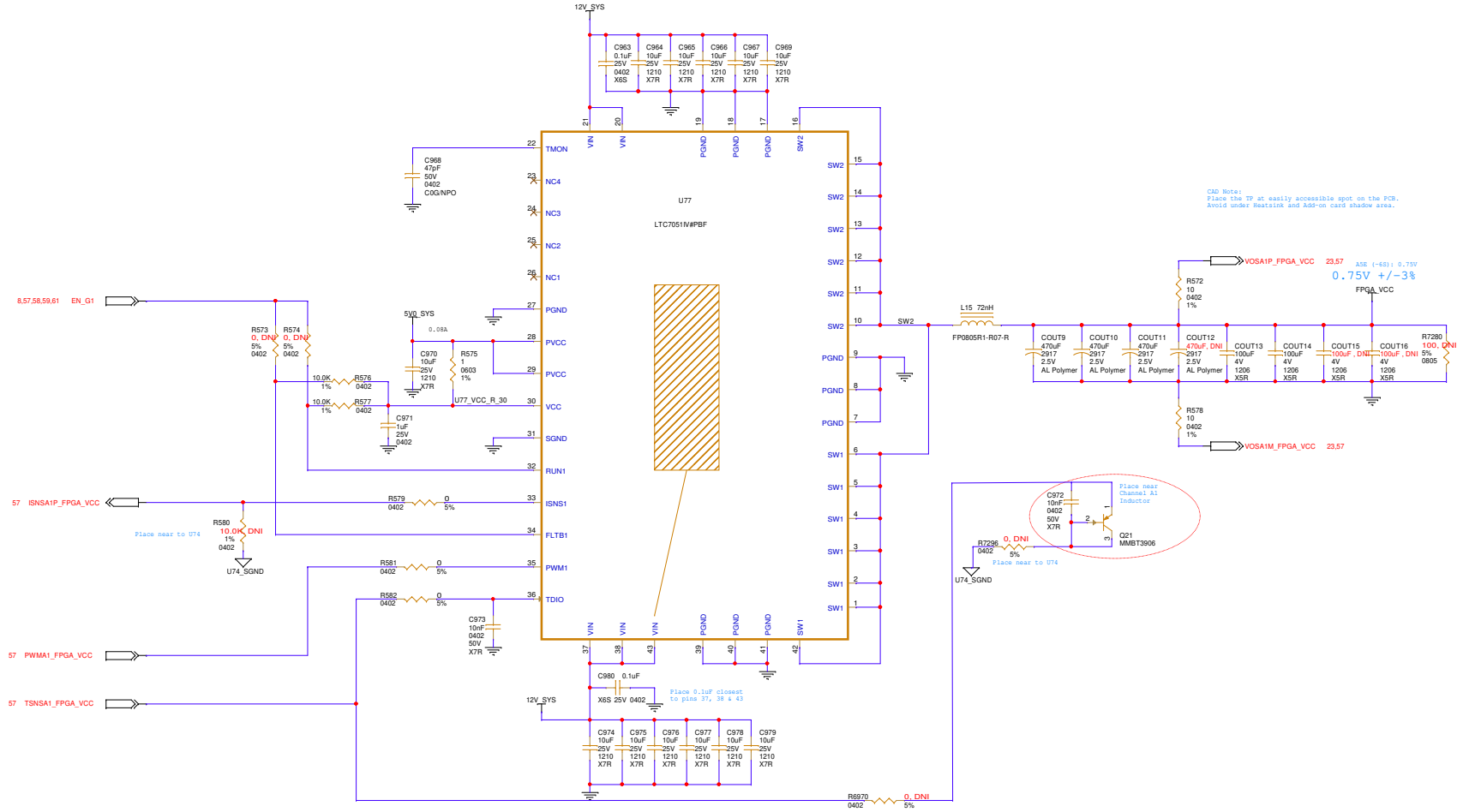

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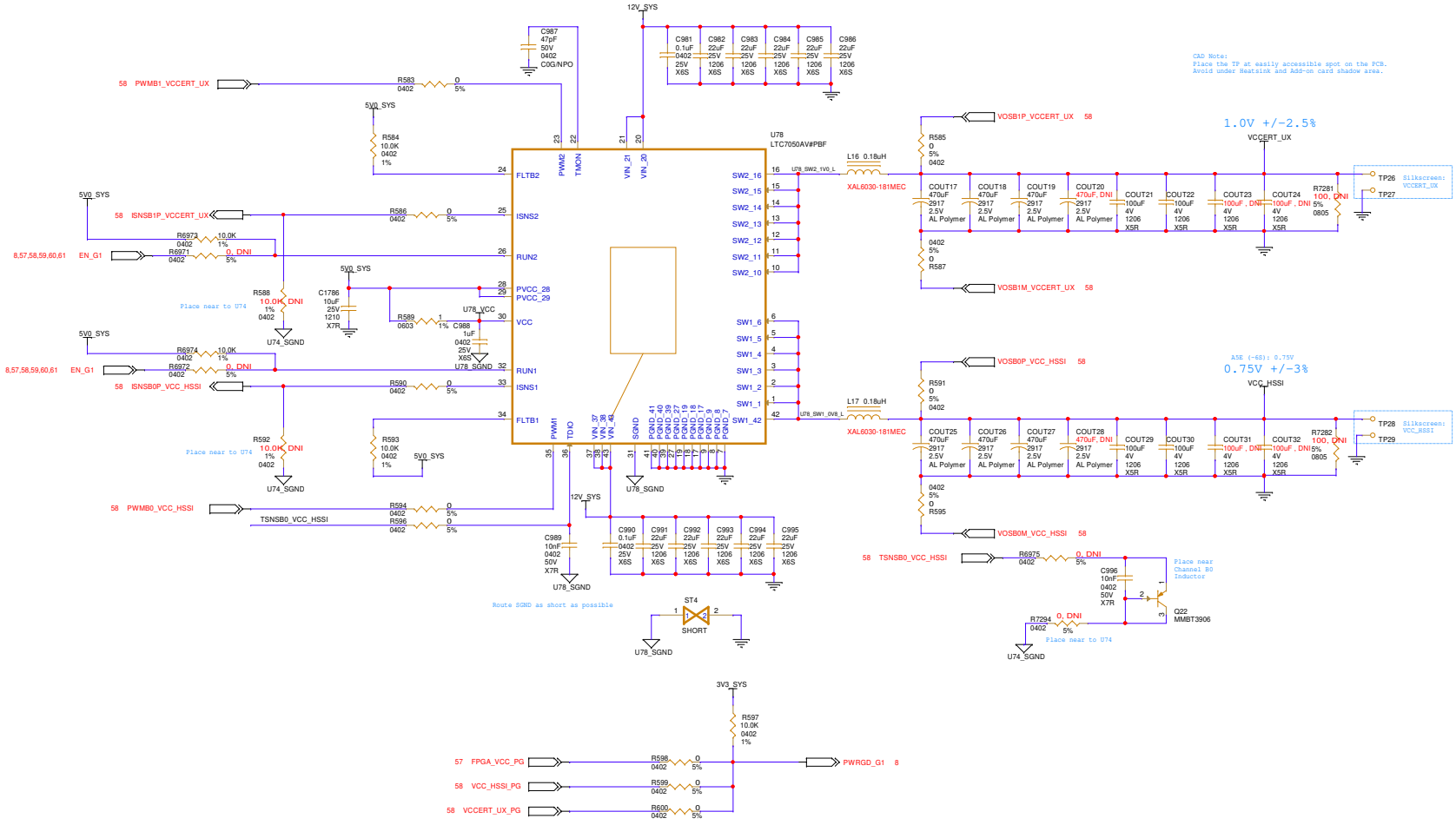

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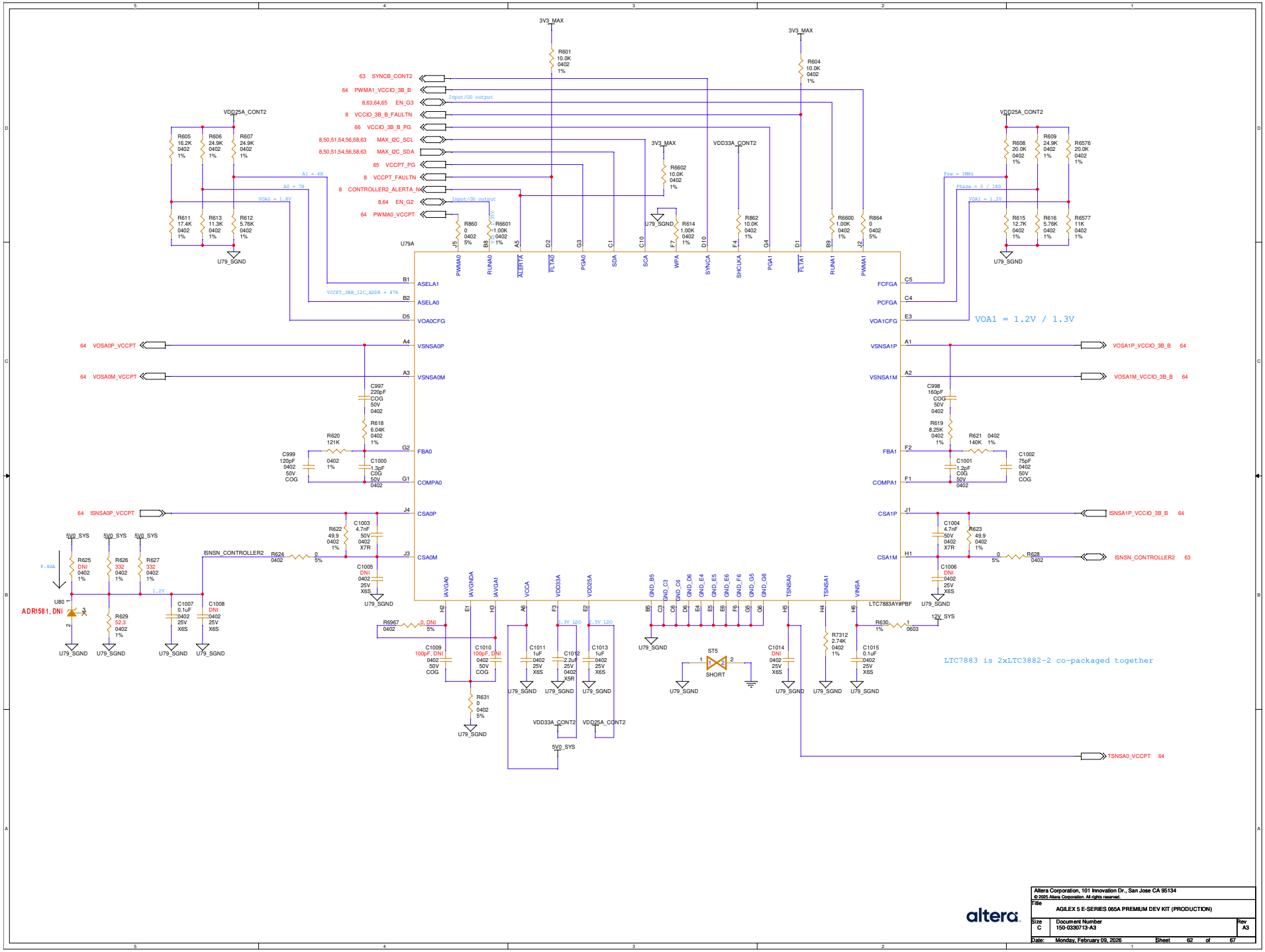

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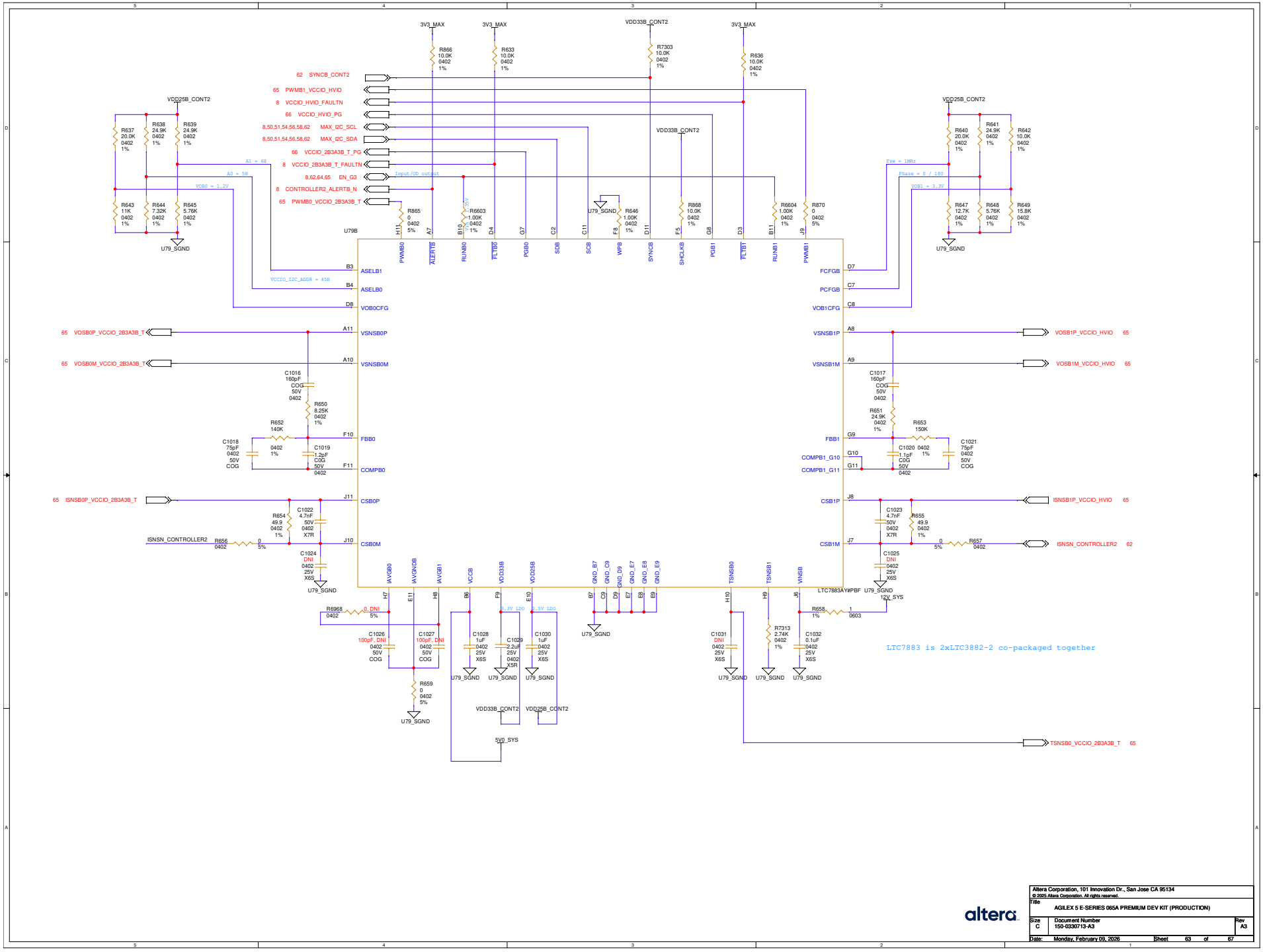

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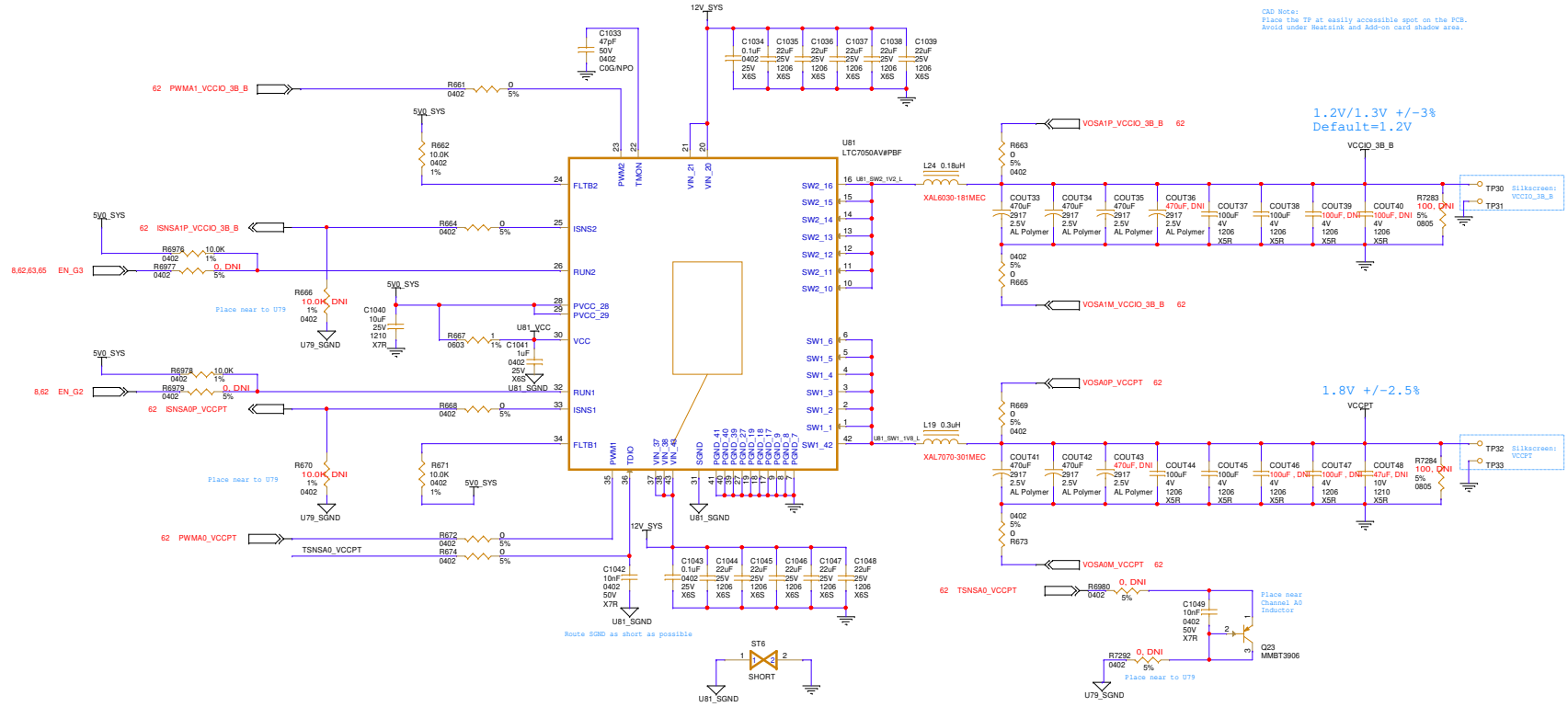

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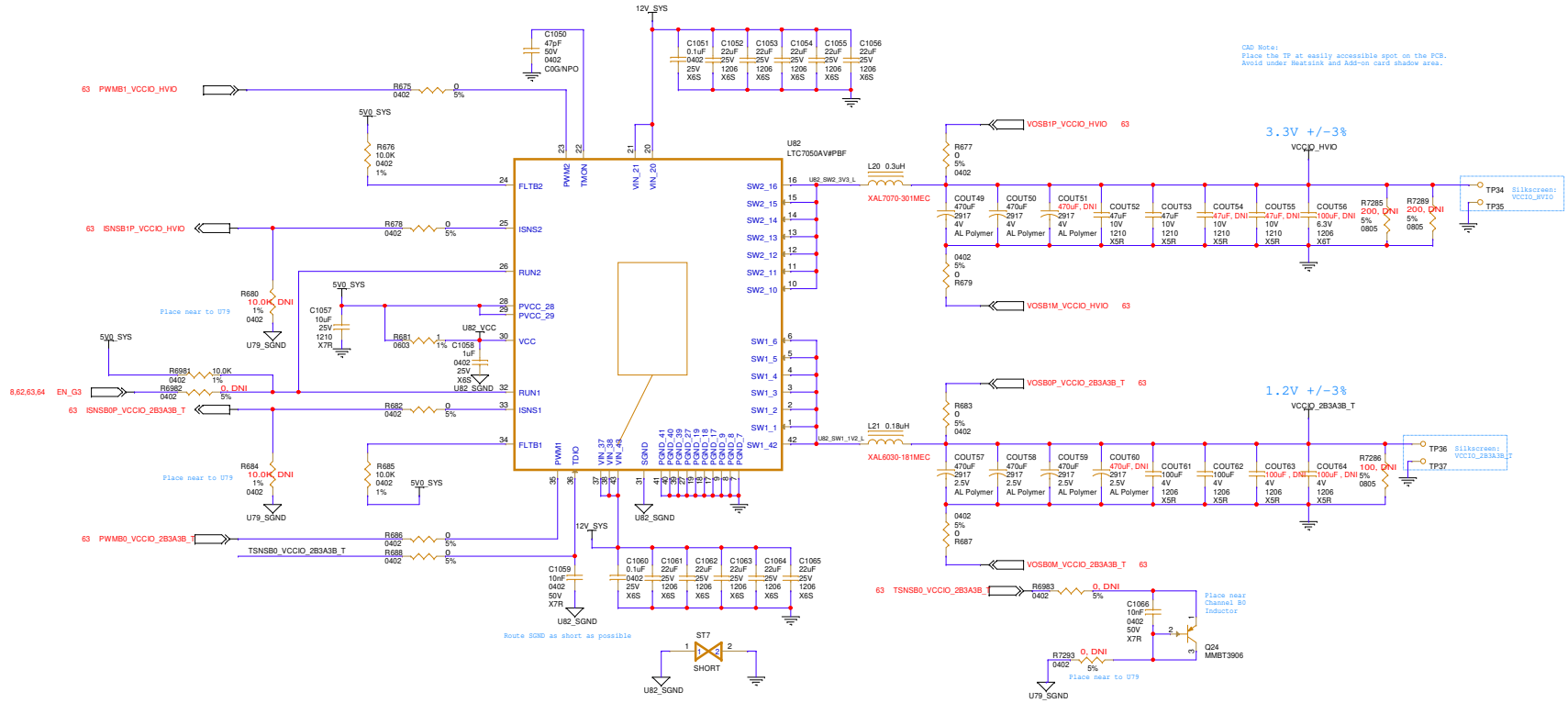

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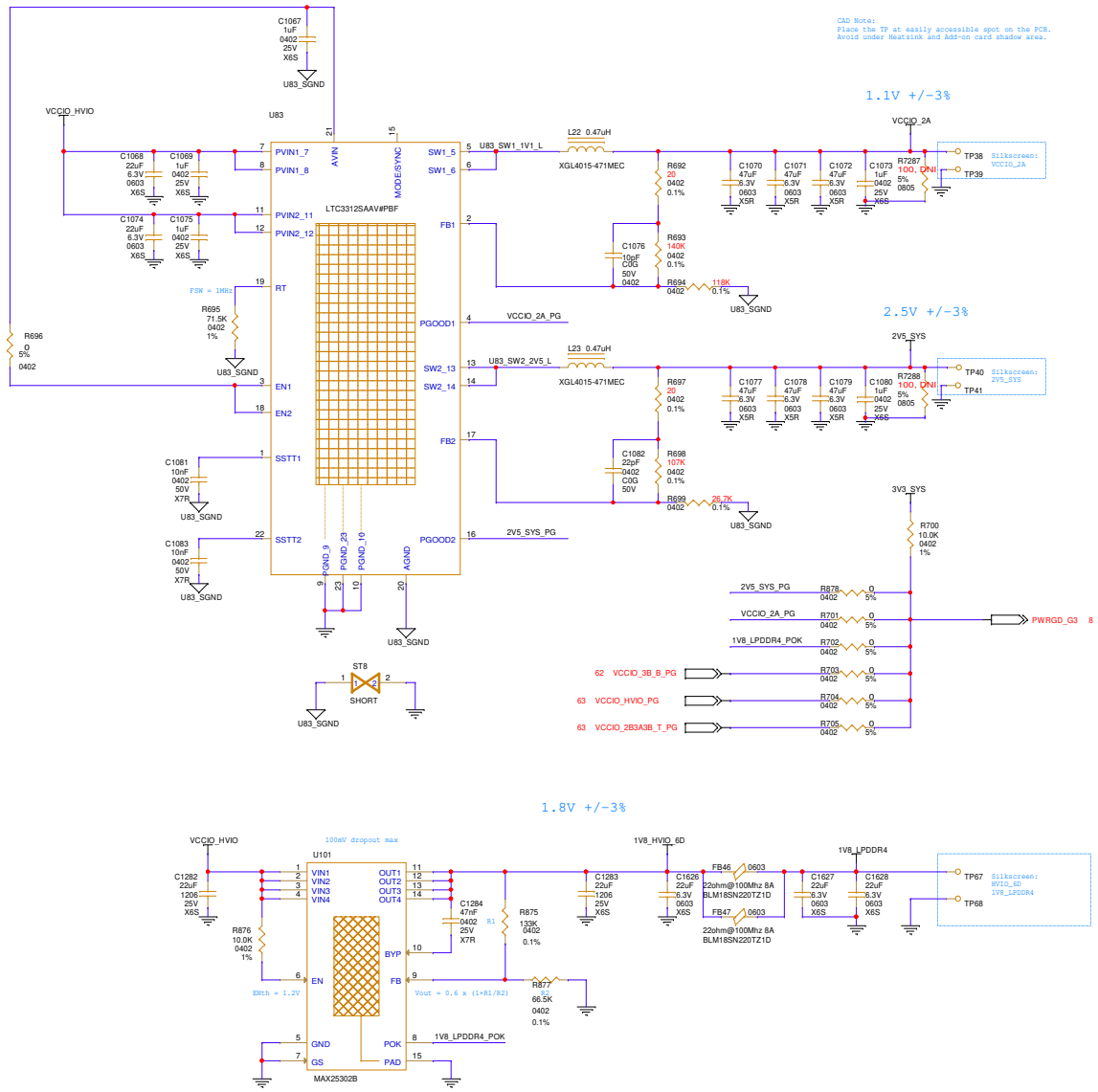

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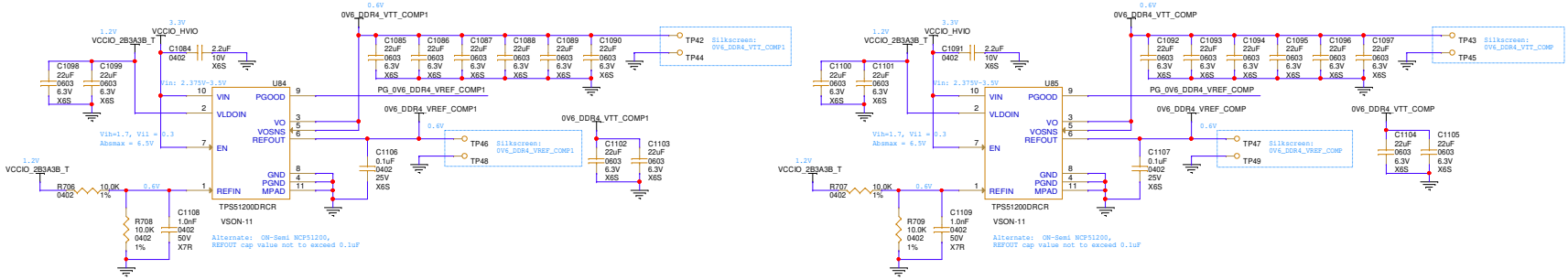
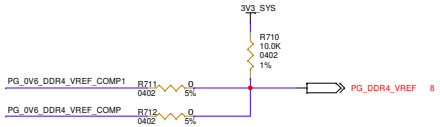
CAD Note:
Place the TP at easily accessible spot on the PCB.
Avoid under Heatsink and Add-on card shadow area.





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